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```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity lcd is
    Port ( clk,reset : in std_logic;
          RS,EN,RW : out std_logic;
          data : out std_logic_vector(7 downto 0));
end lcd;
architecture Behavioral of lcd is
    type state_type is (s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,
                        s12,s13,s14,s15,s16,s17,s18,s19,s20,s21,s22,s23);
    signal state:state_type;
    SIGNAL count:std_logic_vector(22 downto 0);
    SIGNAL clk1:std_logic;
begin
    process(Clk,Reset)
    begin
        if(Clk' event AND Clk='1')then
            count<=count+"0001";
        end if;
        clk1<=count(20);
    end process;
    RW<='0';
    process(clk1, reset)
    begin
        if reset = '1' then
            state <= s0;
        elsif rising_edge(clk1) then
            if state = s0 then
                state <= s1;
                RS<='0'; -- Write commands to LCD.
                EN <= '1';
                data <= "00110000"; -- Function set for 8 bit interface, 1 line mode
                and 5x7 dot matrix.
            end if;
            if state = s1 then
                state <= s2;
                EN <= '0';
            end if;
            if state = s2 then
                state <= s3;
                EN <= '1';
                data <= "00001111"; -- Display cursor and blinking ON.
            end if;
            if state = s3 then
                state <= s4;
                EN <= '0';
            end if;
```

```

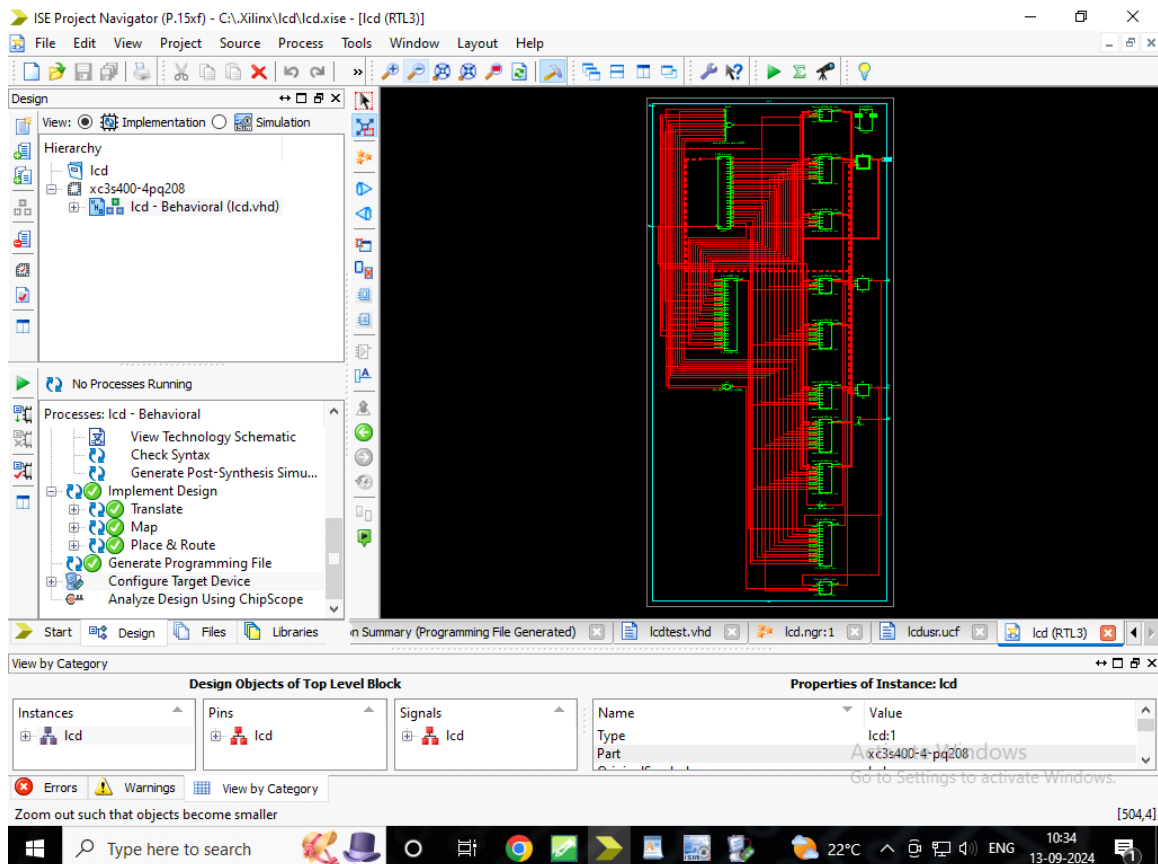
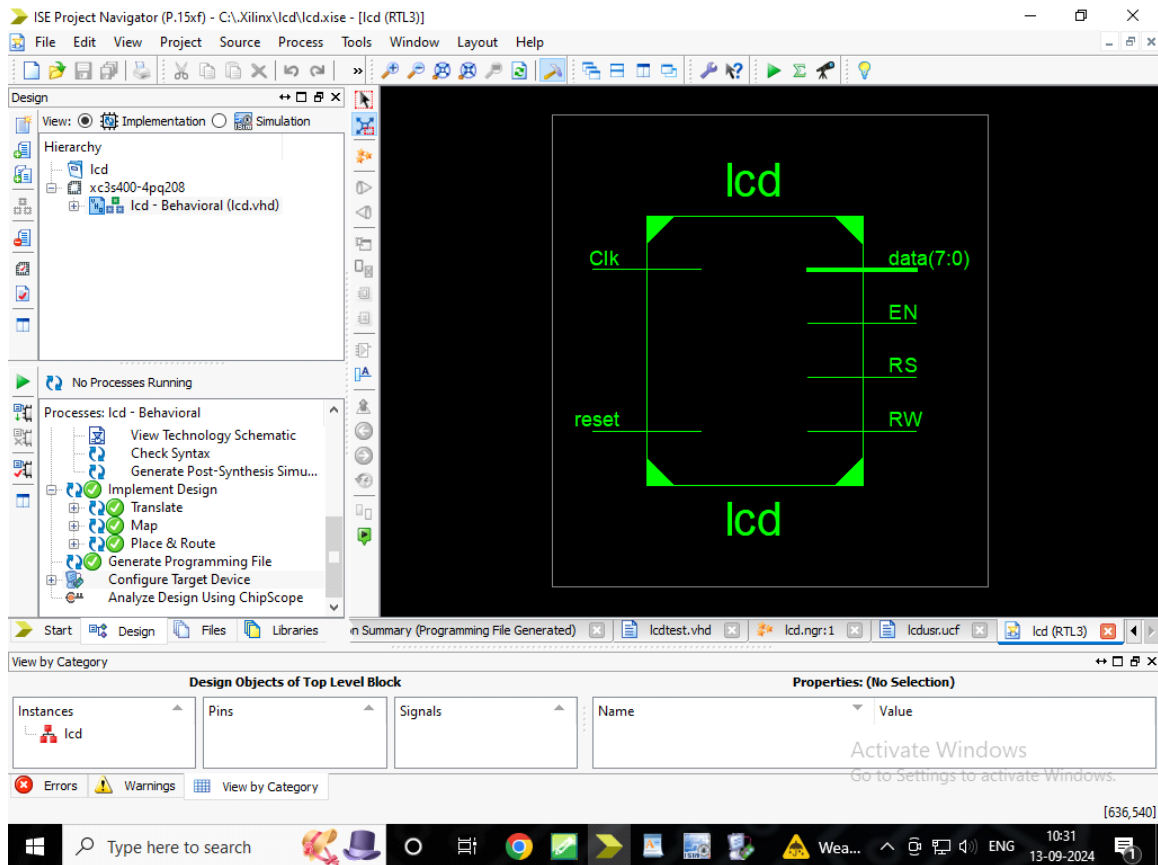
if state = s4 then
    state <= s5;
    EN <= '1';
    data <= "00000001";    -- Clear display.
end if;
if state = s5 then
    state <= s6;
    EN <= '0';
end if;
if state = s6 then
    state <= s7;
    EN <= '1';
    data <= "10000100"; -- Display address.
end if;
if state = s7 then
    state <= s8;
    EN <= '0';
end if;
if state = s8 then
    RS <= '1'; -- Write data to LCD.
    state <= s9;
    EN <= '1';
    data <= "00101010"; --(*)
end if;
if state = s9 then
    state <= s10;
    EN <= '0';
end if;
if state = s10 then
    state <= s11;
    EN <= '1';
    data <= "01010011"; --S
end if;
if state = s11 then
    state <= s12;
    EN <= '0';
end if;
if state = s12 then
    state <= s13;
    EN <= '1';
    data <= "01001011"; --K
end if;
if state = s13 then
    state <= s14;
    EN <= '0';
end if;
if state = s14 then
    state <= s15;
    EN <= '1';
    data <= "01001110"; --N
end if;

```

```

        if state = s15 then
            state <= s16;
            EN <= '0';
        end if;
        if state = s16 then
            state <= s17;
            EN <= '1';
            data <= "01000011"; --C
        end if;
        if state = s17 then
            state <= s18;
            EN <= '0';
        end if;
        if state = s18 then
            state <= s19;
            EN <= '1';
            data <= "01001111"; --O
        end if;
        if state = s19 then
            state <= s20;
            EN <= '0';
        end if;
        if state = s20 then
            state <= s21;
            EN <= '1';
            data <= "01000101"; --E
        end if;
        if state = s21 then
            state <= s22;
            EN <= '0';
        end if;
        if state = s22 then
            state <= s23;
            EN <= '1';
            data <= "00101010"; --(*)
        end if;
        if state = s23 then
            EN <= '0';
        end if;
    end if;
end process;
end Behavioral;

```



```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY lcdtest IS
END lcdtest;

ARCHITECTURE behavior OF lcdtest IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT lcd
    PORT(
        clk1 : IN std_logic;
        reset : IN std_logic;
        RS : OUT std_logic;
        EN : OUT std_logic;
        RW : OUT std_logic;
        data : OUT std_logic_vector(7 downto 0)
    );
    END COMPONENT;

    --Inputs
    signal clk1 : std_logic := '0';
    signal reset : std_logic := '0';

    --Outputs
    signal RS : std_logic;
    signal EN : std_logic;
    signal RW : std_logic;
    signal data : std_logic_vector(7 downto 0);

    -- Clock period definitions
    constant clk1_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: lcd PORT MAP (
        clk1 => clk1,
        reset => reset,
        RS => RS,
        EN => EN,
        RW => RW,
        data => data
    );

    -- Clock process definitions

```

```

clk1_process :process
begin
    clk1 <= '0';
    wait for clk1_period/2;
    clk1 <= '1';
    wait for clk1_period/2;
end process;

```

```

-- Stimulus process
stim_proc: process
begin
    -- hold reset state for 100 ns.

```

```

        reset<='0';

```

```

    wait for clk1_period*10;

```

```

    -- insert stimulus here

```

```

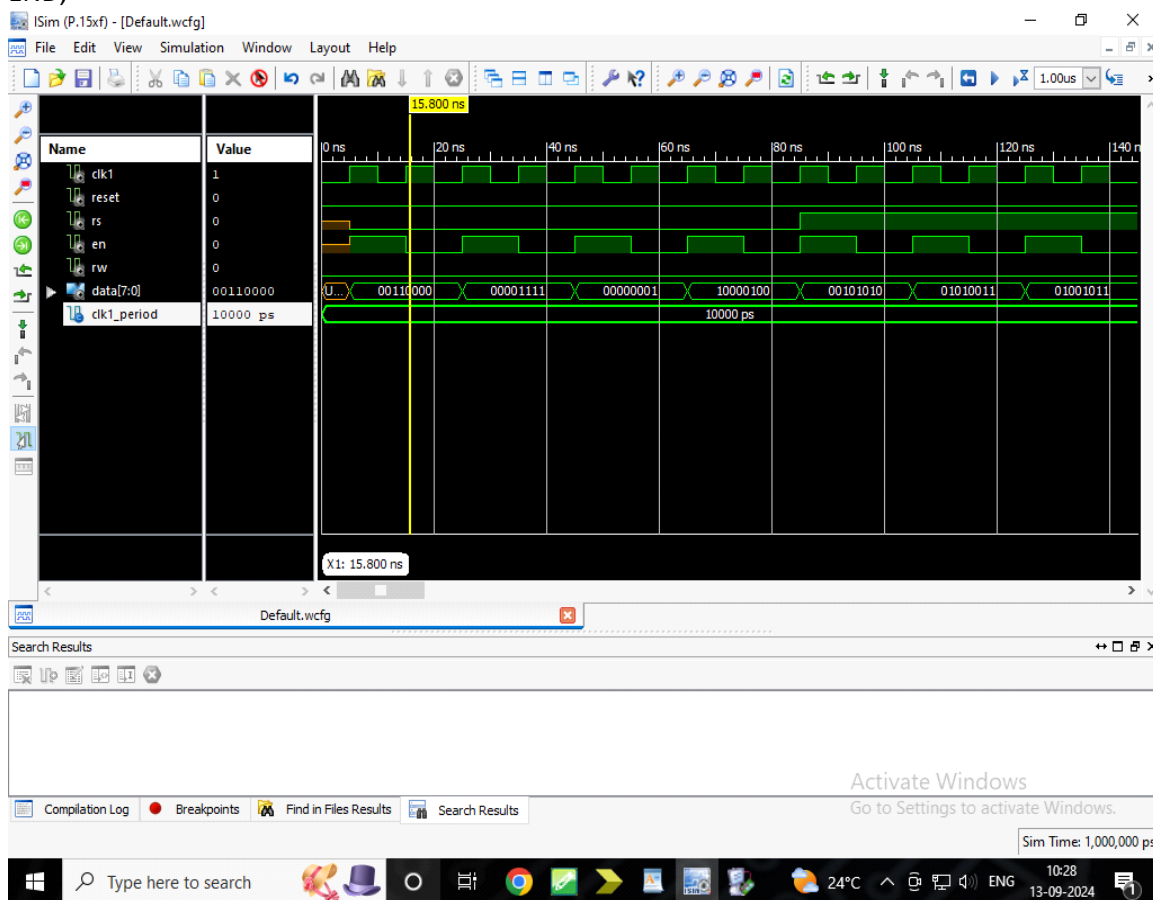
    wait;
end process;

```

```

END;

```



NET data(0) LOC =P62;  
NET data(1) LOC =P63;  
NET data(2) LOC =P64;  
NET data(3) LOC =P65;  
NET data(4) LOC =P67;  
NET data(5) LOC =P68;  
NET data(6) LOC =P71;  
NET data(7) LOC =P72;  
NET Clk LOC =P183;  
NET reset LOC =P102;  
NET RS LOC =P57;  
NET EN LOC =P61;  
NET RW LOC =P58;

Release 14.1 - xst P.15xf (nt64)  
Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved.  
--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs  
Total CPU time to Xst completion: 0.10 secs

--> Parameter xsthdprdir set to xst

Total REAL time to Xst completion: 0.00 secs  
Total CPU time to Xst completion: 0.10 secs

--> Reading design: lcd.prj

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```
=====
*           Synthesis Options Summary           *
=====
```

---- Source Parameters

Input File Name : "lcd.prj"  
Input Format : mixed  
Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "lcd"  
Output Format : NGC  
Target Device : xc3s400-4-pq208

---- Source Options

Top Module Name : lcd  
Automatic FSM Extraction : YES  
FSM Encoding Algorithm : Auto  
Safe Implementation : No  
FSM Style : LUT  
RAM Extraction : Yes  
RAM Style : Auto  
ROM Extraction : Yes  
Mux Style : Auto  
Decoder Extraction : YES  
Priority Encoder Extraction : Yes  
Shift Register Extraction : YES  
Logical Shifter Extraction : YES  
XOR Collapsing : YES  
ROM Style : Auto  
Mux Extraction : Yes  
Resource Sharing : YES  
Asynchronous To Synchronous : NO  
Multiplier Style : Auto  
Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES  
Global Maximum Fanout : 500  
Add Generic Clock Buffer(BUFG) : 8  
Register Duplication : YES  
Slice Packing : YES  
Optimize Instantiated Primitives : NO  
Use Clock Enable : Yes  
Use Synchronous Set : Yes  
Use Synchronous Reset : Yes  
Pack IO Registers into IOBs : Auto  
Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed  
Optimization Effort : 1  
Keep Hierarchy : No  
Netlist Hierarchy : As\_Optimized  
RTL Output : Yes



Global Optimization : AllClockNets  
Read Cores : YES  
Write Timing Constraints : NO  
Cross Clock Analysis : NO  
Hierarchy Separator : /  
Bus Delimiter : <>  
Case Specifier : Maintain  
Slice Utilization Ratio : 100  
BRAM Utilization Ratio : 100  
Verilog 2001 : YES  
Auto BRAM Packing : NO  
Slice Utilization Ratio Delta : 5

=====

=====

\* HDL Compilation \*

=====

Compiling vhdl file "C:/Xilinx/lcd/lcd.vhd" in Library work.  
Architecture behavioral of Entity lcd is up to date.

=====

\* Design Hierarchy Analysis \*

=====

Analyzing hierarchy for entity <lcd> in library <work> (architecture <behavioral>).

=====

\* HDL Analysis \*

=====

Analyzing Entity <lcd> in library <work> (Architecture <behavioral>).

WARNING:Xst:819 - "C:/Xilinx/lcd/lcd.vhd" line 36: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<count>

Entity <lcd> analyzed. Unit <lcd> generated.

=====

\* HDL Synthesis \*

=====

Performing bidirectional port resolution...

Synthesizing Unit <lcd>.

Related source file is "C:/Xilinx/lcd/lcd.vhd".

Found finite state machine <FSM\_0> for signal <state>.

-----  
| States | 24 |

Transitions	24	
Inputs	0	
Outputs	24	
Clock	clk1	(rising_edge)
Reset	reset	(positive)
Reset type	asynchronous	
Reset State	s0	
Power Up State	s0	
Encoding	automatic	
Implementation	LUT	

Found 1-bit register for signal <RS>.  
Found 1-bit register for signal <EN>.  
Found 8-bit register for signal <data>.  
Found 23-bit up counter for signal <count>.  
Summary:  
inferred 1 Finite State Machine(s).  
inferred 1 Counter(s).  
inferred 10 D-type flip-flop(s).

Unit <lcd> synthesized.

### HDL Synthesis Report

#### Macro Statistics

```
# Counters          : 1
 23-bit up counter  : 1
# Registers         : 3
1-bit register      : 2
8-bit register      : 1
```

### \* Advanced HDL Synthesis \*

Analyzing FSM <FSM\_0> for best encoding.  
Optimizing FSM <state/FSM> on signal <state[1:24]> with one-hot encoding.

#### State | Encoding

```
s0 | 000000000000000000000001
s1 | 100000000000000000000000
s2 | 010000000000000000000000
s3 | 001000000000000000000000
s4 | 000100000000000000000000
s5 | 000010000000000000000000
s6 | 000001000000000000000000
s7 | 000000100000000000000000
```

s8 | 000000010000000000000000  
s9 | 000000001000000000000000  
s10 | 000000000100000000000000  
s11 | 000000000010000000000000  
s12 | 000000000001000000000000  
s13 | 000000000000100000000000  
s14 | 000000000000010000000000  
s15 | 000000000000001000000000  
s16 | 000000000000000100000000  
s17 | 000000000000000010000000  
s18 | 000000000000000001000000  
s19 | 000000000000000000100000  
s20 | 000000000000000000010000  
s21 | 000000000000000000001000  
s22 | 000000000000000000000100  
s23 | 000000000000000000000010

=====

## Advanced HDL Synthesis Report

### Macro Statistics

# FSMs	: 1
# Counters	: 1
23-bit up counter	: 1
# Registers	: 10
Flip-Flops	: 10

=====

### \* Low Level Synthesis \*

=====

WARNING:Xst:2677 - Node <count\_21> of sequential type is unconnected in block <lcd>.  
WARNING:Xst:2677 - Node <count\_22> of sequential type is unconnected in block <lcd>.

Optimizing unit <lcd> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block lcd, actual ratio is 1.

Final Macro Processing ...

=====

## Final Register Report

### Macro Statistics

# Registers	: 55
Flip-Flops	: 55

=====

\* Partition Report \*

=====

Partition Implementation Status

-----

No Partitions were found in this design.

-----

=====

\* Final Report \*

=====

Final Results

RTL Top Level Output File Name : lcd.ngr

Top Level Output File Name : lcd

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 13

Cell Usage :

# BELS : 92

# GND : 1

# INV : 2

# LUT1 : 20

# LUT2 : 1

# LUT2\_L : 3

# LUT3 : 3

# LUT3\_D : 1

# LUT4 : 14

# LUT4\_D : 1

# LUT4\_L : 4

# MUXCY : 20

# VCC : 1

# XORCY : 21

# FlipFlops/Latches : 55

# FD : 21

# FDC : 22

# FDCE : 1

# FDE : 10

# FDP : 1

# Clock Buffers : 2

# BUFG : 1

# BUFGP : 1

# IO Buffers : 12

# IBUF : 1  
# OBUF : 11

Device utilization summary:

Selected Device : 3s400pq208-4

Number of Slices: 35 out of 3584 0%  
Number of Slice Flip Flops: 55 out of 7168 0%  
Number of 4 input LUTs: 49 out of 7168 0%  
Number of IOs: 13  
Number of bonded IOBs: 13 out of 141 9%  
Number of GCLKs: 2 out of 8 25%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.  
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT  
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
count_201	BUFG	34
Clk	BUFGP	21

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
reset	IBUF	24

Timing Summary:

Speed Grade: -4

Minimum period: 6.071ns (Maximum Frequency: 164.717MHz)

Minimum input arrival time before clock: 4.921ns

Maximum output required time after clock: 7.241ns

Maximum combinational path delay: No path found

Timing Detail:

-----  
All values displayed in nanoseconds (ns)

=====

Timing constraint: Default period analysis for Clock 'count\_201'

Clock period: 6.071ns (frequency: 164.717MHz)

Total number of paths / destination ports: 193 / 33

-----

Delay: 6.071ns (Levels of Logic = 3)

Source: state\_FSM\_FFd4 (FF)

Destination: EN (FF)

Source Clock: count\_201 rising

Destination Clock: count\_201 rising

Data Path: state\_FSM\_FFd4 to EN

	Gate	Net			
Cell:in->out	fanout	Delay	Delay	Logical Name	(Net Name)
FDC:C->Q	3	0.720	1.246	state_FSM_FFd4	(state_FSM_FFd4)
LUT4:I0->O	1	0.551	1.140	EN_mux00009	(EN_mux00009)
LUT3_D:I0->O	8	0.551	1.109	data_or000023	(data_or00000)
LUT4:I3->O	1	0.551	0.000	data_mux0000<3>1	(data_mux0000<3>)
FDE:D		0.203		data_4	
-----					
Total		6.071ns (2.576ns logic, 3.495ns route)			
		(42.4% logic, 57.6% route)			

=====

Timing constraint: Default period analysis for Clock 'Clk'

Clock period: 5.170ns (frequency: 193.424MHz)

Total number of paths / destination ports: 231 / 21

-----

Delay: 5.170ns (Levels of Logic = 21)

Source: count\_1 (FF)

Destination: count\_20 (FF)

Source Clock: Clk rising

Destination Clock: Clk rising

Data Path: count\_1 to count\_20

	Gate	Net			
Cell:in->out	fanout	Delay	Delay	Logical Name	(Net Name)
FD:C->Q	1	0.720	1.140	count_1	(count_1)



Source: EN (FF)  
Destination: EN (PAD)  
Source Clock: count\_201 rising

Data Path: EN to EN

	Gate	Net			
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)	
-----					
FDE:C->Q	2	0.720	0.877	EN (EN_OBUF)	
OBUF:I->O		5.644		EN_OBUF (EN)	
-----					
Total		7.241ns (6.364ns logic, 0.877ns route)			
		(87.9% logic, 12.1% route)			

=====

Total REAL time to Xst completion: 4.00 secs  
Total CPU time to Xst completion: 3.89 secs

-->

Total memory usage is 4509380 kilobytes

Number of errors : 0 ( 0 filtered)  
Number of warnings : 3 ( 0 filtered)  
Number of infos : 0 ( 0 filtered)