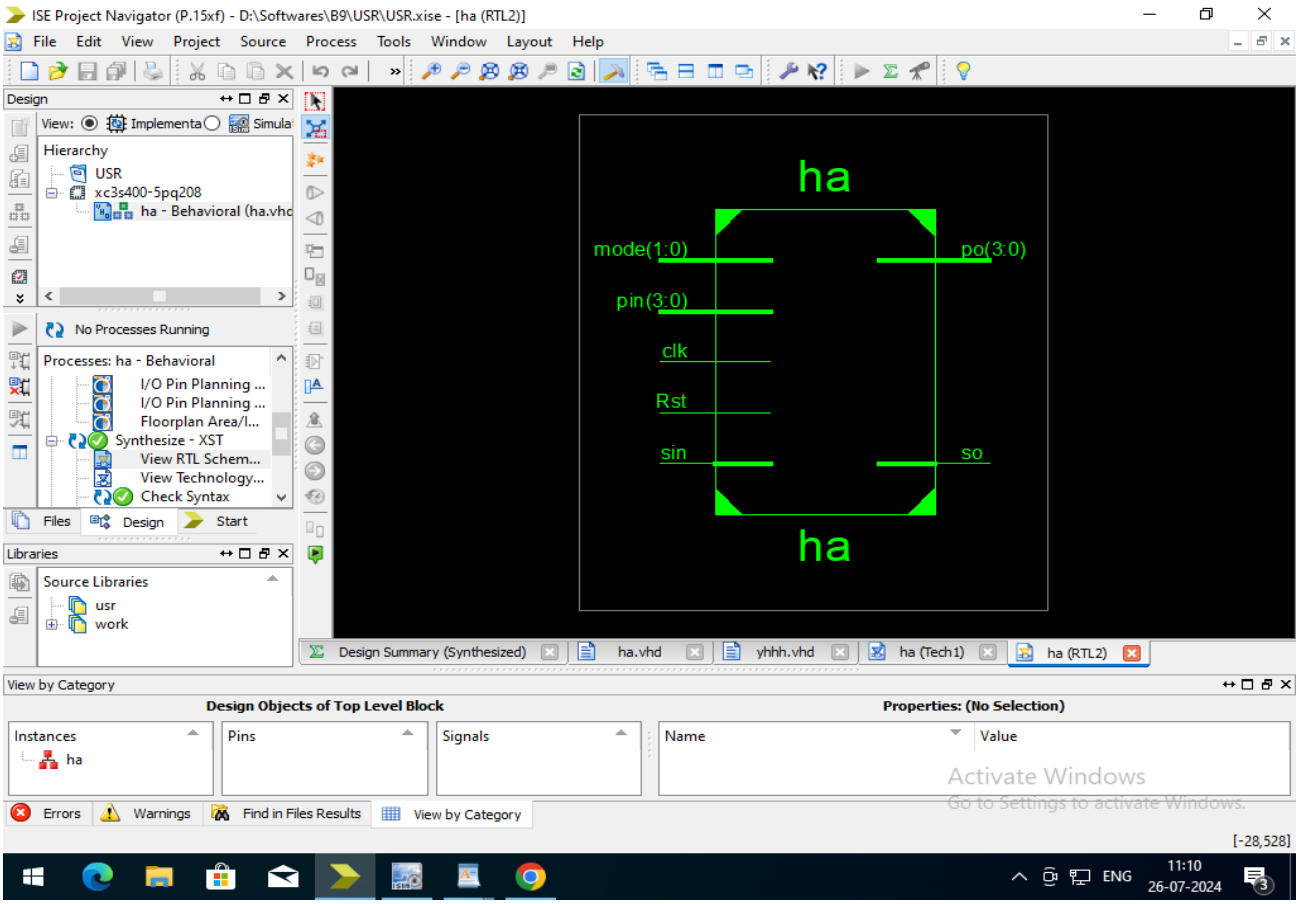
Name: Om Gajanan Mane Roll no- E41039

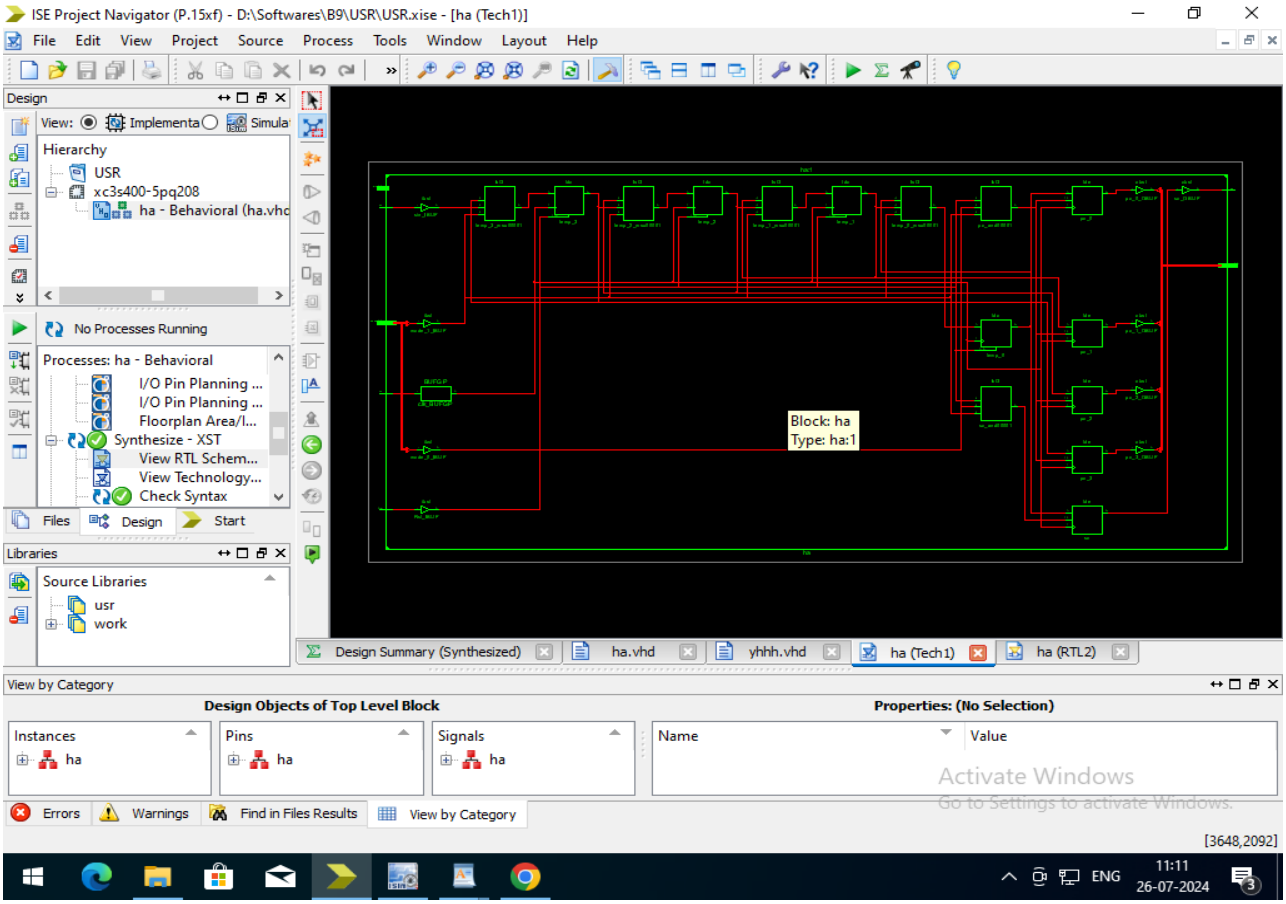
exp 3:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ha is
    Port ( Rst : in    STD_LOGIC;
           sin : in    STD_LOGIC;
           pin : in    STD_LOGIC_VECTOR (3 downto 0);
           clk : in    STD_LOGIC;
           mode : in    STD_LOGIC_VECTOR (1 downto 0);
           so : out    STD_LOGIC;
           po : out    STD_LOGIC_VECTOR (3 downto 0));
end ha;

architecture Behavioral of ha is
signal temp : std_logic_vector(3 downto 0);
begin
```

```
process(clk, Rst)
begin
if(Rst ='1' )then
temp <= "0000";
elsif( clk'event and clk='1') then

case mode is
when "00" => temp(3)<= sin;
temp(2 downto 0) <= temp (3 downto 1);
so <= temp(0);
when "01" => temp(3)<= sin;
temp(2 downto 0) <= temp (3 downto 1);
po <= temp;
when "10" => po<= pin;
when "11" => temp<= pin;
temp(2 downto 0) <= temp (3 downto 1);
so <= temp(0);

when others => null;
end case;
end if;
end process;
end Behavioral;
```

• RTL schematic -





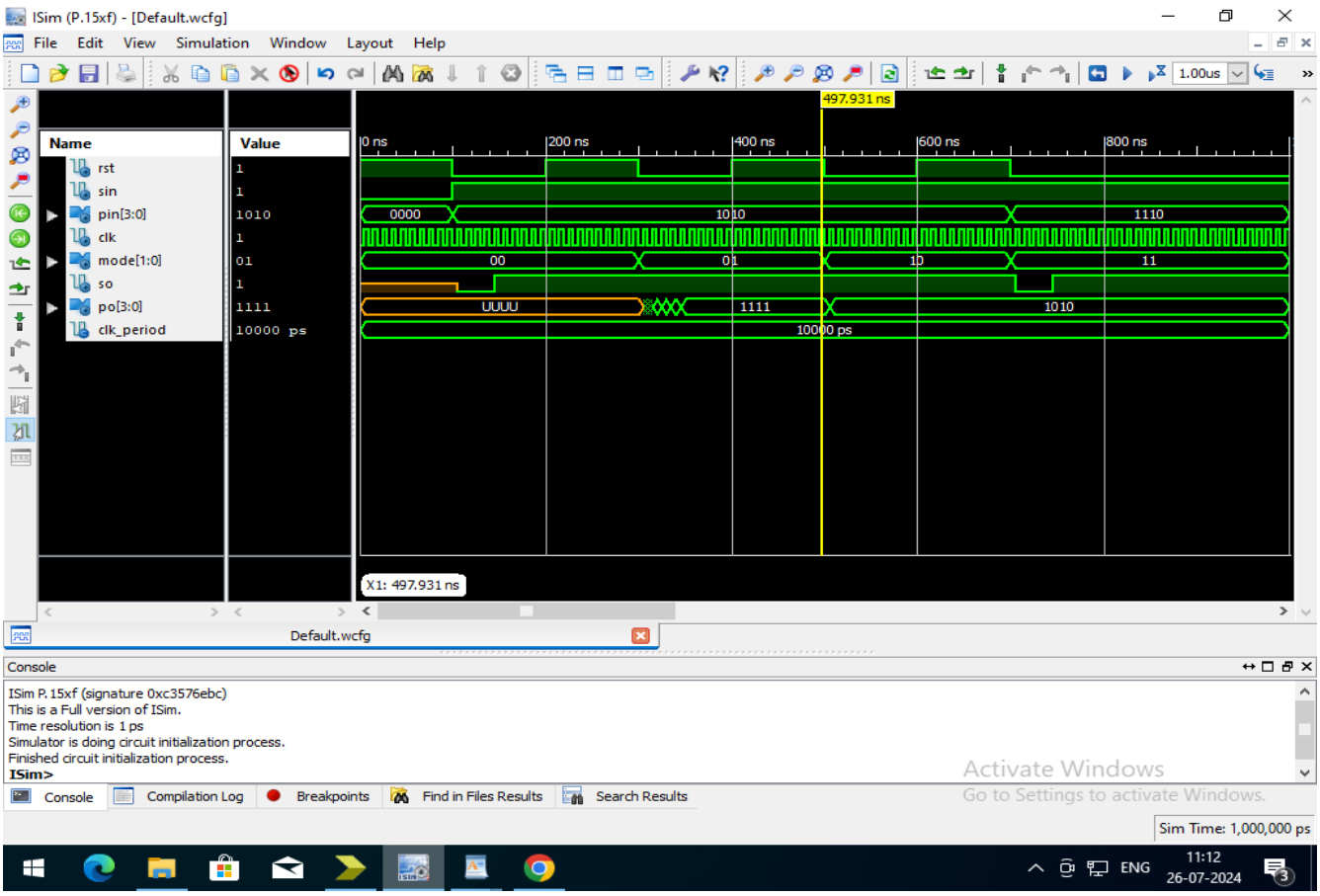
• TestBench –

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY yhhh IS
END yhhh;

ARCHITECTURE behavior OF yhhh IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT ha
    PORT(
            Rst : IN    std_logic;
            sin : IN    std_logic;
            pin : IN    std_logic_vector(3 downto 0);
            clk : IN    std_logic;
            mode : IN    std_logic_vector(1 downto 0);
            so : OUT    std_logic;
            po : OUT    std_logic_vector(3 downto 0)
          );
    END COMPONENT;

   --Inputs
   signal Rst : std_logic := '0';
   signal sin : std_logic := '0';
   signal pin : std_logic_vector(3 downto 0) := (others => '0');
   signal clk : std_logic := '0';
   signal mode : std_logic_vector(1 downto 0) := (others => '0');
```

```
        --Outputs
    signal so : std_logic;
    signal po : std_logic_vector(3 downto 0);

    -- Clock period definitions
    constant clk_period : time := 10 ns;

BEGIN

        -- Instantiate the Unit Under Test (UUT)
    uut: ha PORT MAP (
            Rst => Rst,
            sin => sin,
            pin => pin,
            clk => clk,
            mode => mode,
            so => so,
            po => po
          );

    -- Clock process definitions
    clk_process :process
    begin
                clk <= '0';
                wait for clk_period/2;
                clk <= '1';
                wait for clk_period/2;
    end process;
    -- Stimulus process
    stim_proc: process
    begin
```

```
        Rst <= '1';
        wait for 100 ns;
        Rst <= '0';

        sin<= '1';
        pin<="1010";
        mode<= "00";
        wait for 100 ns;
        Rst <= '1';
        wait for 100 ns;
        Rst <= '0';

        sin<= '1';
        pin<="1010";
        mode<= "01";
        wait for 100 ns;

        -- hold reset state for 100 ns.
        --wait for 100 ns;
Rst <= '1';
        wait for 100 ns;
        Rst <= '0';

        sin<= '1';
        pin<="1010";
        mode<= "10";
        wait for 100 ns;

        Rst <= '1';
        wait for 100 ns;
        Rst <= '0';
```

```
        sin<= '1';
        pin<="1110";
        mode<= "11";
        wait for 100 ns;
        wait for clk_period*10;

        -- insert stimulus here

        wait;
    end process;

END;
```




```
NET "Clk" LOC = "P182";
NET "Rst" LOC = "P102";
NET "Mode(0)" LOC = "P93";
```

NET "Mode(1)" LOC = "P90";

NET "si" LOC = "P101";

NET "so" LOC = "p181";

NET "pin(0)" LOC = "P87";

NET "pin(1)" LOC = "P86";

NET "pin(2)" LOC = "P85";

NET "pin(3)" LOC = "P81";

NET "pin(4)" LOC = "P80";

NET "pin(5)" LOC = "P78";

NET "pin(6)" LOC = "P77";

NET "pin(7)" LOC = "P74";

NET "po(0)" LOC = "P162";

NET "po(1)" LOC = "P165";

NET "po(2)" LOC = "P166";

NET "po(3)" LOC = "P167";

NET "po(4)" LOC = "P168";

NET "po(5)" LOC = "P171";

NET "po(6)" LOC = "P172";

NET "po(7)" LOC = "P175";

Design Summary

Release 14.1 - xst P.15xf (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: ha.prj

TABLE OF CONTENTS

===

* Synthesis Options Summary *

===

---- Source Parameters

Input File Name : "ha.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "ha"

Output Format : NGC

Target Device : xc3s400-5-pq208

---- Source Options

Top Module Name : ha

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

==========

==========

* HDL Compilation *

==========

Compiling vhdl file "D:/Softwares/B9/USR/ha.vhd" in Library work.

```
Architecture behavioral of Entity ha is up to date.
=========================================================================
*                          Design Hierarchy Analysis                    *
=========================================================================
Analyzing hierarchy for entity <ha> in library <work> (architecture <behavioral>).
=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing Entity <ha> in library <work> (Architecture <behavioral>).
Entity <ha> analyzed. Unit <ha> generated.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Performing bidirectional port resolution...


Synthesizing Unit <ha>.
    Related source file is "D:/Softwares/B9/USR/ha.vhd".
    Found 1-bit register for signal <so>.
    Found 4-bit register for signal <po>.
    Found 4-bit 4-to-1 multiplexer for signal <po$mux0000> created at line 53.
    Found 1-bit 4-to-1 multiplexer for signal <so$mux0000> created at line 53.
    Found 4-bit register for signal <temp>.
    Found 1-bit 4-to-1 multiplexer for signal <temp_0$mux0000> created at line 53.
    Found 1-bit 4-to-1 multiplexer for signal <temp_1$mux0000> created at line 53.
    Found 1-bit 4-to-1 multiplexer for signal <temp_2$mux0000> created at line 53.
    Found 1-bit 4-to-1 multiplexer for signal <temp_3$mux0000> created at line 53.
    Summary:
        inferred      9 D-type flip-flop(s).
        inferred      9 Multiplexer(s).
Unit <ha> synthesized.
```

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                          : 6
  1-bit register                                     : 5
  4-bit register                                     : 1
# Multiplexers                                       : 6
  1-bit 4-to-1 multiplexer                           : 5
  4-bit 4-to-1 multiplexer                           : 1

=========================================================================

=========================================================================
*                            Advanced HDL Synthesis                     *
=========================================================================

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                          : 9
  Flip-Flops                                         : 9
# Multiplexers                                       : 6
  1-bit 4-to-1 multiplexer                           : 5
  4-bit 4-to-1 multiplexer                           : 1
=========================================================================

=========================================================================
*                            Low Level Synthesis                        *
=========================================================================
Optimizing unit <ha> ...

Mapping all equations...
```

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block ha, actual ratio is 0.

Final Macro Processing ...

==========

Final Register Report

Macro Statistics

Registers : 9

Flip-Flops : 9

==========

==========

* Partition Report *

==========

Partition Implementation Status

No Partitions were found in this design.

==========

* Final Report *

==========

Final Results

RTL Top Level Output File Name : ha.ngr

Top Level Output File Name : ha

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 14

Cell Usage :

BELS : 20

INV : 1

LUT4 : 14

MUXF5 : 5

FlipFlops/Latches : 9

FDC : 4

FDE : 5

Clock Buffers : 1

BUFGP : 1

IO Buffers : 13

IBUF : 8

OBUF : 5

Device utilization summary:

Selected Device : 3s400pq208-5

Number of Slices:	7	out of 3584	0%
Number of Slice Flip Flops:	9	out of 7168	0%
Number of 4 input LUTs:	15	out of 7168	0%
Number of IOs:	14		
Number of bonded IOBs:	14	out of 141	9%
Number of GCLKs:	1	out of 8	12%

Partition Resource Summary:

No Partitions were found in this design.

==========

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	9

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
Rst	IBUF	4

Timing Summary:

Speed Grade: -5

Minimum period: 2.661ns (Maximum Frequency: 375.806MHz)

Minimum input arrival time before clock: 3.284ns

Maximum output required time after clock: 6.306ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

===

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.661ns (frequency: 375.806MHz)

Total number of paths / destination ports: 21 / 9

Delay: 2.661ns (Levels of Logic = 2)

Source: po_0 (FF)

Destination: po_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: po_0 to po_0

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDE:C->Q	3	0.626	1.066	po_0 (po_0)
LUT4:I0->O	1	0.479	0.000	Mmux_po_mux00003_G (N25)
MUXF5:I1->O	1	0.314	0.000	Mmux_po_mux00003 (po_mux0000<0>)
FDE:D		0.176		po_0
Total		2.661ns (1.595ns logic, 1.066ns route) (59.9% logic, 40.1% route)		

===

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 45 / 14

Offset: 3.284ns (Levels of Logic = 2)

Source: Rst (PAD)

Destination: po_0 (FF)

Destination Clock: clk rising

Data Path: Rst to po_0

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	5	0.715	0.783	Rst_IBUF (Rst_IBUF)
INV:I->O	5	0.479	0.783	Rst_inv1_INV_0 (Rst_inv)
FDE:CE		0.524		po_0
Total		3.284ns (1.718ns logic, 1.566ns route) (52.3% logic, 47.7% route)		

==========

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 5 / 5

Offset: 6.306ns (Levels of Logic = 1)

Source: po_3 (FF)

Destination: po<3> (PAD)

Source Clock: clk rising

Data Path: po_3 to po<3>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)

FDE:C->Q 3 0.626 0.771 po_3 (po_3)

OBUF:I->O 4.909 po_3_OBUF (po<3>)

Total 6.306ns (5.535ns logic, 0.771ns route)

(87.8% logic, 12.2% route)

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.91 secs

-->

Total memory usage is 4493184 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 0 (0 filtered)