Name :- swarupa omkar Maskalle Roll NO. E41038

exp 10:

```vhdl
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity HA is

      Port ( a : in    STD_LOGIC;

                b : in    STD_LOGIC;

                sum : out    STD_LOGIC;

                carry : out    STD_LOGIC);

end HA;

architecture Behavioral of HA is

begin

sum<= a xor b;

carry<= a and b;

end Behavioral;
```

Full adder Program

```vhdl
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;
```

```vhdl
-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity fa is

    Port ( a : in    STD_LOGIC;

                b : in    STD_LOGIC;

                cin : in    STD_LOGIC;

                s : out    STD_LOGIC;

                cot : out    STD_LOGIC);

end fa;

architecture Behavioral of fa is

component HA

Port ( a : in    STD_LOGIC;

                b : in    STD_LOGIC;

                sum : out    STD_LOGIC;

                carry : out    STD_LOGIC);

                        end component;

                        signal s1, c1, c2: std_logic;

begin

HA1: HA port map( a,b, s1, c1);

HA2: HA port map(s1, cin, s, c2);

cot<= c1 or c2;

end Behavioral;
```
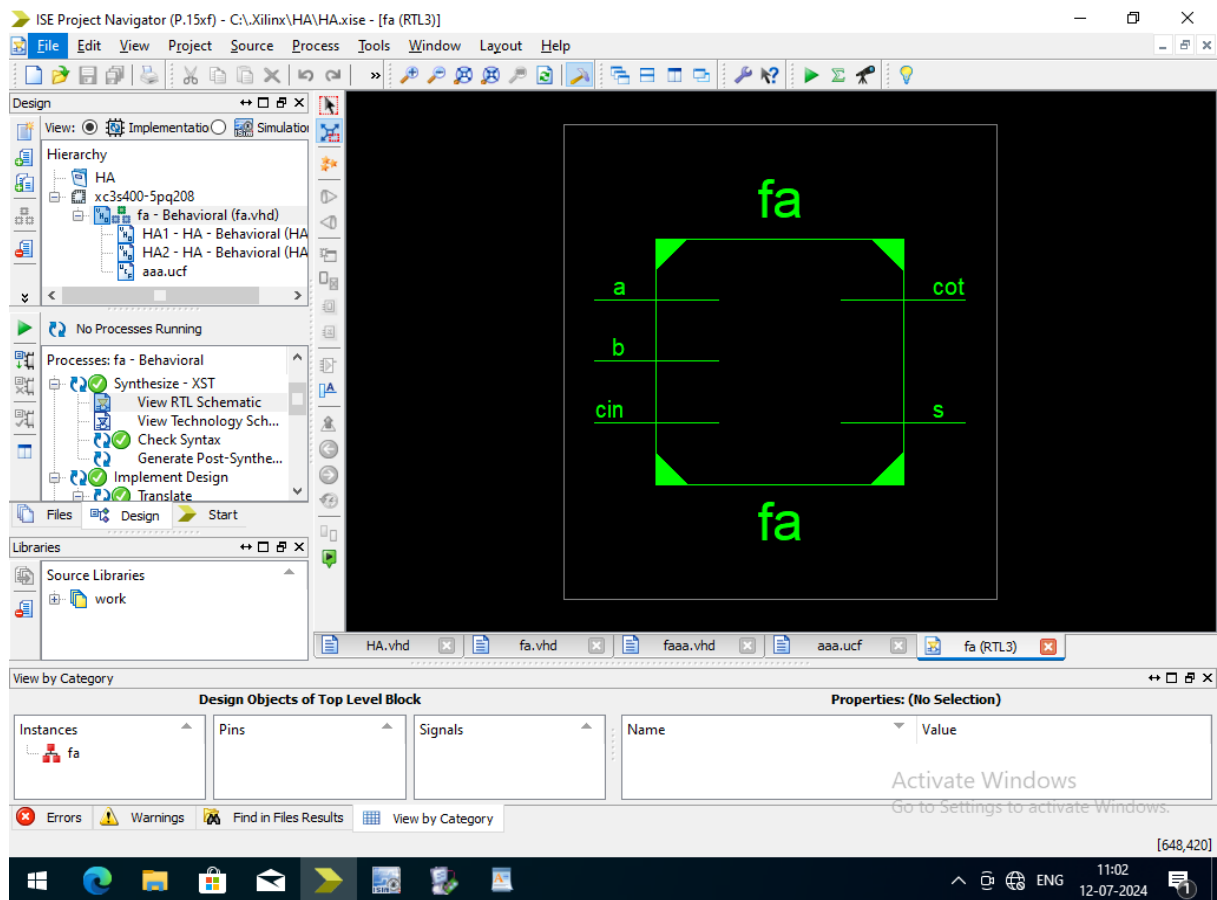
ENTITY bbbb IS

END bbbb;

 ARCHITECTURE behavior OF bbbb IS

    -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT fa111

      PORT(

            a : IN   std_logic;

            b : IN   std_logic;

            cin : IN   std_logic;

            s : OUT   std_logic;

            cout : OUT   std_logic

          );

      END COMPONENT;

```vhdl
   --Inputs

   signal a : std_logic := '0';

   signal b : std_logic := '0';

   signal cin : std_logic := '0';

   --Outputs

   signal s : std_logic;

   signal cout : std_logic;

   -- No clocks detected in port list. Replace <clock> below with

   -- appropriate port name

  -- constant <clock>_period : time := 10 ns;

 BEGIN

 -- Instantiate the Unit Under Test (UUT)

   uut: fa111 PORT MAP (

           a => a,

           b => b,

           cin => cin,

           s => s,

           cout => cout );

  -- Clock process definitions

--     <clock>_process :process

--     begin

--              <clock> <= '0';

--              wait for <clock>_period/2;

--              <clock> <= '1';

--              wait for <clock>_period/2;

--     end process;

   -- Stimulus process

   stim_proc: process

   begin
```

```vhdl
a<='0';

b<='0';

cin<='0';

        -- hold reset state for 100 ns.

        wait for 100 ns;

                a<='0';

b<='0';

cin<='1';

        -- hold reset state for 100 ns.

        wait for 100 ns;

a<='0';

b<='1';

cin<='0';

        -- hold reset state for 100 ns.

        wait for 100 ns;

a<='0';

b<='1';

cin<='1';

        -- hold reset state for 100 ns.

        wait for 100 ns;

a<='1';

b<='0';

cin<='0';

        -- hold reset state for 100 ns.

        wait for 100 ns;

a<='1';

b<='0';

cin<='1';

        -- hold reset state for 100 ns.

        wait for 100 ns;
```

```vhdl
a<='1';

b<='1';

cin<='0';

      -- hold reset state for 100 ns.

      wait for 100 ns;

a<='1';

b<='1';

cin<='1';

      -- hold reset state for 100 ns.

      wait for 100 ns;

a<='0';

b<='0';

cin<='0';

      -- hold reset state for 100 ns.

      wait for 100 ns;
--       wait for <clock>_period*10;

  -- insert stimulus here

  wait;

    end process;

END;
```
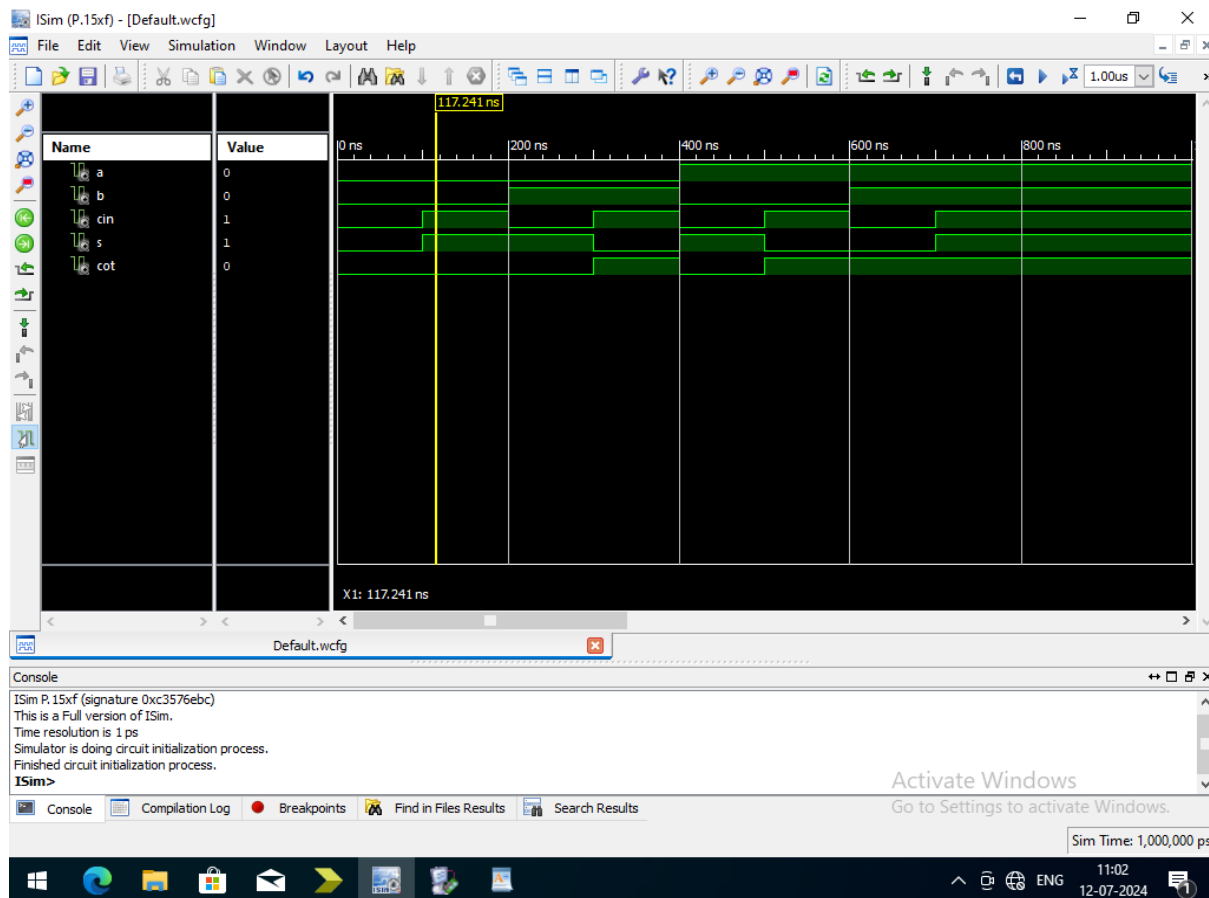
User Constraint file

net a loc = p87;

net b loc= p86;

net cin loc= p85;

net s loc = p162;

net cot loc = p165;

Design summary

Release 14.1 - xst P.15xf (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: fa.prj

TABLE OF CONTENTS

===

*   Synthesis Options Summary   *

===

---- Source Parameters

Input File Name   : "fa.prj"

Input Format   : mixed

Ignore Synthesis Constraint File   : NO

---- Target Parameters

Output File Name   : "fa"

Output Format   : NGC

Target Device   : xc3s400-5-pq208

---- Source Options

Top Module Name   : fa

Automatic FSM Extraction   : YES

FSM Encoding Algorithm   : Auto

Safe Implementation   : No

FSM Style   : LUT

RAM Extraction   : Yes

RAM Style   : Auto

ROM Extraction   : Yes

Mux Style   : Auto

Decoder Extraction   : YES

Priority Encoder Extraction   : Yes

Shift Register Extraction   : YES

Logical Shifter Extraction   : YES

XOR Collapsing   : YES

ROM Style   : Auto

Mux Extraction   : Yes

Resource Sharing   : YES

Asynchronous To Synchronous   : NO

Multiplier Style   : Auto

Automatic Register Balancing   : No

---- Target Options

Add IO Buffers   : YES

Global Maximum Fanout   : 500

Add Generic Clock Buffer(BUFG)   : 8

Register Duplication   : YES

Slice Packing   : YES

Optimize Instantiated Primitives   : NO

Use Clock Enable   : Yes

Use Synchronous Set   : Yes

Use Synchronous Reset   : Yes

Pack IO Registers into IOBs   : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

===

===
*   HDL Compilation   *
===
Compiling vhdl file "C:/.Xilinx/ha/HA.vhd" in Library work.

Architecture behavioral of Entity ha is up to date.

Compiling vhdl file "C:/.Xilinx/ha/fa.vhd" in Library work.

Architecture behavioral of Entity fa is up to date.

==

*   Design Hierarchy Analysis   *

==

Analyzing hierarchy for entity <fa> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <HA> in library <work> (architecture <behavioral>).

==

*   HDL Analysis   *

==

Analyzing Entity <fa> in library <work> (Architecture <behavioral>).

Entity <fa> analyzed. Unit <fa> generated.

Analyzing Entity <HA> in library <work> (Architecture <behavioral>).

Entity <HA> analyzed. Unit <HA> generated.

==

*   HDL Synthesis   *

==

Performing bidirectional port resolution...

Synthesizing Unit <HA>.

    Related source file is "C:/.Xilinx/ha/HA.vhd".

    Found 1-bit xor2 for signal <sum>.

Unit <HA> synthesized.

Synthesizing Unit <fa>.

   Related source file is "C:/.Xilinx/ha/fa.vhd".

Unit <fa> synthesized.

===

HDL Synthesis Report

Macro Statistics

Xors   : 2

  1-bit xor2   : 2

===

===
*   Advanced HDL Synthesis   *
===

===

Advanced HDL Synthesis Report

Macro Statistics

Xors   : 2

  1-bit xor2   : 2

===

===
*   Low Level Synthesis   *
===

Optimizing unit <fa> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block fa, actual ratio is 0.

Final Macro Processing ...

===
Final Register Report

Found no macro
===

===
*   Partition Report   *
===

Partition Implementation Status

   No Partitions were found in this design.

===
*   Final Report   *
===
Final Results

RTL Top Level Output File Name   : fa.ngr

Top Level Output File Name   : fa

Output Format   : NGC

Optimization Goal   : Speed

Keep Hierarchy   : No

Design Statistics

IOs   : 5

Cell Usage :

BELS   : 2

LUT3   : 2

IO Buffers   : 5

IBUF   : 3

OBUF   : 2

===

Device utilization summary:

Selected Device : 3s400pq208-5

 Number of Slices: 1   out of   3584   0%

 Number of 4 input LUTs: 2   out of   7168   0%

 Number of IOs: 5

 Number of bonded IOBs: 5   out of   141   3%

Partition Resource Summary:

No Partitions were found in this design.

==

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -5

    Minimum period: No path found

    Minimum input arrival time before clock: No path found

    Maximum output required time after clock: No path found

    Maximum combinational path delay: 7.824ns

Timing Detail:

All values displayed in nanoseconds (ns)

==

Timing constraint: Default path analysis

   Total number of paths / destination ports: 6 / 2

Delay: 7.824ns (Levels of Logic = 3)

  Source: b (PAD)

  Destination: cot (PAD)

  Data Path: b to cot

		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	0.715	1.040	b_IBUF (b_IBUF)
LUT3:I0->O	1	0.479	0.681	cot1 (cot_OBUF)
OBUF:I->O		4.909		cot_OBUF (cot)

  Total   7.824ns (6.103ns logic, 1.721ns route)

                                  (78.0% logic, 22.0% route)

==

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.73 secs

-->

Total memory usage is 4493212 kilobytes

Number of errors   :   0 (0 filtered)

Number of warnings :   0 (0 filtered)

Number of infos   :   0 (0 filtered)