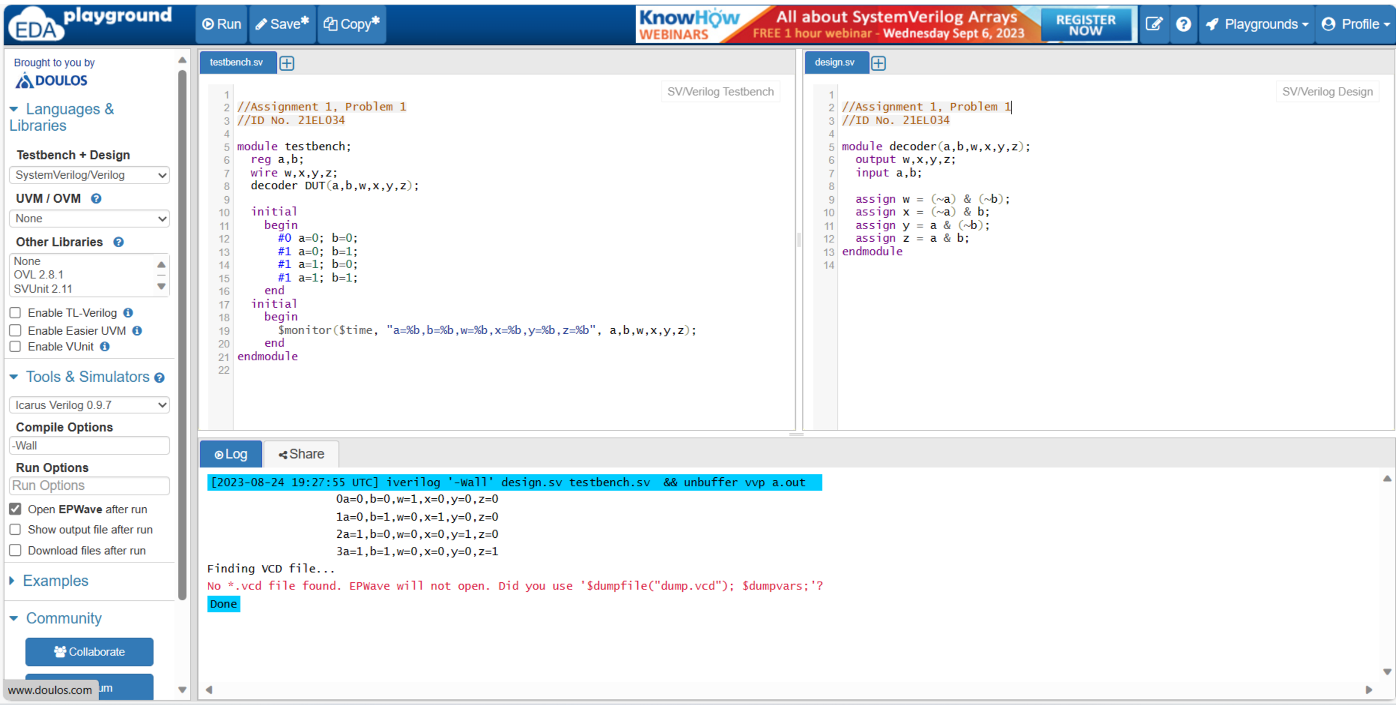
ID No. 21EL034

ASSIGNMENT – 1

Q1. Write a Verilog code for 2X4 decoder.



Testbench + Design: SystemVerilog/Verilog
UVM / OVM: None
Other Libraries: None, OVL 2.8.1, SVUnit 2.11
□ Enable TL-Verilog
□ Enable Easier UVM
□ Enable VUnit
Tools & Simulators: Icarus Verilog 0.9.7
Compile Options: -Wall
Run Options: Run Options
☑ Open EPWave after run
□ Show output file after run
□ Download files after run

SV/Verilog Testbench

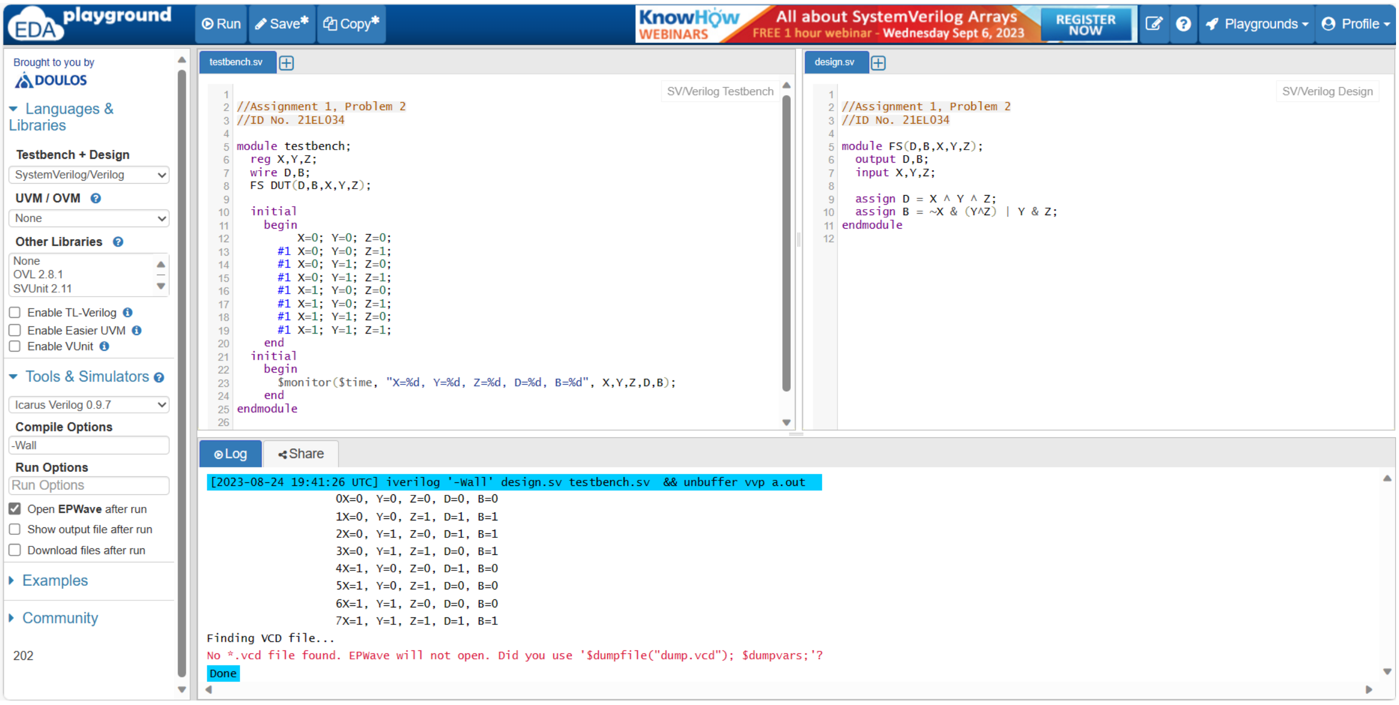
```
//Assignment 1, Problem 1
//ID No. 21EL034

module testbench;
  reg a,b;
  wire w,x,y,z;
  decoder DUT(a,b,w,x,y,z);

  initial
    begin
      #0 a=0; b=0;
      #1 a=0; b=1;
      #1 a=1; b=0;
      #1 a=1; b=1;
    end
  initial
    begin
      $monitor($time, "a=%b,b=%b,w=%b,x=%b,y=%b,z=%b", a,b,w,x,y,z);
    end
endmodule
```

SV/Verilog Design

```
//Assignment 1, Problem 1
//ID No. 21EL034

module decoder(a,b,w,x,y,z);
  output w,x,y,z;
  input a,b;

  assign w = (~a) & (~b);
  assign x = (~a) & b;
  assign y = a & (~b);
  assign z = a & b;
endmodule
```

```
[2023-08-24 19:27:55 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
                   0a=0,b=0,w=1,x=0,y=0,z=0
                   1a=0,b=1,w=0,x=1,y=0,z=0
                   2a=1,b=0,w=0,x=0,y=1,z=0
                   3a=1,b=1,w=0,x=0,y=0,z=1
Finding VCD file...
No *.vcd file found. EPWave will not open. Did you use '$dumpfile("dump.vcd"); $dumpvars;'?
Done
```

Q2. Write a Verilog code for Full subtractor.



Testbench + Design: SystemVerilog/Verilog
UVM / OVM: None
Other Libraries: None, OVL 2.8.1, SVUnit 2.11
□ Enable TL-Verilog
□ Enable Easier UVM
□ Enable VUnit
Tools & Simulators: Icarus Verilog 0.9.7
Compile Options: -Wall
Run Options: Run Options
☑ Open EPWave after run
□ Show output file after run
□ Download files after run

SV/Verilog Testbench

```
//Assignment 1, Problem 2
//ID No. 21EL034

module testbench;
  reg X,Y,Z;
  wire D,B;
  FS DUT(D,B,X,Y,Z);

  initial
    begin
        X=0; Y=0; Z=0;
      #1 X=0; Y=0; Z=1;
      #1 X=0; Y=1; Z=0;
      #1 X=0; Y=1; Z=1;
      #1 X=1; Y=0; Z=0;
      #1 X=1; Y=0; Z=1;
      #1 X=1; Y=1; Z=0;
      #1 X=1; Y=1; Z=1;
    end
  initial
    begin
      $monitor($time, "X=%d, Y=%d, Z=%d, D=%d, B=%d", X,Y,Z,D,B);
    end
endmodule
```

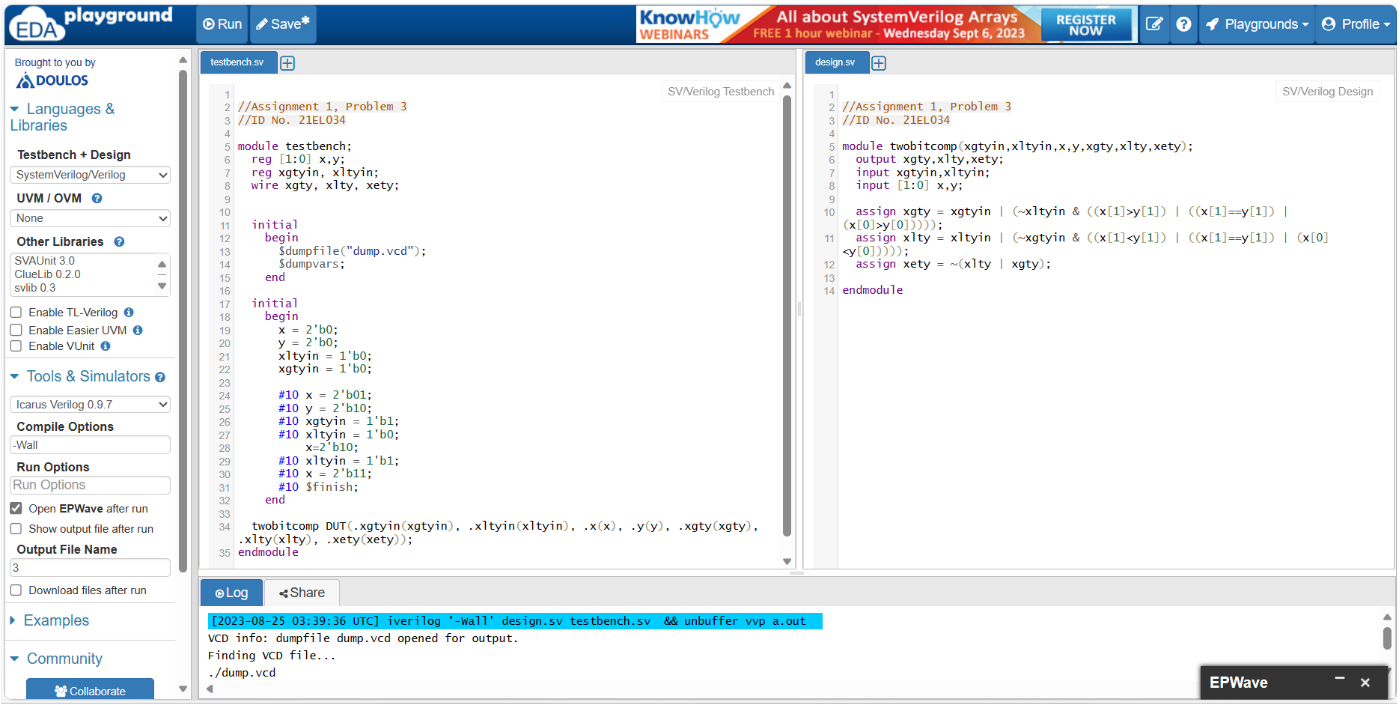
SV/Verilog Design

```
//Assignment 1, Problem 2
//ID No. 21EL034

module FS(D,B,X,Y,Z);
  output D,B;
  input X,Y,Z;

  assign D = X ^ Y ^ Z;
  assign B = ~X & (Y^Z) | Y & Z;
endmodule
```

```
[2023-08-24 19:41:26 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
                   0X=0, Y=0, Z=0, D=0, B=0
                   1X=0, Y=0, Z=1, D=1, B=1
                   2X=0, Y=1, Z=0, D=1, B=1
                   3X=0, Y=1, Z=1, D=0, B=1
                   4X=1, Y=0, Z=0, D=1, B=0
                   5X=1, Y=0, Z=1, D=0, B=0
                   6X=1, Y=1, Z=0, D=0, B=0
                   7X=1, Y=1, Z=1, D=1, B=1
Finding VCD file...
No *.vcd file found. EPWave will not open. Did you use '$dumpfile("dump.vcd"); $dumpvars;'?
Done
```

ID No. 21EL034

Q3. Write a Verilog code for 2-bit comparator.



Testbench + Design: SystemVerilog/Verilog

UVM / OVM: None

Other Libraries: SVAUnit 3.0, ClueLib 0.2.0, svlib 0.3

□ Enable TL-Verilog
□ Enable Easier UVM
□ Enable VUnit

Icarus Verilog 0.9.7

Compile Options: -Wall

Run Options: Run Options

☑ Open EPWave after run
□ Show output file after run

Output File Name: 3

□ Download files after run

testbench.sv

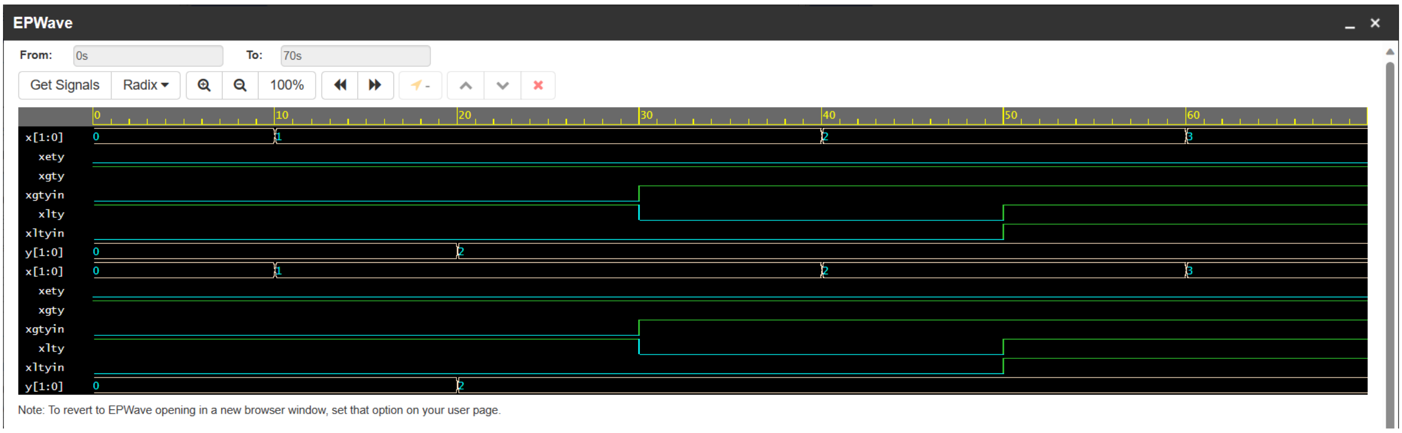
```verilog

//Assignment 1, Problem 3
//ID No. 21EL034

module testbench;
  reg [1:0] x,y;
  reg xgtyin, xltyin;
  wire xgty, xlty, xety;


  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars;
    end

  initial
    begin
      x = 2'b0;
      y = 2'b0;
      xltyin = 1'b0;
      xgtyin = 1'b0;

      #10 x = 2'b01;
      #10 y = 2'b10;
      #10 xgtyin = 1'b1;
      #10 xltyin = 1'b0;
          x=2'b10;
      #10 xltyin = 1'b1;
      #10 x = 2'b11;
      #10 $finish;
    end

  twobitcomp DUT(.xgtyin(xgtyin), .xltyin(xltyin), .x(x), .y(y), .xgty(xgty),
.xlty(xlty), .xety(xety));
endmodule
```

design.sv

```verilog

//Assignment 1, Problem 3
//ID No. 21EL034

module twobitcomp(xgtyin,xltyin,x,y,xgty,xlty,xety);
  output xgty,xlty,xety;
  input xgtyin,xltyin;
  input [1:0] x,y;

  assign xgty = xgtyin | (~xltyin & ((x[1]>y[1]) | ((x[1]==y[1]) |
(x[0]>y[0]))));
  assign xlty = xltyin | (~xgtyin & ((x[1]<y[1]) | ((x[1]==y[1]) | (x[0]
<y[0]))));
  assign xety = ~(xlty | xgty);

endmodule
```

```
[2023-08-25 03:39:36 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
Finding VCD file...
./dump.vcd
```

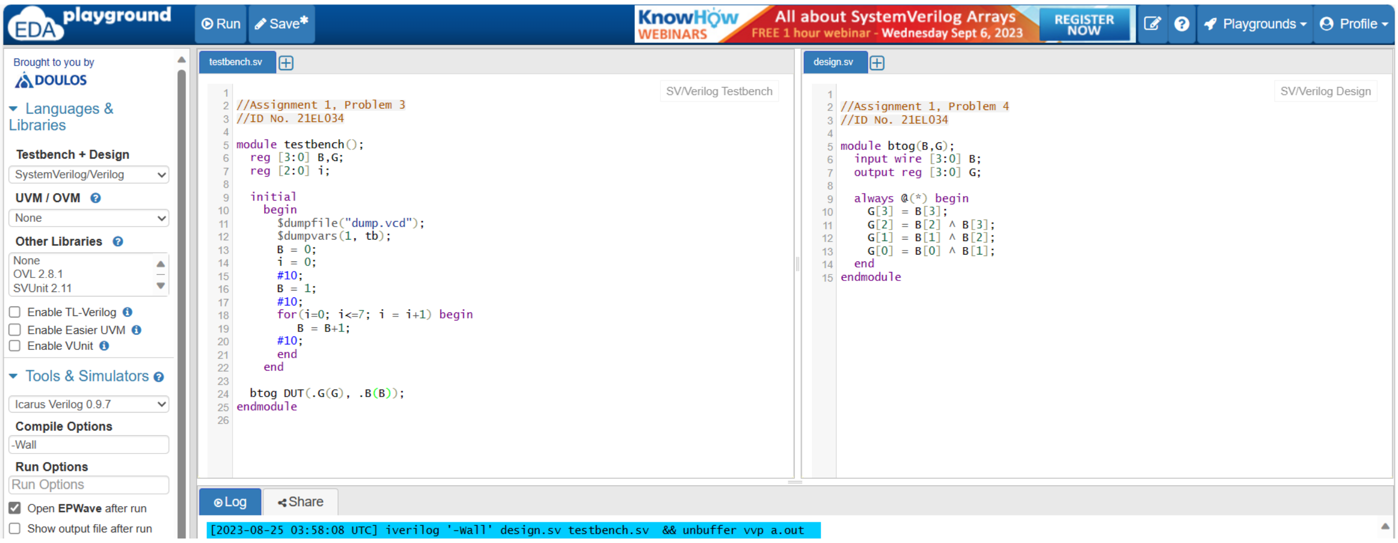
OUTPUT:



From: 0s To: 70s

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Q4. Write a Verilog code for 3 bit binary to Gray convertor.



Testbench + Design: SystemVerilog/Verilog

UVM / OVM: None

Other Libraries: None, OVL 2.8.1, SVUnit 2.11

□ Enable TL-Verilog

□ Enable Easier UVM

□ Enable VUnit

Tools & Simulators: Icarus Verilog 0.9.7

Compile Options: -Wall

Run Options: Run Options

☑ Open EPWave after run

□ Show output file after run

testbench.sv

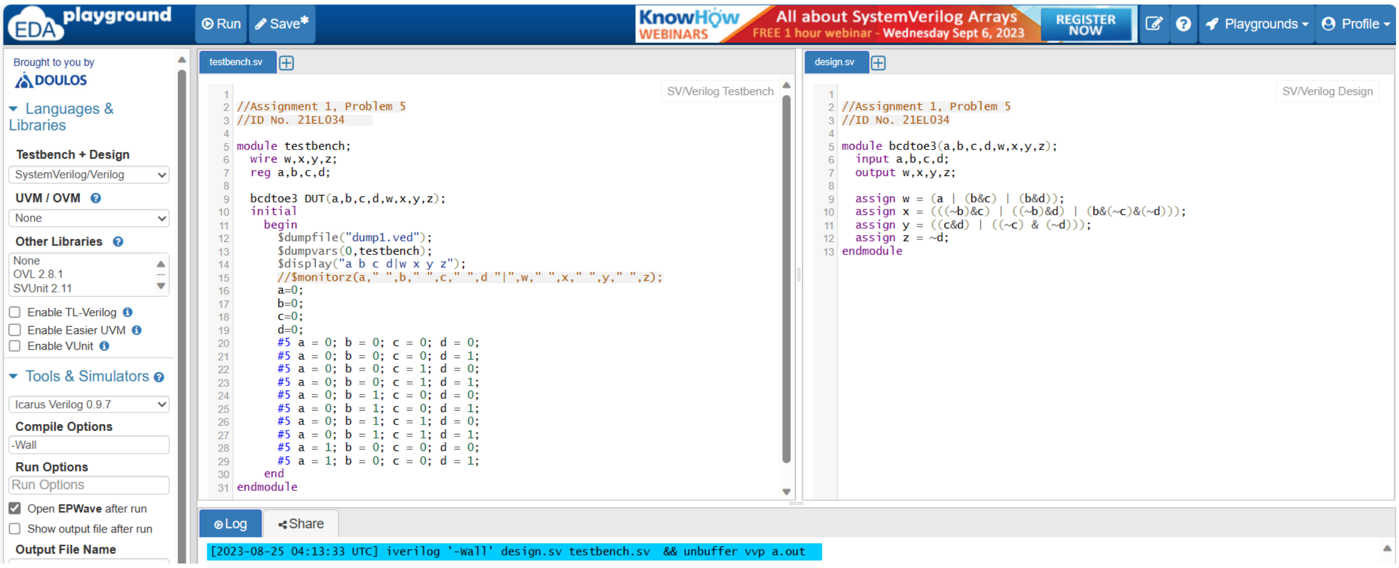
```verilog

//Assignment 1, Problem 3
//ID No. 21EL034

module testbench();
  reg [3:0] B,G;
  reg [2:0] i;

  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1, tb);
      B = 0;
      i = 0;
      #10;
      B = 1;
      #10;
      for(i=0; i<=7; i = i+1) begin
         B = B+1;
      #10;
      end
    end

  btog DUT(.G(G), .B(B));
endmodule

```

design.sv

```verilog

//Assignment 1, Problem 4
//ID No. 21EL034

module btog(B,G);
  input wire [3:0] B;
  output reg [3:0] G;

  always @(*) begin
    G[3] = B[3];
    G[2] = B[2] ^ B[3];
    G[1] = B[1] ^ B[2];
    G[0] = B[0] ^ B[1];
  end
endmodule
```

```
[2023-08-25 03:58:08 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
```

Q5. Write a Verilog code for BCD to excess 3 convertors.



Testbench + Design: SystemVerilog/Verilog

UVM / OVM: None

Other Libraries: None, OVL 2.8.1, SVUnit 2.11

□ Enable TL-Verilog

□ Enable Easier UVM

□ Enable VUnit

Tools & Simulators: Icarus Verilog 0.9.7

Compile Options: -Wall

Run Options: Run Options

☑ Open EPWave after run

□ Show output file after run

Output File Name

testbench.sv

```verilog

//Assignment 1, Problem 5
//ID No. 21EL034

module testbench;
  wire w,x,y,z;
  reg a,b,c,d;

  bcdtoe3 DUT(a,b,c,d,w,x,y,z);
  initial
    begin
      $dumpfile("dump1.ved");
      $dumpvars(0,testbench);
      $display("a b c d|w x y z");
      //$monitorz(a," ",b," ",c," ",d "|",w," ",x," ",y," ",z);
      a=0;
      b=0;
      c=0;
      d=0;
      #5 a = 0; b = 0; c = 0; d = 0;
      #5 a = 0; b = 0; c = 0; d = 1;
      #5 a = 0; b = 0; c = 1; d = 0;
      #5 a = 0; b = 0; c = 1; d = 1;
      #5 a = 0; b = 1; c = 0; d = 0;
      #5 a = 0; b = 1; c = 0; d = 1;
      #5 a = 0; b = 1; c = 1; d = 0;
      #5 a = 0; b = 1; c = 1; d = 1;
      #5 a = 1; b = 0; c = 0; d = 0;
      #5 a = 1; b = 0; c = 0; d = 1;
    end
endmodule
```

design.sv

```verilog

//Assignment 1, Problem 5
//ID No. 21EL034

module bcdtoe3(a,b,c,d,w,x,y,z);
  input a,b,c,d;
  output w,x,y,z;

  assign w = (a | (b&c) | (b&d));
  assign x = (((~b)&c) | ((~b)&d) | (b&(~c)&(~d)));
  assign y = ((c&d) | ((~c) & (~d)));
  assign z = ~d;
endmodule
```

```
[2023-08-25 04:13:33 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
```