Instruction	op5	op4	op3	op2	op1	op0	Jump	Branch	B_type1	B_type0	SignSLc	SourceSlc	RegWrite	B_ALUSrc	WbSlc1	WbSlc0	WrMemory	ReadMemory
R_Type	0	0	0	0	0	0	0	0	x	x	x	0	1	1	0	0	0	0
SLLI	0	0	0	0	0	1	0	0	x	x	x	0	1	0	0	0	0	0
SRLI	0	0	0	0	1	0	0	0	x	x	x	0	1	0	0	0	0	0
SRAI	0	0	0	0	1	1	0	0	x	x	x	0	1	0	0	0	0	0
RORI	0	0	0	1	0	0	0	0	x	x	x	0	1	0	0	0	0	0
ADDI	0	0	0	1	0	1	0	0	x	x	1	0	1	0	0	0	0	0
SLTI	0	0	0	1	1	0	0	0	x	x	1	0	1	0	0	0	0	0
SLTIU	0	0	0	1	1	1	0	0	x	x	0	0	1	0	0	0	0	0
SEQI	0	0	1	0	0	0	0	0	x	x	1	0	1	0	0	0	0	0
XORI	0	0	1	0	0	1	0	0	x	x	0	0	1	0	0	0	0	0
ORI	0	0	1	0	1	0	0	0	x	x	0	0	1	0	0	0	0	0
ANDI	0	0	1	0	1	1	0	0	x	x	0	0	1	0	0	0	0	0
NORI	0	0	1	1	0	0	0	0	x	x	0	0	1	0	0	0	0	0
SET	0	0	1	1	0	1	0	0	x	x	1	x	1	0	0	0	0	0
SSET	0	0	1	1	1	0	0	0	x	x	x	1	1	0	0	0	0	0
JALR	0	0	1	1	1	1	1	0	x	x	1	0	1	0	1	0	0	0
LW	0	1	0	0	0	0	0	0	x	x	1	0	1	0	0	1	0	1
SW	0	1	0	0	0	1	0	0	x	x	x	0	0	0	x	x	1	0
BEQ	0	1	0	0	1	0	0	1	0	0	x	0	0	1	x	x	0	0
BNE	0	1	0	0	1	1	0	1	0	1	x	0	0	1	x	x	0	0
BLT	0	1	0	1	0	0	0	1	1	0	x	0	0	1	x	x	0	0
BGE	0	1	0	1	0	1	0	1	1	1	x	0	0	1	x	x	0	0
BLTU	0	1	0	1	1	0	0	1	1	0	x	0	0	1	x	x	0	0
BGEU	0	1	0	1	1	1	0	1	1	1	x	0	0	1	x	x	0	0