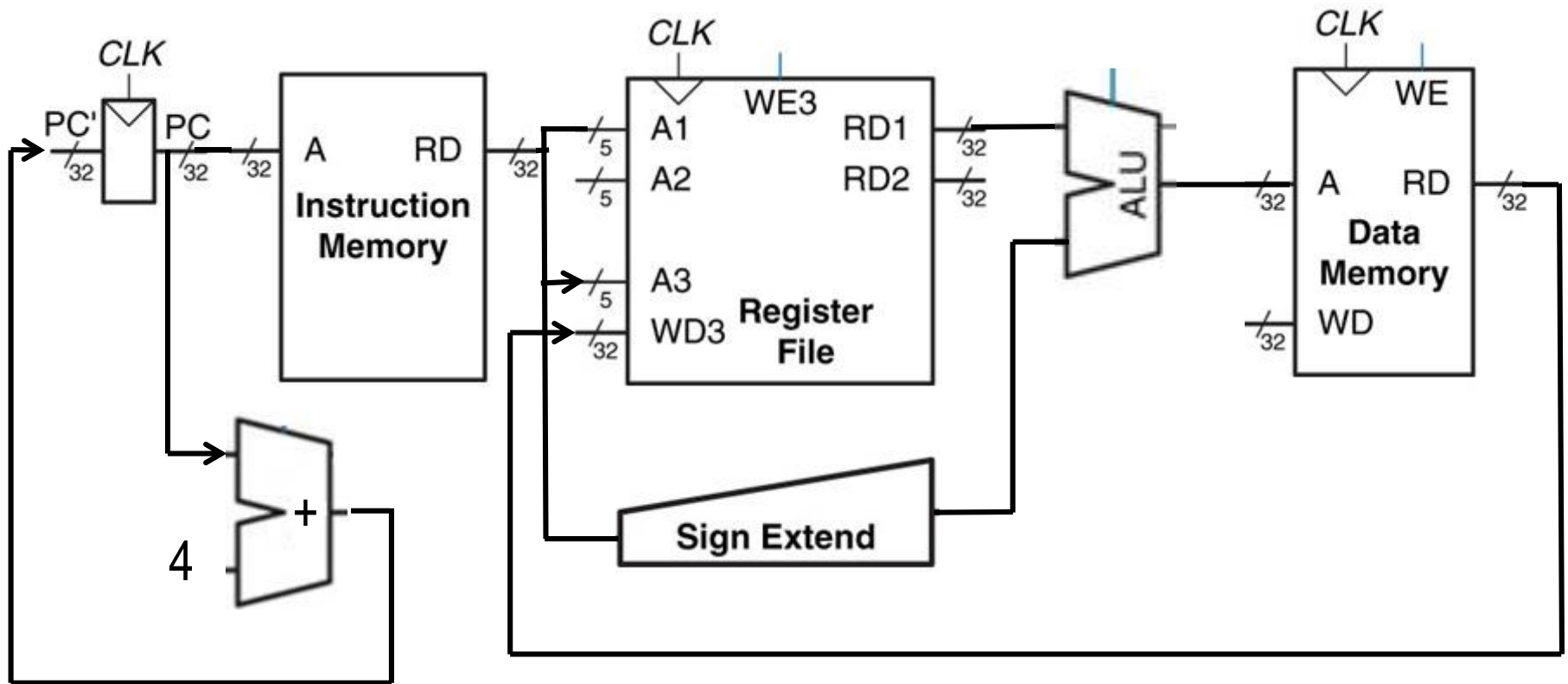


MIPS Assembly Programming

The Language of a MIPS CPU

32-bit RegisterFile + ALU

MIPS



Why Assembly?

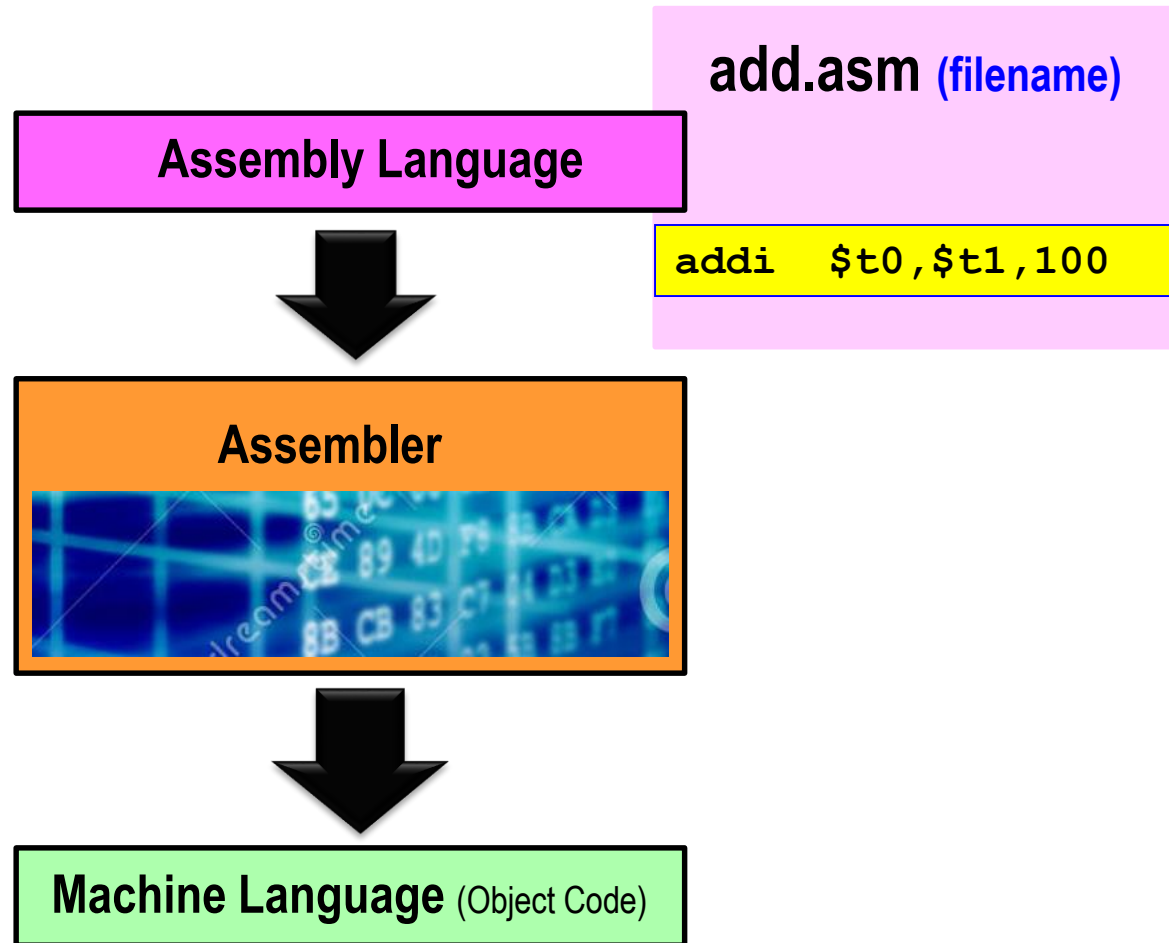
- **Assembly is widely used in industry:**
 - Embedded systems
 - Real time systems
 - Low level and direct access to hardware
- **Assembly is widely used **not** in industry:**
 - Cracking software protections: patching, patch-loaders and emulators ... **software reverse engineering**
 - Hacking into computer systems: buffer under/overflows, worms and Trojans.

Assembly-Machine Language

- Each assembly language is specific to a particular computer architecture (CPU)
- Each computer architecture (CPU) has its own machine language.



Assembly & Machine Languages



0000 0001 0010 1011 1000 0000 0010 0000

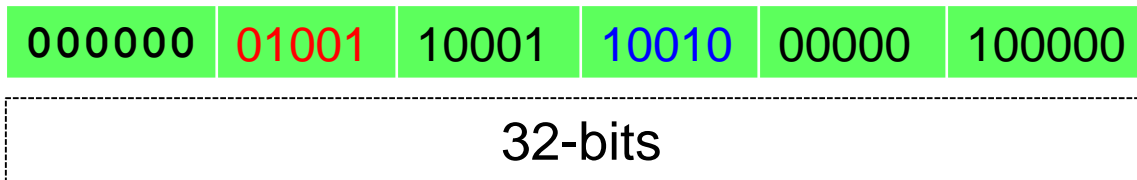
MIPS Architecture

- MIPS architecture is ...
 - Register-to-Register
 - Load/Store
- The destination and sources must **all** be Registers
- To access the main memory, special instructions (Load/Store) are needed.

MIPS: Register File

MIPS processors have **32-registers**, each of which holds a **32-bit** value

- The data inputs and outputs are **32-bits** wide.



MIPS register names convention

- MIPS register names begin with a dollar sign → \$

1. By number:

\$0, \$1, ... , \$31

2. By a letter and a number:

\$a0-\$a2 ...

MIPS registers

Registers	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194304
hi		0
lo		0

Name	Number	Use	Preserved across a call?
\$zero	0	The constant value 0	N.A.
\$at	1	Assembler temporary	No
\$v0-\$v1	2-3	Values for function results and expression evaluation	No
\$a0-\$a3	4-7	Arguments	No
\$t0-\$t7	8-15	Temporaries	No
\$s0-\$s7	16-23	Saved temporaries	Yes
\$t8-\$t9	24-25	Temporaries	No
\$k0-\$k1	26-27	Reserved for OS kernel	No
\$gp	28	Global pointer	Yes
\$sp	29	Stack pointer	Yes
\$fp	30	Frame pointer	Yes
\$ra	31	Return address	Yes

Figure 1.4 MIPS registers and usage conventions. In addition to the 32 general-purpose registers (R0-R31), MIPS has 32 floating-point registers (F0-F31) that can hold either a 32-bit single-precision number or a 64-bit double-precision number.



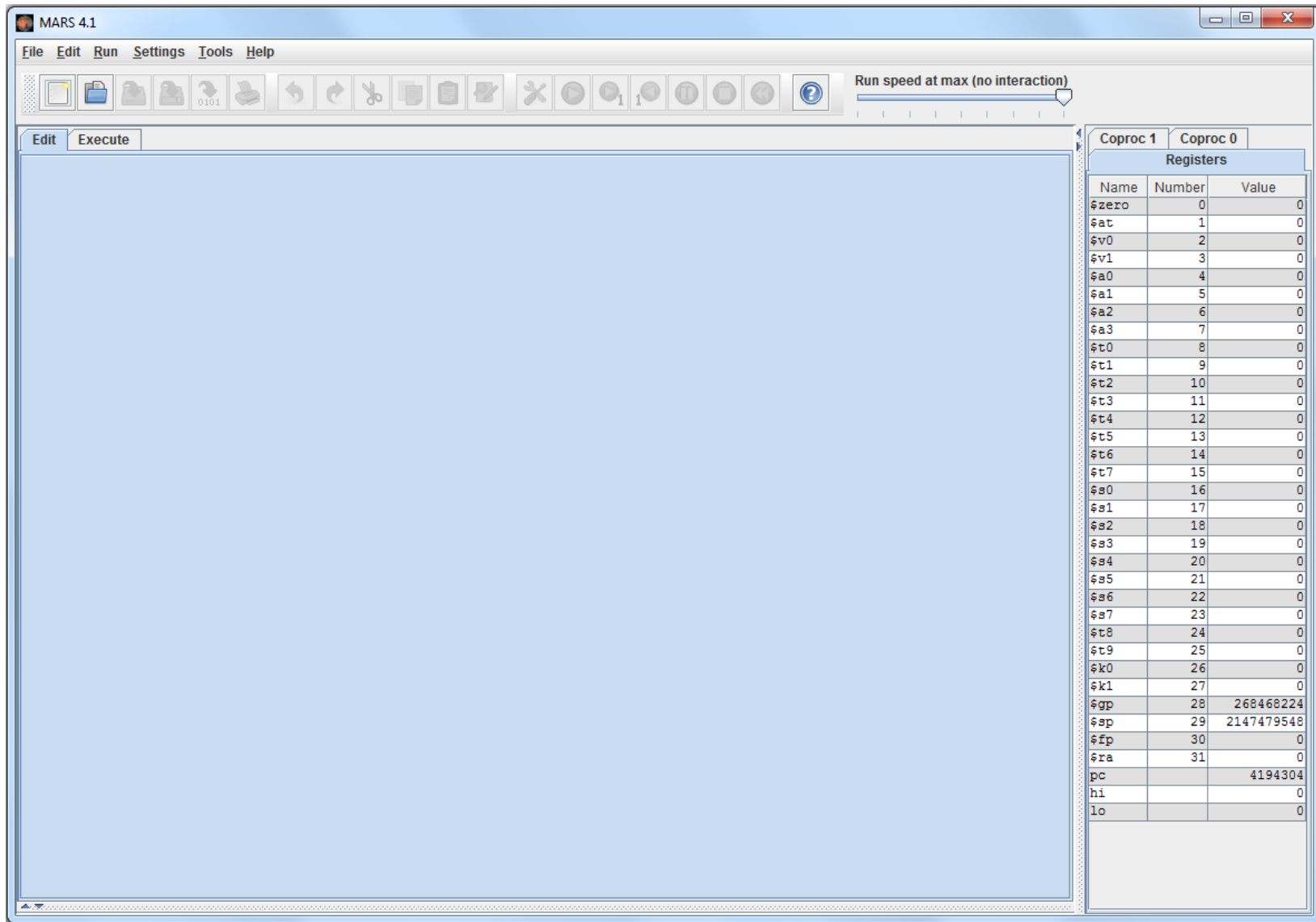
MARS (MIPS Assembler and Runtime Simulator)

An interactive development environment (IDE) for MIPS Assembly Language Programming

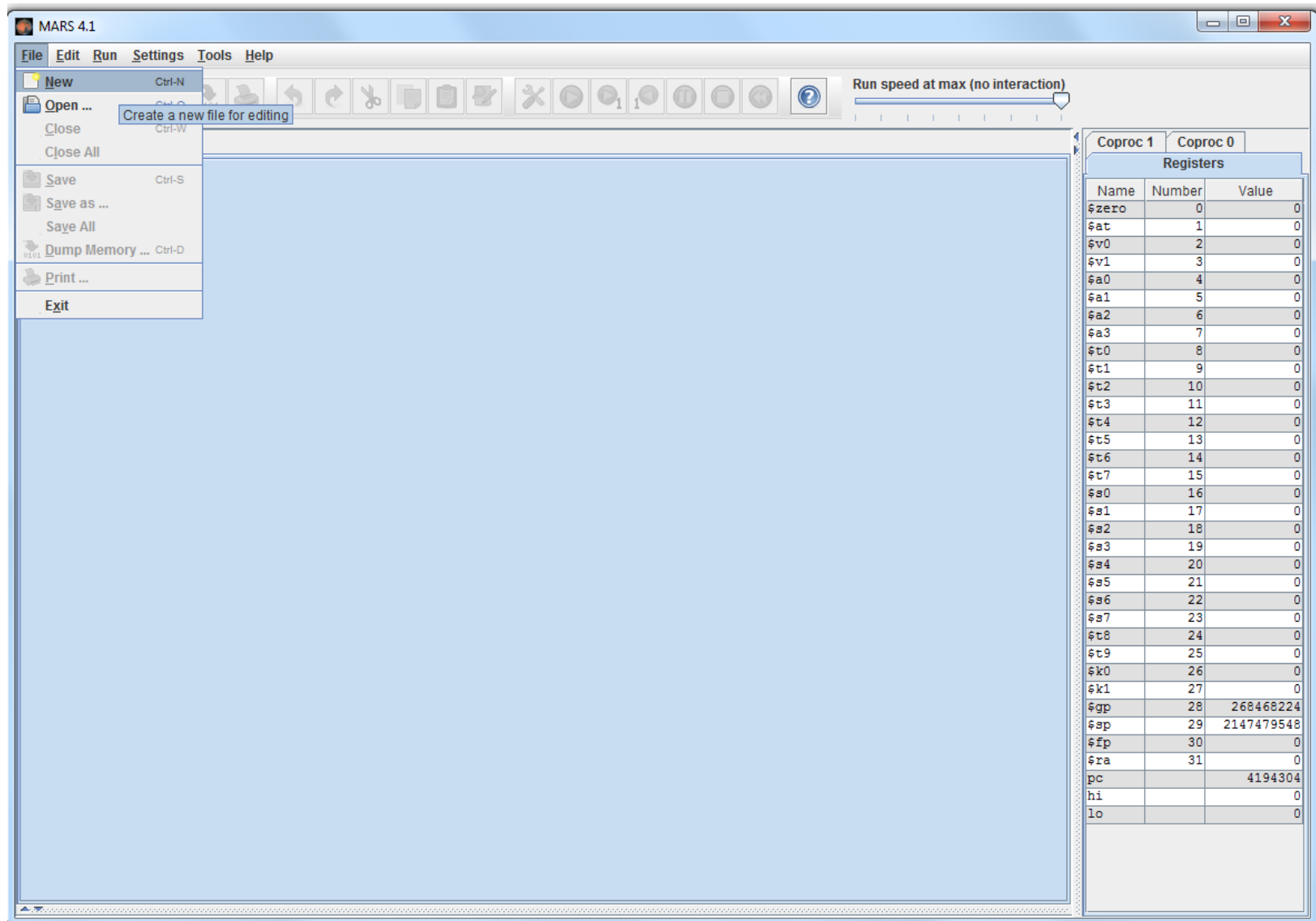
<http://courses.missouristate.edu/kenvollmar/mars/>

Download MARS

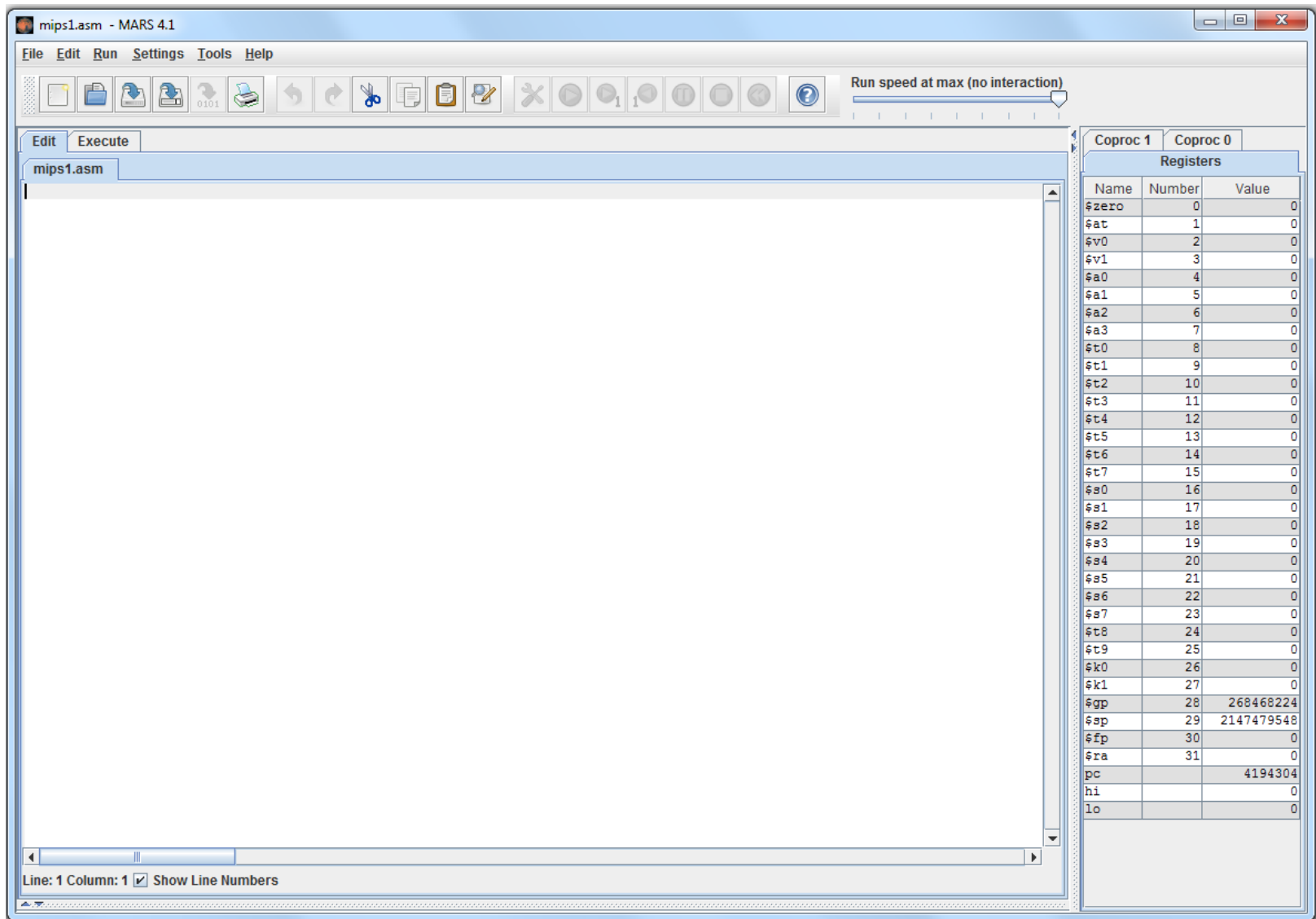
MARS



New [file] ...



Write the code ...



Save As >>> filename.asm

GA\2016-GEA-usb\All-here-1\Courses\2016-courses\230-2015-S\3. Assembly-AL1-AL6\AS-2-Arithm-(HW4)\DemoCode\L2-arithmetic\1.asm* - MARS 4.1

File Edit Run Settings Tools Help

Run speed at max (no interaction)

Edit Execute

mips1.asm 1.asm*

```
1 # Folder L1/1.asm
2
3 .text           # Informs the assembler that instructions follow
4 .globl main     # Declare as global the label main
5 main:          # Execution starts at main:
6 li $t0, 2       # $t0 = 2
7 li $t1, 3       # $t1 = 3
8 add $t5, $t1, $t0 # $t5 = $t1 + $t0
9 li $v0, 10      # System call for exit (Load code 10)
10 syscall        # Call operating system to perform operation (exit)
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
```

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194304
hi		0
lo		0

Line: 12 Column: 2 ☒ Show Line Numbers

Run the code

Assemble

The screenshot shows the MARS MIPS assembler interface. The main window displays assembly code for a MIPS program. The code includes comments and instructions for adding registers, loading a value, and making a system call. The 'Run' menu is open, showing options like 'Assemble', 'Go', 'Step', 'Backstep', 'Pause', 'Stop', and 'Reset'. The 'Registers' window on the right shows the state of various registers, including \$zero, \$at, \$v0, \$v1, \$a0, \$a1, \$a2, \$a3, \$t0, \$t1, \$t2, \$t3, \$t4, \$t5, \$t6, \$t7, \$s0, \$s1, \$s2, \$s3, \$s4, \$s5, \$s6, \$s7, \$t8, \$t9, \$k0, \$k1, \$gp, \$sp, \$fp, \$ra, pc, hi, and lo.

File Edit Run Settings Tools Help

Assemble F3
Go F7
Step F8
Backstep F9
Pause F11
Stop F12
Reset F12
Clear all breakpoints Ctrl-K
Toggle all breakpoints Ctrl-T

Run speed at max (no interaction)

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194304
hi		0
lo		0

Line: 12 Column: 2 ☒ Show Line Numbers

Go

G:\2016-GEA-usb\All-here-1\Courses\2016-courses\230-2015-S\3. Assembly-AL1-AL6\AS-2-Arithm-(HW4)\DemoCode\L2-arithmetic\1.asm - MARS 4.1

File Edit Run Settings Tools Help

Run speed at max (no interaction)

Run the current program

Basic

Address	Source
6: \$0, 2	li \$t0, 2 # \$t0 = 2
7: \$0, 3	li \$t1, 3 # \$t1 = 3
8: \$9, \$8	add \$t5, \$t1, \$t0 # \$t5 = \$t1 + \$t0
9: \$0, 10	li \$v0, 10 # System call for exit (Load cod...
10:	syscall # Call operating system to perfo...

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+12)	Value (+16)	Value (+20)	Value (+24)	Value (+28)
268500992	0	0	0	0	0	0	0	0
268501024	0	0	0	0	0	0	0	0
268501056	0	0	0	0	0	0	0	0
268501088	0	0	0	0	0	0	0	0
268501120	0	0	0	0	0	0	0	0
268501152	0	0	0	0	0	0	0	0
268501184	0	0	0	0	0	0	0	0
268501216	0	0	0	0	0	0	0	0
268501248	0	0	0	0	0	0	0	0
268501280	0	0	0	0	0	0	0	0
268501312	0	0	0	0	0	0	0	0
268501344	0	0	0	0	0	0	0	0
268501376	0	0	0	0	0	0	0	0
268501408	0	0	0	0	0	0	0	0

0x10010000 (.data) ☐ Hexadecimal Addresses ☐ Hexadecimal Values ☐ ASCII

Coproc 1 Coproc 0

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194304
hi		0
lo		0

The result

The output... **uncheck for decimal results**

G:\2016-GEA-usb\All-her-1\Courses\2016-courses\230-2015-S\3. Assembly-AL1-AL6\AS-2-Arithm-(HW4)\DemoCode\L2-arithmetic\1.asm - MARS 4.1

File Edit Run Settings Tools Help

Run speed at max (no interaction)

Execute

Text Segment

Bkpt	Address	Code	Basic	Source
	4194304	0x24080002	addiu \$8,\$0,2	6: li \$t0, 2 # \$t0 = 2
	4194308	0x24090003	addiu \$9,\$0,3	7: li \$t1, 3 # \$t1 = 3
	4194312	0x01286820	add \$13,\$9,\$8	8: add \$t5, \$t1, \$t0 # \$t5 = \$t1 + \$t0
	4194316	0x2402000a	addiu \$2,\$0,10	9: li \$v0, 10 # System call for exit (Load cod...
	4194320	0x0000000c	syscall	10: syscall # Call operating system to perfo...

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+12)	Value (+16)	Value (+20)	Value (+24)	Value (+28)
268500992	0	0	0	0	0	0	0	0
268501024	0	0	0	0	0	0	0	0
268501056	0	0	0	0	0	0	0	0
268501088	0	0	0	0	0	0	0	0
268501120	0	0	0	0	0	0	0	0
268501152	0	0	0	0	0	0	0	0
268501184	0	0	0	0	0	0	0	0
268501216	0	0	0	0	0	0	0	0
268501248	0	0	0	0	0	0	0	0
268501280	0	0	0	0	0	0	0	0
268501312	0	0	0	0	0	0	0	0
268501344	0	0	0	0	0	0	0	0
268501376	0	0	0	0	0	0	0	0
268501408	0	0	0	0	0	0	0	0

0x10010000 (.data) ☐ Hexadecimal Addresses ☐ Hexadecimal Values ☐ ASCII

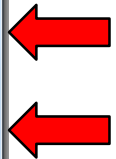
Coproc 1 Coproc 0

Registers

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	10
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	2
\$t1	9	3
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	5
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194324
hi		0
lo		0



uncheck



Our first assembly demo program

```
# Folder L1/1.asm
```

```
.text
```

```
.globl main
```

```
main:
```

```
li    $t0, 2
```

```
li    $t1, 3
```

```
add   $t5, $t1, $t0
```

```
li    $v0, 10
```

```
syscall
```

System Call: 10

Registers	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	0
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	0
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194304
hi		0
lo		0

Our first assembly demo program

The diagram shows an assembly program with the following code and annotations:

```
1.as .
1  # Folder L1/1.asm
2
3      .text
4      .globl main
5  main:
6      li      $t0, 2
7      li      $t1, 3
8      add     $t5, $t1, $t0
9      li      $v0, 10
10     syscall
```

Annotations:

- Comments:** Points to the line `# Folder L1/1.asm`.
- Assembly directives:** Points to the lines `.text` and `.globl main`.
- Label:** Points to the label `main:` on line 5.
- Opcode:** Points to the instruction `li` on line 6.
- Operand:** Points to the register and immediate value `$t0, 2` on line 6.

Additional comments on the right side of the code:

- `#` Informs the assembler that instructions follow
- `#` Declare as global the label main
- `#` Execution starts at main:
- `#` \$t0 = 2
- `#` \$t1 = 3
- `#` \$t5 = \$t1 + \$t0
- `#` System call for exit (Load code 10)
- `#` Call operating system to perform operation (exit)

`li` = LOAD IMMEDIATE, is a pseudo-instruction; will talk about it in the next lecture

Comments and Labels

- **Comments:** Text following a '#' (sharp) to the end of the line is ignored
- **Labels:** Are symbols that represent memory addresses
 - Labels take on the values of the address where they are declared
 - Labels declarations appear at the beginning of a line, and are terminated by a colon (:

.text and .globl directives

- .text directive
 - Defines the section of a program containing instructions
- .globl main
 - Declares main as global
- main: Label that represents a memory address.

```
.text
.globl main
main:
    li    $t0, 2
    li    $t1, 3
    add   $t5, $t1, $t0
    li    $v0, 10
    syscall
```


A Breakdown of Segment and Linker Directives

Name	Parameters	Description
<code>.data</code>	<i>addr</i>	The following items are to be assembled into the data segment. By default, begin at the next available address in the data segment. If the optional argument <i>addr</i> is present, then begin at <i>addr</i> .
<code>.text</code>	<i>addr</i>	The following items are to be assembled into the text segment. By default, begin at the next available address in the text segment. If the optional argument <i>addr</i> is present, then begin at <i>addr</i> . In SPIM, the only items that can be assembled into the text segment are instructions and words (via the <code>.word</code> directive).
<code>.kdata</code>	<i>addr</i>	The kernel data segment. Like the data segment, but used by the Operating System.
<code>.ktext</code>	<i>addr</i>	The kernel text segment. Like the text segment, but used by the Operating System.
<code>.extern</code>	<i>sym size</i>	Declare as global the label <i>sym</i> , and declare that it is <i>size</i> bytes in length (this information can be used by the assembler).
<code>.globl</code>	<i>sym</i>	Declare as global the label <i>sym</i> .

li *des, const* # load the constant *const* into *des*

li *\$t0, 2*

li *\$t1, 3*

Op	Operands	Description
○ la	<i>des, addr</i>	Load the address of a label.
lb(u)	<i>des, addr</i>	Load the byte at <i>addr</i> into <i>des</i> .
lh(u)	<i>des, addr</i>	Load the halfword at <i>addr</i> into <i>des</i> .
○ li	<i>des, const</i>	Load the constant <i>const</i> into <i>des</i> .
lui	<i>des, const</i>	Load the constant <i>const</i> into the upper halfword of <i>des</i> , and set the lower halfword of <i>des</i> to 0.
lw	<i>des, addr</i>	Load the word at <i>addr</i> into <i>des</i> .
lwl	<i>des, addr</i>	
lwr	<i>des, addr</i>	
○ ulh(u)	<i>des, addr</i>	Load the halfword starting at the (possibly unaligned) address <i>addr</i> into <i>des</i> .
○ ulw	<i>des, addr</i>	Load the word starting at the (possibly unaligned) address <i>addr</i> into <i>des</i> .

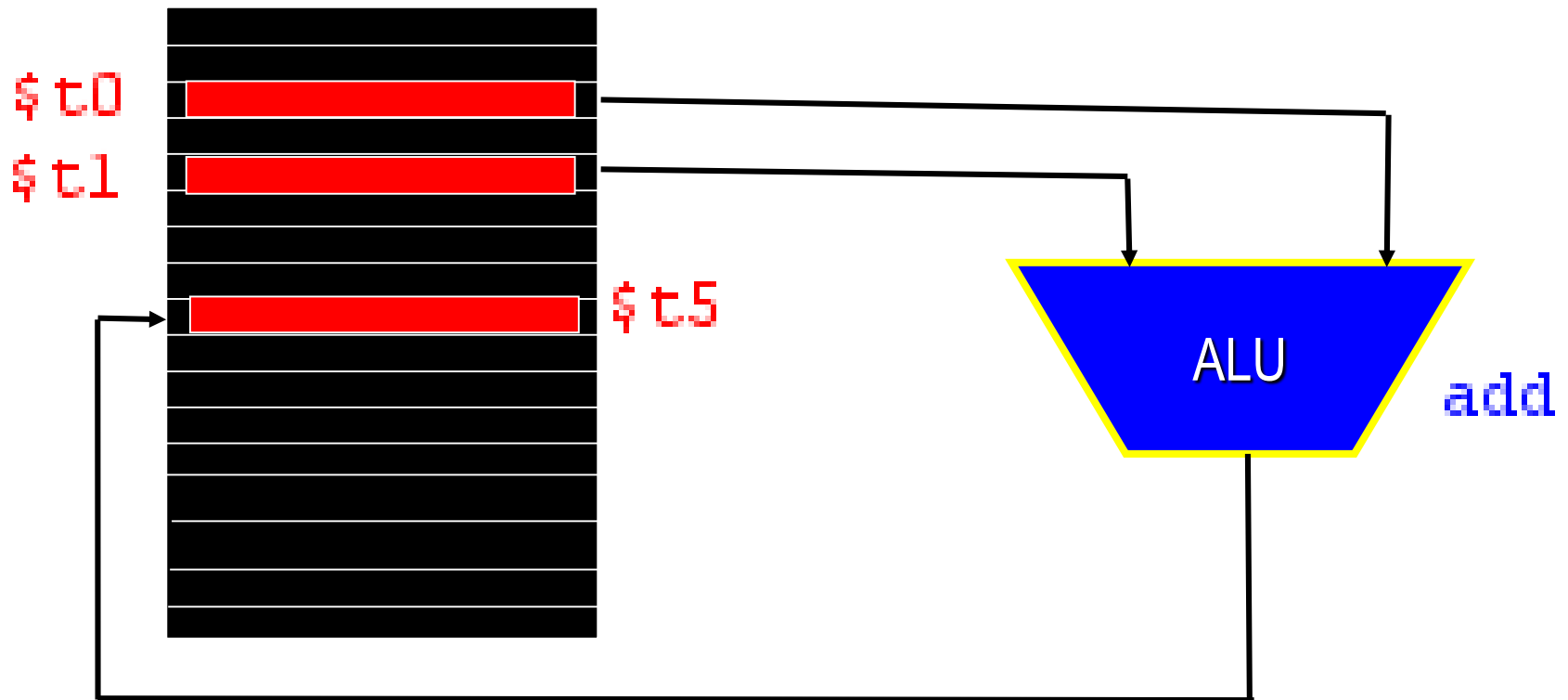
Assemble ...and ... GO

\$t0	8	2
\$t1	9	3
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	5
\$t6	14	0
\$t7	15	0

Registers	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	10
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	2
\$t1	9	3
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	5
\$t6	14	0
\$t7	15	0
\$s0	16	0
\$s1	17	0
\$s2	18	0
\$s3	19	0
\$s4	20	0
\$s5	21	0
\$s6	22	0
\$s7	23	0
\$t8	24	0
\$t9	25	0
\$k0	26	0
\$k1	27	0
\$gp	28	268468224
\$sp	29	2147479548
\$fp	30	0
\$ra	31	0
pc		4194324
hi		0
lo		0

[32] 32-bit RegisterFile + ALU

add \$t5, \$t1, \$t0



Instructions are divided into three kinds of format

- (**R**, **I** and **J** format)
 - **Register** arithmetic instructions (**R**-format)
 - Memory **Immediate** load and store (**I**-format)
 - Branching and **Jump** instructions (**J**-format).

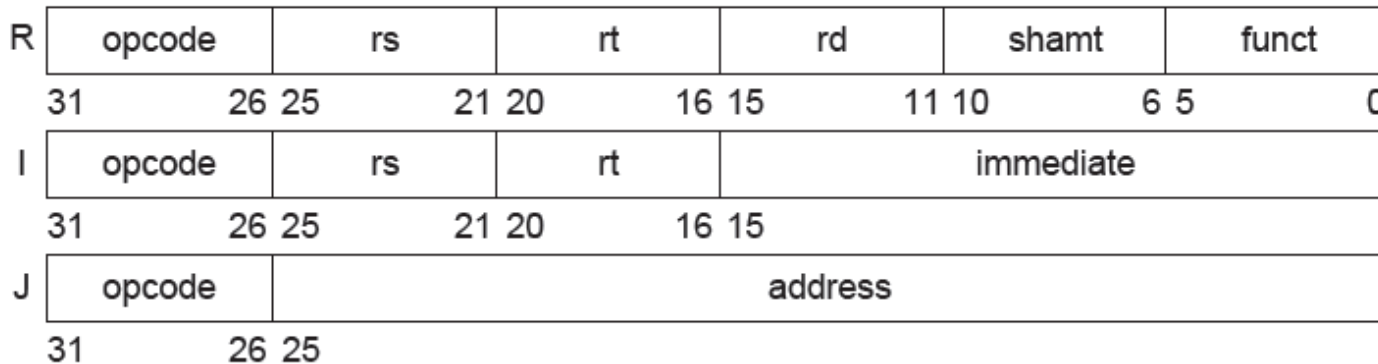
MIPS instruction format (Basic)

Basic instruction formats

R	opcode	rs	rt	rd	shamt	funct
	31	26 25	21 20	16 15	11 10	6 5 0
I	opcode	rs	rt	immediate		
	31	26 25	21 20	16 15		
J	opcode	address				
	31	26 25				

MIPS instruction format (Floating-point)

Basic instruction formats



Floating-point instruction formats

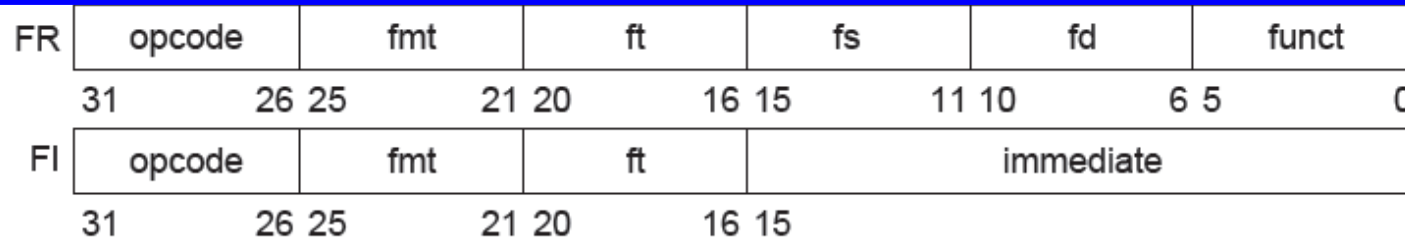


Figure 1.6 MIPS64 instruction set architecture formats. All instructions are 32 bits long. The R format is for integer register-to-register operations, such as DADDU, DSUBU, and so on. The I format is for data transfers, branches, and immediate instructions, such as LD, SD, BEQZ, and DADDIs. The J format is for jumps, the FR format for floating-point operations, and the FI format for floating-point branches.

MIPS instruction format

Format	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	Comments
R	op	rs	rt	rd	shamt	funct	Arithmetic
I	op	rs	rt	address/immediate			Transfer, branch,immediate
J	op	target address					Jump

- **op**: basic operation of instruction
- **funct**: variant of instruction
- **rs**: first register source operand
- **rt**: second register source operand
- **rd**: register destination operand
- **shamt**: shift amount

MIPS **Instruction** set

- Arithmetic, Logic, and Shifting Instructions
- Conditional Branch Instructions
- Load and Store Instructions
- Function Call Instructions.

Example:

Arithmetic

```
add $t5, $t1, $t0
```

Example with **add**

```
1 # Folder L1/1.asm
2
3     .text
4     .globl main
5 main:
6     li      $t0, 2
7     li      $t1, 3
8     add     $t5, $t1, $t0
9     li      $v0, 10
10    syscall
```

li

add

li

syscall

add; signed addition

- Performs the Binary Addition algorithm on two 32-bits;
 - Signed Binary
- `add $t5, $t1, $t0` # `[$t5]=[$t1]+[$t0]`
- Three registers (`$t5`, `$t1`, `$t0`) are involved
- Overflow **trap** is possible

$$\begin{array}{r} 1001 \ 1001 \\ + 0111 \ 0001 \\ \hline 10001 \ 1010 \end{array}$$

- A **trap** is an interruption in the normal machine cycle.

More add instructions

More `add` instructions (MIPS)

- `addu`
- `addiu`

addu ← new instruction

4.4.1 Arithmetic Instructions

Op	Operands	Description
o <code>abs</code>	<i>des, src1</i>	<i>des</i> gets the absolute value of <i>src1</i> .
<code>add(u)</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> + <i>src2</i> .
<code>and</code>	<i>des, src1, src2</i>	<i>des</i> gets the bitwise and of <i>src1</i> and <i>src2</i> .
<code>div(u)</code>	<i>src1, reg2</i>	Divide <i>src1</i> by <i>reg2</i> , leaving the quotient in register <code>lo</code> and the remainder in register <code>hi</code> .
o <code>div(u)</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> / <i>src2</i> .
o <code>mul</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> × <i>src2</i> .
o <code>mulo</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> × <i>src2</i> , with overflow.
<code>mult(u)</code>	<i>src1, reg2</i>	Multiply <i>src1</i> and <i>reg2</i> , leaving the low-order word in register <code>lo</code> and the high-order word in register <code>hi</code> .
o <code>neg(u)</code>	<i>des, src1</i>	<i>des</i> gets the negative of <i>src1</i> .
<code>nor</code>	<i>des, src1, src2</i>	<i>des</i> gets the bitwise logical nor of <i>src1</i> and <i>src2</i> .
o <code>not</code>	<i>des, src1</i>	<i>des</i> gets the bitwise logical negation of <i>src1</i> .
<code>or</code>	<i>des, src1, src2</i>	<i>des</i> gets the bitwise logical or of <i>src1</i> and <i>src2</i> .
o <code>rem(u)</code>	<i>des, src1, src2</i>	<i>des</i> gets the remainder of dividing <i>src1</i> by <i>src2</i> .
o <code>rol</code>	<i>des, src1, src2</i>	<i>des</i> gets the result of rotating left the contents of <i>src1</i> by <i>src2</i> bits.
o <code>ror</code>	<i>des, src1, src2</i>	<i>des</i> gets the result of rotating right the contents of <i>src1</i> by <i>src2</i> bits.
<code>sll</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> shifted left by <i>src2</i> bits.
<code>sra</code>	<i>des, src1, src2</i>	Right shift arithmetic.
<code>srl</code>	<i>des, src1, src2</i>	Right shift logical.
<code>sub(u)</code>	<i>des, src1, src2</i>	<i>des</i> gets <i>src1</i> - <i>src2</i> .
<code>xor</code>	<i>des, src1, src2</i>	<i>des</i> gets the bitwise exclusive or of <i>src1</i> and <i>src2</i> .

`addu`; unsigned addition

- Performs the Binary Addition algorithm on two 32-bits ;
 - Unsigned Binary
- The destination register can be the same as one of the source registers
- `add(u) $t0, $t0, $t1` # $[\$t0] = [\$t0] + [\$t1]$
- `addu` ... ignores overflow trap.

add ... addu

- The **add** instruction is used in the cases that overflow is an important factor. Otherwise we use the **addu** instruction
 - For **signed** numbers, use **add**
 - For **unsigned** numbers, use **addu**.

addiu

← new instruction

addiu ← add immediate unsigned

- **addiu** \$t0, \$t0, 1 # [\$t0] = [\$t0] + 1

constant



(No overflow trap)

addi ← known add instruction

addi (add immediate)

addi \$t2 \$t1 4

addi	\$rt	\$rs	4
001000	01001	01010	000000000000000100
Op Code			Immediate value 4

addi ... add-i mmediate

```
a = b + 4; (10 is decimal)
```

MIPS Code

```
addi $t2,$t1,4
```

```
a = b - 4; -4 is decimal)
```

MIPS Code

```
addi $t2,$t1,-4
```

Example with **addi**

addi

2.asm*

```
1 # Folder L1/2.asm
2
3     .text
4     .globl main
5 main:
6     li      $t0, 2
7     addi    $t5, $t0, 3
8     li      $v0, 10
9     syscall
10
```

addi

```
main:      .text
           .globl main
           # Informs the assembler that instructions follow
           # Declare as global the label main
           # Execution starts at main:
           # $t0 = 2
           # $t5 = $t0 + 3
           # System call for exit (Load code 10)
           # Call operating system to perform operation (exit)
           li      $t0, 2
           addi     $t5, $t0, 3
           li      $v0, 10
           syscall
```

Assemble ... GO

```
1 # Folder L1/2.asm
2
3     .text
4     .globl main
5 main:
6     li      $t0, 2
7     addi    $t5, $t0, 3
8     li      $v0, 10
9     syscall
10
```

\$t0	8	2
\$t1	9	0
\$t2	10	0
\$t3	11	0
\$t4	12	0
\$t5	13	5
\$t6	14	0
\$t7	15	0

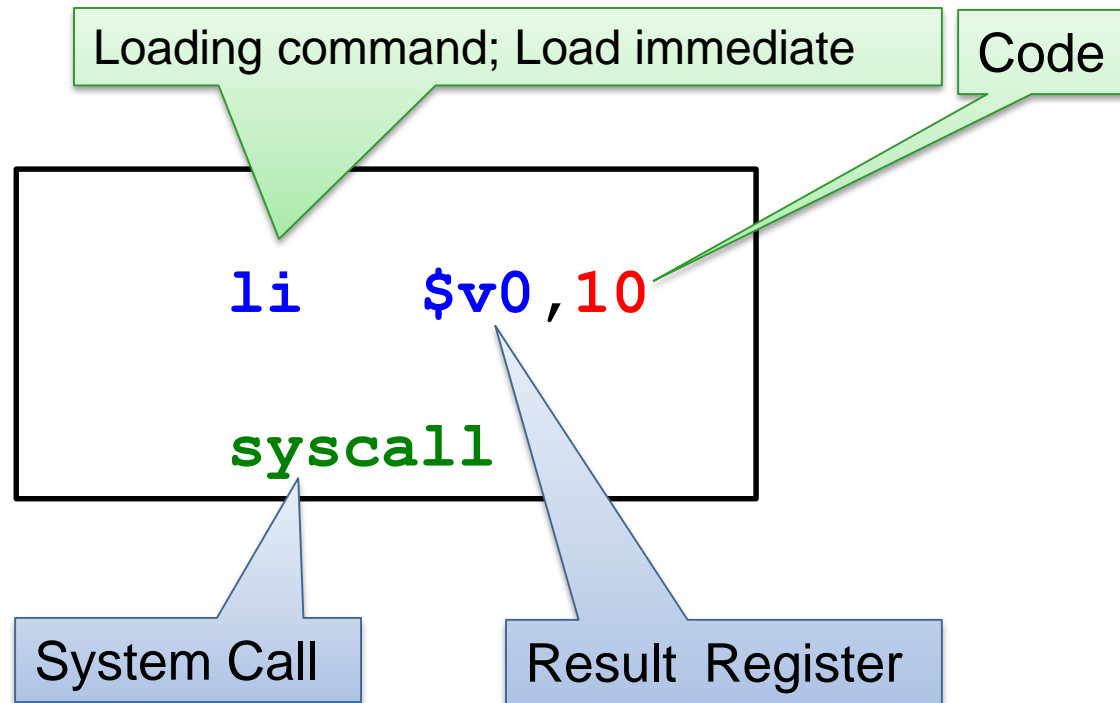
li (**l**oad **i**mmEDIATE)

Another immediate instruction

li (load immediate)

- `li $v0, 10` # load immediate `$v0` = 10
- `Syscall` # instruction; action depends on code loaded in the register: `$v0`

Load 10 into \$v0; ... terminate



- A system call starts off by loading a specific code into the Result Register
- Then, the `syscall` instruction is called. The final result depends on the code loaded into the Result register
- The above example is the exit `syscall`, since loading the code "10" and calling the "`syscall`" instruction terminates the program.

Example-1

Class examples

1. Add three numbers ...

- **1 + 3 + 4**
- add the above numbers using only the instructions:

add and **li**

5 minutes...

In Class

Registers
Name
\$zero
\$at
\$v0
\$v1
\$a0
\$a1
\$a2
\$a3
\$t0
\$t1
\$t2
\$t3
\$t4
\$t5
\$t6
\$t7
\$s0
\$s1
\$s2
\$s3
\$s4
\$s5
\$s6
\$s7
\$t8
\$t9

Program/Solution

```
.text
.globl main
main:
    li    $t0,1           # $t0 = 1
    li    $t1,3           # $t1 = 3
    li    $t2,4           # $t2 = 4
    add   $t6,$t1,$t0      # $t6 = 4
    add   $t7,$t6,$t2      # $t7 = 8

    li    $v0,10          # Exit (code 10)
    syscall
```

Assemble ... GO



Registers	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	10
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	1
\$t1	9	3
\$t2	10	4
\$t3	11	0
\$t4	12	0
\$t5	13	0
\$t6	14	4
\$t7	15	8

Example-2

2. New problem: Add three numbers ...

- $1 + 3 + 4$
- add the above numbers using only the instructions:

addi and **li**

5 minutes...

In class

Registers	
Name	
\$zero	
\$at	
\$v0	
\$v1	
\$a0	
\$a1	
\$a2	
\$a3	
\$t0	
\$t1	
\$t2	
\$t3	
\$t4	
\$t5	
\$t6	
\$t7	
\$s0	
\$s1	
\$s2	
\$s3	
\$s4	
\$s5	
\$s6	
\$s7	
\$t8	
\$t9	

Solution

```
.text
.globl main
main:
    li    $t0, 1
    addi  $t1, $t0, 3
    addi  $t2, $t1, 4

    li    $v0, 10
    syscall
```

Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	10
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	1
\$t1	9	4
\$t2	10	8
\$t3	11	0

Example-3

3. New problem: Add three numbers ...

- $1 + 3 + 4$
- add the above numbers using only the instructions:

addi and **li**

... use only one register (**\$t0**)

5 minutes...

In Class

Add three numbers ... using **addi**

Paul Kelusak, S2015

```
.text
.globl main

main:
    li    $t0, 1
    addi   $t0, $t0, 3
    addi   $t0, $t0, 4

    li    $v0, 10
    syscall
```

Registers	Coproc 1	Coproc 0
Name	Number	Value
\$zero	0	0
\$at	1	0
\$v0	2	10
\$v1	3	0
\$a0	4	0
\$a1	5	0
\$a2	6	0
\$a3	7	0
\$t0	8	8
\$t1	9	0