In this CAD assignment, a CMOS rising edge triggered flip-flop with an asynchronous reset was designed using 45 nm static CMOS technology. The D flip-flop was designed with 3 inputs data (D), clock (Clk), and reset and one output (Q) in Cadence Virtuoso. The schematic was designed as shown in figure 1. To design the d flip flop, the schematics and layout of the transmission gate, NAND gate, tristate inverter, tristate NAND gate were created. Those cells were used in the d flip flop schematic. There were two additional inverters included in the schematic to obtain the clock and clock bar signals. The output of the first inverter was used internally in the D flip-flop schematic for the clock bar signal. The second inverter output was used for the clock signal. The d flip flop symbol was created seen in figure 2.

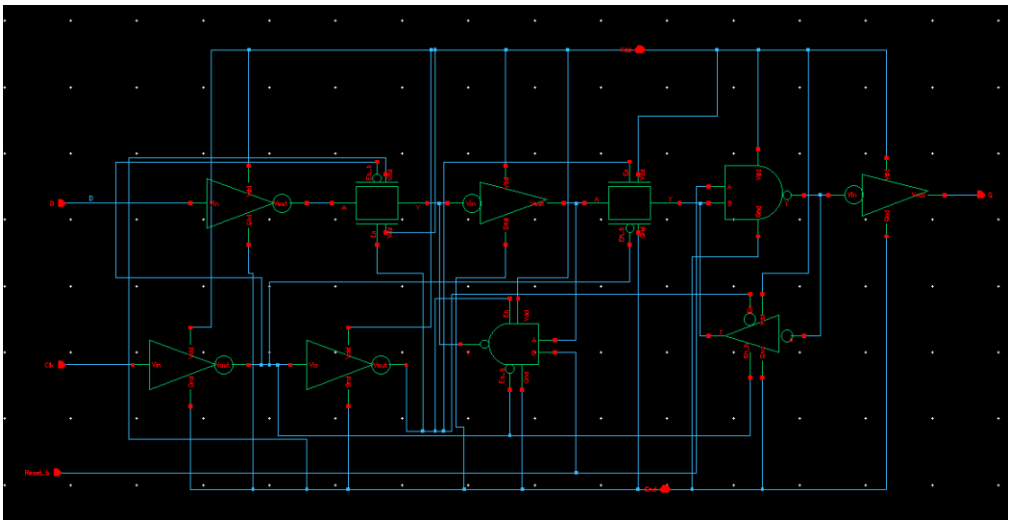

Figure 1 D flip-flop schematic

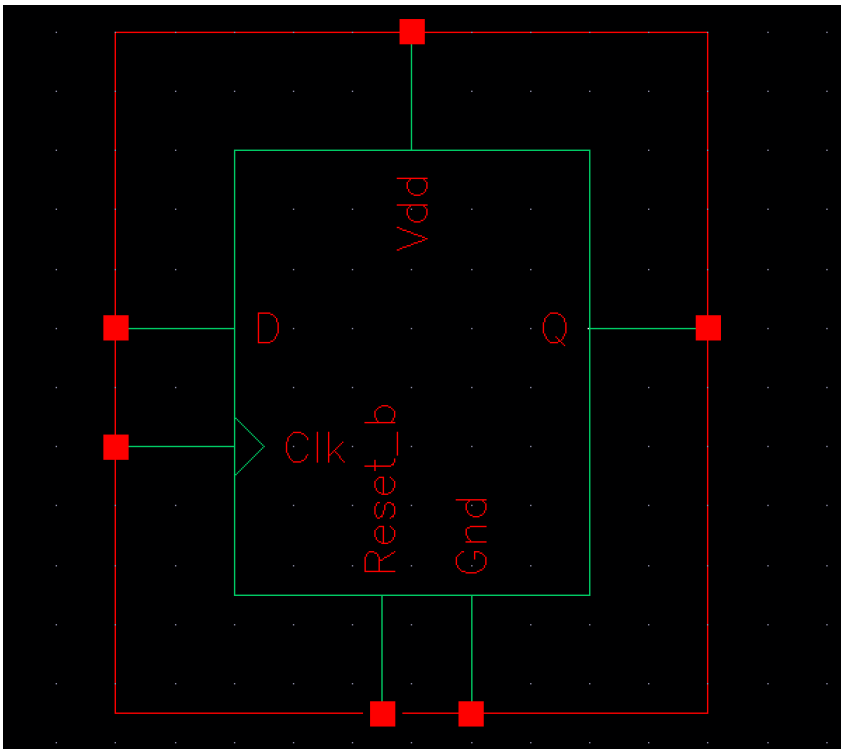

Figure 2 D flip-flop symbol

To test the D flip-flop, transient and DC analyses were completed using Spectre in the ADE Explorer. The D flip-flop was first tested to confirm it could drive an external load of 5 fF. Figure 3 shows that one flip flop could drive a 5 fF load. The supply voltage for the simulation was 1.1 V. The rise and fall times of the input data and clock signal were set to 20 ps each. The data path stated in the CAD assignment was created in the test cell for the flip-flop shown in figure 4. The data for the first flip flop was configured to run at 1/10 the clock frequency programmatically by adding step sizes for the clock signal, a variable for the clock signal (named "f_clk"), a variable for the data (named "f_data") as the input value for the schematic. f_data was set to f_clk/10. The simulation time was set for 5 clock periods of the data signal by setting it to 5 * 1/f_clk. f_clk was set to step between the values "2e9:1e9:10e9".

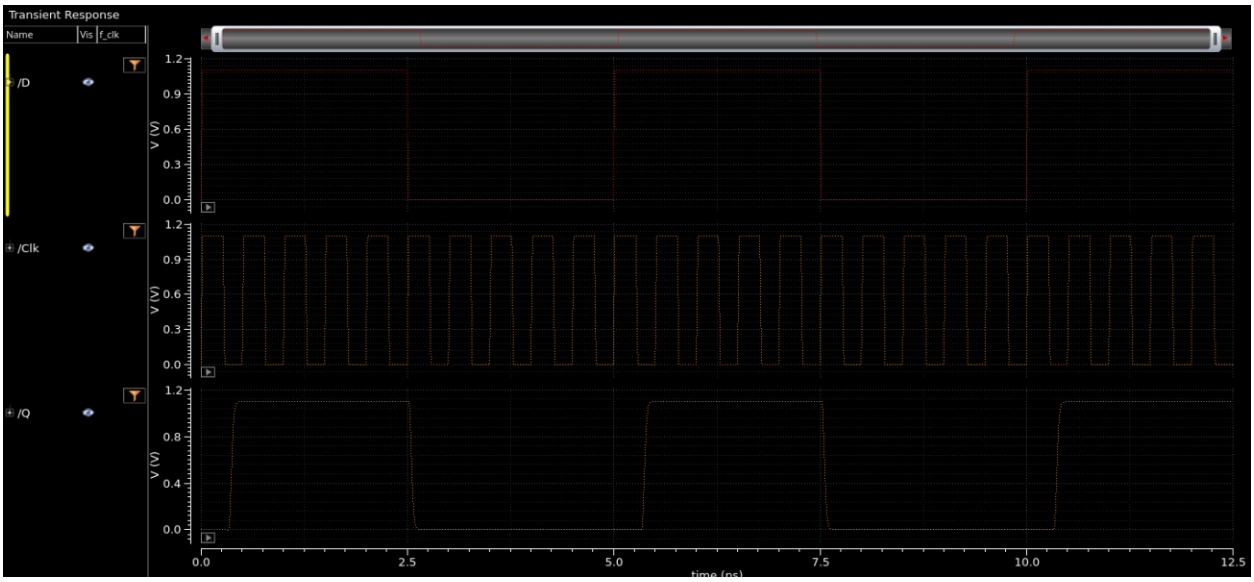

Figure 3 D flip-flop 5 fF load transient response simulation

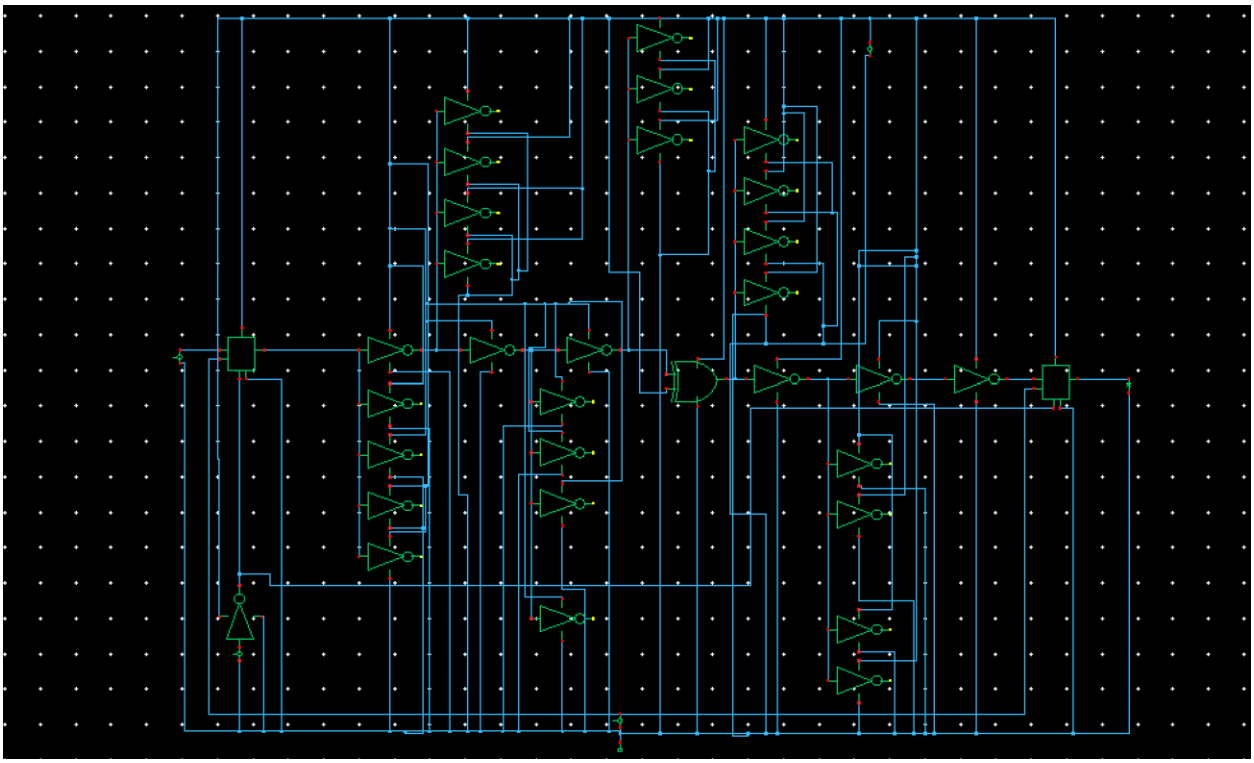

Figure 4 Data path for testing D flip-flop

Figure 5 shows that the data path works at a minimum of 2 GHz clock signal (a 200 MHz data signal) with a 5 fF load. The data and clock frequencies were iteratively increased to determine the maximum frequency with which the data path can operate. The first rising clock edge, D was latched by the first d flip flop. It propagates through the combinational logic to then be latched by the second D flip-flop during the second rising clock edge at 2 GHz. The maximum clock frequency appeared to be frequencies over 7 GHz due to the second flip flop nearly failing to latch to the input signal after this frequency seen in figure 6. This shows that the data path suffered max delay constraint violations at frequencies after 7 GHz. Figure 7 shows an example of a max delay constraint violation at 10 GHz. Figures 5 and 6 also verify the asynchronous reset functionality as the reset occurs outside of the rising clock edge and pulls the output to 0 (shown in net 9).

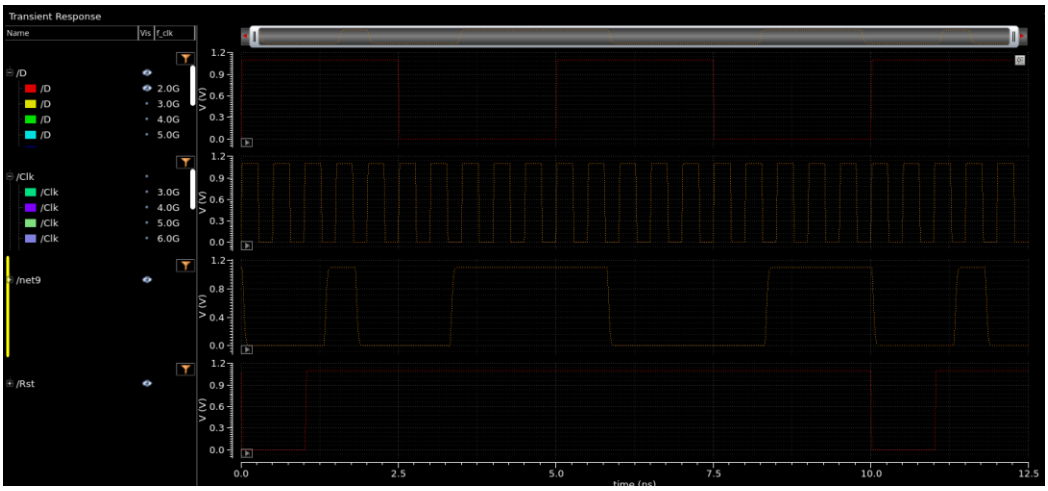

Figure 5 Verification of data path for a 2 GHz clock with a 5 fF load capacitance

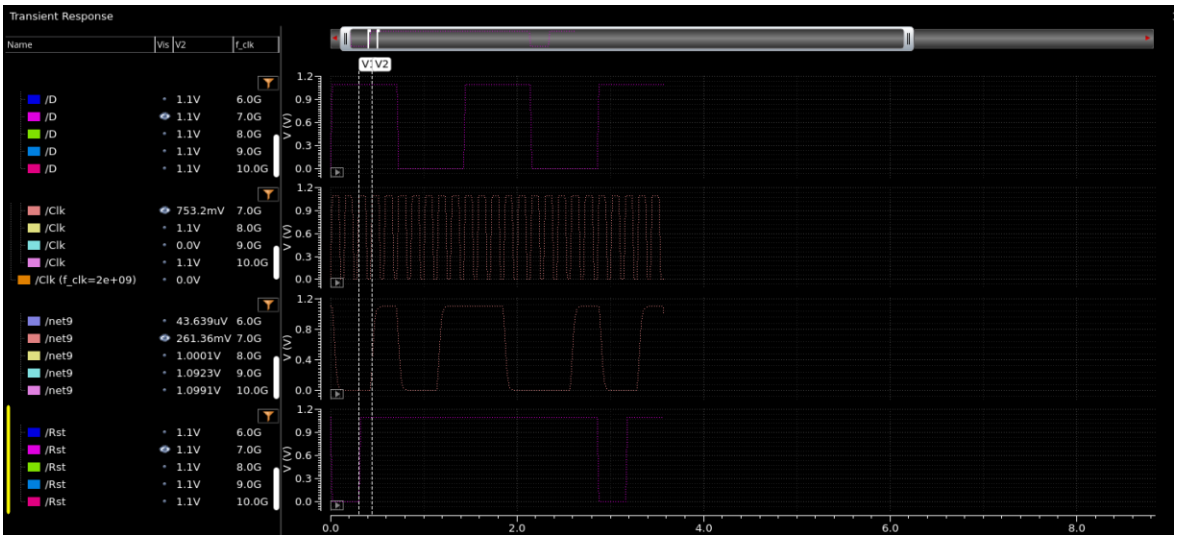

Figure 6 Maximum frequency graph

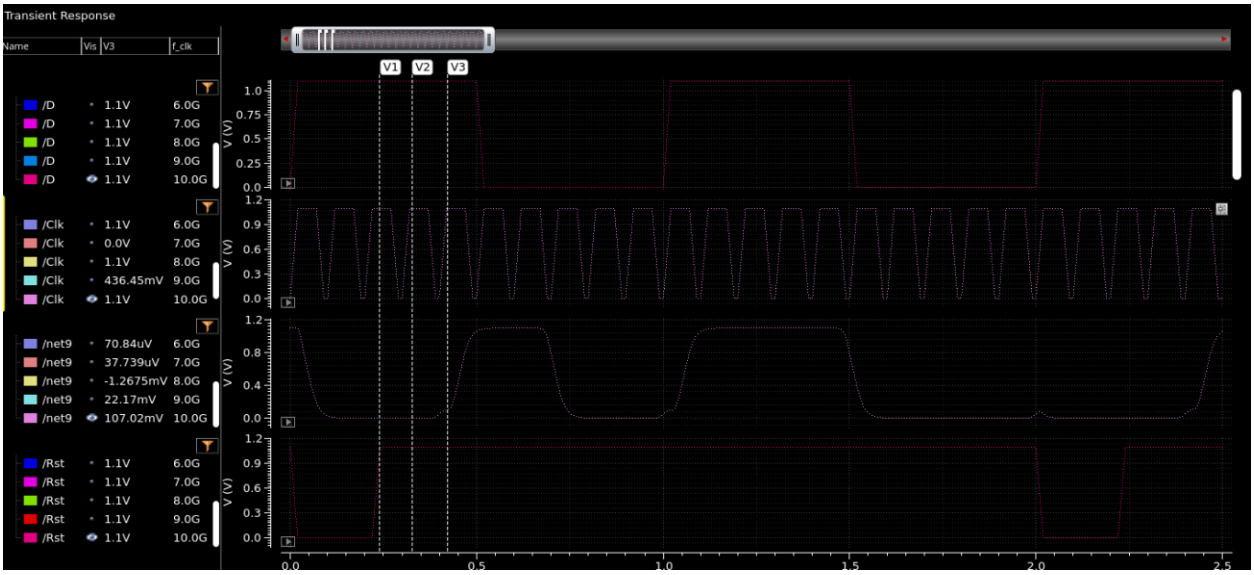

Figure 7 Example of max delay constraint violation at 10 GHz clock frequency

Figure 8 further shows the functionality of the asynchronous reset. The reset signal was set to 0 to verify functionality. When the value of the reset signal was set to zero, the output was 0 as well. This is due to the reset signal of the flip flop being an active low signal that is internally produced by the flip flip therefore the vpulse signal in the test is set to 0V to initiate

the reset.

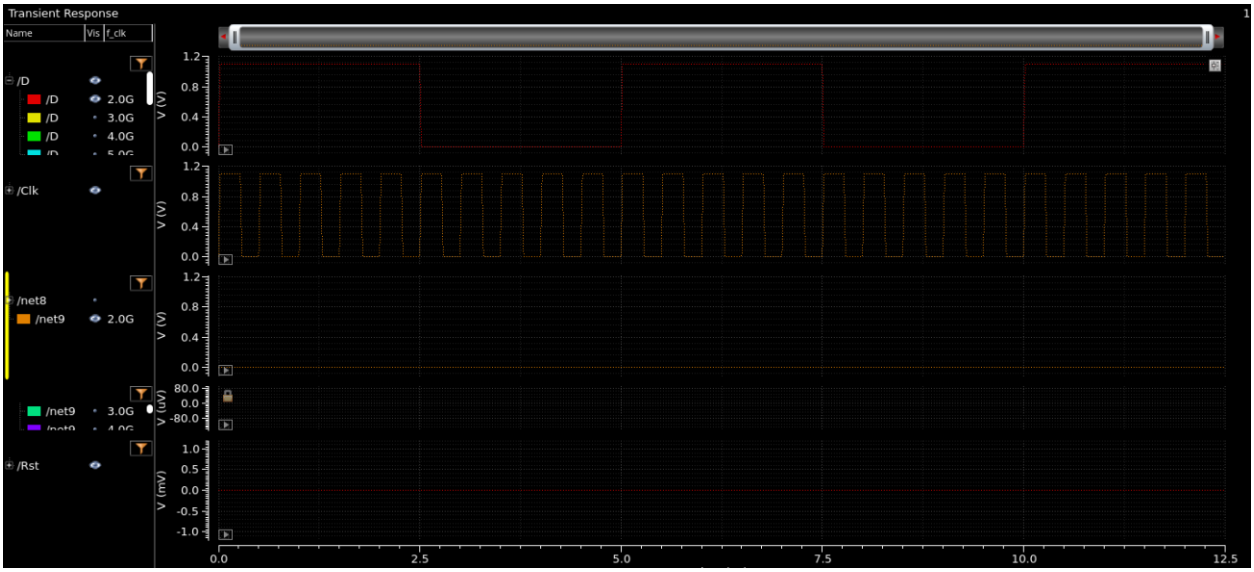

Figure 8 Reset functionality verification

After the verification of the operation of the D flip-flop, the layout of the cell was completed, shown in figure 9. Figures 10 and 11 show the passing DRC and LVS checks.

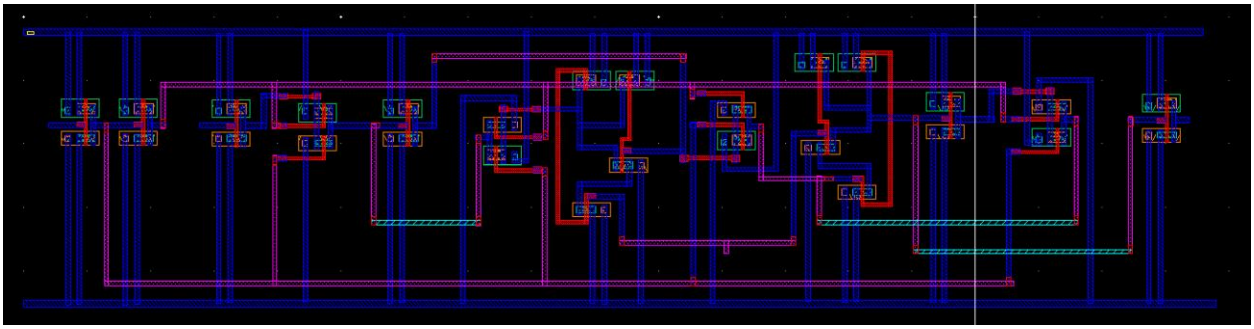

Figure 9 Layout of D flip-flop

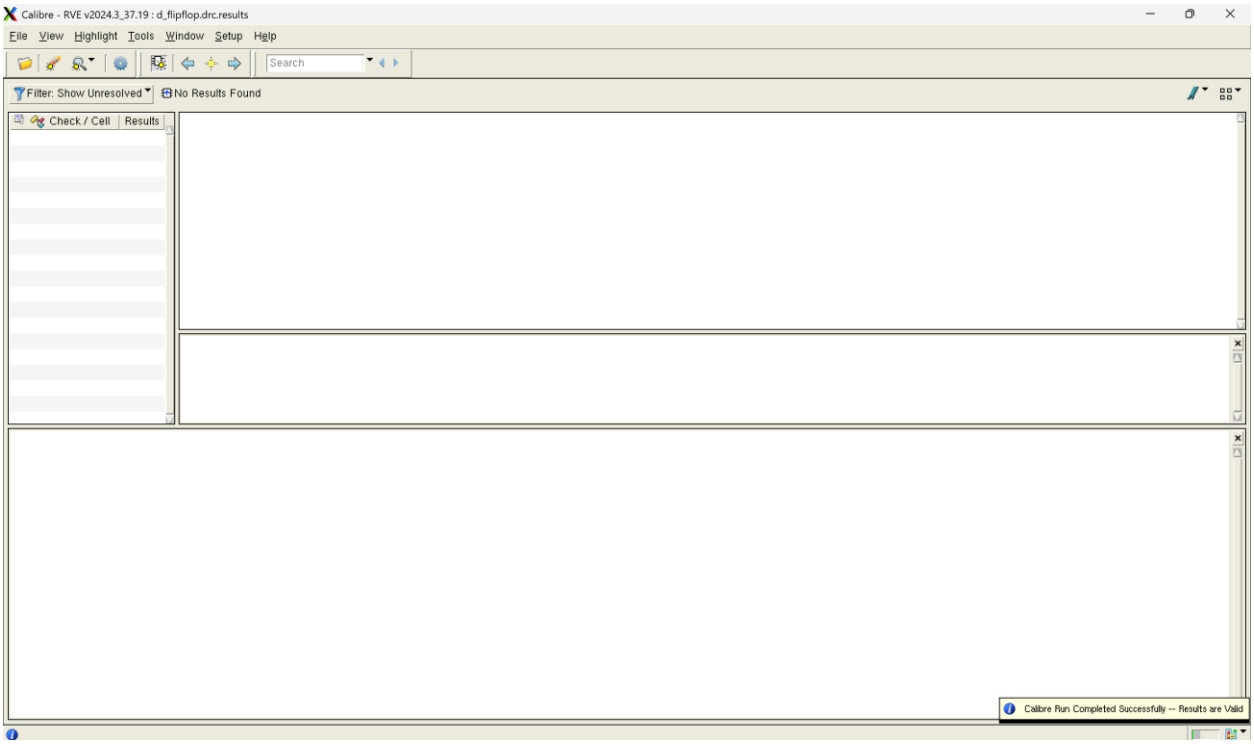

Figure 10 Passing DRC check

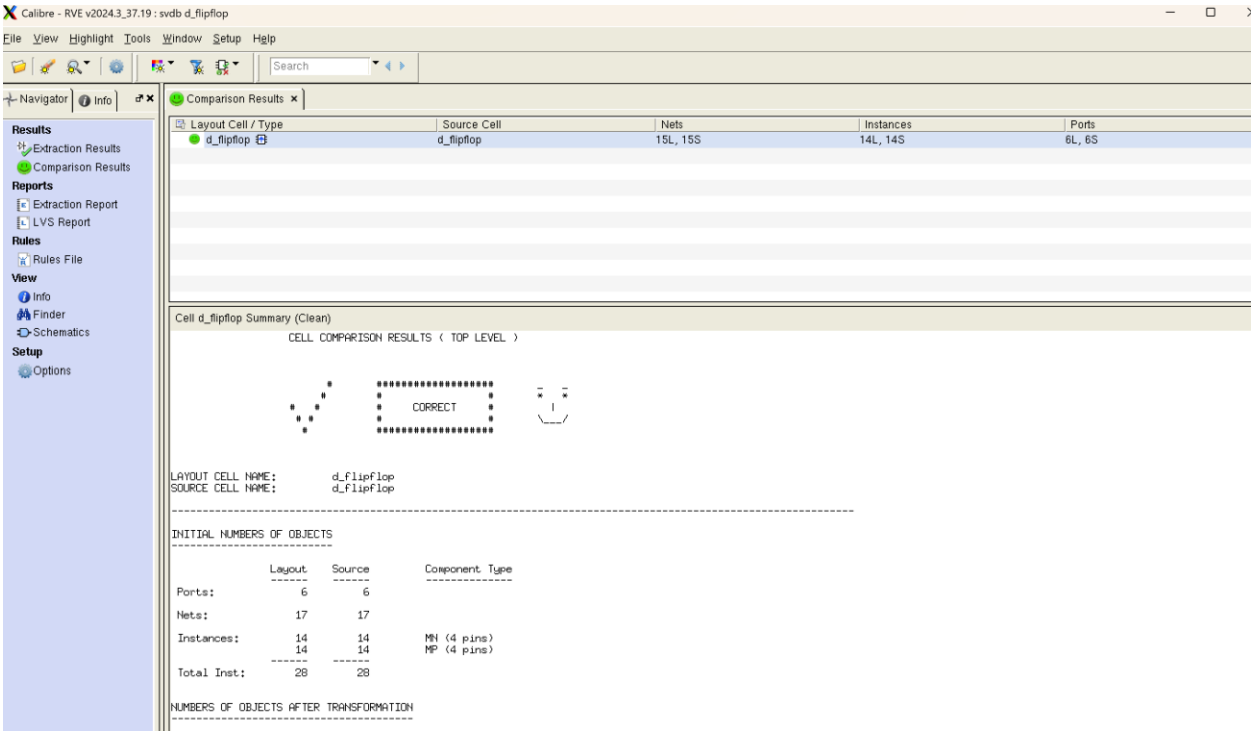

Figure 11 Passing LVS check

Post-layout simulations using HSpice were completed to view the Clock-to-Q delay for latching logic-low and latching logic-high were completed. To measure the Clock-to-Q delay the measurement tool in Synopsys WaveView was used. The Clk and Q signals were selected to measure the delay starting at 50% of the rise and fall times of the signals. The outputs of the HSpice simulation are shown in figure 12 with markers for the Clock-to-Q delay for the latching logic-low and logic-high. The Clock-to-Q delay was 989 ps for latching low logic and 440 ps for latching high logic.

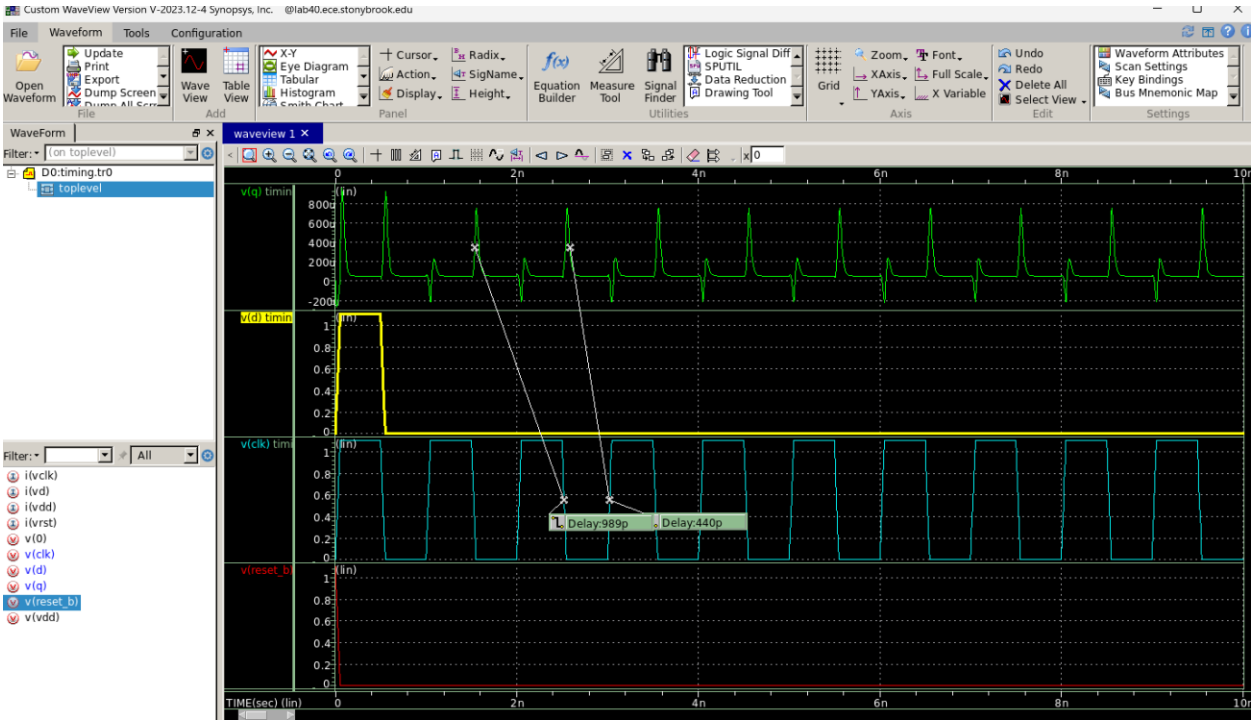

Figure 12 WaveView output of HSpice simulation with Clk-to-Q Delay markers for latching high and low logic