The one stage amplifier shown in the project document was created in Cadence Virtuoso. The annotated schematic is shown in figure 1. A symbol was created of the schematic and used in a test cell to complete transient and DC analysis of the amplifier.

The biasing voltage of V_b was set to 1.2116V in order for I_{D5} to be 40µA in the test cell by solving the following:

$$I_{D5} = \frac{1}{2} k_n \frac{W_5}{L_5} \left(V_{GS5} - V_{th,n}\right)^2 (1 + \lambda_{n5} V_{DS5})$$

$$V_{ov} = V_{GS5} - V_{th,n} = \sqrt{\frac{2I_{D5}}{k_n \left(\frac{W}{L}\right)_5}} = \sqrt{\frac{2 * 40\mu A}{\left(115 \frac{\mu A}{V^2}\right) \frac{7.2\mu m}{2.4\mu m}}} = 0.4816\ V$$

$$V_B = V_{th,n} - V_{ov} = 0.73 + 0.4816 = 1.2116\ V$$

$V_{in,+}$ and $V_{in,-}$ were connected to a DC voltage source V_{IC} in order to find the DC analysis of the output voltage as the function of V_{IC}. A 1 pf capacitor was added to the output to complete the construction of the test cell. The test cell schematic is shown in figure 2. The range of the voltage V_{IC} where all transistors operate in saturation is 1.194 V to 5V according to the DC analysis plot in figure 3. The calculated voltage range is 1.382V to 4.995V and was found by computing the equations below. The calculated values are within a reasonable range compared to the values obtained from the plot.

$$V_{IC,min} = V_B + \sqrt{\frac{2I_D}{k_n}} = 1.212 + 0.1703 = 1.382\ V$$

$$V_{IC,max} = V_{DD} - \sqrt{\frac{2I_D}{k_p}} + V_{th,n} = 4.2648 + 0.73 = 4.995V$$

The small signal common-mode voltage gain was measured in Virtuoso by computing and graphing the calculator function “deriv(v("/Vout" ?result "dc"))/deriv(v("/net2" ?result "dc"))” where net2 is Vin shown in figure 4. The simulation returned a common-mode voltage gain value of 0.006097. This value was also calculated by computing the following equation.

$$A_{cm} = \frac{V_{OUT}}{V_{IN}} = \frac{g_{m1}}{1 + g_{m1}(2r_{o5})} * \frac{1}{g_{m3}} = 0.0095$$

The calculated and measured values appear consistent because both values are very small.

The differential voltage source v_{id} was connected to $V_{in,+}$ in series with $V_{IC.}$ Both voltage sources were set to 2.5V. v_{id} was swept from -0.25V to 0.25V with a step of 0.001mV. The small signal differential mode voltage gain was measured shown in figure 5. The measured value was 81.50962. The calculated value was approximately 206. The calculated differential mode voltage gain was calculated by doing the following calculation.

$$A_{dm} = \frac{V_{Out}}{V_{id}} = g_{m1}(r_{o1}||r_{o4}) = \frac{2I_D}{V_{ov}}\left(\frac{1}{\lambda_{n1}\frac{I_D}{2}} + \frac{1}{\lambda_{n4}\frac{I_D}{2}}\right) = 206$$

The circuit did produce a high gain, but the discrepancy in the calculated and measured gain may be due to how the sweep was performed for the circuit. Since there was a single ended drive for the voltage performed on the circuit, the gain was reduced from what the maximum potential could be (which would be about double the measured gain) which would be more consistent with the theoretical measurement. The output voltage range was

estimated by computing $V_{out,min}$ and $V_{out,max}$ then finding ΔV_{out}. The output voltage range estimate is 2.8548 V.

$$V_{out,min} = V_{IC} - V_{th,n} = 2.5 - 0.73 = 1.77\ V$$

$$V_{out,max} = V_{G4} + |V_{th,p}| = 5 - 1.6752 + 0.4816 = 4.2648\ V$$

$$\Delta V_{out} = 4.2648 - 1.77 = 2.8548\ V$$

A capacitor of size 50fF was added to the output of the amplifier. AC analysis was done to plot the magnitude and phase of the transfer function of the amplifier shown in figure 6. The measured dominant pole was 2.27 MHz. The location of the dominant pole was calculated by the following equation.

$$f_{p1} = \frac{1}{2\pi R_{out2} C_{out2}} = \frac{1}{2\pi (r_{o2} || r_{o4})(C_{gd1} + C_{bd4} + C_{gd2} + C_L)} = 2.218\ MHz$$

The measured location compared to the calculated one by 2.4% which shows the measurement and calculation are consistent.

The other poles and zeros were calculated by the below equations. The circuit should have 2 poles and 1 zero. The estimated locations of the second pole and the zero are shown on the plot of the magnitude and phase of the transfer function using markers also shown in figure 6, which are 60.31 MHz and 103.157 MHz respectively.

$$f_{p2} = \frac{1}{2\pi R_{out1} C_{out1}} = \frac{g_{m3}}{2\pi (C_{gd1} + C_{bd1} + C_{bd3} + C_{gs3} + C_{gs4})} = 94.3\ MHz$$

$$f_z = \frac{2 g_{m3}}{2\pi (C_{gd1} + C_{bd1} + C_{bd3} + C_{gs3} + C_{gs4})} = 188.6\ MHz$$

Appendix

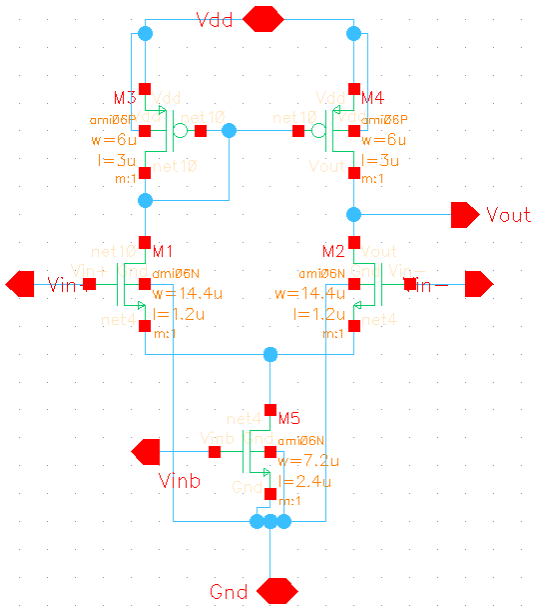

Figure 1 Schematic of One Stage Amplifier

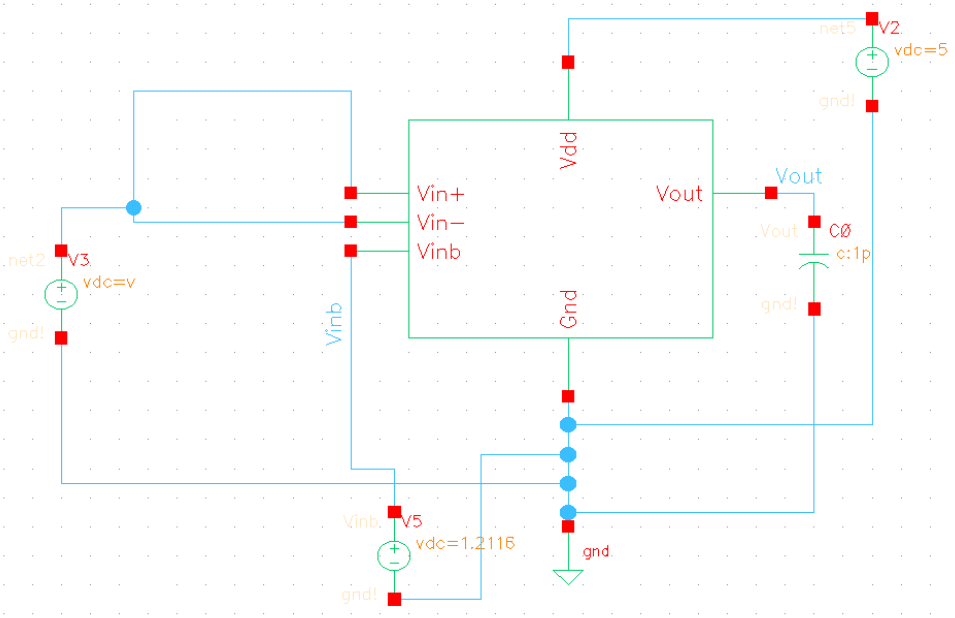

Figure 2 Test cell to calculate Vic

Appendix

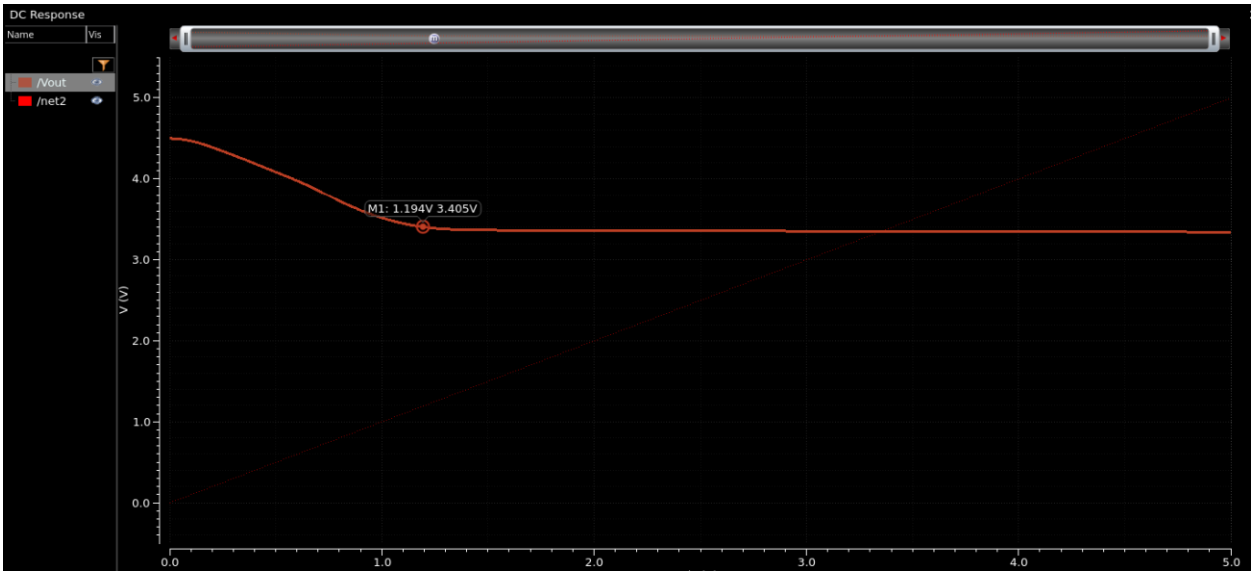

Figure 3 DC Analysis plot of Vout with marker for the beginning of saturation of all transistors

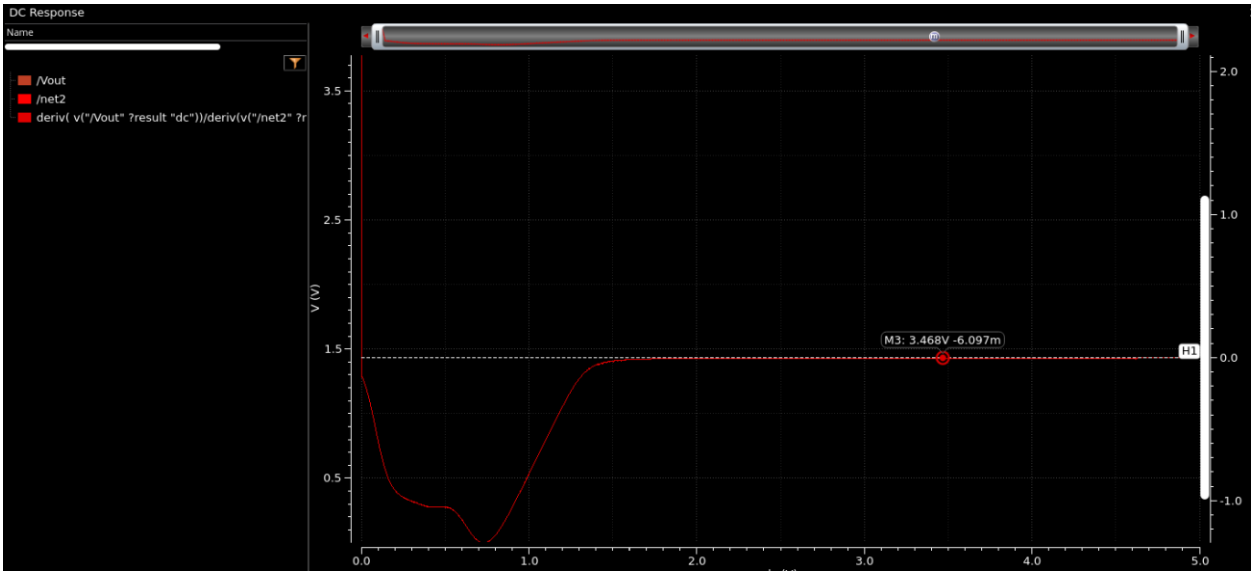

Figure 4 Small signal common mode gain plot

Appendix

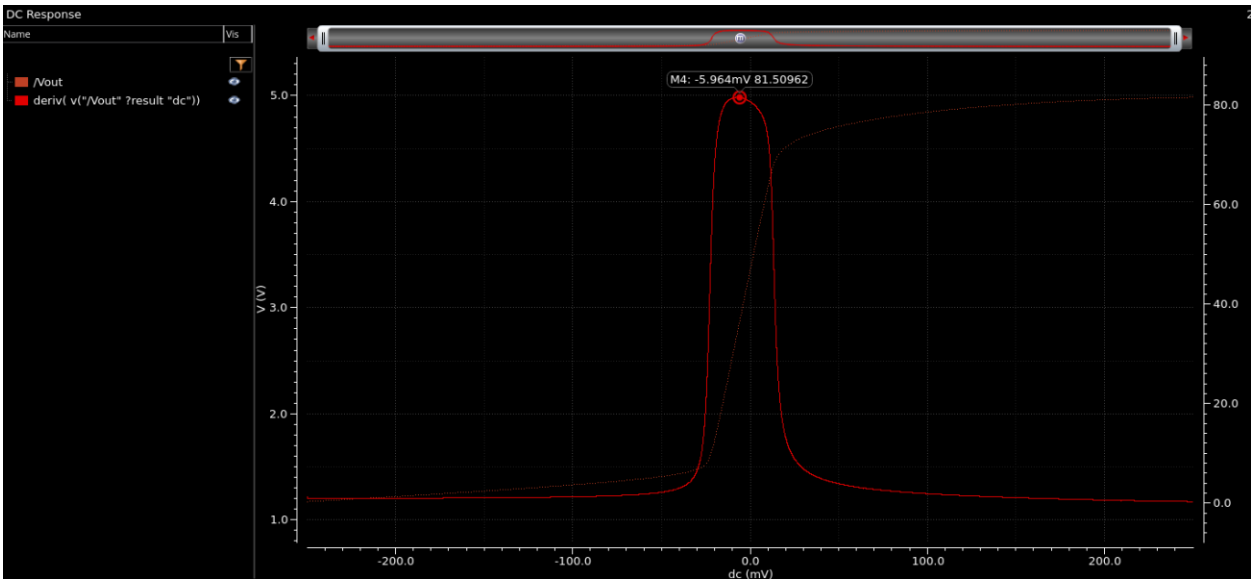

Figure 5 Small signal differential mode gain plot

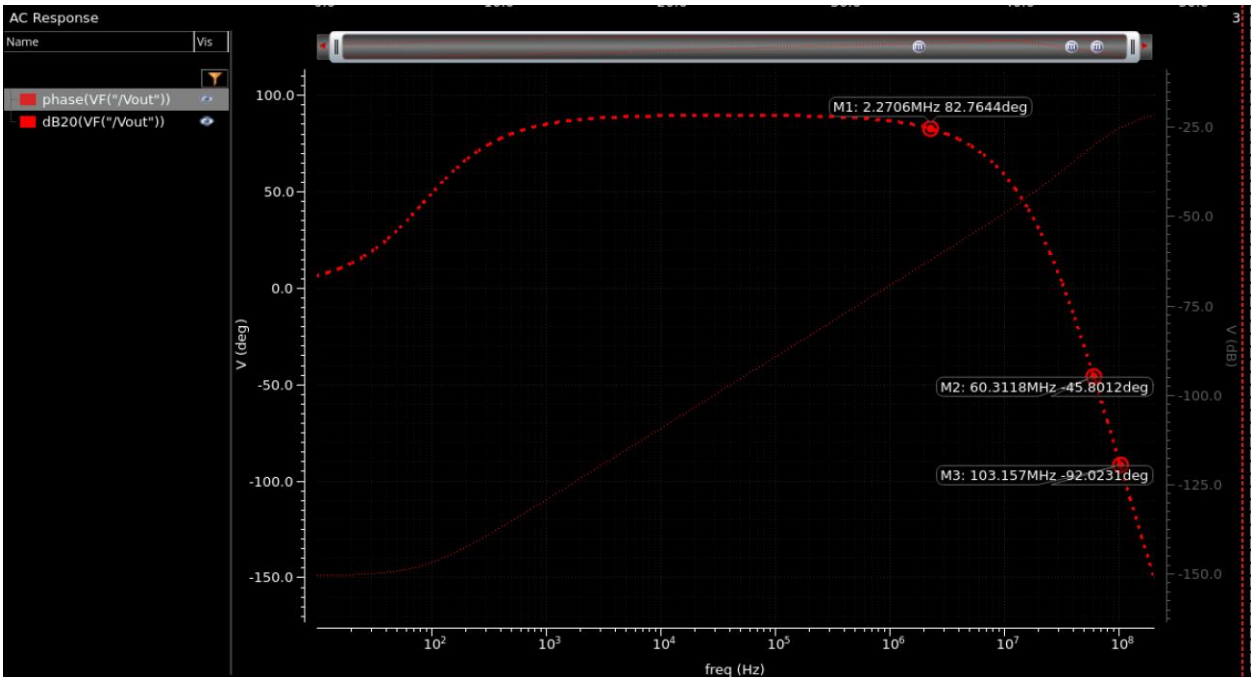

Figure 6 AC magnitude and phase plot with pole markers