IRAM Cache & Address Translation

Cache-based hardware solution is presented to the Instruction Memory (IRAM) space issue. The solution supports pages protection, so user can block eviction of certain pages.

The method make use of three main hardware mechanisms: (1) Latch-based Mapping table of the IRAM page addresses to the Flash Memory page addresses. (2) Flop-based link-list implementation of the cache LRU eviction policy. (3) Combinatorial mechanism, Miss Handler, routes requests according to the address space of the request.

Another hardware solution, called Address Translation, is presented to the use of Address Virtualization. Enabling several virtual sources of several OSs to share the same shared hardware, supporting large amount of virtual users of different types and demands.

The method uses two main hardware mechanisms: (1) Pipe Line architecture achieves top performance and divides the translation into stages. (2) Parallel logic in order to calculate many translations at the same time and match the correct result.

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