Address Translation & IRAM Cache

Progress Report #3

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Achievements

- Completed MAS (Micro-Architectural Specifications) documents for both of the units – IRAM Cache, Address Translation. The MASs specify the followings:
    - Overview: features and external interfaces
    - Block diagrams
    - Main control flows
    - Clock and reset domains
    - Sub-Blocks description: functionality, interfaces, wave diagrams.
    - MISC: verification aspects and potential hazards.
- Creating empty wrappers only with interfaces for both Address Translation and IRAM Cache.
- Completed revising adjacent blocks for the Cache unit:
    - Adding the cache as an agent on the SPI interface to the NVM.
    - Took off a sample stage from the "read data path" in the CPU's wrapper.
- Completed revising adjacent blocks for the Address Translation unit:
    - Adjusting the interfaces of the "interconnect block" and the "per home logic" to the Address Translation.
- Created wrapper with basic translation function for "4k-request".

Challenges

- Finish coding all sub-blocks for full mapping of the IRAM Cache:
    - Miss Handler
    - LRU (eviction policy management) – as a linked list.
    - CAM – as latches rather than flip-flops
- Finish coding all sub-blocks for basic translation:
    - 4k-translation
    - Vf2pf translation
    - Access type – might be affective to generate the Verilog file using a script (pearl/python) as the requirements for this classification vary frequently.
    - Calculator – Must return result within at most 2 cycles and must be able to receive requests every cycle.
- As we received a new architectural requirement regarding the security vulnerability among processes in the Address Translation, we still need to figure how to block some requests that are outputs of the calculator stage.
- Contacting Intel Legal department in order to get permission of viewing part of the MAS (Micro Architectural Specifications) document – WIP*.

Correspondence with advisor

- In our weekly 1:1 meetings with our advisor we discussed:
    - The SPI block adjustment which was a bit complicated so Nadav helped us to split the assignment into 3 small assignment.
    - The ways to achieve MVP on schedule:
        - Which coding assignments can be postpone for P1/P2.
        - Which coding assignments need to be altered in order to meet the schedule.
- We had our weekly meetings with our advisor and the team's micro-architect (Alon) concerning the architectural design changes described above.