Address Translation & IRAM Cache

Progress Report #4

Members:
ori.yeffet@mail.huji.ac.il – Ori Yefet
omrids@gmail.com – Omri Dassa
Group 327

Advisor:
nadav.rotter@intel.com – Nadav Rotter

Achievements

- Finished coding all sub-blocks for full mapping of the IRAM Cache (MVP):
    - Miss Handler
    - LRU (eviction policy management) – as a linked list.
    - CAM – as latches rather than flip-flops
- Succeeded to push P1 target (Pining addresses) into the MVP!!! =]
- Built TestBench for covering the IRAM Cache Functionality correctness.
- Finished coding all sub-blocks for basic translation:
    - Vf2pf translation
    - Calculator – Must return result within at most 2 cycles and must be able to receive requests every cycle.
    - Arbitration of several CPUs.
    - Register controllers' implementation for configuration.
- Built TestBench for covering the Translation correctness.
- Defined a practical an efficient solution to address protection.
- Generated (LOL – Logical Level) synthesis reports of timing and area – almost without any issues!!!
- Broke critical path that did not meet timing by sampling.

Challenges

- Finish adjustments to MissHandler and LRU for supporting IRAM partial mapping via threshold address by the end of WW15.
- Finish coding Address protection by the end of WW16.
- Adjust the TestBenches to cover the new features' functionality correctness.
- Reproduce fresh Area and Timing reports.
- Start thinking of good rules for formal verification for our blocks.

Correspondence with advisor

- We had a meeting with our advisor and the team's micro-architect (Alon) concerning the need of adding address protection and defining the solution.
- In our weekly 1:1 meetings with our advisor we discussed:
    - The address protection feature and the critical path we discovered in the timing reports, forced us to reconsider the pipe-line architectural for VF translation into PF and PF protection. The main concern was the new sample stages in the pipe-line.
    - Threshold address bypass requires to add a bit to the address from the CPU so we were advised on how to change some of the interfaces of the CPU with the Cache block in order to match the new demand.