# Address Translation
# &
# IRAM Cache

Group 327

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# Abstract

A cache-based hardware solution is presented to the Instruction Memory (IRAM) space issue. The solution supports pages protection, so users can block the eviction of certain pages.

The method makes use of three main hardware mechanisms:

1. Latch-based Mapping table of the IRAM page addresses to the Flash Memory page addresses.
2. Flop-based link-list implementation of the cache LRU eviction policy.
3. A combinatorial mechanism, Miss Handler, routes requests according to the address space of the request.

Another hardware solution, called Address Translation, is presented to the use of Address Virtualization. Enabling several virtual sources of several OSs to share the same shared hardware, supporting a large number of virtual users of different types and demands.

The method uses two main hardware mechanisms:

1. Pipe Line architecture achieves top performance and divides the translation into stages.
2. Parallel logic in order to calculate many translations at the same time and match the correct result.

# Introduction & Related Work

Nowadays NICs (Network Interface Controllers) has several CPU Controllers that process, analyze and route data according to the network protocols. These CPUs are controlled using a set of firmware instructions that are stored in the CPUs' IRAM (Instruction RAM). In order to add certain functionality to the NIC's CPUs, one must load an upgraded set of Instructions to the IRAM. This way a customer of the NIC can apply many features that are costumed to specific or several clients (servers/PCs). As the years pass by, there is a greater need for assimilating a greater number of features that require much more of IRAM space.

In addition, when one is interested in upgrading the NIC performances, a parallel compute-system architecture must be applied, and data transfer must be done by using several channels. In this scenario, several software entities that own several processes run in parallel while assuming that they are the sole user of the NIC's resources. For example, if a certain process of certain software entity (some client of the NIC) wants to access address 0x10 and a second process of a second software entity (or even the same one) wants to access the same address. It would be wrong to assume that both entities mean to access the same data as these addresses are virtual. There is a crucial need for translation the virtual address to a physical one before accessing the public memory according to several parameters that are related to the original request.

Solutions to both of the above mentioned problems are significantly important as they are important milestones in the NICs' development and future capabilities: Widening the IRAM address space is necessary for enabling the NIC's costumers to extend the number of supported features, and without translating and mapping virtual addresses to physical addresses, a parallel architecture wouldn't be feasible.

The NIC industry and data transfer took a major leap in the last few years as far as it concerns the demands from NICs manufactures, and this project which is planned to serve clock rates that has yet to be seen in the market, is located in the front of the NICs' technology. Solutions to the above-mentioned problems hold great challenges related to hardware common issues such as timing and area. These solutions must meet performance demands and area constraints as well as being versatile and adapted to changes in order to be suitable also for future projects.

In previous projects, there was no use of parallel computations and so the translation function used to be simple. In the current project, there is a need for splitting the NICs memory resources to several software entities and so to map the requested address from several entities to the public Memory space. In addition, a new protection mechanism must be applied between different software entities as one might try to access the other's address space. A second challenge that NICs' developers face is to provide a wider IRAM address space without consuming any more of the NIC's area and so to support more features for the NIC's costumers. Caching is a known solution to these kinds of problems, however, our solution must support protection on some parts of the IRAM. The protection is necessary for storing the interrupt and error handlers and prevent them from being evicted and also highly useful for NIC's customers who would like to keep a high performance of certain features.

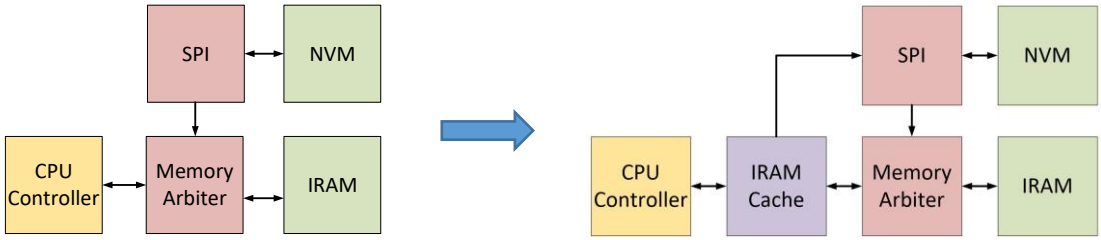
# IRAM Cache

## Peripheral

The process of fetching instruction to the CPU Controller is being done by several existing blocks. These blocks are responsible for a couple of operations:

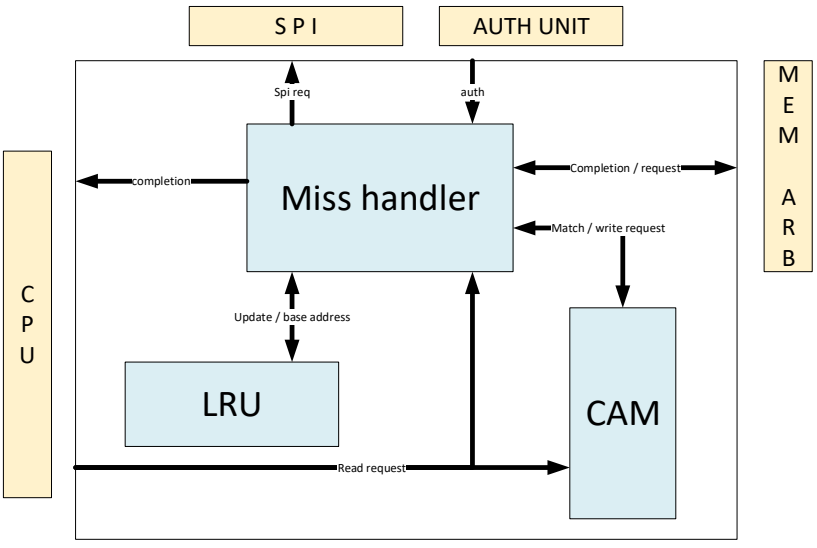
1. Load the entire firmware image from a Non Volatile external Flash Memory (NVM) to the IRAM on boot sequence. The loading process is using the SPI (Serial Peripheral Interface) mechanism and the Memory Arbiter block which routes every memory access request from each client to every memory.
2. Send a read request from the CPU to the IRAM via the Memory arbiter and roll the instruction data back to the CPU. This mechanism must comply with 2 cycles per request constraint.

The Cache block is functioning as a bridge between the CPU and the Memory Arbiter and is also a client of the SPI block.




In order to expand the IRAM address space, we used a caching methodology that made the IRAM a cached memory to the NVM, meaning that we mapped the NVM address space to the IRAM address space. The CPU from now on will offer read requests with addresses of the NVM address space. Those addresses will be mapped to the IRAM address space by the caching mechanism in case the referred page indeed resides in the IRAM. In case the requested page is not in the IRAM, the cache mechanism will generate a request to write the page from the NVM to the IRAM via the SPI block.

## Sub-Blocks



**CAM –** Latch based inverted page table. The indices of the table are the IRAM page addresses while page size is 4kbytes. The table content is the matching NVM page addresses. For every incoming read request, a match operation is begin processed on the table. If the NVM address of the request is found in the table, an indication with the corresponding table index (IRAM address) is sent to the Miss Handler sub-block. A valid bit is also attached to each entry in the table. Accessing the table cost a single clock cycle.

**Miss Handler –** Combinatorial Data and Control Flow manger. Responsible for initiating read requests towards the IRAM in case of matched address in the CAM, and initiating SPI requests to write pages from NVM to IRAM in case of unmatched address. In addition, Miss Handler updates the LRU mechanism with IRAM addresses that were used recently and fetches addresses for eviction. These addresses for eviction are sent by Miss Handler as part of the SPI request (so that the SPI would write the NVM data to evicted address in the IRAM). These addresses are also sent by Miss Handler to the CAM for invalidation until the requested page is written to the IRAM.

Another responsibility of Miss Handler is to handle some of the protection-resolution on pages. Miss Handler reads a configurable register which contains a threshold address that partitions the IRAM to cached IRAM and uncached IRAM. A request will be forwarded directly to the IRAM (bypass mode in the cache mechanism) if the MSB (Most Significant Bit) of its address is set and the address is larger than the threshold address. A request will be forwarded through the cache mechanism if the MSB of its address is not set and the address is smaller than the threshold address. This partitioning creates an eviction-safe IRAM address space and thus protecting a configurable address space. Miss handler will roll any successful read request completion back to the CPU.

**LRU –** Flip-Flop based, 2-way cycled link-list eviction policy manager. Each IRAM page address (points to 4kbytes page) is represented as a node in a register table which pointes to the next address that was used earlier chronologically (Head points to the least recently used address). LRU sub-block is responsible for the page protection as well. LRU link-list only links registers that represent an unpinned IRAM addresses and so protects the pinned ones from eviction. The second and third MSBs of the incoming address to the Cache block specify the pinning status (pin/unpin) requested for each page, and the LRU sub-block updates its link-list according to those. LRU update operation must be done in a single cycle as a different read request from the CPU might arrive in each cycle.

## Data Flows

**RESET Flow:** When the NIC is going out of reset a boot sequence is initialized simultaneously.

| Step | Description |
|---|---|
| * | CAM invalidates all of its entries. When it is finished it raises a “done” signal. |
| * | LRU sub-block is linking all IRAM page addresses in ascending order from the threshold address up to the IRAM last page address. Any address below the threshold is unlinked and will never be evicted, so is safe to be accessed via the Bypass mechanism. When it is finished it raises a “done” signal. |
| * | The Cache operates in Bypass Mode only until the boot sequence is done. |

**HIT Flow:** A NVM page address was matched in the CAM

| Step | Description |
|---|---|
| 1. | Miss handler receives a read request from the CPU with an address that its MSB is set (not Bypass Mode). |
| 2. | The upper bits of the address (the page address) are being matched in the CAM successfully and a Match signal with the corresponding IRAM page address is sent to Miss Handler. |
| 3. | Miss Handler builds the request address to the IRAM using the IRAM page address from CAM and the lower bits of the original address (offset). A translated read request is sent to the IRAM. |
| 4. | Miss Handler updates the LRU mechanism with the IRAM page address that was used and its pinning status. If an address was asked to be pinned, the LRU removes it from the link-list. If an address was asked to be unpinned, the LRU links it to the head of the list. If no pinning was asked then LRU links the address to the tail of the list. |

**MISS Flow:** A NVM page address was not matched in the CAM

| Step | Description |
|---|---|
| 1. | Miss handler receives a read request from the CPU with an address that its MSB is set (not Bypass Mode). |
| 2. | The upper bits of the address (the page address) are being matched in the CAM unsuccessfully and the Match signal to Miss Handler is not set. |
| 3. | Miss Handler pops an IRAM page address for eviction from the LRU, and sends a request to the SPI mechanism to write the page of the original request from the NVM to the IRAM address of the evicted page. Miss Handler also invalidate the address of the evicted IRAM page address in the CAM. |
| 4. | Miss handler updates LRU to replace its head address. |
| 5. | Miss handler masks any other MISS and allows only HITS. Meaning that any consecutive MISS will be silently dropped. |
| 6. | The SPI mechanism sends an indication of a successful read and write operation and that the data from the NVM was authenticated. Only then Miss Handler writes the original NVM page address to the CAM in the IRAM page address index and removes the mask on MISS flow. |

**BYPASS Flow**: Read request to the Uncached IRAM

| Step | Description |
|---|---|
| 1. | Miss handler receives a read request from the CPU with an address that its MSB is not set (Bypass Mode). |
| 2. | The cache mechanism is masked and the request is sent out to the IRAM directly. |
| 3. | Data completion is rolled back to the CPU. |

## Evaluation

**Functionality –** in order to check that the cache mechanism works as expected several executing scenarios were simulated to cover basic and corner cases: single HIT, single MISS, pin, unpin, Bypass Mode, LRU wraparound and many others. In addition, random testing was simulated on the design in order to ensure its functionality. Last but not least, we assimilated Formal Verification environment that includes rules we wanted to prove mathematically.

**Timing –** one of the challenges in assimilating the cache mechanism is to handle the long and loaded combinatorial rout from the CPU to the Memories and back. The distance of the memories and the logic that wraps the CPU makes it difficult to meet timing under the restriction of a higher clock rate. The synthesis tool we ran calculated all of the critical paths and estimated good results (positive slack) regarding the mentioned routes.

```
  ------------------------------------------------------------
------------------------
  data required time
2163.3
  data arrival
time                                                        -
1889.2
  ------------------------------------------------------------
------------------------
  slack (MET)
274.1
```

**Area –** No less important issue is keeping the cache mechanism as small as possible, as we were asked to increase the IRAM address space without increasing its actual size on the NIC. The cache mechanism size is mainly determined by the number of non-combinatorial cells of the CAM and LRU mechanisms and the large Mux components that enable their functionality. While we were investigating the mapping process of the CAM we realized that there are no racing conditions on the table entries (as only one line of the table is accessed in each clock cycle) and so there are no risks in using Latches instead of Flip-Flops. This optimization helped us reduce the size of the entire cache mechanism by over 21% and the CAM by 50%.

```
Combinational area:                21752.281764
Buf/Inv area:                       4999.281138
Noncombinational area:             26280.430359
Macro/Black Box area:                350.441005
Net Interconnect area:      undefined  (No wire load
specified)

Total cell area:                   48383.153128
Total area:                 undefined

Core Area:                          76204
Aspect Ratio:                      1.0012
Utilization Ratio:                 0.6369
```

## Conclusions & Future work

This document presents the feasibility and capability of assimilation of a cache mechanism to the IRAM of NIC's management CPU, supporting eviction protection and bypass mode. The cache mechanism is required to operate on the path of an existing rout between the CPU and the IRAM, under the limitation of a higher clock rate and minimal area impact. All functional tests that were predefined passed successfully and the synthesis tool results showed the design met timing on the critical path.

Assumptions & Restrictions:

1. Interrupts and errors handlers must be either pinned or reside in an uncached part of the IRAM in order to avoid deadlock
2. The LRU link-list must hold at least 2 nodes at any given cycle. Meaning the threshold address can be at most LAST_IRAM_PAGE_ADDRESS -2 and both of these pages must not be pinned. Unless the required configuration is for a fully uncached IRAM which in that case the threshold address will be set to LAST_IRAM_PAGE_ADDRESS.
3. CPU will not try to access Cached IRAM in bypass mode.
4. The cache mechanism is applicable only after a threshold address was set.

Future work:

Miss rate – in order to supply the CPU a useful information on the locality of pages in the IRAM there is a need to count the number of Misses in the cache relatively to the number of requests from the CPU. The SPI mechanism can handle a single request at a time and so it is better to calculate the miss rate as 1-hit rate. Additionally, it is sufficient to provide only the hit count, as the calculation of the rate is not performance-oriented and can be done by software entities.

# Address Translation

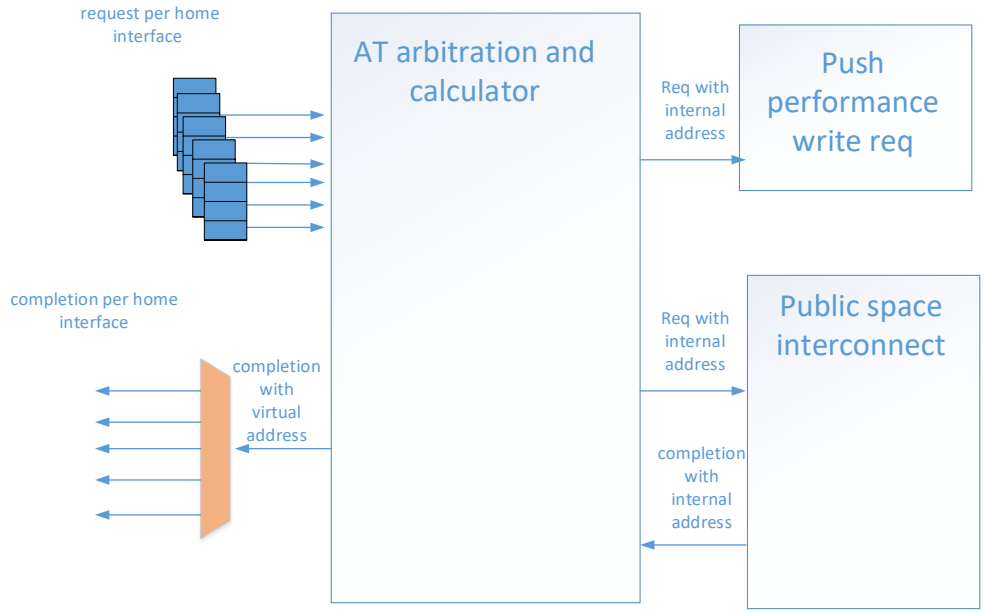
## Peripheral

**Home -** A hardware entity that generates requests to the public space using virtual addresses. If the request is a read request, the home will get a completion containing the data it wanted to read. Every home is an independent entity that is not aware of the existence of other homes.

**Interconnect -** A hardware device that receives read or write requests with addresses and data, and implement those requests as actual read or write operations on the public memory space.

**Push-** An output lane that handles only the write requests which are critical to the device performance. This output lane handles those requests faster than the Interconnect.

**AT –** Address translation.



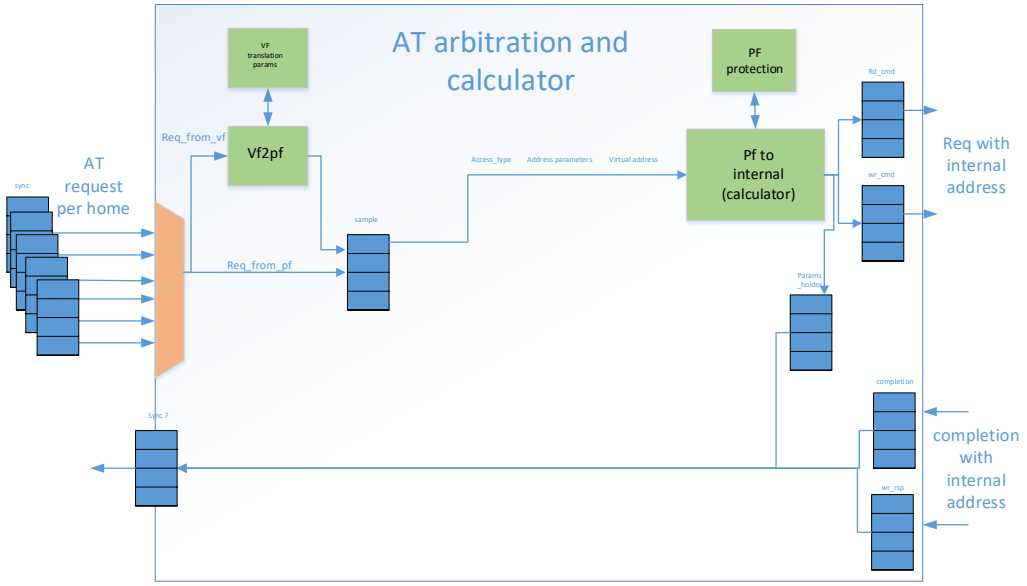

Address translation is a virtualization layer between two hardware components. The first is the requester (one of the homes) that sends a read/write request using a virtual address. The other is the public space interconnect/push which receives read/write requests and generate actual read/write to the public memory space. The goal of the Address Translation unit is to translate requests dynamically from homes for the Interconnect/Push, and return completions from the Interconnect back to the correct home. In addition, the Address Translation mechanism must protect the users of the public space from requests that comes from a different home than their owner. The Address Translation must achieve the above-mentioned goals with a maximum latency of 5 clock cycles and throughput of a single request per clock cycle.

Dynamically translation means that the formulas that the Calculator is using in order to translate requests, contain parameters that can be changed in real-time to match the demands of the home. A latency of 5 clock cycles means each request can take up to 5 clock cycles to reach from the request interface to the Interconnect/Push (actually done in 4 =] ). Throughput of 1 means that the AT unit has to be able to output a single translated request per clock cycle - no bobbles allowed.

## Sub Blocks

The Address Translation unit contains the following sub-blocks: VF2PF, Calculator, VF Translation Params and PF Protection, all of which can be seen in green. The blue components are FIFOs that are being used as buffers and synchronization units between different clocks and resets domains. The orange component is an arbiter that arbitrates between requests of the different homes.

We designed the Address Translation unit as a pipeline consisting the above mentioned 4 main sub-blocks. The pipeline architecture enables us to achieve throughput of 1. The number of stages in the pipeline will determine the latency of our module, and as there are 4 stages which each of them takes one clock cycle, the module achieves latency of 4 clock cycles (better than the architectural specifications). Pipeline architecture also helped us to divide address translation and protection into simple 4 stages, each with a simple well-defined purpose.

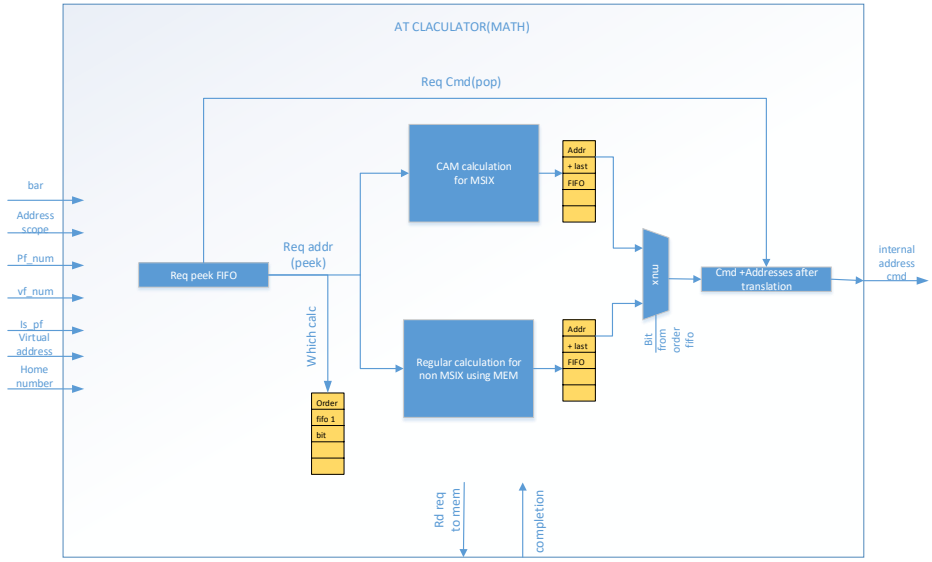



**VF2PF -** The first stage of the Address Translation pipeline. As mentioned, each home is not aware of the existence of the other homes, and so the home number can only be assigned at the Address Translation module (it doesn't have any meaning outside this module) according to the winning index of the arbitration process. The inputs of this stage are the request from one of the homes containing the VF and PF number, read/write indication and the virtual address. VF2PF extracts from the arbitration process the home number and also receives the translations parameters which are VF Translation Params unit completion to VF2PF query for parameters

The purpose of this stage is to initialize a translation process according to the VF number using VF related parameters that reside in the VF Translation Params module. Therefore it has 2 output lanes: One is to VF Translation Params module to ask for the parameters needed for the translation, the other is to a buffer which sends the request to the Calculator unit. If the request was generated by PF and not by VF this module only passes it to the next stage without any translation. VF2PF module can always handle 2 requests in parallel: One that arrives to the module without matching parameters and it is the VF2PF responsibility to supply those, another one is a request that already asked for its matching parameters at the previous clock cycle and can now do the calculation for VF translation.

**VF Translation Params -** The second stage of the pipeline. The purpose of this stage is to answer VF2PF requests for parameters. In order to dynamically translate requests of different homes, CSRs (Control and Status registers) are set in order to determine the way we calculate our translation. For example a CSR is set to define whether the translation will be done by page tables or by base + offset method and the parameters related to those methods. The total number of VFs is extremely large (number of homes * number of VFs) and so we chose to implement those CSRs using SRAM memory and not Flip-Flops. This implementation saves a lot of area in this module (we pay with 1 clock cycle of latency to retrieve data from memory). The input for this stage is the VF number and the output of this stage is the parameters related to this VF. It is the host responsibility to write those CSRs for configuration of the translation. Address Translation unit only read those registers, and it is Address Translation unit responsibility to know the coherency state of those registers.

**Calculator -** The third stage of the pipeline. This stage purpose is to calculate the final translation from virtual to internal (physical) address, determine if the request should be sent via the Interconnect or Push interface, and whether the request is valid or not (protection).




As one can see at the scheme above, this stage is composed of 2 inner modules one for translation of regular requests and the other for translation of interrupts (MSIX according to PCIE spec). This unit uses the Home and PF numbers in order to translate the request, in addition to send a query to the PF Protection unit that determines whether the request is valid or not (Protection). According to the type of the request and its translated address space the unit sends the translated request to Push/Interconnect units.

The structure of this unit is unique as it begins and ends with buffers and in the middle we created two lanes for the different jobs. We faced two major challenges in this task. The first was that we had to balance the timing between the lanes and. The other was maintaining the order of the requests. We solved both of the issues using the yellow FIFOs. The one that is called “order fifo” reserves only one bit per request in order to indicate whether the request will be answered from the regular or MSIX lane, and so maintaining the order. The other two yellow FIFOs were designed to balance the timing between the lanes with back pressure from each FIFO. At the end of both lanes we have a MUX that selects the translated address from the correct lane according to the order FIFO.

**PF Protection -** The fourth and last stage of the pipeline. The purpose of this stage is to answer Calculator unit queries for parameters (the parameters indicate the owner id of some memory). In order to dynamically change the owners of chunks of memory, CSRs were set in order to determine the owner of each chunk. We faced a similar challenge to VF Translation Params so we also chose to implement the CSRs here as SRAM and not Flip-Flops, which saved a lot of area in this module. It is the host responsibility to write those CSRs for configuration of the protection. Address Translation unit only read those registers, and it is Address Translation unit responsibility to know the coherency state of those registers.

## Data Flow:

**Regular request:**

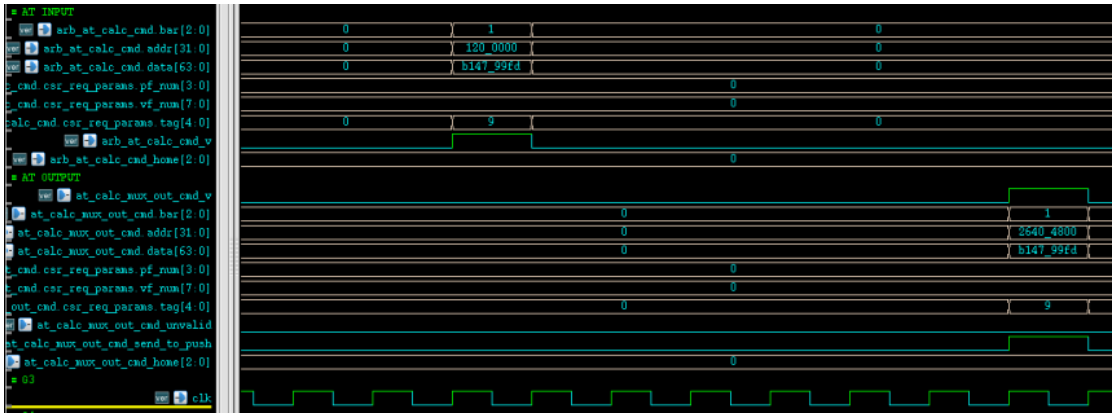
| Stage/Sub-block | Description |
|---|---|
| Interface | Some Home initiates a write request that for translation. The request arrives AT module interface and won the arbitration between the other Homes. |
| VF2PF | VF2PF receives the request that won at the arbitration process and query VF Translation Params for the VF-parameters of the request. |
| VF Translation Params | Checks the value of the related CSRs (1'st cycle of latency) and return their data to VF2PF. |
| VF2PF | Calculating the VF-translation for this request using the parameters that VF Translation Params provided and send it to the Calculator (2'nd cycle of latency) |
| Calculator | Receives the request from VF2PF and query PF Protection unit with the related parameters. |
| PF Protection | Return the value of the related CSRs. (3'rd cycle of latency) |
| Calculator | Receives the protection parameters from PF Protection and checks that the request is in/valid according to the type of the request. The lane (Interconnect/Push) is also being determined according to those parameters. (4'th cycle of latency) |
| Interface (Interconnect/Push) | Routes the request to the correct lane: nonperformance oriented writes/reads to the Interconnect and performance oriented writes to Push. Invalid requests are completed with a special signature. |
| Interface (Interconnect /Push to one of the homes) | Write requests will follow by response and read requests will follow by completion. Both are routed back to the related Home. |

**Unsupported request:**

| Stage/Sub-block | Description |
|---|---|
| Interface | Some Home initiates a write request that for translation. The request arrives AT module interface and won the arbitration between the other Homes. |
| VF2PF | VF2PF receives the request that won at the arbitration process and query VF Translation Params for the VF-parameters of the request. |
| VF Translation Params | Checks the value of the related CSRs (1'st cycle of latency) and return their data to VF2PF. |
| VF2PF | Calculating the VF-translation for this request using the parameters that VF Translation Params provided and were found malicious. A special indication is sent to the Calculator (2'nd cycle of latency). |
| Calculator | Receives the request from VF2PF and query PF Protection unit with the related parameters while keeping the malicious indication. |
| PF Protection | Return the value of the related CSRs. (3'rd cycle of latency) |
| Calculator | Receives the protection parameters from PF Protection, ignores them, and complete the request with a special signature without forwarding it either one of AT output lanes. (4'th cycle of latency) |
| Interface<br>(to one of the homes) | Special completion or write response is sent. |

## Evaluation:

**Functionality** – in order to check that Address Translation module works as expected we generated sequential tests that check the translation for every possible combination of VF, PF, Home with many different addresses. Those tests used randomized values of CSRs that configure the translation process. For the protection mechanism some rules of Formal Verification were used in order to prove infeasibility of abnormities. By passing all of these tests we ensured the functionality of the design.




**Timing** – in order to enable real synthesis of our code we needed to bring our design to pass timing with positive slack. This task was challenging because the clock rate in this project was 30% higher than that of the previous, meaning that every clock cycle is shorter. In order to face this challenge we built our Address Translation unit with new pipeline architecture that can handle the new clock timing by cutting the long routs in the middle and divide AT unit from being one huge module that works at single cycle architecture into many sub blocks with defined purpose resulting with minimal latency and maximal throughput.

```
data required time                                                    0.828
data arrival time                                                    -0.823
-------------------------------------------------------------------------
slack                                                                 0.005
```

**Area** – Address translation unit ought to keep huge number of tables (VF translation parameters, PF protection) with information for each VF/PF. These tables cost the majority of the area of the AT unit (tables -73% functional logic - 27%). When we decided to move to pipeline architecture we figured that we can spare another 2 clock cycles of latency in order to save a lot of area by holding these tables with SRAM memory and not Flip-Flops. By doing so, 40% of AT total area was saved. The second consideration regarding AT area was how much flexibility the unit will be able to provide each home. The flexibility is measured by the number of page tables a VF can use for translations. By calculating the area of a single page table and getting as close as we could to the area limit specified for the AT unit, we estimated that the unit could provide 16 page tables per VF. Note that we could not have been able to keep as that many page tables if we kept them stored as Flip-Flops.

```
Number of ports:                        52541
Number of nets:                        135852
Number of cells:                        89870
Number of combinational cells:          74310
Number of sequential cells:             15441
Number of macros/black boxes:               0
Number of buf/inv:                      11174
Number of references:                       8

Combinational area:               5936.121393
Buf/Inv area:                      547.692477
Noncombinational area:            5815.942465
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 11752.063858
Total area:                 undefined
```

## Conclusions & Future Work:

This document presents the functionality and capability of translating virtual addresses of requests from multiple software entities to a shared resource, supporting smart and configurable protection mechanism. The Address Translation unit is a necessary requirement for operating in a parallel architecture, and is set on the path of an existing rout between multiple Homes and a shared resource, under the limitation of a higher clock rate and minimal area impact. All functional tests that were predefined passed successfully and the synthesis tool results showed the design met timing on the critical path.

Future work:

1. Formal Verification – extend our formal verification for all of the AT unit. Assemble more rules for all sub-blocks of the unit, make wider coverage on the design and its features. By doing so, we can prove without doubt that important functionalities are working, and that unwanted behaviors are not.
2. Create a special sequence that handles reset of the Interconnect while the Homes still generate requests, as the Interconnect is at a different reset domain from the Homes.

# Backmatter

## Bibliography


1. HAS – Hardware Architectural Specifications.

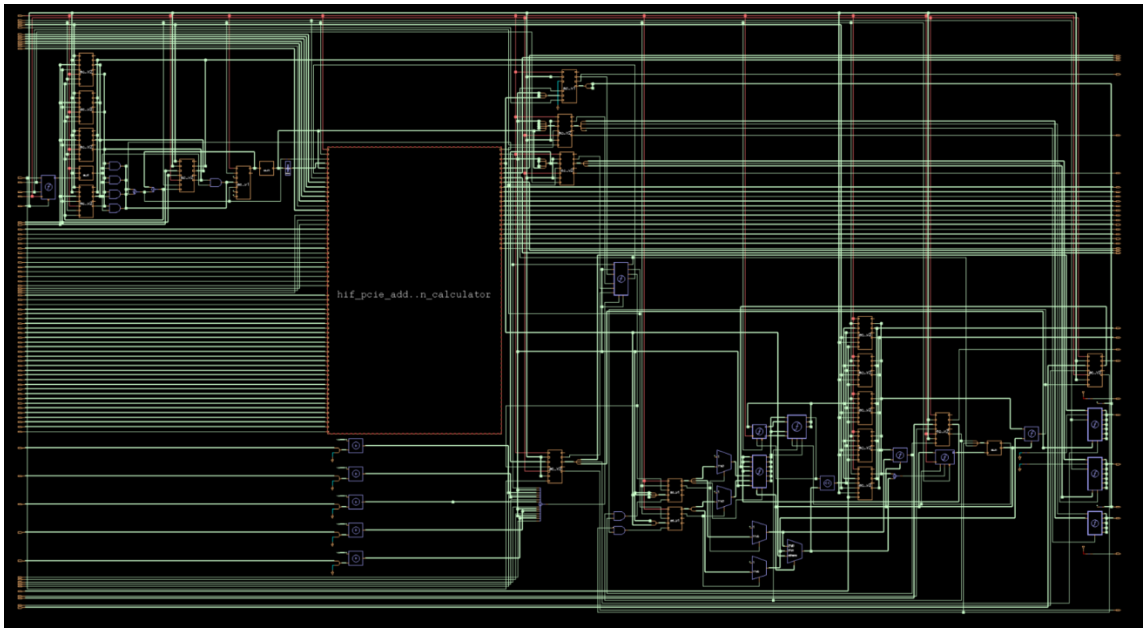
   One of the cornerstones of any ASIC (Application Specific Integrated Circuit) flow is a HAS which is written by the product's architects and that defines the high level functionality and specifications of a product. The product, which our project is a part of, lays on the cutting edge of Ethernet development. For that reason, the product documentation is classified as Intel Top Secret, preventing us from disclosing it. The HAS defines the top level architecture, data flow rates, area limitations, supported features list, etc. Note that the HAS does not describe the design of the features implementations, only the definitions, specifications and limitations.

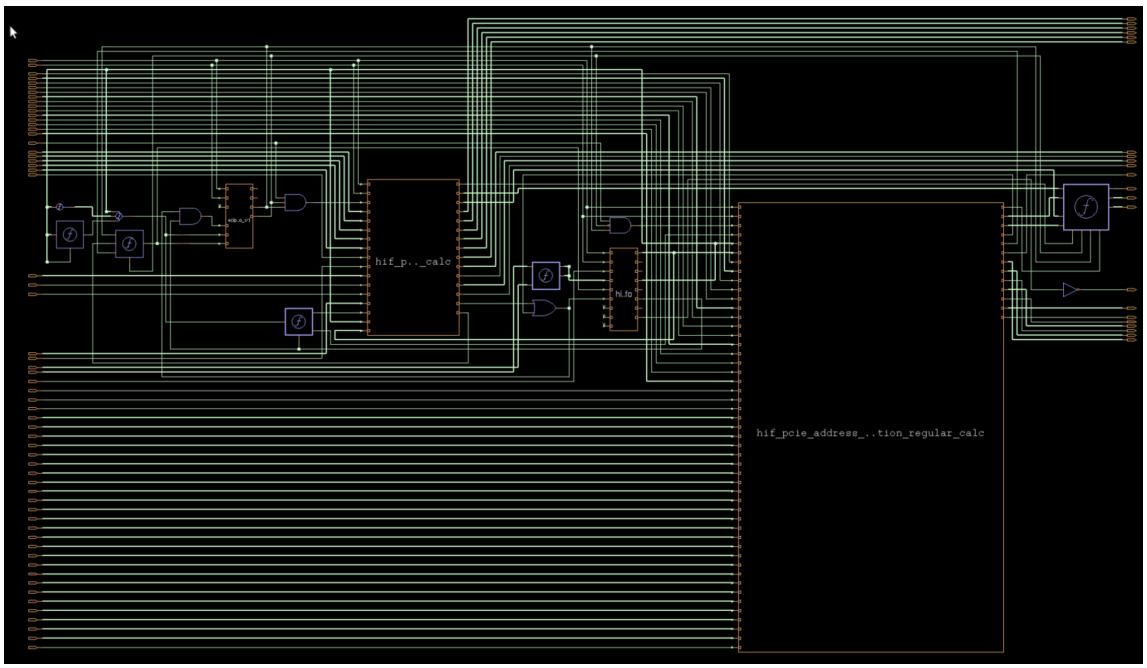
2. PCIE SPEC
   http://www.lttconn.com/res/lttconn/pdres/201402/20140218105502619.pdf

   PCI Express (Peripheral Component Interconnect Express), is a high-speed serial computer expansion bus standard, designed to replace the older PCI, PCI-X and AGP bus standards. It is the common motherboard interface for personal computers' graphics cards, hard drives, SSDs, Wi-Fi and **Ethernet hardware** connections.
   PCIE defines all software entities that were mentioned in this document. It also defines PF, VF and their relationship with Hosts and address translation. The NIC that we are a part of its development team implements the PCIE protocol and thus, we were bounded to use this document and support all of its specifications.

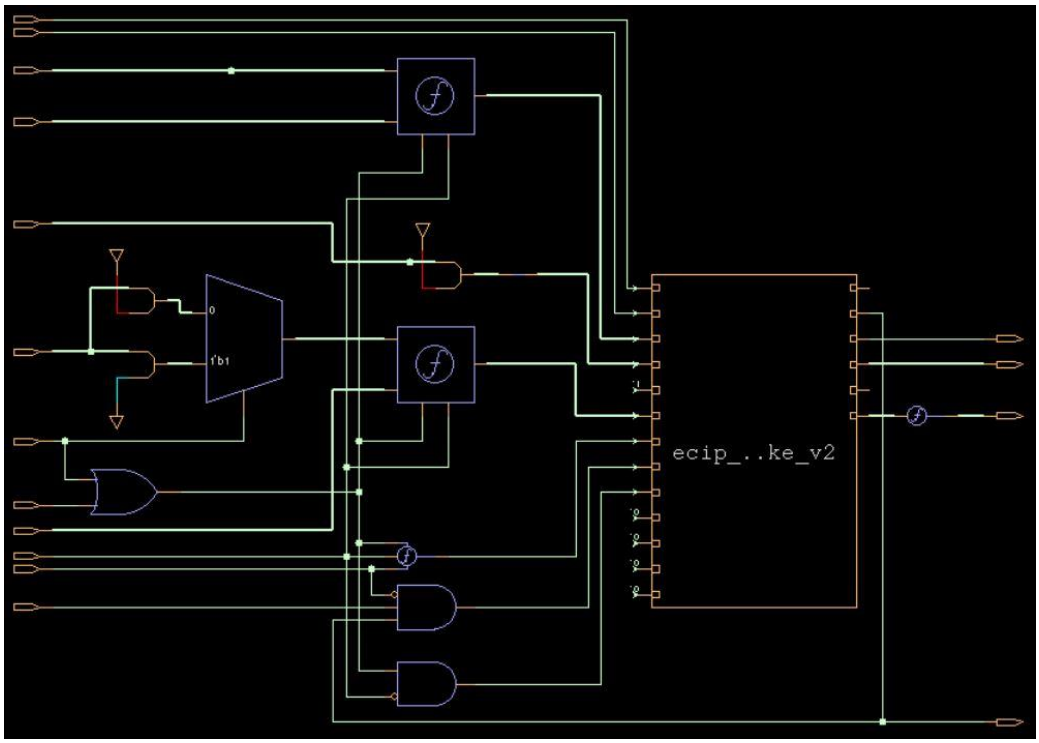
# Appendices

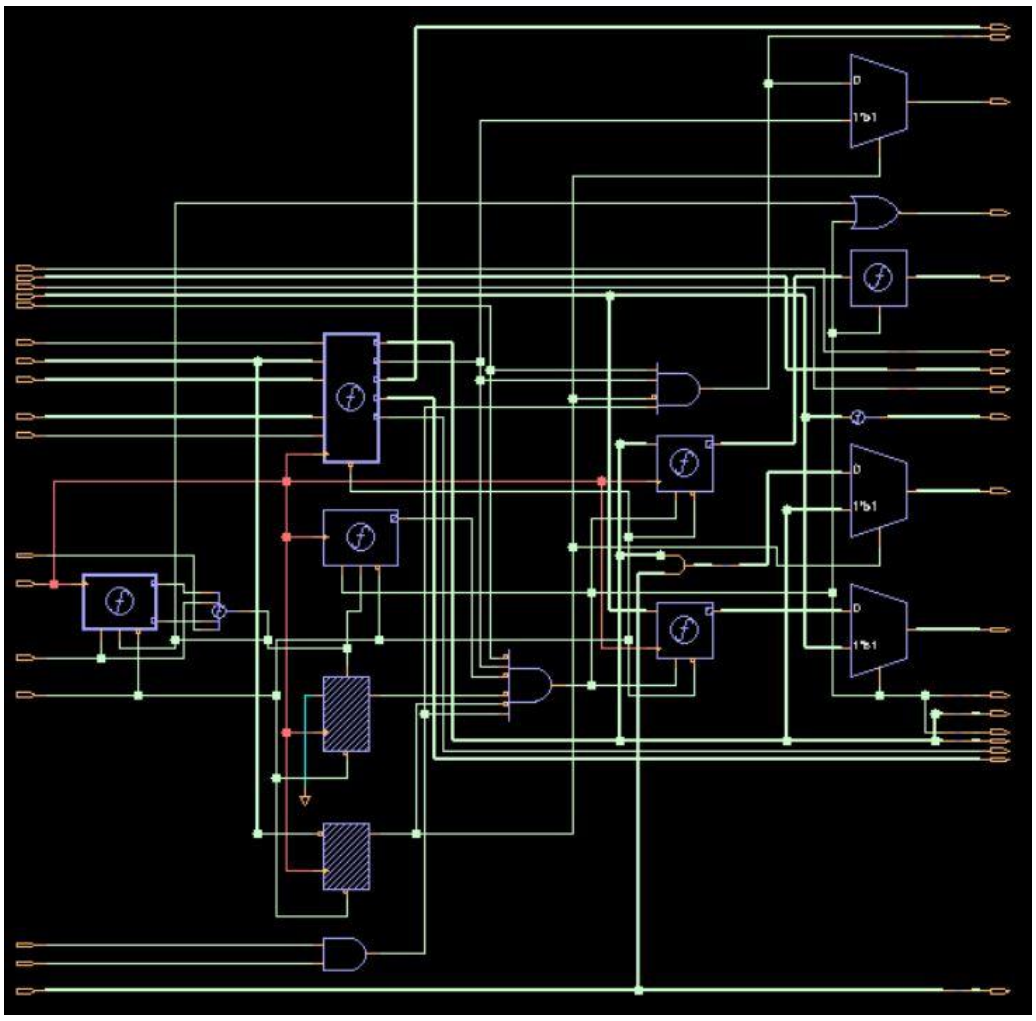
1. Visual synthesis results:
    a. Address Translation:

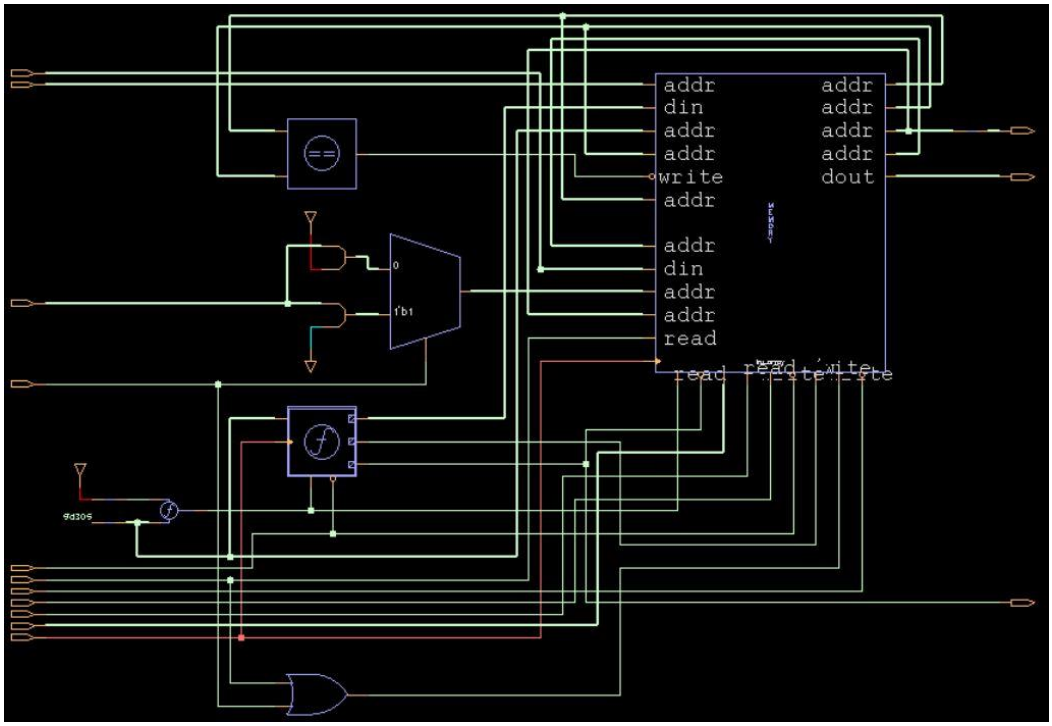


b. IRAM Cache:

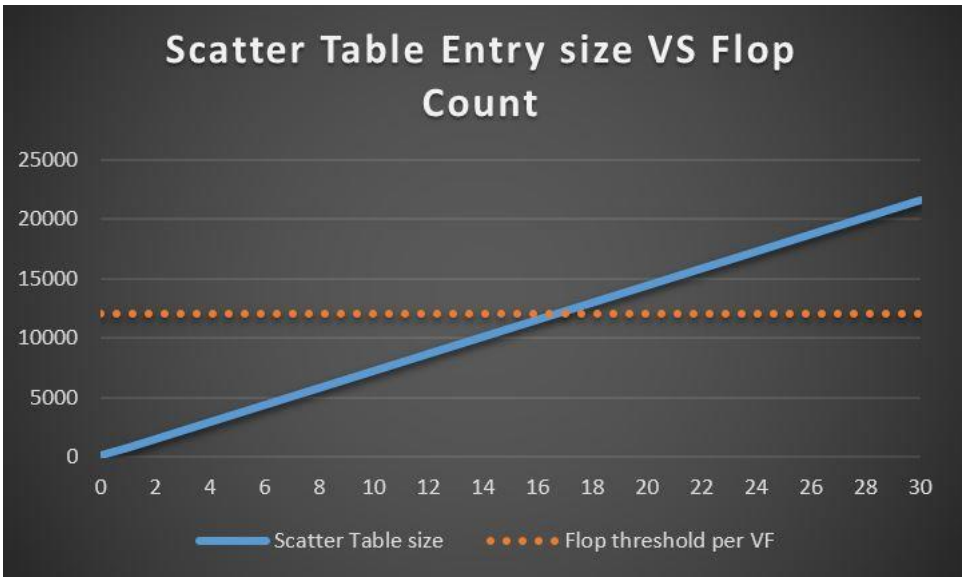


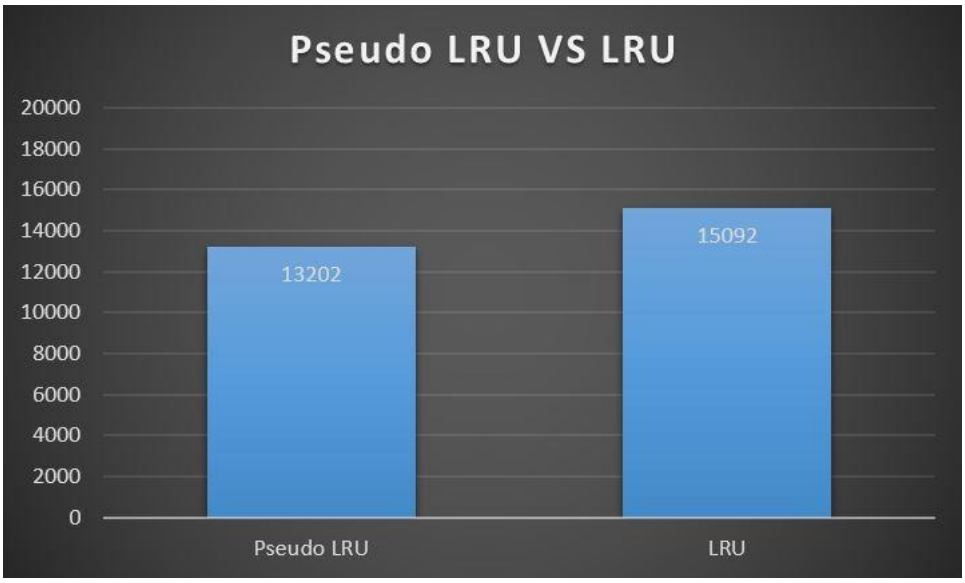

addr
din
addr
addr
write
addr
addr
din
addr
addr
read
addr
addr
addr
addr
dout
0
1'b1
read
write

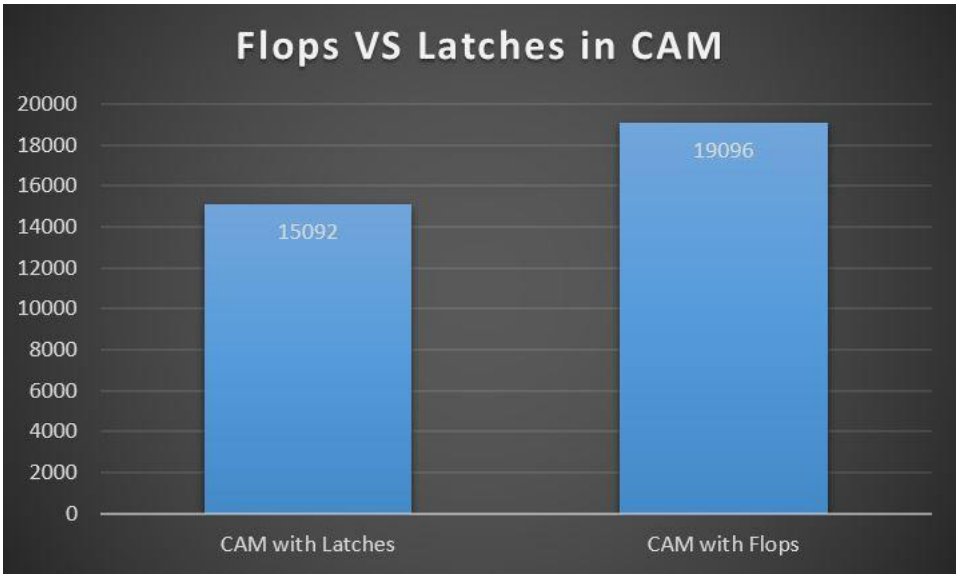
2. Area considerations graphs:

    a. Address Translation:




    b. IRAM Cache:




Flops VS Latches in CAM
20000
18000
16000
14000
12000
10000
8000
6000
4000
2000
0
15092
19096
CAM with Latches
CAM with Flops

3. Timing Reports: (The full report is 250 pages, we only show an example from it)

```
****************************************
Report : timing
        -path full
        -delay max
        -input_pins
        -nets
        -transition_time
        -sort_by slack
****************************************


Some/all delay information is back-annotated.

 # A fanout number of 10000 was used for high fanout net
computations.

Operating Conditions: typical_1.00   Library:
ec0_ln_p1274d3_tttt_v065_t100_max_ccst
Wire Load Model Mode: Inactive.

  Startpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0
              (rising edge-triggered flip-flop clocked by
ascan_preclk_mgmt_clk)
  Endpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_229.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo
             (positive nochange timing check for clock
ascan_preclk_mgmt_clk')
  Path Group: ascan_preclk_mgmt_clk
  Path Type: max

  Point                                          Fanout     Trans
Incr       Path
  ----------------------------------------------------------------
------------------------
  clock ascan_preclk_mgmt_clk (rise edge)
0.0        0.0
  clock network delay (ideal)
0.0        0.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/clk
(ec0faw003al2n03x5)      0.0      0.0      0.0 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/o
(ec0faw003al2n03x5)      7.2     18.2     18.2 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
```

```
sa.PCandIFetch.returnFromOCD_C2 (net)     2      0.0     18.2
f
  U145922/b (ec0nor002al1n01x5)                              7.2
0.0 *     18.2 f
  U145922/o1 (ec0nor002al1n01x5)                            15.4
15.9       34.1 r
  n160623 (net)                                  1
0.0       34.1 r
  syn_253469/a (ec0bfn000al1n04x5)                          15.4
0.0 *     34.1 r
  syn_253469/o (ec0bfn000al1n04x5)                           8.6
17.6       51.7 r
  n368824 (net)                                  2
0.0       51.7 r
  syn_186517/c (ec0nand03al1n12x5)                           8.6
0.0 *     51.7 r
  syn_186517/o1 (ec0nand03al1n12x5)                         24.7
23.6       75.3 f
  n309155 (net)                                  4
0.0       75.3 f
  syn_184533/a (ec0bfn000al1n08x5)                          24.7
3.2 *     78.6 f
  syn_184533/o (ec0bfn000al1n08x5)                          20.4
32.6      111.2 f
  n336143 (net)                                  9
0.0      111.2 f
  syn_184534/a (ec0inv000al2n08x5)                          20.4
2.4 *     113.6 f
  syn_184534/o1 (ec0inv000al2n08x5)                         14.1
15.9      129.5 r
  n336144 (net)                                  6
0.0      129.5 r
  syn_226018/a (ec0aoi022al2n08x5)                          14.1
0.0 *     129.5 r
  syn_226018/o1 (ec0aoi022al2n08x5)                         23.1
22.2      151.7 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PC_E_1_0 (net)     5      0.0    151.7 f
  U145990/b (ec0qbfno2bl2n18x5)                             23.1
2.6 *     154.4 f
  U145990/o1 (ec0qbfno2bl2n18x5)                            19.5
25.8      180.1 r
  n173989 (net)                                  4
0.0      180.1 r
  U145991/c (ec0oai022al2n01x3)                             19.5
2.0 *     182.1 r
  U145991/o1 (ec0oai022al2n01x3)                            26.8
27.2      209.3 f
  n142897 (net)                                  1
0.0      209.3 f
  syn_250934/a (ec0bfn000al1n04x5)                          26.8
0.0 *     209.4 f
  syn_250934/o (ec0bfn000al1n04x5)                          19.1
28.6      237.9 f
```

```
  n366256 (net)                                  3
0.0      237.9 f
  syn_226009/a (ec0oaoi03al2n02x5)                          19.1
0.1 *    238.0 f
  syn_226009/o1 (ec0oaoi03al2n02x5)                         32.4
29.8      267.8 r
  intadd_22.B_0_ (net)                           1
0.0      267.8 r
  intadd_22.syn_6/a (ec0rm0023al1n04x7)                     32.4
0.0 *    267.8 r
  intadd_22.syn_6/carry (ec0rm0023al1n04x7)                  7.8
24.3      292.1 r
  intadd_22.n5 (net)                             1
0.0      292.1 r
  intadd_22.syn_5/c (ec0rm0023al1n02x5)                      7.8
0.0 *    292.1 r
  intadd_22.syn_5/carry (ec0rm0023al1n02x5)                 10.9
24.1      316.3 r
  intadd_22.n4 (net)                             1
0.0      316.3 r
  intadd_22.syn_4/c (ec0rm0023al1n02x5)                     10.9
0.0 *    316.3 r
  intadd_22.syn_4/carry (ec0rm0023al1n02x5)                 11.2
25.6      341.9 r
  intadd_22.n3 (net)                             1
0.0      341.9 r
  intadd_22.syn_3/c (ec0rm0023al1n02x5)                     11.2
0.0 *    342.0 r
  intadd_22.syn_3/carry (ec0rm0023al1n02x5)                 14.7
28.9      370.9 r
  intadd_22.n2 (net)                             1
0.0      370.9 r
  intadd_22.syn_2/c (ec0rm0023al1n04x7)                     14.7
0.1 *    371.0 r
  intadd_22.syn_2/carry (ec0rm0023al1n04x7)                  6.5
20.5      391.4 r
  intadd_22.n1 (net)                             1
0.0      391.4 r
  syn_226005/a (ec0bfn000al1n04x5)                           6.5
0.0 *    391.5 r
  syn_226005/o (ec0bfn000al1n04x5)                           6.1
13.2      404.6 r
  n319486 (net)                                  1
0.0      404.6 r
  syn_226006/a (ec0inv000al2n08x5)                           6.1
0.0 *    404.7 r
  syn_226006/o1 (ec0inv000al2n08x5)                          3.6
4.6      409.3 f
  n142848 (net)                                  3
0.0      409.3 f
  U263389/b (ec0orn002al1n01x3)                              3.6
0.0 *    409.3 f
  U263389/o (ec0orn002al1n01x3)                             10.4
21.8      431.0 f
  n300566 (net)                                  1
0.0      431.0 f
```

```
  syn_226001/c (ec0ao0012al2n04x5)                        10.4
0.0 *    431.1 f
  syn_226001/o (ec0ao0012al2n04x5)                         8.3
21.5      452.5 f
  intadd_8.CI (net)                               1
0.0       452.5 f
  intadd_8.syn_23/c (ec0rm0023al1n04x7)                    8.3
0.0 *     452.6 f
  intadd_8.syn_23/carry (ec0rm0023al1n04x7)                8.1
22.1      474.7 f
  intadd_8.n22 (net)                              1
0.0       474.7 f
  intadd_8.syn_22/c (ec0rm0023al1n02x5)                    8.1
0.0 *     474.7 f
  intadd_8.syn_22/carry (ec0rm0023al1n02x5)               11.9
26.9      501.6 f
  intadd_8.n21 (net)                              1
0.0       501.6 f
  intadd_8.syn_21/c (ec0rm0023al1n02x5)                   11.9
0.1 *     501.7 f
  intadd_8.syn_21/carry (ec0rm0023al1n02x5)               12.4
28.7      530.4 f
  intadd_8.n20 (net)                              1
0.0       530.4 f
  intadd_8.syn_20/c (ec0rm0023al1n02x5)                   12.4
0.1 *     530.5 f
  intadd_8.syn_20/carry (ec0rm0023al1n02x5)               11.9
28.4      558.9 f
  intadd_8.n19 (net)                              1
0.0       558.9 f
  intadd_8.syn_19/c (ec0rm0023al1n02x5)                   11.9
0.1 *     558.9 f
  intadd_8.syn_19/carry (ec0rm0023al1n02x5)               11.2
27.5      586.4 f
  intadd_8.n18 (net)                              1
0.0       586.4 f
  intadd_8.syn_18/c (ec0rm0023al1n02x5)                   11.2
0.0 *     586.5 f
  intadd_8.syn_18/carry (ec0rm0023al1n02x5)               11.5
27.6      614.1 f
  intadd_8.n17 (net)                              1
0.0       614.1 f
  intadd_8.syn_17/c (ec0rm0023al1n02x5)                   11.5
0.0 *     614.1 f
  intadd_8.syn_17/carry (ec0rm0023al1n02x5)               12.1
28.2      642.3 f
  intadd_8.n16 (net)                              1
0.0       642.3 f
  intadd_8.syn_16/c (ec0rm0023al1n02x5)                   12.1
0.1 *     642.4 f
  intadd_8.syn_16/carry (ec0rm0023al1n02x5)               11.4
27.7      670.1 f
  intadd_8.n15 (net)                              1
0.0       670.1 f
  intadd_8.syn_15/c (ec0rm0023al1n02x5)                   11.4
0.0 *     670.1 f
```

```
  intadd_8.syn_15/carry (ec0rm0023al1n02x5)              11.6
27.8      697.9 f
  intadd_8.n14 (net)                           1
0.0       697.9 f
  intadd_8.syn_14/c (ec0rm0023al1n02x5)                  11.6
0.0 *     698.0 f
  intadd_8.syn_14/carry (ec0rm0023al1n02x5)              11.2
27.5      725.5 f
  intadd_8.n13 (net)                           1
0.0       725.5 f
  intadd_8.syn_13/c (ec0rm0023al1n02x5)                  11.2
0.0 *     725.5 f
  intadd_8.syn_13/carry (ec0rm0023al1n02x5)              11.5
27.6      753.1 f
  intadd_8.n12 (net)                           1
0.0       753.1 f
  intadd_8.syn_12/c (ec0rm0023al1n02x5)                  11.5
0.0 *     753.1 f
  intadd_8.syn_12/carry (ec0rm0023al1n02x5)              12.0
28.2      781.4 f
  intadd_8.n11 (net)                           1
0.0       781.4 f
  intadd_8.syn_11/c (ec0rm0023al1n02x5)                  12.0
0.1 *     781.4 f
  intadd_8.syn_11/carry (ec0rm0023al1n02x5)              11.1
27.5      808.9 f
  intadd_8.n10 (net)                           1
0.0       808.9 f
  intadd_8.syn_10/c (ec0rm0023al1n02x5)                  11.1
0.0 *     808.9 f
  intadd_8.syn_10/carry (ec0rm0023al1n02x5)              11.7
27.8      836.7 f
  intadd_8.n9 (net)                            1
0.0       836.7 f
  intadd_8.syn_9/c (ec0rm0023al1n02x5)                   11.7
0.1 *     836.7 f
  intadd_8.syn_9/carry (ec0rm0023al1n02x5)               11.1
27.4      864.2 f
  intadd_8.n8 (net)                            1
0.0       864.2 f
  intadd_8.syn_8/c (ec0rm0023al1n02x5)                   11.1
0.0 *     864.2 f
  intadd_8.syn_8/carry (ec0rm0023al1n02x5)               11.3
27.4      891.5 f
  intadd_8.n7 (net)                            1
0.0       891.5 f
  intadd_8.syn_7/c (ec0rm0023al1n02x5)                   11.3
0.0 *     891.6 f
  intadd_8.syn_7/carry (ec0rm0023al1n02x5)               11.4
27.5      919.1 f
  intadd_8.n6 (net)                            1
0.0       919.1 f
  intadd_8.syn_6/c (ec0rm0023al1n02x5)                   11.4
0.0 *     919.2 f
  intadd_8.syn_6/carry (ec0rm0023al1n02x5)               11.7
27.9      947.1 f
```

```
  intadd_8.n5 (net)                                1
0.0      947.1 f
  intadd_8.syn_5/c (ec0rm0023al1n02x5)                    11.7
0.1 *    947.1 f
  intadd_8.syn_5/carry (ec0rm0023al1n02x5)                11.4
27.7      974.8 f
  intadd_8.n4 (net)                                1
0.0      974.8 f
  intadd_8.syn_4/c (ec0rm0023al1n02x5)                    11.4
0.0 *    974.8 f
  intadd_8.syn_4/carry (ec0rm0023al1n02x5)                11.4
27.5     1002.3 f
  intadd_8.n3 (net)                                1
0.0     1002.3 f
  intadd_8.syn_3/c (ec0rm0023al1n02x5)                    11.4
0.0 *   1002.4 f
  intadd_8.syn_3/carry (ec0rm0023al1n02x5)                11.1
27.3     1029.6 f
  intadd_8.n2 (net)                                1
0.0     1029.6 f
  intadd_8.syn_2/c (ec0rm0023al1n02x5)                    11.1
0.0 *   1029.7 f
  intadd_8.syn_2/carry (ec0rm0023al1n02x5)                 8.7
24.2     1053.9 f
  intadd_8.n1 (net)                                1
0.0     1053.9 f
  syn_208971/a (ec0bfn000al1n04x5)                         8.7
0.0 *   1053.9 f
  syn_208971/o (ec0bfn000al1n04x5)                         4.9
12.7     1066.6 f
  n313243 (net)                                    1
0.0     1066.6 f
  syn_208972/a (ec0xnr002al1n02x5)                         4.9
0.0 *   1066.6 f
  syn_208972/out0 (ec0xnr002al1n02x5)                     15.0
9.6     1076.2 r
  n313244 (net)                                    1
0.0     1076.2 r
  syn_208973/a (ec0xnr002al1n02x5)                        15.0
0.0 *   1076.2 r
  syn_208973/out0 (ec0xnr002al1n02x5)                     13.9
14.6     1090.8 r
  n313245 (net)                                    1
0.0     1090.8 r
  syn_208974/b (ec0aoi022al2n04x5)                        13.9
0.0 *   1090.9 r
  syn_208974/o1 (ec0aoi022al2n04x5)                       18.6
15.7     1106.6 f
  n313246 (net)                                    1
0.0     1106.6 f
  syn_208975/b (ec0nand02al1n15x5)                        18.6
0.1 *   1106.6 f
  syn_208975/o1 (ec0nand02al1n15x5)                       18.7
20.3     1126.9 r
  n333624 (net)                                    9
0.0     1126.9 r
```

```
  syn_225965/b (ec0nor004al2n02x7)                        19.4
5.6 *   1132.5 r
  syn_225965/o1 (ec0nor004al2n02x7)                       20.2
18.8     1151.3 f
  n300412 (net)                                 1
0.0      1151.3 f
  U210350/b (ec0aoit12al1n09x5)                           20.2
0.1 *    1151.4 f
  U210350/o1 (ec0aoit12al1n09x5)                          25.0
22.9     1174.3 r
  n250487 (net)                                 3
0.0      1174.3 r
  syn_185283/a (ec0nand22al2n03x5)                        25.0
3.2 *    1177.5 r
  syn_185283/o1 (ec0nand22al2n03x5)                       15.9
17.0     1194.5 f
  n308762 (net)                                 1
0.0      1194.5 f
  syn_185284/b (ec0nand02al1n08x5)                        15.9
0.2 *    1194.7 f
  syn_185284/o1 (ec0nand02al1n08x5)                       17.8
17.7     1212.4 r
  n300786 (net)                                 4
0.0      1212.4 r
  syn_185285/b (ec0nand02al1n15x5)                        17.8
0.2 *    1212.6 r
  syn_185285/o1 (ec0nand02al1n15x5)                       25.1
24.5     1237.1 f
  n319469 (net)                                 7
0.0      1237.1 f
  syn_225962/b (ec0aoai13al2n03x5)                        25.3
4.3 *    1241.4 f
  syn_225962/o1 (ec0aoai13al2n03x5)                       18.9
21.1     1262.6 r
  n319470 (net)                                 1
0.0      1262.6 r
  syn_225963/a (ec0oaoi13al2n04x5)                        18.9
0.1 *    1262.6 r
  syn_225963/o1 (ec0oaoi13al2n04x5)                       27.6
17.7     1280.3 f
  n300135 (net)                                 1
0.0      1280.3 f
  U178825/clk1 (ec0cnanc2al2n20x5)                        27.6
0.1 *    1280.4 f
  U178825/clkout (ec0cnanc2al2n20x5)                       0.0
7.0      1287.4 r
  n144251 (net)                                 4
0.0      1287.4 r
  syn_185280/a (ec0nor002al2n06x5)                         0.0
0.0      1287.4 r
  syn_185280/o1 (ec0nor002al2n06x5)                       22.7
16.7     1304.1 f
  n300665 (net)                                 6
0.0      1304.1 f
  syn_185281/a (ec0nand02al1n05x5)                        22.7
0.1 *    1304.2 f
```

```
  syn_185281/o1 (ec0nand02al1n05x5)                          11.6
13.8     1318.0 r
  n319463 (net)                                 2
0.0      1318.0 r
  syn_185282/a (ec0inv000al2n08x5)                           11.6
0.0 *    1318.0 r
  syn_185282/o1 (ec0inv000al2n08x5)                          23.8
23.5     1341.5 f
  n143012 (net)                                12
0.0      1341.5 f
  syn_185292/c (ec0aoi022al2n04x5)                           23.8
0.4 *    1342.0 f
  syn_185292/o1 (ec0aoi022al2n04x5)                          20.5
22.4     1364.4 r
  n308764 (net)                                 1
0.0      1364.4 r
  syn_185293/b (ec0oai112al2n16x5)                           20.5
0.1 *    1364.4 r
  syn_185293/o1 (ec0oai112al2n16x5)                          26.6
25.5     1390.0 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.aux_probe0
_6_0 (net)      1       0.0    1390.0 f
  syn_195113/a (ec0bfn000al1n08x5)                           27.2
6.0 *    1396.0 f
  syn_195113/o (ec0bfn000al1n08x5)                           29.3
39.9     1435.8 f
  n340292 (net)                                11
0.0      1435.8 f
  U167267/b (ec0nor002al1n01x5)                              29.3
0.5 *    1436.3 f
  U167267/o1 (ec0nor002al1n01x5)                             21.9
24.3     1460.7 r
  n148105 (net)                                 1
0.0      1460.7 r
  syn_211132/b (ec0nanb02al1n05x5)                           21.9
0.0 *    1460.7 r
  syn_211132/out0 (ec0nanb02al1n05x5)                        12.5
14.4     1475.0 f
  n148106 (net)                                 2
0.0      1475.0 f
  syn_211133/b (ec0nor002al2n06x5)                           12.5
0.0 *    1475.0 f
  syn_211133/o1 (ec0nor002al2n06x5)                          23.2
21.7     1496.7 r
  n315706 (net)                                 3
0.0      1496.7 r
  syn_217505/b (ec0nand02al1n15x5)                           23.2
0.4 *    1497.1 r
  syn_217505/o1 (ec0nand02al1n15x5)                          23.5
23.3     1520.4 f
  n147798 (net)                                 3
0.0      1520.4 f
  U167278/b (ec0qbfno2bl2n18x5)                              28.7
14.2 *   1534.6 f
```

```
  U167278/o1 (ec0qbfno2bl2n18x5)                          27.1
33.6     1568.2 r
  n192581 (net)                                  8
0.0      1568.2 r
  syn_243547/a (ec0bfn000al1n06x5)                        27.1
0.5 *    1568.7 r
  syn_243547/o (ec0bfn000al1n06x5)                        24.6
32.7     1601.4 r
  n358712 (net)                                 15
0.0      1601.4 r
  U167484/a (ec0qsfca4cl2n06x5)                           24.6
0.9 *    1602.3 r
  U167484/o1 (ec0qsfca4cl2n06x5)                          25.1
25.6     1627.9 f
  n147862 (net)                                  1
0.0      1627.9 f
  U167485/a (ec0oai012al1n01x3)                           25.1
0.5 *    1628.4 f
  U167485/o1 (ec0oai012al1n01x3)                          22.9
17.5     1645.9 r
  n147863 (net)                                  1
0.0      1645.9 r
  U167486/a (ec0aoi012al1n01x5)                           22.9
0.0 *    1646.0 r
  U167486/o1 (ec0aoi012al1n01x5)                          18.8
17.2     1663.2 f
  n148053 (net)                                  1
0.0      1663.2 f
  syn_258036/a (ec0bfn000al1n04x5)                        18.8
0.0 *    1663.2 f
  syn_258036/o (ec0bfn000al1n04x5)                         6.5
16.8     1680.0 f
  n373085 (net)                                  1
0.0      1680.0 f
  syn_228945/a (ec0bfn000al1n04x5)                         6.5
0.2 *    1680.2 f
  syn_228945/o (ec0bfn000al1n04x5)                        15.4
20.6     1700.8 f
  n349068 (net)                                  1
0.0      1700.8 f
  syn_248308/a (ec0bfn000al1n08x5)                        15.4
1.9 *    1702.7 f
  syn_248308/o (ec0bfn000al1n08x5)                        13.9
24.9     1727.7 f
  n363566 (net)                                  6
0.0      1727.7 f
  syn_222430/b (ec0nor002al1n03x7)                        13.9
0.2 *    1727.9 f
  syn_222430/o1 (ec0nor002al1n03x7)                       21.8
20.7     1748.6 r
  n317915 (net)                                  2
0.0      1748.6 r
  syn_222608/a (ec0nand02al1n08x5)                        21.8
0.1 *    1748.7 r
  syn_222608/o1 (ec0nand02al1n08x5)                       28.6
28.0     1776.7 f
```

```
  n251131 (net)                                  14
0.0     1776.7 f
  U296343/a (ec0nanb02al1n01x3)                                28.6
0.6 *   1777.3 f
  U296343/out0 (ec0nanb02al1n01x3)                             17.7
25.5     1802.8 f
  n251132 (net)                                   1
0.0     1802.8 f
  syn_202393/a (ec0bfn000al1n04x5)                             17.7
0.0 *   1802.8 f
  syn_202393/o (ec0bfn000al1n04x5)                              4.2
14.2     1817.0 f
  n342349 (net)                                   1
0.0     1817.0 f
  syn_224911/a (ec0bfn000al1n08x5)                              4.2
0.0 *   1817.0 f
  syn_224911/o (ec0bfn000al1n08x5)                              5.1
13.0     1830.0 f
  n348052 (net)                                   3
0.0     1830.0 f
  syn_248088/a (ec0bfn000al1n04x5)                              5.1
0.0 *   1830.0 f
  syn_248088/o (ec0bfn000al1n04x5)                             18.7
22.6     1852.6 f
  n363335 (net)                                  15
0.0     1852.6 f
  U296351/b (ec0nor002al1n01x5)                                18.7
0.2 *   1852.8 f
  U296351/o1 (ec0nor002al1n01x5)                               18.8
21.1     1873.9 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.addr_vec_and
_wr_en_229_0 (net)      1      0.0   1873.9 r
  syn_221256/a (ec0bfn000al1n04x5)                             18.8
0.0 *   1873.9 r
  syn_221256/o (ec0bfn000al1n04x5)                              7.1
16.9     1890.8 r
  n347584 (net)                                   1
0.0     1890.8 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_229.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/en (ec0cnan02al1n06x5)      7.1      0.0 *
1890.8 r
  data arrival time
1890.8

  clock ascan_preclk_mgmt_clk' (rise edge)
2163.0     2163.0
  clock network delay (ideal)
0.0     2163.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
```

```
k_and_en_229.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/clk (ec0cnan02al1n06x5)      0.0   2163.0 r
  library nochange setup time
0.3     2163.3
  data required time
2163.3
  ------------------------------------------------------------
------------------------
  data required time
2163.3
  data arrival time
-1890.8
  ------------------------------------------------------------
------------------------
  slack (MET)
272.5


  Startpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0
              (rising edge-triggered flip-flop clocked by
ascan_preclk_mgmt_clk)
  Endpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_240.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo
            (positive nochange timing check for clock
ascan_preclk_mgmt_clk')
  Path Group: ascan_preclk_mgmt_clk
  Path Type: max

  Point                                          Fanout     Trans
Incr       Path
  ------------------------------------------------------------
------------------------
  clock ascan_preclk_mgmt_clk (rise edge)
0.0        0.0
  clock network delay (ideal)
0.0        0.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/clk
(ec0faw003al2n03x5)      0.0      0.0      0.0 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/o
(ec0faw003al2n03x5)      7.2     18.2     18.2 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.returnFromOCD_C2 (net)     2      0.0     18.2
f
  U145922/b (ec0nor002al1n01x5)                              7.2
0.0 *     18.2 f
```

```
  U145922/o1 (ec0nor002al1n01x5)                          15.4
15.9       34.1 r
  n160623 (net)                                 1
0.0        34.1 r
  syn_253469/a (ec0bfn000al1n04x5)                        15.4
0.0 *      34.1 r
  syn_253469/o (ec0bfn000al1n04x5)                         8.6
17.6       51.7 r
  n368824 (net)                                 2
0.0        51.7 r
  syn_186517/c (ec0nand03al1n12x5)                         8.6
0.0 *      51.7 r
  syn_186517/o1 (ec0nand03al1n12x5)                       24.7
23.6       75.3 f
  n309155 (net)                                 4
0.0        75.3 f
  syn_184533/a (ec0bfn000al1n08x5)                        24.7
3.2 *      78.6 f
  syn_184533/o (ec0bfn000al1n08x5)                        20.4
32.6      111.2 f
  n336143 (net)                                 9
0.0       111.2 f
  syn_184534/a (ec0inv000al2n08x5)                        20.4
2.4 *     113.6 f
  syn_184534/o1 (ec0inv000al2n08x5)                       14.1
15.9      129.5 r
  n336144 (net)                                 6
0.0       129.5 r
  syn_226018/a (ec0aoi022al2n08x5)                        14.1
0.0 *     129.5 r
  syn_226018/o1 (ec0aoi022al2n08x5)                       23.1
22.2      151.7 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PC_E_1_0 (net)      5       0.0    151.7 f
  U145990/b (ec0qbfno2bl2n18x5)                           23.1
2.6 *     154.4 f
  U145990/o1 (ec0qbfno2bl2n18x5)                          19.5
25.8      180.1 r
  n173989 (net)                                 4
0.0       180.1 r
  U145991/c (ec0oai022al2n01x3)                           19.5
2.0 *     182.1 r
  U145991/o1 (ec0oai022al2n01x3)                          26.8
27.2      209.3 f
  n142897 (net)                                 1
0.0       209.3 f
  syn_250934/a (ec0bfn000al1n04x5)                        26.8
0.0 *     209.4 f
  syn_250934/o (ec0bfn000al1n04x5)                        19.1
28.6      237.9 f
  n366256 (net)                                 3
0.0       237.9 f
  syn_226009/a (ec0oaoi03al2n02x5)                        19.1
0.1 *     238.0 f
```

```
  syn_226009/o1 (ec0oaoi03al2n02x5)                       32.4
29.8      267.8 r
  intadd_22.B_0_ (net)                             1
0.0       267.8 r
  intadd_22.syn_6/a (ec0rm0023al1n04x7)                   32.4
0.0 *     267.8 r
  intadd_22.syn_6/carry (ec0rm0023al1n04x7)                7.8
24.3      292.1 r
  intadd_22.n5 (net)                               1
0.0       292.1 r
  intadd_22.syn_5/c (ec0rm0023al1n02x5)                    7.8
0.0 *     292.1 r
  intadd_22.syn_5/carry (ec0rm0023al1n02x5)               10.9
24.1      316.3 r
  intadd_22.n4 (net)                               1
0.0       316.3 r
  intadd_22.syn_4/c (ec0rm0023al1n02x5)                   10.9
0.0 *     316.3 r
  intadd_22.syn_4/carry (ec0rm0023al1n02x5)               11.2
25.6      341.9 r
  intadd_22.n3 (net)                               1
0.0       341.9 r
  intadd_22.syn_3/c (ec0rm0023al1n02x5)                   11.2
0.0 *     342.0 r
  intadd_22.syn_3/carry (ec0rm0023al1n02x5)               14.7
28.9      370.9 r
  intadd_22.n2 (net)                               1
0.0       370.9 r
  intadd_22.syn_2/c (ec0rm0023al1n04x7)                   14.7
0.1 *     371.0 r
  intadd_22.syn_2/carry (ec0rm0023al1n04x7)                6.5
20.5      391.4 r
  intadd_22.n1 (net)                               1
0.0       391.4 r
  syn_226005/a (ec0bfn000al1n04x5)                         6.5
0.0 *     391.5 r
  syn_226005/o (ec0bfn000al1n04x5)                         6.1
13.2      404.6 r
  n319486 (net)                                    1
0.0       404.6 r
  syn_226006/a (ec0inv000al2n08x5)                         6.1
0.0 *     404.7 r
  syn_226006/o1 (ec0inv000al2n08x5)                        3.6
4.6       409.3 f
  n142848 (net)                                    3
0.0       409.3 f
  U263389/b (ec0orn002al1n01x3)                            3.6
0.0 *     409.3 f
  U263389/o (ec0orn002al1n01x3)                           10.4
21.8      431.0 f
  n300566 (net)                                    1
0.0       431.0 f
  syn_226001/c (ec0ao0012al2n04x5)                        10.4
0.0 *     431.1 f
  syn_226001/o (ec0ao0012al2n04x5)                         8.3
21.5      452.5 f
```

```
  intadd_8.CI (net)                                1
0.0      452.5 f
  intadd_8.syn_23/c (ec0rm0023al1n04x7)                8.3
0.0 *    452.6 f
  intadd_8.syn_23/carry (ec0rm0023al1n04x7)            8.1
22.1      474.7 f
  intadd_8.n22 (net)                               1
0.0      474.7 f
  intadd_8.syn_22/c (ec0rm0023al1n02x5)                8.1
0.0 *    474.7 f
  intadd_8.syn_22/carry (ec0rm0023al1n02x5)           11.9
26.9      501.6 f
  intadd_8.n21 (net)                               1
0.0      501.6 f
  intadd_8.syn_21/c (ec0rm0023al1n02x5)               11.9
0.1 *    501.7 f
  intadd_8.syn_21/carry (ec0rm0023al1n02x5)           12.4
28.7      530.4 f
  intadd_8.n20 (net)                               1
0.0      530.4 f
  intadd_8.syn_20/c (ec0rm0023al1n02x5)               12.4
0.1 *    530.5 f
  intadd_8.syn_20/carry (ec0rm0023al1n02x5)           11.9
28.4      558.9 f
  intadd_8.n19 (net)                               1
0.0      558.9 f
  intadd_8.syn_19/c (ec0rm0023al1n02x5)               11.9
0.1 *    558.9 f
  intadd_8.syn_19/carry (ec0rm0023al1n02x5)           11.2
27.5      586.4 f
  intadd_8.n18 (net)                               1
0.0      586.4 f
  intadd_8.syn_18/c (ec0rm0023al1n02x5)               11.2
0.0 *    586.5 f
  intadd_8.syn_18/carry (ec0rm0023al1n02x5)           11.5
27.6      614.1 f
  intadd_8.n17 (net)                               1
0.0      614.1 f
  intadd_8.syn_17/c (ec0rm0023al1n02x5)               11.5
0.0 *    614.1 f
  intadd_8.syn_17/carry (ec0rm0023al1n02x5)           12.1
28.2      642.3 f
  intadd_8.n16 (net)                               1
0.0      642.3 f
  intadd_8.syn_16/c (ec0rm0023al1n02x5)               12.1
0.1 *    642.4 f
  intadd_8.syn_16/carry (ec0rm0023al1n02x5)           11.4
27.7      670.1 f
  intadd_8.n15 (net)                               1
0.0      670.1 f
  intadd_8.syn_15/c (ec0rm0023al1n02x5)               11.4
0.0 *    670.1 f
  intadd_8.syn_15/carry (ec0rm0023al1n02x5)           11.6
27.8      697.9 f
  intadd_8.n14 (net)                               1
0.0      697.9 f
```

```
  intadd_8.syn_14/c (ec0rm0023al1n02x5)                   11.6
0.0 *    698.0 f
  intadd_8.syn_14/carry (ec0rm0023al1n02x5)               11.2
27.5      725.5 f
  intadd_8.n13 (net)                              1
0.0       725.5 f
  intadd_8.syn_13/c (ec0rm0023al1n02x5)                   11.2
0.0 *    725.5 f
  intadd_8.syn_13/carry (ec0rm0023al1n02x5)               11.5
27.6      753.1 f
  intadd_8.n12 (net)                              1
0.0       753.1 f
  intadd_8.syn_12/c (ec0rm0023al1n02x5)                   11.5
0.0 *    753.1 f
  intadd_8.syn_12/carry (ec0rm0023al1n02x5)               12.0
28.2      781.4 f
  intadd_8.n11 (net)                              1
0.0       781.4 f
  intadd_8.syn_11/c (ec0rm0023al1n02x5)                   12.0
0.1 *    781.4 f
  intadd_8.syn_11/carry (ec0rm0023al1n02x5)               11.1
27.5      808.9 f
  intadd_8.n10 (net)                              1
0.0       808.9 f
  intadd_8.syn_10/c (ec0rm0023al1n02x5)                   11.1
0.0 *    808.9 f
  intadd_8.syn_10/carry (ec0rm0023al1n02x5)               11.7
27.8      836.7 f
  intadd_8.n9 (net)                               1
0.0       836.7 f
  intadd_8.syn_9/c (ec0rm0023al1n02x5)                    11.7
0.1 *    836.7 f
  intadd_8.syn_9/carry (ec0rm0023al1n02x5)                11.1
27.4      864.2 f
  intadd_8.n8 (net)                               1
0.0       864.2 f
  intadd_8.syn_8/c (ec0rm0023al1n02x5)                    11.1
0.0 *    864.2 f
  intadd_8.syn_8/carry (ec0rm0023al1n02x5)                11.3
27.4      891.5 f
  intadd_8.n7 (net)                               1
0.0       891.5 f
  intadd_8.syn_7/c (ec0rm0023al1n02x5)                    11.3
0.0 *    891.6 f
  intadd_8.syn_7/carry (ec0rm0023al1n02x5)                11.4
27.5      919.1 f
  intadd_8.n6 (net)                               1
0.0       919.1 f
  intadd_8.syn_6/c (ec0rm0023al1n02x5)                    11.4
0.0 *    919.2 f
  intadd_8.syn_6/carry (ec0rm0023al1n02x5)                11.7
27.9      947.1 f
  intadd_8.n5 (net)                               1
0.0       947.1 f
  intadd_8.syn_5/c (ec0rm0023al1n02x5)                    11.7
0.1 *    947.1 f
```

```
  intadd_8.syn_5/carry (ec0rm0023al1n02x5)                11.4
27.7      974.8 f
  intadd_8.n4 (net)                                  1
0.0       974.8 f
  intadd_8.syn_4/c (ec0rm0023al1n02x5)                    11.4
0.0 *     974.8 f
  intadd_8.syn_4/carry (ec0rm0023al1n02x5)                11.4
27.5     1002.3 f
  intadd_8.n3 (net)                                  1
0.0      1002.3 f
  intadd_8.syn_3/c (ec0rm0023al1n02x5)                    11.4
0.0 *    1002.4 f
  intadd_8.syn_3/carry (ec0rm0023al1n02x5)                11.1
27.3     1029.6 f
  intadd_8.n2 (net)                                  1
0.0      1029.6 f
  intadd_8.syn_2/c (ec0rm0023al1n02x5)                    11.1
0.0 *    1029.7 f
  intadd_8.syn_2/carry (ec0rm0023al1n02x5)                 8.7
24.2     1053.9 f
  intadd_8.n1 (net)                                  1
0.0      1053.9 f
  syn_208971/a (ec0bfn000al1n04x5)                         8.7
0.0 *    1053.9 f
  syn_208971/o (ec0bfn000al1n04x5)                         4.9
12.7     1066.6 f
  n313243 (net)                                      1
0.0      1066.6 f
  syn_208972/a (ec0xnr002al1n02x5)                         4.9
0.0 *    1066.6 f
  syn_208972/out0 (ec0xnr002al1n02x5)                     15.0
9.6      1076.2 r
  n313244 (net)                                      1
0.0      1076.2 r
  syn_208973/a (ec0xnr002al1n02x5)                        15.0
0.0 *    1076.2 r
  syn_208973/out0 (ec0xnr002al1n02x5)                     13.9
14.6     1090.8 r
  n313245 (net)                                      1
0.0      1090.8 r
  syn_208974/b (ec0aoi022al2n04x5)                        13.9
0.0 *    1090.9 r
  syn_208974/o1 (ec0aoi022al2n04x5)                       18.6
15.7     1106.6 f
  n313246 (net)                                      1
0.0      1106.6 f
  syn_208975/b (ec0nand02al1n15x5)                        18.6
0.1 *    1106.6 f
  syn_208975/o1 (ec0nand02al1n15x5)                       18.7
20.3     1126.9 r
  n333624 (net)                                      9
0.0      1126.9 r
  syn_225965/b (ec0nor004al2n02x7)                        19.4
5.6 *    1132.5 r
  syn_225965/o1 (ec0nor004al2n02x7)                       20.2
18.8     1151.3 f
```

```
  n300412 (net)                                  1
0.0     1151.3 f
  U210350/b (ec0aoit12al1n09x5)                                20.2
0.1 *   1151.4 f
  U210350/o1 (ec0aoit12al1n09x5)                               25.0
22.9     1174.3 r
  n250487 (net)                                  3
0.0     1174.3 r
  syn_185283/a (ec0nand22al2n03x5)                             25.0
3.2 *   1177.5 r
  syn_185283/o1 (ec0nand22al2n03x5)                            15.9
17.0     1194.5 f
  n308762 (net)                                  1
0.0     1194.5 f
  syn_185284/b (ec0nand02al1n08x5)                             15.9
0.2 *   1194.7 f
  syn_185284/o1 (ec0nand02al1n08x5)                            17.8
17.7     1212.4 r
  n300786 (net)                                  4
0.0     1212.4 r
  syn_185285/b (ec0nand02al1n15x5)                             17.8
0.2 *   1212.6 r
  syn_185285/o1 (ec0nand02al1n15x5)                            25.1
24.5     1237.1 f
  n319469 (net)                                  7
0.0     1237.1 f
  syn_225962/b (ec0aoai13al2n03x5)                             25.3
4.3 *   1241.4 f
  syn_225962/o1 (ec0aoai13al2n03x5)                            18.9
21.1     1262.6 r
  n319470 (net)                                  1
0.0     1262.6 r
  syn_225963/a (ec0oaoi13al2n04x5)                             18.9
0.1 *   1262.6 r
  syn_225963/o1 (ec0oaoi13al2n04x5)                            27.6
17.7     1280.3 f
  n300135 (net)                                  1
0.0     1280.3 f
  U178825/clk1 (ec0cnanc2al2n20x5)                             27.6
0.1 *   1280.4 f
  U178825/clkout (ec0cnanc2al2n20x5)                            0.0
7.0     1287.4 r
  n144251 (net)                                  4
0.0     1287.4 r
  syn_185280/a (ec0nor002al2n06x5)                              0.0
0.0     1287.4 r
  syn_185280/o1 (ec0nor002al2n06x5)                            22.7
16.7     1304.1 f
  n300665 (net)                                  6
0.0     1304.1 f
  syn_185281/a (ec0nand02al1n05x5)                             22.7
0.1 *   1304.2 f
  syn_185281/o1 (ec0nand02al1n05x5)                            11.6
13.8     1318.0 r
  n319463 (net)                                  2
0.0     1318.0 r
```

```
  syn_185282/a (ec0inv000al2n08x5)                          11.6
0.0 *   1318.0 r
  syn_185282/o1 (ec0inv000al2n08x5)                         23.8
23.5     1341.5 f
  n143012 (net)                                  12
0.0      1341.5 f
  syn_185292/c (ec0aoi022al2n04x5)                          23.8
0.4 *   1342.0 f
  syn_185292/o1 (ec0aoi022al2n04x5)                         20.5
22.4     1364.4 r
  n308764 (net)                                   1
0.0      1364.4 r
  syn_185293/b (ec0oai112al2n16x5)                          20.5
0.1 *   1364.4 r
  syn_185293/o1 (ec0oai112al2n16x5)                         26.6
25.5     1390.0 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.aux_probe0
_6_0 (net)      1      0.0   1390.0 f
  syn_195113/a (ec0bfn000al1n08x5)                          27.2
6.0 *   1396.0 f
  syn_195113/o (ec0bfn000al1n08x5)                          29.3
39.9     1435.8 f
  n340292 (net)                                  11
0.0      1435.8 f
  U167267/b (ec0nor002al1n01x5)                             29.3
0.5 *   1436.3 f
  U167267/o1 (ec0nor002al1n01x5)                            21.9
24.3     1460.7 r
  n148105 (net)                                   1
0.0      1460.7 r
  syn_211132/b (ec0nanb02al1n05x5)                          21.9
0.0 *   1460.7 r
  syn_211132/out0 (ec0nanb02al1n05x5)                       12.5
14.4     1475.0 f
  n148106 (net)                                   2
0.0      1475.0 f
  syn_211133/b (ec0nor002al2n06x5)                          12.5
0.0 *   1475.0 f
  syn_211133/o1 (ec0nor002al2n06x5)                         23.2
21.7     1496.7 r
  n315706 (net)                                   3
0.0      1496.7 r
  syn_217505/b (ec0nand02al1n15x5)                          23.2
0.4 *   1497.1 r
  syn_217505/o1 (ec0nand02al1n15x5)                         23.5
23.3     1520.4 f
  n147798 (net)                                   3
0.0      1520.4 f
  U167278/b (ec0qbfno2bl2n18x5)                             28.7
14.2 *   1534.6 f
  U167278/o1 (ec0qbfno2bl2n18x5)                            27.1
33.6     1568.2 r
  n192581 (net)                                   8
0.0      1568.2 r
```

```
  syn_243547/a (ec0bfn000al1n06x5)                        27.1
0.5 *   1568.7 r
  syn_243547/o (ec0bfn000al1n06x5)                        24.6
32.7     1601.4 r
  n358712 (net)                                 15
0.0     1601.4 r
  U167484/a (ec0qsfca4cl2n06x5)                           24.6
0.9 *   1602.3 r
  U167484/o1 (ec0qsfca4cl2n06x5)                          25.1
25.6     1627.9 f
  n147862 (net)                                  1
0.0     1627.9 f
  U167485/a (ec0oai012al1n01x3)                           25.1
0.5 *   1628.4 f
  U167485/o1 (ec0oai012al1n01x3)                          22.9
17.5     1645.9 r
  n147863 (net)                                  1
0.0     1645.9 r
  U167486/a (ec0aoi012al1n01x5)                           22.9
0.0 *   1646.0 r
  U167486/o1 (ec0aoi012al1n01x5)                          18.8
17.2     1663.2 f
  n148053 (net)                                  1
0.0     1663.2 f
  syn_258036/a (ec0bfn000al1n04x5)                        18.8
0.0 *   1663.2 f
  syn_258036/o (ec0bfn000al1n04x5)                         6.5
16.8     1680.0 f
  n373085 (net)                                  1
0.0     1680.0 f
  syn_228945/a (ec0bfn000al1n04x5)                         6.5
0.2 *   1680.2 f
  syn_228945/o (ec0bfn000al1n04x5)                        15.4
20.6     1700.8 f
  n349068 (net)                                  1
0.0     1700.8 f
  syn_248308/a (ec0bfn000al1n08x5)                        15.4
1.9 *   1702.7 f
  syn_248308/o (ec0bfn000al1n08x5)                        13.9
24.9     1727.7 f
  n363566 (net)                                  6
0.0     1727.7 f
  syn_222430/b (ec0nor002al1n03x7)                        13.9
0.2 *   1727.9 f
  syn_222430/o1 (ec0nor002al1n03x7)                       21.8
20.7     1748.6 r
  n317915 (net)                                  2
0.0     1748.6 r
  syn_222608/a (ec0nand02al1n08x5)                        21.8
0.1 *   1748.7 r
  syn_222608/o1 (ec0nand02al1n08x5)                       28.6
28.0     1776.7 f
  n251131 (net)                                 14
0.0     1776.7 f
  U296343/a (ec0nanb02al1n01x3)                           28.6
0.6 *   1777.3 f
```

```
  U296343/out0 (ec0nanb02al1n01x3)                          17.7
25.5     1802.8 f
  n251132 (net)                                        1
0.0      1802.8 f
  syn_202393/a (ec0bfn000al1n04x5)                          17.7
0.0 *    1802.8 f
  syn_202393/o (ec0bfn000al1n04x5)                           4.2
14.2     1817.0 f
  n342349 (net)                                        1
0.0      1817.0 f
  syn_224911/a (ec0bfn000al1n08x5)                           4.2
0.0 *    1817.0 f
  syn_224911/o (ec0bfn000al1n08x5)                           5.1
13.0     1830.0 f
  n348052 (net)                                        3
0.0      1830.0 f
  syn_248089/a (ec0bfn000al1n04x5)                           5.1
0.0 *    1830.0 f
  syn_248089/o (ec0bfn000al1n04x5)                          18.9
22.7     1852.7 f
  n363336 (net)                                       15
0.0      1852.7 f
  U296363/b (ec0nor002al1n01x5)                             18.9
0.2 *    1853.0 f
  U296363/o1 (ec0nor002al1n01x5)                            18.1
20.6     1873.6 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.addr_vec_and
_wr_en_240_0 (net)      1       0.0    1873.6 r
  syn_219548/a (ec0bfn000al1n04x5)                          18.1
0.0 *    1873.6 r
  syn_219548/o (ec0bfn000al1n04x5)                           7.1
16.8     1890.4 r
  n347214 (net)                                        1
0.0      1890.4 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_240.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/en (ec0cnan02al1n06x5)       7.1       0.0 *
1890.4 r
  data arrival time
1890.4

  clock ascan_preclk_mgmt_clk' (rise edge)
2163.0     2163.0
  clock network delay (ideal)
0.0      2163.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_240.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/clk (ec0cnan02al1n06x5)      0.0    2163.0 r
  library nochange setup time
0.3      2163.3
```

```
  data required time
2163.3
  ------------------------------------------------------------
------------------------
  data required time
2163.3
  data arrival time
-1890.4
  ------------------------------------------------------------
------------------------
  slack (MET)
272.9


  Startpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0
              (rising edge-triggered flip-flop clocked by
ascan_preclk_mgmt_clk)
  Endpoint:
physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_244.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo
             (positive nochange timing check for clock
ascan_preclk_mgmt_clk')
  Path Group: ascan_preclk_mgmt_clk
  Path Type: max

  Point                                          Fanout     Trans
Incr       Path
  ------------------------------------------------------------
------------------------
  clock ascan_preclk_mgmt_clk (rise edge)
0.0        0.0
  clock network delay (ideal)
0.0        0.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/clk
(ec0faw003al2n03x5)      0.0      0.0      0.0 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.InstFetch.returnFromOCD_C2_reg.tmp_reg_0/o
(ec0faw003al2n03x5)      7.2     18.2     18.2 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PCandIFetch.returnFromOCD_C2 (net)     2      0.0     18.2
f
  U145922/b (ec0nor002al1n01x5)                               7.2
0.0 *      18.2 f
  U145922/o1 (ec0nor002al1n01x5)                             15.4
15.9       34.1 r
  n160623 (net)                                 1
0.0        34.1 r
```

```
  syn_253469/a (ec0bfn000al1n04x5)                        15.4
0.0 *     34.1 r
  syn_253469/o (ec0bfn000al1n04x5)                         8.6
17.6       51.7 r
  n368824 (net)                                 2
0.0       51.7 r
  syn_186517/c (ec0nand03al1n12x5)                         8.6
0.0 *     51.7 r
  syn_186517/o1 (ec0nand03al1n12x5)                       24.7
23.6       75.3 f
  n309155 (net)                                 4
0.0       75.3 f
  syn_184533/a (ec0bfn000al1n08x5)                        24.7
3.2 *     78.6 f
  syn_184533/o (ec0bfn000al1n08x5)                        20.4
32.6      111.2 f
  n336143 (net)                                 9
0.0      111.2 f
  syn_184534/a (ec0inv000al2n08x5)                        20.4
2.4 *     113.6 f
  syn_184534/o1 (ec0inv000al2n08x5)                       14.1
15.9      129.5 r
  n336144 (net)                                 6
0.0      129.5 r
  syn_226018/a (ec0aoi022al2n08x5)                        14.1
0.0 *     129.5 r
  syn_226018/o1 (ec0aoi022al2n08x5)                       23.1
22.2      151.7 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.Xttop.Xten
sa.PC_E_1_0 (net)     5      0.0    151.7 f
  U145990/b (ec0qbfno2bl2n18x5)                           23.1
2.6 *     154.4 f
  U145990/o1 (ec0qbfno2bl2n18x5)                          19.5
25.8      180.1 r
  n173989 (net)                                 4
0.0      180.1 r
  U145991/c (ec0oai022al2n01x3)                           19.5
2.0 *     182.1 r
  U145991/o1 (ec0oai022al2n01x3)                          26.8
27.2      209.3 f
  n142897 (net)                                 1
0.0      209.3 f
  syn_250934/a (ec0bfn000al1n04x5)                        26.8
0.0 *     209.4 f
  syn_250934/o (ec0bfn000al1n04x5)                        19.1
28.6      237.9 f
  n366256 (net)                                 3
0.0      237.9 f
  syn_226009/a (ec0oaoi03al2n02x5)                        19.1
0.1 *     238.0 f
  syn_226009/o1 (ec0oaoi03al2n02x5)                       32.4
29.8      267.8 r
  intadd_22.B_0_ (net)                          1
0.0      267.8 r
```

```
  intadd_22.syn_6/a (ec0rm0023al1n04x7)                    32.4
0.0 *    267.8 r
  intadd_22.syn_6/carry (ec0rm0023al1n04x7)                 7.8
24.3      292.1 r
  intadd_22.n5 (net)                              1
0.0       292.1 r
  intadd_22.syn_5/c (ec0rm0023al1n02x5)                     7.8
0.0 *    292.1 r
  intadd_22.syn_5/carry (ec0rm0023al1n02x5)                10.9
24.1      316.3 r
  intadd_22.n4 (net)                              1
0.0       316.3 r
  intadd_22.syn_4/c (ec0rm0023al1n02x5)                    10.9
0.0 *    316.3 r
  intadd_22.syn_4/carry (ec0rm0023al1n02x5)                11.2
25.6      341.9 r
  intadd_22.n3 (net)                              1
0.0       341.9 r
  intadd_22.syn_3/c (ec0rm0023al1n02x5)                    11.2
0.0 *    342.0 r
  intadd_22.syn_3/carry (ec0rm0023al1n02x5)                14.7
28.9      370.9 r
  intadd_22.n2 (net)                              1
0.0       370.9 r
  intadd_22.syn_2/c (ec0rm0023al1n04x7)                    14.7
0.1 *    371.0 r
  intadd_22.syn_2/carry (ec0rm0023al1n04x7)                 6.5
20.5      391.4 r
  intadd_22.n1 (net)                              1
0.0       391.4 r
  syn_226005/a (ec0bfn000al1n04x5)                          6.5
0.0 *    391.5 r
  syn_226005/o (ec0bfn000al1n04x5)                          6.1
13.2      404.6 r
  n319486 (net)                                   1
0.0       404.6 r
  syn_226006/a (ec0inv000al2n08x5)                          6.1
0.0 *    404.7 r
  syn_226006/o1 (ec0inv000al2n08x5)                         3.6
4.6       409.3 f
  n142848 (net)                                   3
0.0       409.3 f
  U263389/b (ec0orn002al1n01x3)                             3.6
0.0 *    409.3 f
  U263389/o (ec0orn002al1n01x3)                            10.4
21.8      431.0 f
  n300566 (net)                                   1
0.0       431.0 f
  syn_226001/c (ec0ao0012al2n04x5)                         10.4
0.0 *    431.1 f
  syn_226001/o (ec0ao0012al2n04x5)                          8.3
21.5      452.5 f
  intadd_8.CI (net)                               1
0.0       452.5 f
  intadd_8.syn_23/c (ec0rm0023al1n04x7)                     8.3
0.0 *    452.6 f
```

```
  intadd_8.syn_23/carry (ec0rm0023al1n04x7)                8.1
22.1      474.7 f
  intadd_8.n22 (net)                              1
0.0       474.7 f
  intadd_8.syn_22/c (ec0rm0023al1n02x5)                    8.1
0.0 *     474.7 f
  intadd_8.syn_22/carry (ec0rm0023al1n02x5)               11.9
26.9      501.6 f
  intadd_8.n21 (net)                              1
0.0       501.6 f
  intadd_8.syn_21/c (ec0rm0023al1n02x5)                   11.9
0.1 *     501.7 f
  intadd_8.syn_21/carry (ec0rm0023al1n02x5)               12.4
28.7      530.4 f
  intadd_8.n20 (net)                              1
0.0       530.4 f
  intadd_8.syn_20/c (ec0rm0023al1n02x5)                   12.4
0.1 *     530.5 f
  intadd_8.syn_20/carry (ec0rm0023al1n02x5)               11.9
28.4      558.9 f
  intadd_8.n19 (net)                              1
0.0       558.9 f
  intadd_8.syn_19/c (ec0rm0023al1n02x5)                   11.9
0.1 *     558.9 f
  intadd_8.syn_19/carry (ec0rm0023al1n02x5)               11.2
27.5      586.4 f
  intadd_8.n18 (net)                              1
0.0       586.4 f
  intadd_8.syn_18/c (ec0rm0023al1n02x5)                   11.2
0.0 *     586.5 f
  intadd_8.syn_18/carry (ec0rm0023al1n02x5)               11.5
27.6      614.1 f
  intadd_8.n17 (net)                              1
0.0       614.1 f
  intadd_8.syn_17/c (ec0rm0023al1n02x5)                   11.5
0.0 *     614.1 f
  intadd_8.syn_17/carry (ec0rm0023al1n02x5)               12.1
28.2      642.3 f
  intadd_8.n16 (net)                              1
0.0       642.3 f
  intadd_8.syn_16/c (ec0rm0023al1n02x5)                   12.1
0.1 *     642.4 f
  intadd_8.syn_16/carry (ec0rm0023al1n02x5)               11.4
27.7      670.1 f
  intadd_8.n15 (net)                              1
0.0       670.1 f
  intadd_8.syn_15/c (ec0rm0023al1n02x5)                   11.4
0.0 *     670.1 f
  intadd_8.syn_15/carry (ec0rm0023al1n02x5)               11.6
27.8      697.9 f
  intadd_8.n14 (net)                              1
0.0       697.9 f
  intadd_8.syn_14/c (ec0rm0023al1n02x5)                   11.6
0.0 *     698.0 f
  intadd_8.syn_14/carry (ec0rm0023al1n02x5)               11.2
27.5      725.5 f
```

```
  intadd_8.n13 (net)                              1
0.0      725.5 f
  intadd_8.syn_13/c (ec0rm0023al1n02x5)                  11.2
0.0 *    725.5 f
  intadd_8.syn_13/carry (ec0rm0023al1n02x5)              11.5
27.6      753.1 f
  intadd_8.n12 (net)                              1
0.0      753.1 f
  intadd_8.syn_12/c (ec0rm0023al1n02x5)                  11.5
0.0 *    753.1 f
  intadd_8.syn_12/carry (ec0rm0023al1n02x5)              12.0
28.2      781.4 f
  intadd_8.n11 (net)                              1
0.0      781.4 f
  intadd_8.syn_11/c (ec0rm0023al1n02x5)                  12.0
0.1 *    781.4 f
  intadd_8.syn_11/carry (ec0rm0023al1n02x5)              11.1
27.5      808.9 f
  intadd_8.n10 (net)                              1
0.0      808.9 f
  intadd_8.syn_10/c (ec0rm0023al1n02x5)                  11.1
0.0 *    808.9 f
  intadd_8.syn_10/carry (ec0rm0023al1n02x5)              11.7
27.8      836.7 f
  intadd_8.n9 (net)                               1
0.0      836.7 f
  intadd_8.syn_9/c (ec0rm0023al1n02x5)                   11.7
0.1 *    836.7 f
  intadd_8.syn_9/carry (ec0rm0023al1n02x5)               11.1
27.4      864.2 f
  intadd_8.n8 (net)                               1
0.0      864.2 f
  intadd_8.syn_8/c (ec0rm0023al1n02x5)                   11.1
0.0 *    864.2 f
  intadd_8.syn_8/carry (ec0rm0023al1n02x5)               11.3
27.4      891.5 f
  intadd_8.n7 (net)                               1
0.0      891.5 f
  intadd_8.syn_7/c (ec0rm0023al1n02x5)                   11.3
0.0 *    891.6 f
  intadd_8.syn_7/carry (ec0rm0023al1n02x5)               11.4
27.5      919.1 f
  intadd_8.n6 (net)                               1
0.0      919.1 f
  intadd_8.syn_6/c (ec0rm0023al1n02x5)                   11.4
0.0 *    919.2 f
  intadd_8.syn_6/carry (ec0rm0023al1n02x5)               11.7
27.9      947.1 f
  intadd_8.n5 (net)                               1
0.0      947.1 f
  intadd_8.syn_5/c (ec0rm0023al1n02x5)                   11.7
0.1 *    947.1 f
  intadd_8.syn_5/carry (ec0rm0023al1n02x5)               11.4
27.7      974.8 f
  intadd_8.n4 (net)                               1
0.0      974.8 f
```

```
  intadd_8.syn_4/c (ec0rm0023al1n02x5)                    11.4
0.0 *    974.8 f
  intadd_8.syn_4/carry (ec0rm0023al1n02x5)                11.4
27.5     1002.3 f
  intadd_8.n3 (net)                              1
0.0      1002.3 f
  intadd_8.syn_3/c (ec0rm0023al1n02x5)                    11.4
0.0 *    1002.4 f
  intadd_8.syn_3/carry (ec0rm0023al1n02x5)                11.1
27.3     1029.6 f
  intadd_8.n2 (net)                              1
0.0      1029.6 f
  intadd_8.syn_2/c (ec0rm0023al1n02x5)                    11.1
0.0 *    1029.7 f
  intadd_8.syn_2/carry (ec0rm0023al1n02x5)                 8.7
24.2     1053.9 f
  intadd_8.n1 (net)                              1
0.0      1053.9 f
  syn_208971/a (ec0bfn000al1n04x5)                         8.7
0.0 *    1053.9 f
  syn_208971/o (ec0bfn000al1n04x5)                         4.9
12.7     1066.6 f
  n313243 (net)                                  1
0.0      1066.6 f
  syn_208972/a (ec0xnr002al1n02x5)                         4.9
0.0 *    1066.6 f
  syn_208972/out0 (ec0xnr002al1n02x5)                     15.0
9.6      1076.2 r
  n313244 (net)                                  1
0.0      1076.2 r
  syn_208973/a (ec0xnr002al1n02x5)                        15.0
0.0 *    1076.2 r
  syn_208973/out0 (ec0xnr002al1n02x5)                     13.9
14.6     1090.8 r
  n313245 (net)                                  1
0.0      1090.8 r
  syn_208974/b (ec0aoi022al2n04x5)                        13.9
0.0 *    1090.9 r
  syn_208974/o1 (ec0aoi022al2n04x5)                       18.6
15.7     1106.6 f
  n313246 (net)                                  1
0.0      1106.6 f
  syn_208975/b (ec0nand02al1n15x5)                        18.6
0.1 *    1106.6 f
  syn_208975/o1 (ec0nand02al1n15x5)                       18.7
20.3     1126.9 r
  n333624 (net)                                  9
0.0      1126.9 r
  syn_225965/b (ec0nor004al2n02x7)                        19.4
5.6 *    1132.5 r
  syn_225965/o1 (ec0nor004al2n02x7)                       20.2
18.8     1151.3 f
  n300412 (net)                                  1
0.0      1151.3 f
  U210350/b (ec0aoit12al1n09x5)                           20.2
0.1 *    1151.4 f
```

```
  U210350/o1 (ec0aoit12al1n09x5)                          25.0
22.9     1174.3 r
  n250487 (net)                                 3
0.0      1174.3 r
  syn_185283/a (ec0nand22al2n03x5)                        25.0
3.2 *    1177.5 r
  syn_185283/o1 (ec0nand22al2n03x5)                       15.9
17.0     1194.5 f
  n308762 (net)                                 1
0.0      1194.5 f
  syn_185284/b (ec0nand02al1n08x5)                        15.9
0.2 *    1194.7 f
  syn_185284/o1 (ec0nand02al1n08x5)                       17.8
17.7     1212.4 r
  n300786 (net)                                 4
0.0      1212.4 r
  syn_185285/b (ec0nand02al1n15x5)                        17.8
0.2 *    1212.6 r
  syn_185285/o1 (ec0nand02al1n15x5)                       25.1
24.5     1237.1 f
  n319469 (net)                                 7
0.0      1237.1 f
  syn_225962/b (ec0aoai13al2n03x5)                        25.3
4.3 *    1241.4 f
  syn_225962/o1 (ec0aoai13al2n03x5)                       18.9
21.1     1262.6 r
  n319470 (net)                                 1
0.0      1262.6 r
  syn_225963/a (ec0oaoi13al2n04x5)                        18.9
0.1 *    1262.6 r
  syn_225963/o1 (ec0oaoi13al2n04x5)                       27.6
17.7     1280.3 f
  n300135 (net)                                 1
0.0      1280.3 f
  U178825/clk1 (ec0cnanc2al2n20x5)                        27.6
0.1 *    1280.4 f
  U178825/clkout (ec0cnanc2al2n20x5)                       0.0
7.0      1287.4 r
  n144251 (net)                                 4
0.0      1287.4 r
  syn_185280/a (ec0nor002al2n06x5)                         0.0
0.0      1287.4 r
  syn_185280/o1 (ec0nor002al2n06x5)                       22.7
16.7     1304.1 f
  n300665 (net)                                 6
0.0      1304.1 f
  syn_185281/a (ec0nand02al1n05x5)                        22.7
0.1 *    1304.2 f
  syn_185281/o1 (ec0nand02al1n05x5)                       11.6
13.8     1318.0 r
  n319463 (net)                                 2
0.0      1318.0 r
  syn_185282/a (ec0inv000al2n08x5)                        11.6
0.0 *    1318.0 r
  syn_185282/o1 (ec0inv000al2n08x5)                       23.8
23.5     1341.5 f
```

```
  n143012 (net)                                  12
0.0     1341.5 f
  syn_185292/c (ec0aoi022al2n04x5)                          23.8
0.4 *   1342.0 f
  syn_185292/o1 (ec0aoi022al2n04x5)                         20.5
22.4     1364.4 r
  n308764 (net)                                   1
0.0     1364.4 r
  syn_185293/b (ec0oai112al2n16x5)                          20.5
0.1 *   1364.4 r
  syn_185293/o1 (ec0oai112al2n16x5)                         26.6
25.5     1390.0 f

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.aux_probe0
_6_0 (net)     1      0.0   1390.0 f
  syn_195113/a (ec0bfn000al1n08x5)                          27.2
6.0 *   1396.0 f
  syn_195113/o (ec0bfn000al1n08x5)                          29.3
39.9     1435.8 f
  n340292 (net)                                  11
0.0     1435.8 f
  U167267/b (ec0nor002al1n01x5)                             29.3
0.5 *   1436.3 f
  U167267/o1 (ec0nor002al1n01x5)                            21.9
24.3     1460.7 r
  n148105 (net)                                   1
0.0     1460.7 r
  syn_211132/b (ec0nanb02al1n05x5)                          21.9
0.0 *   1460.7 r
  syn_211132/out0 (ec0nanb02al1n05x5)                       12.5
14.4     1475.0 f
  n148106 (net)                                   2
0.0     1475.0 f
  syn_211133/b (ec0nor002al2n06x5)                          12.5
0.0 *   1475.0 f
  syn_211133/o1 (ec0nor002al2n06x5)                         23.2
21.7     1496.7 r
  n315706 (net)                                   3
0.0     1496.7 r
  syn_217505/b (ec0nand02al1n15x5)                          23.2
0.4 *   1497.1 r
  syn_217505/o1 (ec0nand02al1n15x5)                         23.5
23.3     1520.4 f
  n147798 (net)                                   3
0.0     1520.4 f
  U167278/b (ec0qbfno2bl2n18x5)                             28.7
14.2 *   1534.6 f
  U167278/o1 (ec0qbfno2bl2n18x5)                            27.1
33.6     1568.2 r
  n192581 (net)                                   8
0.0     1568.2 r
  syn_243547/a (ec0bfn000al1n06x5)                          27.1
0.5 *   1568.7 r
  syn_243547/o (ec0bfn000al1n06x5)                          24.6
32.7     1601.4 r
```

```
  n358712 (net)                                  15
0.0     1601.4 r
  U167484/a (ec0qsfca4cl2n06x5)                          24.6
0.9 *   1602.3 r
  U167484/o1 (ec0qsfca4cl2n06x5)                         25.1
25.6     1627.9 f
  n147862 (net)                                   1
0.0     1627.9 f
  U167485/a (ec0oai012al1n01x3)                          25.1
0.5 *   1628.4 f
  U167485/o1 (ec0oai012al1n01x3)                         22.9
17.5     1645.9 r
  n147863 (net)                                   1
0.0     1645.9 r
  U167486/a (ec0aoi012al1n01x5)                          22.9
0.0 *   1646.0 r
  U167486/o1 (ec0aoi012al1n01x5)                         18.8
17.2     1663.2 f
  n148053 (net)                                   1
0.0     1663.2 f
  syn_258036/a (ec0bfn000al1n04x5)                       18.8
0.0 *   1663.2 f
  syn_258036/o (ec0bfn000al1n04x5)                        6.5
16.8     1680.0 f
  n373085 (net)                                   1
0.0     1680.0 f
  syn_228945/a (ec0bfn000al1n04x5)                        6.5
0.2 *   1680.2 f
  syn_228945/o (ec0bfn000al1n04x5)                       15.4
20.6     1700.8 f
  n349068 (net)                                   1
0.0     1700.8 f
  syn_248308/a (ec0bfn000al1n08x5)                       15.4
1.9 *   1702.7 f
  syn_248308/o (ec0bfn000al1n08x5)                       13.9
24.9     1727.7 f
  n363566 (net)                                   6
0.0     1727.7 f
  syn_222430/b (ec0nor002al1n03x7)                       13.9
0.2 *   1727.9 f
  syn_222430/o1 (ec0nor002al1n03x7)                      21.8
20.7     1748.6 r
  n317915 (net)                                   2
0.0     1748.6 r
  syn_222608/a (ec0nand02al1n08x5)                       21.8
0.1 *   1748.7 r
  syn_222608/o1 (ec0nand02al1n08x5)                      28.6
28.0     1776.7 f
  n251131 (net)                                  14
0.0     1776.7 f
  U296343/a (ec0nanb02al1n01x3)                          28.6
0.6 *   1777.3 f
  U296343/out0 (ec0nanb02al1n01x3)                       17.7
25.5     1802.8 f
  n251132 (net)                                   1
0.0     1802.8 f
```

```
  syn_202393/a (ec0bfn000al1n04x5)                          17.7
0.0 *   1802.8 f
  syn_202393/o (ec0bfn000al1n04x5)                           4.2
14.2     1817.0 f
  n342349 (net)                                    1
0.0     1817.0 f
  syn_224911/a (ec0bfn000al1n08x5)                           4.2
0.0 *   1817.0 f
  syn_224911/o (ec0bfn000al1n08x5)                           5.1
13.0     1830.0 f
  n348052 (net)                                    3
0.0     1830.0 f
  syn_248088/a (ec0bfn000al1n04x5)                           5.1
0.0 *   1830.0 f
  syn_248088/o (ec0bfn000al1n04x5)                          18.7
22.6     1852.6 f
  n363335 (net)                                   15
0.0     1852.6 f
  U296367/b (ec0nor002al1n01x5)                             18.7
0.3 *   1852.8 f
  U296367/o1 (ec0nor002al1n01x5)                            18.0
20.5     1873.4 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.addr_vec_and
_wr_en_244_0 (net)     1      0.0   1873.4 r
  syn_219558/a (ec0bfn000al1n04x5)                          18.0
0.0 *   1873.4 r
  syn_219558/o (ec0bfn000al1n04x5)                           7.1
16.7     1890.1 r
  n347218 (net)                                    1
0.0     1890.1 r

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_244.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/en (ec0cnan02al1n06x5)      7.1      0.0 *
1890.1 r
  data arrival time
1890.1

  clock ascan_preclk_mgmt_clk' (rise edge)
2163.0     2163.0
  clock network delay (ideal)
0.0     2163.0

physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core.u_emp_cach
e.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike.ctech_lib_cl
k_and_en_244.ctech_lib_clk_and_en_to_nand_en_1.ctech_lib_clk_n
and_en_dcszo/clk (ec0cnan02al1n06x5)      0.0   2163.0 r
  library nochange setup time
0.3     2163.3
  data required time
2163.3
  -----------------------------------------------------------
-----------------------
```

```
  data required time
2163.3
  data arrival time
-1890.1
  ---------------------------------------------------------------
-------------------------
  slack (MET)
273.2
```

4. Area Reports:

```
**************************************************
Report : area -physical
Design : parphyss_ctrl
**************************************************

Boundary            : {0.000 0.000} {275.886 0.000} {275.886
276.216} {0.000 276.216} {0.000 0.000}
Core Area           : 76204.127376
Placement Area      : 0.000 0.000 275.886 276.216


****************************************
Report : area
****************************************

Library(s) Used:

    ec0_ln_p1274d3_tttt_v085_t100_max_ccst (File:
/p/hdk/cad/stdcells/ec0/17ww27.5_ec0_g.3.p2.all/lib/ccst/p12
74d3/ln/ec0_ln_p1274d3_tttt_v085_t100_max_ccst.ldb)
    ec0hs_ln_p1274d3_tttt_v085_t100_max_ccst (File:
/p/hdk/cad/stdcells/ec0hs/17ww27.5_ec0hs_g.3.p2.all/lib/ccst
/p1274d3/ln/ec0hs_ln_p1274d3_tttt_v085_t100_max_ccst.ldb)
    ec0sdgalpha_ln_p1274d3_tttt_v085_t100_max_ccst (File:
/p/hdk/cad/stdcells/ec0sdgalpha/17ww27.5_ec0sdgalpha_g.3.p2.
sdg/lib/ccst/p1274d3/ln/ec0sdgalpha_ln_p1274d3_tttt_v085_t10
0_max_ccst.ldb)
    ec0cnlalpha_ln_p1274d3_tttt_v065_t100_max_ccst (File:
/p/hdk/cad/stdcells/ec0cnlalpha/17ww27.5_ec0cnlalpha_g.3.p2.
cnl/lib/ccst/p1274d3/ln/ec0cnlalpha_ln_p1274d3_tttt_v065_t10
0_max_ccst.ldb)
    ec0ser_ln_p1274d3_tttt_v065_t100_max_ccst (File:
/p/hdk/cad/stdcells/ec0ser/17ww27.5_ec0ser_g.3.p2.all/lib/cc
st/p1274d3/ln/ec0ser_ln_p1274d3_tttt_v065_t100_max_ccst.ldb)


Combinational area:              21752.281764
Buf/Inv area:                     4999.281138
Noncombinational area:           26280.430359
Macro/Black Box area:              350.441005
Net Interconnect area:      undefined  (No wire load
specified)

Total cell area:                 48383.153128
Total area:                 undefined

Core Area:                     76204
Aspect Ratio:                1.0012
Utilization Ratio:           0.6369
```

The above information was reported from the logical library.
The following are from the physical library:

  Total moveable cell area: 48383.2
  Total fixed cell area: 184.0
  Total physical cell area: 48567.2
 Core area: 0.000, 0.000, 275.886, 276.216

Hierarchical area distribution
------------------------------

| Hierarchical cell | Global cell area: Absolute Total | Global cell area: Percent Total | Local cell area: Combi-national | Local cell area: Noncombi-national | Local cell area: Black-boxes | Design |
|---|---|---|---|---|---|---|
| parphyss_ctrl | 48383.1531 | 100.0 | 21752.2818 | 26205.0809 | 350.4410 | parphyss_ctrl |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_0_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_189 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_1_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_188 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_2_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_187 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_3_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_186 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_dc_ctl.mem_rd_data_q_reg_80 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_81 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_0_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_7 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_1_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_9 |
| clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg_3_0 | 0.3966 | 0.0 | 0.0000 | 0.3966 | 0.0000 | SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_6 |

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.mgck_ring0
_physs_lsm_rpl_cdc.u_r_mgmt_lsm_dve_pipe.o_data_reg_31
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_47
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_dc_ctl.mem_rd_data_q_re
g_0 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_157
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg
_0_7 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_185
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg
_1_7 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_184
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg
_2_7 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_183
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.int_cdc_fifo_ve.u_fifo_reg.mem_data_q_reg
_3_7 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_182
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_dc_ctl.mem_rd_data_q_r
eg_0 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_8
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_re
g_0_1 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_87
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_re
g_1_71 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_42
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_re
g_2_67 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_12
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.mgmt_cdc_fifo_ve.u_fifo_reg.mem_data_q_re
g_3_66 0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_17
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.u_r_int_lsm_dve_pipe.o_data_reg_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_181
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.ring0_mgck
_physs_lsm_rpl_cdc.u_r_mgmt_lsm_dve_pipe.o_data_reg_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_5
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.AccessPort.jtagPrcCapture_reg.tmp_reg_0 0.3966
0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_92

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.Datapath.IterativeDivider.quotient_reg.tmp_reg
_0     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_41
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.ExternInt.instresponsebuffer.respbuf_vaddr_reg
.tmp_reg_4     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_29
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.LoadStore.LSElement.lb0VPage_reg.tmp_reg_2
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_14
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.LoadStore.LSElement.lb1VPage_reg.tmp_reg_2
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_13
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.InstFetch.Instr_R_reg.tmp_reg_79
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_4
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.InstFetch.instBuffer_R_reg.tmp_reg
_0     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_10
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.InstFetch.last3_R_reg.tmp_reg_10
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_156
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.InstFetch.savedMHTInstLookupBusErr
or_reg.tmp_reg_1     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_101
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.LENDMinus1_E_reg.tmp_reg_31
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_27
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.count_X_reg.tmp_reg_31
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_26
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.loopEndPC_R_reg.tmp_reg_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_30
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.missVAddr_reg.tmp_reg_2
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_25
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.myPC_W_reg.tmp_reg_1
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_31
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.Xttop.Xtensa.PCandIFetch.PCUnit.pc_I_reg.tmp_reg_29
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_28

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.cram_boundary_en_reg     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_91
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.dram0_boundary_en_reg     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_90
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.protected_area_end_arr_reg_0_2     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_155
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.protected_area_start_arr_reg_1_2     0.3966
0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_100
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.protected_area_start_arr_reg_2_2     0.3966
0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_180
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_arb.protected_area_waiver_reg_2     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_99
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_cam.u_ecip_gen_camlike_v2.gen_camlike
.match_vec_reg_119     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_0
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_112.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_154
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_124.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_153
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_128.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_152
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_130.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_151
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_131.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_179
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_133.prev_ptr_1
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_178
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_139.prev_ptr_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_150

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_140.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_149
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_141.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_148
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_142.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_147
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_143.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_177
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_144.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_146
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_145.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_145
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_146.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_144
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_148.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_143
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_150.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_176
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_152.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_142
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_155.prev_ptr_1
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_175
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_157.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_141
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_158.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_174
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_160.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_140

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_161.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_173
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_164.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_139
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_166.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_138
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_167.prev_ptr_1
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_137
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_168.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_136
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_170.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_172
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_172.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_135
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_173.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_134
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_174.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_133
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_181.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_132
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_182.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_131
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_186.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_130
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_188.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_129
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_190.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_128

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_196.next_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_127
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_196.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_126
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_198.next_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_125
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_198.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_124
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_217.next_ptr_1
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_171
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_217.prev_ptr_1
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_170
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_230.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_123
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_240.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_122
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_241.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_121
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_242.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_120
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_243.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_119
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_249.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_118
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_252.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_117
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_253.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_169

clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_260.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_116
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_261.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_115
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_262.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_168
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_264.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_114
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_265.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_113
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_266.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_112
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_276.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_111
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_277.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_110
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_278.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_109
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_282.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_167
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_288.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_108
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_80.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_107
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_85.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_106
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_cache.emp_cache_lru.lru_array_reg_88.prev_ptr_0
0.3966 0.0 0.0000 0.3966 0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_105

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clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.mem_addr_reg_30     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_98
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.mem_data_wr_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_40
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.p_dcb_pfclda_reg_1_7     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_166
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.p_dcb_pfclda_reg_3_7     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_165
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_0_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_104
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_1_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_79
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_2_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_96
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_3_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_95
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_4_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_86
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_5_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_94
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_6_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_85
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_ext_reg_reg_7_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_89
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_0_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_39
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_1_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_38
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_2_0     0.3966     0.0
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0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_37
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_3_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_36
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_4_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_35
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_5_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_34
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_6_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_33
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_hcsr.sha256_rom_reg_reg_7_0     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_32
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_0_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_78
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_10_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_69
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_11_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_68
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_12_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_77
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_13_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_93
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_14_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_53
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_15_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_67
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_2_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_66
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_3_28     0.3966     0.0
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0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_65
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_4_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_64
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_5_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_63
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_6_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_62
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_7_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_76
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_8_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_75
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier0_reg_9_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_74
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_0_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_46
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_10_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_61
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_11_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_73
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_12_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_72
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_13_30     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_52
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_14_28     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_71
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_15_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_51
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_1_31     0.3966     0.0
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0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_45
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_2_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_44
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_3_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_60
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_4_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_59
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_5_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_80
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_6_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_58
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_7_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_57
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_8_31     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_56
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.agt_l2_ier1_reg_9_30     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_55
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_10_reg_26     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_164
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_12_reg_23     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_163
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_14_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_83
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_18_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_103
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_19_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_97
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_27_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_162
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_28_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_82
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clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_4_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_84
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_int.i_en_6_reg_0     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_54
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_dram_params.u_emp_dram0_wrapper.pss_emp_d
ram.u_dram0.u_master_1rw_shell.RD_ADDRESS_SAMPLING.u_gen_fif
o.reg_mem_reg_0_0     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_161
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_dram_params.u_emp_dram0_wrapper.pss_emp_d
ram.u_dram0.u_master_1rw_shell.RD_ADDRESS_SAMPLING.u_gen_fif
o.reg_mem_reg_1_0     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_160
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_dram_params.u_emp_dram0_wrapper.pss_emp_d
ram.u_dram0.u_master_1rw_shell.RD_ADDRESS_SAMPLING.u_gen_fif
o.reg_mem_reg_2_0     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_159
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_dram_params.u_emp_dram0_wrapper.pss_emp_d
ram.u_dram0.u_master_1rw_shell.RD_ADDRESS_SAMPLING.u_gen_fif
o.reg_mem_reg_3_0     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_158
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_dram_params.u_emp_dram0_wrapper.pss_emp_d
ram.u_dram0.u_master_1rw_shell.ecc_err_adr_reg_0     0.3966
0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_50
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_mem.pss_emp_iram_params.u_emp_cram_wrapper.pss_emp_cr
am.u_cram.u_master_1rw_shell.ecc_err_adr_reg_0     0.3966
0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_49
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_timer.gpt_init_val_sav_reg_17     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_70
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_emp_timer.phase1_res_reg_2     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_88
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_in_to_ll_lsm_dve_pi
pe.o_data_reg_92     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_48
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_in_to_ll_lsm_dve_pi
pe.seq.split.data_hold_q_reg_96     0.3966     0.0
0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_3
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm

t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_0_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_24
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_1_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_23
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_2_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_22
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_3_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_21
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_4_0     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_11
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_5_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_20
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_6_96     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_16
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_emp_core
.u_lsm_to_mng_regs_shim.lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgm
t_junc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data
_reg_7_96     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_15
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_cpi_regs.PHYSS_CPI_PHY_OWNER_RESERVED_r
eg_15     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_19
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_cpi_regs.PHYSS_CPI_PHY_PHY_CMD_reg_0
0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_18
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgmt_j
unc32_bypass.u_lsm_mgmt_junc_bypass.u_in_to_ll_lsm_dve_pipe.
o_data_reg_0     0.3966     0.0     0.0000     0.3966
0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_1
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgmt_j
unc32_bypass.u_lsm_mgmt_junc_bypass.u_in_to_ll_lsm_dve_pipe.
seq.split.data_hold_q_reg_91     0.3966     0.0     0.0000
0.3966   0.0000 SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_102

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clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgmt_j
unc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.data_re
g_0_0     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_2
clk_gate_physs_ctrl_apr.physs_ctrl_apr_func_logic.u_physs_ct
rl_regs_wrap.u_physs_lsm_rpl_junc32.u_mgmt_junc.u_lsm_mgmt_j
unc32_bypass.u_lsm_mgmt_junc_bypass.u_lfifo_dff_fifo.o_out_r
eg_63     0.3966     0.0     0.0000     0.3966   0.0000
SNPS_CLOCK_GATE_HIGH_parphyss_ctrl_43
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Total
21752.2818  26280.4304  350.4410
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