Address Translation
&
IRAM Cache

Progress Report #5

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Achievements

- Finished adjustments to MissHandler and LRU for supporting IRAM partial mapping via threshold address.
- Finished coding Address protection.
- Adjusted the TestBenches to cover the new features' functionality correctness.
- Reproduced fresh Area and Timing reports.
- Gathered a list of rules for future formal verification.

Challenges

- Apply formal verification on our blocks and clean any issues found.

Correspondence with advisor

- In our weekly 1:1 meetings with our advisor we discussed:
    - The generic SVA (System Verilog Assertion) Library – how to enable it, navigate its documentation and how to use it.
    - Brain-stormed for good formal verification rules.