Address Translation
&
IRAM Cache

Progress Report #1

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Achievements

- Completed Verification For Logic-Designers course.
- Completed Advanced Design Concepts course.
- Finished ramp task: Asynchronies FIFO (pushed to GIT repo):
    - Improved our design skills.
    - Learned about CDC (clock domain crossing).
    - Formal verification hands on.
- Investigation:
    - Cache methodologies.
    - Address translation methodologies.
    - Arbitration methodologies.

Challenges

- Learning the adjacent blocks interfaces and timing constrains. The blocks around the IRAM cache are:
    - SPI engine – the block that connects the CPU controller to the NVM (Non Violated Memory)
    - Memory arbiter – arbitrate between all agents to all the memories on the chip. The CPU controller used to be one of those agents, now the cache block should be.

  The blocks around Address Translation are:
    - Interconnect – have master-slave interfaces. Capable of routing desired requests from master interface to the correct slave interface.
    - Host Interface – request of translation will come from this block.
- Understanding the architectural specifications of our own blocks and the implications:
    - Timing constraints – number of clock cycles allowed.
    - Size – meet estimation (counted by Flip-Flops and Latches)
    - Deduce basic knowledge of our future design.
- We need to start thinking of design that will concur the problem along with the architectural constraints.
- Contacting Intel Legal department in order to get permission of viewing part of the MAS (Micro Architectural Specifications) document.

Correspondence with advisor

- We had a lesson of CDC in order for us to solve the Async-FIFO task.
- We had a meeting regarding the control and data path of our block's peripheral.
- With our advisor guidance we decided on several important issues:
    - Using fully associative cache with LRU (Least Recently Used) eviction policy.
    - Using Round-Robin algorithm as arbitration methodology.
    - Dividing the addresses of the requests to different types called scopes and investigate translation function according to this partition.
- In order to get to know the adjacent blocks we were advised to follow the Code of those blocks and to set short meetings with the lead-designer of those for understanding the data and control flow.