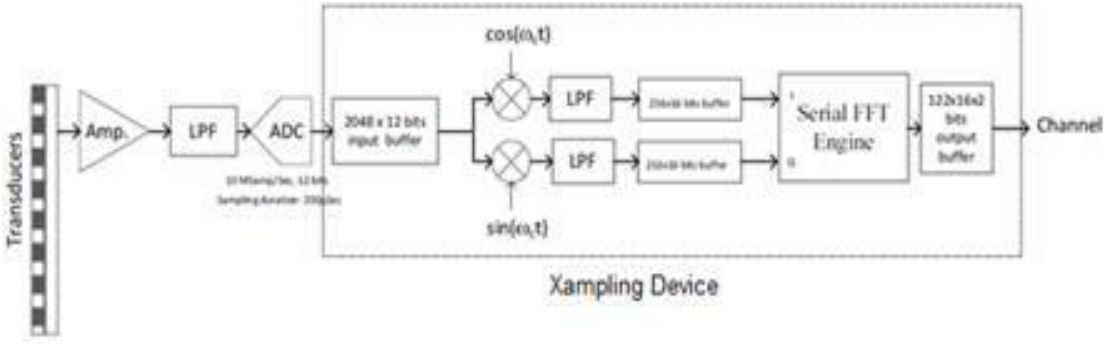
Project Definition

The mixed signal solution of the US cloud processing project includes an ASIC which is comprised of the following signal path:

Buffer -> Mixer -> Digital LPF -> buffer -> FFT engine -> buffer



The requirements of this project is to implement the second half of the signal path i.e: .

buffer -> FFT engine -> buffer

The FFT engine will receive 2 sets of inputs, each with 256 samples and each sample is 16 bits wide.

One set of samples represents the real part of the sample and the other the imaginary part.

The goal is to implement an efficient VLSI architecture which meets timing requirements and requires a minimal amount of area.

Timing requirements will be derived from the specs.

General Requirements

- Meet with us once a week
- Expected work load : 12-14 hrs/week
- Work consistently throughout the semester
- Mid semester report
- Final presentation
- Final report

Project stages include:

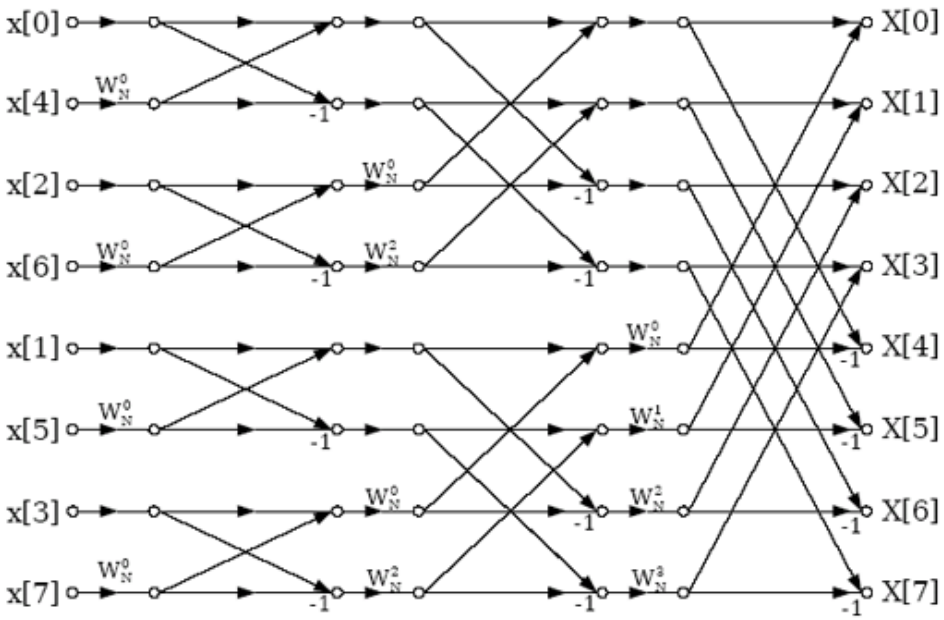
- Learn the specs
- Implement in matlab
- Design architecture
- Implement in Verilog
- Functional simulation
- Synthesis
- Layout

Every 256 clock cycles, a set of inputs will be ready for processing by the FFT unit. In other words, the FFT unit must complete the computation within 256 cycles.

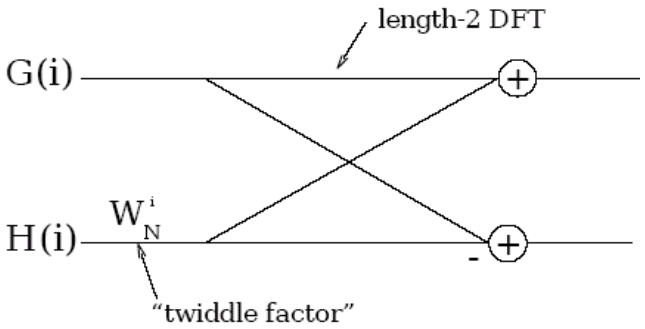
FFT formula :

$$X(k)=\sum_{n=0}^{N-1} x(n)\, e^{\frac{-i2\pi nk}{N}}, k=0 \ldots N-1$$

The algorithm for the computation of the FFT for a series of 8 inputs is shown below:



Basic unit :



Note that the inputs here are complex. For a 256 sample input, the above diagram will have 8 stages.

Issues for the students to consider :

- How many stages of the FFT algorithm will be performed in one clock cycle ?
- How can we maximize the usage of 256 clock cycles to minimize the total area ?
- Once we have determined the number of computational blocks (comprised of complex adders and multipliers) we have in our design, how do we route the outputs of these units back to the inputs so that the computation is performed correctly ?
- How do we ensure that the accuracy of the results is sufficient ?