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About

I am an Assistant Professor in the Department of Electronics and Communications Engineering (ECE) at the Indian Institute of Information Technology Guwahati (IIIT-G) working from July, 2019. Prior to that, I received the Ph.D. degree in VLSI Design from the Indian Institute of Technology Guwahati (IITG). My research interests are on VLSI Design for Digital/Analog/Mixed-Signal Systems. For more information, please visit my homepage ([Link](#))

Research Interests

Low-power Transceiver (Baseband/WF) Design, VLSI for Signal Processing and Communications, Analog and Mixed-Signal Circuit Design

Teaching

At IITG, I have taught the following courses:

- EC 103: Basic Electronic Circuits
- EC 241: Signals and Systems
- EC 361: VLSI Design
- EC 110: Digital Design Lab
- EC 111: Basic Electronics Lab
- EC 244: Digital Signal Processing Lab
- EC 302: Analog Integrated Circuit Lab
- EC 362: VLSI Design Lab
- EC 661: VLSI Circuits and Systems
- EC 672: Semiconductor Device Modeling
- EC 662: VLSI CAD Lab
- EC668: VLSI Solid State Circuits Lab

Research Grant

- VITTRIA, SERB (JANVR/2022/0317): **Towards VLSI and Embedded System Design using FPGA Boards**, 2022 (1.50,000)

Publication

Conference

- S. Singh, S. Patel, S. Kumar, M. Das and B. Jodda, "FPGA-Optimized Eight-Term Karatsuba Multiplications for Large Integer Multiplications", 2024 IEEE International Conference on Recent Innovation in Smart and Sustainable Technology (ICRISST), (2024), pages. 1-6, Presidency University, Igatpura, Raparukurta, Nashik, Bangalore, Karnataka, India
- S. Kumar, S. Patel, S. Singh, M. Das and B. Jodda, "Design and Evaluation of FPGA-Optimized Symmetrical Three-Term Karatsuba Multipliers", 2024 IEEE International Conference on Recent Innovation in Smart and Sustainable Technology (ICRISST), (2024), pages. 1-6, Presidency University, Igatpura, Raparukurta, Nashik, Bangalore, Karnataka, India
- S. Kumar, S. Patel, S. Singh, M. Das and B. Jodda, "FPGA-Optimized Two-Term Karatsuba Multiplications for Large Integer Multiplications", 2024 12th IEEE International Conference on Signal Processing and Integrated Networks (SPIN), (2024), pages. 1-6, ASET, Army University, Sec-125, Rohtak, Delhi-NCR, India
- Jibesh Lahari, Diana Linnet, Babita Jodda, Mandar B. Pande, Amit Patel, Kishit Dave and B. R. Niklesh, "Efficient Earth Observation Satellites Mission Planning with Quantum Algorithms", 2024 Second IEEE International Conference in Trends in Quantum Computing & Emerging Business Technologies (TQCBE), (2024), pages. 1-6, Christ (Deemed to be University), Pune Lavasa Campus, Pune, India
- Jibesh Lahari, Diana Linnet, Babita Jodda, Mandar B. Pande, Amit Patel, Kishit Dave and B. R. Niklesh, "Efficient Earth Observation Satellites Mission Planning with Quantum Algorithms", 2024 Second IEEE International Conference in Trends in Quantum Computing & Emerging Business Technologies (TQCBE), (2024), pages. 1-6, Christ (Deemed to be University), Pune Lavasa Campus, Pune, India
- M. Thakare and B. Jodda, "Hardware Implementation for Determining Perfect and Non-Perfect Square Roots using Dvandwa Yuga on FPGA", in 2022 IEEE International Conference on Electrical, Computer and Energy Technologies (ICECET), (2022), Prague, Czech Republic
- P. Das and B. Jodda, "Design Automation of Two-Stage Operational Amplifier Using Multi-Objective Genetic Algorithm and SPICE Framework", in 2022 IEEE 5th International Conference on Intellectual Computation Technologies (ICCT), Luthian, Nepal, 20-22 July, (2022).
- V. Mishra, D. Pandey, S. Singh, S. Satapathy, K. Goswami, B. Jodda and D.S. Banerjee, "MIT-MAC: An Approximate Rounding and Truncation-Based MAC Unit for Fast Embedded Applications", in 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, Texas, USA, 18-May-June 1, (2022).
- S. Singh, V. Mishra, S. Satapathy, D. Pandey, K. Goswami, D.S. Banerjee and B. Jodda, "RFCSA: An Efficient Carry Speculative Approximate Adder with Rectification", in 2022 IEEE 23rd International Symposium on Quality Electronic Design (ISQED), San Jose, California, USA, 6-8 April, (2022).
- D. Pandey, V. Mishra, S. Singh, S. Satapathy, B. Jodda and D.S. Banerjee, "WRMA: An 8-bit High-Performance Approximate Multiplier Design for Error Resilient Applications", in 2022 IEEE 23rd International Symposium on Quality Electronic Design (ISQED), San Jose, California, USA, 6-8 April, (2022).
- P. Yash, M. Thakare and B. Jodda, "Optimized Hardware Implementation of Vedic Binary Multiplier using Nikhilam Sutra on FPGA", in 2022 IEEE 13th Latin American Symposium on Circuits and Systems (LASCAS), Puerto Varas, Chile, 1-4 March, (2022).
- S. Jakhodia and B. Jodda, "Numerical Methods for Solving High-Order Mathematical Problems Using Quantum Linear System Algorithm on IBM QXQ Platform", in 2022 IEEE 3rd International Conference on Innovative Trends in Information Technology (ICTIT), (2022), pages. 1-7, Virtual Mode
- M.Das and B. Jodda, "Hardware Design of Optimized Large Integer Schoolbook Polynomial Multiplication on FPGA", 2022 19th IEEE International Soc. Conference (ISCC), (2022), pages. 1-2, Laksh Sandipine Resort, Gangang-ii, Gangang-dh, India
- M. Karthik, J. Lahari and B. Jodda, "Quantum Text Segmentation Protocol for Secure Text Transfer by using Quantum Segmentation and Huffman Coding", 2022 IEEE International Conference in Trends in Quantum Computing & Emerging Business Technologies, (2022), pages. 1-6, Christ (Deemed to be University), Pune Lavasa Campus, 13-15 October, 2022
- A. Chandra, J. Lahari and B. Jodda, "Towards an Optimal Hybrid Algorithm for EV Charging Stations Placement using Quantum Annealing and Genetic Algorithms", 2022 IEEE International Conference in Trends in Quantum Computing & Emerging Business Technologies, (2022), pages. 1-6, Christ (Deemed to be University), Pune Lavasa Campus, 13-15 October, 2022
- M. Karthik, J. Lahari and B. Jodda, "Quantum Image Segmentation Protocol (QITP) and Quantum Audio Segmentation Protocol (QATP) by using Quantum Segmentation and Huffman Coding", 2022 IEEE International Conference in Trends in Quantum Computing & Emerging Business Technologies, (2022), pages. 1-6, Christ (Deemed to be University), Pune Lavasa Campus, 13-15 October, 2022
- M.Das and B. Jodda, "FPGA Implementation of Hybrid Karatsuba Multiplications for MST Post-Quantum Cryptographic Hardware Primitives", 2022 19th IEEE International Soc. Conference (ISCC), (2022), pages. 1-2, Laksh Sandipine Resort, Gangang-ii, Gangang-dh, Korea
- B. Raju and B. Jodda, "Efficient Hardware Implementation of High-Speed Recursive Vedic Squaring Architecture on FPGA", in 2021 IEEE International Conference on Electrical, Computer and Energy Technologies (ICECET), Cape Town, South Africa, (2021), pages. 1-6.
- M. Thakare, P. Yash, D. Chhabra and B. Jodda, "Efficient Hardware Implementation of Cube Architecture using Vedic Sutra on FPGA", in 2021 IEEE 64th International Midwest Symposium on Circuits and Systems (MWSCAS), (2021), pages. 173-176.
- R. Thakare and B. Jodda, "Experimental Analysis of Attacks on RSA & Rabin Cryptosystems using Quantum Shor's Algorithm", in Proceedings of International Conference on Women Researchers in Electronics and Computing (WRREC), AIPR Proceedings, (2021), pages. 181-180, (Best Paper Award)
- J. Raju and B. Jodda, "Squaring Technique using Vedic Mathematics", in Proceedings of International Conference on Women Researchers in Electronics and Computing (WRREC), (2021), pages. 581-600, AIPR Proceedings
- B. Jodda, S. R. Ahmed and A. Mahanta, "Demodulation Techniques in IEEE 802.15.4 R-LWB DPMK WBAN Transceivers", in IEEE 5th International Conference on Smart Instrumentation, Measurement and Applications (ICSMA), Putrajaya Marriott Hotel, Malaysia, (2015), pages. 1-5.
- B. Jodda, S. R. Ahmed and A. Mahanta, "PPM Demodulation Scheme for IEEE 802.15.6 R-LWB WBAN Receivers", in IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES), (2015), pages. 1-5, NET Calicut, India
- B. Jodda, A. Mahanta and S. R. Ahmed, "A Six-Segment SRMC Pulse Generator for IEEE 802.15.6 WBAN Standard", in BODYNETS 2014- 6th International Conference on Body Area Networks, Sardinia House, London, Great Britain, (2014), pages. 46-49.

Book Chapters

- S. Jakhodia, D. Singh and B. Jodda, "Experimental Evaluation of QFT Adders on IBM QX Hardware", 2nd International Conference on Emerging Technologies for Computing, Communication and Smart Cities (ETCC), Lecture Notes in Electrical Engineering vol. 875, (2022), pages. 431-435, Springer, Singapore, Print ISBN: 978-981-19-0283-4, Online ISBN: 978-981-19-0284-0
- D. Singh, S. Jakhodia and B. Jodda, Srivatsa S., Balaji V.R., Parthasarathy R., "Experimental Evaluation of Adder Circuits on IBM QX Hardware", Intellectual Computation and Information Technologies (ICIT), Lecture Notes in Networks and Systems vol. 516, (2022), pages. 333-347, Springer, Singapore, Print ISBN: 978-981-16-4722-0, Online ISBN: 978-981-16-4723-7

Others

- P. Das and B. Jodda, "Design Optimization of Analog Circuit Using Multi-Objective Genetic Algorithm and SPICE Framework", in North-East Research Conclave, Indian Institute of Technology Guwahati, (2022), Technical Presentation on Extended Abstracts

Posters

- D. Pandey, V. Mishra, S. Singh, S. Satapathy and B. Jodda, "WRMA: An 8-bit High-Performance Approximate Multiplier Design for Error Resilient Applications", in 20th IEEE International Conference on High Performance Computing, Data, and Analytics (HPCDAS) Student Research Symposium (SRS), Bangalore, Karnataka, (2021), (Best Poster Award)

Journal

- B. Jodda, A. Mahanta and S. R. Ahmed, "Energy efficient DAC switching technique for single-ended SAR ADCs", AEU-



- International Journal of Electronics and Communications, Vol. 124, (2020), pages: 153334. Elsevier.
- R. Jaisidla, A. Mahanta and S.R. Ahmed, "IEEE 802.15.6 WBAN Standard Compliant IR-UWB Time-Hopping PPM Transmitter using SBRG signaling pulse", 4634 International Journal of Electronics and Communications, Vol. 117, (2020), pages: 153119. Elsevier
 - R. Jaisidla, A. Mahanta and S.R. Ahmed, "Mixed-Signal Demodulator for IEEE 802.15.6 IR-UWB WBAN Energy Detection based Receiver", 1871 Circuits, Devices & Systems, Vol. 12, No. 5, (2018), pages: 525-531.



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