Dr. Sounak Roy
Associate Professor
PhD (IIT Kharagpur)
Department of Electronics & Communication Engineering
sounak@iiitg.ac.in
Joined the Institute in July 2014

About

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B. Tech : From Kalyani University, 2001

MS (By Research) : From IIT Kharagpur, 2009

PhD : From IIT Kharagpur, 2014

2001-2002 : GET at Reliance Telecomm Ltd.

2002-2004 : Sr. NMS Engineer at Bharti Televentures Ltd.

2004 : Executive at Siemens Public Communications Network Ltd

Research Interests

Area of Expertise :

Analog and mixed signal ASIC design. Following are the details of the ASIC developed :

1. **ASIC1** : Design and implementation of building blocks of a pipeline ADC using 180 nm CMOS process technology provided by National Semiconductor Inc.

2. **ASIC2** : Design and implementation of a pipeline ADC using 180 nm CMOS process technology provided by National Semiconductors Inc. The prototype was tested at 80 MSPS with linearity of 5 bits

3. **ASIC3** : Design and implementation of a quad-parallel pipeline ADC using 180 nm CMOS process technology provided by National Semiconductors Inc. The prototype was tested at 75 MSPS, with linearity of 7 bits

4. **ASIC4** : Design and implementation of a pipeline ADC along with foreground calibration unit using 180 nm CMOS process technology provided by National Semiconductors Inc.

5. **ASIC 5** : Design, implementation of an Octal LVDS driver done using UMC 180 nm CMOS process

Journal Publications

[1] Sounak Roy, Hiranmoy Basak, and Swapna Banerjee, "Foreground Calibration Technique of a Pipelined ADC using Capacitor Ratio of Multiplying Digital-to-Analog Converter(MDAC)", in ***Microelectronics Journal, Elsevier***, Vol. 44, No. 12, pp 1336-1347,Dec. 2013

[2] Sounak Roy, and Swapna Banerjee, "A 9-Bit 50 MSPS Quadrature Parallel Pipeline ADC for Communication Receiver Application", ***Journal of the Institute of Engg. (India), Series B, Springer***, Vol 99, No. 3, pp 221-234, 2018

[3] S. Chatterjee and S. Roy, "A Square Wave based Digital Foreground Calibration Algorithm of a Pipeline ADC Using Approximate Harmonic Sampling," in ***IEEE Transactions on Circuits and Systems II (TCAS II): Express Briefs,*** Vol 68, No. 4, pp 1068-1072, April 2020, *DOI: 10.1109/TCSII.2020.3037812*.

[4] S. Chatterjee and S. Roy. "A Self Calibration Method Of a Pipeline ADC Based on Dynamic Capacitance Allotment". ***IEEE Transactions on Very Large Scale Integration (TVLSI) Systems***. vol.30, no.5, pp.666-670,Mar 2022,10.1109/TVLSI.2022.3151479

[5] J. Sharma, S. Chatterjee, R. Biswas and S. Roy, "A digitally controlled adaptive LDO for power management unit in sensor node".***Integration, Elsevier,*** Vol :87, pg 29-39, November, 2022

[6] S. Chatterjee and S. Roy, "A low power offset voltage calibration method for flash ADCs".***Integration, Elsevier,*** Vol :88, pg 58-69, January, 2023

Conference Publications

[1] Sounak Roy and Swapna Banerjee, "A 9 bit 400 MHz CMOS Double-Sampled Sample-and-Hold Amplifier," in *IEEE International conference on VLSI Design*, 2008.

[2] Sanjay Kr. Dey, Sounak Roy and Swapna Banerjee, "A 10 -bit 2.5GS/s Low-Power BiCMOS THA for High Performance ADC," in *International Conference on Computers and Devices for Communication (CODEC)*, 2006.

[3] Sounak Roy, Sanjay Kr. Dey and Swapna Banerjee, "A parallel pipeline ADC with a sub-ADC employing an improvized dynamic comparator," in *TENCON 2009 – 2009 IEEE Region 10 Conference, Singapore, 2009*.

[4] Sounak Roy, Bibhu DattaSahoo, and Swapna Banerjee, "Radix Based Digital Calibration Technique for Pipelined ADC Using Nyquist Sampling of Sinusoid" in *IEEE International Symposium on Circuits and Systems (ISCAS),Seoul, Korea*, 2012.

[5] Sounak Roy, Raju Naik, Archana Kumari, Durgam Mahesh, "A flash assisted dynamic range segmented successive approximation register (SAR) analog to digital converter", *IEEE International Conference on Circuits, Systems and Simulations (ICCSS), London, 2017*

[6] Sounak Roy, Shatadal Chatterjee, "Sinusoid Based Foreground Calibration Algorithm of a Pipeline ADC Using Time Averaged Radix Extraction",*IEEE Region 10 conference (TENCON), Jeju, Korea, 2018.*

[7] M. Mahendra Reddy, S. Roy; "Clock Pulse Based Foreground Calibration of a Sub-Radix-2 Successive Approximation Register ADC", *International Symposium on VLSI Design and Test (VDAT), 2019*

[8] Sounak Roy, Shatadal Chatterjee, "A Low Power mixed Signal Foreground Calibration Technique of a Pipeline ADC using a Variable Gain Amplifier", *IEEE Region 10 conference, (TENCON 2019), Kerala, India*

[9] J. Sarma, S. Chatterjee, R. Biswas and S. Roy, "An Adaptive Digitally Tuned Flash-based LDO with Reduced Hardware for Sensor Nodes in WBAN," *2020 24th International Symposium on VLSI Design and Test (VDAT)*, Bhubaneswar, India, 2020, pp. 1-6

[10] J. Sarma, S. Chatterjee, R. Biswas and S. Roy, "A Fast Transient Digitally Assisted Flash-Based Modular LDO for Sensor Nodes in WBAN," *2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Limassol, Cyprus, 2020, pp. 363-367

[11] Shatadal Chatterjee; Maryaradhiya Daimari; Sounak Roy. "A Fully Digital Foreground Calibration Technique of A Flash ADC". 2021 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). Jul 2021, 10.1109/ISVLSI51109.2021.00012

Courses Taught

1. Analog Integrated Circuit (UG, Theory + Tutorial)
2. Semiconductor Device Physics (UG, Theory)
4. Analog Circuits (UG, Theory + Tutorial)
5. VLSI Design (UG, Theory)
6. VLSI Design Lab (UG, Practical)
7. Basic Electronics Circuit (UG, Theory + Tutorial)
8. System Modeling Lab (PG, Practical)
9. CAD VLSI Testing (PG, Theory)
10. Semiconductor Device Modelling (PG, theory)

PhD Students

1. Name : **Dr Shatadal Chatterjee**

   Thesis Topic : Calibration of Fast ADCs

   Status : Degree awarded

2. Name : **Abhijit Roy**

   Thesis Topic : Design of High Speed Flash ADC

   Status : Ongoing

Sponsored Project

Name of the Project : **Design of 8 bit 1 GSPS Flash ADC**

Duration of the Project : **2 years**

Sponsoring Agency : **SCL, ISRO**

IIIT Guwahati

Bongora, Assam
Guwahati -781015
INDIA

0824 2474000

registrar@iiitg.ac.in

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