Dr. Sheikh Wasmir Hussain
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Joined the Institute in August 2023

About

Hello, welcome to my home page. I'm an Assistant Professor in the Department of Electronics and Communication Engineering (ECE) at IIIT Guwahati. I joined IIIT Guwahati in August, 2023. Prior to that, I worked as a Senior Research Scientist in the MeLoDe (Memory Logic Devices & Logic Design) Laboratory, with the Dept. of Electrical Engineering at IIT Bombay, Mumbai from October, 2021 to August, 2023. I received the Ph.D. and M.Tech degrees in VLSI Design in 2022 and 2017, respectively, from NIT Meghalaya, Shillong, India and the B.E. degree in ECE in 2013 from NIE Mysore, India.

Research Interests

- Semiconductor Memories (Volatile and Non-Volatile)
- CMOS Digital Circuits
- Low Power VLSI Design
- In-Memory Computing (IMC)
- Low Power Content Addressable Memory (CAM)

Teaching

At IIIT Guwahati, I taught the following courses in Monsoon Semester (2022-2023):

- EC110: Digital Design Lab *(B.Tech)*
- EC302: Analog Integrated Circuit Lab *(B.Tech)*
- EC102: Electrical Circuit Analysis Tutorial *(B.Tech)*
- EC694: Seminar II *(M.Tech)*

and, I'm currently teaching the following courses in Winter Semester (2023-2024):

- EC103: Basic Electronic Circuits *(B.Tech)*
- EC382: Embedded Systems Laboratory *(B.Tech)*

Tapeout

- One time programmable (OTP) memory, physical unclonable function (PUF) and secure circuits in SCL 180-nm technology ***[Role: Layout design]***
- Pre-charge free dynamic content addressable memory in SCL 180-nm technology ***[Role: Layout design]***

Invited Talk

1. ***Expert Speaker*** for Cadence Tutorial, Accelerate Vigyan SERB Workshop on Custom IC Design using EDA, Feb. 27 – Mar. 5, 2022, IIIT Pune, Pune.
2. ***Invited Talk*** on Low-Power and High-Speed Nanometer-CMOS CAMs, Faculty Development Program (FDP), Apr. 26 – May 8, 2021, GITA Autonomous College, Bhubaneshwar.

Achievements, Awards, Fellowships & Others

1. ***Representation of R & D Works,*** G20 Research and Innovation Initiative Gathering (RIIG) Summit & Research Ministers' Meeting, Jul. 2023, IIT Bombay, Mumbai.
2. ***Representation of R & D Works,*** India Semiconductor Mission's Semicon India Conference, July 2023, Mahatma Mandir, Gandhinagar.
3. ***First Prize in Oral Presentation*** in Engineering Discipline, 2nd Research Conclave, Feb. 28 - Mar. 1, 2021, NIT Meghalaya, Shillong.
4. Recognition among ***Top 12 Ph.D. Thesis Works*** in Student Research Form, 34th International Conference on VLSI Design & 20th International Conference on Embedded Systems 2021 (VLSID 2021), Feb. 20 – 24, 2021, India (Virtual).
5. ***International Travel Support***, from MeitY, Govt. of India for Presenting Research Paper at IEEE 6th International Conference on Engineering Technologies and Applied Sciences (ICETAS), Dec. 20-21, 2019, UTMKL, Kuala Lumpur.
6. ***JRF and SRF Fellowships***, under NIT Meghalaya from MoE (then MHRD), Govt. of India for Pursuing Ph.D., Jul. 2017 - Jul. 2021.
7. ***GATE Fellowship***, under NIT Meghalaya from MoE (then MHRD), Govt. of India for Pursuing M.Tech and Teaching Assistantship, Jul. 2015 - May 2017.
8. ***GATE-2015 Qualified***, 6592 All India Rank (AIR) in ECE Discipline, 96.18 Percentile.
9. ***Merit Cum Means (MCM) Scholarship***, under Minority & OBC, Govt. of Manipur for Pursuing B.E., 2010 - 2013.
10. ***AIEEE-2009 Qualified***, 31579 AIR and 47 Manipur State Rank in OBC Category.
11. ***Most Regular Student Award,*** 100% Attendance Record during Academic Session 2006 – 2007 at Herbert School, Imphal.
12. ***Academic Prizes, Appreciations, and Awards*** from various state organizations, Manipur, India for merit in High School Board and Higher Secondary School Council Examinations, 2006 - 2008.

Publication

Journal

- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat, "SMS-CAM: Shared matchline scheme for content addressable memory", Elsevier Integration the VLSI Journal,Vol. 88, (2023), pages. 70-79,
- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat, "Match-line control unit for power and delay reduction in hybrid CAM", IET Circuits, Devices & Systems,15(3), (2021), pages. 272-283, Wiley
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "A novel low-power matchline evaluation technique for content addressable memory (CAM)", Institute of Information Science Journal of Information Science and Engineering,Vol. 36, No. 5, (2020), pages. 1035-1053, (https://doi.org/10.6688/JISE.202009_36(5).0007)
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Energy-efficient precharge-free ternary content addressable memory (TCAM) for high search rate applications", IEEE Transactions on Circuits and Systems I: Regular Papers,Vol. 67, No. 7, (2020), pages. 2345-2357, (https://doi.org/10.1109/TCSI.2020.2978295)
- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat, "Low-power content addressable memory design using two-layer PN match-line control and sensing", Elsevier Integration the VLSI Journal,,Vol. 75, (2020), pages. 73-84, (https://doi.org/10.1016/j.vlsi.2020.06.001)
- S. Mishra, T. V. Mahendra, S. W. Hussain, and A. Dandapat, "The analogy of matchline sensing techniques for content addressable memory (CAM)", IET Computers & Digital Techniques,Vol. 14, No. 3, (2020), pages. 87 - 96, (https://doi.org/10.1049/iet-cdt.2019.0178)
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Low discharge precharge free matchline structure for energy- efficient search using CAM", Elsevier Integration the VLSI Journal,Vol. 69, (2019), pages. 31-39,
- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat, "Match-line division and control to reduce power dissipation in content addressable memory", IEEE Transactions on Consumer Electronics,Vol. 64, No. 3, (2018), pages. 301-309,
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Precharge free dynamic content addressable memory", IET Electronics Letters,Vol. 54, No. 9, (2018), pages. 556-558,

Conference

- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat,, "Pseudo-static master-slave match-line scheme for sustainable-performance and energy-efficient content addressable memory", in IEEE Region 10 Symposium (TENSYMP), Dhaka, Bangladesh, (2020), pages. 258-261,
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "A low-power split-controlled single ended storage content addressable memory", in IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Rourkela, India, (2019), pages. 369-372,
- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat, "Efficient matchline controller for hybrid content addressable memory,", in IEEE 2nd International Conference on Electronics and Communication Engineering (ICECE), Xi'an, China, (2019), pages. 418-422,
- S. W. Hussain, T. V. Mahendra, S. Mishra, and A. Dandapat,, "A quasi-static storage and decision block for performance-efficient content addressable memory", in IEEE 6th International Conference on Engineering Technologies and Applied Sciences (ICETAS), Kuala Lumpur, Malaysia, (2019), pages. 1-6,
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Design and implementation of drivers and selectors for content addressable memory (CAM)", in IEEE 2nd International Conference on Electronics and Communication Engineering (ICECE), Xi'an, China, (2019), pages. 216-220,
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Low match-line voltage swing technique for content addressable memory,", in IEEE 7th International Conference on Smart Computing & Communications (ICSCC), Sarawak, Malaysia, (2019), pages. 1-5,
- T. V. Mahendra, S. W. Hussain, S. Mishra, and A. Dandapat, "Performance analysis of N-CAM, P-CAM and TG-CAM using 45-nm technology", 2019 International Conference on Intelligent Computing and Control Systems (ICCS), (2019), pages. 621-625, IEEE
- K. B. Singh, S. W. Hussain, T. V. Mahendra, and C. V. Rama Rao, "Implementation of OFDM and pulsed-OFDM", in IEEE 15th International Conference on Information Technology (ICIT), Bhubaneswar, India, (2016), pages. 110-113,