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Joined the Institute in January 2022

## About

I am an Assistant Professor in the Department of CSE at Indian Institute of Information Technology, Guwahati. I joined IIITG in January, 2022.

## Research Interests

In-Memory Computing, Neuromorphic Computing using emerging memory technologies.

## Publication

### Journal

- P. L. Thangkhiew, A. Zulehner, R. Wille, K. Datta, I. Sengupta, "An efficient memristor crossbar architecture for mapping Boolean functions using Binary Decision Diagrams (BDD)", Integration,vol 71, (2020), pages. 125-133,
- D. N. Yadav, P. L. Thangkhiew, K. Datta, "Look-ahead mapping of Boolean functions in memristive crossbar array", Integration,vol. 64, (2019), pages. 152-162,
- P. L. Thangkhiew, R. Gharpinde and K. Datta, "Efficient Mapping of Boolean Functions to MemristorCrossbar Using MAGIC NOR Gates", in IEEE Transactions on Circuits and Systems I,vol. 65, no. 8, (2018), pages. 2466-2476, Regular Papers
- P. L. Thangkhiew, K. Datta, "Scalable in-memory mapping of Boolean functions in memristive crossbar array using simulated annealing", in Journal of Systems Architecture,vol. 89, (2018), pages. 49-59,
- R. Gharpinde, P. L. Thangkhiew, K. Datta and I. Sengupta, "A Scalable In-Memory Logic Synthesis Approach Using Memristor Crossbar", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems,vol. 26, no. 2, (2018), pages. 355-366,

### Conference

- P. L. Thangkhiew and K. Datta, "Fast In-Memory Computation of Boolean Functions in Memristive Crossbar Array", 2018 8th International Symposium on Embedded Computing and System Design (ISED), (2018), pages. 105-109, Cochin, India
- D. N. Yadav and P. L. Thangkhiew, "Towards an In-Memory Reconfiguration of Arithmetic Logical Unit using Memristor Crossbar Array", 2018 IEEE International Conference on Electronics, (2018), pages. 1-6, Computing and Communication Technologies (CONECCT),Bangalore, India
- P. L. Thangkhiew, R. Gharpinde, D. N. Yadav, K. Datta, and Indranil Sen Gupta, "Efficient implementation of adder circuits in memristive crossbar array", In TENCON 2017 - 2017 IEEE Region 10 Conference (TENCON 2017), (2017), pages. 207-212, Penang, Malaysia
- P. L. Thangkhiew, R. Gharpinde, P. V. Chowdhary, K. Datta, and I. Sengupta, "Area efficient implementation of ripple carry adder using memristor crossbar arrays", In 2016 11th International Design Test Symposium (IDT), (2016), pages. 142-147, Hammamet, Tunisia

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