

SEQUENTIAL CIRCUIT

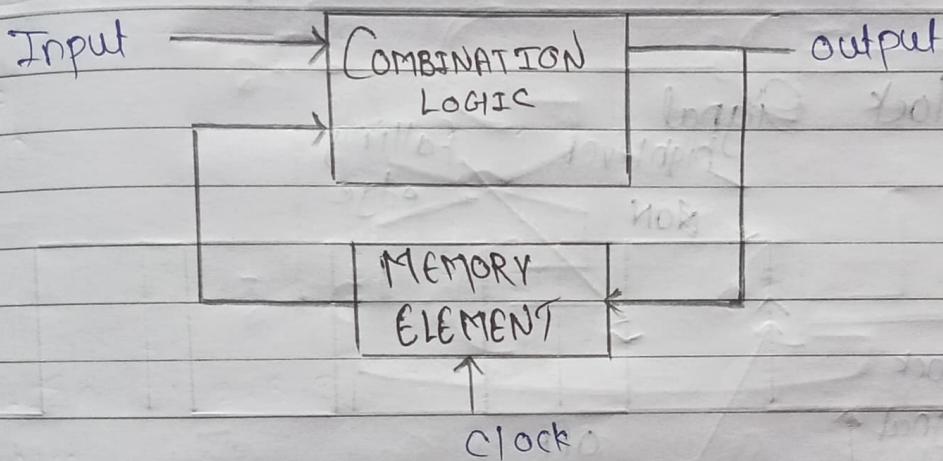
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SEQUENTIAL CIRCUIT :- In this Sequential circuit timing parameter comes into picture.

The output of Sequential circuit depends on the present time inputs, the previous output and the sequence in which inputs are applied.

In order to provide the previous inputs or output a memory element is required.

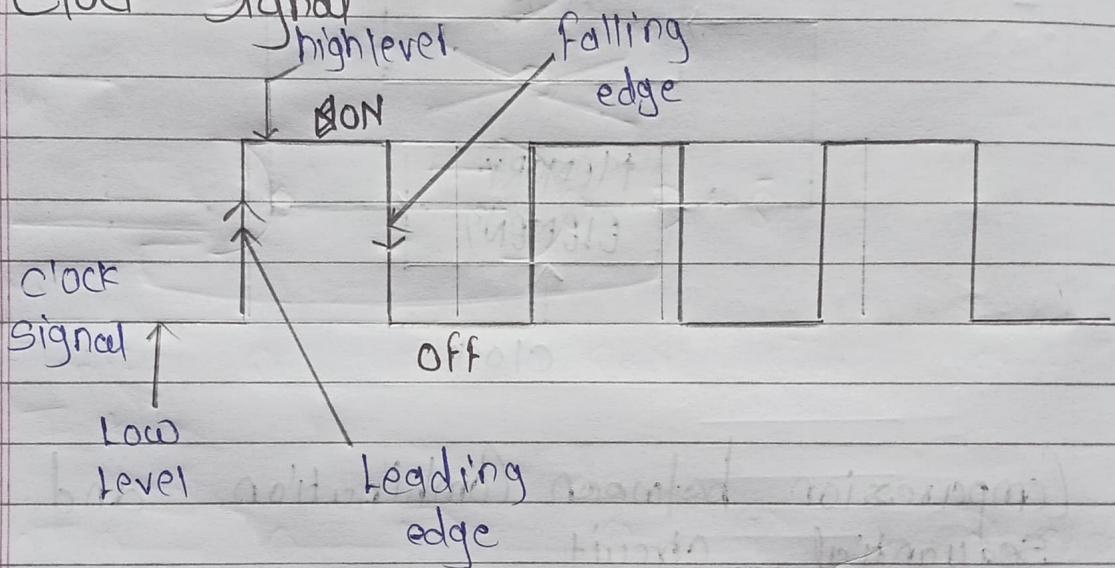


Comparison between Combination and Sequential circuit

Parameter	Combinational	Sequential
1) Output depend on present input	Output depend present input	present input and previous output
2) Memory element	It is not required	It is required

3) Clock Signal	not required	J+ is required
4) Feedback Path	J+ is not present	J+ is present
5) Example	Adder code converter, Subtractor, encoder decoder, 4 Subtractor etc.	flip flop shift registers

Clock Signal

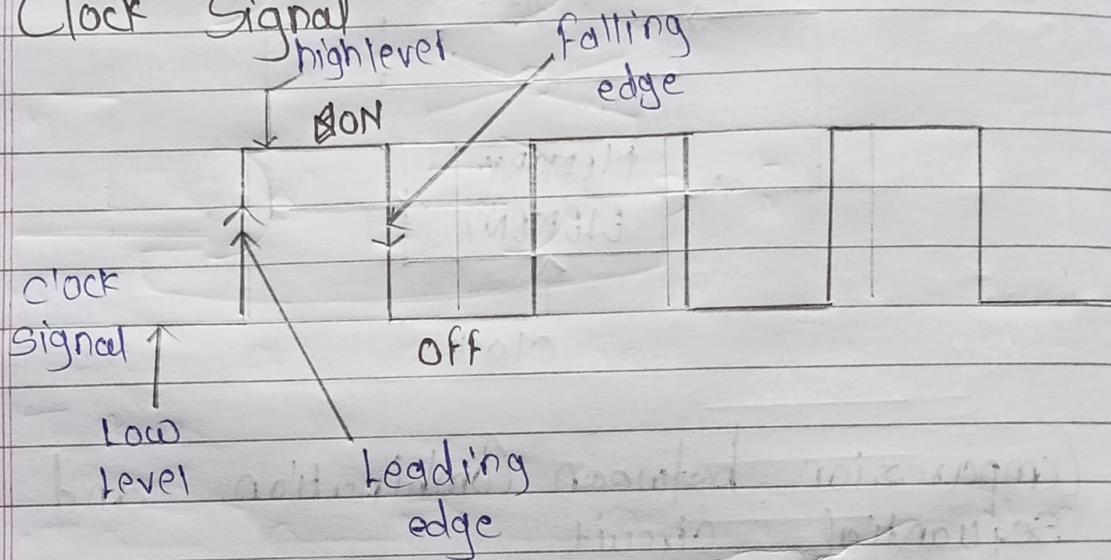


flip-flop

- flip flop is a basic building element of sequential circuit
- It is used as a memory element
- It is also called unit memory cell as it stores single bit at a time

3) Clock signal	not required	It is required
4) Feedback Path	It is not present	It is present
5) Example	Adder code converter, Subtractor, encoder decoder, 4 subtracter etc.	flip flop shift registers

Clock Signal



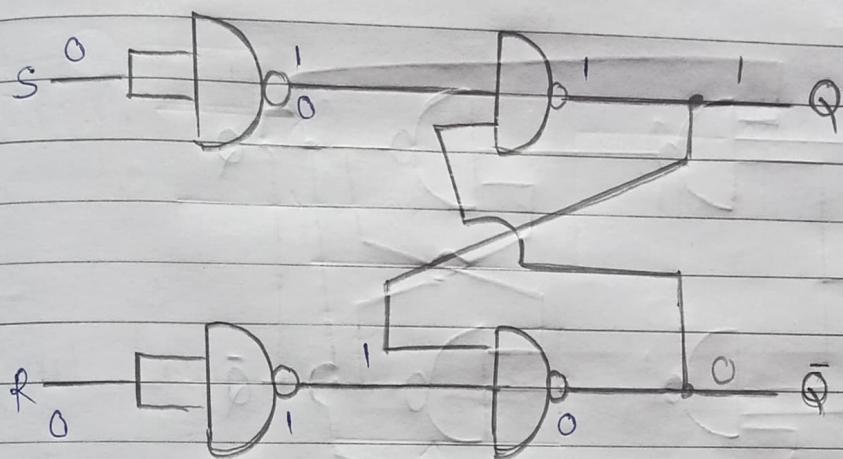
flip-flop

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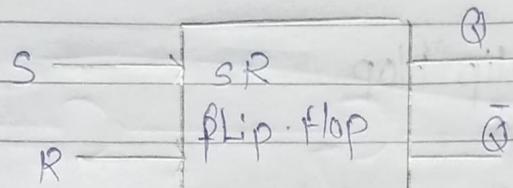
Types of Flip Flop

- 1) SR flip flop
- 2) JK flip flop
- 3) D - flip flop
- 4) T - flip flop

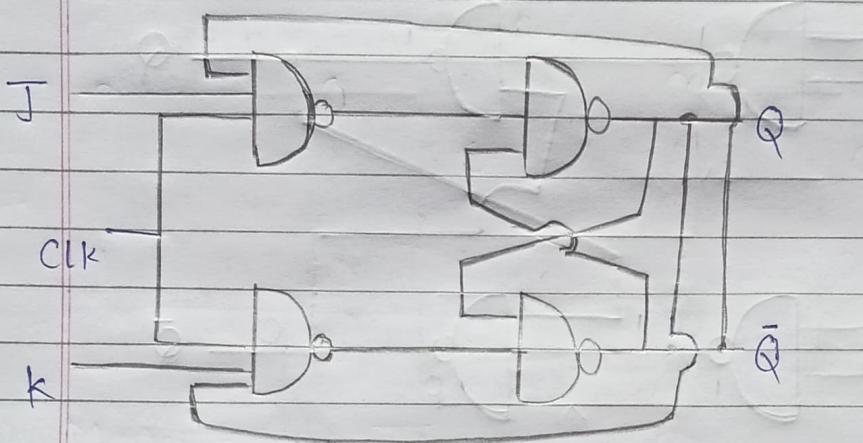
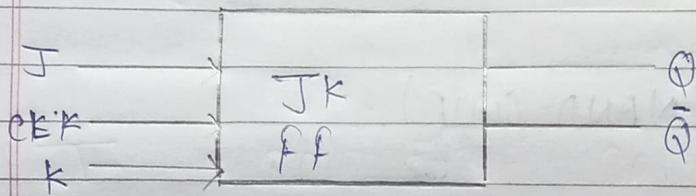
1) SR Flip-Flop (NAND GATE)



Input	Previous O/P	Next O/P	State
S R	Q P Q̄ P	Qn+1 Q̄n+1	
0 0	0 1	0 1	No change
	1 0	1 0	
0 1	0 1	0 1	Reset
	1 0	0 1	
1 0	0 1	1 0	Set
	1 0	1 0	
1 1	0 1	X X	Race (Avoided)
	1 0	X X	

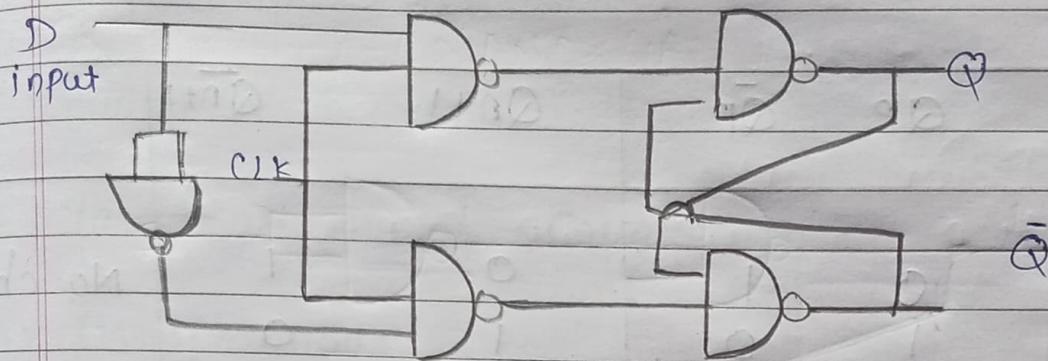
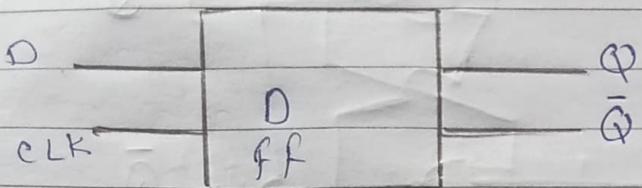


2) JK Flip - Flop



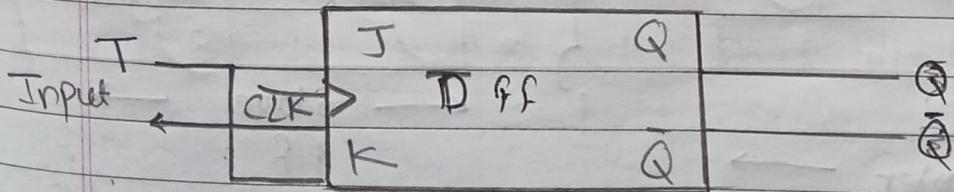
Input	Q_P	\bar{Q}_P	Q_{n+1}	\bar{Q}_{n+1}	state
J K					
0 0	0	1	0	1	No Change
	1	0	1	0	
0 1	0	1	0	1	Reset
	1	0	0	1	
1 0	0	1	1	0	Set
	1	0	1	0	
1 1	0	1	1	0	Toggle
	1	0	0	1	

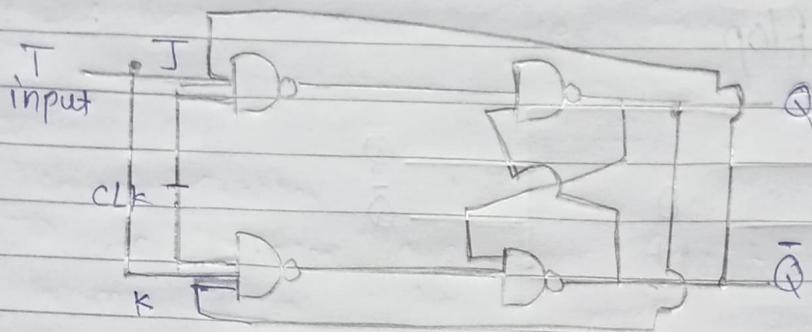
3) D Flip Flop



Input	Q_p	\bar{Q}_p	Q_{n+1}	\bar{Q}_{n+1}	state
0	0	1	0	1	Reset
1	1	0	0	1	Set

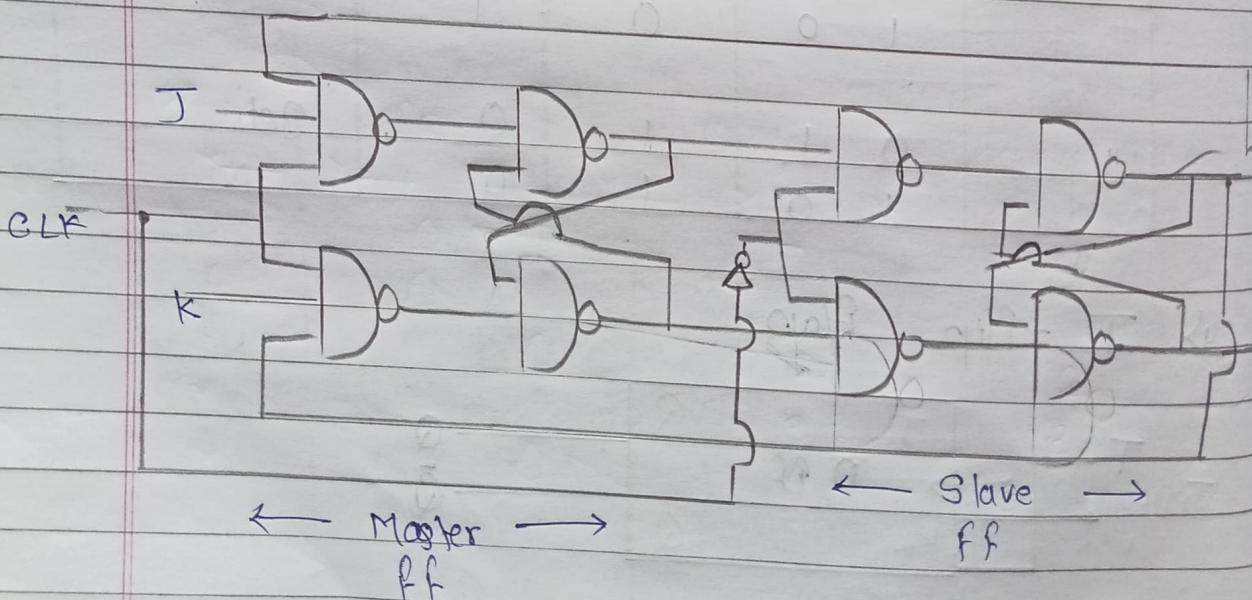
4) T - Flip Flop





T input	Q _n	\bar{Q}_n	Q _{n+1}	\bar{Q}_{n+1}	
0	0	1	0	1	No change
1	1	0	1	0	Toggle

Master - Slave JK flip-flop



10/23

Counters :- The digital circuit used for counting pulses known as counter

- It is a sequential circuit
- Counter is the most widely used application of flip-flop
- Counter counts the number of clock pulses

Classification of counters

(1) Asynchronous
or Ripple

(2) Synchronous

Counters have basically of two types Asynchronous or Ripple or Synchronous

(1) Asynchronous

For this counters the external clock signal is applied to 1 flip flop and then they output preceding flip flop connected to the clock of next flip flop

(2) Synchronous Counter

In this counter all the flip flop receive the external clock single simultaneously

(3) Up Counter

Up counter are the counter the count from

Small to larger value there output goes on increasing for every clock pulses

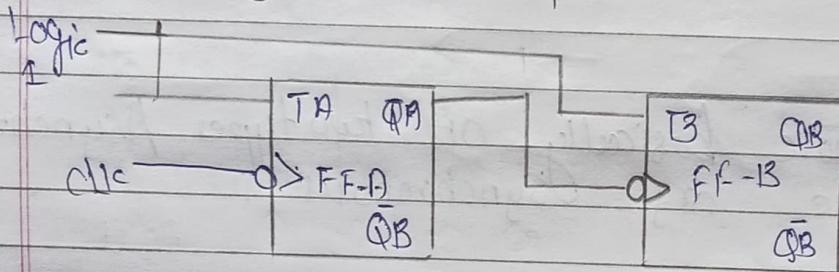
④ Down Counter

Down Counter are the Counters that counts from large to small value. their output goes on decreasing for every clock pulses.

⑤ Up / Down Counter

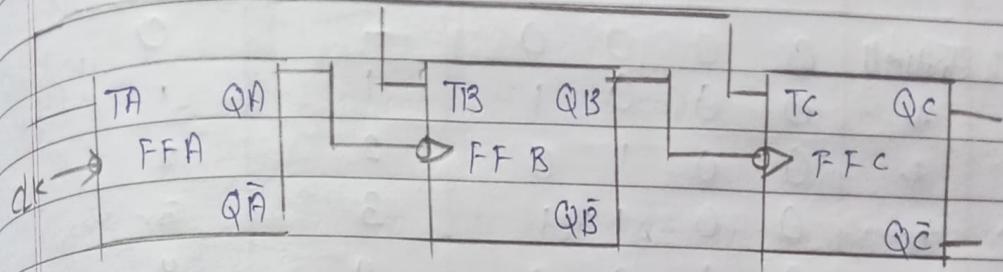
Combination of up & down counter

2-bit asynchronous up Counter

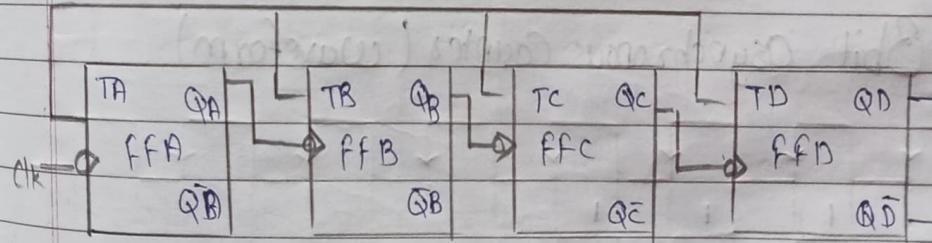


clock	Q _B	Q _A	State	Decimal value
Initially	0	0	-	0
+	0	1	1	1
+	1	0	2	2
+	1	1	3	3
+	0	0	4	0 (Reset)

3-bit Asynchronous Up Counter



Clock	Q_C	Q_B	Q_A	State	Decimal value
Initial	0	0	0	-	0
↓	0	0	1	1	1
↓	0	1	0	2	2
↓	0	1	1	3	3
↓	1	0	0	4	4
↓	1	0	1	5	5
↓	1	1	0	6	6
↓	1	1	1	7	7
↓	0	0	0	8	8 (Reset)



4-bit Asynchronous Up Counter

clock	QD	QC	QB	QA	state	Decimal value
Initial	0	0	0	0	-	0
↓	0	0	0	1	1	1
↓	0	0	1	0	2	2
↓	0	0	1	1	3	3
↓	0	1	0	0	4	4
↓	0	1	0	1	5	5
↓	0	1	1	0	6	6
↓	0	1	1	1	7	7
↓	1	0	0	0	8	18
↓	1	0	0	1	9	9
↓	1	0	1	0	10	10
↓	1	0	1	1	11	11
↓	1	1	0	0	12	12
↓	1	1	0	1	13	13
↓	1	1	1	0	14	14
↓	1	1	1	1	15	15
↓	0	0	0	0	16	16 (Reset)

Date
11/10/2023

8bit Asynchronous Counter (waveform)

Design MOD-5 asynchronous Ripple Counter.

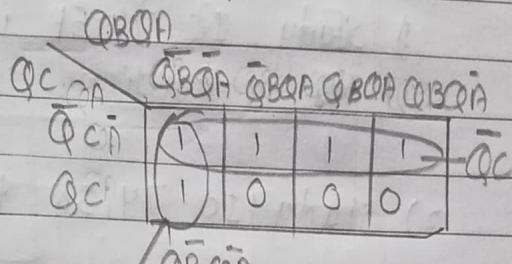
MON - 5

$N=5 \rightarrow$ No. of states

Count values $\rightarrow 0 + 4$

3 bit counter $\rightarrow 3FF$

K-map for Y



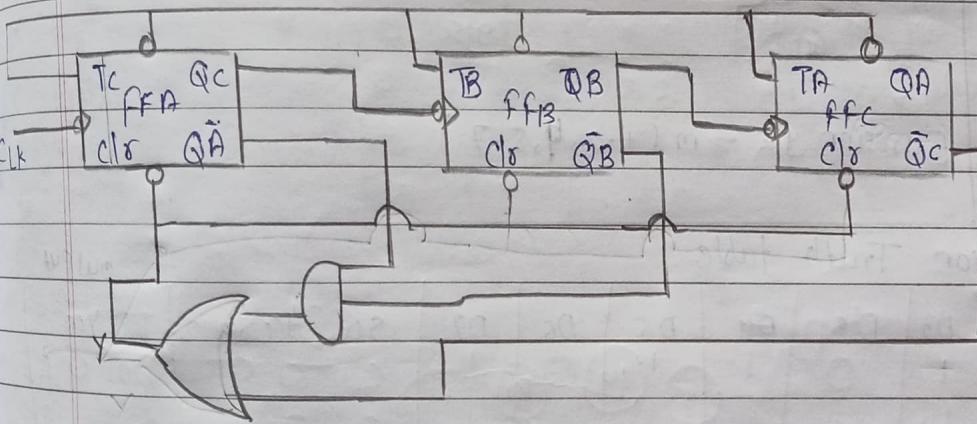
$$Y = \bar{Q}_C + \bar{Q}_B \bar{Q}_A$$

State	Q_C	Q_B	Q_A	Output
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

Pr Cr

1 0 \rightarrow 0 clear

0 1 \rightarrow 1 pre



* ① Decade Ripple Counter (Mode 10 counter)

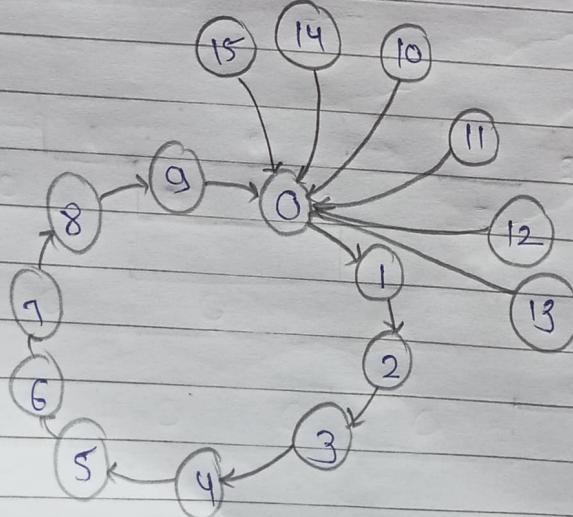
Step 2

Reset circuit.

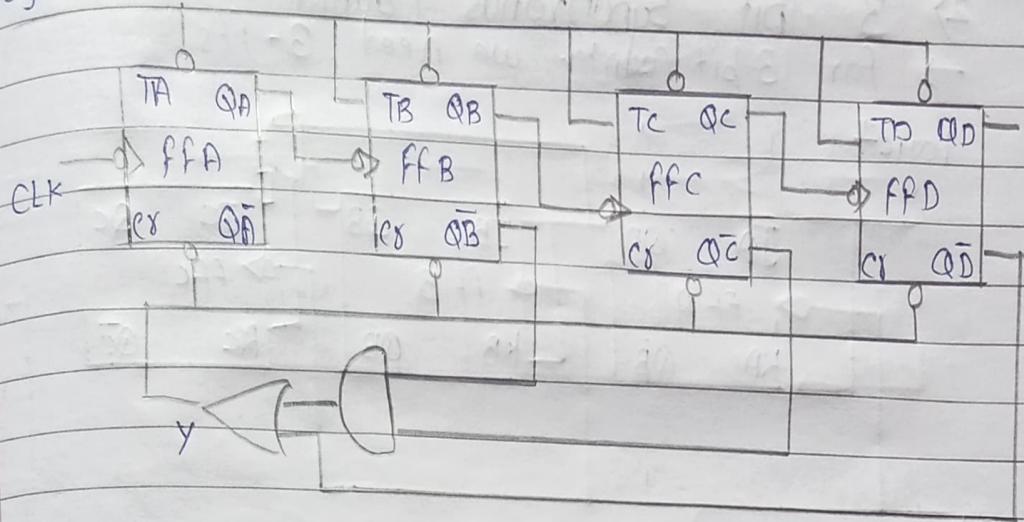
Q_D	Q_C	Q_B	Q_A	y	$Q_D Q_B$	$Q_D Q_C$	$Q_B Q_A$	$Q_B Q_D$	$Q_C Q_A$	$Q_C Q_D$	$Q_D \bar{Q}_C$	$\bar{Q}_D Q_C$	$Q_D \bar{Q}_A$	$\bar{Q}_B Q_D$	$Q_B \bar{Q}_A$	$Q_C \bar{Q}_B$
0	0	0	0	1	00	00	00	00	00	00	11	11	11	11	11	11
0	0	0	1	1	00	00	01	01	01	01	11	11	11	11	11	11
0	0	1	0	1	00	00	01	01	01	01	11	11	11	11	11	11
0	0	1	1	1	00	00	01	01	01	01	11	11	11	11	11	11
0	1	0	0	0	01	01	00	00	00	00	11	11	11	11	11	11
0	1	0	1	1	01	01	00	00	00	00	11	11	11	11	11	11
0	1	1	0	1	01	01	10	10	10	10	11	11	11	11	11	11
0	1	1	1	0	01	01	11	11	11	11	11	11	11	11	11	11
1	0	0	0	0	10	10	00	00	00	00	11	11	11	11	11	11
1	0	0	1	1	10	10	01	01	01	01	11	11	11	11	11	11
1	0	1	0	0	10	10	11	11	11	11	11	11	11	11	11	11
1	0	1	1	1	10	10	11	11	11	11	11	11	11	11	11	11
1	1	0	0	0	11	11	00	00	00	00	11	11	11	11	11	11
1	1	0	1	1	11	11	01	01	01	01	11	11	11	11	11	11
1	1	1	0	0	11	11	11	11	11	11	11	11	11	11	11	11
1	1	1	1	1	11	11	11	11	11	11	11	11	11	11	11	11

State diagram

Step :-



Log 1

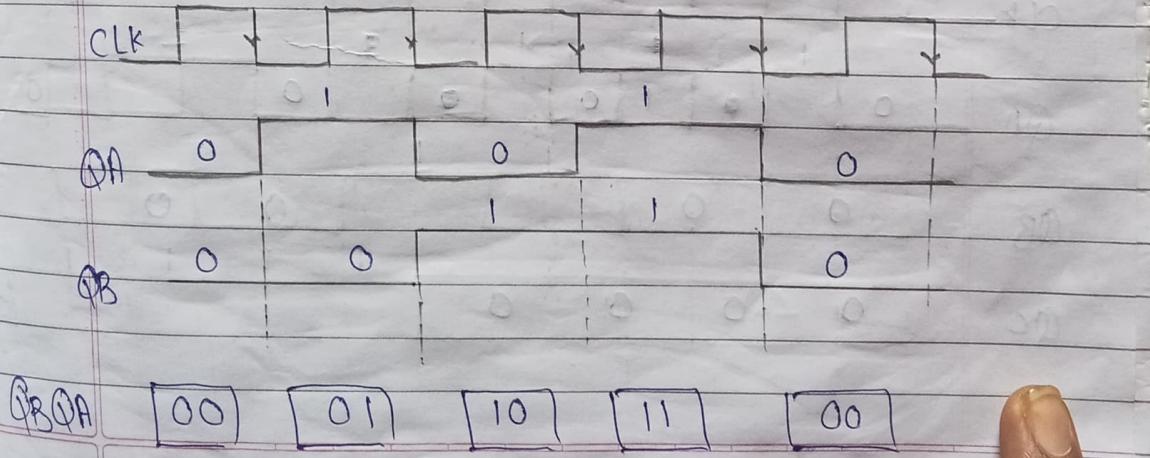


Synchronous Counter

↳ 2 bit Synchronous Counter
→ For 2 bit we need 2-ff

logic \pm

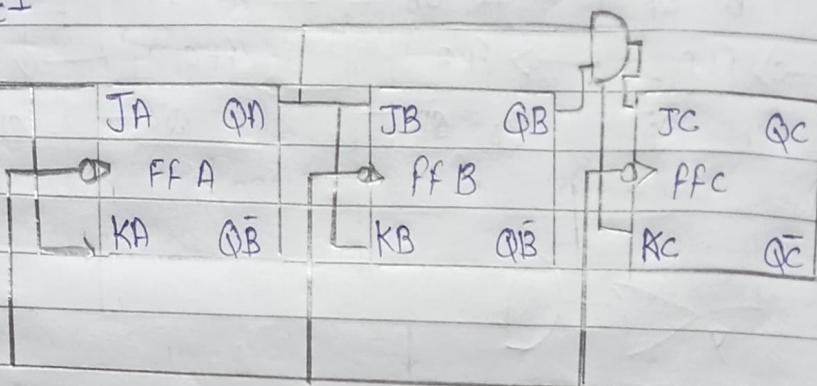
			clock	Counter output	Decimal value
			Initially	Q _B Q _A	Q _B Q _A
JK FF A	JA Q _A	JK FF B	↓	0 1	1
K _A Q _A	KB Q _B	↓	1 0	2	
CL			↓	1 1	3
			↑	0 0	0



2) 3 bit Synchronous Counter

→ For 3-bit Counter we need 3-FFs

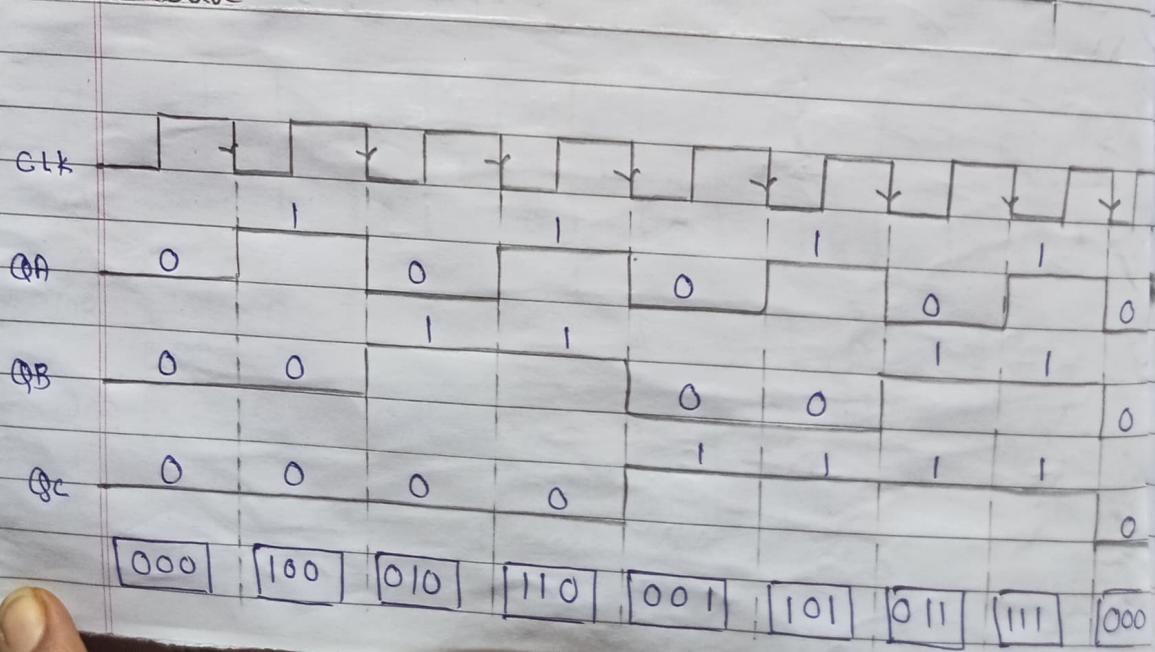
Logic¹



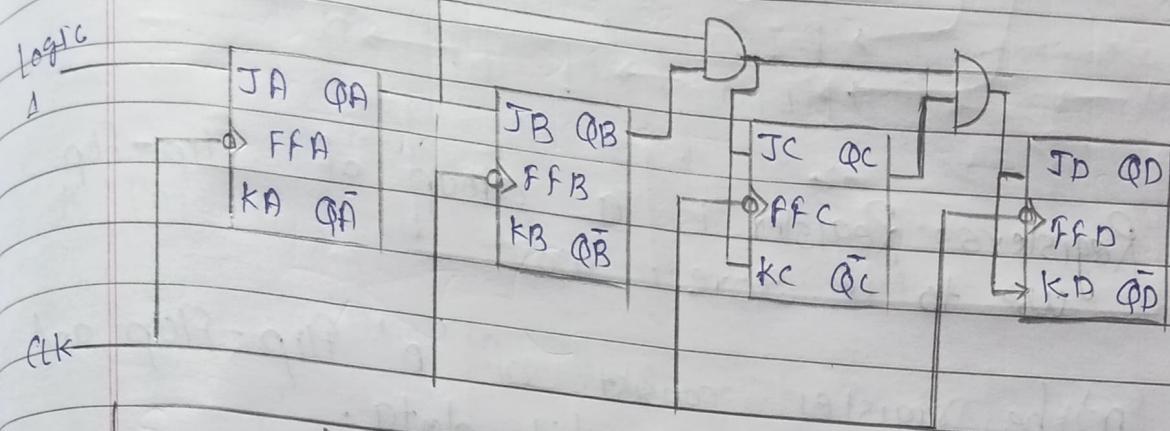
CLK

CLK	Counter output Q_A Q_B Q_C	Decimal
Initially	0 0 0	0
↓	0 0 1	1
↓	0 1 0	2
↓	0 1 1	3
↓	1 0 0	4
↓	1 0 1	5
↓	1 1 0	6
↓	1 1 1	7
↓	0 0 0	0 (Reset)

Wave

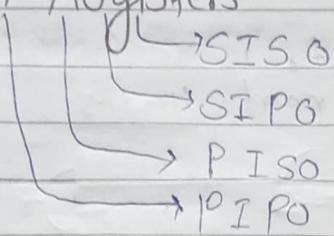


4 bit Synchronous Counter
→ for 4-bit Counter we need 4-PFs



CLK	Counter Output				Decimal
	Q _D	Q _C	Q _B	Q _A	
Initially	0	0	0	0	0
↓	0	0	0	1	1
↓	0	0	1	0	2
↓	0	0	1	1	3
↓	0	1	0	0	4
↓	0	1	0	1	5
↓	0	1	1	0	6
↓	0	1	1	1	7
↓	1	0	0	0	8
↓	1	0	0	1	9
↓	1	0	1	0	10
↓	1	0	1	1	11
↓	1	1	0	0	12
↓	1	1	0	1	13
↓	1	1	1	0	14
↓	1	1	1	1	15
↓	0	0	0	0	16 Reset

Shift Registers



* Registers: Register is a group of flip-flop used to store word

'n' bit register consist of 'n' flip-flop and able to stored n bit data.

* Shift Register: The binary data in a register can be transfer while within within the register from 1 flip-flop to another with application of clock pulses

the registers that allow such as data transfer are called shift register.

* Mode of operation of shift register.

-i) Serial in serial out (SISO)

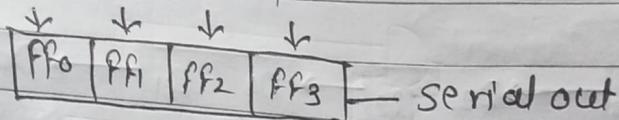
Serial data input \rightarrow [ff₀ | ff₁ | ff₂ | ff₃] \rightarrow Serial data out put

* Serial input - serial parallel output (SIPO)

Serial input \rightarrow [ff₀ | ff₁ | ff₂ | ff₃]
 ↓ ↓ ↓ ↓
 parallel output

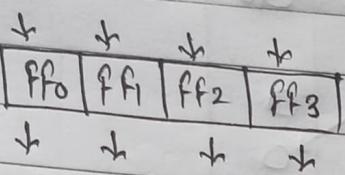
* Parallel input and serial output (PISO)

Parallel Input



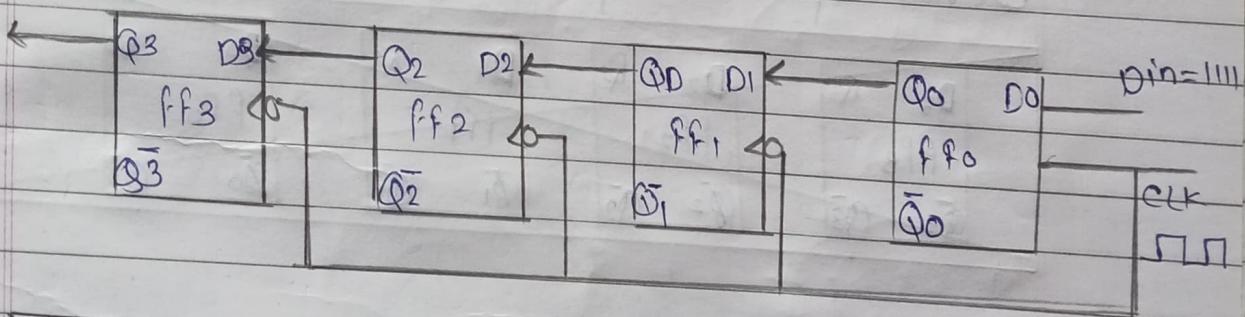
* Parallel input and parallel output

Parallel Input

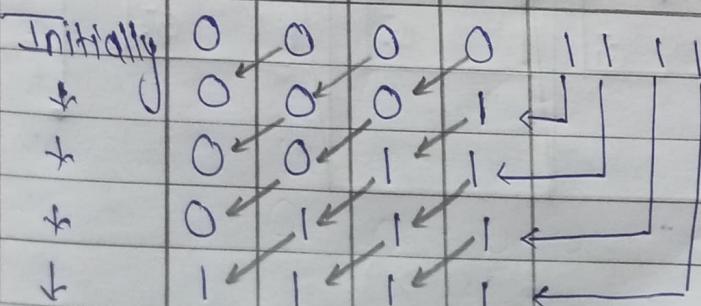


Parallel output

▷ Serial input Serial output (Shift left mode)

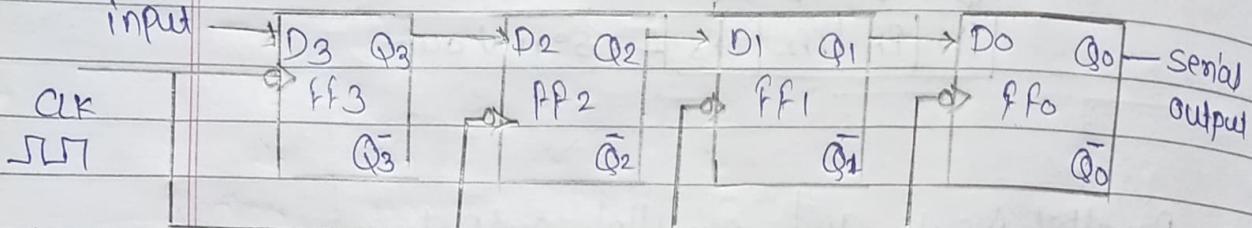


CLK	Q3	Q2	Q1	Q0	Data in Din
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- Serial input Serial output (shift right mode)

Serial data

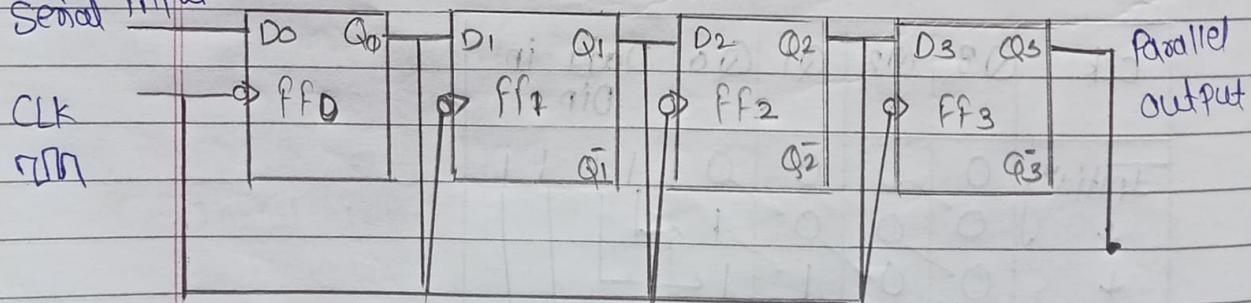


CLF	Din	Q ₃	Q ₂	Q ₁	Q ₀
Initially		0	0	0	0
↓	1 →	1	0	0	0
↓	1 →	1	1	0	0
↓	1 →	1	1	1	0
↓	1 →	1	1	1	1

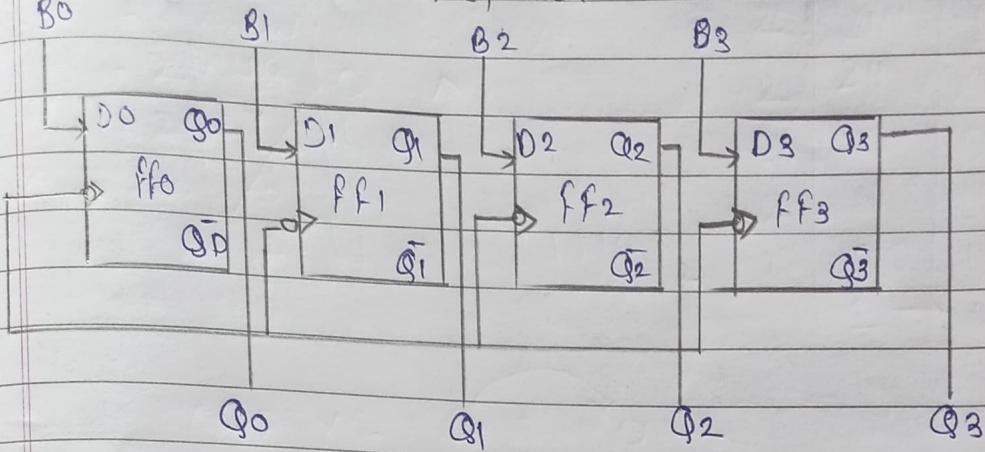
- Serial input and parallel output (shift left mode)

Q ₃	Q ₂	Q ₁	Q ₀
FF ₃	FF ₂	FF ₁	FF ₀
Q̄ ₃	Q̄ ₂	Q̄ ₁	Q̄ ₀

Serial input



Parallel in Parallel out.



Parallel in Serial out

