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Sum-of-Products (SOP) form

ex. – $Y = AB + AC + BC$

– $Y = ABC + BCD + AB\bar{D}$

Product of the sum (POS) form

ex. $Y = (A+B)\cdot(B+C)\cdot(A+C)$

Standard or canonical SOP

– Each term must contain all the available input variables

ex. $Y = ABC + A\bar{B}\bar{C} + \bar{A}BC \rightarrow$ standard SOP

$Y = AB + AB\bar{C} + \bar{A}BC \rightarrow$ Non-standard SOP

Conversion of logic expression to standard SOP

1) For each term find missing variable
2) Form term by ORing the missing variable & its complement and AND with term.

ex.

a) convert $Y = AB + A\bar{C} + BC$ into canonical SOP

$Y = AB\cdot(C+\bar{C}) + A\bar{C}(B+\bar{B}) + BC(A+\bar{A})$

$= ABC + AB\bar{C} + A\bar{C}B + A\bar{C}\bar{B} + BCA + BC\bar{A}$

$= (ABC + BCA) + (AB\bar{C} + A\bar{C}B) + A\bar{B}\bar{C} + BC\bar{A}$

$= ABC + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$

$\cancel{= AB(C+\bar{C})}$

b) $Y = \cancel{AB + AC + BC}\ A + BC + ABC$

$= A\cdot(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A}) + ABC$

$= (AB + A\bar{B})(C+\bar{C}) + BCA + BC\bar{A} + ABC$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + BCA + BC\bar{A} + ABC$

$Y = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + BC\bar{A}$

Standard OR canonical POS

$Y = (A+B+\bar{C}) \cdot (A+\bar{B}+C) \cdot (\bar{A}+\bar{B}+\bar{C})$ – Standar

$Y = (\bar{A}+B) \cdot (A+B+C) \rightarrow$ Non Standard POS

conversion into POS form

1) Find missing variable
2) Form term by ANDing the missing variable with its complement and OR with term.

ex:

a) convert $Y = (A+B)(A+C)(B+\bar{C})$ into Standard POS form

$\rightarrow$

$Y = \cancel{(A+B)+}$

$= (A+B+C\cdot\bar{C})(A+C+B\cdot\bar{B})\cdot(B+\bar{C}+A\cdot\bar{A})$

$= (A+B+C)(A+B+\bar{C})\cdot(A+C+B)(A+C+\bar{B})$
$(B+\bar{C}+A)(B+\bar{C}+\bar{A})$

$= (A+B+C) + (A+B+\bar{C})(A+C+\bar{B})$
$(\bar{A}+B+\bar{C}$

H.W

b) $Y = (A+B)(\bar{B}+C)$ convert into Standard POS form

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Minterm: Each individual term in the standard SOP form is called as minterm

Maxterm: Each individual term in the standard POS form is called as maxterm.

Standard SOP $Y = ABC + A\bar{B}\bar{C} + \bar{A}B\bar{C}$ → minterms

standard POS $Y = (A+B)\cdot(A+\bar{B})$ → maxterms

Variables A	B	C	minterms m_i	Maxterms M_i
0	0	0	$\bar{A}\bar{B}\bar{C} = m_0$	$A+B+C = M_0$
0	0	1	$\bar{A}\bar{B}C = m_1$	$A+B+\bar{C} = M_1$
0	1	0	$\bar{A}B\bar{C} = m_2$	$A+\bar{B}+C = M_2$
0	1	1	$\bar{A}BC = m_3$	$A+\bar{B}+\bar{C} = M_3$
1	0	0	$A\bar{B}\bar{C} = m_4$	$\bar{A}+B+C = M_4$
1	0	1	$A\bar{B}C = m_5$	$\bar{A}+B+\bar{C} = M_5$
1	1	0	$AB\bar{C} = m_6$	$\bar{A}+\bar{B}+C = M_6$
1	1	1	$ABC = m_7$	$\bar{A}+\bar{B}+\bar{C} = M_7$

* $Y = \underbrace{ABC}_{m_7} + \underbrace{\bar{A}BC}_{m_3} + \underbrace{A\bar{B}\bar{C}}_{m_4}$

$Y = m_7 + m_3 + m_4$

$\boxed{Y = \Sigma m(3,4,7)}$ minterm representation

* $Y = \underbrace{(A+\bar{B}+C)}_{M_2}\cdot\underbrace{(A+B+C)}_{M_0}\underbrace{(\bar{A}+\bar{B}+C)}_{M_6}$

$Y = M_2 \cdot M_0 \cdot M_6$

$\boxed{Y = \Pi M(0,2,6)}$ maxterm representatio

* convert SOP into POS

① $Y = A\bar{C} + AB$

convert POS into SOP

② $Y = (A+B)(B+C)$

Karnaugh-Map (K-map)

K-map is a graphical method of simplifying a boolean equation.

K-Map structure

1) 2-variable ($2^2 = 4$ boxes)

A \ B	$\bar{B}$	B
0 $\bar{A}$	0	1
1 A	2	3

2) 3-variables ($2^3 = 8$ boxes)

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	3	2
A 1	4	5	7	6

3) 4-variables ($2^4 = 16$)

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	1	3	2
$\bar{A}B$ 01	4	5	7	6
AB 11	12	13	15	14
$A\bar{B}$ 10	8	9	11	10

Truth table to K-map

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$\Rightarrow$

A \ B	$\bar{B}$	B
$\bar{A}$	0	0
A	0	1

Represent the equation on K-map

① $Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C} + ABC \longrightarrow$ SOP form

→ 3-variables are there A, B, C

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	0	0
A	1	0	1	1

$Y = \bar{A}\bar{B} + \bar{B}\bar{C} + AB$

HW ② $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}BC\bar{D} + AB\bar{C}\bar{D}$

* Way of grouping
  - Pairs
  - Quads
  - Octets

* Minimization of SOP expression using K-map

① $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1		1	1
A 1		1		

$\bar{A}\bar{C}$

$\bar{A}B$

$A\bar{B}C$

$Y = \bar{A}B + \bar{A}\bar{C} + A\bar{B}C$

② $Y = \sum m(0, 1, 2, 5, 13, 15)$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	0	1
$\bar{A}B$		1	0	
AB		1	1	
$A\bar{B}$				

$\rightarrow \bar{A}\bar{B}\cancel{C}\bar{D}$

$\bar{A}\bar{C}D$

ABD

HW!

$Y = \cancel{\bar{A}\bar{B}\bar{D}} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{C}D + ABD$

③ Simplify the expression using k-map

$Y = \Sigma m(1,3,7,11,15) + d(0,2,5)$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	X	1	1	X
$\bar{A}B$		X	1	
$A\bar{B}$			1	
AB			1	

$\bar{A}\bar{B}$

CD

$Y = \bar{A}\bar{B} + CD$

<u>Minimization of POS expression using k-map</u>

① $Y = (A+B+C)\cdot(A+\bar{B}+C)(\bar{A}+\bar{B}+C)$

$Y = (000)\cdot(010)(110)$

$\quad M_0 \quad M_2 \quad M_6$

$Y = \pi M(\cancel{M_0}\ 0,2,6)$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
0 $\bar{A}$	0			0
1 A				0

$A+C$

$\bar{B}+C$

$Y = (\bar{B}+C)(A+C)$

② $Y = \pi M(0,2,3,5,7,\cancel{9},8,11,15)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	(1)	0 (3)	0 (2)
$\bar{A}B$	(4)	0 (5)	0 (7)	(6)
AB	(12)	(13)	0 (15)	(14)
$A\bar{B}$	0 (8)	(9)	0 (11)	(10)

$(A+B+\bar{D})$

$(A+\bar{B}+\bar{D})$

$\bar{C}+\bar{D}$

$Y = (A+B+D)\cdot(A+\bar{B}+\bar{D})\cdot(\bar{C}+\bar{D})$

(3) $Y = \pi M(0,2,5,7,8,10,12,14)$ simplify using k-map

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	(1)	(3)	0 (2)
$\bar{A}B$	(4)	0 (5)	0 (7)	(6)
AB	0 (12)	(13)	(15)	0 (14)
$A\bar{B}$	0 (8)	(9)	(11)	0 (10)

$B + D$

$A + \bar{B} + \bar{D}$

$\bar{A} + D$

$$Y = (B+D)(A+\bar{B}+\bar{D})(\bar{A}+D)$$

* 5-variable k-map

ex. simplify the following equation using k-map

$$Y = \Sigma m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$$

→ The number of cells in a five variable is 32 (2^5)

→ Therefore two 16-cell k-maps are used

A = 0

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	1 (0)	(1)	(3)	1 (2)
$\bar{B}C$	1 (4)	(5)	(7)	1 (6)
BC	(12)	1 (13)	1 (15)	(14)
$B\bar{C}$	(8)	1 (9)	1 (11)	(10)

$\leftarrow \bar{A}\bar{B}\bar{E}$

A = 1

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	(16)	1 (17)	(19)	(18)
$\bar{B}C$	(20)	1 (21)	(23)	(22)
BC	(28)	1 (29)	1 (31)	(30)
$B\bar{C}$	(24)	1 (25)	1 (27)	(26)

$A\bar{D}E$

BE

$$\boxed{Y = \bar{A}\bar{B}\bar{E} + A\bar{D}E + BE}$$

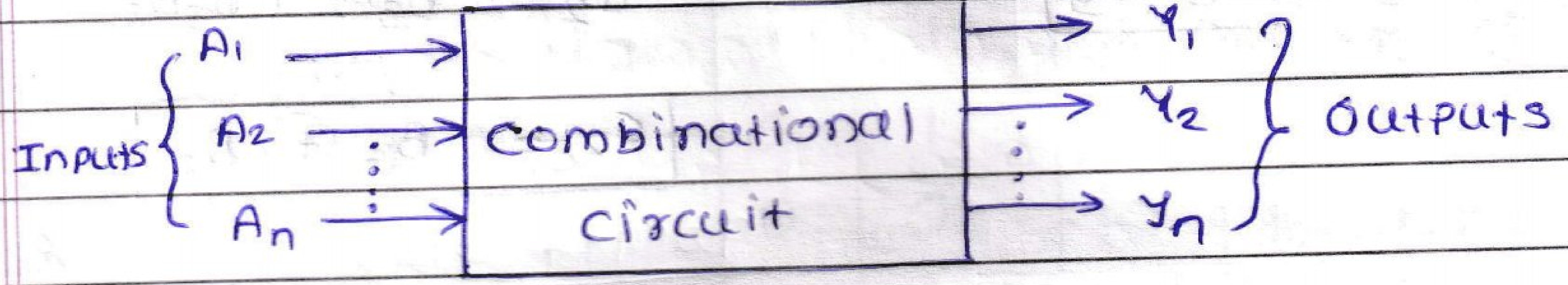
UNIT III

Combinational Logic Circuits & Arithmetic Circuits

Types of Digital circuits:

1) combinational logic circuits
2) sequential logic circuits

combinational circuits



Code converter

① Binary to Gray code converter

Decimal	Binary inputs B_3	B_2	B_1	B_0	Gray outputs G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-map for each Gray output

For G_3

$B_3B_2 \backslash B_1B_0$	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	0	0	0	0
$\bar{B_3}B_2$	0	0	0	0
B_3B_2	1	1	1	1
$B_3\bar{B_2}$	1	1	1	1

$Y = B_3$ $\boxed{G_3 = B_3}$

For output G_2

$B_3B_2 \backslash B_1B_0$	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	0	0	0	0
$\bar{B_3}B_2$	1	1	1	1
B_3B_2	0	0	0	0
$B_3\bar{B_2}$	1	1	1	1

$G_2 = \bar{B_3}B_2 + B_3\bar{B_2}$

$\boxed{G_2 = B_3 \oplus B_2}$

For output G_1

$B_3B_2 \backslash B_1B_0$	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	0	0	1	1
$\bar{B_3}B_2$	1	1	0	0
B_3B_2	1	1	0	0
$B_3\bar{B_2}$	0	0	1	1

$G_1 = B_2\bar{B_1} + \bar{B_2}B_1$

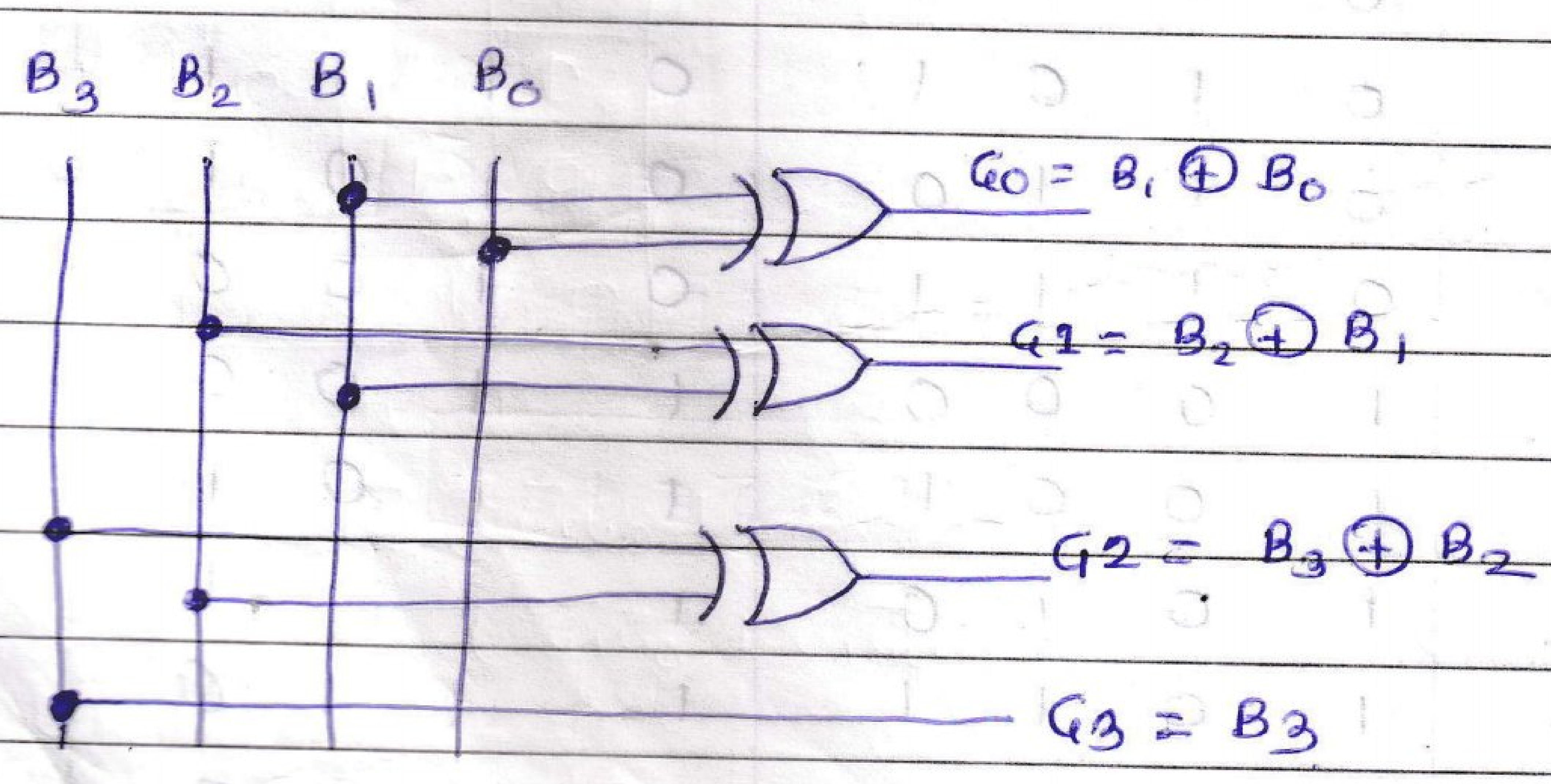
$\boxed{G_1 = B_2 \oplus B_1}$

For output G_0

$B_3B_2 \backslash B_1B_0$	$\bar{B_1}\bar{B_0}$	$\bar{B_1}B_0$	B_1B_0	$B_1\bar{B_0}$
$\bar{B_3}\bar{B_2}$	0	1	0	1
$\bar{B_3}B_2$	0	1	0	1
B_3B_2	0	1	0	1
$B_3\bar{B_2}$	0	1	0	1

$G_0 = \bar{B_1}B_0 + B_1\bar{B_0}$

$\boxed{G_0 = B_1 \oplus B_0}$



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(2) Gray to Binary converter

Decimal	Gray code input G_3	G_2	G_1	G_0	Binary output B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1	0
2	0	0	1	0	0	0	1	1
6	0	1	1	0	0	1	0	0
7	0	1	1	1	0	1	0	1
5	0	1	0	1	0	1	1	0
4	0	1	0	0	0	1	1	1
12	1	1	0	0	1	0	0	0
13	1	1	0	1	1	0	0	1
15	1	1	1	1	1	0	1	0
14	1	1	1	0	1	0	1	1
10	1	0	1	0	1	1	0	0
11	1	0	1	1	1	1	0	1
9	1	0	0	1	1	1	1	0
8	1	0	0	0	1	1	1	1

K-map

For output B_3

$G_3G_2 \backslash G_1G_0$	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0	0	0	0
$\bar{G}_3G_2$	0	0	0	0
G_3G_2	1	1	1	1
$G_3\bar{G}_2$	1	1	1	1

$\boxed{B_3 = G_3}$

For output B_2

	0_0	0_1	0_3	0_2
	1_4	1_5	1_7	1_6
	0_{12}	0_{13}	0_{15}	0_{14}
	1_8	1_9	1_{11}	1_{10}

$B_2 = G_2 \oplus G_3$

For output B1

$G_3G_2 \backslash G_1G_0$	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0 (0)	0 (1)	1 (3)	1 (2)
$\bar{G}_3G_2$	1 (4)	1 (5)	0 (7)	0 (6)
G_3G_2	0 (12)	0 (13)	1 (15)	1 (14)
$G_3\bar{G}_2$	1 (8)	1 (9)	0 (11)	0 (10)

$Y = \bar{G}_3\bar{G}_2G_1 + \bar{G}_3G_2\bar{G}_1 + G_3G_2G_1 + G_3\bar{G}_2\bar{G}_1$

$$Y = \bar{G}_3\bar{G}_2G_1 + \bar{G}_3G_2\bar{G}_1 + G_3G_2G_1 + G_3\bar{G}_2\bar{G}_1$$
$$= G_1(\bar{G}_3\bar{G}_2 + G_3G_2) + \bar{G}_1(\bar{G}_3G_2 + G_3\bar{G}_2)$$
$$= G_1(\overline{G_3 \oplus G_2}) + \bar{G}_1(G_3 \oplus G_2)$$

Let $G_3 \oplus G_2 = X$

$$= G_1\bar{X} + \bar{G}_1X$$
$$= G_1 \oplus X$$

$$\boxed{B1 = G_1 \oplus G_2 \oplus G_3}$$

For output B0

	$\bar{G}_1\bar{G}_0$	$\bar{G}_1G_0$	G_1G_0	$G_1\bar{G}_0$
$\bar{G}_3\bar{G}_2$	0 (0)	1 (1)	0 (3)	1 (2)
$\bar{G}_3G_2$	1 (4)	0 (5)	1 (7)	0 (6)
G_3G_2	0 (12)	1 (13)	0 (15)	1 (14)
$G_3\bar{G}_2$	1 (8)	0 (9)	1 (11)	0 (10)

$Y = \bar{G}_1G_0\bar{G}_3\bar{G}_2 + \bar{G}_3\bar{G}_2G_1\bar{G}_0 + \bar{G}_3G_2\bar{G}_1\bar{G}_0 + \bar{G}_3G_2G_1G_0 + G_3G_2\bar{G}_1G_0 + G_3G_2G_1\bar{G}_0 + G_3\bar{G}_2\bar{G}_1\bar{G}_0 + G_3\bar{G}_2G_1G_0$

$$B0 = \bar{G}_3\bar{G}_2(\bar{G}_1G_0 + G_1\bar{G}_0) + \bar{G}_3G_2(\bar{G}_1\bar{G}_0 + G_1G_0) + G_3G_2(\bar{G}_1G_0 + G_1\bar{G}_0) + G_3\bar{G}_2(\bar{G}_1\bar{G}_0 + G_1G_0)$$

$$= \bar{G}_3\bar{G}_2(G_1 \oplus G_0) + \bar{G}_3G_2(\overline{G_1 \oplus G_0}) + G_3G_2(G_1 \oplus G_0) + G_3\bar{G}_2(\overline{G_1 \oplus G_0})$$

$$B_0 = G_1 \oplus G_0 \left(\overline{G_3}\,\overline{G_2} + G_3 G_2 \right) + \overline{G_1 \oplus G_0} \left(\overline{G_3} G_2 + G_3 \overline{G_2} \right)$$

$$= G_1 \oplus G_0 \left(\overline{G_3 \oplus G_2} \right) + \overline{G_1 \oplus G_0} \cdot \left(G_3 \oplus G_2 \right)$$

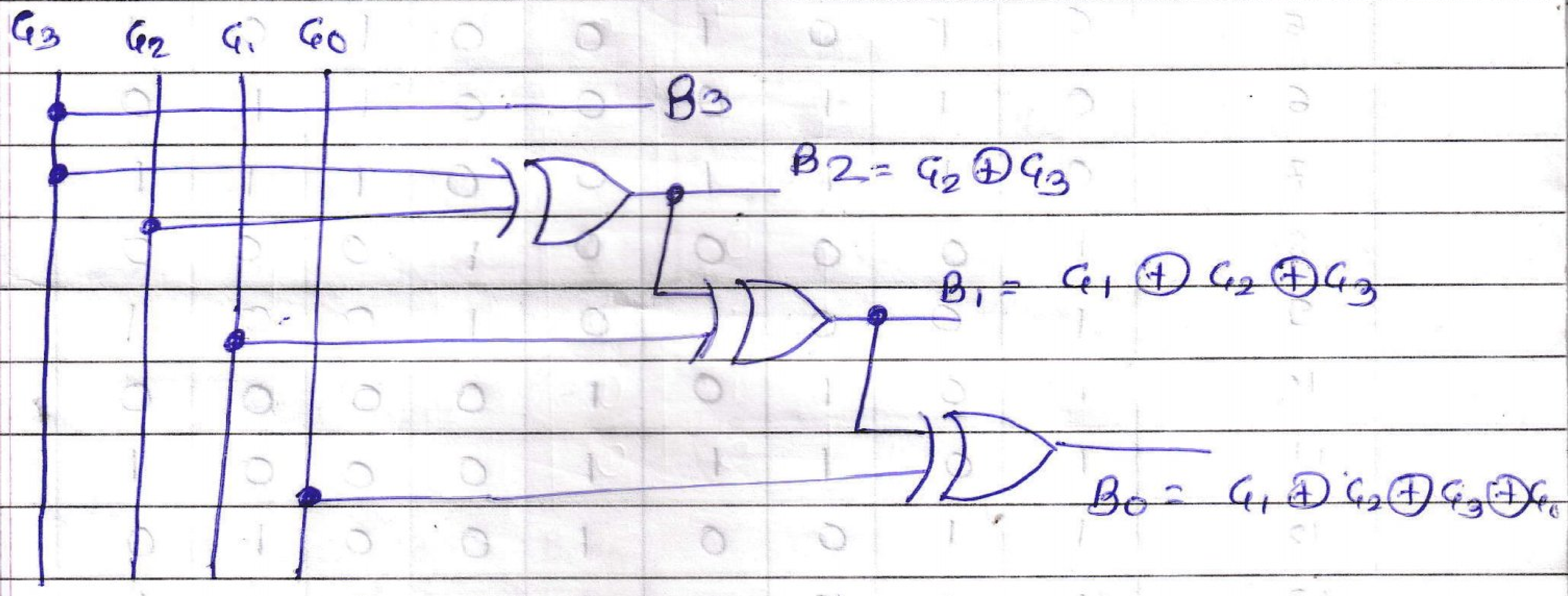
$$= X \overline{Y} + \overline{X} Y$$

where $X = G_1 \oplus G_0$, $Y = \overline{G_3 \oplus G_2}$

$$B_0 = X \oplus Y$$

$$B_0 = G_1 \oplus G_0 \oplus G_3 \oplus G_2$$

$$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$$



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BCD Adder :

- A BCD adder adds two BCD digits and produces a BCD digit. A BCD cannot be greater than 9.
- If sum is less than or equal to 9 and carry=0 then no correction is necessary.
- But if sum is invalid BCD or carry = 1, then the result is wrong and needs correction.
- The wrong result can be corrected by adding six (0110) to it.

Pin 5 - Vcc
12 - GND
IC 7483

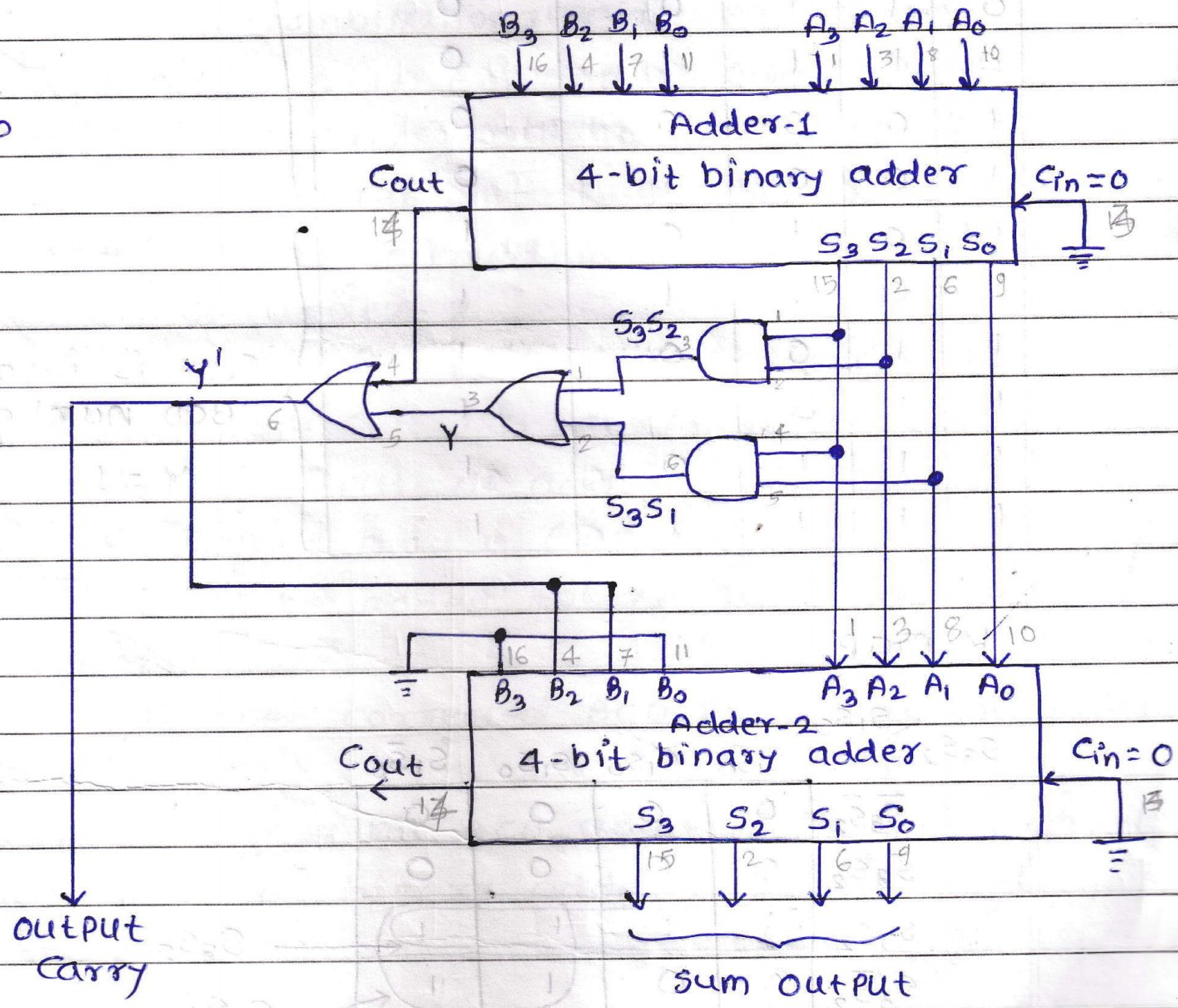


Fig. 3.1

Truth Table for combinational circuit

Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Rows 1–10: sum is valid BCD number $\therefore Y = 0$

Rows 11–16: sum is invalid BCD number $\therefore Y = 1$

K-map

$S_3S_2 \backslash S_1S_0$	$\bar{S}_1\bar{S}_0$	$\bar{S}_1S_0$	S_1S_0	$S_1\bar{S}_0$
$\bar{S}_3\bar{S}_2$	0	0	0	0
$\bar{S}_3S_2$	0	0	0	0
S_3S_2	1	1	1	1
$S_3\bar{S}_2$	0	0	1	1

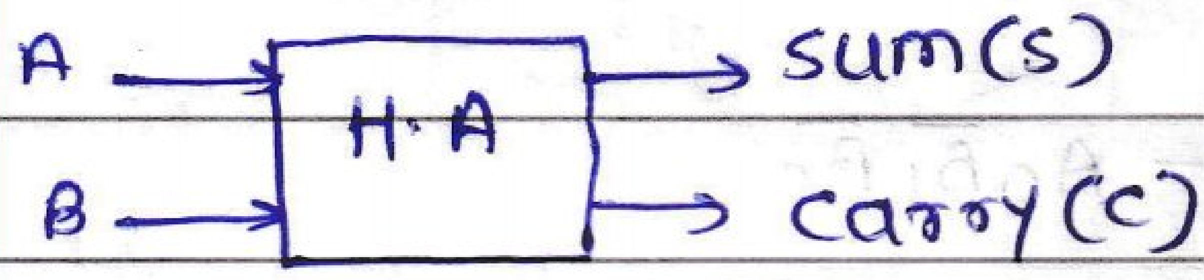
S_3S_2

S_3S_1

$$\boxed{Y = S_3S_2 + S_3S_1}$$

Adder

* Half Adder



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K-map for sum

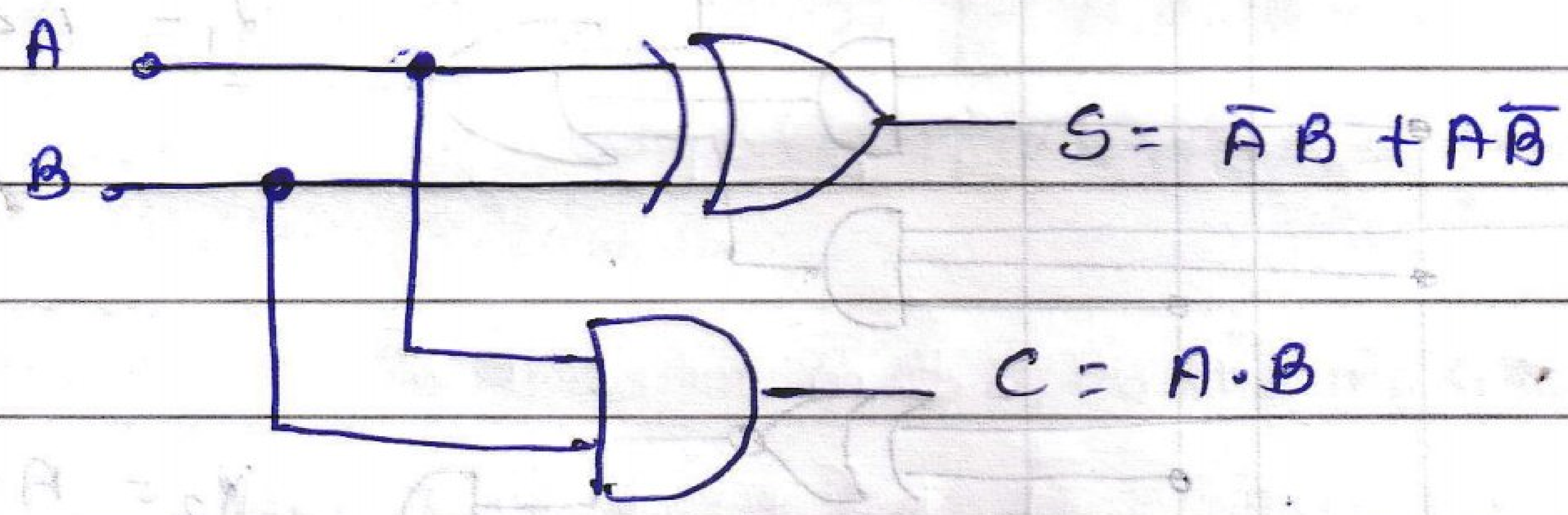
A \ B		
	0	1
	1	0

$S = \bar{A}B + A\bar{B}$

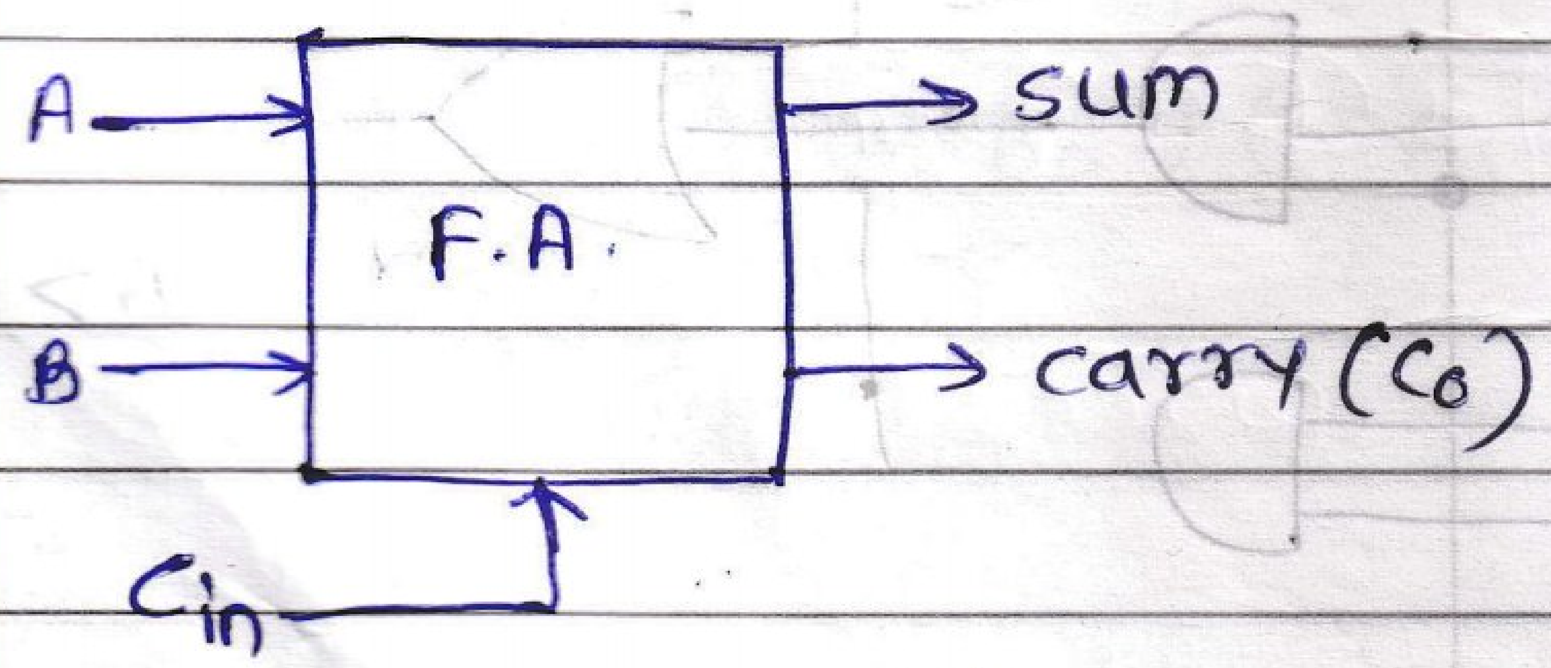
K-map for carry

A \ B		
	0	0
	0	1

$C = AB$



Full Adder



A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for sum

A \ BCin				
	0	1	0	1
	1	0	1	0

$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + ABC_{in} + A\bar{B}\bar{C}_{in}$

$S = C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$

$S = C_{in}(\overline{\bar{A}B + A\bar{B}}) + \bar{C}_{in}(\bar{A}B + A\bar{B})$

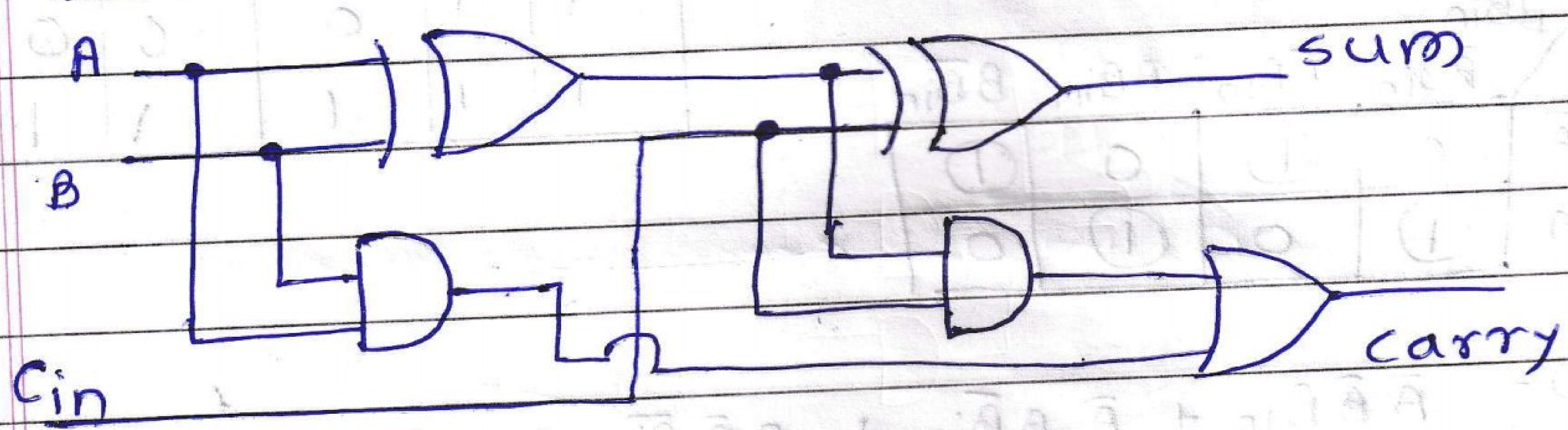
$S = C_{in}\bar{X} + \bar{C}_{in}X$ where $X = A \oplus B$

$S = C_{in} \oplus X$

$\boxed{S = C_{in} \oplus A \oplus B}$

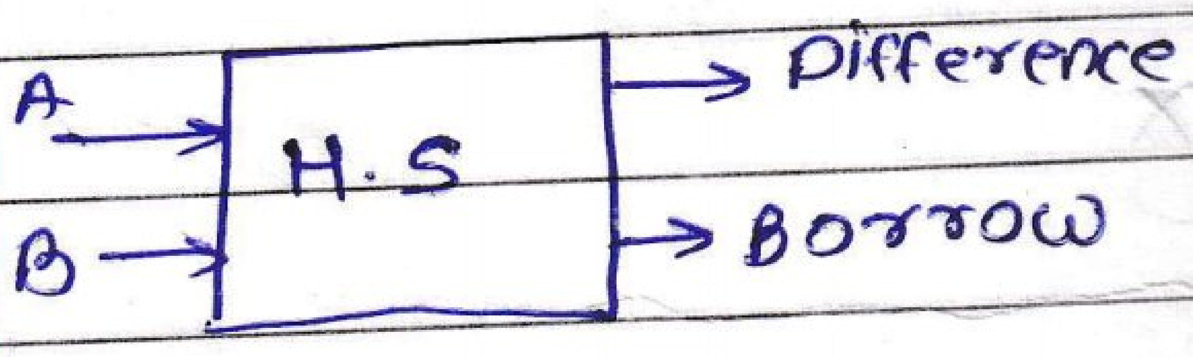
$\boxed{C_0 = AB + AC_{in} + BC_{in}}$

Full Adder using Half Adders



Subtractor

Half subtractor



A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-map for Difference

A \ B	$\bar{B}$	B
$\bar{A}$	0	1
A	1	0

$D = A\bar{B} + \bar{A}B$

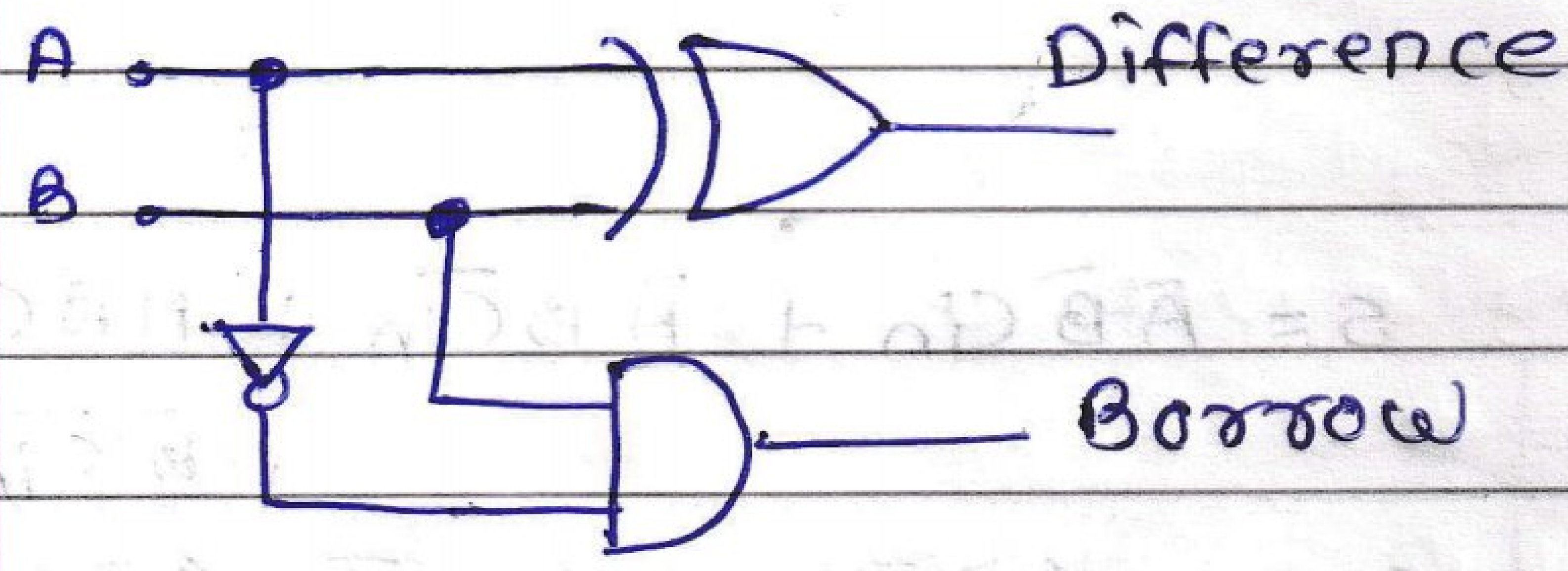
$D = A \oplus B$

K-map for Borrow

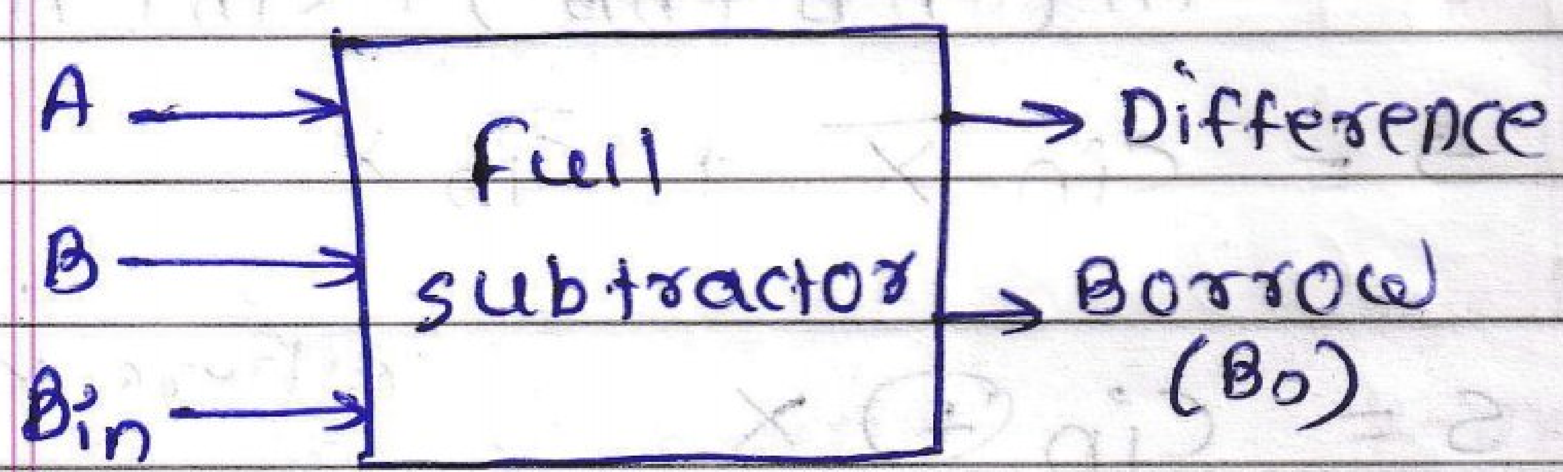
A \ B	$\bar{B}$	B
$\bar{A}$	0	1
A	0	0

$B = \bar{A}B$

15



Full subtractor



A	B	Cin	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

* K-map for Difference

A \ BBin	$\bar{B}\bar{B}_{in}$	$\bar{B}B_{in}$	BB_{in}	$B\bar{B}_{in}$
$\bar{A}$	0	1	0	1
A	1	0	1	0

$$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$$

$$= B_{in}(\bar{A}\bar{B} + AB) + \bar{B}_{in}(\bar{A}B + A\bar{B})$$

$$= B_{in}(\overline{A \oplus B}) + \bar{B}_{in}(A \oplus B)$$

put $A \oplus B = X$

$$D = B_{in}\bar{X} + \bar{B}_{in}X$$

$$\boxed{D = B_{in} \oplus A \oplus B}$$

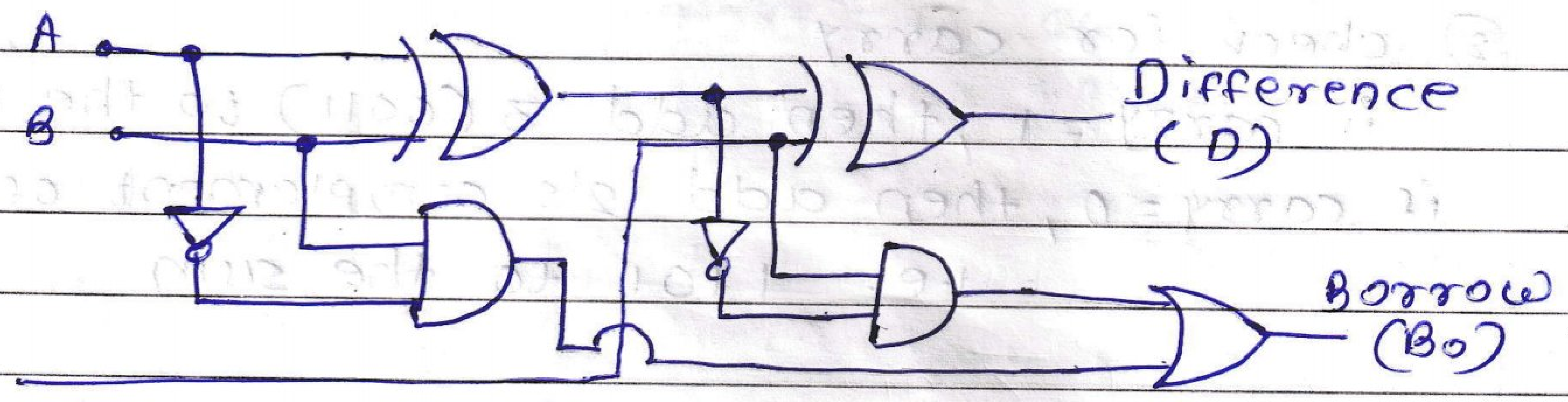
K-map for Borrow

A \ BBin	$\bar{B}\bar{B}_{in}$	$\bar{B}B_{in}$	BB_{in}	$B\bar{B}_{in}$
$\bar{A}$	0	1	1	1
A	0	0	1	0

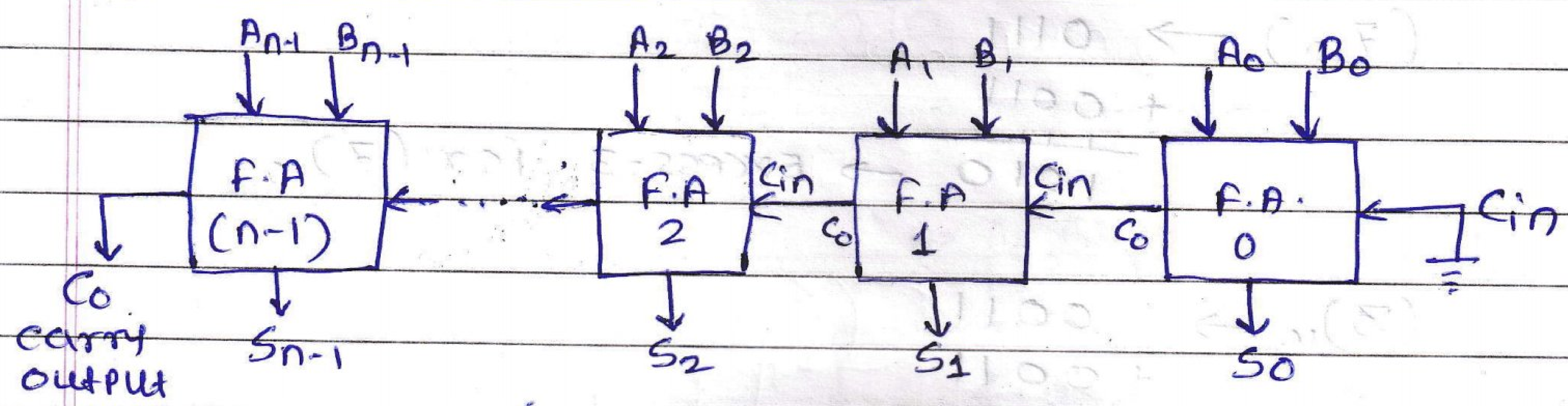
$$B_0 = \bar{A}B_{in} + \bar{A}B + BB_{in}$$

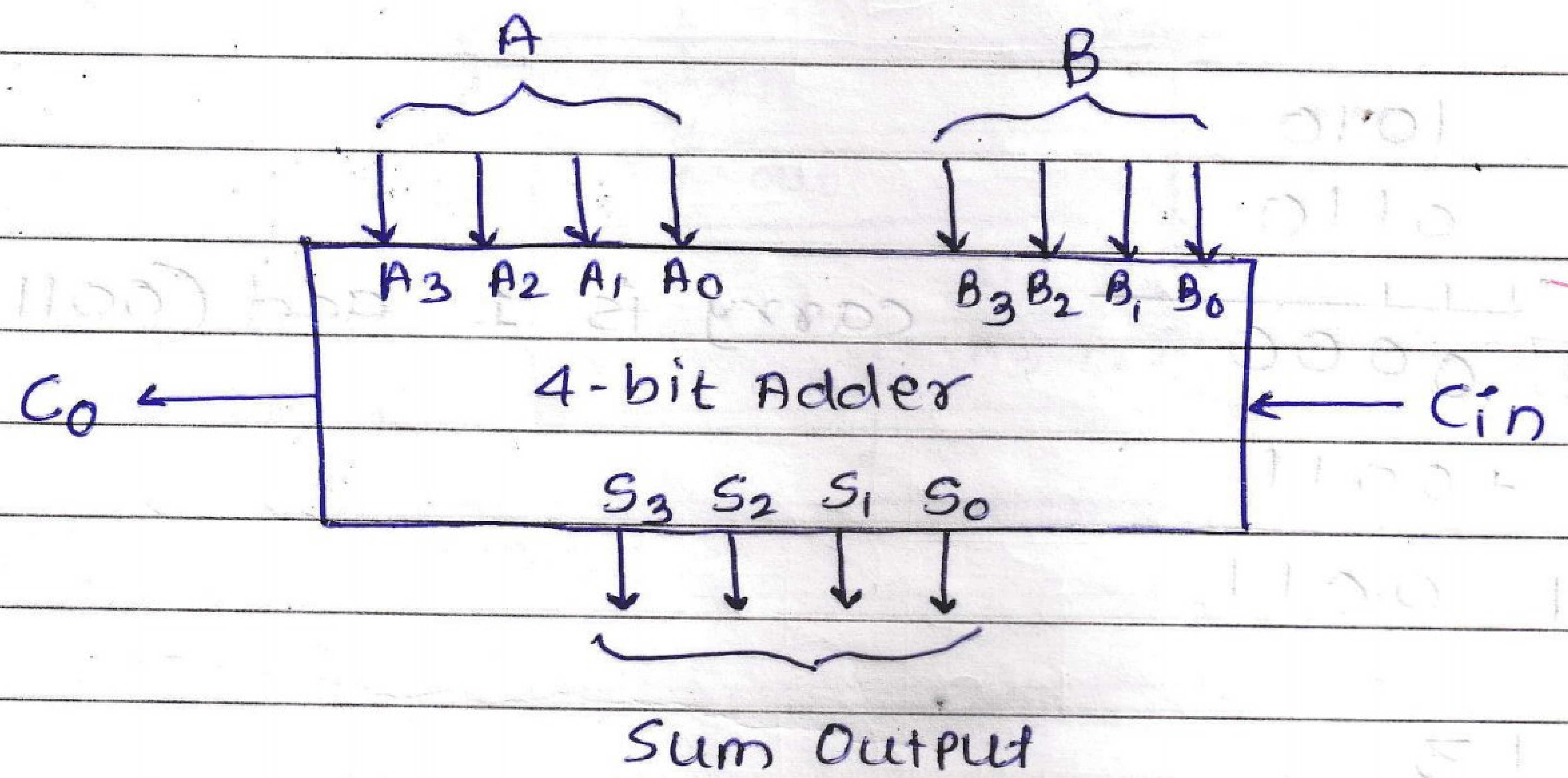
$$\boxed{B_0 = \bar{A}B + \bar{A}B_{in} + BB_{in}}$$

Full subtractor using Half subtractor



The n-bit parallel Adder

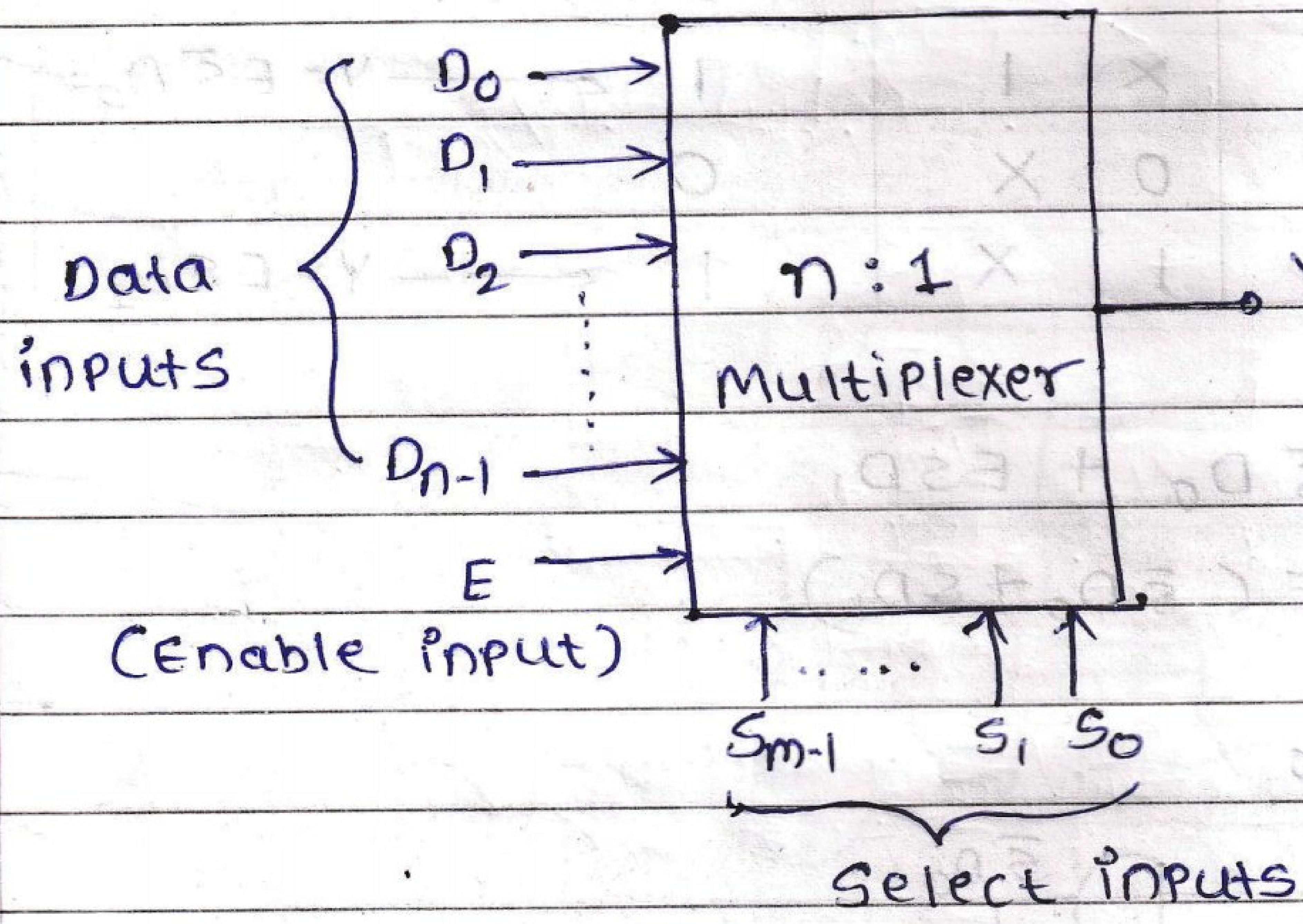




Multiplexer, Demultiplexer, ALU, Encoder & Decoder,
Sequential Circuits: Flip Flop

Multiplexer:

A multiplexer is a digital circuit which selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select inputs. $(n = 2^m)$



Types of multiplexer

1. 2:1 multiplexer
2. 4:1 multiplexer
3. 8:1 multiplexer
4. 16:1 multiplexer

1) 2:1 Multiplexer

It has two data inputs D_0 and D_1, one select input S, an enable input and one output.

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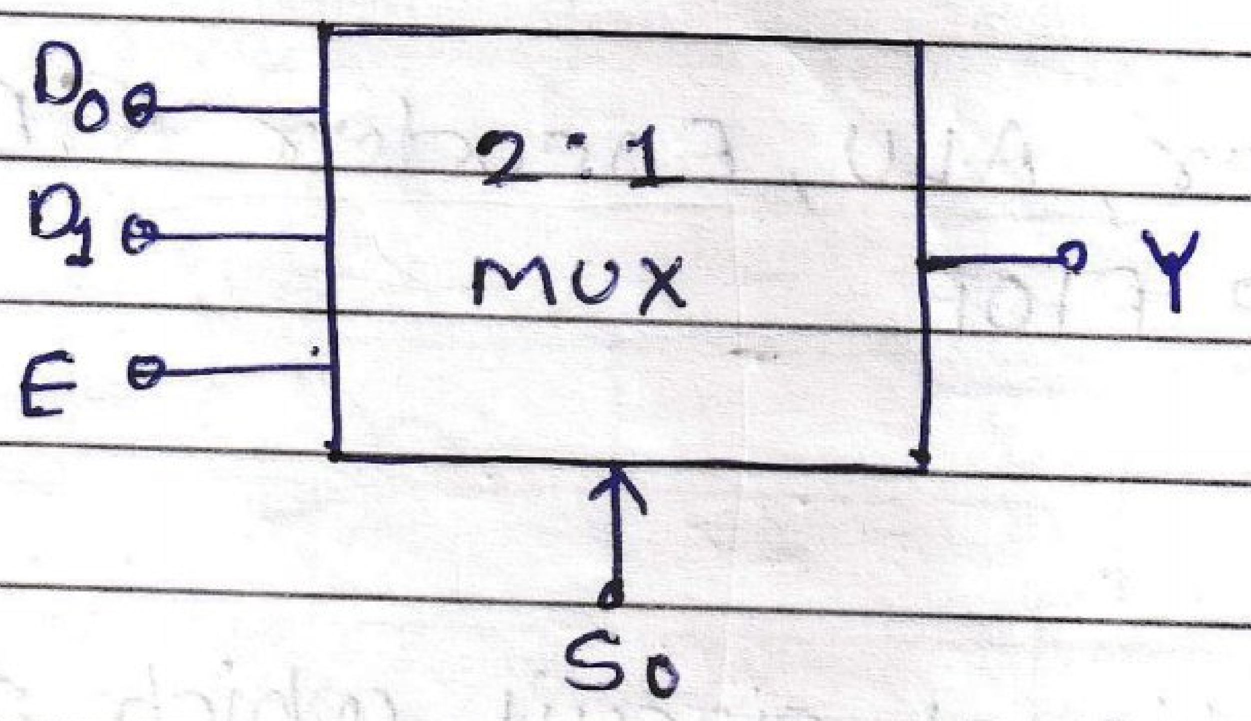
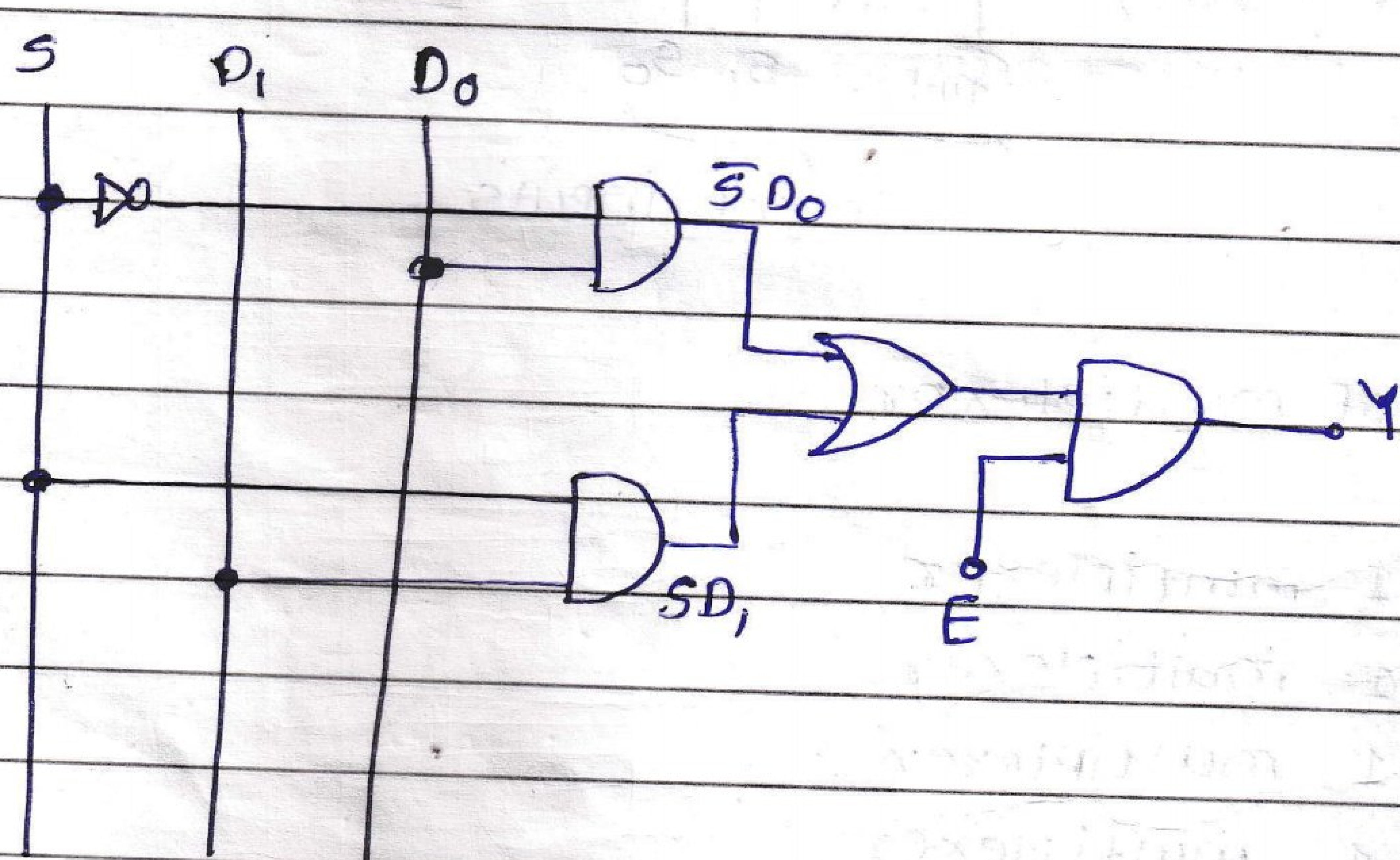


Enable	Select i/p S
0	X
1	0
1	1

Enable E	Select S	D_1	D_0	Output Y	
0	X	X	X	0	
1	0	X	0	0	
1	0	X	1	1	← $Y = E\bar{S}D_0$
1	1	0	X	0	
1	1	1	X	1	← $Y = ESD_1$

$$Y = E\bar{S}D_0 + ESD_1$$
$$= E(\bar{S}D_0 + SD_1)$$



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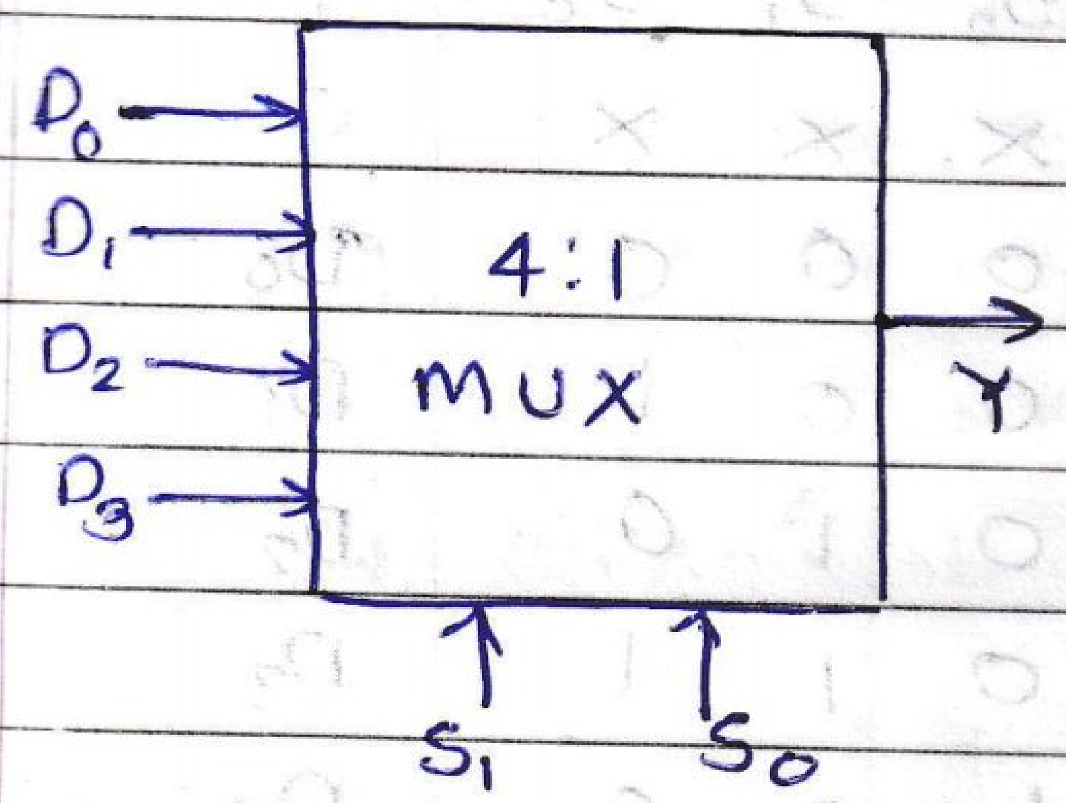
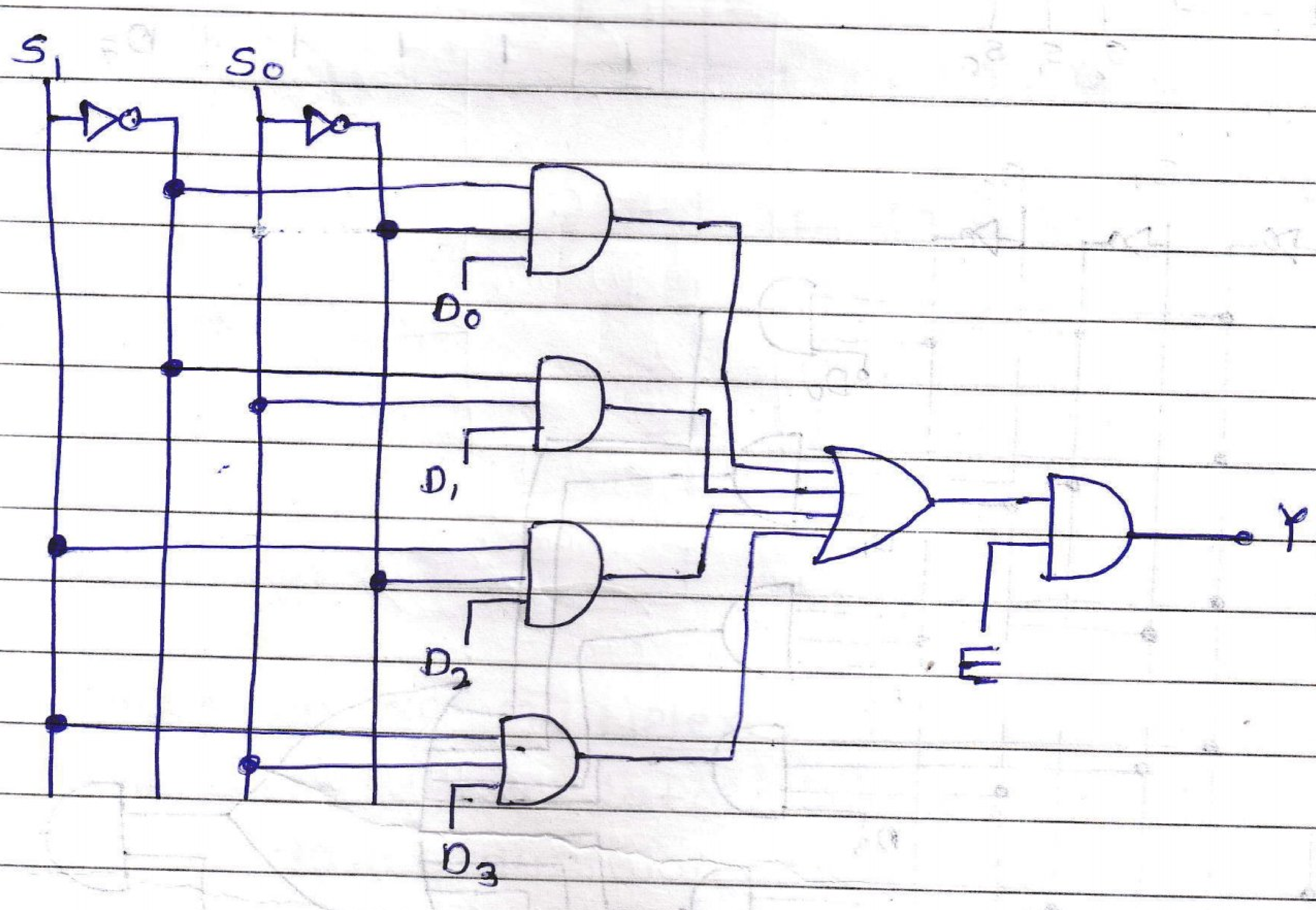
2) 4:1 multiplexer



Select inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$Y = E(\bar{S}_1\bar{S}_0D_0 + \bar{S}_1S_0D_1 + S_1\bar{S}_0D_2 + S_1S_0D_3)$$



Note that $n = 4$ (inputs) hence number of select lines i.e $m = 2$ so that $2^m = n$.

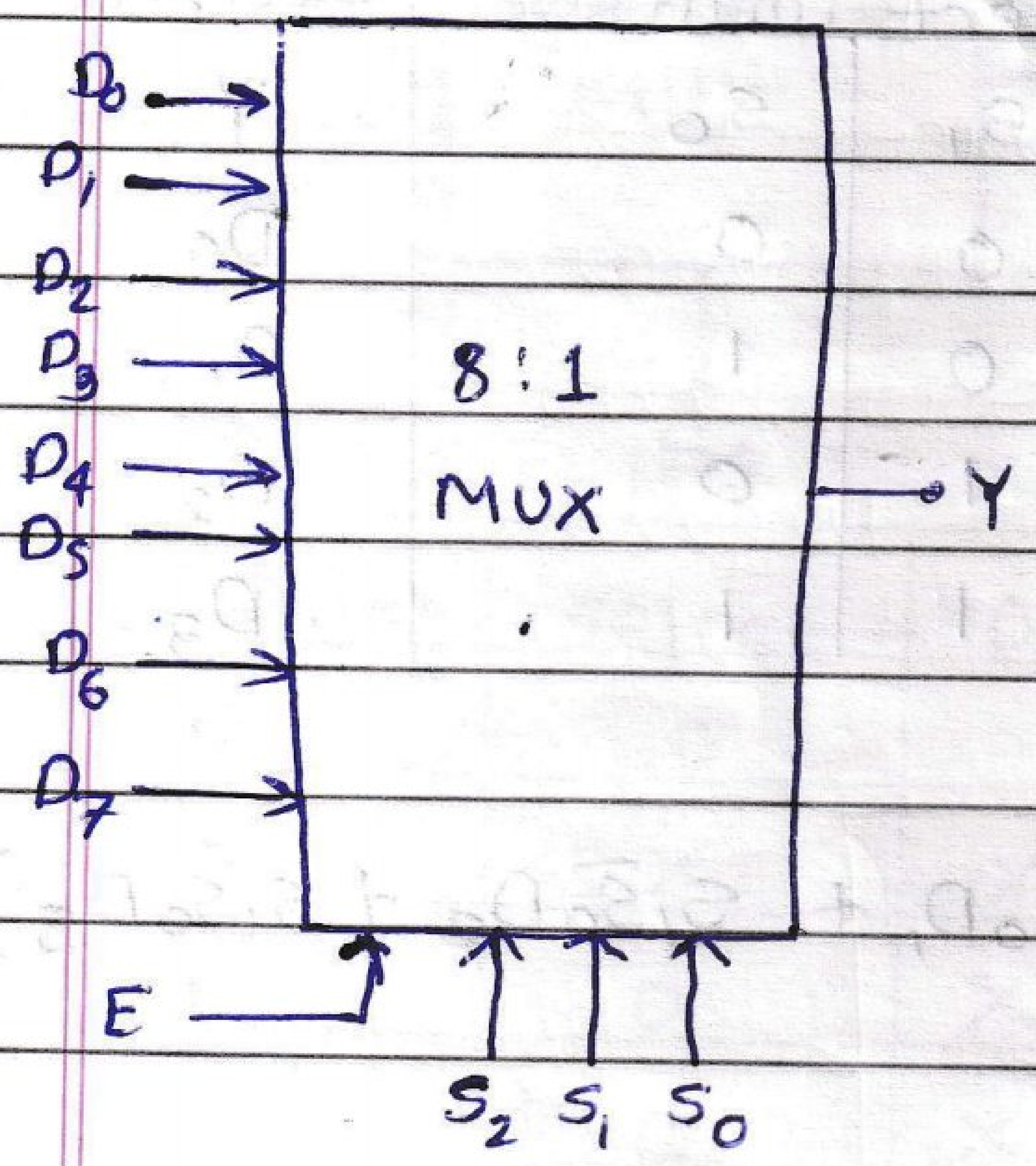
$Y = D_0$ when $S_1S_0 = 00$

$Y = D_1$ when $S_1S_0 = 01$

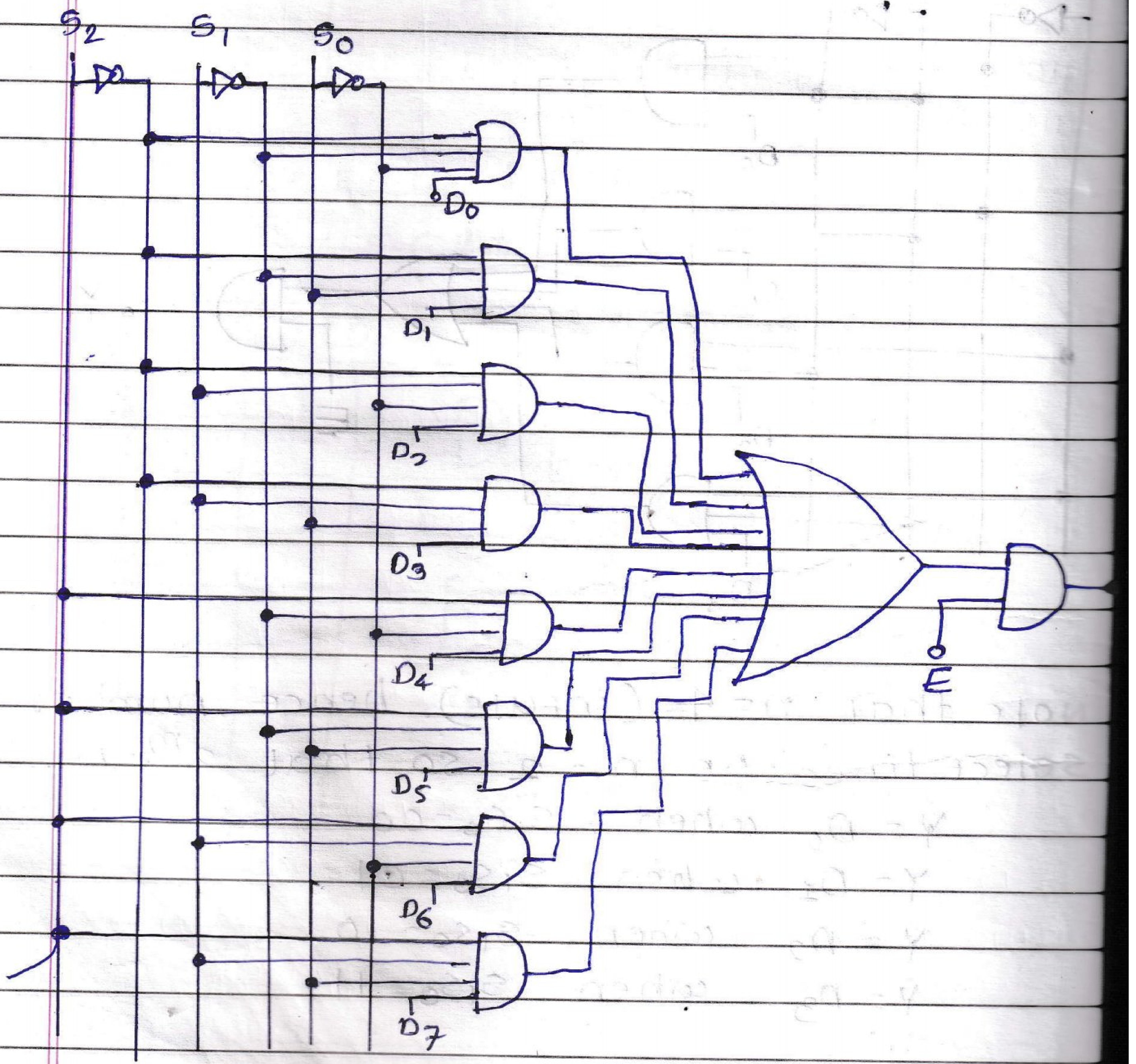
$Y = D_2$ when $S_1S_0 = 10$

$Y = D_3$ when $S_1S_0 = 11$

3) 8:1 Multiplexer: It has 8 data inputs, 1 output and 3 select inputs



E	S_2	S_1	S_0	Y
0	X	X	X	0
1	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7



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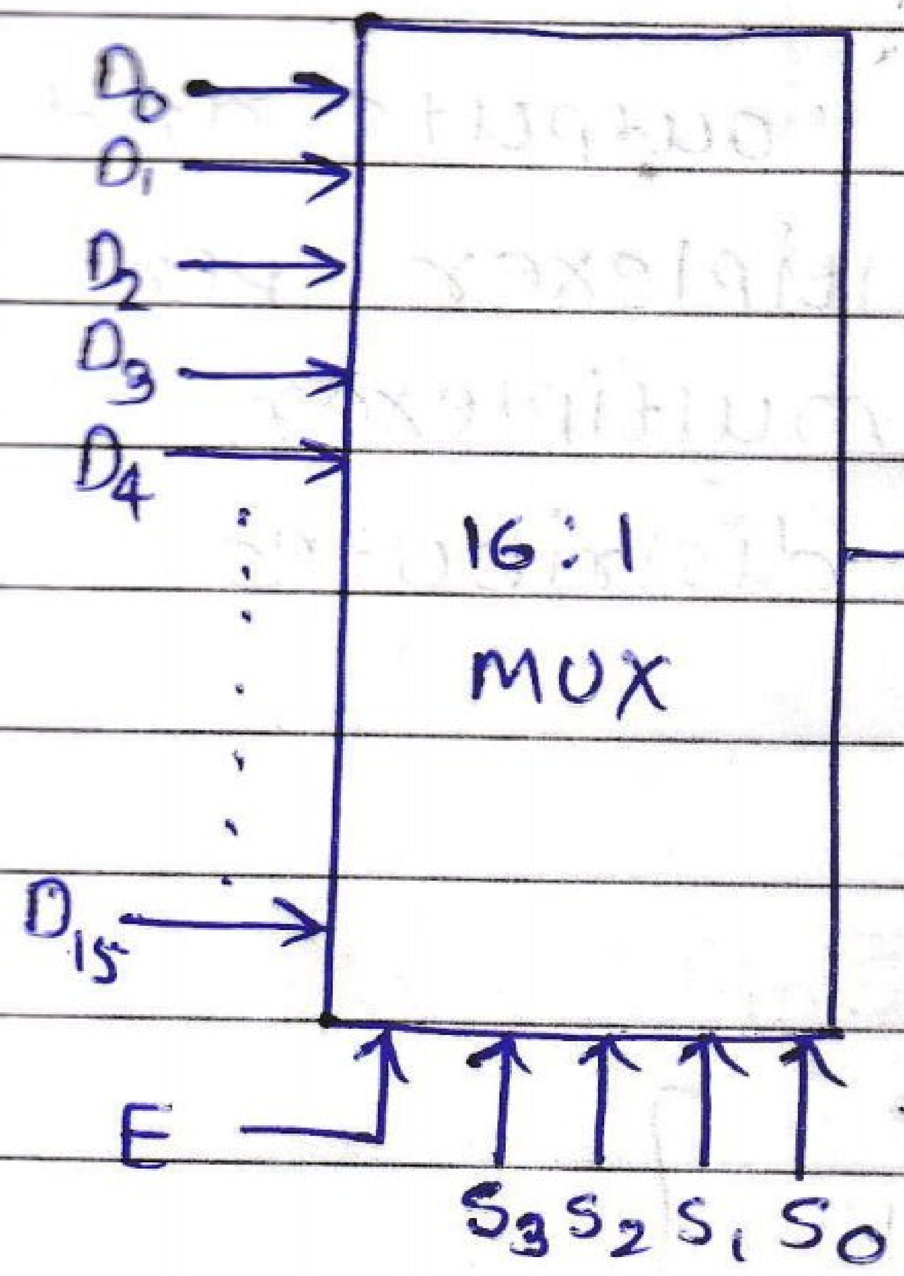
4) 16:1 MUX



E	S_3	S_2	S_1	S_0	Y
0	X	X	X	X	0
1	0	0	0	0	D_0
1	0	0	0	1	D_1
1	0	0	1	0	D_2
1	0	0	1	1	D_3
1	0	1	0	0	D_4
1	0	1	0	1	D_5
1	0	1	1	0	D_6
1	0	1	1	1	D_7
1	1	0	0	0	D_8
1	1	0	0	1	D_9
1	1	0	1	0	D_{10}
1	1	0	1	1	D_{11}
1	1	1	0	0	D_{12}
1	1	1	0	1	D_{13}
1	1	1	1	0	D_{14}
1	1	1	1	1	D_{15}

Applications of Multiplexer

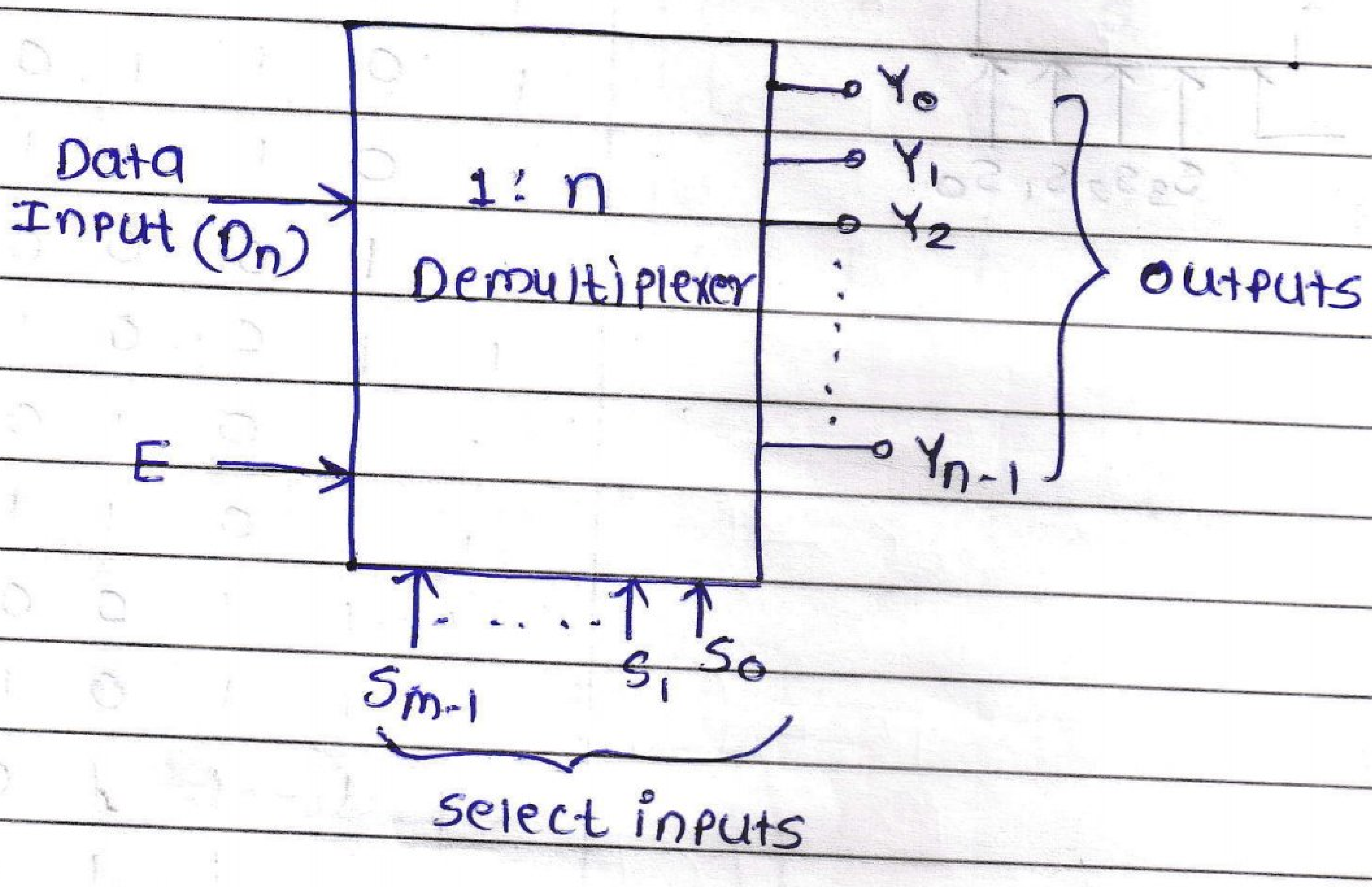
- It is used as a data selector
- In the data aquisition system
- It is used for simplification of logic design
- In designing the combinational circuits
- In D/A (Digital to Analog) converter

① Realize the logic function $Y = \Sigma m(1,3,4,6)$ using a multiplexer.

② Realize ~~the~~ / Implement a full adder using 8:1 multiplexer

Demultiplexer

It has only one input, "n" outputs and "m" select inputs. A demultiplexer performs the reverse operation of a multiplexer. It receives one input and distributes it over several outputs.

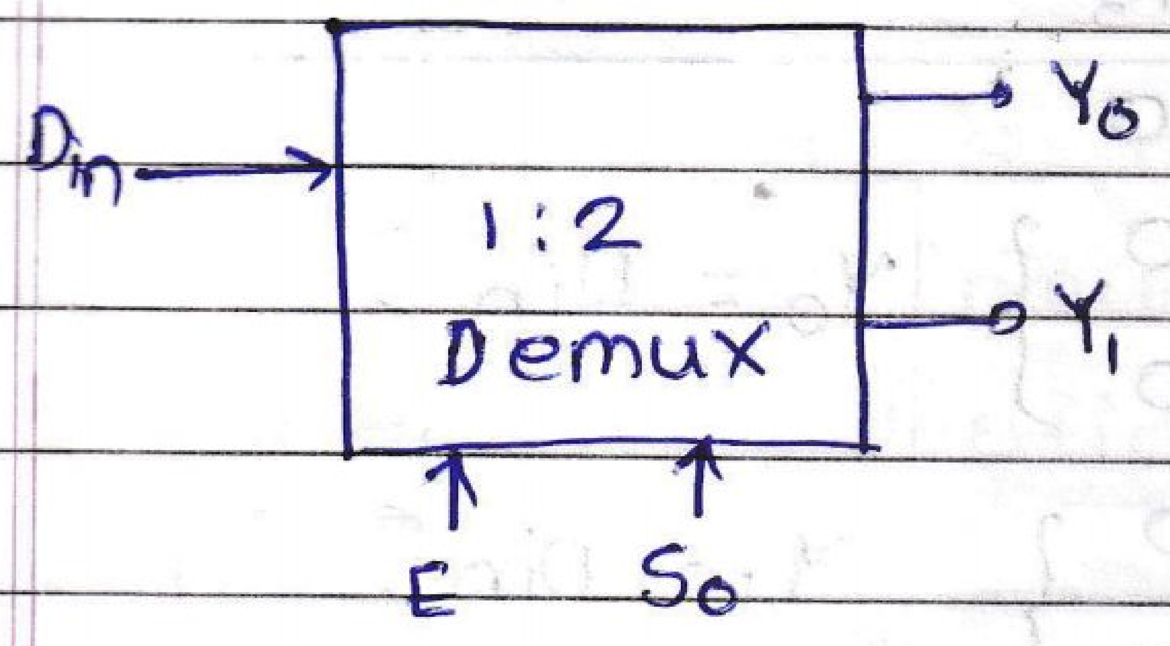


Types of Demultiplexer

1. 1:2 Demultiplexer
2. 1:4 Demultiplexer
3. 1:8 Demultiplexer
4. 1:16 Demultiplexer

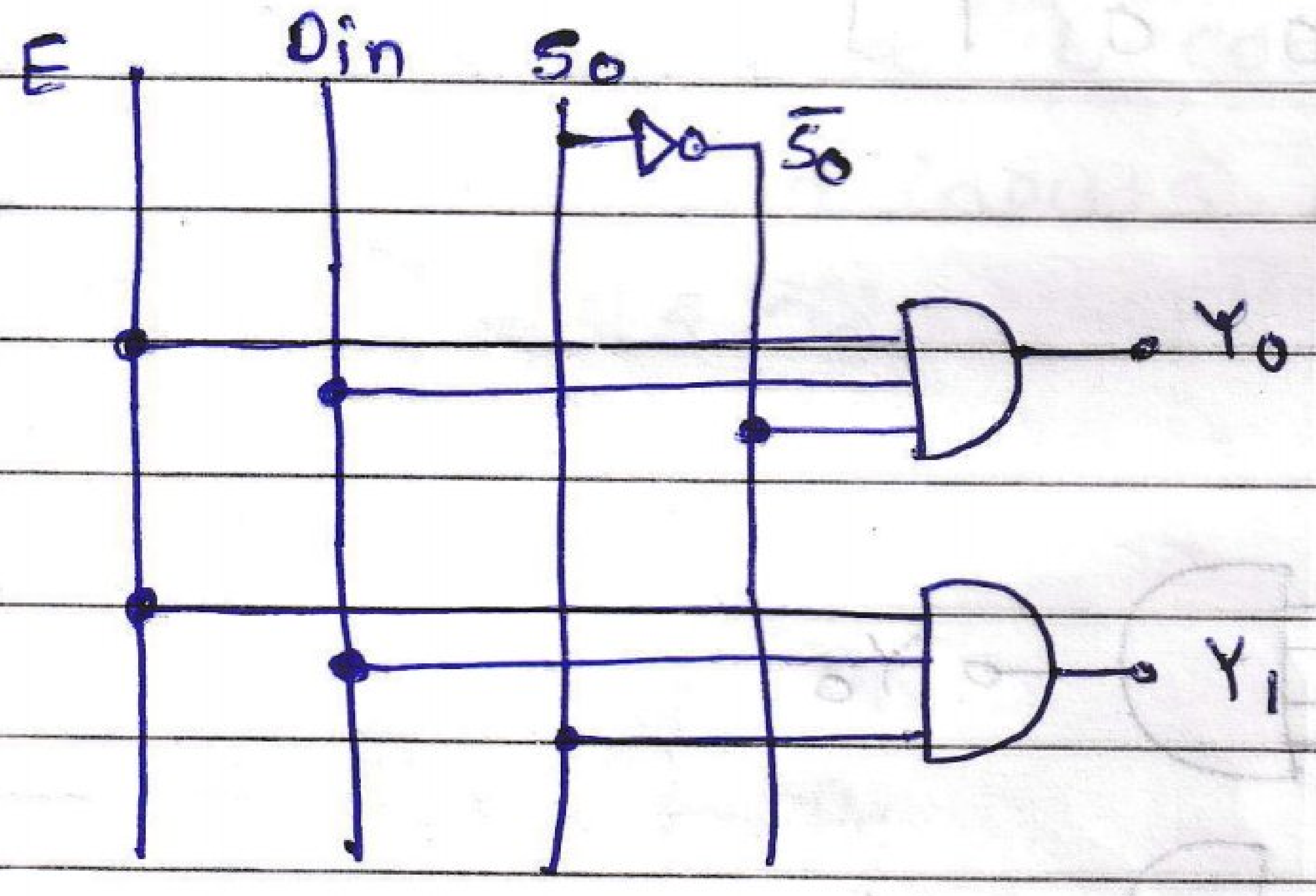
1) 1:2 Demultiplexer

It has one data input D_{in}, 1 select input S_0, 1 enable input and two outputs Y_0 and Y_1.



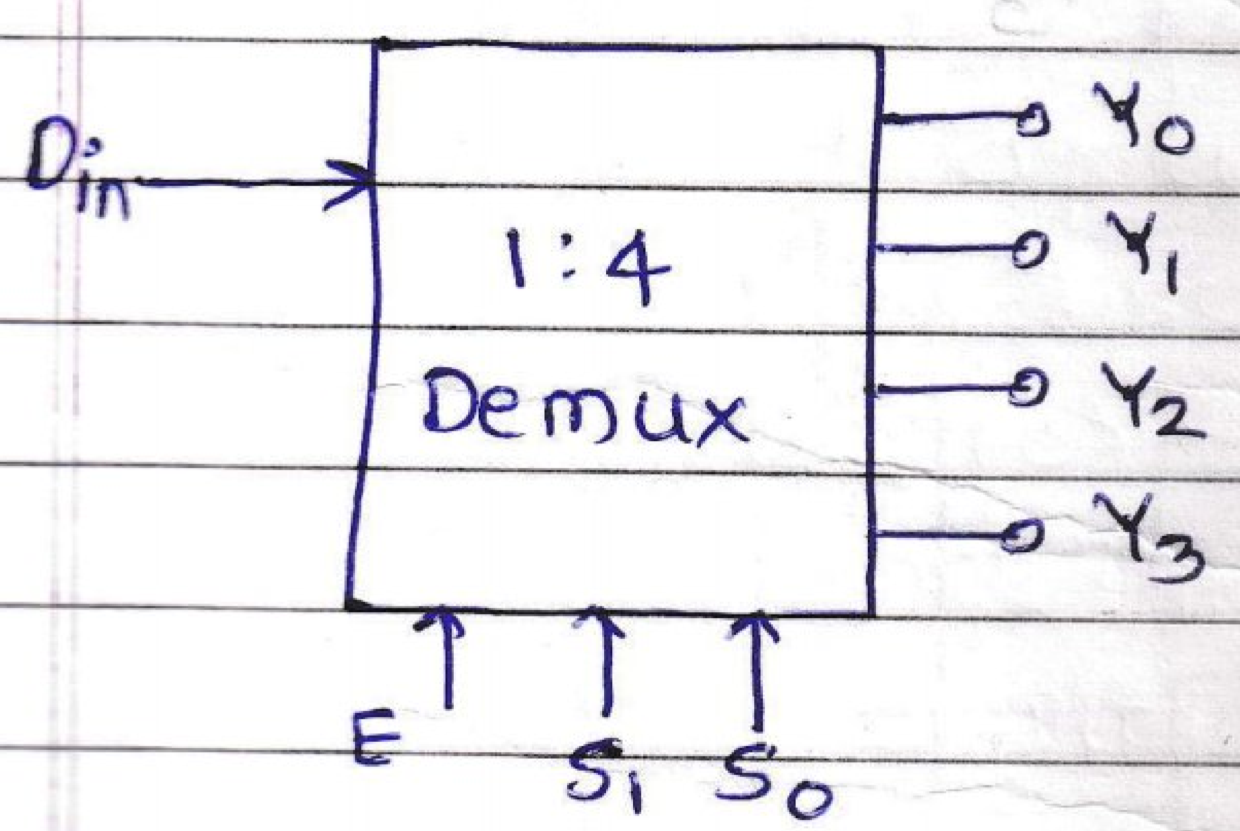
E	Din	S_0	Y_1	Y_0	
0	X	X	0	0	
1	0	0	0	0	$Y_0 = D_{in}$
1	1	0	0	1	
1	0	1	0	0	$Y_1 = D_{in}$
1	1	1	1	0	

$Y_0 = E D_{in} \overline{S_0}$ and $Y_1 = E D_{in} S_0$



2) 1:4 Demultiplexer

It has 1 data input and 4 outputs Y_0, Y_1, Y_2 & Y_3



Din is connected to Y_0 when $S_1S_0 = 00$
It is connected to Y_1 when $S_1S_0 = 01$
It is connected to Y_2 when $S_1S_0 = 10$
It is connected to Y_3 when $S_1S_0 = 11$

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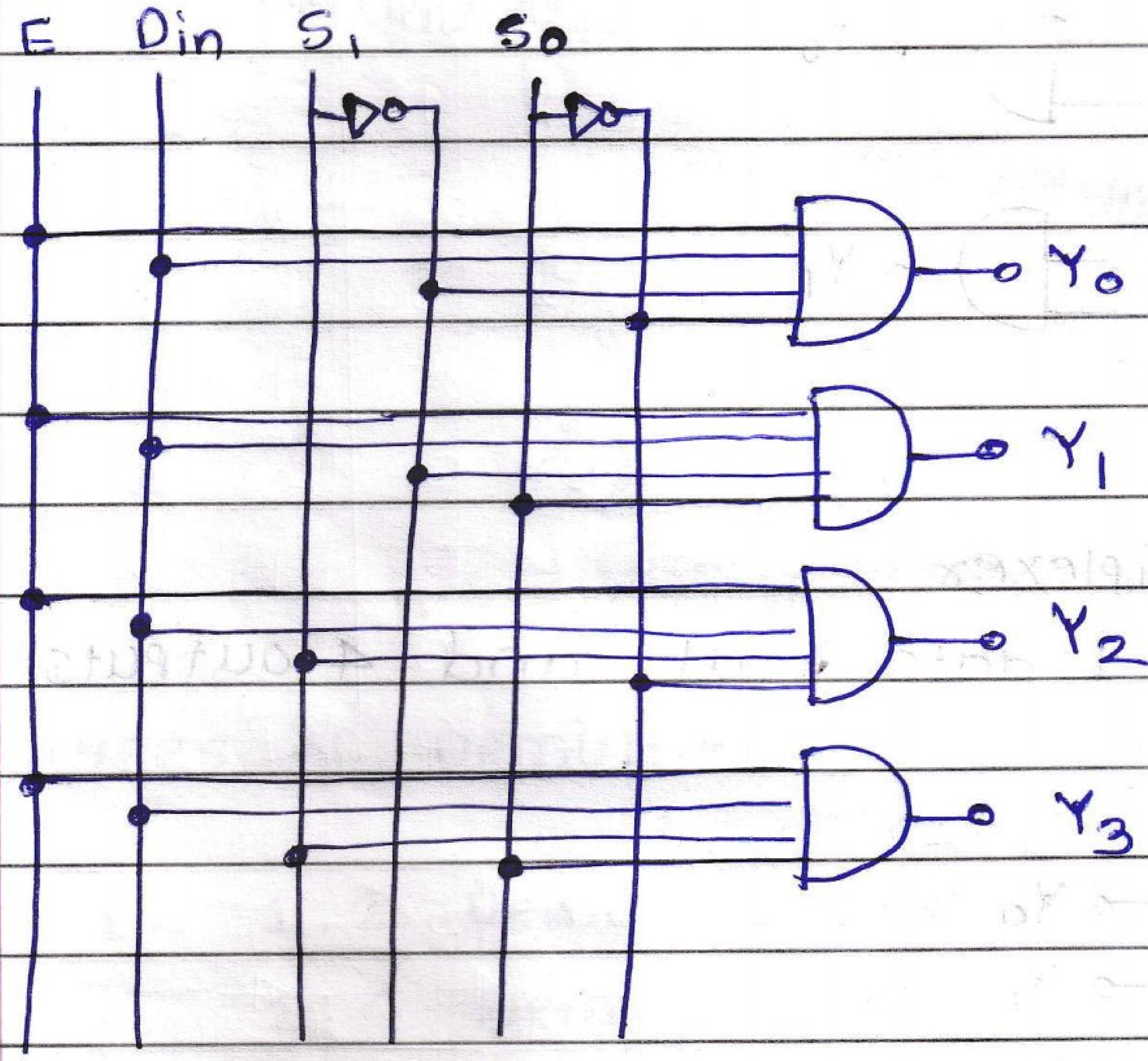
E	Din	S_1	S_0	Y_0	Y_1	Y_2	Y_3	
0	x	x	x	0	0	0	0	
1	0	0	0	0	0	0	0	$Y_0 = Din$
1	1	0	0	1	0	0	0	
1	0	0	1	0	0	0	0	$Y_1 = Din$
1	1	0	1	0	1	0	0	
1	0	1	0	0	0	0	0	$Y_2 = Din$
1	1	1	0	0	0	1	0	
1	0	1	1	0	0	0	0	$Y_3 = Din$
1	1	1	1	0	0	0	1	



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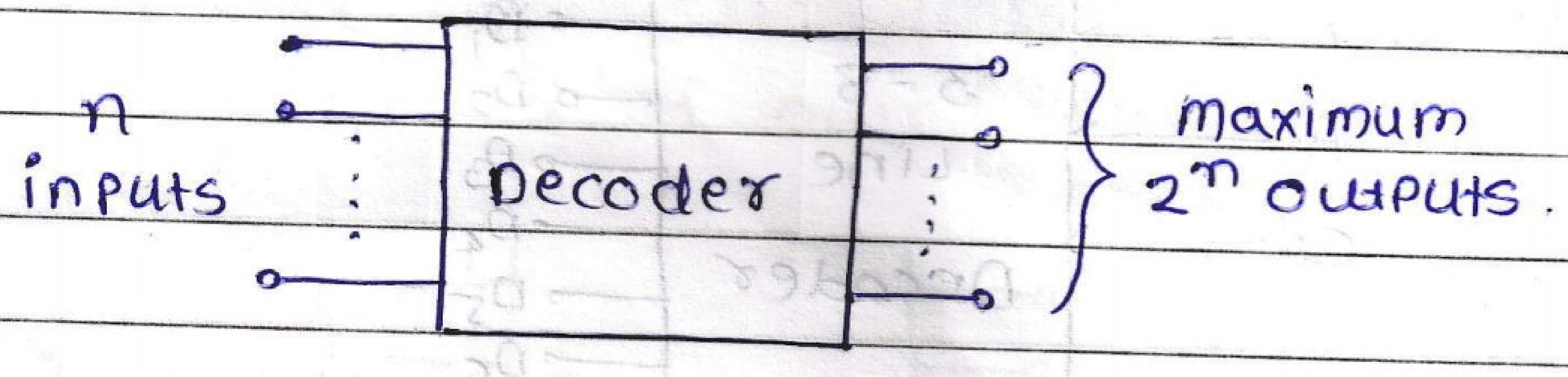
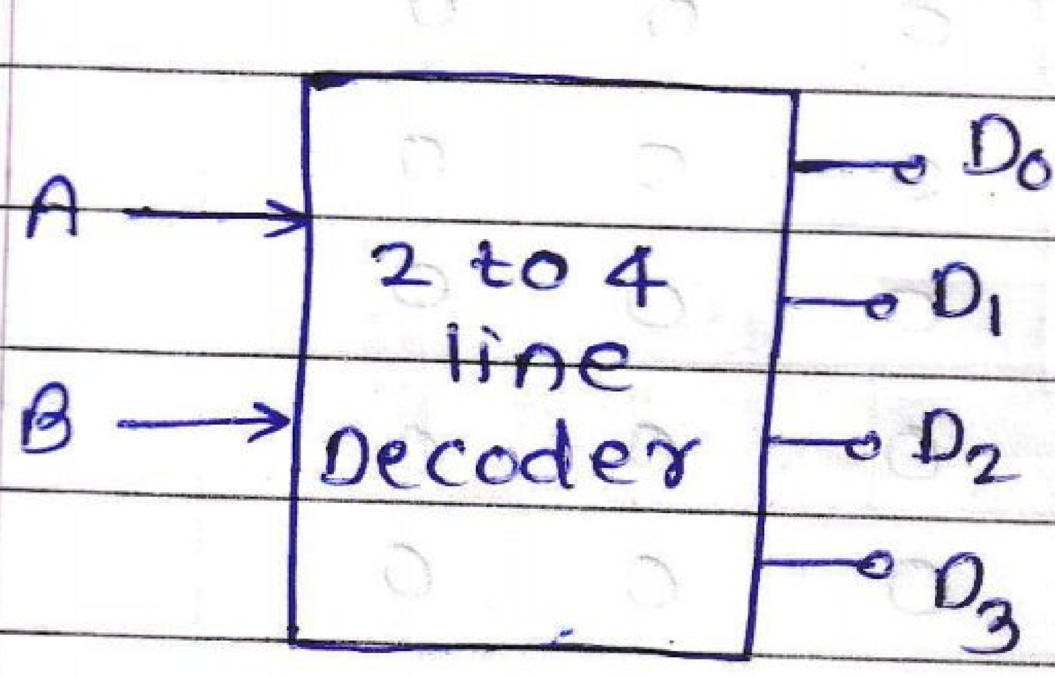
Decoder

A decoder is a combinational circuit. It has 'n' inputs and to a maximum 2^n outputs. Decoder is identical to a demultiplexer.



1) 2 to 4 Line Decoder

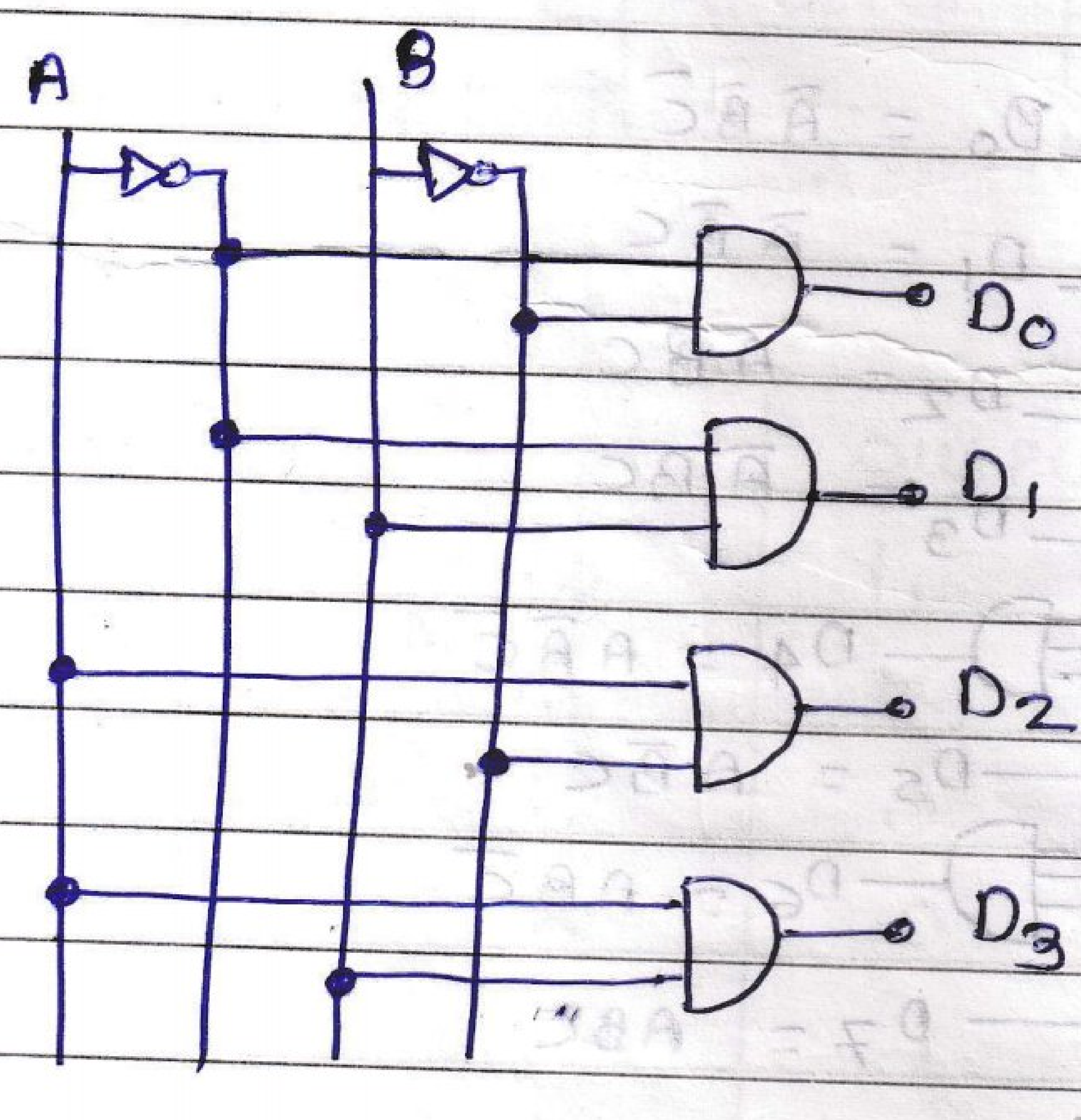
It has two inputs A & B and four outputs D_0, D_1, D_2 & D_3.



Inputs		Outputs			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$D_0 = \bar{A}\bar{B}$, $D_1 = \bar{A}B$,

$D_2 = A\bar{B}$, $D_3 = AB$

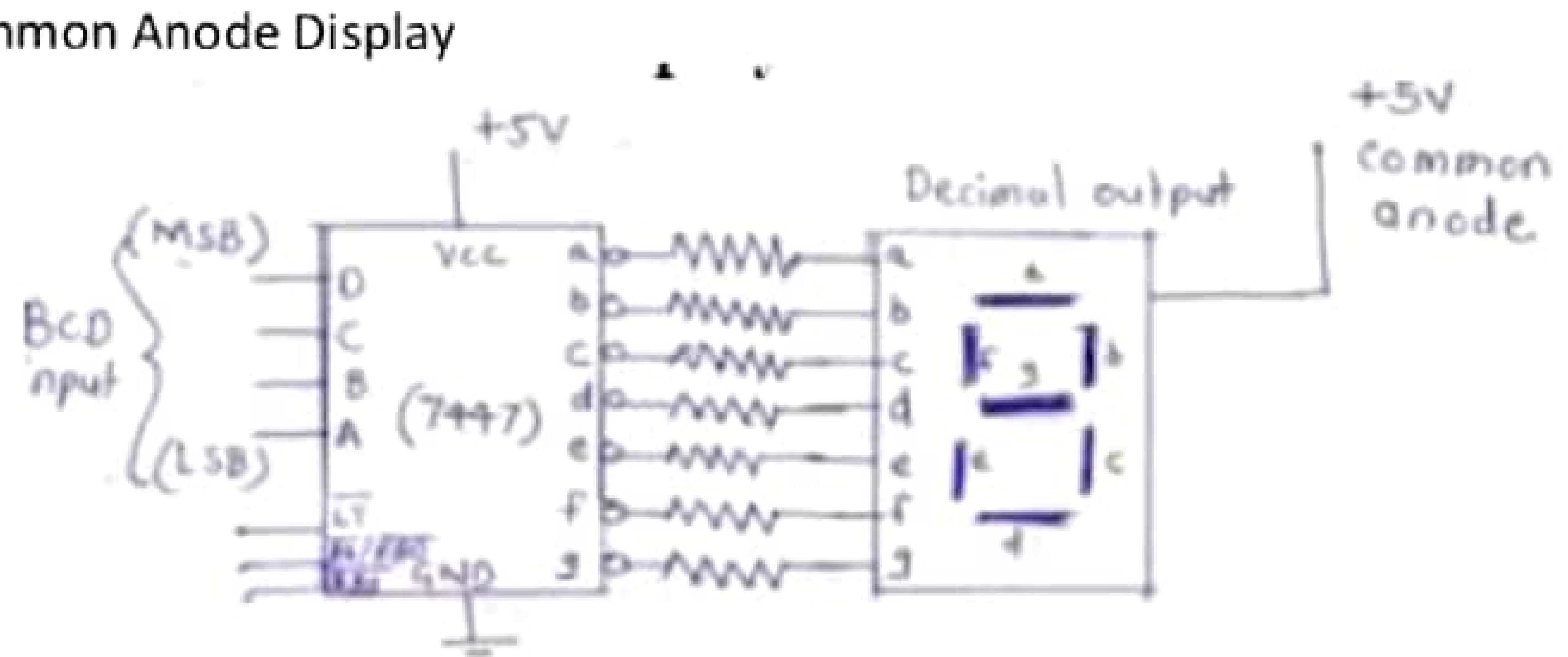


Q. N.		Scheme
	Attempt any TWO of the following:	12- Total Marks
a)	Design BCD to seven segment decoder using IC 7447 with its truth table.	6M

Ans: **Note: Any one type of display shall be considered**

1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode Display :

Common Anode Display



For normal functioning LT, BI/RBO & RBI should be connected to logic 1

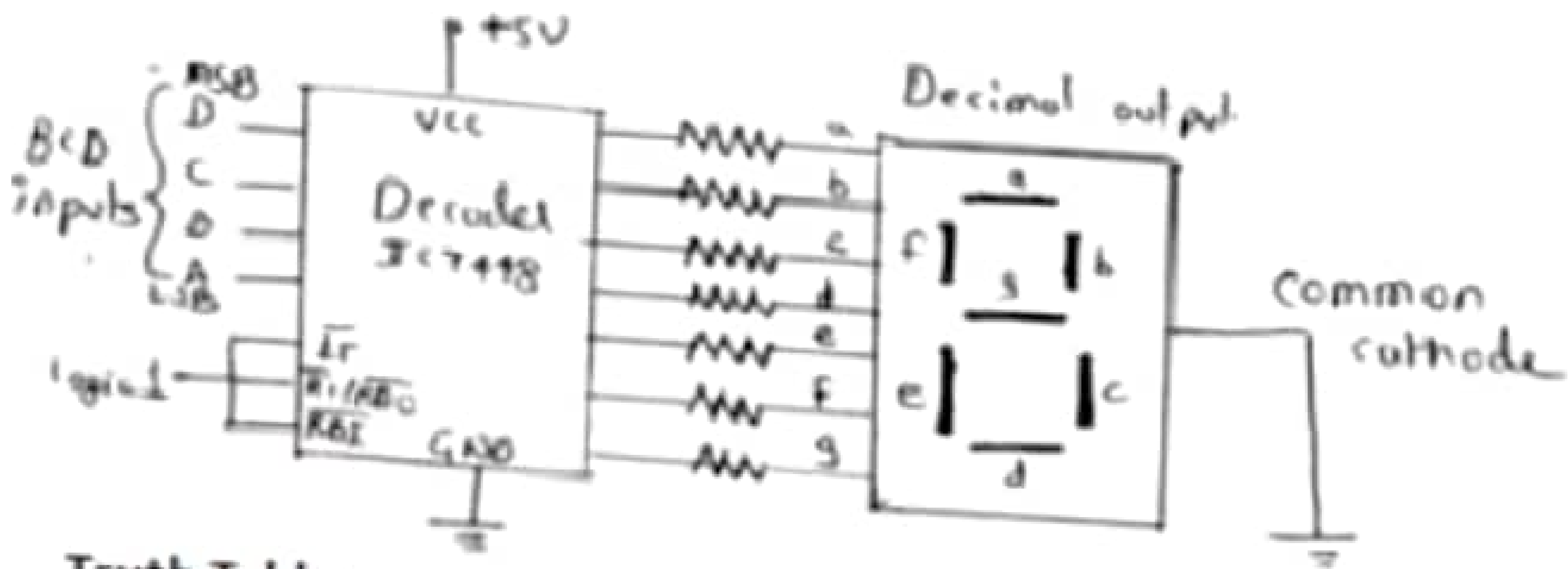
Truth Table

For seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

Explanation 2M
Circuit Diagram 2M
Truth Table 2M

Common Cathode Display:



Truth Table

BCD inputs				7 segment coded outputs							Display outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

b)	**Describe the working of 4 bit universal shift register.**	**6M**
Ans:		