

Unit III: Combinational Logic Circuits
(Weightage - 18 marks)

Combinational logic circuit

- * It is a digital circuit made up of combination of different logic gates in which output depends only on present inputs.
- * In combinational logic circuit, memory element and clock signal is not required.

Standard Boolean representation

Any Boolean expression is represented by two formats -

→ Sum of Product (SOP)

→ Product of Sum (POS)

Sum of Product (SOP)

* SOP expression consist of two or more AND terms (product) that are OR together.

* In SOP an inversion cannot cover more than one variable in term.

Example

$$ABC + \bar{A}BC$$

$$AB + A\bar{B} + A\bar{B}$$

$$ABC + \bar{A}\bar{B}C$$

$$AB + A\bar{B}\bar{C} + C\bar{D} + \bar{C}$$

ABC	2	no. of variable Her 2 2
AB		
A B		
A B		
A B		

Product of Sum (POS)

POS expression consist of two or more OR terms (sum) that are ANDed together.

Example

$$Y = (A + \bar{B} + C)(A + C)$$

$$Y = (A + \bar{B})(\bar{C} + D) F$$

$$Y = (A + \bar{B}) \cdot (B + C)$$

$$Y = (\bar{B} + \bar{C} + D)(B + C + E)$$

$$Y = (A + \bar{C})(B + E)(C + D)$$

Standard / Canonical forms (SOP)

Min term

- Product (AND function)
- Contains all variables.
- Evaluates to '1' for a specific combination.

Example

$$\begin{array}{l}
 A=0 \quad \bar{A} \quad \bar{B} \quad \bar{C} \\
 B=0 \quad (\bar{0}) \quad (\bar{0}) \quad (\bar{0}) \\
 C=0 \quad + \quad + \quad + \\
 \quad \quad \quad | \cdot | \cdot | = 1
 \end{array}$$

	A	B	C	Min term
0	0	0	0	m ₀ A'B'C'
1	0	0	1	m ₁ A'B'C
2	0	1	0	m ₂ A'B'C'
3	0	1	1	m ₃ A'B'C
4	1	0	0	m ₄ A'B'C'
5	1	0	1	m ₅ A'B'C
6	1	1	0	m ₆ A'B'C'
7	1	1	1	m ₇ A'B'C

Maxterms

- Sum (OR function)
- Contains all variables
- Evaluates to '0' for a specific combination.

Example

$$\begin{array}{l}
 A=1 \quad \bar{A} \quad \bar{B} \quad \bar{C} \\
 B=1 \quad 1 + \bar{1} + \bar{1} = 0 \\
 C=1 \quad 0 \quad 0 \quad 0
 \end{array}$$

	A	B	C	Maxterm
0	0	0	0	m ₀ A'B'C
1	0	0	1	m ₁ A'B'C'
2	0	1	0	m ₂ A'B'C
3	0	1	1	m ₃ A'B'C'
4	1	0	0	m ₄ A'B'C
5	1	0	1	m ₅ A'B'C'
6	1	1	0	m ₆ A'B'C
7	1	1	1	m ₇ A'B'C

(Q) Convert the following expression into canonical SOP form.

$$\begin{aligned}
 & A + B\bar{C}\bar{D} \\
 & \text{if Identify missing variable in each term.} \\
 & = \bar{A}(\bar{B}+\bar{B})(\bar{C}+\bar{C})(\bar{D}+\bar{D}) + (\bar{A}+\bar{A}) B\bar{C}\bar{D} \\
 & = (\bar{A}B+\bar{A}\bar{B})(\bar{C}+\bar{C})(\bar{D}+\bar{D}) + (A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}) \\
 & = \bar{A}B\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} (\bar{D}+\bar{D}) + (\bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}) \\
 & = \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} \\
 & = \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} \\
 & + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} \\
 & - \text{Any}
 \end{aligned}$$

$$A\bar{B}C + B\bar{D}$$

Identify the missing variables in each term.

$$A\bar{B}C(D+\bar{D}) + B\bar{D}(A+\bar{A})(C+\bar{C})$$

$$A\bar{B}CD + A\bar{B}C\bar{D}) + ABD + \bar{A}\bar{B}D(C+\bar{C})$$

~~$$A\bar{B}CD + A\bar{B}C\bar{D} + ABC\bar{D} + A\bar{B}\bar{C}D$$~~

~~$$= A\bar{B}CD + A\bar{B}C\bar{D} + ABC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D}$$~~

Q1) $Y = AB + AC + BC$ (2m) *Wing day 9*

→ Identify missing variables in each term.

$$= AB(C+\bar{C}) + A\bar{C}(B+\bar{B}) + (A+\bar{A})BC$$

$$= \underline{ABC} + \underline{ABC} + \underline{ABC} + \underline{ABC} + \underline{ABC}$$

$$= \underline{ABC} + \underline{ABC} + \underline{ABC} + \underline{ABC}$$

Q1) $Y = \bar{A}B + AC + \bar{C}$

→ Identify missing variables in the above

$$\rightarrow \bar{A}\bar{B}(C+\bar{C}) + AC(B+\bar{B}) + \bar{C}(A+\bar{A})(B+\bar{B})$$

$$\rightarrow \bar{A}\bar{B}C(C+\bar{C}) + AC(B+\bar{B}) + \bar{C}(A+\bar{A})(B+\bar{B})$$

$$\rightarrow \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}C + (\bar{A}\bar{C} + \bar{A}C)(B+\bar{B})$$

$$\rightarrow \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$$

$$\rightarrow \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$Q11 \quad (A+B)(B+C)(A+\bar{C})$$

$$\Rightarrow (A+B+(A\bar{C}))(B+C+(A\bar{C})) (A+\bar{C}+(B+\bar{B}))$$

$$(A+B+C)(A+B+\bar{C})(B+C+A)(A+B+C) \quad | \quad (A+B+\bar{C})(A+B+C)$$

$$(A+B+C)(A+B+\bar{C})(\bar{A}+B+C)(A+\bar{B}+\bar{C})$$

K-map Imp

K-map reduction technique for the Boolean expression,

K-map Karnaugh Map Method (SOP) SOP

- * A graphical method for simplifying logic equations or truth table.
- * Also called K-map.
- * Theoretically can be used for any number of input variables, but practically limited to 5 to 6 variables.

Question - Draw four variable K-map (2 marks)

① 2 input variables

① (A) ② (B)

$$2^n = \text{no. of boxes}$$

$$2^2 = 4$$

<u>(A B)</u>	<u>B</u>	<u>B</u>
<u>A</u>	m ₀	m ₁
<u>A</u>	m ₂	m ₃

② 3 input variables

<u>A</u>	<u>BC</u>	<u>$\bar{B}\bar{C}$</u>	<u>$\bar{B}C$</u>	<u>$B\bar{C}$</u>	<u>BC</u>
<u>A</u>	m ₀	m ₁	m ₂	m ₃	m ₄
<u>A</u>	m ₅	m ₆	m ₇	m ₈	m ₉

* 4 variables K-map

A B C D

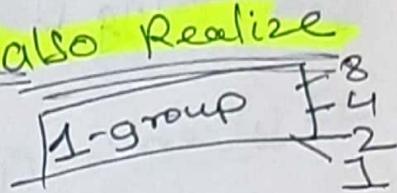
$$2^4 = 16$$

<u>A B / CD</u>	<u>$\bar{B}\bar{D}$</u>	<u>$\bar{B}D$</u>	<u>$B\bar{D}$</u>	<u>BD</u>	<u>$B\bar{D}$</u>
<u>$\bar{A}\bar{B}$</u>	m ₀	m ₁	m ₃	m ₂	m ₅
<u>$\bar{A}B$</u>	m ₄	m ₅	m ₇	m ₆	m ₈
<u>A \bar{B}</u>	m ₁₂	m ₁₃	m ₁₅	m ₁₄	m ₁₀
<u>A B</u>	m ₈	m ₉	m ₁₁	m ₁₀	m ₁₂

SSTE Questions

Minimization of SOP using K-map also Realize it

(Σm) -Keyword structure



Minimize the following expression using K-map.

$$f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 10)$$

Answer:

Given, $f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 10)$

Given variables are 4 so 2^n bit K-map
 \therefore given form is in SOP form

$$2^4 = 16$$

K-map table

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	1	1	0	0
$\bar{A}B$	1	1	1	0
AB	0	0	0	1
$A\bar{B}$	1	1	0	0

Add all the egn obtained from table.

$$\bar{B}CD + \bar{B}\bar{C} + \bar{A}BD + \bar{A}\bar{C}$$

$$\therefore f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 10)$$

$$= \bar{B}CD + \bar{A}\bar{C} + \bar{A}BD + \bar{B}\bar{C}$$

minimize the four variable logic function
using K-map. $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 11, 14)$

Q2

4m

\Rightarrow Given: $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9)$

There are 4 variables given so, we will

Plot K-map for 4 variables

$2^n = 2^4 = 16$ \therefore Given expression in SOP form

		K-map			
		CD	$\bar{C}D$	CD	$\bar{C}\bar{D}$
AB		$\bar{C}\bar{D}$	$\bar{C}D$	CD	$\bar{C}\bar{D}$
$\bar{A}\bar{B}$		1	1	1	1
$\bar{A}B$		0	1	1	0
$A\bar{B}$		0	0	0	1
AB		1	0	0	0
		① $\bar{B}\bar{C}\bar{D}$	1	1	② $ABC\bar{D}$
		1	1	1	③ $\bar{A}\bar{B}$
		1	1	1	④ $\bar{A}B\bar{D}$

Add all the above equation.

$$\bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B} + \bar{A}D + BD$$

$$\begin{aligned} \therefore f(A, B, C, D) &= \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14) \\ &= \bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B} + \bar{A}D + BD \end{aligned}$$

= Realize given expression using K-map

$$f(A, B, C, D) = \sum m(3, 5, 7, 8, 10, 11, 12, 13) \quad \text{L-marks}$$

$$\text{Given : } f(A, B, C, D) = \sum m(3, 5, 7, 8, 10, 11, 12, 13)$$

There are 4 variables given so, $n=4$.

$$\therefore \text{Plot K-map for 4 variables } 2^n = 2^4 = 16$$

\therefore given expression is in SOP form.

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD	$\bar{A}\bar{C}\bar{D}$
$\bar{A}\bar{B}$	0	0	1	0	0
$\bar{A}B$	0	1	1	0	0
$A\bar{B}$	1	1	0	0	0
AB	1	0	1	1	1

$\bar{A}\bar{C}\bar{D}$ $B\bar{C}D$

Add all the minterms obtained from upper K-map table.

$$A\bar{C}\bar{D} + B\bar{C}D + A\bar{B}C + \bar{A}CD$$

$$\begin{aligned} \therefore f(A, B, C, D) &= \sum m(3, 5, 7, 8, 10, 11, 12, 13) \\ &= A\bar{C}\bar{D} + B\bar{C}D + A\bar{B}C + \bar{A}CD \end{aligned}$$

Q4 Reduce the following expression using k-map
 $f(A, B, C, D) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$

Given

$$f(A, B, C, D) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$$

There are 4 variables given, so, we will
 Plot k-map for 4 variables. $n=4$

$$2^n = 2^4 = 16$$

: given expression is in SOP form.

		K-map				
		$\bar{C}D$	$\bar{C}D$	$\bar{C}D$	CD	CD
		$A\bar{B}$	AB	AB	AB	$A\bar{B}$
		0	1	0	0	0
		0	1	1	1	1
		1	1	1	1	0
		0	0	1	1	0
		1	1	1	0	0
		$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$AC\bar{D}$	$A\bar{C}D$

Add all above k-map equation

$$ABC + ACD + A\bar{C}D + \bar{A}BC + \cancel{BD}$$

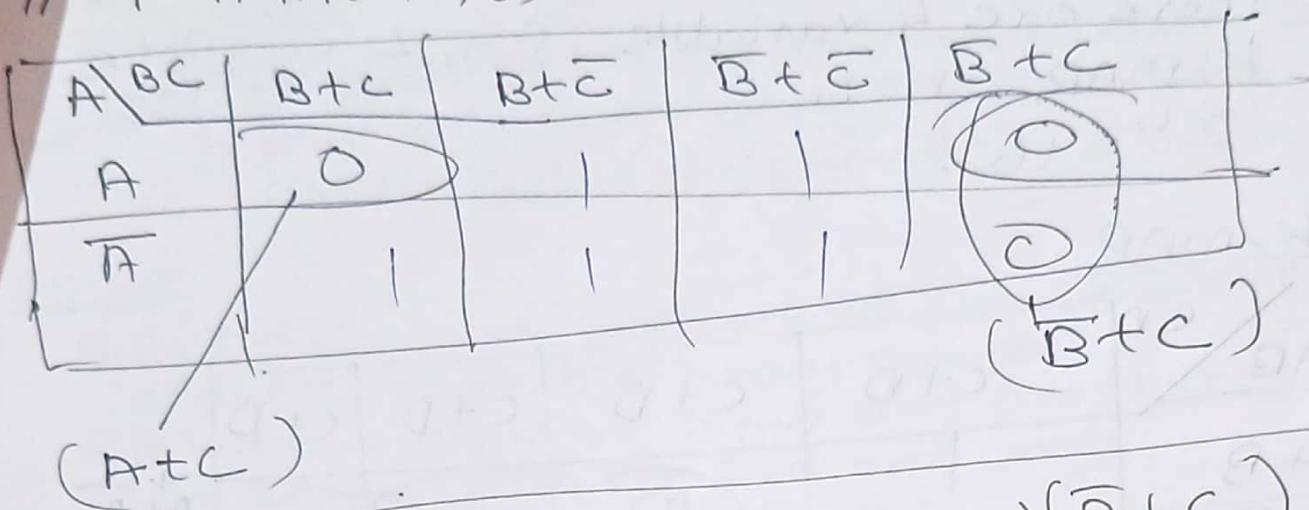
$$\therefore f(A, B, C, D) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$$

$$= A\bar{B}\bar{C} + ACD + A\bar{C}D + \bar{A}BC + BD$$

Multiplication of POS expression using K-MAP

Notes - $A \Rightarrow \bar{A} + \bar{A} \Rightarrow A$ $\bar{A} \Rightarrow A$ 0-groups
 $B \Rightarrow \bar{B}$, $\bar{B} \Rightarrow B$ $\bar{B} \Rightarrow B$ $+ \Rightarrow X$

Q1) $Y = \pi m(0, 2, 6)$



$\therefore \text{So } Y = \pi m(0, 2, 6) = (A+C)(\bar{B}+C)$

MSBTE Question

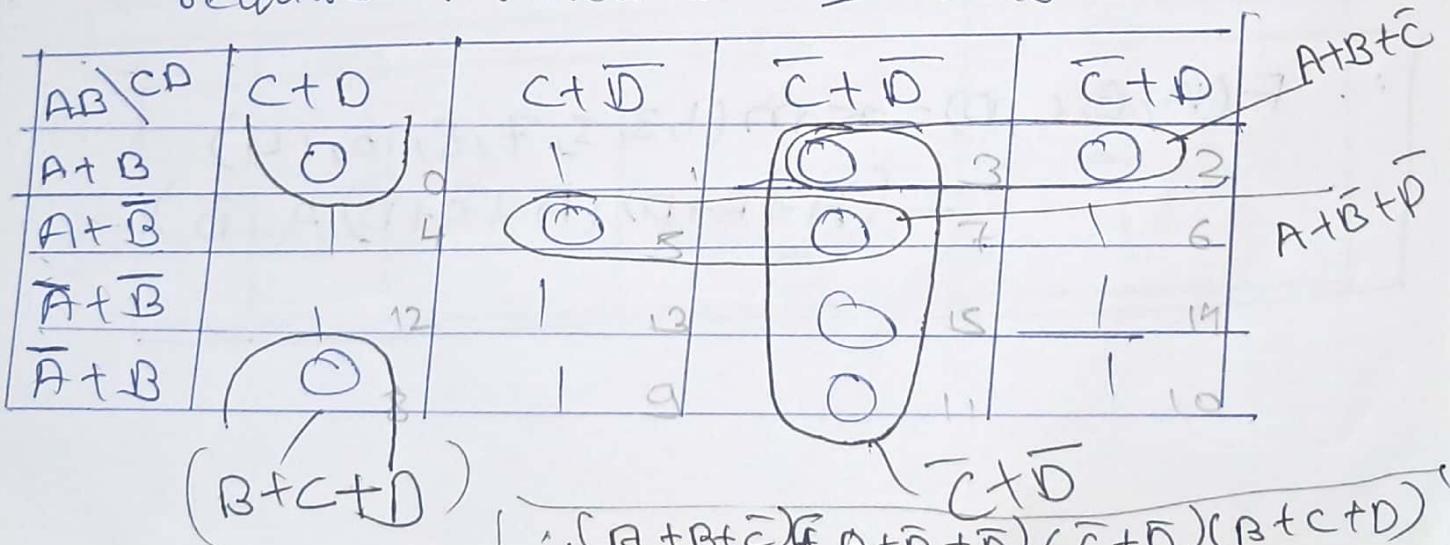
Q1) Realize or simplify following eqn using K-MAP.

$$Y = \pi M(0, 2, 3, 5, 7, 8, 14, 15)$$

$\Rightarrow m = \text{maxterms}$. $\therefore \text{Eqn is in form of POS}$

$$\text{So, given } = \pi m(0, 2, 3, 5, 7, 8, 14, 15)$$

As there are 8 max number 15 so, it will require 4 variables. $2^4 = 16$.



$$\therefore (A+B+C')(A+B+D')(C+D)(B+C+D)$$

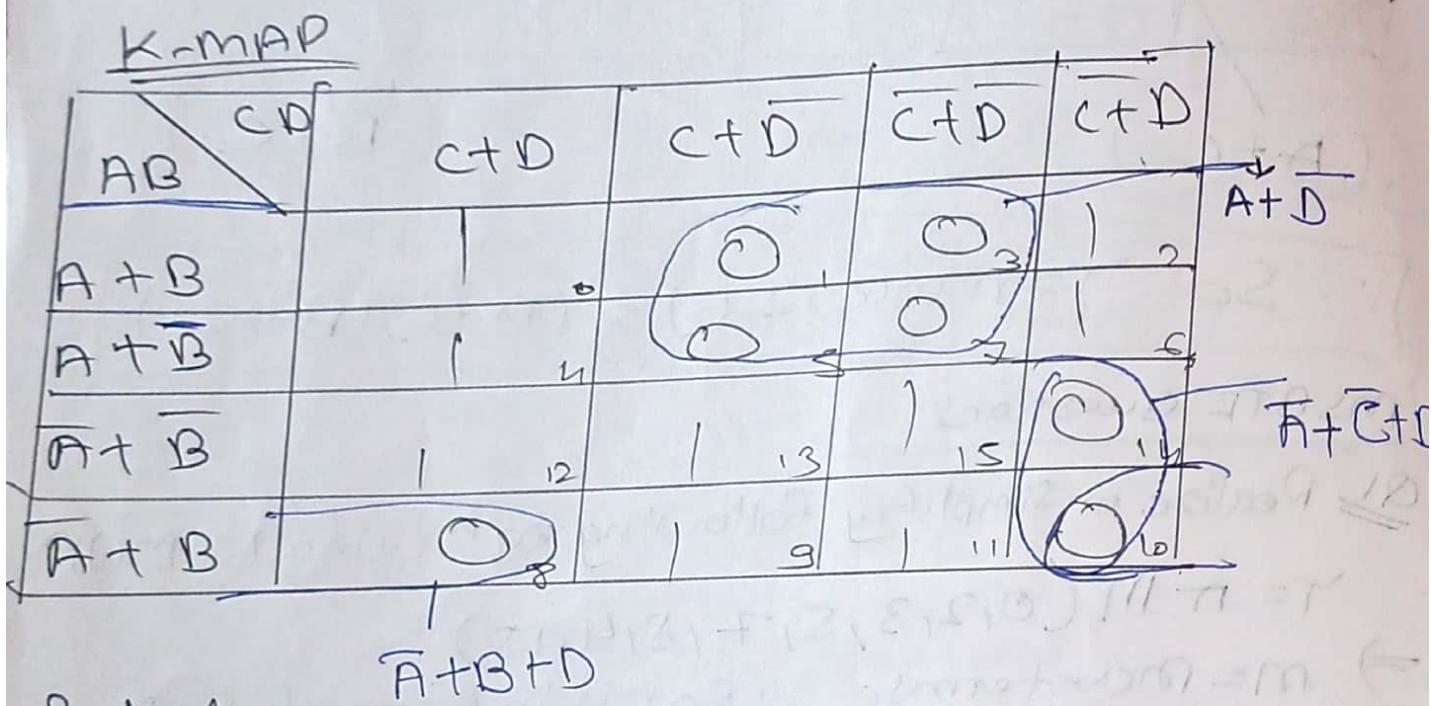
Q2 Reduce the following expression using K-map and implement it if $F(A, B, C, D) = \prod M(1, 3, 5, 7, 8, 10, 14)$

$\therefore \prod M = \text{max term}$ \therefore It is in POS form

Given : $F(A, B, C, D) = \prod M(1, 3, 5, 7, 8, 10, 14)$

There are 4 variable. So, 4 variable K-MAP. $n=4$.

$$2^4 = 16.$$



Product

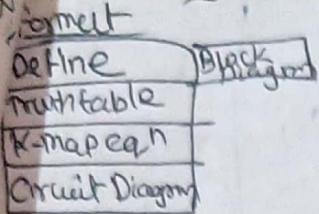
Add all above obtain eqn from K-MAP.

$$(\bar{A}+B+D) (\bar{A}+\bar{C}+D) (A+\bar{D})$$

$\therefore F(A, B, C, D) = \prod M(1, 3, 5, 7, 8, 10, 14)$

$$= (\bar{A}+B+D) (\bar{A}+\bar{C}+D) (A+\bar{D})$$

3. Design of arithmetic circuits and code converter using K-map



- Half Adder and Subtractor
- Full Adder and Subtractor
- Gray to Binary (4 bits)
- Binary to Gray (4 bits)

Half Adder

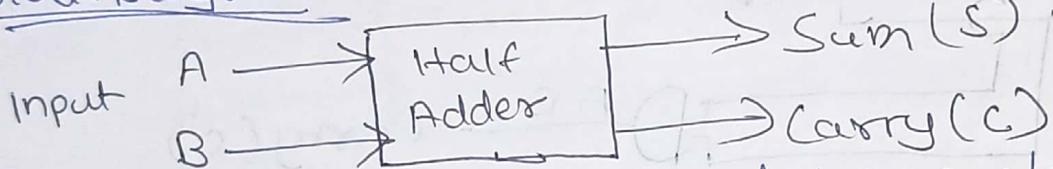
Questions

→ Draw an Circuit Diagram of Half Adder. (2m)
 → Draw logic diagram of half adder circuit & classify/Explain it. (4marks)

Answer

- * Half Adder is an combinationel circuit which adds two single bit binary numbers.
- * It has two single bit inputs and produces two outputs which are sum and carry.

Block Diagram



There are two inputs A, B and two outputs Sum and Carry to perform arithmetic operation.

Truth Table

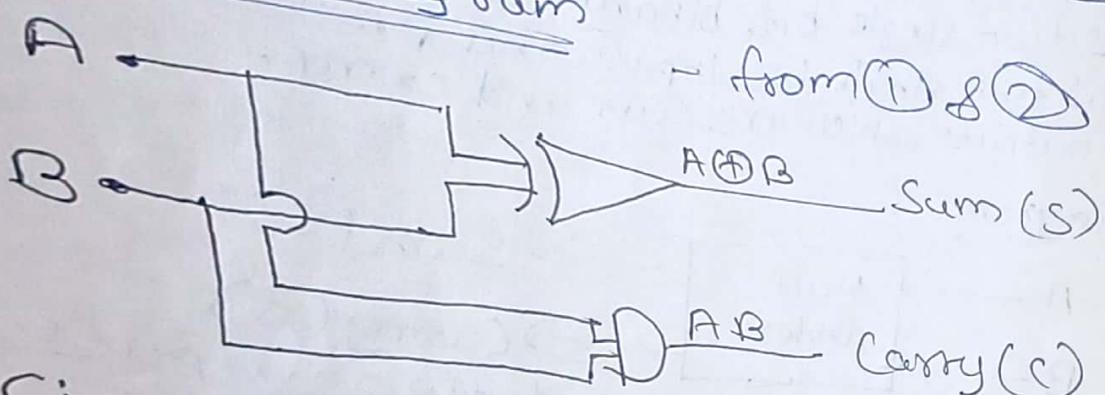
<u>Inputs</u>		<u>Outputs</u>	
<u>A</u>	<u>B</u>	<u>Sum (S)</u>	<u>Carry (C)</u>
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A	B	Sum	Carry
D	D	0	0
D	A	1	0
D	B	0	0
D	A+B	1	1

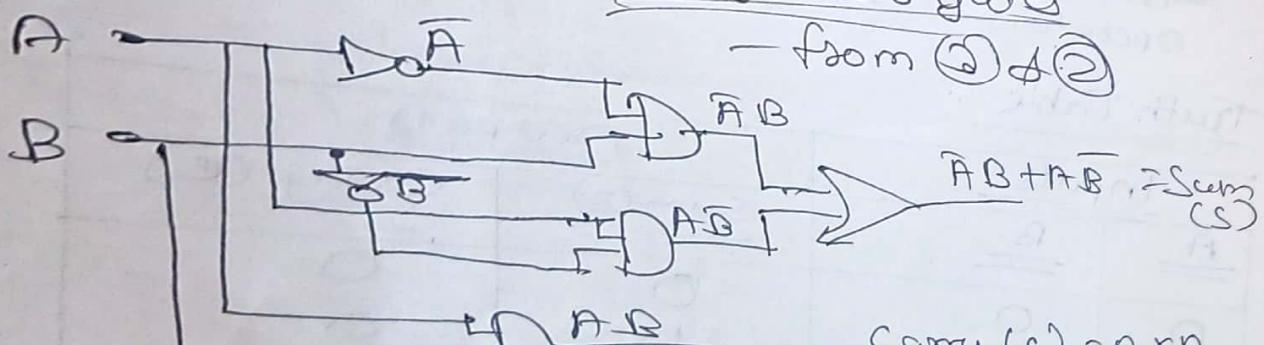
$$\text{Sum} = A \oplus B$$

$$\begin{aligned} \text{Sum} &= \overline{AB} + A\overline{B} - \textcircled{1} \\ \text{Sum} &= A \oplus B \quad (\text{Ex-OR gate}) \end{aligned}$$

Circuit Diagram



Circuit Diagram using Basic Gates



A	B	Sum	Carry
D	D	0	0
D	A	0	0
D	B	0	0
D	A+B	1	1

$$\begin{aligned} \text{Carry} &= A B \\ &= (\text{And gate}) \end{aligned}$$

$$\text{Carry} = A \times B$$

from $\textcircled{1}$ & $\textcircled{2}$

Sum (S)

Carry (C)

from $\textcircled{1}$ & $\textcircled{2}$

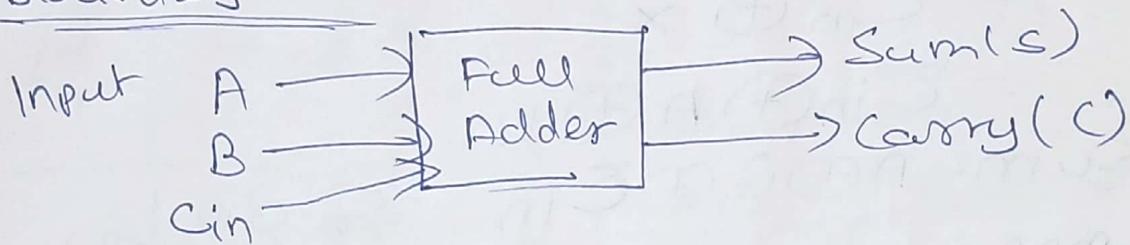
$$\overline{AB} + A\overline{B} = \text{Sum (S)}$$

$$\text{Carry (C)} = A \times B$$

Full Adder

- Question
- Describe the function of Full Adder Circuit using its truth table, K-map simplification and logic diagram. (4m)
 - Design a full Adder using Truth table and K-map. (4m)
 - Draw logic diagram of full adder using K-map simplification with write truth table. (4m)
 - Describe function of Full adder circuit with its truth table and diagram. (4m)
 - Built full Adder using Half Adder circuit. (4m)
- Full Adder is an combinational circuit.
- In which adds 3 single bit inputs and produces two output sum and carry.

Block diagram



Truth table

Inputs			Outputs	
A	B	Cin	Sum(S)	Carry(C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-MAP for Sum

	$A \setminus BC$	$\bar{B}C_{in}$	$\bar{B}C_{in}$	BC_{in}	BC_{in}	
\bar{A}	0	1	0	1	0	$\bar{A}BC_{in}$
A	1	0	1	0	1	ABC_{in}
	$AB\bar{C}_{in}$	$A\bar{B}C_{in}$	$\bar{A}\bar{B}C_{in}$	$\bar{A}BC_{in}$	ABC_{in}	

$$\begin{aligned}
 \text{Sum} &= A\bar{B}\bar{C}_{in} + A\bar{B}C_{in} + \bar{A}\bar{B}C_{in} + \bar{A}\bar{B}\bar{C}_{in} \\
 &= \bar{C}_{in}(A\bar{B} + \bar{A}B) + C_{in}(\bar{A}\bar{B} + \bar{A}B) \\
 &= \bar{C}_{in}(A \oplus B) + C_{in}(\bar{A} \oplus \bar{B})
 \end{aligned}$$

$$A \oplus B = x$$

$$= \bar{C}_{in}x + C_{in}\bar{x}$$

$$= \bar{C}_{in} \oplus x$$

$$= \bar{C}_{in} \oplus A \oplus B$$

$$\boxed{\text{Sum} = A \oplus B \oplus \bar{C}_{in}} \quad \text{≡ SR-OR}$$

K-MAP for Carry

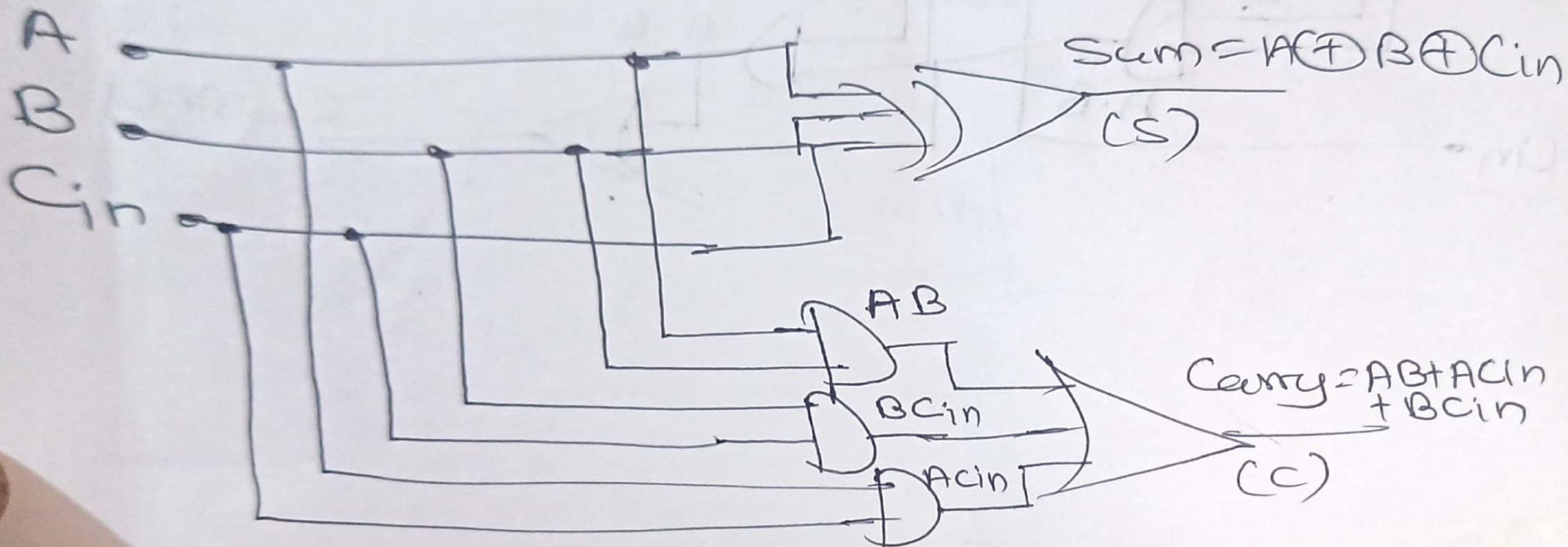
	$A \setminus BC$	$\bar{B}C_{in}$	$\bar{B}C_{in}$	BC_{in}	BC_{in}	
\bar{A}	0	0	1	1	0	
A	0	1	0	1	1	
	AC_{in}	$\bar{A}\bar{B}C_{in}$	$\bar{A}BC_{in}$	ABC_{in}	AB	

Carry = $AB + AC_{in} + BC_{in}$

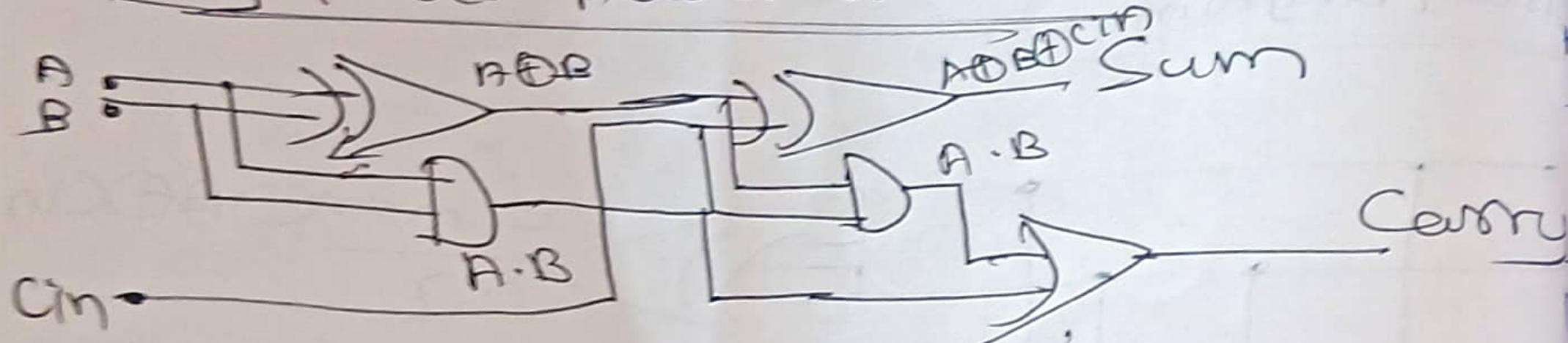
(2)

B Cin | B Cin |

Circuit Diagram



Using Half Adder circuit

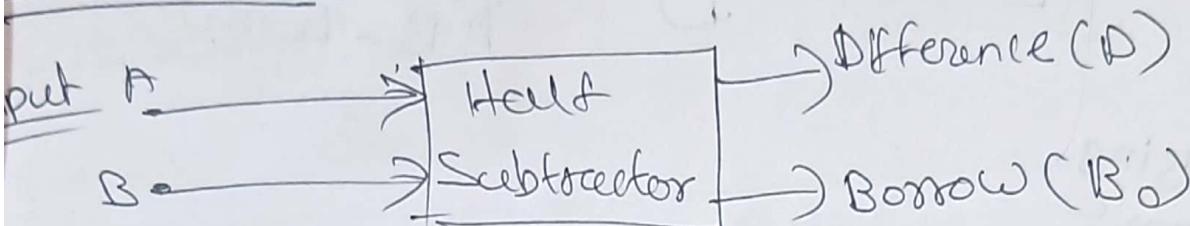


Half Subtractor

is an combinational circuit .

subtract two single bit numbers .

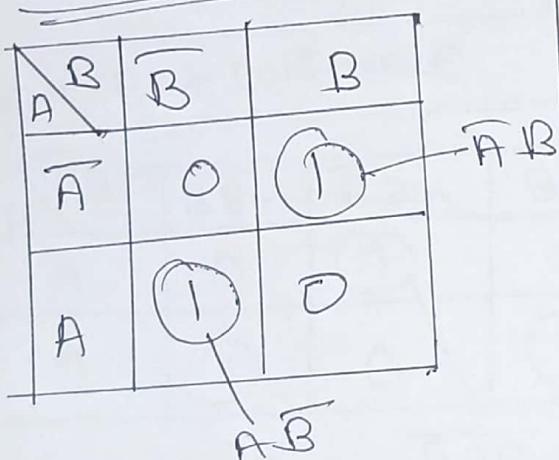
Block Diagram



Truth table

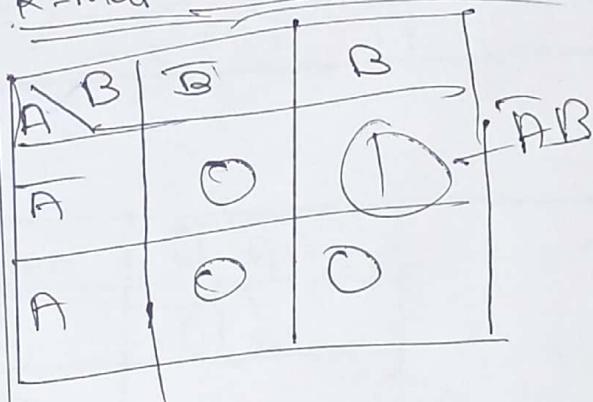
Inputs		Outputs	
A	B	Difference (D)	Borrow (B ₀)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-map for Difference (D)



$$\begin{aligned} \text{Diff} &= A\bar{B} + \bar{A}B \\ &= A \oplus B \end{aligned}$$

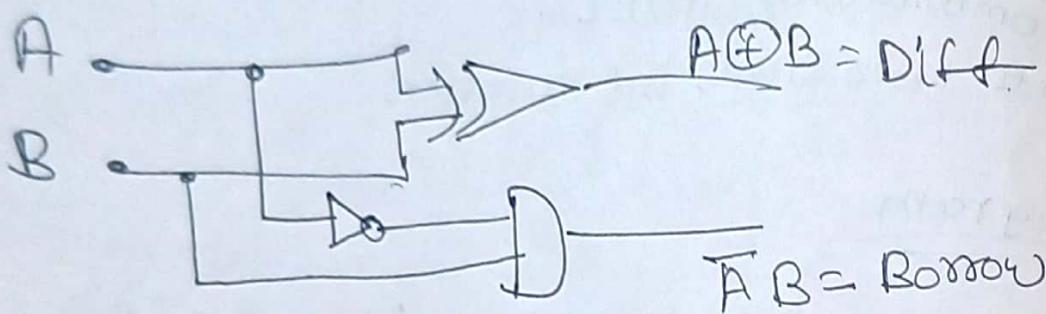
K-map for Borrow B₀



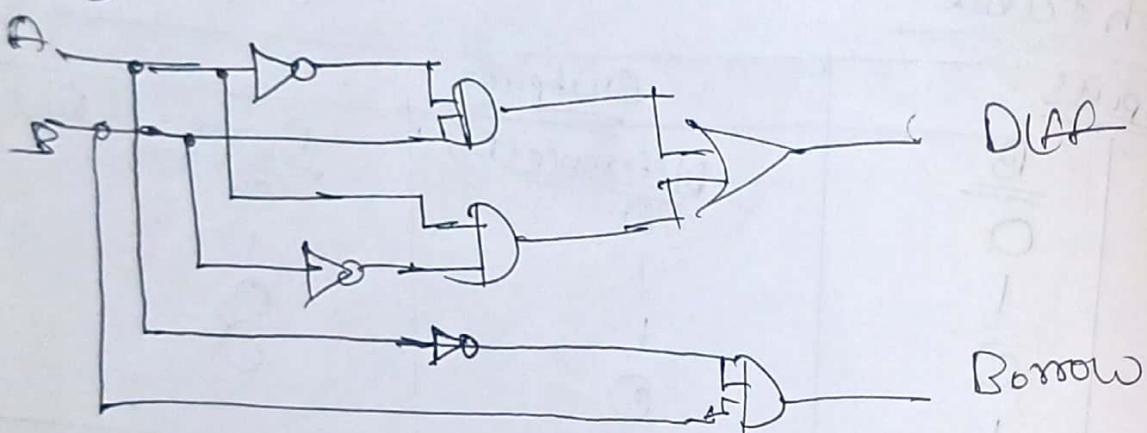
$$\text{Borrow } B_0 = \bar{A}B$$

- 2

Circuit Diagram



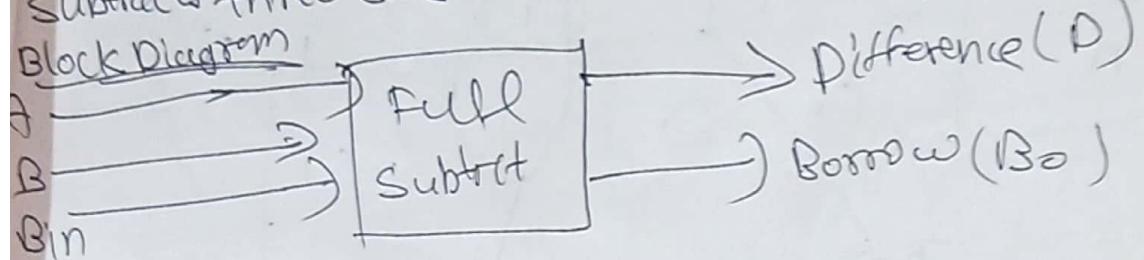
Using
basic
gates



Subtractor

Full Subtractor is a combinational circuit which subtracts three single bit numbers.

Block Diagram



Truth table

<u>Input</u>			<u>Output</u>	
<u>A</u>	<u>B</u>	<u>B_{in}</u>	<u>D</u>	<u>B₀</u>
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-map of Difference

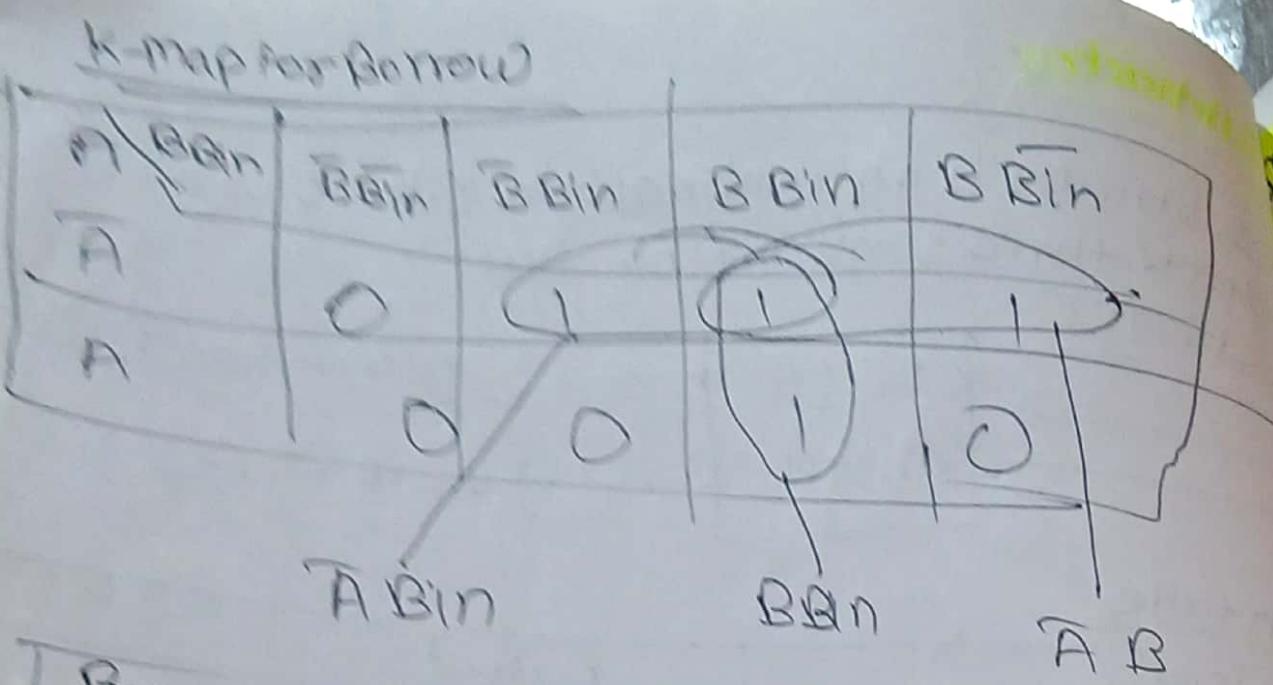
<u>A\B Bin</u>	<u>B Bin</u>	<u>B Bin</u>	<u>B Bin</u>	<u>B Bin</u>
<u>A</u>	0	1	0	1
<u>A</u>	1	0	1	0

$\overline{A} \overline{B} \text{Bin}$ $\overline{A} B \text{Bin}$ $A \overline{B} \text{Bin}$ $A B \text{Bin}$

$\overline{A} B \text{Bin}$

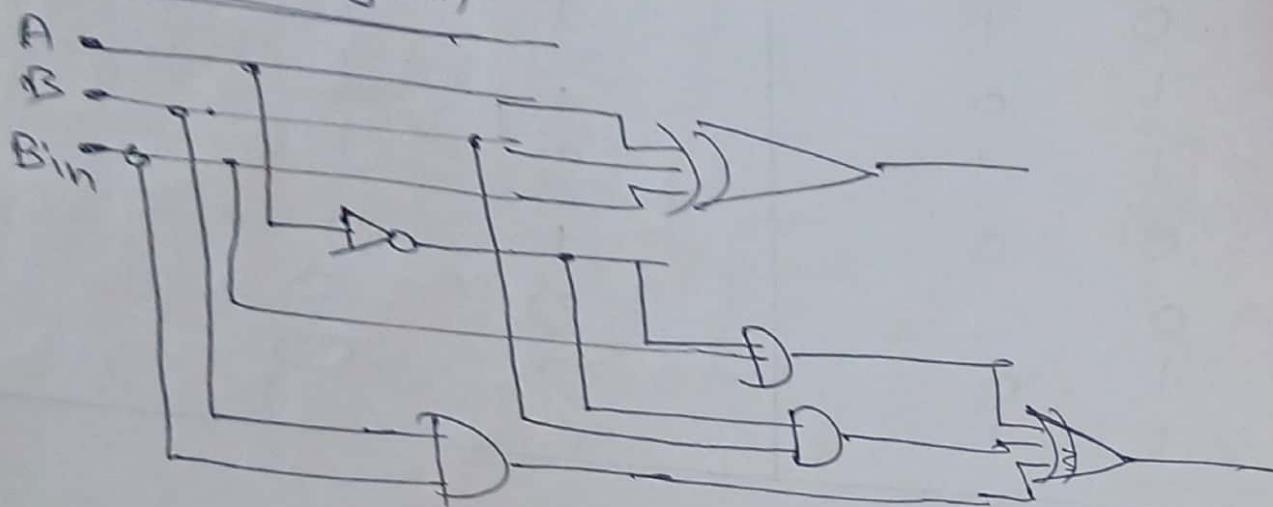
$$\begin{aligned}
 \text{Diff} &= \overline{A} \overline{B} \text{Bin} + \overline{A} B \text{Bin} + A \overline{B} \text{Bin} + A B \text{Bin} \\
 &= \text{Bin}(A \overline{B} + \overline{A} B) + \text{Bin}(\overline{A} B + A \overline{B})
 \end{aligned}$$

$$\begin{aligned}
 \boxed{A \oplus B = X} &= \text{Bin}(A \oplus B) + \text{Bin}(A \oplus B) \\
 &= \text{Bin} X + \text{Bin} \overline{X} \\
 &= \text{Bin} \oplus X \quad \boxed{\text{Bin} \oplus A \oplus B}
 \end{aligned}$$

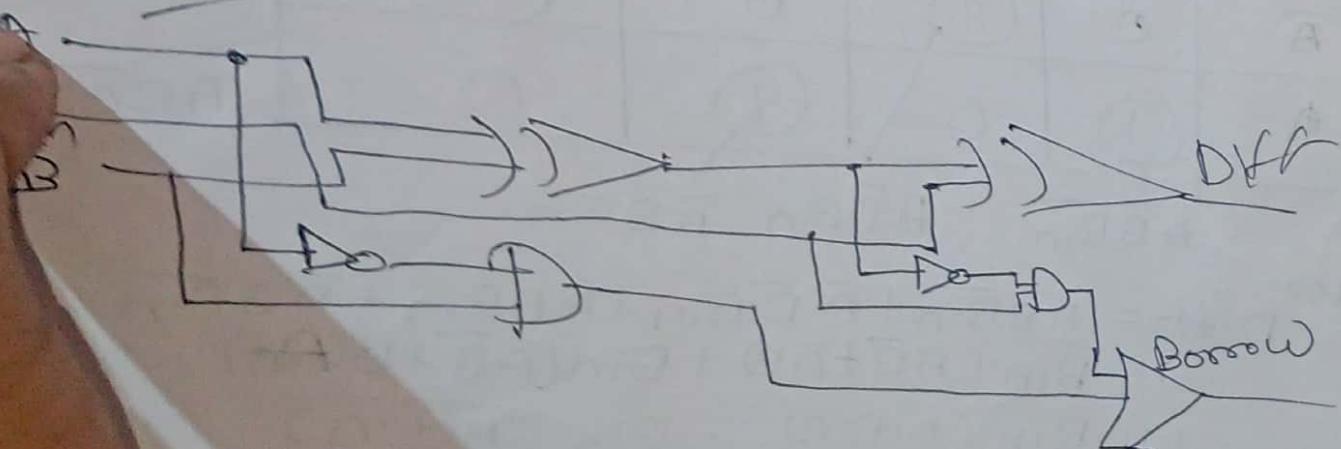


$$\text{Borrow} = \overline{A}B\text{In} + B\text{BIn} + \overline{A}\overline{B}$$

Circuit diagram



Using Half Subtractor



Gray Code to Binary
Binary to Gray Code Converter

(h marked
column)

Binary = input (4bit)
 Gray = output (4bit)

Input				Output			
B ₃	B ₂	B ₁	B ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

K-MAP for Y_3

$B_3 B_2 \backslash B_1 B_0$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$B_3 B_2$	0	0	0	0
$\bar{B}_3 B_2$	0	0	0	0
$B_3 \bar{B}_2$	1	1	1	1
$\bar{B}_3 \bar{B}_2$	1	1	1	1

$$\boxed{Y_3 = B_3} \quad \textcircled{1}$$

K-MAP for Y_2

$B_3 B_2 \backslash B_1 B_0$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$B_3 B_2$	0	0	0	0
$\bar{B}_3 B_2$	1	1	1	1
$B_3 \bar{B}_2$	0	0	0	0
$\bar{B}_3 \bar{B}_2$	1	1	1	1

$$Y_2 = \bar{B}_3 B_2 + B_3 \bar{B}_2$$

$$\boxed{Y_2 = B_3 \oplus B_2} \quad \textcircled{2}$$

K-MAP for Y_1

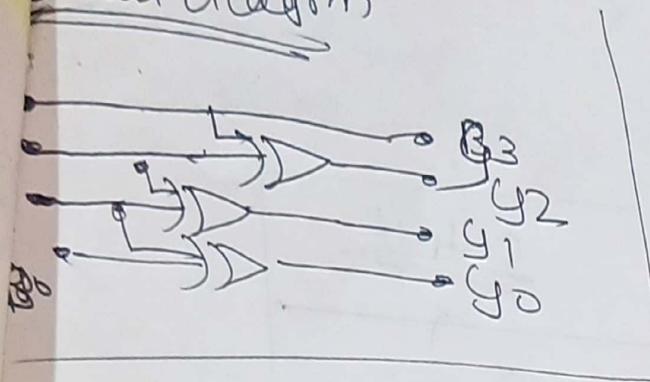
$B_3 B_2 \backslash B_1 B_0$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$B_3 B_2$	0	0	1	1
$\bar{B}_3 B_2$	1	1	0	0
$B_3 \bar{B}_2$	0	0	0	0
$\bar{B}_3 \bar{B}_2$	0	1	0	0

$$Y_1 = B_2 \bar{B}_1 + \bar{B}_2 B_1$$

K-MAP for Y_0

$B_3 B_2 \backslash B_1 B_0$	$\bar{B}_3 \bar{B}_2$	$\bar{B}_3 B_2$	$B_3 \bar{B}_2$	$B_3 B_2$
$B_3 B_2$	0	0	0	0
$\bar{B}_3 B_2$	0	0	1	1
$B_3 \bar{B}_2$	0	0	0	0
$\bar{B}_3 \bar{B}_2$	0	0	0	0

Circuit diagram

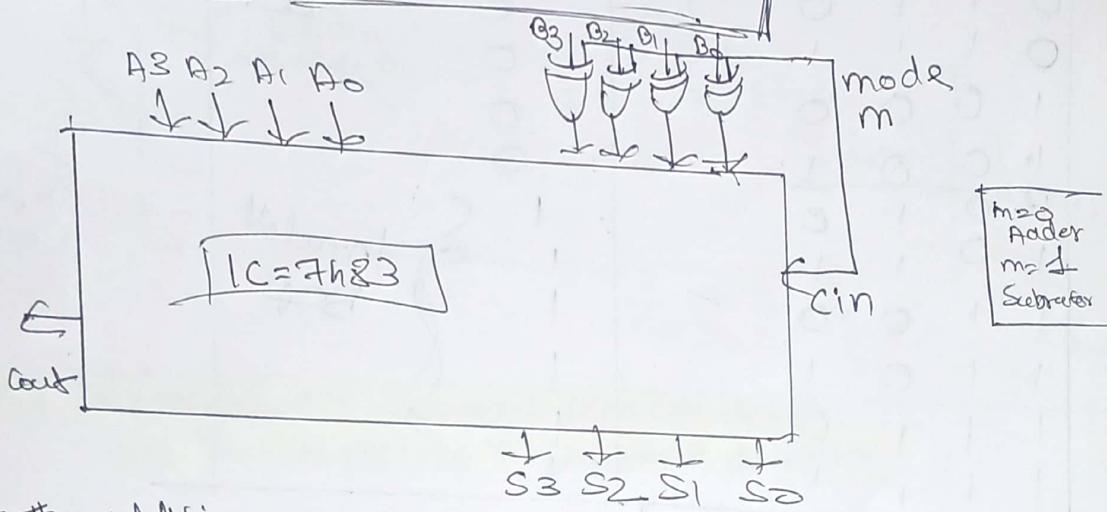


3.4 Arithmetic Circuits : (IC 7483) Adder and Subtractor, BCD Adder.

Questions

- Design four bit BCD adder using IC 7483.
- Design BCD adder using IC 7483.

IC 7483 as Adder & Subtractor



* The addition or subtraction of two 4-bit binary numbers can be implemented using IC 7483, shown above.

* The operation performed by circuit (Addition or Subtraction) depends on the state of mode.)

* Number B is applied to the adder through set of EX-OR gate. One input is (m).

$m=0 \rightarrow$ Adder \rightarrow Addition

$m=1 \rightarrow$ Subtractor \rightarrow Subtraction -

for Addition.

$$m=0$$

$$Cin=0$$

$$S = A + B + Cin$$

for Subtraction

$$m=1$$

$$Cin=1$$

$$S = A + 2^4 \cdot \text{complement}(B) + Cin$$

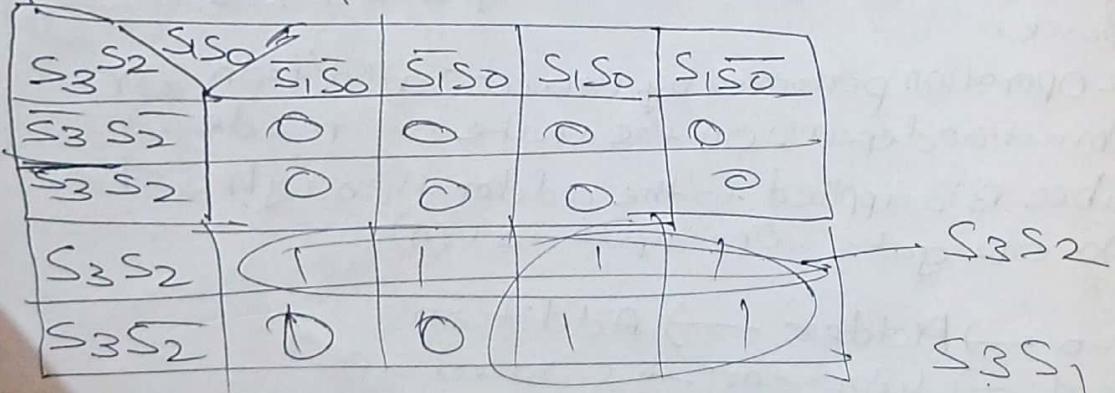
Truth table

<u>Input</u>				<u>Output</u>
S_3	S_2	S_1	S_0	χ
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

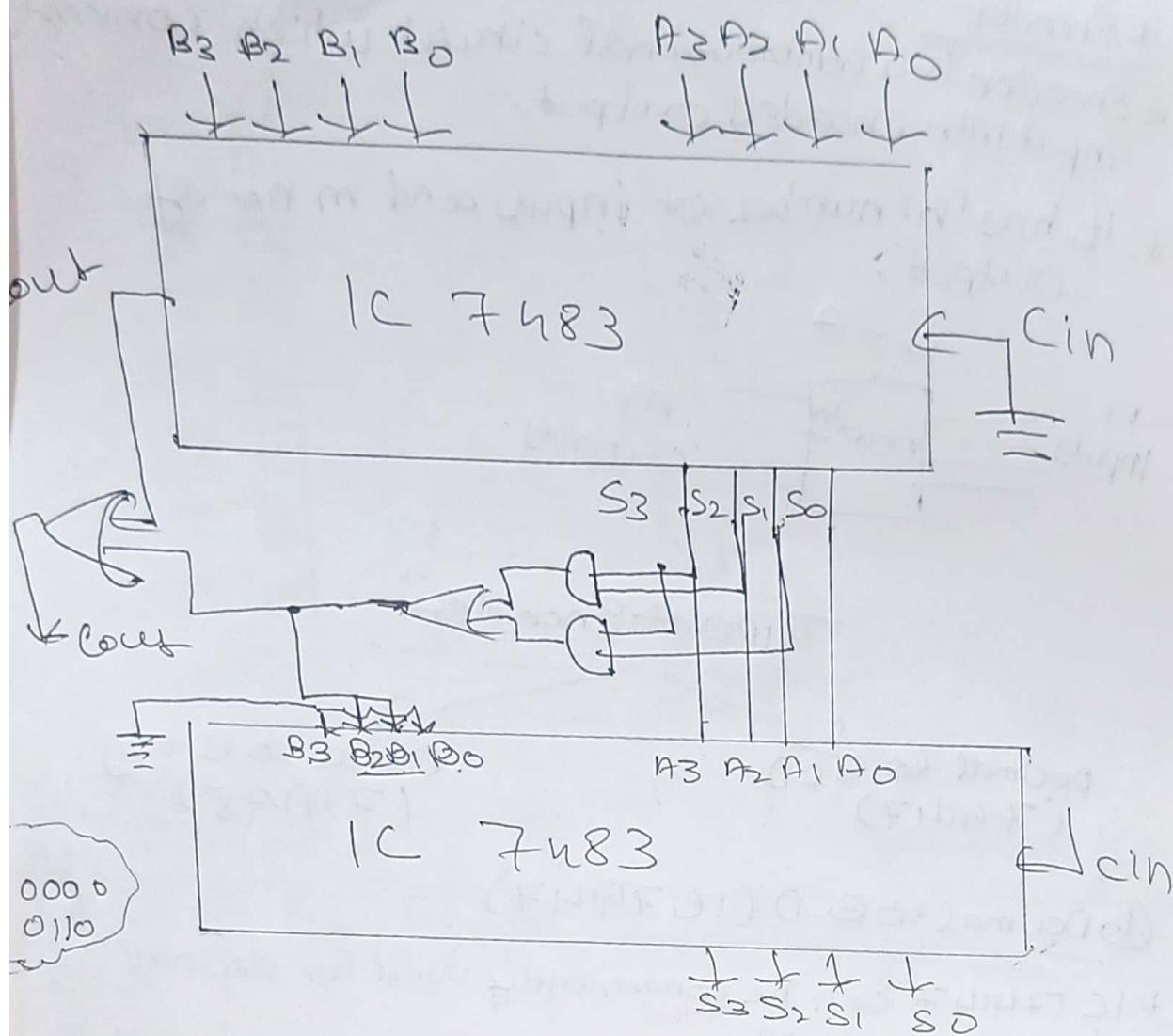
Half
BCD

Inverted
BCD

K-MAP for χ



with Diagram



3.5 Encoder/Decoder: Basics of encoder, decoder.

(IC 7447) BCD to 7 segment decoder.

Questions

Q// Draw a circuit diagram of BCD to seven segment decoder and write its truth table. (4m)

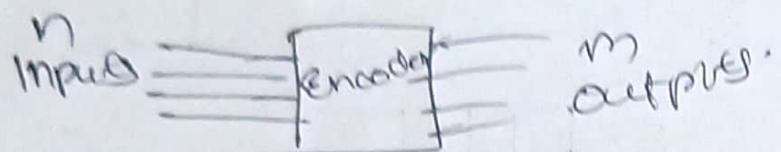
Repeat times : ~~1~~

Q// Design BCD to Seven Segment decoders using IC 7447 with truth table. (6 marks)

Q// Define encoder. write IC number of IC used as decimal to BCD encoder. (2 marks)

* Encoder

- * Encoder is a combinational circuit which converts input into encoded output.
- * It has n number of inputs and m no. of outputs.



Types of Encoder

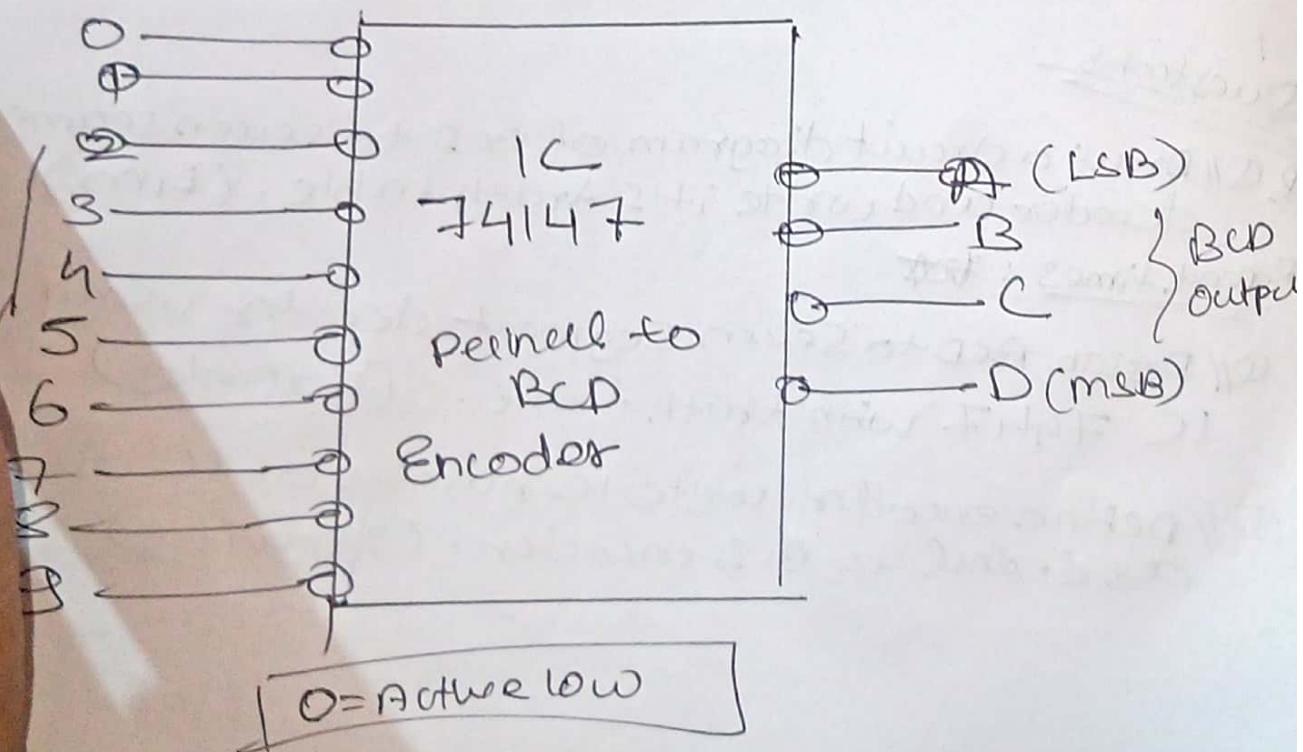
Decimal to BCD
(74147)

Octal to B binary
(74148)

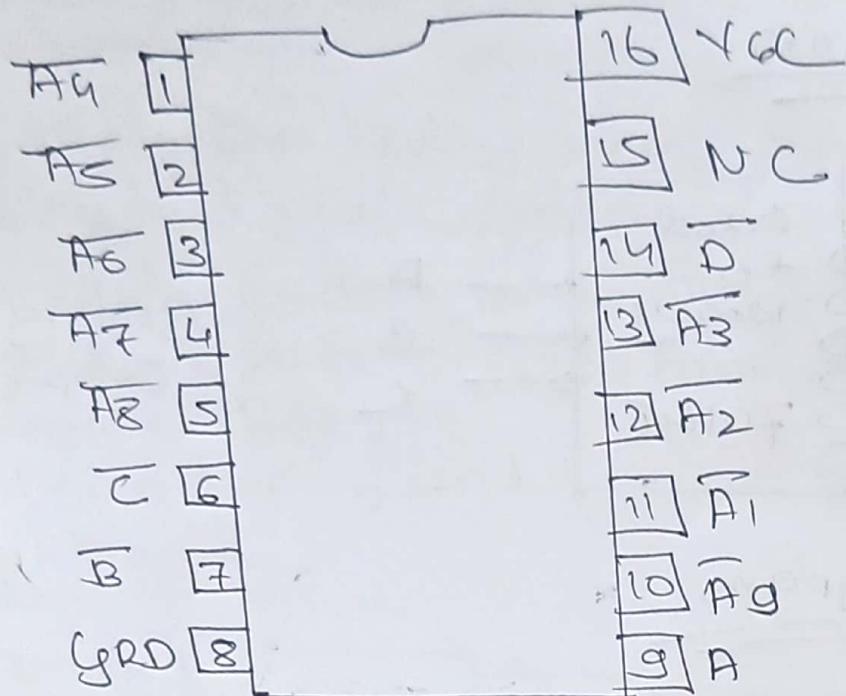
① Decimal to BCD (1C 74147)

- * IC 74147 can be conveniently used for decimal to BCD conversion.

Block Diagram



Diagram



Truth table

Actual logic / P

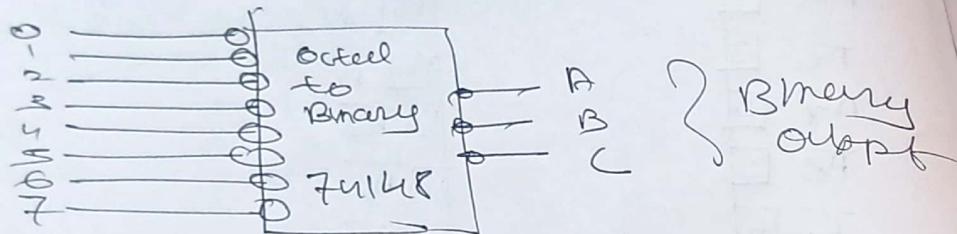
Actual low P/D

A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	D	C	B	A
0	0	1	1	1	1	1	1	1	1	1	1	1	1
X	0	1	1	1	1	1	1	1	1	1	1	1	0
X	X	0	1	1	1	1	1	1	1	1	1	0	0
X	X	X	0	1	1	1	1	1	1	1	1	0	-1
X	X	X	X	0	1	1	1	1	1	1	0	-1	-1
X	X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	X	X	X	0	1	0	1	1	-1
X	X	X	X	X	X	X	X	X	0	0	1	1	0

Response of
of Binary
product

Octal to Binary Encoder (IC 74148)

Block diagram



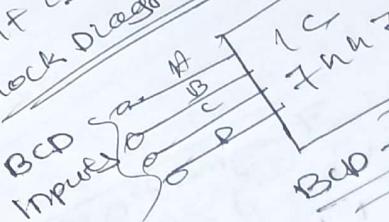
Pin Diagram



Truth table

Input (negative)								Active low output		
A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	C	B	A
0	1	1	1	1	1	1	1	1	1	1
X	0	1	1	1	1	1	1	1	1	0
X	X	0	1	1	1	1	1	1	0	1
X	X	X	0	1	1	1	1	1	0	0
X	X	X	X	0	1	1	1	0	1	1
X	X	X	X	X	0	1	1	0	1	0
X	X	X	X	X	X	0	1	0	0	1
X	X	X	X	X	X	X	0	0	0	0

Decoder
BCD to -7S
 * Seven segment display
 * display in digitalic sust
 * for displaying data usin
 data have to be convert
 Segment code:
 * If it is a display unit
 Block Diagram



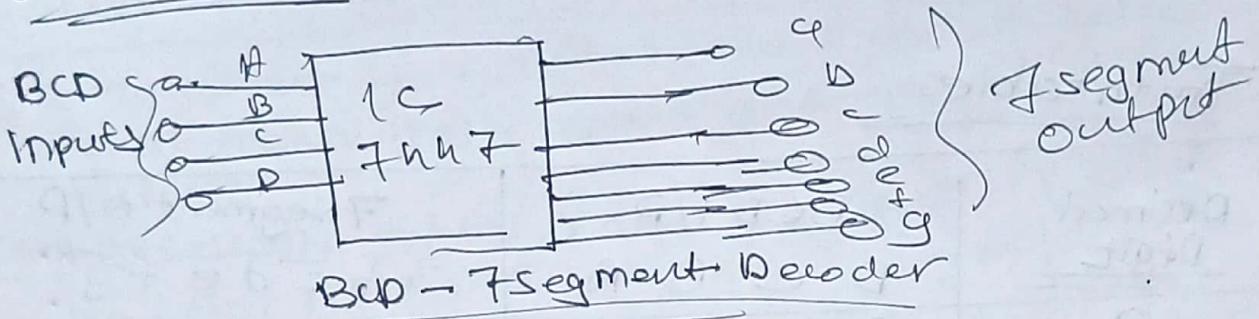
BS-7 Seg

Decoder Imp

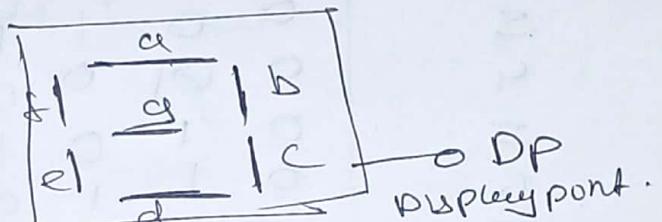
BCD-to-7segment Decoder IC 7447

- * Seven segment display is most popular used display in digital systems.
- * For displaying data using this device, the data have to be converted from BCD to 7-segment code.
- * It is a display unit.

Block Diagram

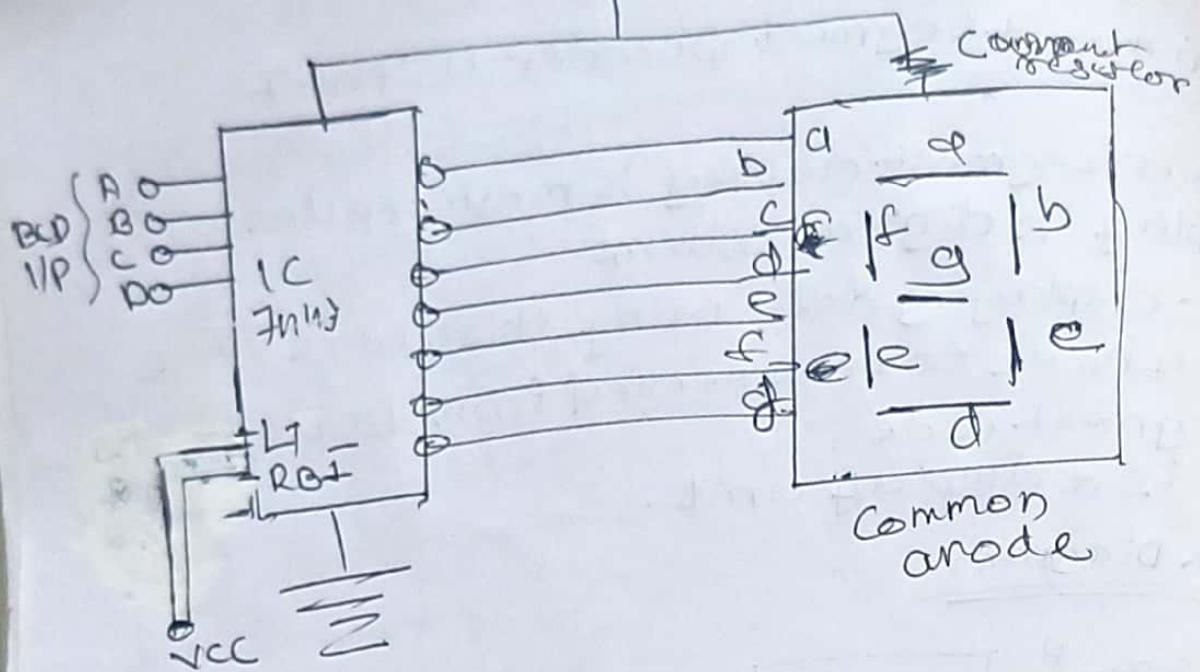


7segment Display



BCD-7segment





Truth table

Decimal Digit	BCD I/P				7Segment O/P						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	1	1	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	0	0	0	1
4	0	1	0	0	0	1	1	1	0	0	1
5	0	1	0	1	0	1	1	1	1	0	1
6	0	1	1	0	0	1	0	1	1	1	1
7	0	1	1	1	1	1	0	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

question

Q1) State necessity of demultiplexer. (2m)

Q2) Design 16:1 multiplexer using 4:1 multiplexers.
IMP (6marks)

Q3) State necessity of multiplexers. (2m)

Q4) Design 1:8 de multiplexer using 1:4 multiplexer.

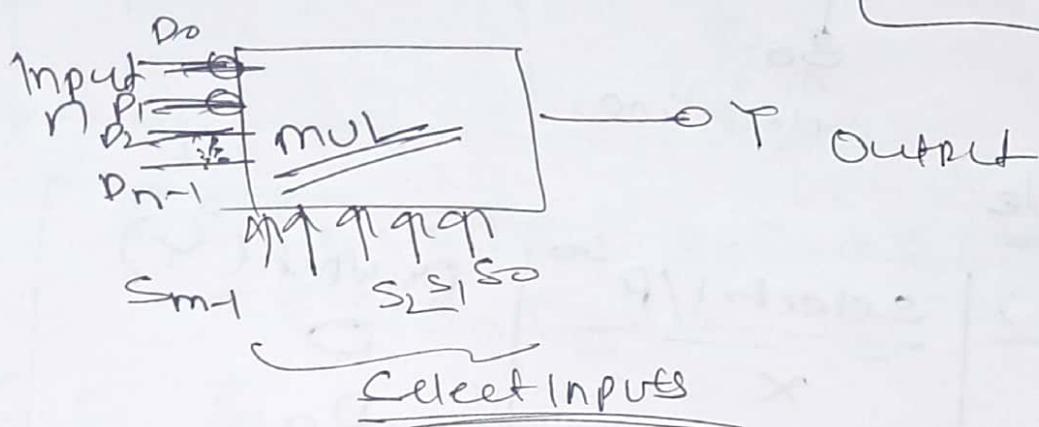
What is multiplexer?

~~one input \Rightarrow many one output~~

① A multiplexer is a digital circuit which selects one of the 'n' data inputs and connects it to n outputs

② The selection of one of the 'n' input is done by select lines and given by

$$\begin{cases} n = 2^m \\ LHS = RHS \end{cases}$$



Select Inputs

Types

32:1
 $2 = 2^m$
 $2 = 2^5$
 $m = 5$

2:1
1

$2 = 2^m$
 $2 = 2^1$
 $m = 1$

$2 = 2^m$
 $2 = 2^2$
 $m = 2$

4:1

8:1

$2 = 2^m$
 $2 = 2^3$
 $m = 3$

$2 = 2^m$
 $2 = 2^4$
 $m = 4$

Necessity of multiplexer

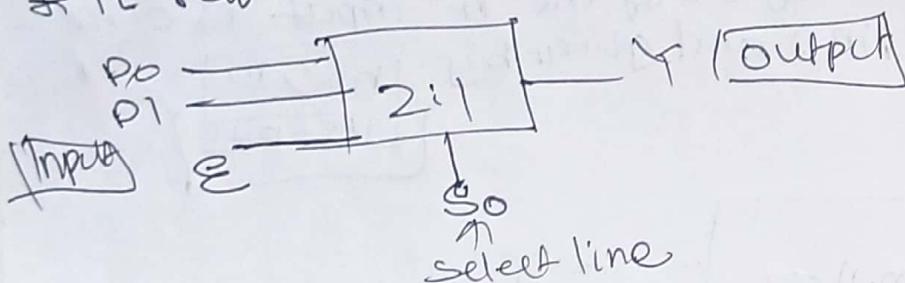
- Reduces the number of wires required for transmission.
- They can be also used to implement Boolean functions and multiple variable.
- In digital techniques, single input from many input lines and route it output using control signal.
- Combination circuits
- Analog to digital

Logic diagram is simplified
minimize IC package count.

2:1

It is having two inputs & one output.

- It is having two inputs & one output.
- It requires 2 select line

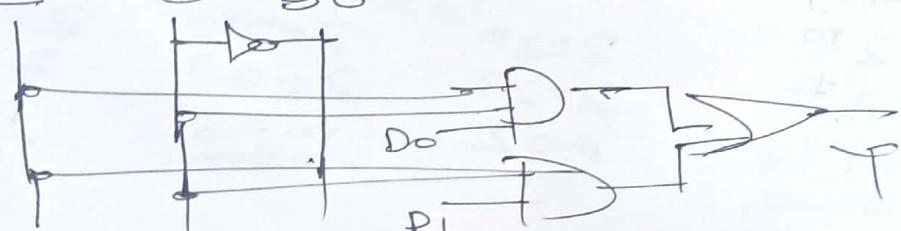


Truth table

Enable (E)	Select I/P ^{S0}	Output (Y)
0	x	0
1	0	D0
1	1	D1

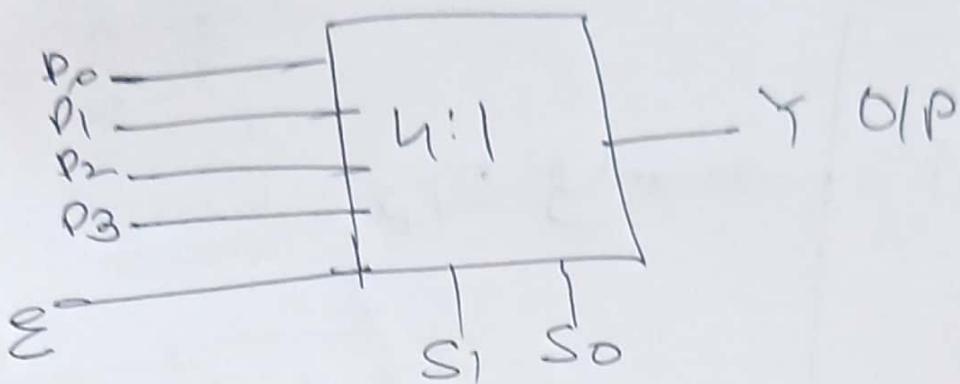
$$Y = E \overline{S_0} D_0 + E S_0 D_1$$

E S0 D0



Multiplexer

4 inputs
1 output
2 select lines.



Truth-table

Enable

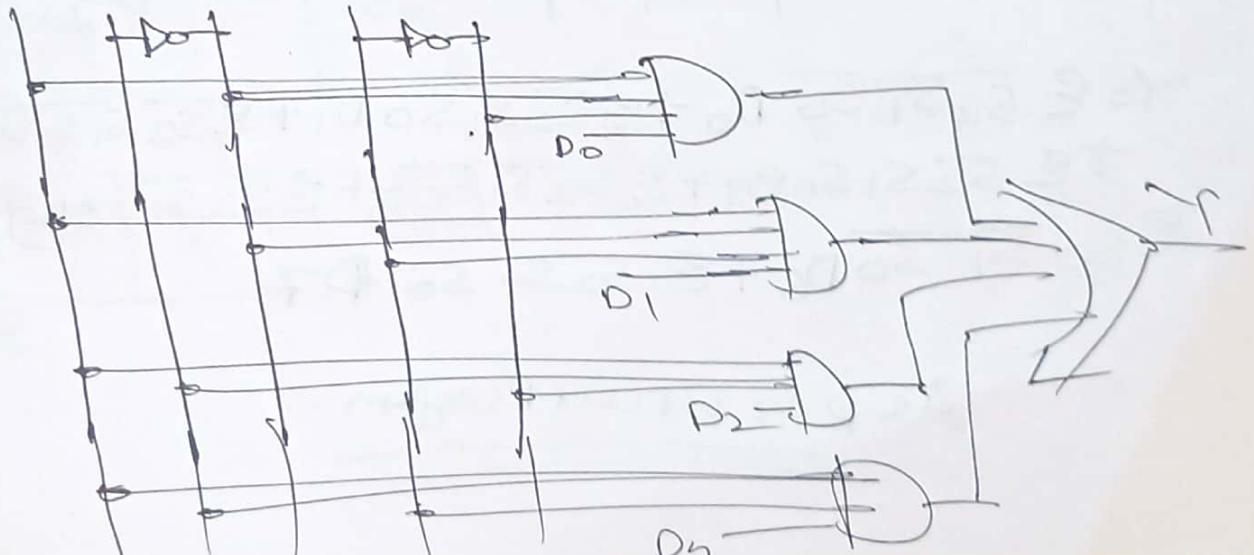
Select Input

O/P

<u>Enable</u>	<u>S₁</u>	<u>S₀</u>	<u>O/P</u>
1	0	0	D ₀
1	0	1	D ₁
1	1	0	D ₂
1	1	1	D ₃

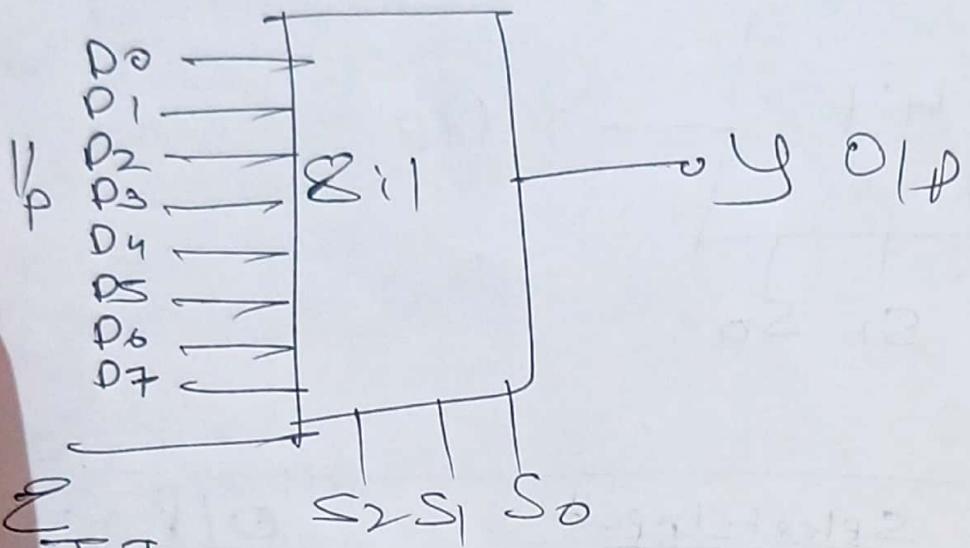
$$E \bar{S}_1 \bar{S}_0 D_0 + E \bar{S}_1 S_0 D_1 + E S_1 \bar{S}_0 D_2 + E S_1 S_0 D_3$$

$$E S_1 \bar{S}_1 S_0 \bar{S}_0$$



8:1

8 input
1 output
3 select lines



E
T.T
Enable

Select line

Output

	S ₂	S ₁	S ₀	
1	0	0	0	D ₆
1	0	0	1	D ₁
1	0	1	0	D ₂
1	0	1	1	D ₃
1	1	0	0	D ₄
1	1	0	1	D ₅
1	1	1	0	D ₆
1	1	1	1	D ₇

$$\begin{aligned}
 Y = & \sum \overline{S_2} \overline{S_1} \overline{S_0} D_0 + \sum \overline{S_2} \overline{S_1} S_0 D_1 + \sum \overline{S_2} S_1 \overline{S_0} D_2 \\
 & + \sum \overline{S_2} S_1 S_0 D_3 + \sum S_2 \overline{S_1} \overline{S_0} D_4 + \sum S_2 \overline{S_1} S_0 D_5 \\
 & + \sum S_2 S_1 \overline{S_0} D_6 + \sum S_2 S_1 S_0 D_7
 \end{aligned}$$

As per circuit diagram

Multiplex tree

Combination of mux is known as mux tree.

Design 16: I using 4:1

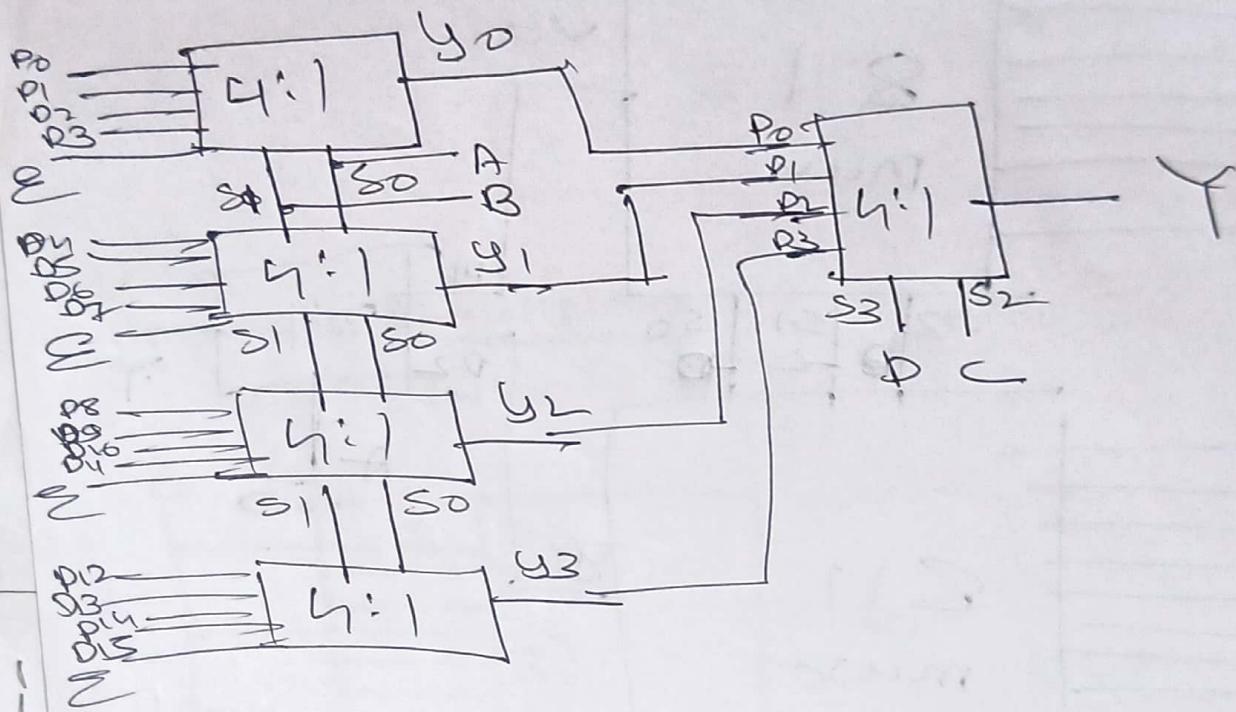
6marks

$$n=16$$

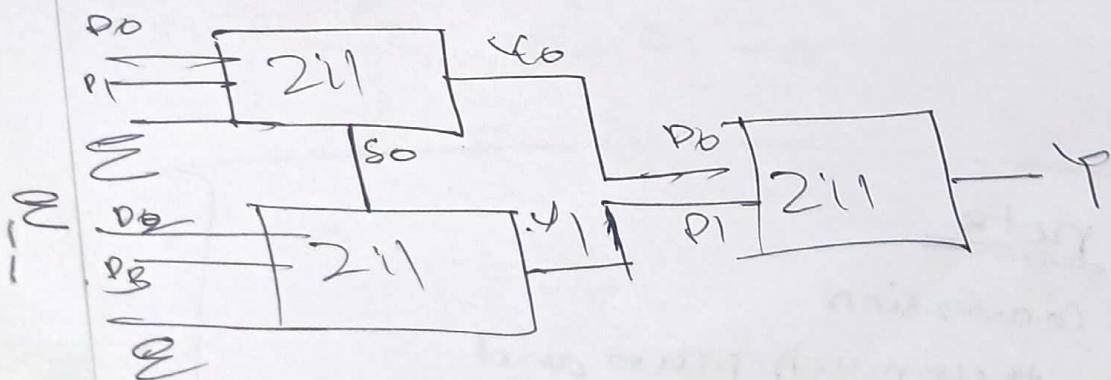
$$y=1$$

$$n=2^4$$

$m=4 \Rightarrow$ select lines.

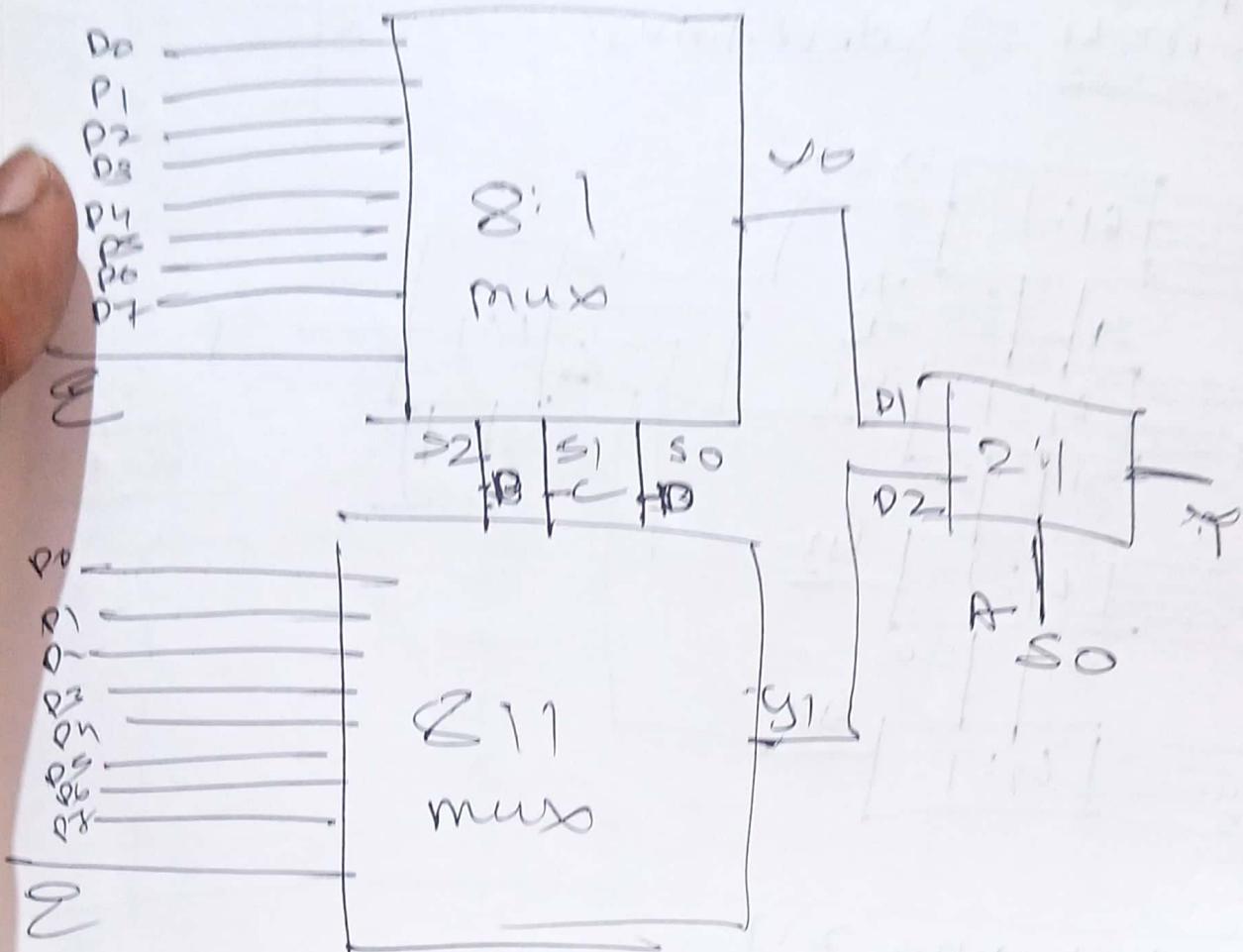


4:1 using 2:1



16:1 using (R)

$$n=16 \\ m=2^4 = 16 \\ \boxed{\text{mesh}}$$



Note

Conversion

that much mux and
output that met $\underline{= 1}$
mux combine

Multiplexer

many outputs \Rightarrow one input

it is a combinational circuit has multiple outputs and single input.

Types

2:1

4:1

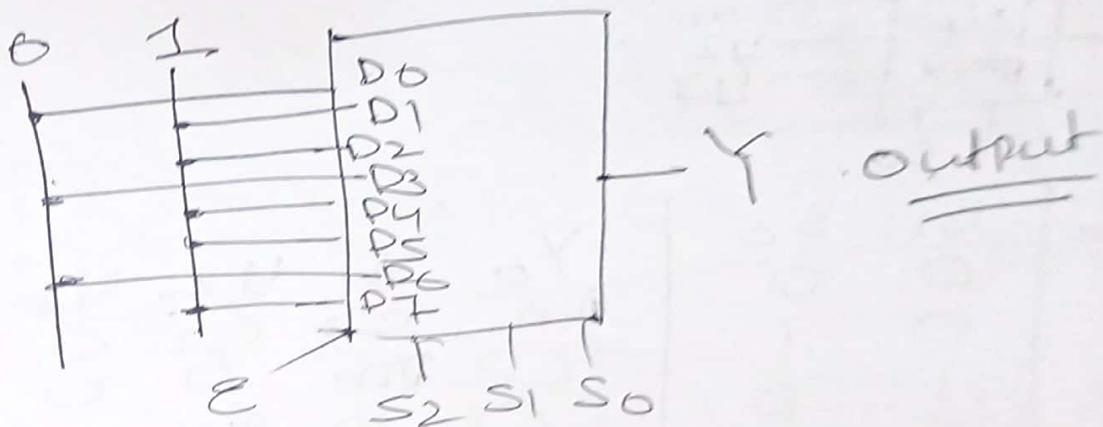
8:1

16:1

Question

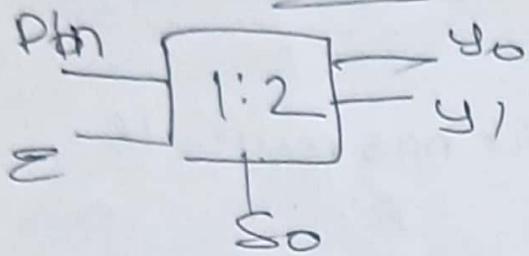
Implement ~~Multiplexer~~

$$Y = \oplus(D_1 \cdot S_1 + D_2 \cdot S_1 \cdot S_0 + D_3 \cdot S_0 + D_4 \cdot S_0 \cdot S_1 + D_5 \cdot S_0 \cdot S_1 \cdot S_2 + D_6 \cdot S_2 + D_7 \cdot S_2 \cdot S_1 + D_8 \cdot S_2 \cdot S_1 \cdot S_0)$$

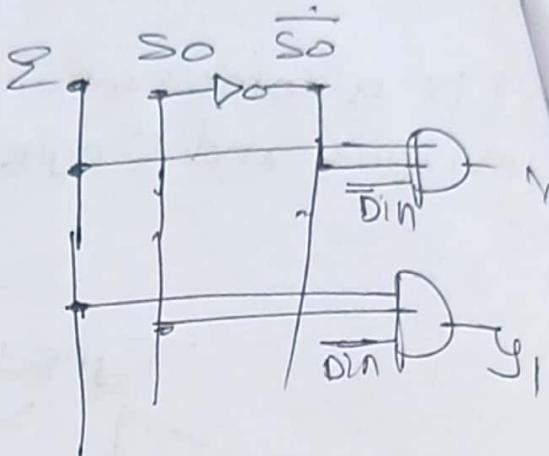


Dmux

1:2



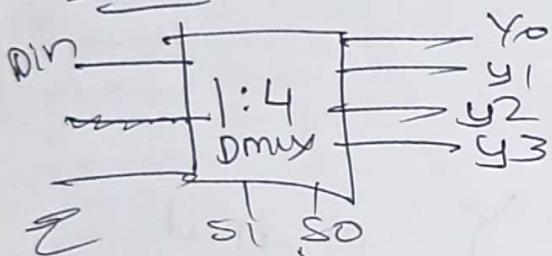
Σ	S_0	Output
0	0	$y_0 \mid y_1$
0	1	0
1	0	D_{in}
1	1	0



$$Y_0 = \Sigma \bar{S}_0 D_{in}$$

$$Y_1 = \Sigma S_0 D_{in}$$

1:4



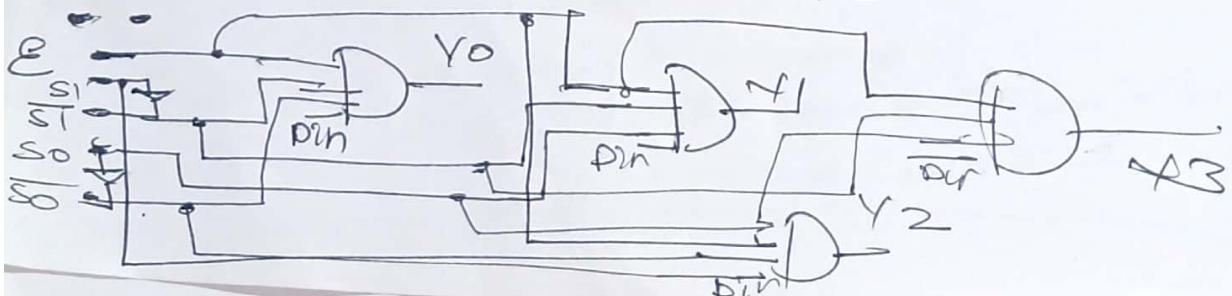
Σ	S_1	S_0	y_0	y_1	y_2	y_3
0	0	0	Din	0	0	0
0	0	1	0	Din	0	0
1	1	0	0	0	Din	0
1	1	1	0	0	0	Din

$$Y_0 = \Sigma \bar{S}_1 \bar{S}_0 D_{in}$$

$$Y_1 = \Sigma \bar{S}_1 S_0 D_{in}$$

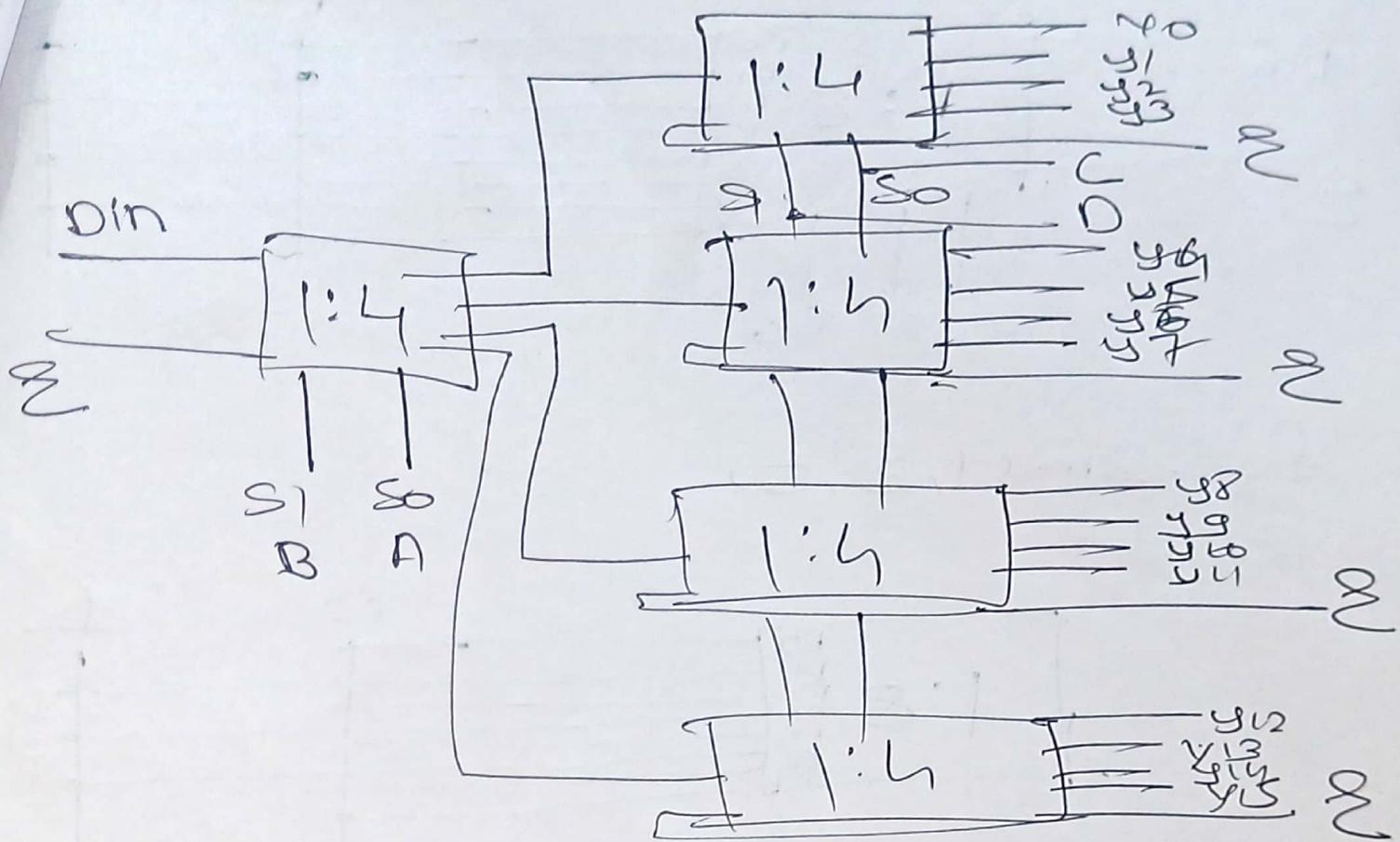
$$Y_2 = \Sigma S_1 \bar{S}_0 D_{in}$$

$$Y_3 = \Sigma S_1 S_0 D_{in}$$

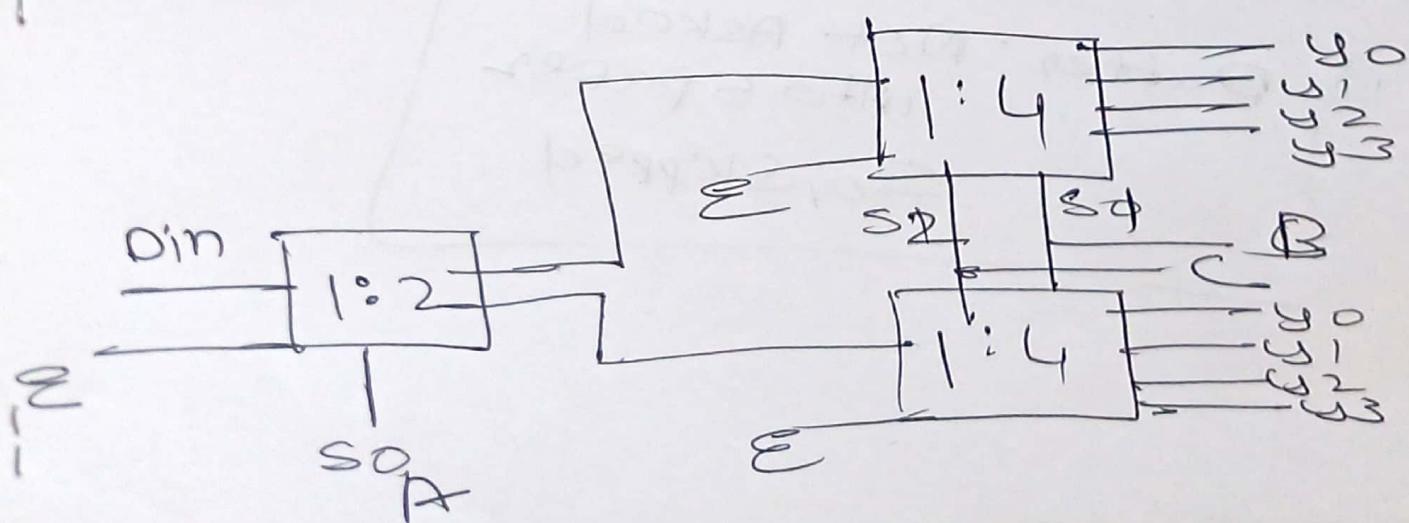


1:8 using 1:4

1:16 Demux using 1:4



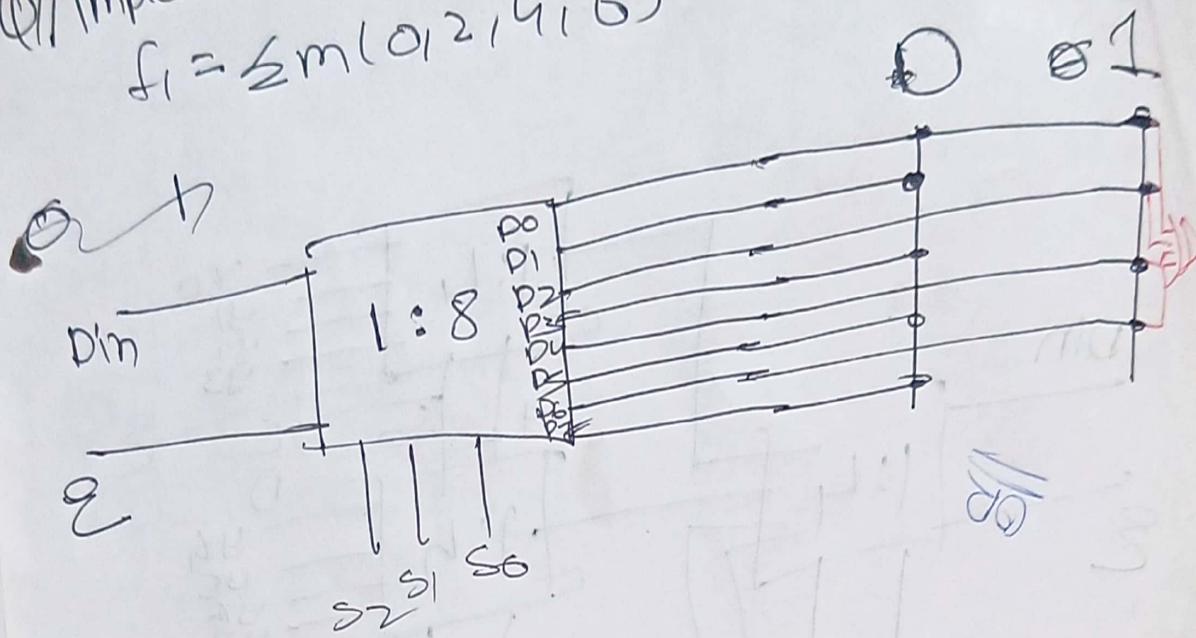
1:8 Demux using 1:4



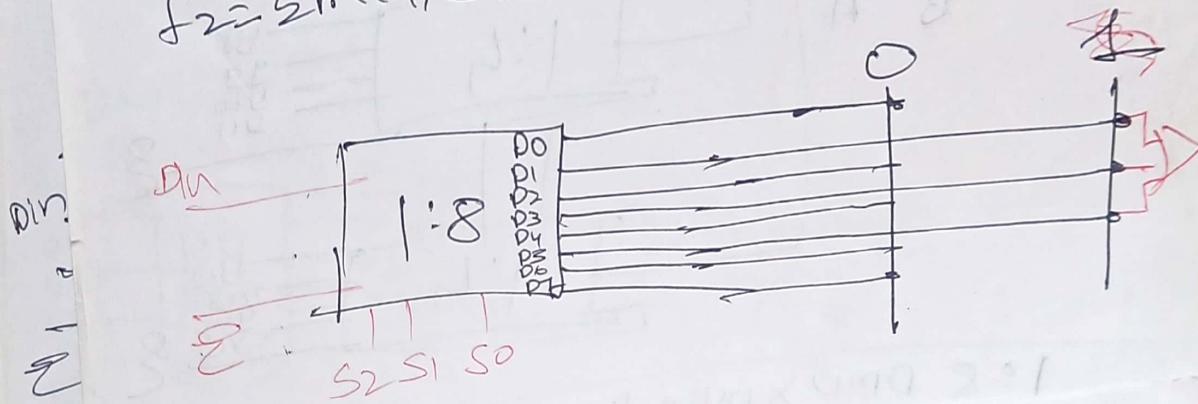
DMUX

Q1 Implement Demultiplexer
 $f_1 = Sm(0_1, 4, 6)$

(Wmerles)



$$f_2 = Sm(1, 3, 5)$$



necessity of Demultiplexers

- | * Connecting single source to several destinations
- | * to transmit several data through single transmission line
- | * Generates multiple outputs -
- | * It's efficient in communication
- | * Converts Digital to Analog

Buffer option = not asked

S1
S2
S0
D0