

Data Converter

It is a combinational digital circuit which converts the one form of data into the other or vice-versa is called as a data converter.

Necessity of Data converters

- It is often necessary that before processing the analog data by a digital system, it should be changed to an equivalent digital form.
- ALSO after processing the data, it may be desirable that the final result obtained in the digital form be converted back to the analog form.
- Therefore, data converters are necessary in digital systems.

* Give classification of Data converters.



Data converters

Digital \downarrow to Analog

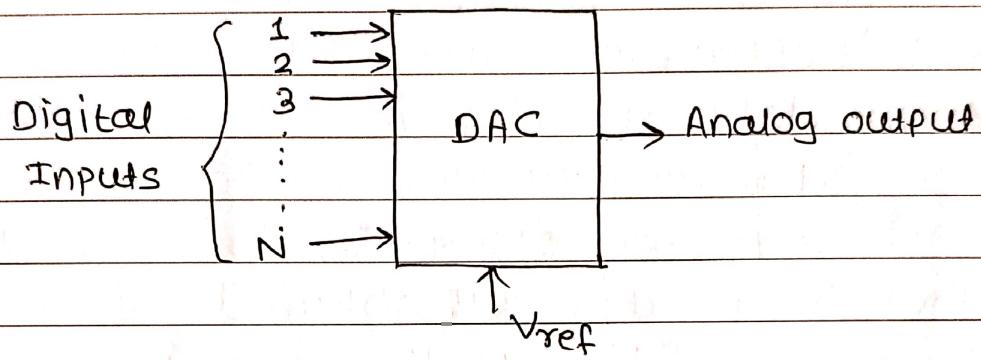
- weighted Resistor DAC
- R-2R ladder DAC

Analog \downarrow to Digital

- single slope ADC
- Dual slope ADC
- Successive Approximation ADC
- Counter type ADC
- Flash type ADC

* Draw block diagram of DAC.

→ DAC: The combinational logic system which converts the analog sig digital signal into analog signal is called digital to analog converter.



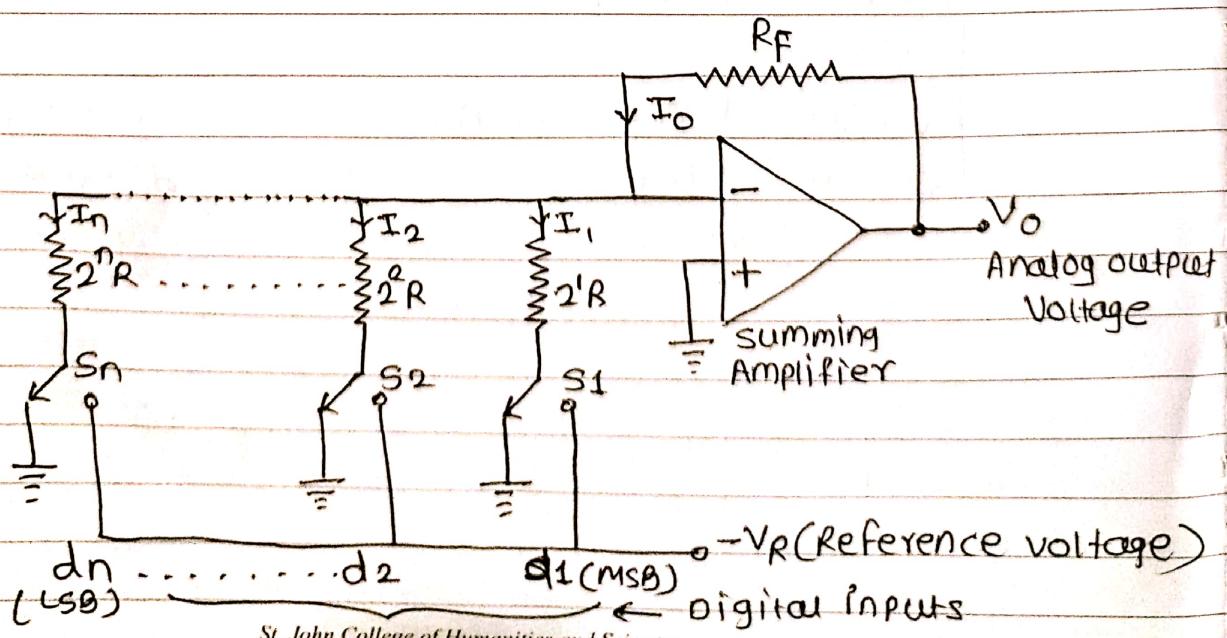
* List types of DAC.

→ DAC is categorized into two types

- 1) Binary weighted resistor DAC
- 2) R-2R Ladder DAC

* Explain working of Binary weighted Resistor DAC with diagram.

→



- It uses a network of binary weighted resistors and op-amp summing amplifier.
- The resistors $2^0 R = 2R$, $2^1 R = 4R$, ... $2^n R$ are form the network of binary weighted resistors.
- Depending upon the positions of various switches, the currents I_1, I_2, \dots, I_n will start flowing through the weighted resistors.
- Assuming the op-amp to be an ideal, the output current I_o can be expressed as

$$I_o = I_1 + I_2 + \dots + I_n$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{4R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

The output voltage V_o is given by

$$V_o = I_o R_F$$

$$= \frac{V_R}{R} \cdot R_F [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

$$\text{If } R_F = R \quad \therefore \frac{R_F}{R} = 1$$

$$\therefore V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

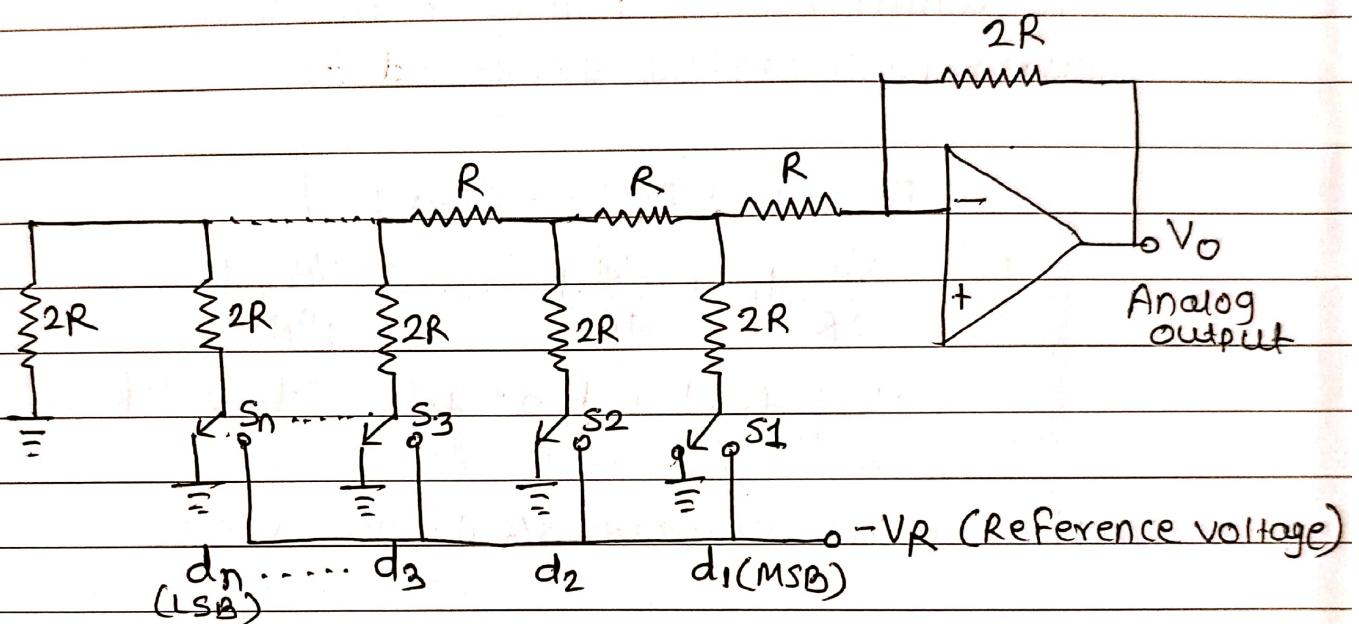
Advantages: Simple implementation
Easy computations.

Disadvantages:

- The accuracy depends on accuracy of resistors used.
- It requires a wide range of resistor values.
- It has poor resolution.

* Explain working of R-2R ladder DAC with diagram.

→ - This type of DAC also has a resistive network to produce binary weighted currents but uses only two values of resistors, namely R and $2R$.

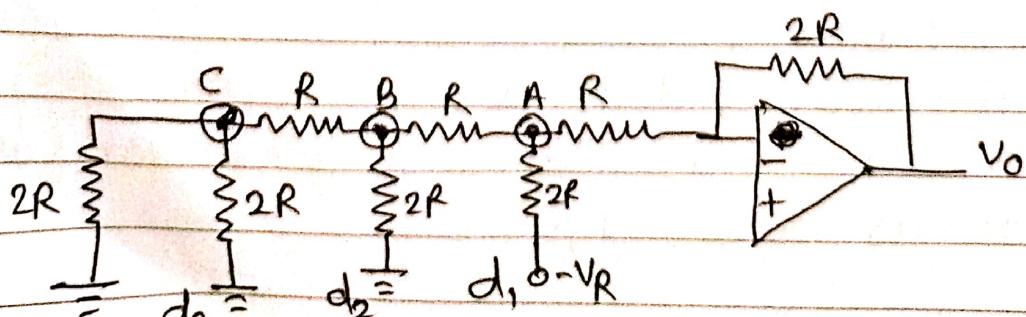


- It consists of R-2R ladder network and op-amp inverting amplifier.

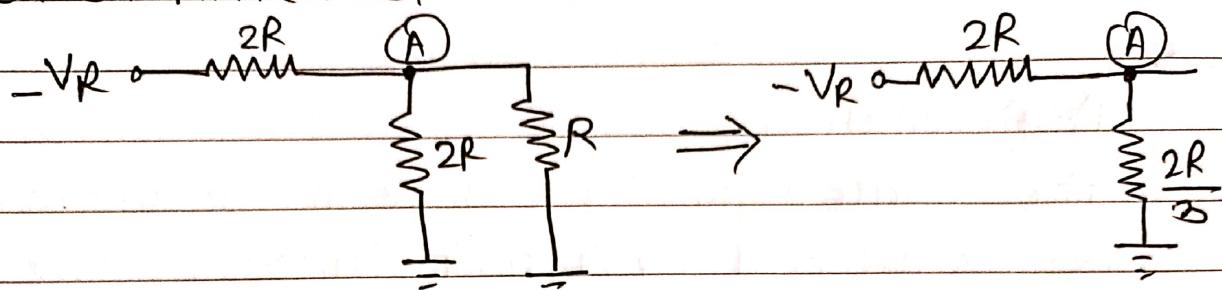
- The resistor $2R$ can either be connected to the reference voltage ($-VR$) or ground through switches.
- To understand the working of this, let consider 3 bit input $d_1, d_2, d_3 = 100$.

as $d_1 = 1 \rightarrow$ it is connected to $-VR$

$d_2, d_3 = 0 \rightarrow$ connected to Ground.



final simplified equivalent circuit is



The voltage at node 'A' is given by

$$V_A = \frac{\frac{2R}{3}}{2R + \frac{2R}{3}} \times (-VR)$$

$V_A = -\frac{VR}{4}$

∴ The output voltage of an op-amp inverting amplifier is given by

$$V_O = -\left(\frac{R_F}{R}\right)V_I = -\left(\frac{2R}{R}\right)\left(-\frac{VR}{4}\right) = +\frac{VR}{2}$$

For a digital input of $d_1 d_2 d_3 = 100$, the analog output produced is $\frac{VR}{2}$

Advantage : Easily expanded

: Only two values of resistors.

: High accuracy and stability

Disadvantages : It requires two resistors per bit.

: Circuit becomes more complex as compared to binary weighted resistor.

* List various specifications of DAC.

1) Resolution :

The smallest possible change in the analog output that is affected by a unit change (i.e. one bit) in digital input is known as the resolution of DAC.

$$\% \text{ Resolution} = \frac{V_{FS}}{2^n - 1} \times 100, \text{ where } V_{FS} \rightarrow \text{Full scale voltage}$$

2) Linearity :

The linearity of DAC is a measure of the precision with which the linear input output relationship is satisfied.

3) Accuracy :

The accuracy of DAC is defined as the closeness of the output analog voltage to the expected

4) Settling time :

It is defined as the amount of time necessary to settle to an analog output value of desired accuracy i.e. within $\frac{1}{2}$ LSB of the final value after the digital input has changed.

5) Temperature stability :

The analog output of DAC should not change due to change in temperature.

6) Speed : It is defined as the time needed to perform a conversion from digital to analog.

① Calculate the analog output for 5-bit weighted resistor type DAC for inputs:

i) 10110 ii) 10001 Assume logic 1 = 10V.

Given

$$\text{Logic 1} = 10V \Rightarrow V_{FS} = V_R$$

i) Input 10110

$$V_o = V_{FS} [d_1 2^1 + d_2 2^2 + d_3 2^3 + d_4 2^4 + d_5 2^5]$$

$$= 10 [1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 + 0 \times 2^5] \\ = 6.875V$$

$$\boxed{V_o = 6.875V}$$

ii) Input 10001

$$V_o = V_{FS} [d_1 2^1 + d_2 2^2 + d_3 2^3 + d_4 2^4 + d_5 2^5]$$

$$= 10 [1 \times 2^1 + 0 \times 2^2 + 0 \times 2^3 + 0 \times 2^4 + 1 \times 2^5] \\ = 5.31V$$

$$\boxed{V_o = 5.31V}$$

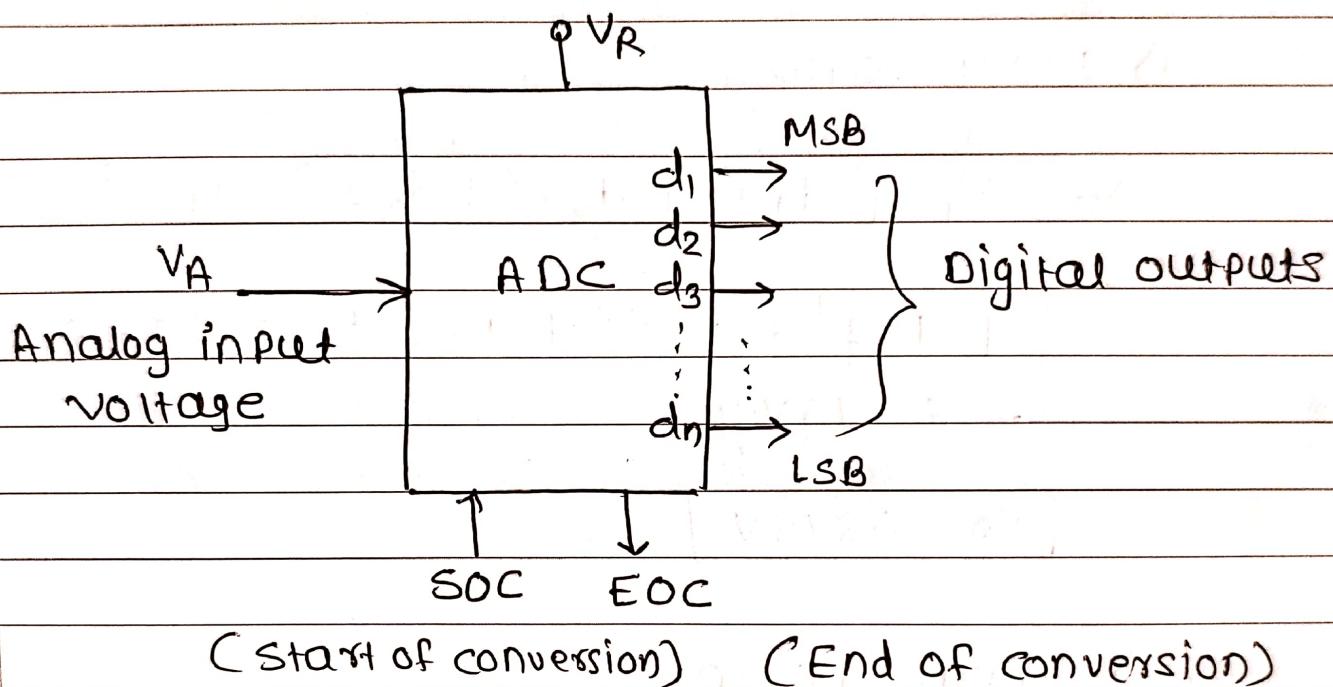
② What is the resolution in volts, for a 6-bit DAC, with +10V full scale output?

Given $V_{FS} = 10V$, $n = 6$ bit

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{10}{2^6 - 1} = \underline{\underline{0.1587V}}$$

Analog to Digital converter

The combinational logic system which converts the analog signal to digital signal is called analog to digital (ADC) converter.

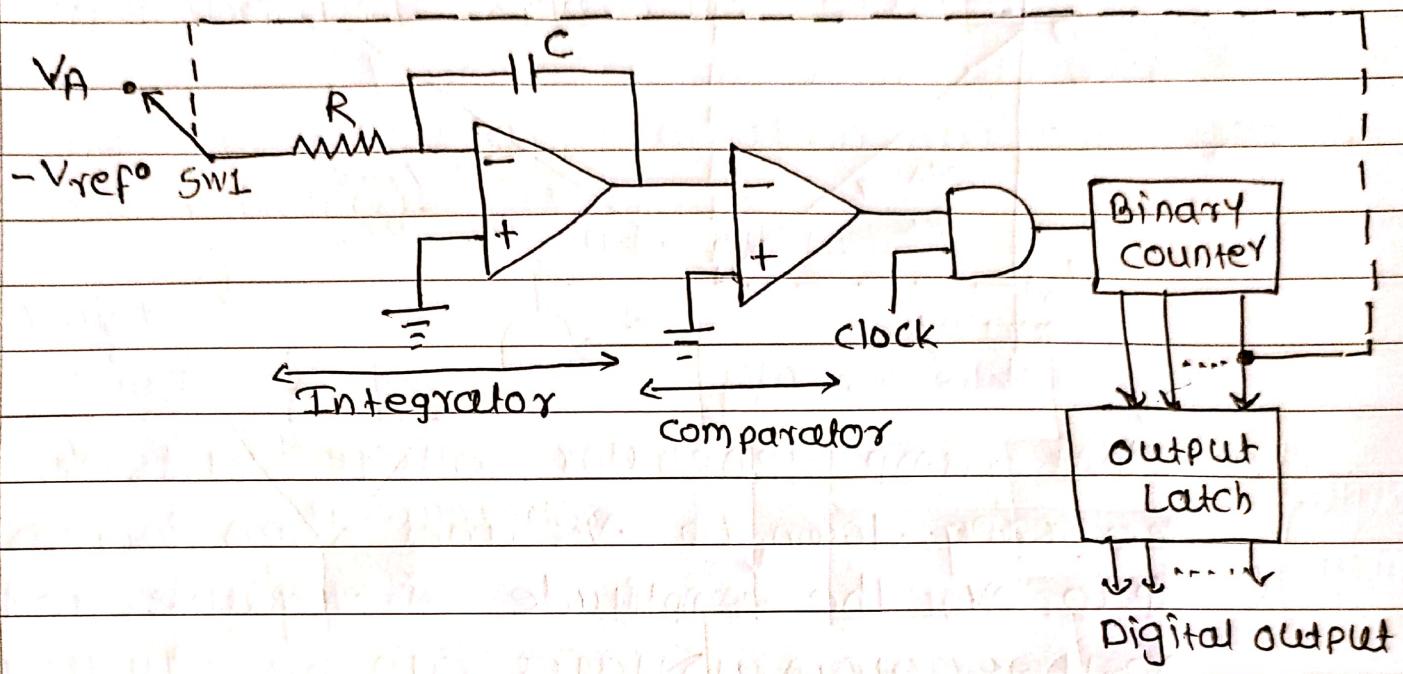


Types of ADC

- 1) Successive Approximation type ADC
- 2) Dual slope ADC.

1) Dual slope ADC

- In this, the integrator generates two different ramps, one with the known analog input voltage V_A and another with a known reference voltage $-V_{ref}$. Hence it is called as dual slope ADC.



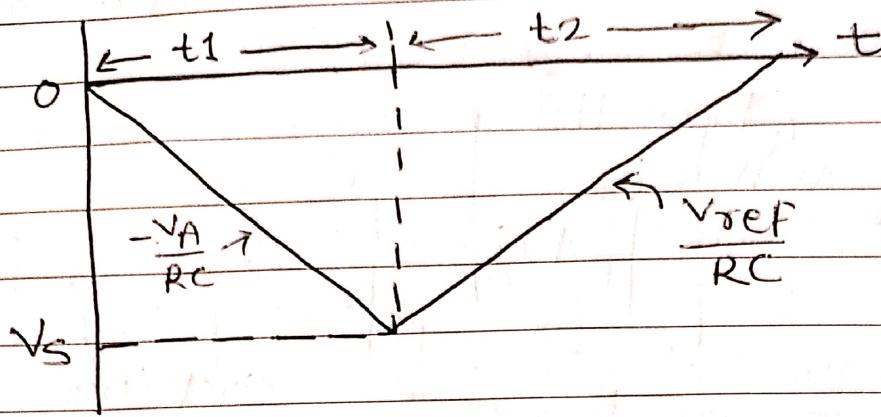
Operation

- First the analog input voltage V_A is connected to an integrator.
- The analog input voltage V_A is integrated by inverting integrator and generates a negative ramp output.
- The negative ramp continues for a fixed time period t_1 .

$$V_S = -\frac{V_A}{RC} \times t_1$$

- When the counter reaches the fixed count at time period t_1 , the binary counter resets to 0000 and switches the integrator input to a negative reference voltage $-V_{ref}$.

$$V_S = \frac{V_{ref}}{RC} \times t_2$$



since ramp generator voltage starts at 0V, decreasing down to $-V_s$ and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as

$$\frac{V_{ref}}{RC} \times t_2 = -\frac{V_A}{RC} \times t_1$$

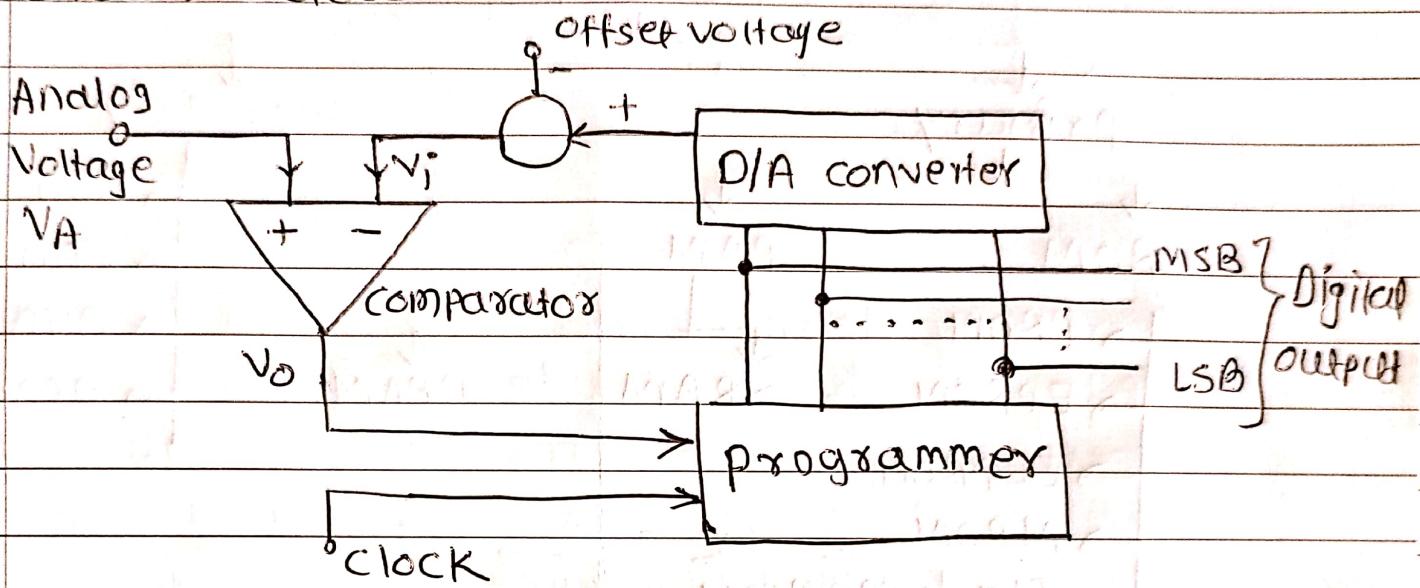
$$t_2 = -t_1 \frac{V_A}{V_{ref}}$$

$V_A = \pm V_{ref} \times \frac{t_2}{t_1}$

Thus the unknown analog input voltage V_A is proportional to the time period t_2 .

* Draw the circuit of successive approximation type ADC and explain its working.

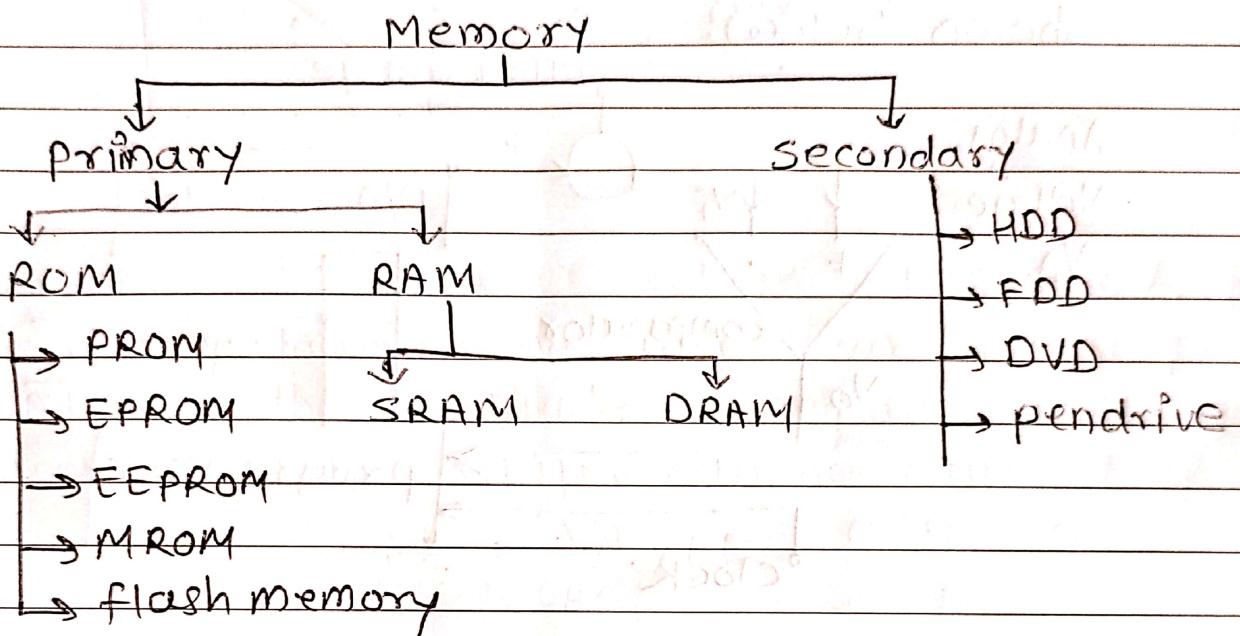
→ The successive approximation A/D converter is shown below:



- An analog voltage (V_A) is constantly compared with voltage V_i , using a comparator.
- The output produced by comparator (V_o) is applied to an electronic programmer.
- If $V_A = V_i$ then $V_o = 0$ & then no conversion is required. The programmer displays the value of V_i in the form of digital O/P.
- But if $V_A > V_i$, then value of V_i is increased by 50% of earlier value.
- If $V_A < V_i$, then V_i is decreased by 50% of earlier value.
- This new value is converted into analog form by D/A converter so as to compare it with V_A again. This procedure is repeated till we get $V_A = V_i$.

Memory

* Give classification of memory.



* Compare RAM and ROM memory.

RAM	ROM
- RAM stands for Random Access Memory	- ROM stands for Read only memory
- Both read & write operations can be performed	- only read operation can be performed.
- These are volatile memories	- These are non-volatile memories.
- Types: SRAM, DRAM	- Types: PROM, EPROM, EEPROM
- Applications: computer, calculators	- Applications: computer, Microprocessor.

* compare static RAM and Dynamic RAM (SRAM vs DRAM)

→	Static RAM	Dynamic RAM
	<ul style="list-style-type: none">- Each SRAM cell is a flip flop.- Less number of memory cells/unit area.- More no. of components per cell.- Does not require refreshing.- Faster memories.- Power consumption is less.	<ul style="list-style-type: none">- A dynamic RAM cell consists of a MOSFET and a capacitor.- More number of cells/unit area.- Only two components per cell.- require refreshing.- slower memories.- More power consumption.

* compare volatile and non-volatile memory

→	Volatile Memory	Non-Volatile Memory
	<ul style="list-style-type: none">- Information stored is lost when power is switched off.- All RAM's are volatile memories.- Stored information is retained as long as power is on.- Used for temporary storage of information.	<ul style="list-style-type: none">- Information stored is retained even after power is switched off.- ROM, EPROM, are non-volatile memories.- No effect of power, on stored information.- Used for permanent storage of information.

* compare EPROM and Flash memory.



EPROM

Flash

- can be erased only byte by byte by giving electrical pulses.
- Byte programmable.
- Cost is more
- programming is ~~faster~~, slower.

- can be erased block by block by giving electrical pulses.
- Block programmable
- cost is less
- programming is faster.

* Compare EEPROM and EPROM



EEPROM

EPROM

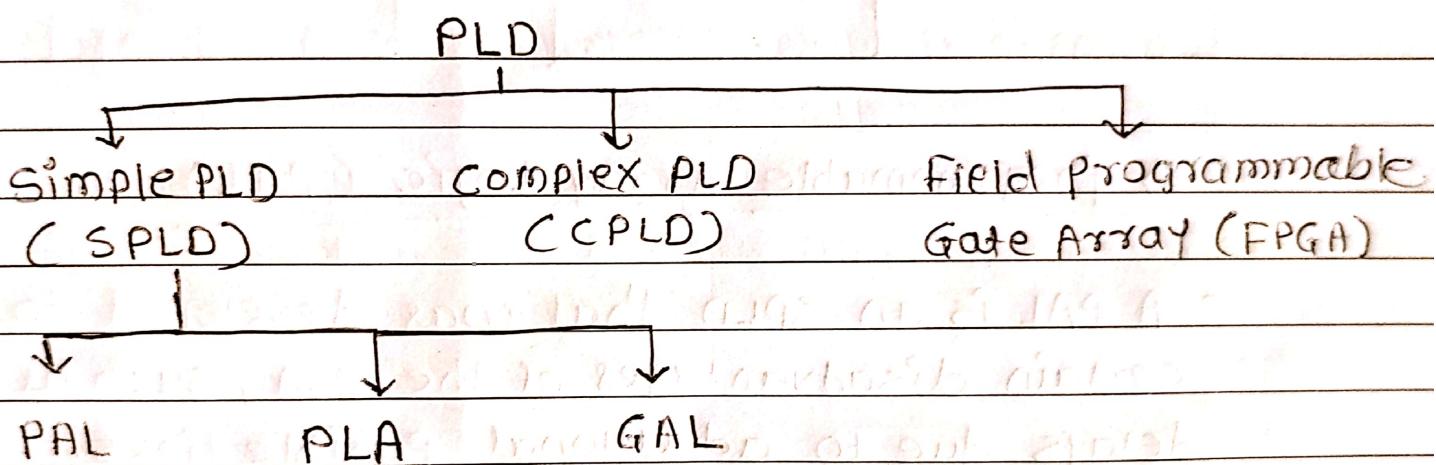
- It stands for Electrically Erasable programmable Read Only Memory.
- It can be programmed & erased electrically.
- can be erased in a small time of 10 ms.
- Low density
- Expensive than EPROM.

- EPROM stands for Erasable programmable Read only memory
- It cannot be erased electrically and requires UV rays to erase.
- Requires 20 to 30 min. for erasing.
- High density
- cheaper than EEPROM

Programmable logic devices (PLD's)

- PLD is an electronic component used to build reconfigurable digital circuits.
- These are the integrated circuits and consists of an array of AND & OR gates.

Classification of PLD's



PAL: programmable Array logic

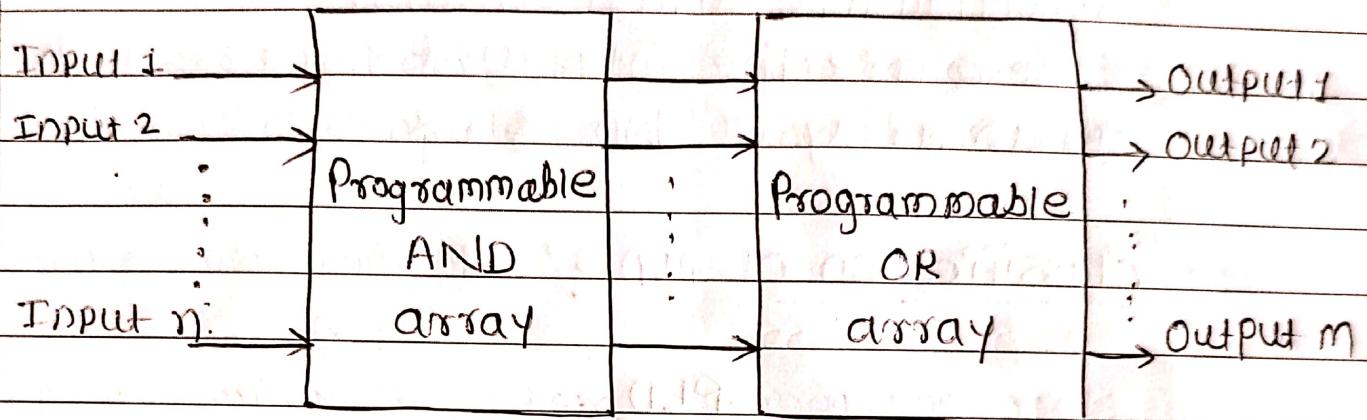
PLA: programmable logic Array

GAL: Generic logic Array.

1) Programmable Logic Array (PLA)

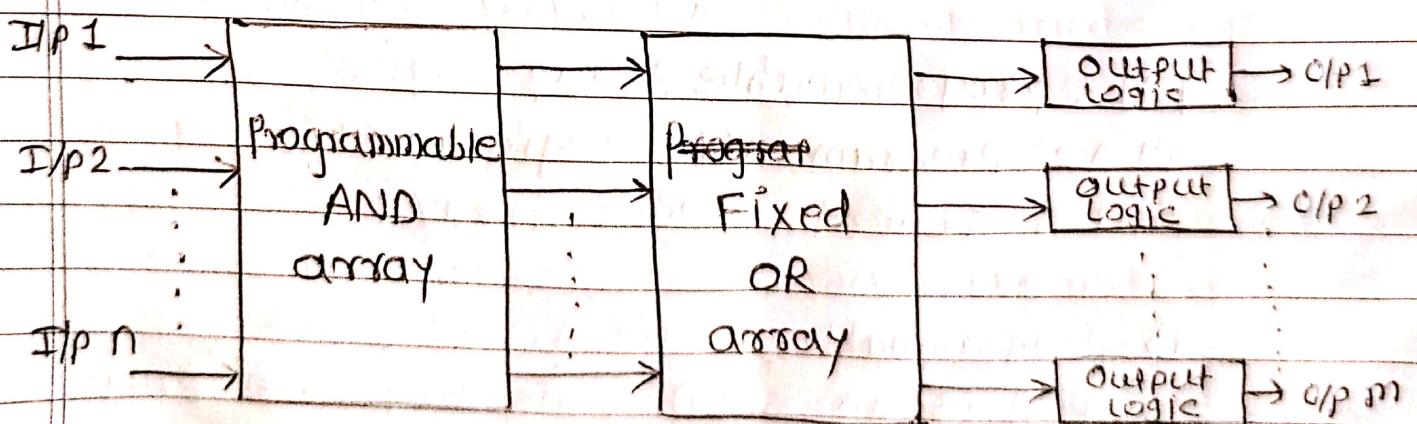
- A PLA is an SPLD consisting of a programmable AND array and a programmable OR array.
- Both the arrays are programmable.
- The PLA is also called as FPLA (Field programmable logic Array).

Block diagram of PLA



2) Programmable Array Logic (PAL)

- A PAL is an SPLD that was developed to overcome certain disadvantages of the PLA, such as longer delays due to additional fusible links.



- In PAL, AND array is programmable and OR array is fixed.

3) Generic Array Logic (GAL)

- The GAL has a programmable AND array and a fixed OR array with programmable output logic.
- GAL is reprogrammable and it has programmable output configurations.

