

Unit IV : Sequential Logic Circuit

(Weightage - 18 marks)

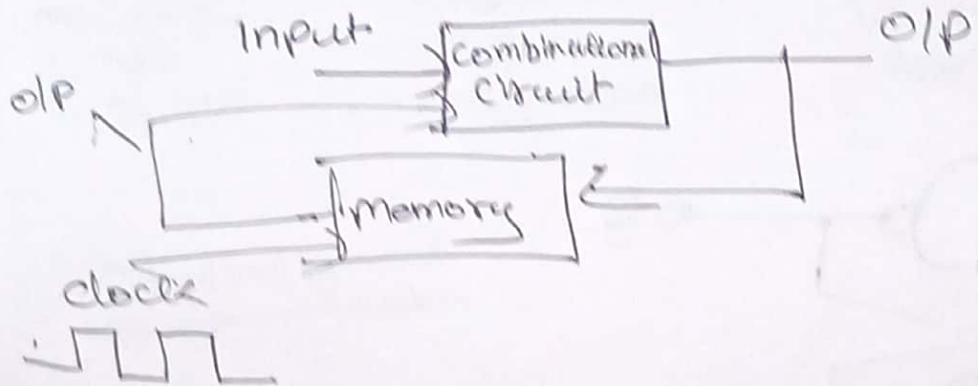
Pranjal Sare (SY-comps)

Digital Techniques
(22320)

Introduction

Basic Terminologies - (Viva)

- ① In sequential logic circuit output depends on present input as well as previous output.
- ② In order to store previous output we need a memory element in sequential circuit.
- ③ In sequential logic circuit, clock signal is used to provide timing and achieve synchronization we need clock signal.



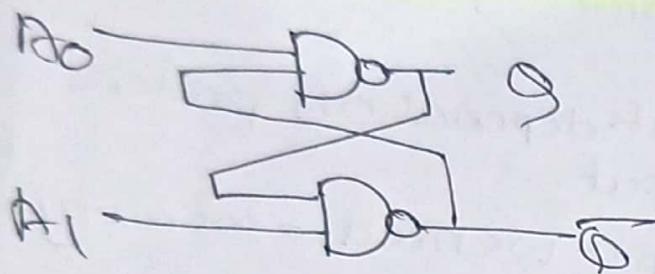
- ④ Difference between Sequential and Combinational circuit

<u>Parameter</u>	<u>Combinational</u>	<u>Sequential</u>
<u>Output depends</u>	Present input	Present input + Previous output
<u>Memory</u>	If it is not required as it does not stores previous output.	Required.
<u>Clock I/P</u>	Not Required	Required / Necessary
<u>Feedback</u>	Not present	Present
<u>Design</u>	Easy and simple	Complex
<u>Speed</u>	Faster	Slower
<u>Storage</u>	Memory element not reqd.	Memory element required
<u>Example</u>	Full Adder, Subtractor, Encoder, Decoder	Multiplexer, shifter, register, counter

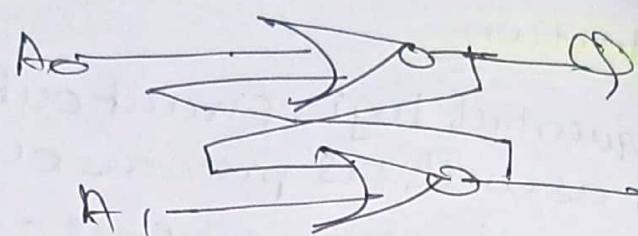
4.1 Basic memory cell = R-S latch using NAND & NOR

Basic (one bit) unit/memory cell.

NAND

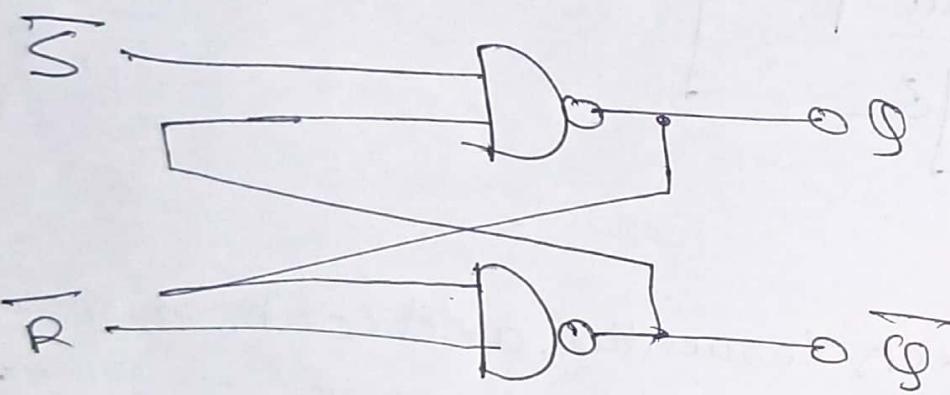


NOR

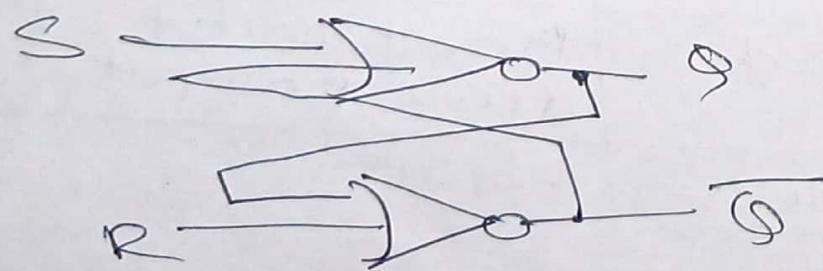


R-S latch
using
NAND

II

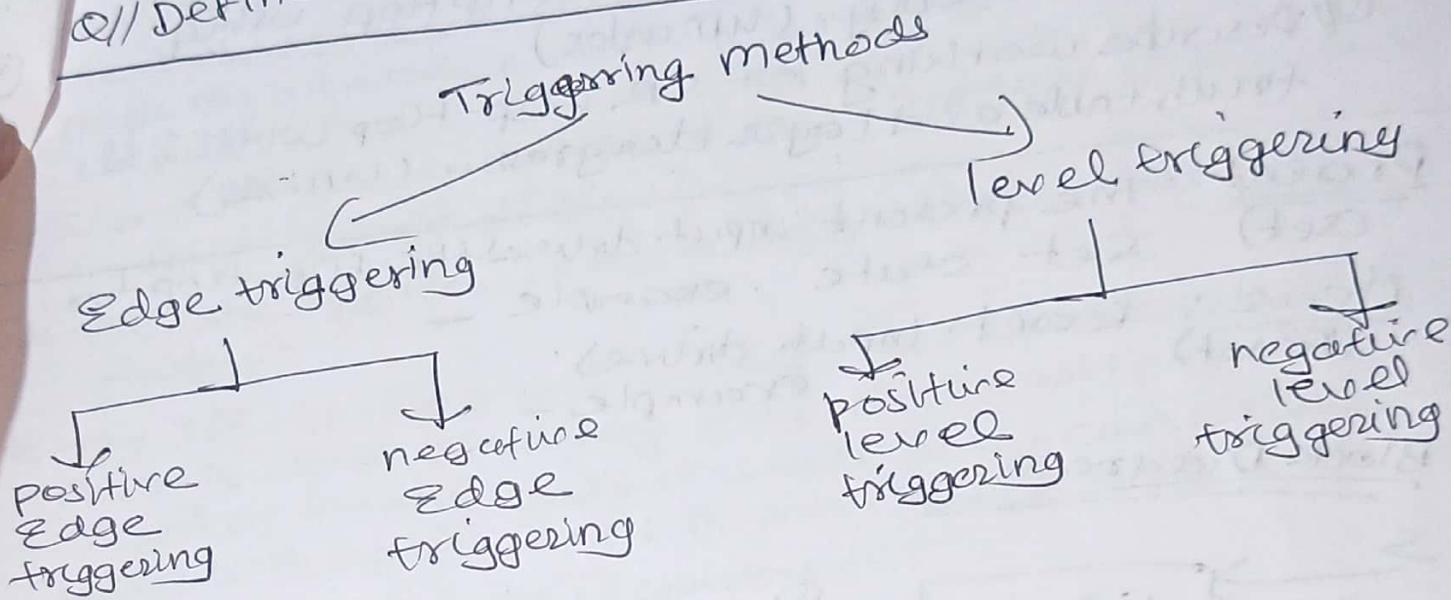


NOR

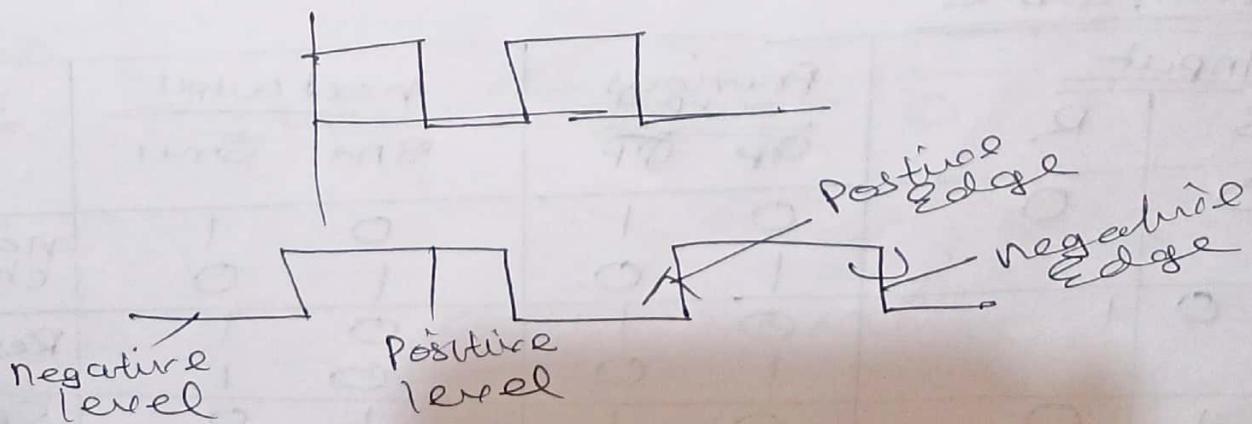
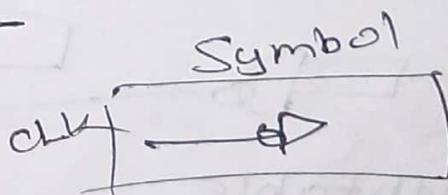
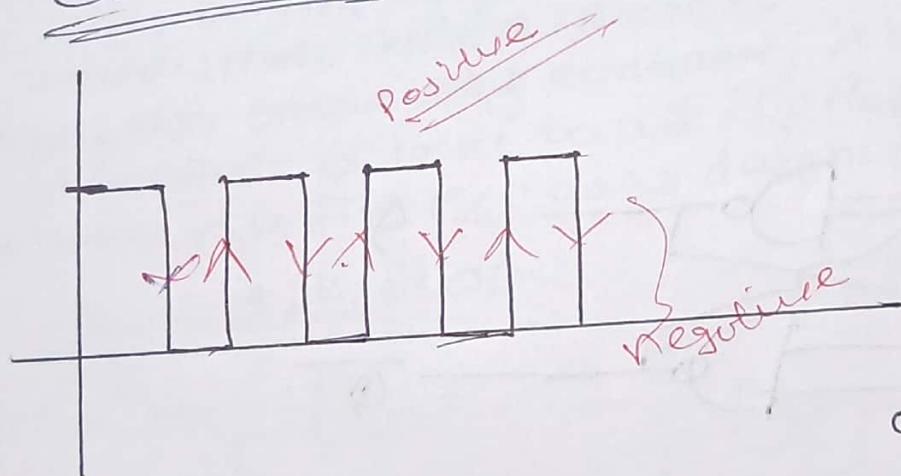


Q1/ List triggering methods using for triggering flip-flop. (2marks)

Q2/ Define triggering. Enlist methods. (2marks)



Clock signal



4.3 S-R flipflops, clocked SR flipflop and its working, advantages and disadvantages of S-R flipflop.

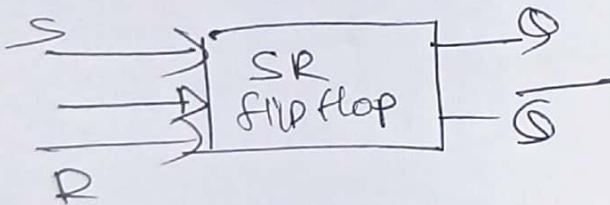
Questions

- Q1/ State the function of present and clear in flip flop. (2marks)
- Q2/ Describe the operation of S-R flip flop using NAND gate only. (unmarks)
- Q3/ Describe working of SR flip-flop with its truth table and logic diagram. (unmarks)

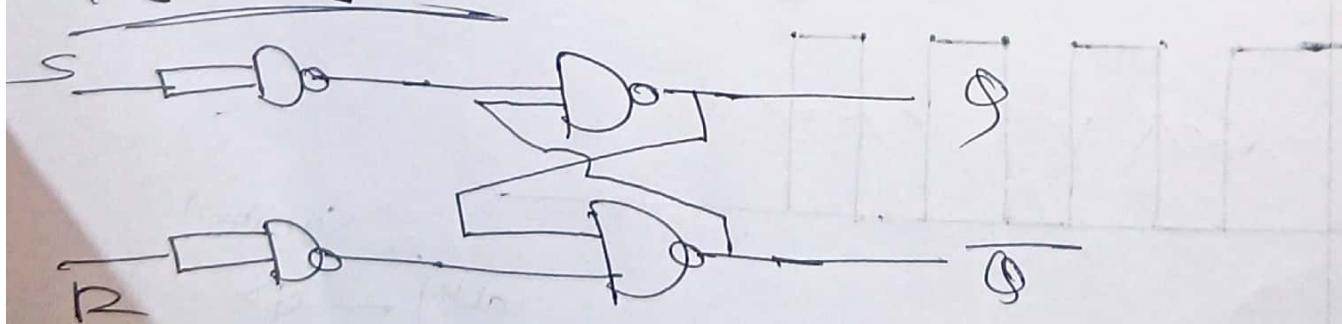
Present: The present input drives the flip-flop to (Set) set state. example - $01 \Rightarrow 10$

Clear: Reset input drives' (Reset) example - $10 \Rightarrow 01$

Block Diagram



Logic Diagram



Truth table

Input		Previous output	Next output	State
S	R	Q _P Q-bar _P	Q _{n+1} Q-bar _{n+1}	
0	0	0 1	0 1	
0	1	1 0	1 0	no change
1	0	0 1	0 1	Reset
1	1	1 0	1 0	Set

	O	I	X	X	forbidden
	I	O	X	X	prohibit Race
<u>working</u>	Set	Set	High to burst	case	Avoided
	Re Reset		Reset	Reset	not possible

↓ Theff is set Reset flip flop.

* The SR flip flop is also known as the gated or clocked SR latch.

* The clocked SR latch or SR flip flop temporarily stores or holds the information until it is needed in digital circuits -

*'S' and 'R' are two inputs to flip-flop. It has two outputs 'Q' and ' \bar{Q} '.

* The SR flip flop is a storage element with only one bit.

- * the SR flip-flop is a gated SR flip-flop with a clock input circuitry that does not prevent illegal or invalid output states that can arise when both inputs S and R are equal logic levels.

* NAND gate SR latch is constructed

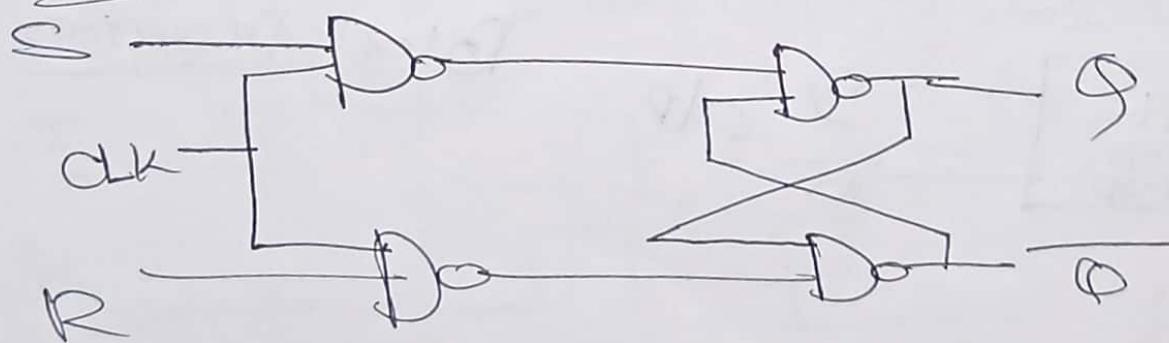
* It is also known as RS Larch.

* When both inputs of SR is high '1' then the indeterminate state is called 'Race'.

In other programming environment, it is required to assign determinate outputs to all flip flop conditions.

Hence SR flip flop was designed.

Clocked flip flop



Drawback of SR flip flop

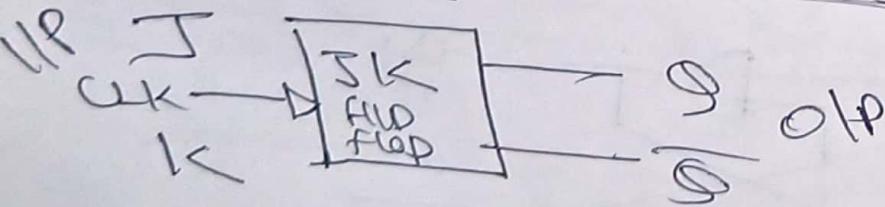
- * Both inputs should not be high when clock is high.
This is considered an invalid input condition.
- * Resulting output is not predictable if this condition occurs.
- * Uncertainty in state of S-R flip-flop, $S = R = 1$ can be eliminated using J-K flip flop.

4.4 : Clocked JK flip flop with present and clear, race around conditions in JK flip flop, master slave JK flip flop. D and T flip flop

Questions

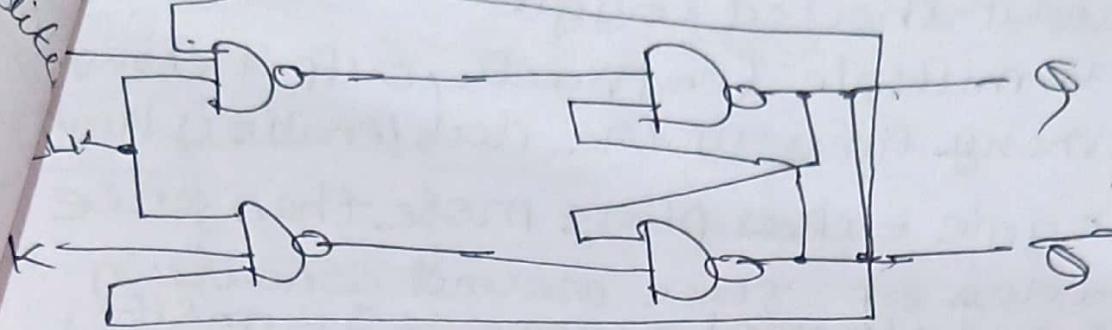
- (Q) Draw symbol and write truth-table for T flip flop.
- (Q) Write Truth-table of D-type flip flop. (2m)
- Imp (Q) Symbol and truth-table for D & T flip flop. (2m)
- (Q) Describe the working of J-K flip-flop and state the race around condition.
- (Q) Describe working of JK flip flop with truth table and logic diagram.
- (Q) Draw master slave JK flip flop and explain its operation.

JK flip flop (See kili by)



Block Diagram

Logic Diagram



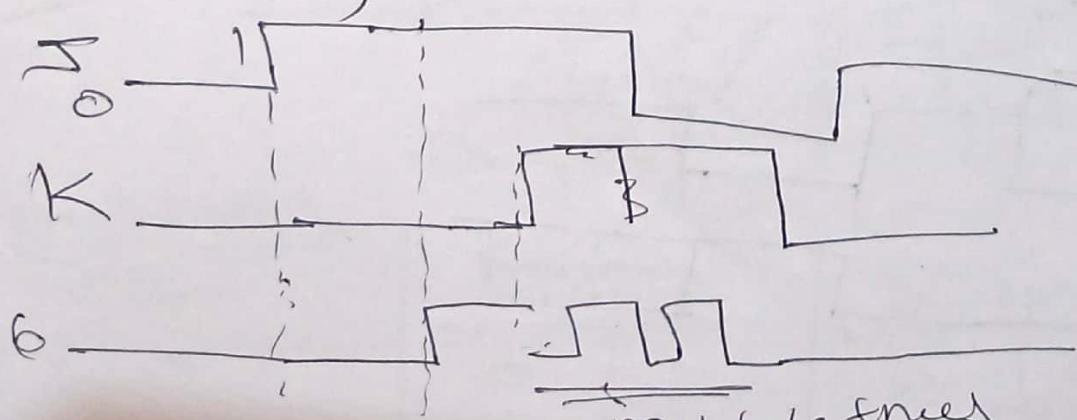
Truth Table

<u>Input</u>	<u>Previous output</u>	<u>Present output</u>	<u>State Comment</u>
J K 0 0	0 1	0 1	no change
0 1	0 1	0 1	Reset
1 0	0 1	1 0	Set
1 1	1 0	1 0	<u>Toggle</u>

Working same as truth table.

Race around condition

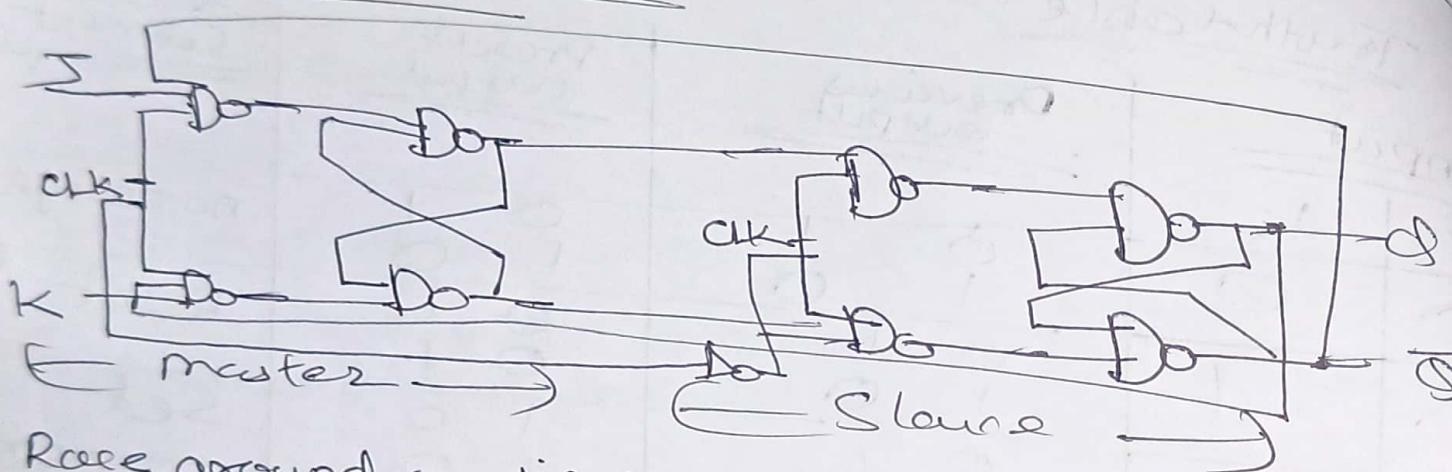
Race around condition occurs in J-K flip flop only when $J=K=1$, and clock/enable is high - (clock 1)



multiple edges
fogging enters prees is
this is race around.

- In JK flip flop when $J=K=1$ when clock is high output should toggle
- But due to multiple feedback, output changes toggles many times all the clock (enable) is high.
- Thus, toggle occurs more than once called racing or race around condition. A more practical method overcome is J-K master-slave.

Master slave flip flop



Race around condition can be overcome by Master Slave JK flip flop.

When clock goes,

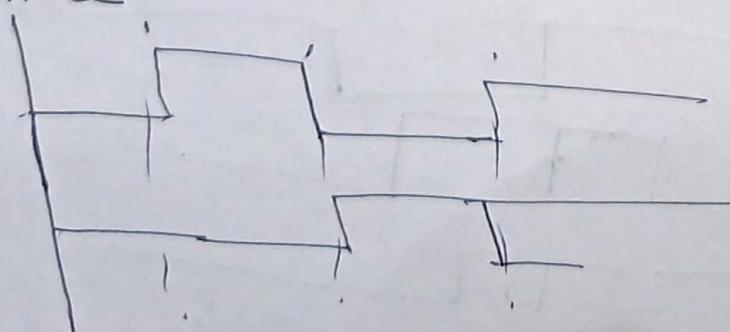
$$\begin{cases} M=0 \\ S=1 \end{cases}$$

$$\begin{cases} S=1 \\ M=0 \end{cases}$$

$$\begin{cases} M=1 \\ S=0 \end{cases}$$

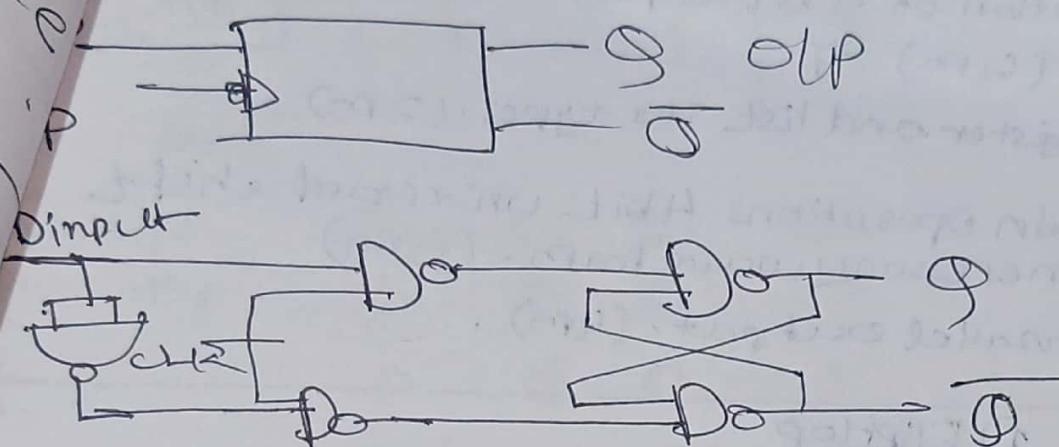
Controls each

Truth table
Same



flip flop

↳ from S-R flip flop

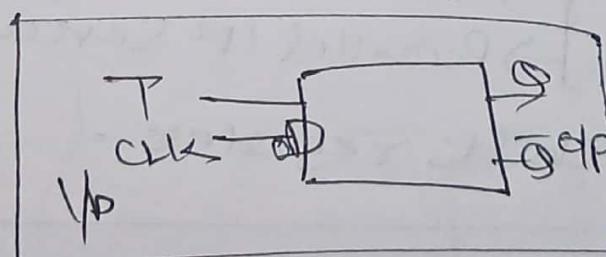


reset/switch

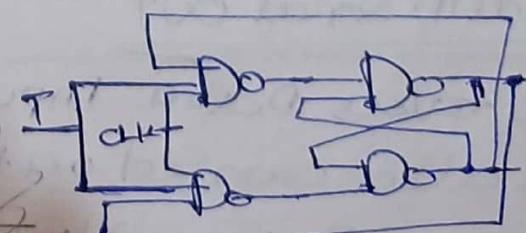
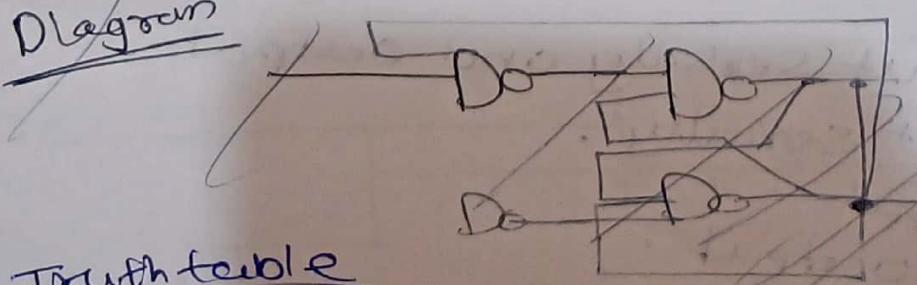
<u>Input</u>	<u>Previous output</u>	<u>Next output</u>	<u>state</u>
0	0 1	0 1	
0	1 0	0 1	Reset
1	0 1	1 0	
1	1 0	1 0	Set

T-flip flop

↳ from J-K



Diagram



Truth table

<u>Input</u>	<u>Previous output</u>	<u>next output</u>	<u>state</u>
0	0 1	0 1	no change
1	0 1	1 0	toggle

Shift Registers / Logic Diagram of 4 bit shift register

4 types, Universal Shift Register

Questions

- Q1// Describe the operation of 4 bit serial out serial in shift register. (4m)
- Q2// Define shift register and list its types. (2m)
- Q3// Draw and explain Operations 4 bit universal shift register. Draw necessary waveforms. (6m)
- Q4// Serial Input Parallel Output. (4m)

Shift register

D Flipflop

- * The binary data in a register can be shifted from one stage to another stage within the register or into or out of the register after application of clock pulses.
- * It is used in microprocessors to carry out arithmetic and logic operations.

Types

- Serial IN Serial OUT
- Parallel IN Parallel OUT
- Serial IN Parallel OUT
- Parallel IN Serial OUT

Universal shift register

Serial IN Serial OUT

It takes Data Input serially and output is also carried out serially.

Enter → Input

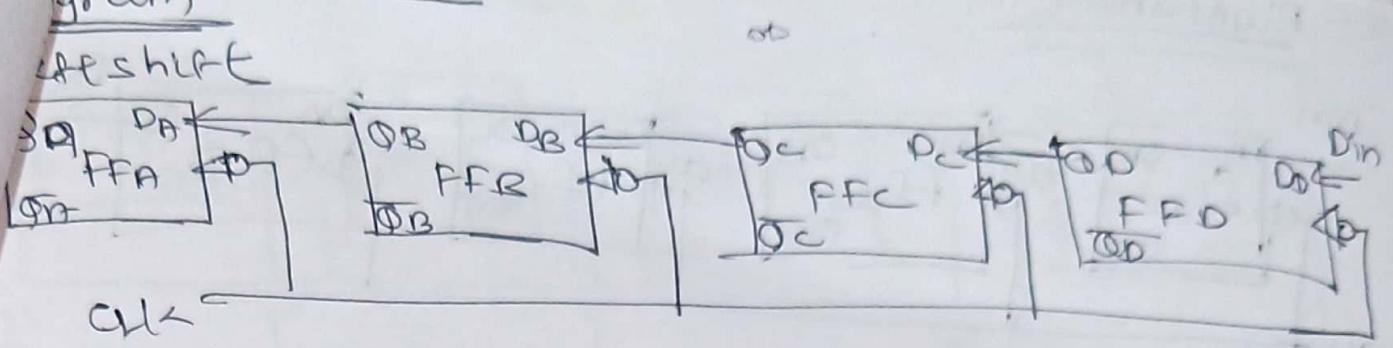
Dataout → Output

There are two types of serial IN serial out

↳ Left shift

↳ Right shift.

Flip Flop used is D-Flip flop.
CLK used - ν e edge triggered.



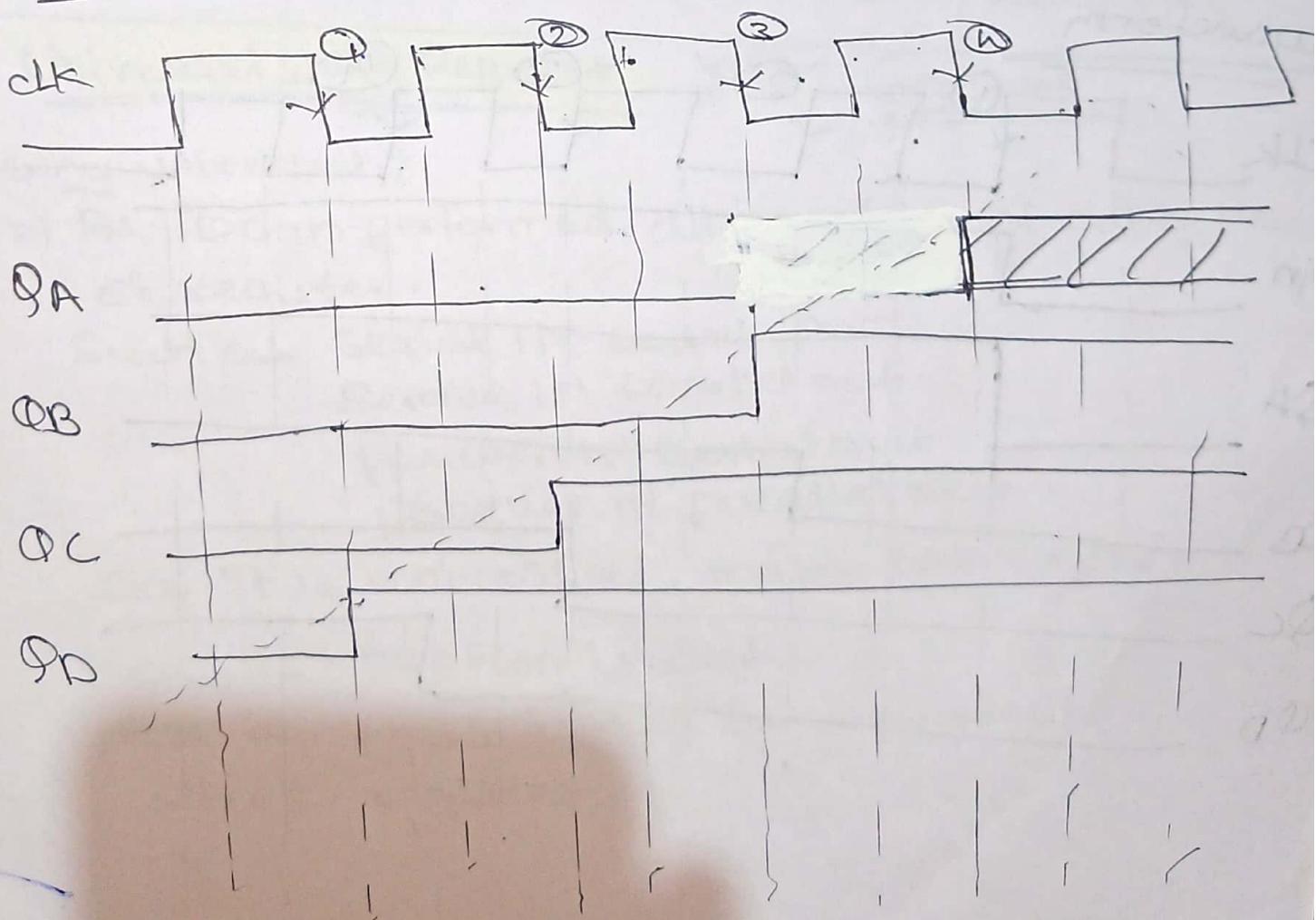
CLK

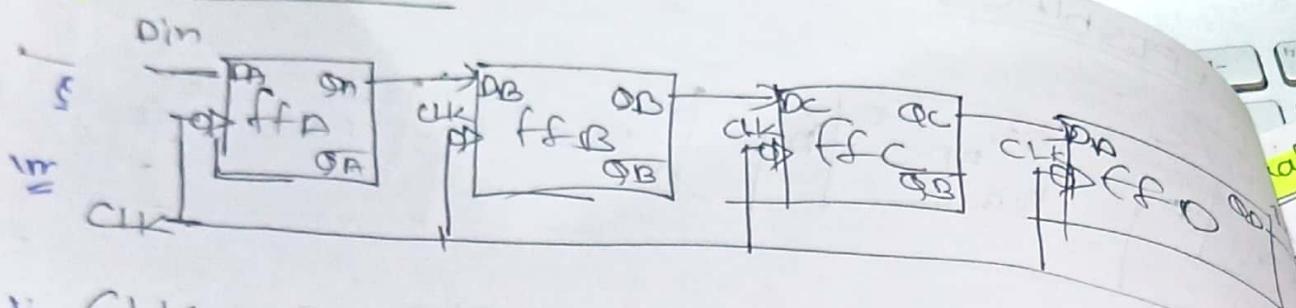
Initially

	Q_A	Q_B	Q_C	Q_D	D_{in}
Initial	0	0	0	0	0

↓ 0 0 0 1 ← 1
 ↓ 0 0 1 1 ← 1
 ↓ 0 1 1 1 ← 1
 ↓ 1 1 1 1 ← 1

Wave form





CH₄S D'in

Initially

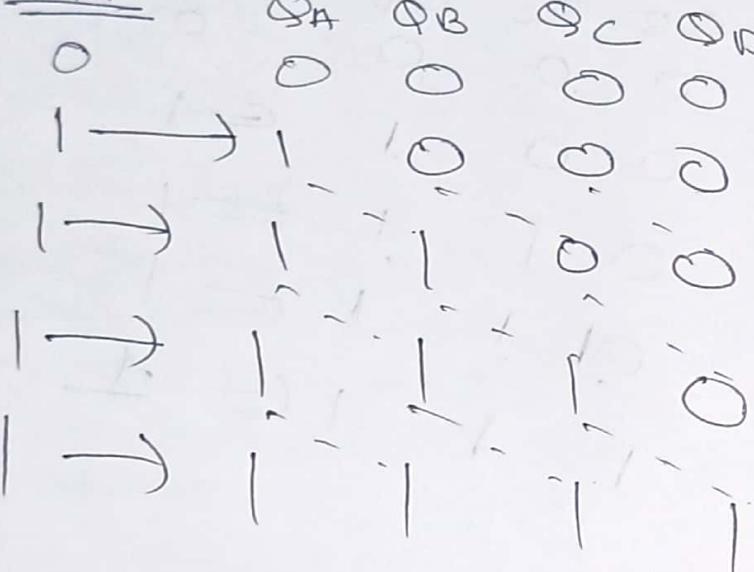
D'in

Q4

① 12

6

1



Waveform

CLK

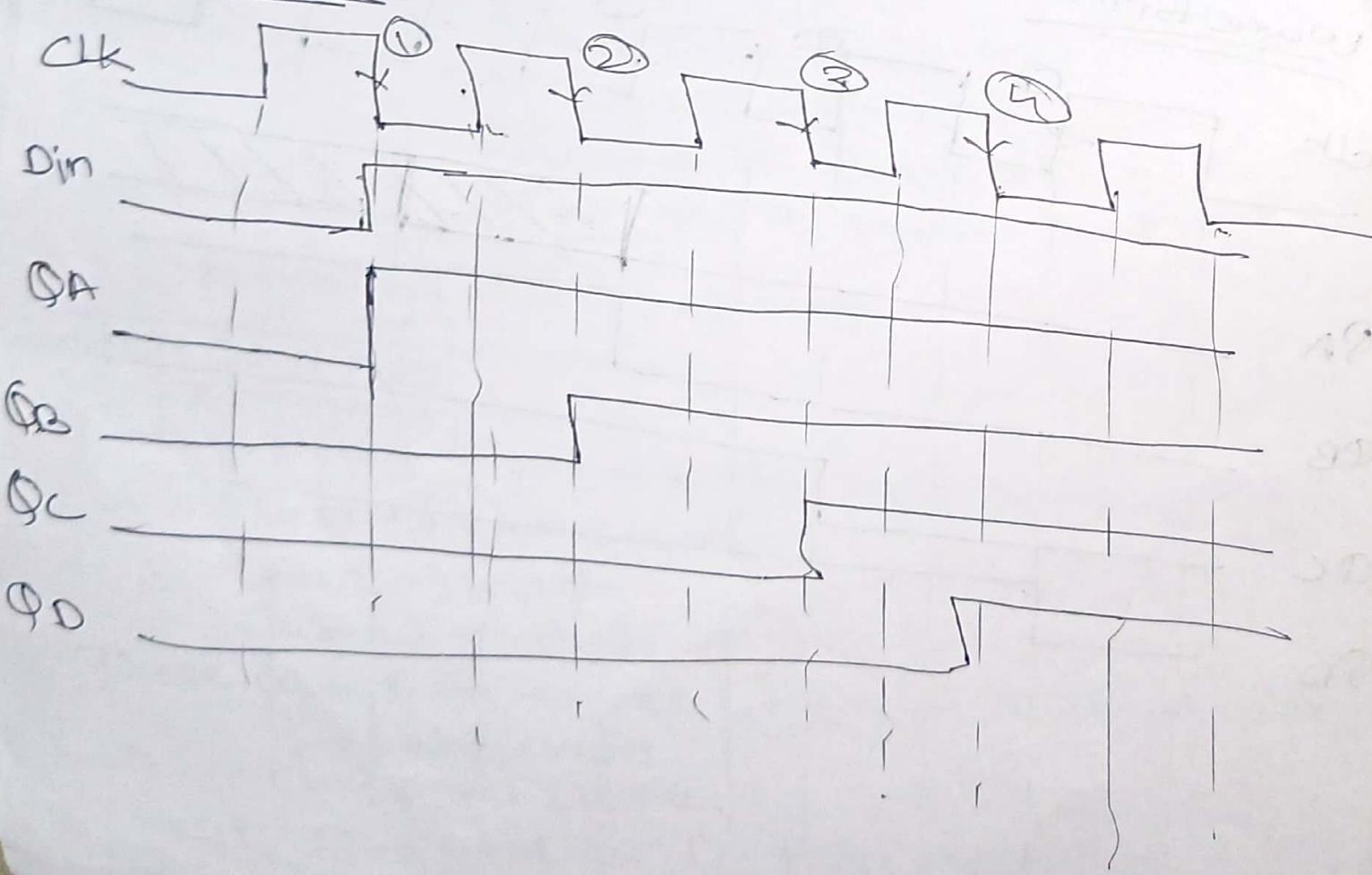
Din

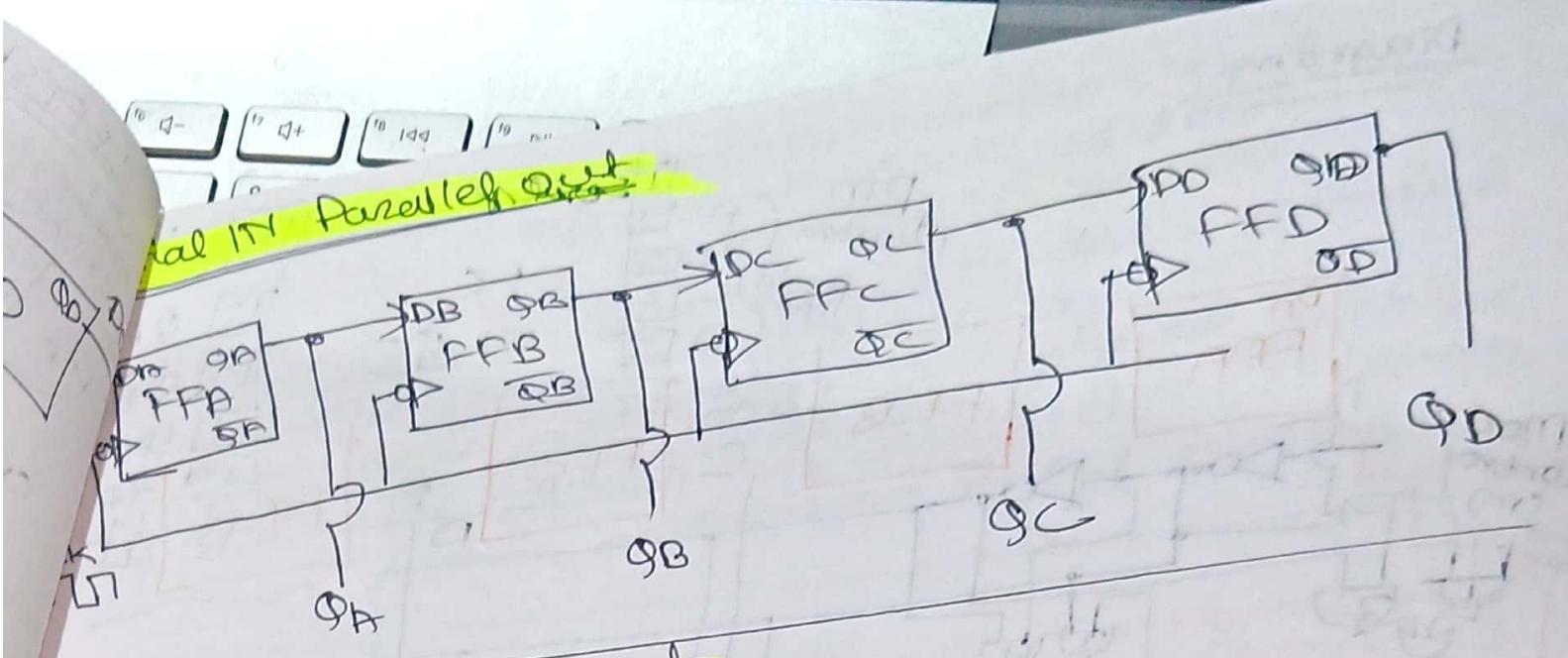
QA

6

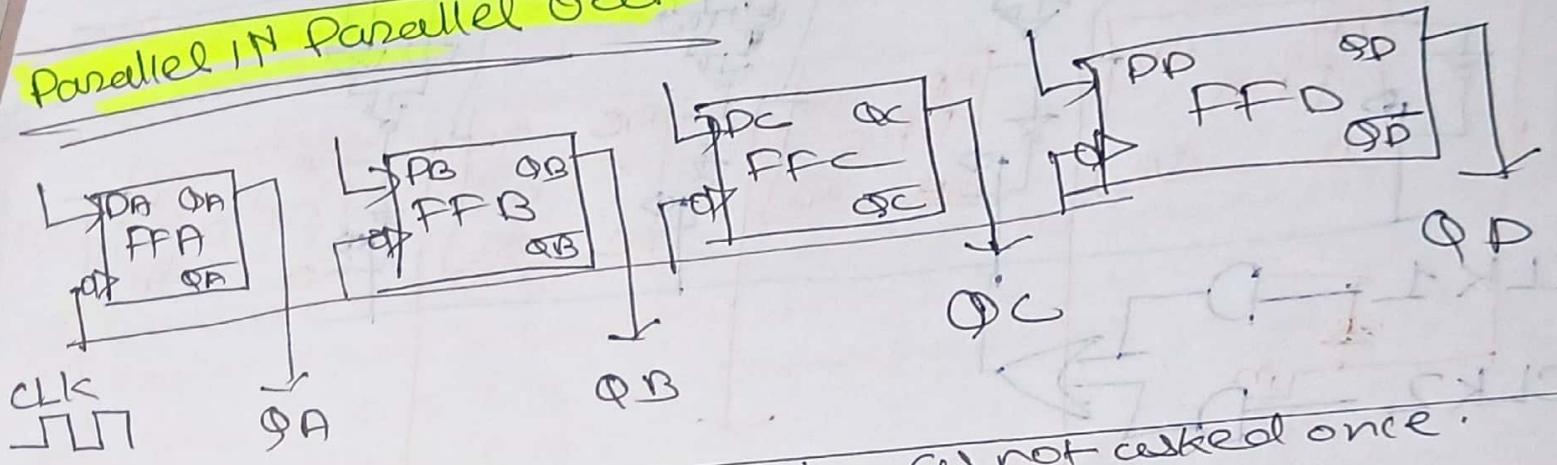
6

6





Parallel IN Parallel OUT



Parallel in serial out \rightarrow option not asked once.

Universal Shift Register

Imp Conclusions

Why universal?

\Rightarrow As it can perform all operations of all type of register.

Such as serial IN serial OUT

Serial IN parallel out.

Parallel IN serial out

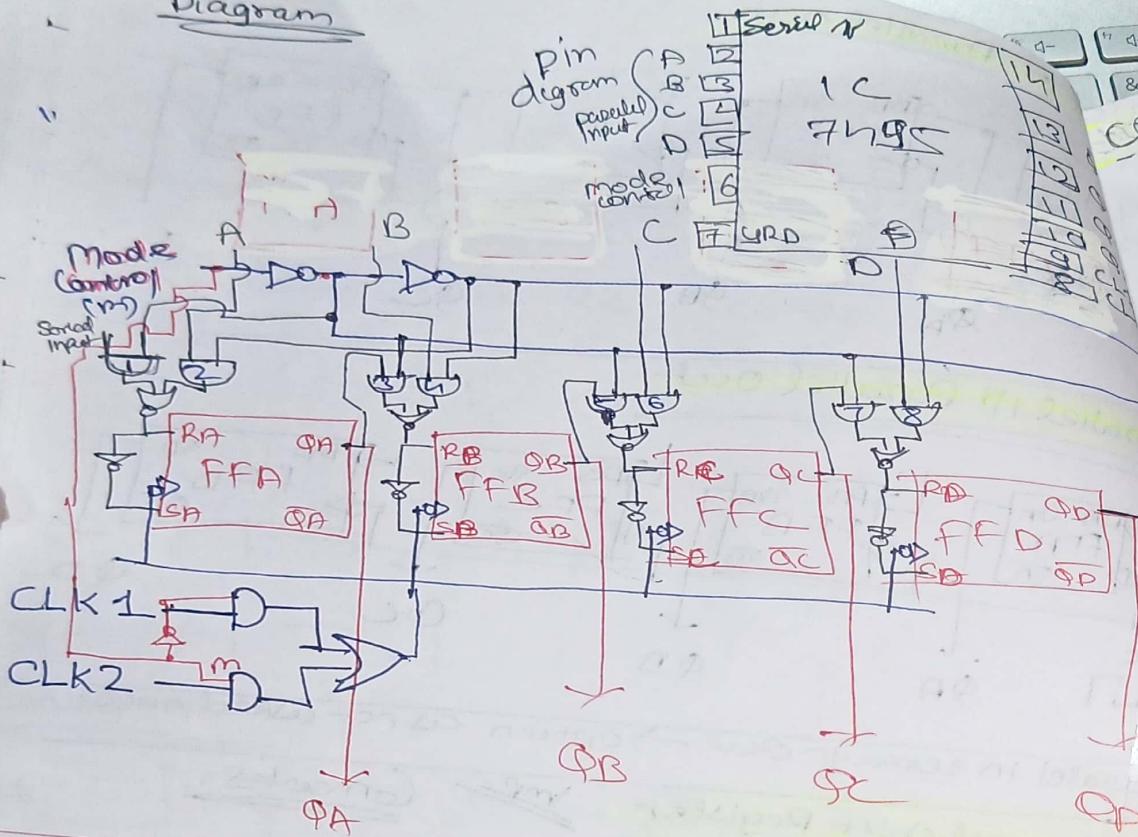
Parallel IN parallel out.

So, it is universal. makes task easier.

Here RS-Flipflop is used.

Here IC 7495 is used for universal shift register.

Diagram



when $M=1$, (1, 3, 5, 7) are disable (OFF).
Then (2, 4, 6, 8) is ON. It acts as left parallel shift.

When $M=0$, (2, 4, 6, 8) are enable & OFF
Then (1, 3, 5, 7) are enable. It acts as right parallel shift.

ABCD - Parallel Input.

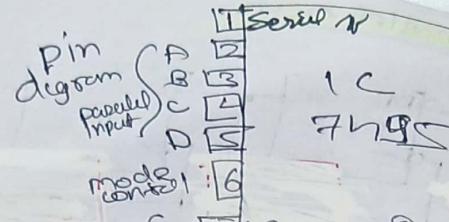
RA RB RC RD Serial Input

QA QB QC QD Serial Output

QA7 PB AC QD Parallel Output

CLK1 → Right.

CLK2 → Left.



Counter
Asynchronous Ripple counter

Synchronous counter
Up/down counter
Decade counter
Decade counter
Ring counter

Questions

- 01 Compare between synchronous and asynchronous
- 02 Explain 3-bit synchronous counter
- 03 Give the design of 4-bit synchronous counter
- 04 Design of 4-bit synchronous counter

Applications

Temporary data storage
Serial-in-serial-out register
produce time delays

Also used for data

Used for data

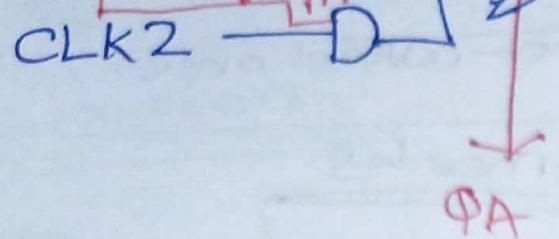
LCDs make fun

Implement sequential

Application of Shift Register.

Temporary data storage used for
serial -in- serial -out & parallel -in-
parallel out register can be used to
reduce time delay to circuit.
Also used for data transfer.

Used for data manipulation
LCDs make funⁿ properly -
implement Sequential Circuit / flipflops.



QB

QC

QD

when $m=1, (1, 3, 5, 7)$ are ~~enable~~ (OFF).

Application of Counter

When

ABC

RN

OR

QA

C

CLK

* Digital Circuits / Sequential Circuits

* To count no. of clock pulses.

* Traffic control system to count the number of vehicles passing through intersection.

* Medical and applications of Industrial to count products.

* To measure frequency of signal.

* digital voltmeters
* frequency counters

Counter

Q1 Asynchronous counter : 4 bit
 Ripple counter, 1bit up down
 Counter modulus of counter.

Synchronous counter : Design 4bit synchronous
 up/down counter

Decade counter : Block schematic of IC 7490
 Decade counter, IC 7490 as mod - N counter,
 Ring counter, Twisted Ring counter

Questions

Q1 Compare between synchronous and asynchronous counter. (2 marks)

Synchronous

Q2 Explain 3bit synchronous counter with output
 waveforms (6 marks)

Q3 Give the block schematic of decade counter IC 7490
 Design mod-7 counter using I_C. (6 marks)

Q4 Design a 3 bit synchronous counter using
 JK flip flop. (6m)

Q5 Design a 4-bit counter synchronous and
 draw its logic diagram (6marks).

Asynchronous

Q1 Design mod-2 ripple counter - Write its truth
 table with waveform (6 marks)

Q2 Design a 4 bit ripple counter using JK flip flop with
 truth table and waveform. (6 m)

Q3 Design a mod-6 Asynchronous counter with
 truth table and logic. (6m).

Q4 Draw 4bit ring counter with truth table &
 its waveform (4m)

Q5 Write down no. of flip flops are required
 to counter 16 clock pulses. (2m).

Q6 Describe working of ring counter using D flip flop
 with diagram and waveform. (4m).

Q7 Define modulus counter. write no. of flip flop
 required for mod-6 counter.

Q1 // Give block structure of decade counter
Design mod-7 counter using this IC.

Counter

It is an Sequential Circuit

A counter is defined as logic circuit that counts the number of clock pulses applied at input.
Each count of binary numbers is known as state of counter.

Here, n bit counter has 2^n different states.

Output = State

2^n
2 bit \rightarrow 4 states.
3 bit \rightarrow 8 states
4 bit \rightarrow 16 states.

Here for JK

Flip Flop is used

In 16 states how many FF are required.

\Rightarrow No. of states = 16.

$$2^n = 16$$

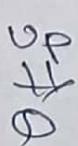
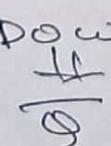
$$2^4 = 16$$

$$\text{So } \underline{\underline{n=4}}$$

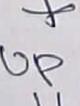
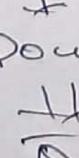
4 flip flop

Types

Asynchronous
Ripple counter

Up

Down


Synchronous
counter

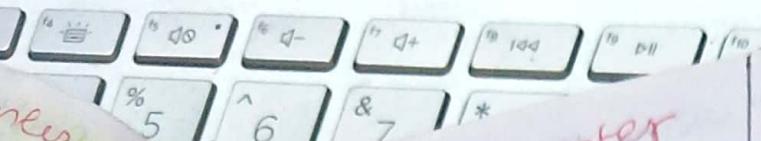
Up

Down


modulus

To Decade
(10)

Johnson
counter

Ring/
Twisted
Ring



Asynchronous Counter

out of previous flip flop is connected to the clock input of the next stage.

Simple logic implementation design is easy.

It is slower.

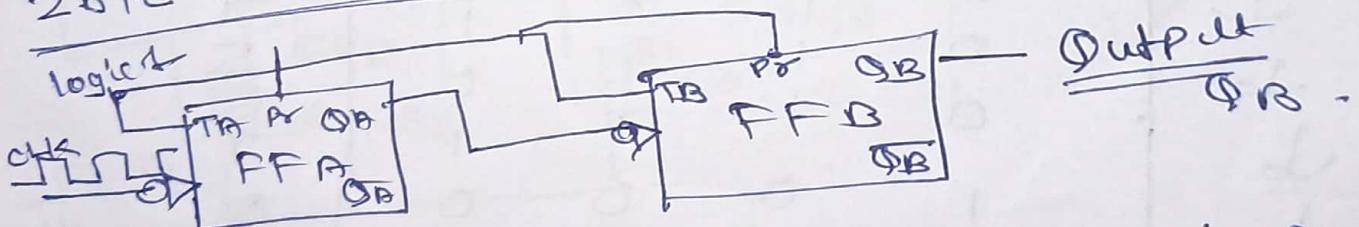
All flipflops are triggered with different clock signal.

Decoding errors are present. Only fixed sequence can be designed.

Asynchronous Counter

No. of bit depends on f.f. output state.
No of state = 2^n .

2bit Asynchronous Counter



$$2^2 = 4$$

Output
 Q_B .

clk= Negative Edge counter output

clock pulse	Q_B	Q_A	state	Decimal no.
Initially	0	0	0	0
+	0	1	1	1
+	1	0	2	2
+	0	1	3	3
+	1	1	4	0

Synchronous Counter

output of previous flip flop is not connected to clock input of next stage.

Complex logic implementation.

Design is complex.

It is faster.

triggered with same clock signal.

Decoding errors are not present.

Only Any sequence can be designed.

Q) Design 4 bit ripple counter using JK flipflop with truthtable & waveform.

(6marks)

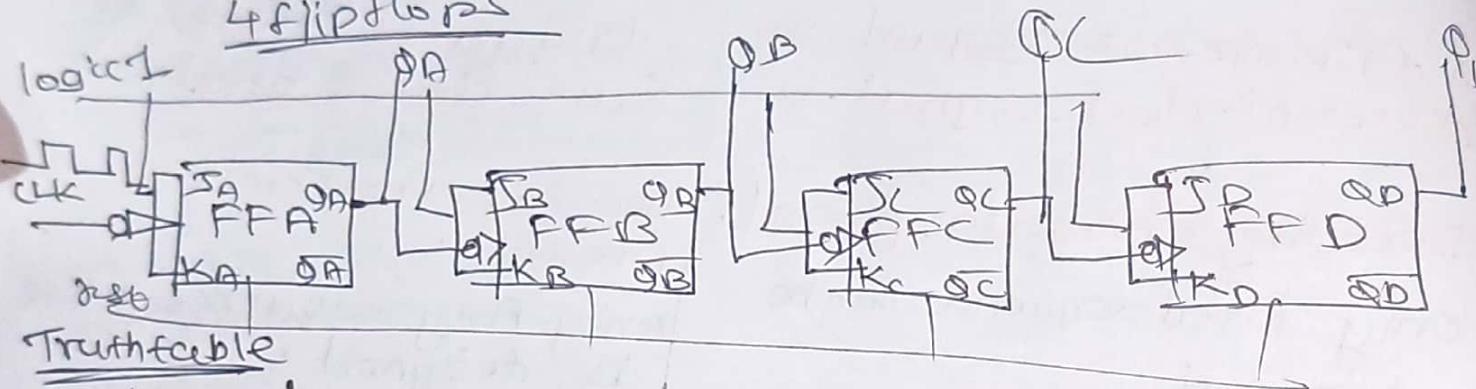
⇒ Using JK we have to short input.

CLK signal is given to first flip flop starting clock signal for other flip flop act as output of previous flip flop.

4bit.

$$2^4 = 16 \text{ states}$$

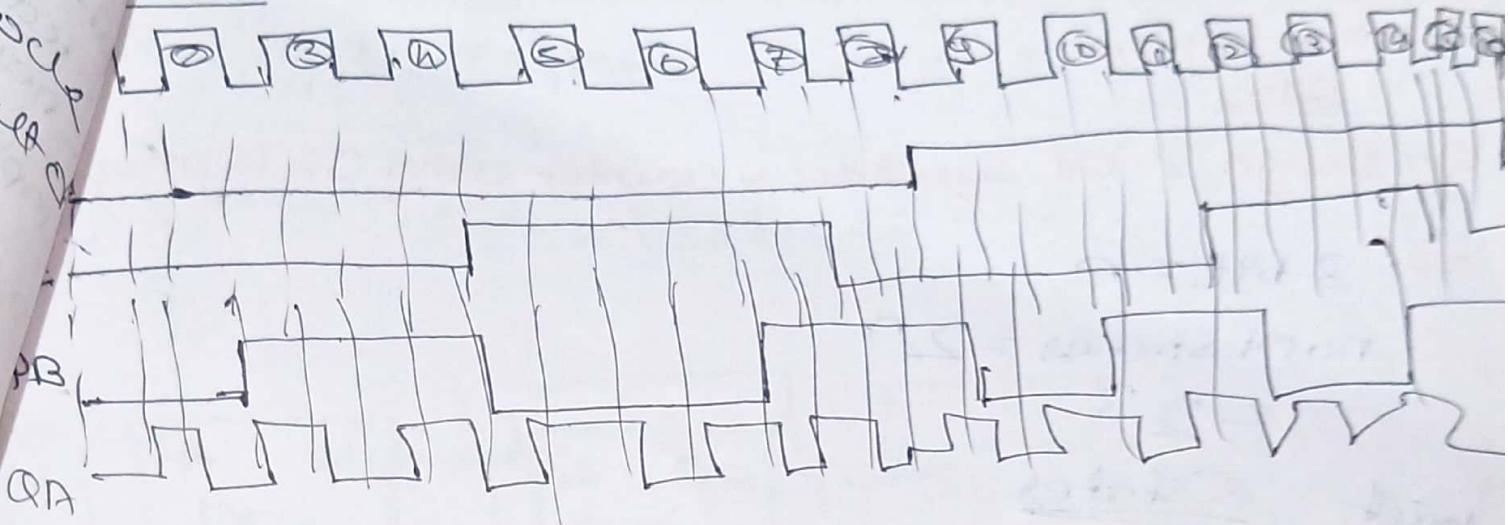
4 flipflops



Truthtable

Count	J K initially	Q _D	Q _C	Q _B	Q _A	State
0	+ +	0	0	0	0	1
1	+ +	0	0	0	1	1
2	+ +	0	0	1	0	2
3	+ +	0	0	0	0	3
4	+ +	0	1	0	0	4
5	+ +	0	1	0	1	5
6	+ +	0	1	1	0	6
7	+ +	0	1	1	1	7
8	+ +	1	0	0	0	8
9	+ +	1	0	0	1	9
10	+ +	1	0	1	0	10
11	+ +	1	0	1	1	11
12	+ +	1	1	0	0	12
13	+ +	1	1	0	1	13
14	+ +	1	1	1	0	14
15	+ +	1	1	1	1	15

reform



Synchronous Counter

CLK signal same.
Design complex.

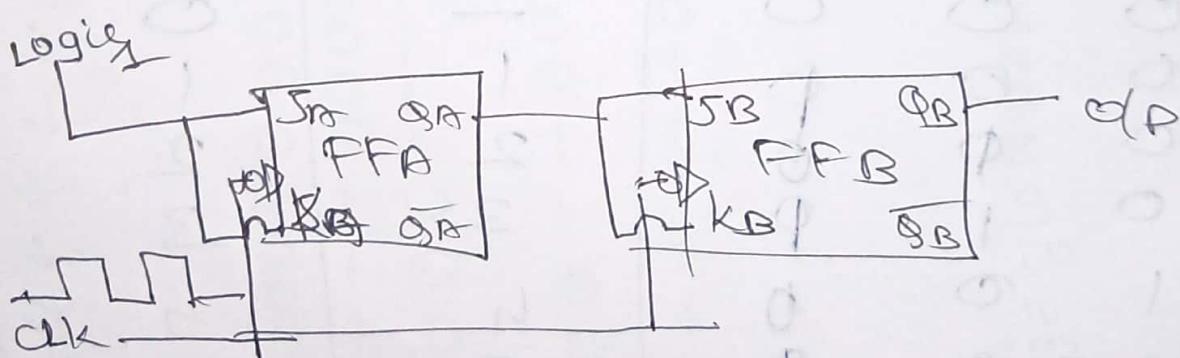
F-F flop function at same time as CLK
Signal.

Flip flop used = JK

Output to next
Input

2bit Synchronous Counter

$$2^n = 2^2 = 4 \text{ states}$$



Truth Table

CLK	Q_B	Q_A	state	No
initial	0	0	0	0
+	0	1	1	1
+	1	0	2	2
+	1	1	3	3
+	0	0	4	0

Q1) Explain 3-bit synchronous waveforms

QB

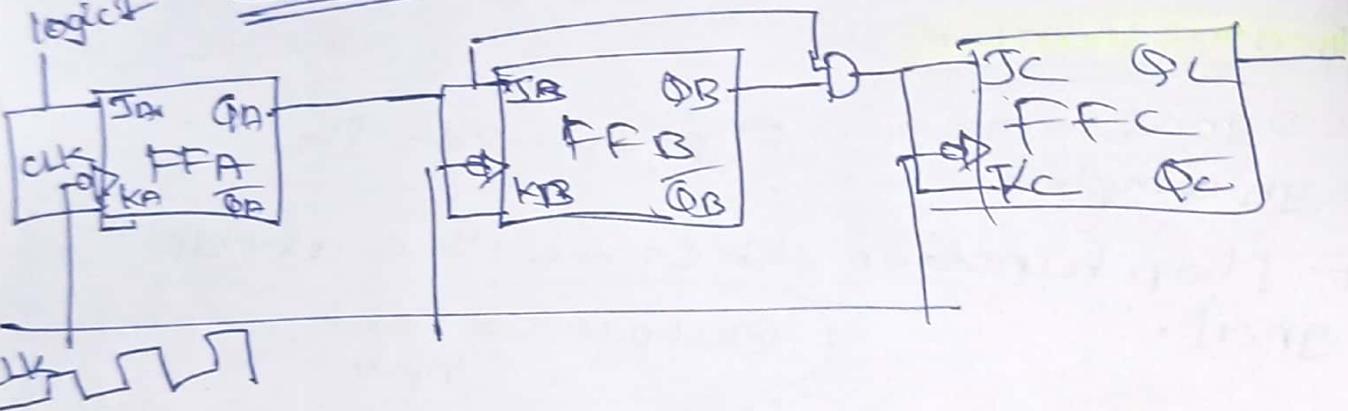
Q2) Design 3-bit synchronous counter using JK flip-flops

$$\Rightarrow 3\text{-bit} = n$$

$$\text{no of states} = 2^n$$

$$= 2^3$$

logic States



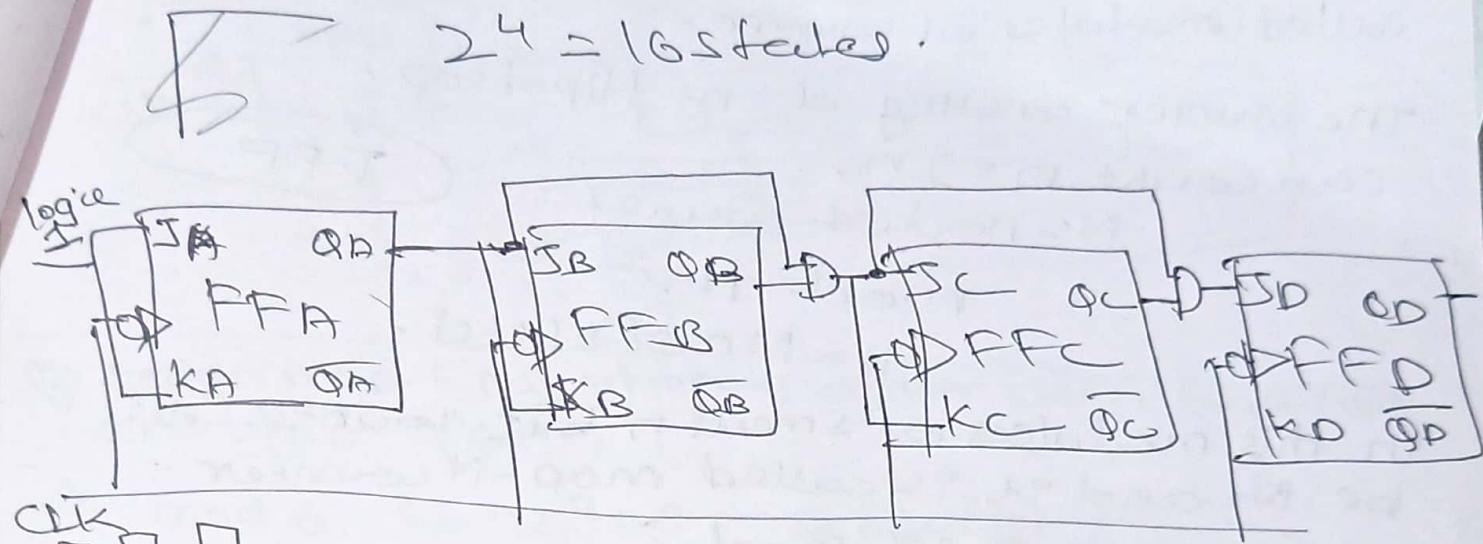
Truth table

<u>CLK</u>	QB	QB	QC	state	decimal
initially	0	0	0	-	0
+	0	0	0	1	1
+	0	0	1	2	2
+	0	1	0	3	3
+	1	0	0	4	4
+	1	0	1	5	5
+	0	1	1	6	6
+	0	1	0	7	7
+	0	0	0	8	8

~~ALPAC~~
design 4-bit synchronous counter and draw its logic diagram.

$$2^5$$

$$2^4 = 16 \text{ states.}$$



CLK

Initial State

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

State

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Decimal

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Mod counter

modulus of counter - total number of discrete states through which counter can pass called modulus of counter.

The counter consisting of 'n' flip-flop.

can count $M = 2^n$.

$N = \text{no. of counts}$

$\text{mod} = N$.

$N = \text{No. of states}$.

T-FF

In this modulus of small n bit counter will be 'N' and it is called mod-N counter.

SFF \rightarrow SFT Mod

Design mod-5 ripple counter

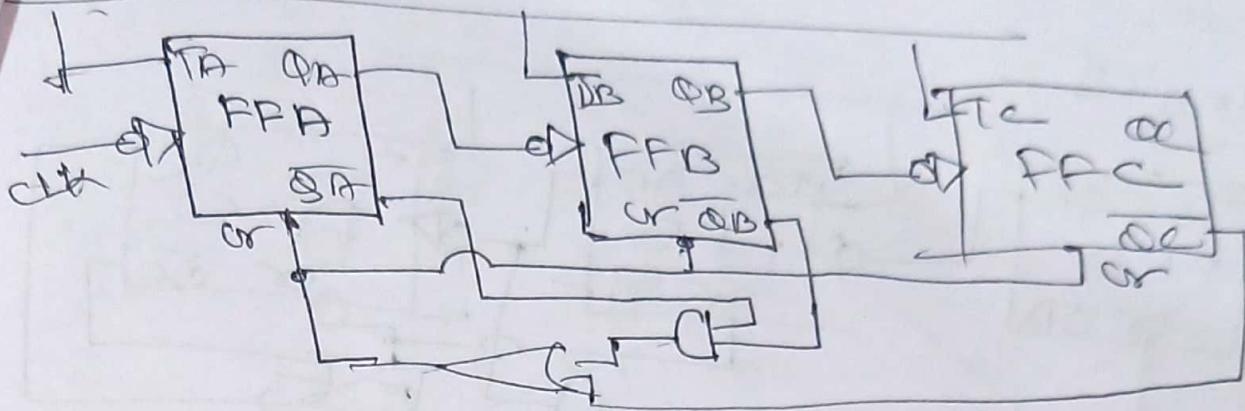
28-28.

State	ff O/P			Y
	Q _C	Q _B	Q _A	
0	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

K-map for Y.

$\bar{Q}_C Q_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$Q_B \bar{Q}_A$	Q_C
\bar{Q}_C					
Q_C					
$\bar{Q}_B \bar{Q}_A$					
\bar{Q}_C					
Q_C					
$\bar{Q}_B Q_A$					
$\bar{Q}_C \bar{Q}_B \bar{Q}_A$					

Q1



(Q1) Design mod-6 Asynchronous counter with truth-table and logic. (6m)

→ mod 6 so $2^3 = 8$. 3 flip flops of T.
Some logic to stop after 0-5 after.
So, K-MAP.

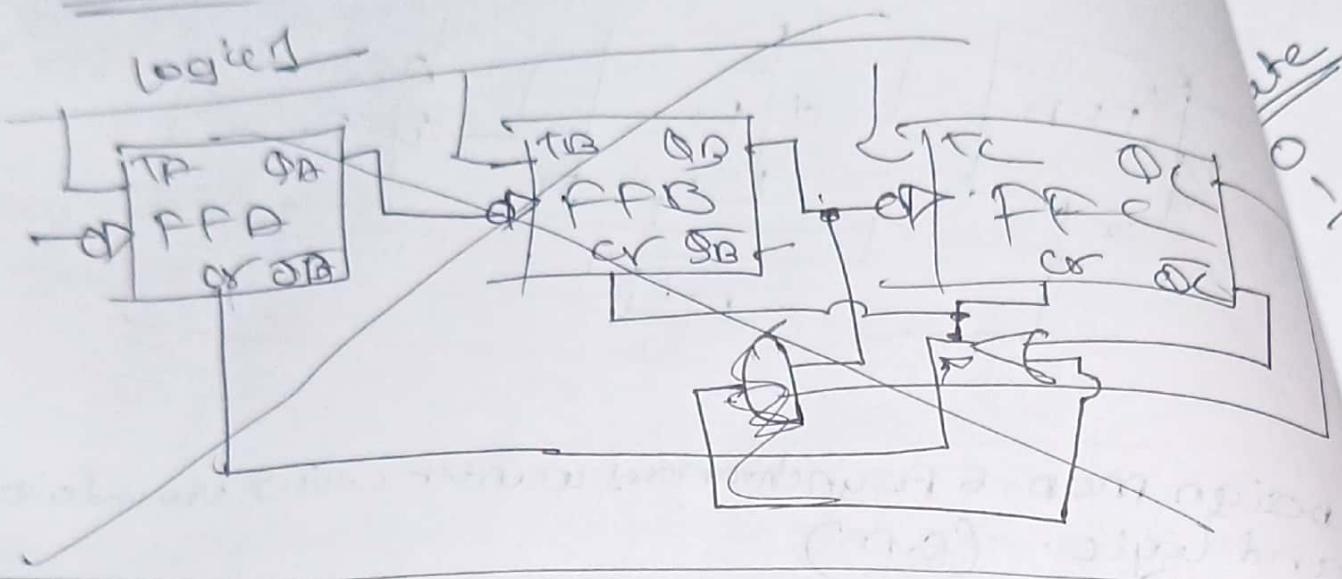
State	\bar{Q}_C	\bar{Q}_B	\bar{Q}_A	
0	0	0	0	1
1	0	0	1	0
2	0	1	1	0
3	0	0	0	0
4	1	0	0	1
5	1	1	0	0
6	1	0	1	0
7	1	1	1	0

K-MAP

$\bar{Q}_C \bar{Q}_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
\bar{Q}_C	1	1	1	1
\bar{Q}_C	1	1	1	1
\bar{Q}_C	1	1	1	1
\bar{Q}_C	1	1	1	1

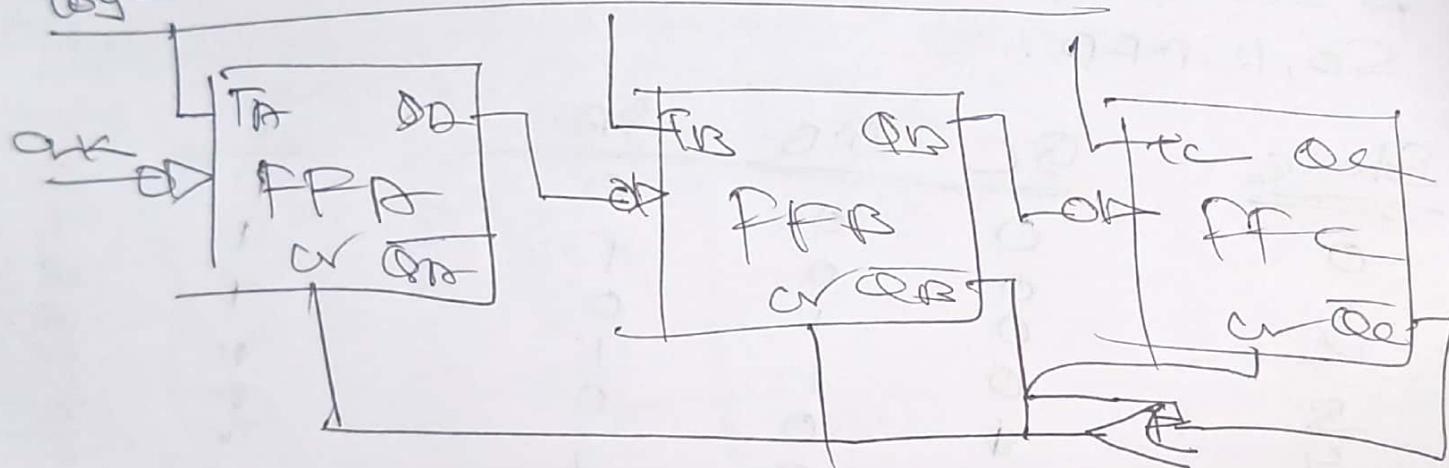
Circuit

logics



$\bar{Q}_B + \bar{Q}_C$

logics



Design mod-12 ripple counter write q.v. truth table and waveform. (6m).

$\Rightarrow 12 =$

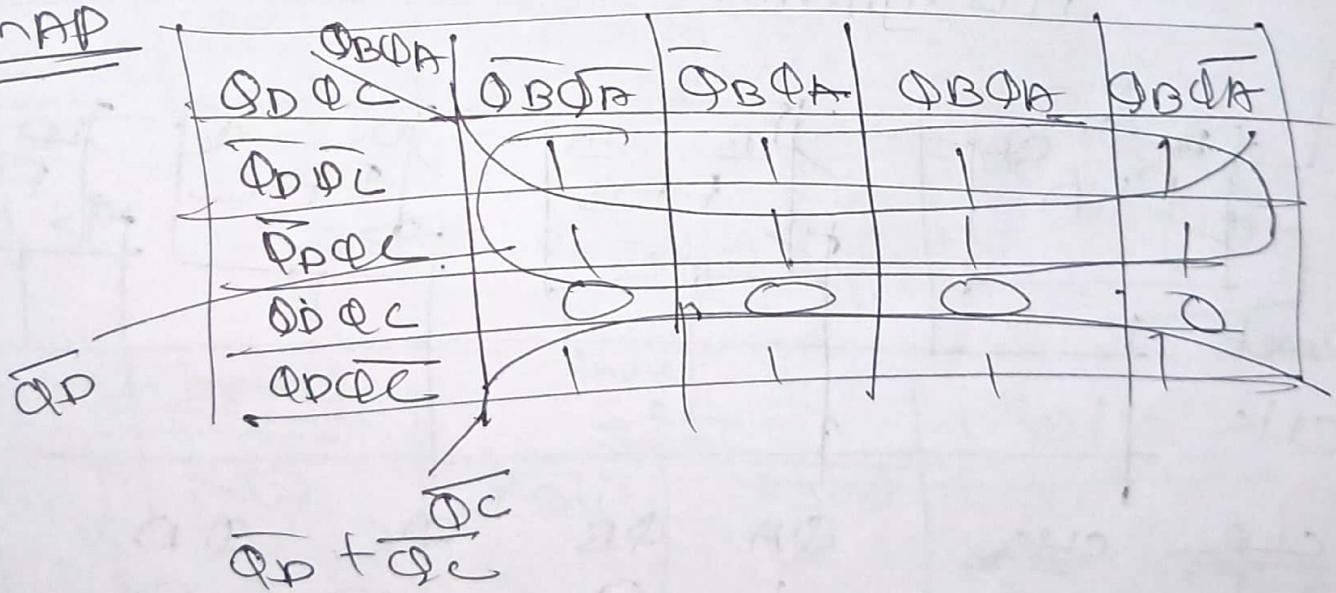
$$2^4 = 16 \text{ states}$$

4 Flip flop.

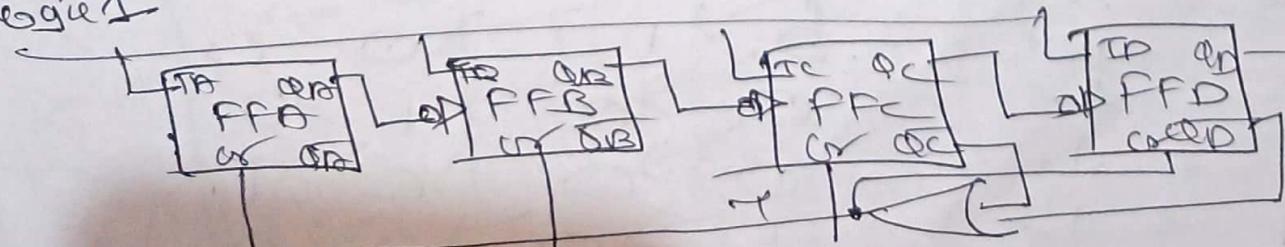
late

	ΦD	ΦC	ΦB	ΦA	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	0	0	
4	0	0	1	1	
5	0	0	0	0	
6	0	0	1	0	
7	0	0	0	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

K-map



logic1



No of flip-flop required for mod-6 counter
→ 2^n

$$2^3 = 8$$

Ring Counter :- Imp

Q/W write down & draw Ring Counter with truth table & its waveform.

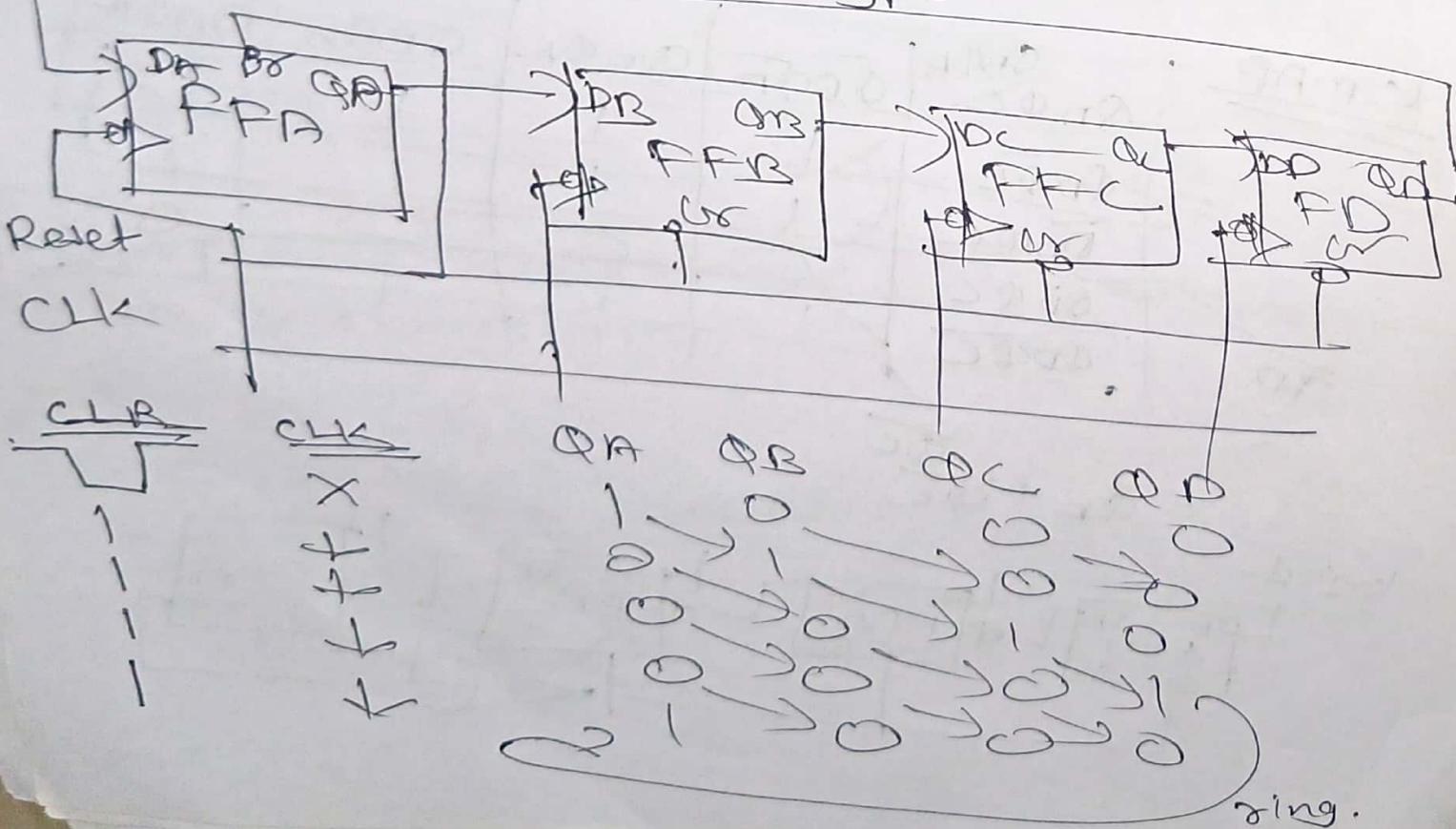
Ring

Ring counter is a special application of shift register.
waveform - D-Flipflop here.

4-D Flipflop.

It is same as shift register output of last flipflop connected to next flipflop of ring.
Data flow in ring.

It is synchronous type.

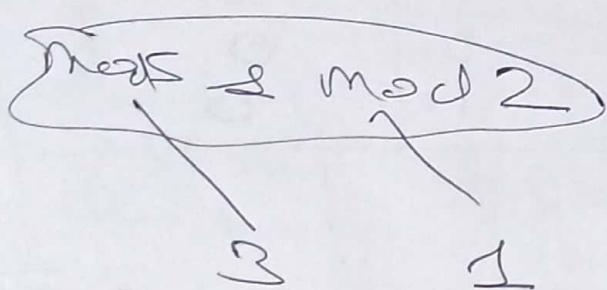


→ (6 m)

⇒ It is an ripple counter + C

This IC Counter BCD counter sequence of
contains 4 negative edge trigger flip flops &

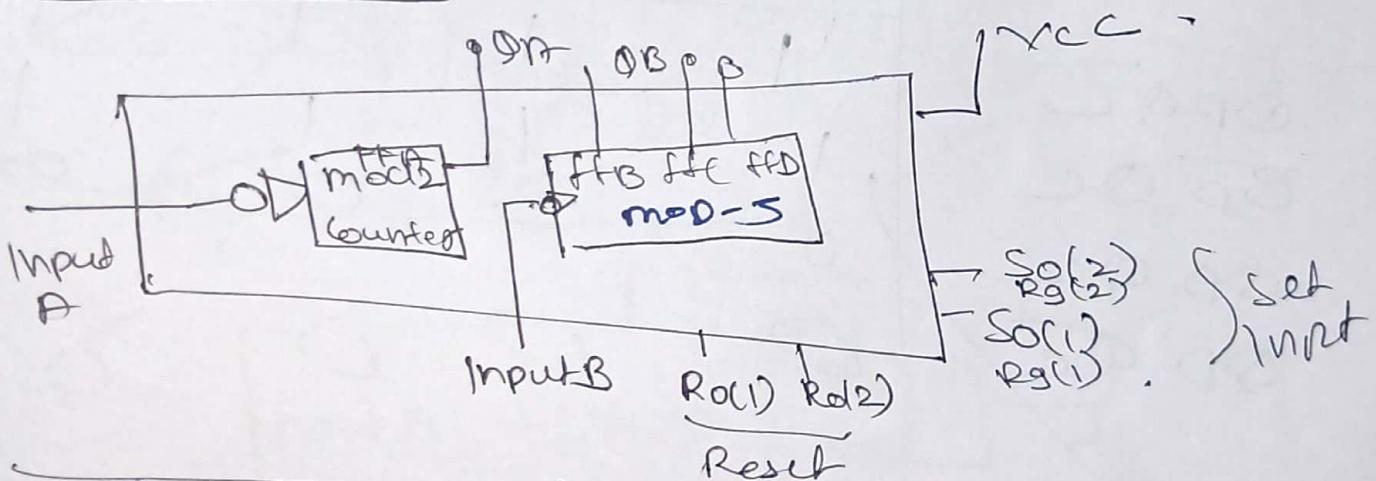
Internally it is made from mod5 & mod2
counter



$$2 \times 5 = 10$$

PF = 100010

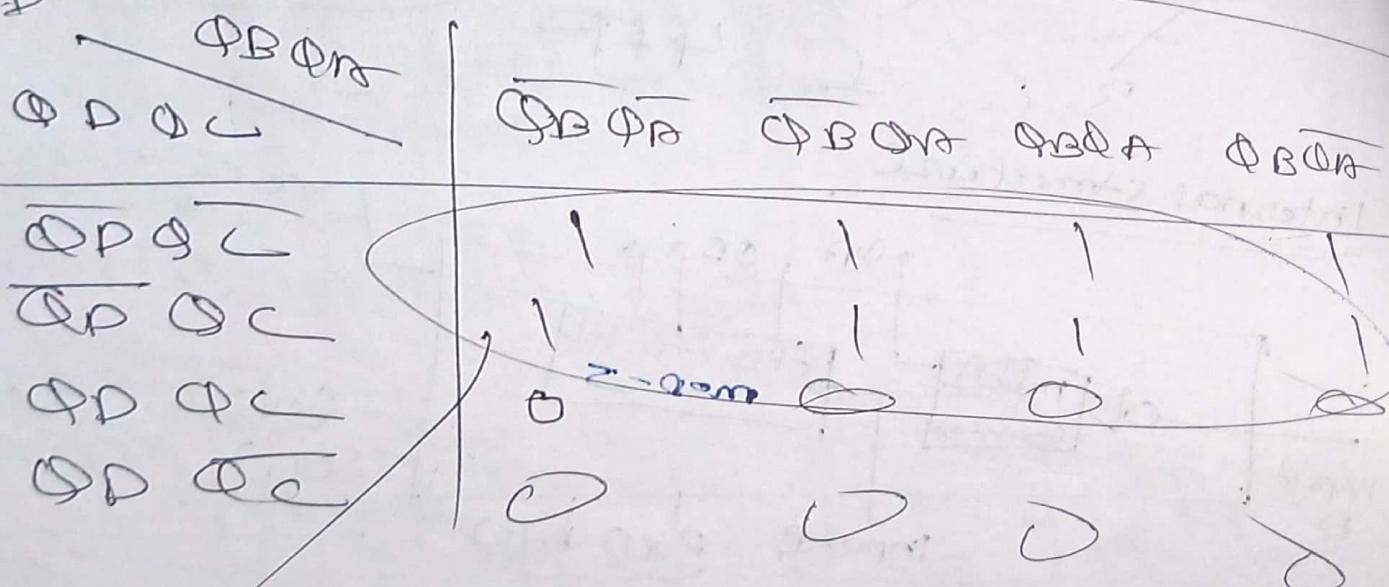
Internal Structure



<u>Reset Inputs</u>		<u>Input Set</u>		<u>O/P</u>
Rg(1)	Rg(2)	Rg(1)	Rg(2)	
1	1	X	X	0000
X	X	1	1	0001
X	0	X	0	Count
0	X	0	X	Count
0	X	X	0	Count
X	0	0	X	Count

Mod-8 using IC7490

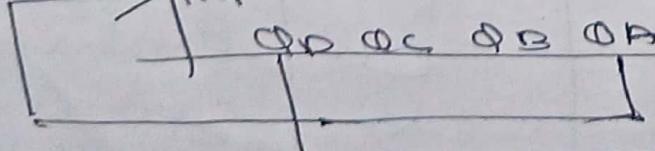
State	ϕD	ϕC	ϕB	ϕA	
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0



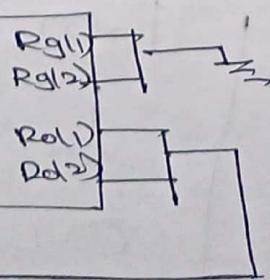
$t = \text{constant}$

$t \rightarrow \text{Input A}$

$t \rightarrow \text{Input B}$



IC7490



Mod6 using IC7490

State

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

Qc

QB

QA

Qc

QB

QA

T

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

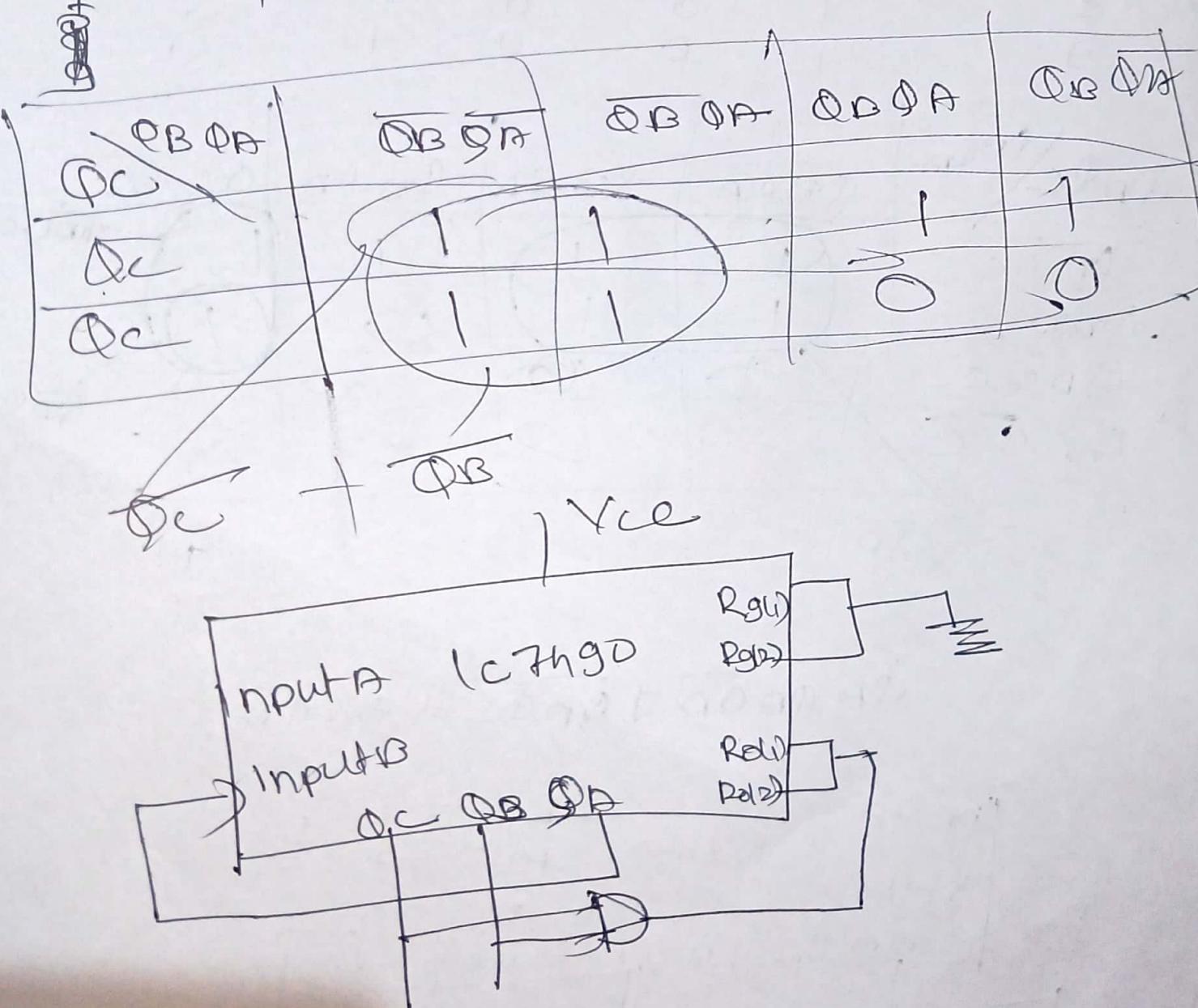
1

1

1

1

1



Q11 Mod-7 counter using IC 7490.

State

0
1
2
3
4
5
6
7

QD
0
0
0
0
0
1
1
1

QC

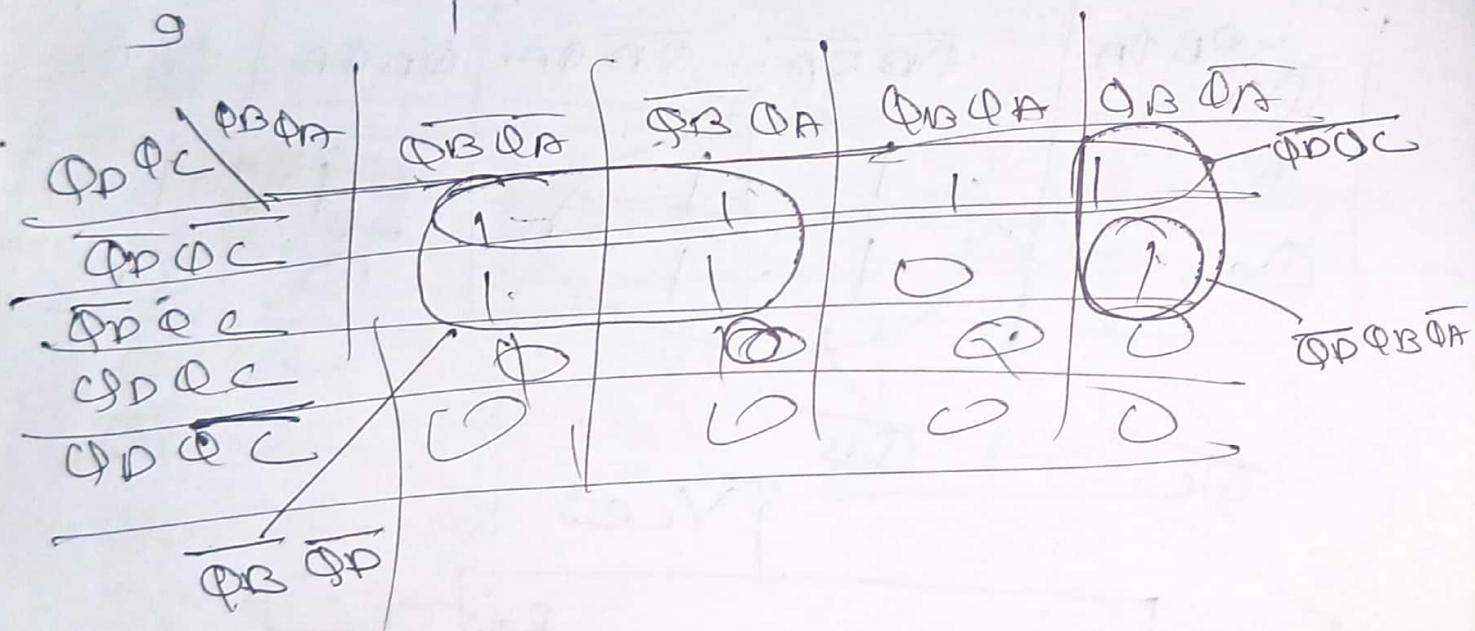
0
0
0
1
1
0
0
0

$(QDQC)$
 $QBQA$

0
0
0
1
1
0
0
0

T

0
0
0
1
1
0
0
0



$$\overline{QB} \overline{QB} \overline{D} + \overline{QD} \overline{QC} + \overline{QB} \overline{D}$$

