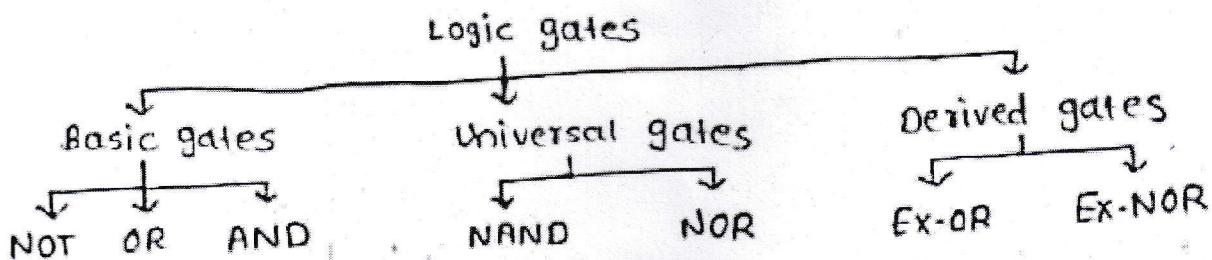


**Logic Gates :** A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels.



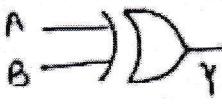
### \* Basic gates

logic gate	Symbol	Equation	Truth Table	IC Number															
NOT gate		$Y = \bar{A}$	<table border="1"> <tr> <td>A</td><td>Y</td></tr> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td></tr> </table>	A	Y	0	1	1	0	IC 7404									
A	Y																		
0	1																		
1	0																		
OR gate		$Y = A + B$	<table border="1"> <tr> <td>A</td><td>B</td><td>Y</td></tr> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </table>	A	B	Y	0	0	0	0	1	1	1	0	1	1	1	1	IC 7432
A	B	Y																	
0	0	0																	
0	1	1																	
1	0	1																	
1	1	1																	
AND gate		$Y = A \cdot B$	<table border="1"> <tr> <td>A</td><td>B</td><td>Y</td></tr> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </table>	A	B	Y	0	0	0	0	1	0	1	0	0	1	1	1	IC 7408
A	B	Y																	
0	0	0																	
0	1	0																	
1	0	0																	
1	1	1																	

### \* Universal gates

logic gate	Symbol	Equation	Truth Table	IC Number															
NAND Gate		$Y = \overline{A \cdot B}$	<table border="1"> <tr> <td>A</td><td>B</td><td>Y</td></tr> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </table>	A	B	Y	0	0	1	0	1	1	1	0	1	1	1	0	IC 7400
A	B	Y																	
0	0	1																	
0	1	1																	
1	0	1																	
1	1	0																	
NOR Gate		$Y = \overline{A + B}$	<table border="1"> <tr> <td>A</td><td>B</td><td>Y</td></tr> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </table>	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	0	IC 7402
A	B	Y																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	0																	

\* Derived logic gates

Logic gate	Symbol	Equation	Truth table	IC Number															
Ex-OR gate		$Y = A \oplus B$ $Y = \bar{A}B + A\bar{B}$	<table border="1"> <tr> <th>A</th><th>B</th><th>Y</th></tr> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </table>	A	B	Y	0	0	0	0	1	1	1	0	1	1	1	0	IC 7486
A	B	Y																	
0	0	0																	
0	1	1																	
1	0	1																	
1	1	0																	
Ex-NOR gate		$Y = A \ominus B$ $Y = \bar{A}\bar{B} + AB$	<table border="1"> <tr> <th>A</th><th>B</th><th>Y</th></tr> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </table>	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	1	IC 74266
A	B	Y																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	1																	

# Boolean Algebra Theorems and Laws

## 1. Commutative Law

$$A+B = B+A$$

## 2. Associative Law

$$(A + B) + C = A + (B + C)$$

$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$

## 3. Distributive Law

This law is composed of two operators, AND and OR.

$$A \cdot (B + C) = A \cdot B + A \cdot C$$

## 5. AND Laws

- A . 0 = 0      where A can be either 0 or 1.
- A . 1 = A      where A can be either 0 or 1.
- A . A = A      where A can be either 0 or 1.
- A .  $\bar{A}$  = 0      where A can be either 0 or 1.

## 6. OR Laws

## 8. Absorption Law

$$A + A \cdot B = A$$

Inputs			Output
A	B	AB	$A+A \cdot B$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

### Duality Theorem

- According to the principle of duality one type of operation can be changed into another type of operation just by interchanging 0 and 1.
- For example the AND and OR operation can be interchanged by changing the values 0 and 1. This principle is used to reduce the Boolean expressions.

**Rule 1:**  
AND  $\longrightarrow$  OR  
OR  $\longrightarrow$  AND

**Rule 2:**  
0  $\longrightarrow$  1  
1  $\longrightarrow$  0

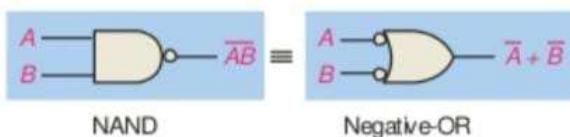
Given Expression	Dual Expression
0=1	1=0
0.1=0	1+0=1
A.0=0	A+1=1
A.B=B.A	A+B=B+A
A.A=0	A+A=1
A.(B.C)=(A.B).C	A+(B+C)=(A+B)+C
AB=A+B	A+B=A.B
(A+B)(A+C)=AB+AC	AB+AC=(A+B)(A+C)

## DeMorgan's Theorem

- The complement of a product of variables is equal to the sum of the complemented variables

### Theorem 1

$$\overline{AB} = \overline{A} + \overline{B}$$

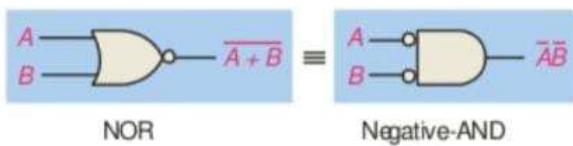


A	B	$\overline{A \cdot B}$	$\overline{\overline{A} + \overline{B}}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

## DeMorgan's Theorem

### Theorem 2

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$



A	B	$\overline{A + B}$	$\overline{\overline{A} \cdot \overline{B}}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

## Implementation of Logic gates using NAND gate

### 1) NOT Gate using NAND

$$Y = \overline{A}$$

$$Y = \overline{\overline{A}} \quad \therefore A = B$$

$$Y = \overline{A}$$

### 2) AND Gate using NAND

$$Y = A \cdot B$$

$$Y = \overline{\overline{A} \cdot B}$$

### 3) OR Gate using NAND

$$Y = A + B$$

$$= \overline{\overline{A} + B}$$

APPLY De'Morgans

$$Y = \overline{\overline{A} \cdot \overline{B}}$$

### 4) NOR Gate using NAND

$$Y = \overline{A + B}$$

$$= \overline{\overline{A} \cdot \overline{B}}$$

$$= \overline{\overline{A} \cdot \overline{B}}$$

### 5) EX-OR Gate using NAND

$$Y = \overline{A}B + A\overline{B}$$

$$= \overline{\overline{A}B + A\overline{B}}$$

$$= \overline{\overline{A} \cdot B + A \cdot \overline{B}}$$

### 6) EX-NOR Gate using NAND

$$Y = \overline{A \oplus B}$$

$$= \overline{\overline{A}B + A\overline{B}}$$

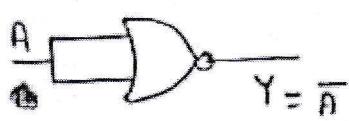
$$= \overline{\overline{A} \cdot B + A \cdot \overline{B}}$$

$$= \overline{\overline{A} \cdot B - A \cdot \overline{B}}$$

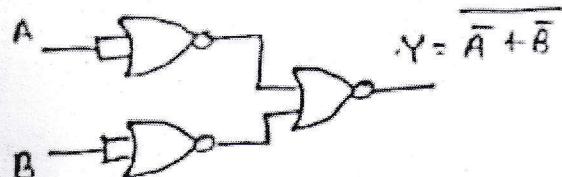
## Implementation of Logic gates using NOR gate

### 1) NOT Gate using NOR

$$Y = \overline{A}$$



### 2) AND Gate using NOR



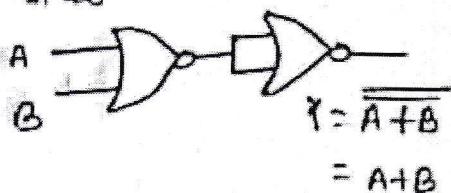
$$\begin{aligned} Y &= A \cdot B \\ &= \overline{\overline{A} \cdot \overline{B}} \\ &\text{apply deMorgan's} \\ &Y = \overline{\overline{A} + \overline{B}} \end{aligned}$$

### 3) OR Gate using NOR

$$Y = A + B$$

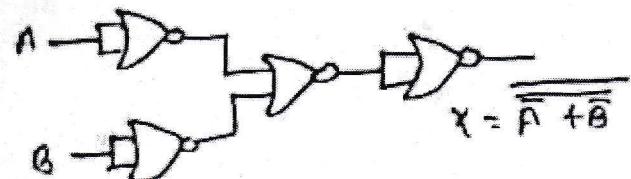
$$Y = \overline{\overline{A} + \overline{B}}$$

$$Y = \overline{\overline{A} \cdot \overline{B}}$$



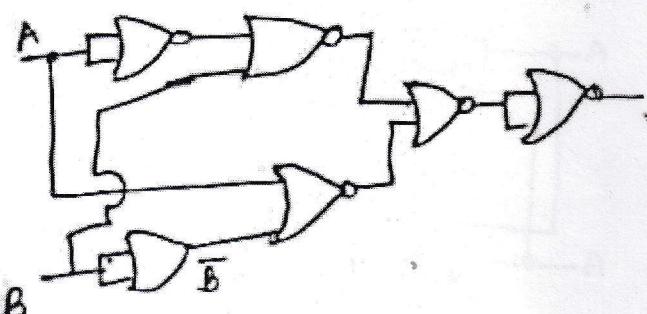
### 4) NAND Gate using NOR

$$\begin{aligned} Y &= \overline{A \cdot B} \\ &= \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A} + \overline{B}} \end{aligned}$$



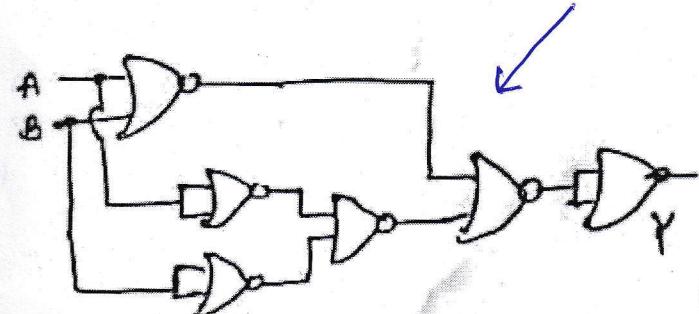
### 5) EX-OR Gate using NOR

$$\begin{aligned} Y &= \overline{\overline{A}B + A\overline{B}} \\ &= \overline{\overline{A}\overline{B} \cdot A\overline{B}} \\ &= \overline{\overline{A}\overline{B}} \\ &= \overline{\overline{A} + \overline{B}} \cdot \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + \overline{B}} \end{aligned}$$



### 6) EX-NOR Gate using NOR

$$\begin{aligned} Y &= \overline{\overline{A}B + A\overline{B}} \quad \text{or} \quad Y = \overline{\overline{A}\overline{B} + AB} \\ &= \overline{\overline{A}\overline{B} \cdot A\overline{B}} \\ &= \overline{\overline{A}\overline{B} \cdot A\overline{B}} \\ &= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + \overline{B}} \end{aligned}$$



## Logic families

- Various digital IC's available in market belong to various types. These types are known as 'families'.  
- Based on the components and devices internally used, the digital IC families are named as

- RTL (Resistor Transistor Logic)
- TTL (Transistor-Transistor Logic)
- DTL (Diode Transistor Logic)
- CMOS (Complementary MOSFET) etc.

\* Classification of IC According to their scale of integration : Based on number of components or gates

1) Small Scale Integration (SSI) :

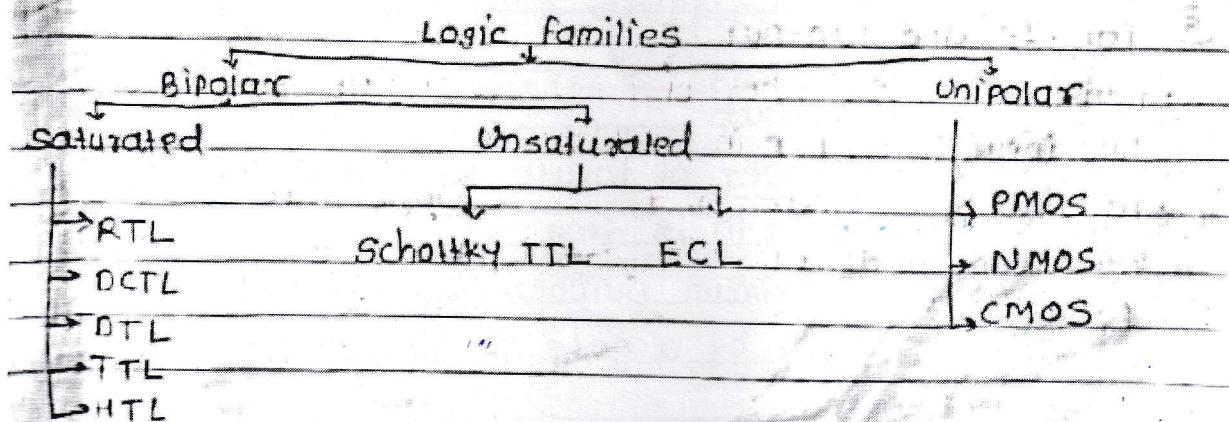
It is the IC manufacturing technique in which less than 30 logic gates are manufactured in a single silicon chip.

2) Medium Scale Integration (MSI) : About 30 to 100 logic gates are manufactured in a single chip.

3) Large Scale Integration (LSI) : About 100 to 10,000

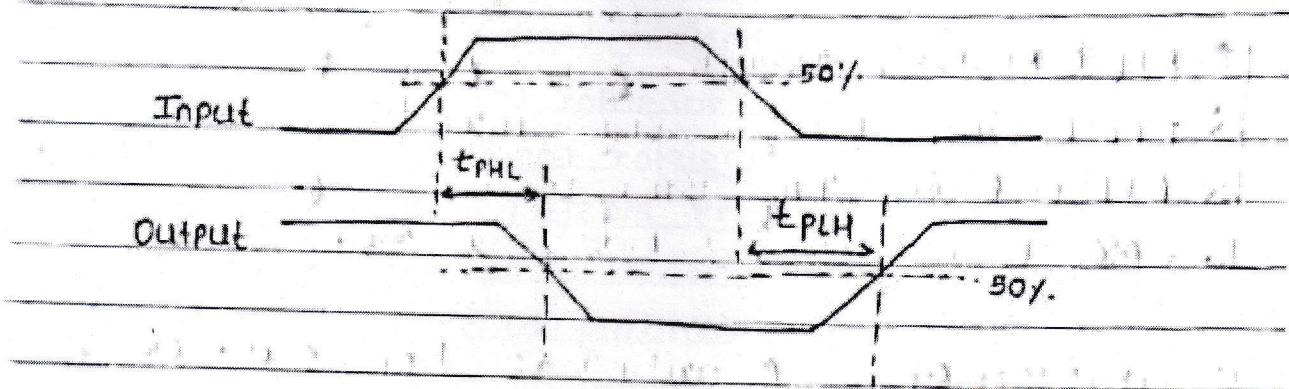
4) Very Large Scale Integration (VLSI) : more than 10,000 logic gates.

\* Classification of logic families :



## Characteristics of logic family:

① Propagation delay: It is defined as the time delay between the instant of application of an input pulse and the instant of occurrence of the corresponding output pulse.



$t_{PHL}$  → delay time when output changes from high to low state.

$t_{PLH}$  → delay time when output changes from low to high state.

• Propagation delay between input and output should be as minimum as possible so that speed of IC remains high.

② Power dissipation: As a result of applied voltage & currents flowing through the logic IC's, some power will be dissipated in it, in the form of heat which is known as power dissipation.  
• Requirement of power is less, if the dissipation of power is less.

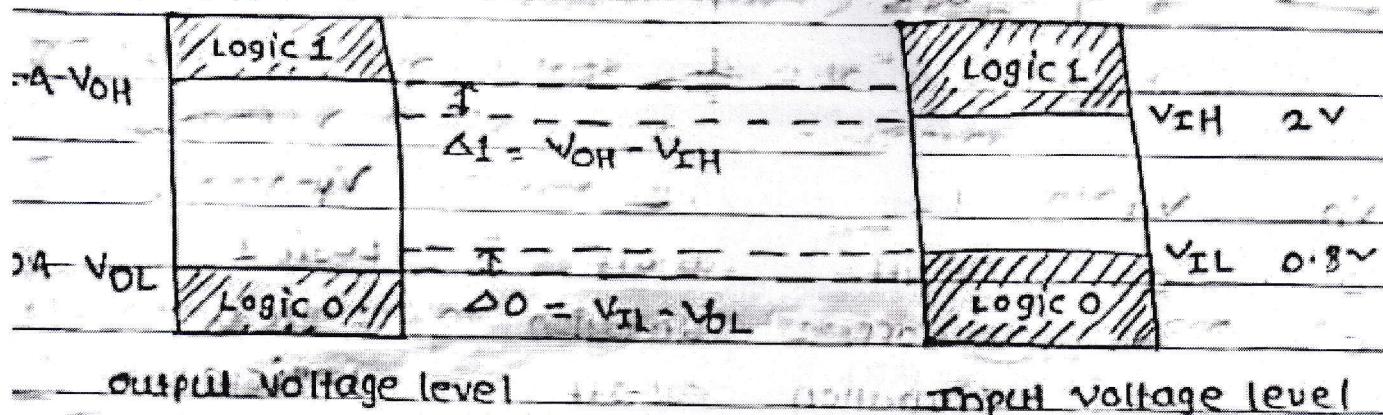
③ Fan-In and fan-out

• Fan-in is the number of inputs to a gate. For a two input gate, fan-in is two.

• Fan-out: The maximum number of logic gates which can be driven by a gate is known as fan-out.

④ Noise Immunity : Unwanted signals are known as noise.

- The noise immunity of digital circuit is defined as the ability of a digital circuit to tolerate the noise signal.
- A quantitative measure of noise immunity is known as noise margin.



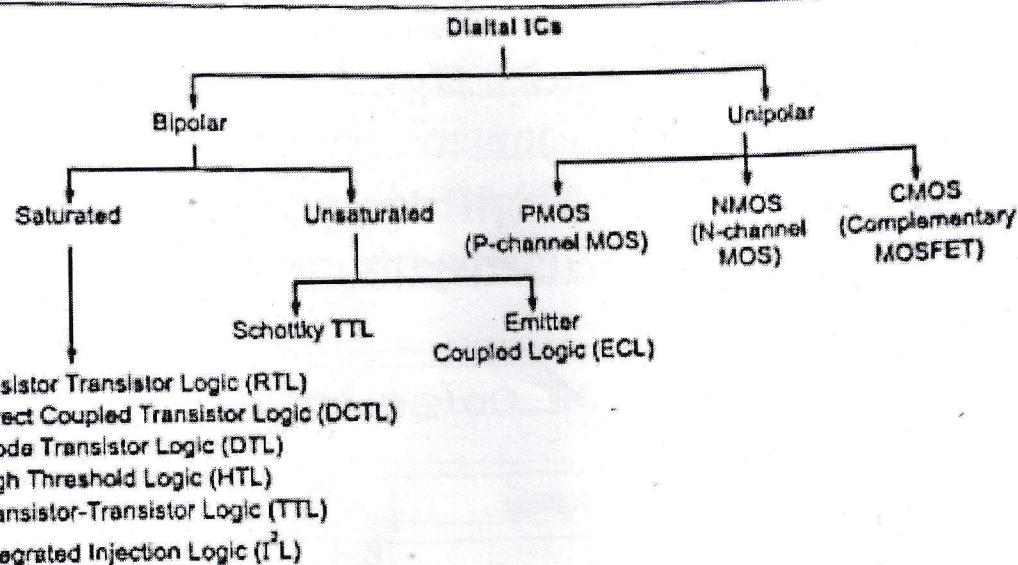
Logic 1 state Noise Margin  $\Delta_1 = V_{OH} - V_{IH}$

Logic 0 state noise Margin  $\Delta_0 = V_{IL} - V_{OL}$

⑤ Power supply requirement : voltage to operate, should be as less as possible.

⑥ Operating Temperature : It is the range of temperature in which an IC functions properly. It is in order of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The accepted temperature range of an IC is 0 to  $+70^{\circ}\text{C}$  for commercial and industrial applications.

### 2.3.2 Classification of Logic Families



- The digital IC families can be classified as:  
(i) Bipolar logic families (ii) Unipolar logic families

#### (I) Bipolar logic families:

There are two types of bipolar families:

- (a) Saturated (b) Unsaturated

(a) **Saturated:** In saturated bipolar logic, the transistors are driven into saturation and cut-off. These are further classified as:

- (i) Resistor-Transistor Logic (RTL).
- (ii) Direct Coupled Transistor Logic (DCTL).
- (iii) Diode Transistor Logic (DTL)
- (iv) High Threshold Logic (HTL)
- (v) Transistor Transistor Logic (TTL)
- (vi) Integrated Injection Logic ( $I^2L$ )

In unsaturated bipolar logic families, the transistor is not driven into saturation but operates between cut-off and active states. These are further classified as:

- (I) Schottky (TTL)
- (II) Emitter Coupled Logic (ECL)

#### (II) Unipolar logic families:

These families use MOSFET for their internal circuitry. The common MOS families are:

- (I) P-channel MOS (PMOS)
- (II) N-channel MOS (NMOS)
- (III) Complementary MOS (CMOS)

[W-14]

### 2.3.3 TTL Family

- TTL means transistor transistor logic. The ICs in TTL family perform the basic logic operations by using only transistors.
- This IC was first introduced in 1964 by Texas Instrument.

#### Important Specifications:

- Supply voltage : 74 series (4.75 to 2.25 V)  
54 series (4.5 to 5.5 V)

- 2. Temperature range** : 74 series : 0 to 70°C  
   54 series : -55 to 125°C  
**3. Voltage levels**                   :  $V_{L(\max.)} = 0.8 \text{ V}$   
    $V_{H(\min.)} = 0.4 \text{ V}$   
    $V_{TH(\min.)} = 2 \text{ V}$   
    $V_{OH(\min.)} = 2.4 \text{ V}$   
**4. Noise margin**                   : 0.4 V  
**5. Propagation delay**              : 10 ns  
**6. Power dissipation**              : 10 mW  
**7. Figure of merit**                 : 100  
**8. Fan-out**                         : 10

15-10

1. Low propagation delay, hence TTL circuits are fast.
  2. Power dissipation is independent of frequency.
  3. No latch ups.
  4. TTL is compatible to other logic families.
  5. High current sourcing and sinking capabilities.

#### **Drawbacks of TTL**

1. High power dissipation.
  2. Low fan-out.
  3. Poor noise immunity.
  4. Low component density.
  5. Require + 5V power supply to operate.

### **2.3.4 ECL (Emitter Coupled Logic)**

IS-13 W-17

This is an unsaturated bipolar family. Since the transistors do not go into saturation, these families have faster speeds.

#### **Specifications:**

1. Average power dissipation: 5 mW
  2. Propagation delay : 500 ps
  3. Noise margin : 150 mV
  4. Speed power product : 0.5 pJ
  5. Fan-out : 25

#### **Advantages:**

1. High fan-out.
  2. Can provide two simultaneous outputs.
  3. Fastest logic family.
  4. Excellent speed power product.

#### **Disadvantages:**

1. Limited logic swing, hence low noise immunity.
  2. High power dissipation.
  3. Voltage and current transients are generated due to high speeds.

### 2.3.5 CMOS Logic

- CMOS means Complementary MOSFET is obtained by using a P-channel MOSFET and N-channel MOSFET connected in series. The input is applied at the common gate terminal and output is taken from a common drain point.

## Specifications of CMOS:

1. Propagation delay: 105 ns.
2. Power dissipation per gate: 0.1 mW.
3. Fan-out: 50.
4. Speed power product: 10.5 pJ.
5. Power supply voltage: 3 V to 15 V.
6. Noise margin: High level: 1.45 V.  
Low level: 1.45 V.

## Advantages of CMOS:

1. High fan-out.
2. High packaging density.
3. High noise margin.
4. Low power dissipation.
5. Wide range of supply voltage.

## Disadvantages of CMOS:

1. These are susceptible to damages due to static charge.
2. Longer propagation delay.
3. Slower than TTL.
4. Latch ups can take place.

## 2.3.6 Comparison of TTL, CMOS and ECL

[S-17, 16, 15, 14; W-17, 16, 15]

Table 2.3

Parameter	TTL	CMOS	ECL
Basic Gates	NAND	NOR or NAND	OR-NOR
Fan-out	10	50	25
Propagation delay	10 ns	70-105 ns	2 ns
Power dissipation	10 mW	1.01 mW	40-55 mW
Speed power product	100 pJ	0.7 pJ	100 pJ
Clock rate	35 MHz	10 MHz	760 MHz

## 2.3.7 TTL NAND Gate with Totem-pole Output

[S-17, 15, 14; W-17, 16, 15]

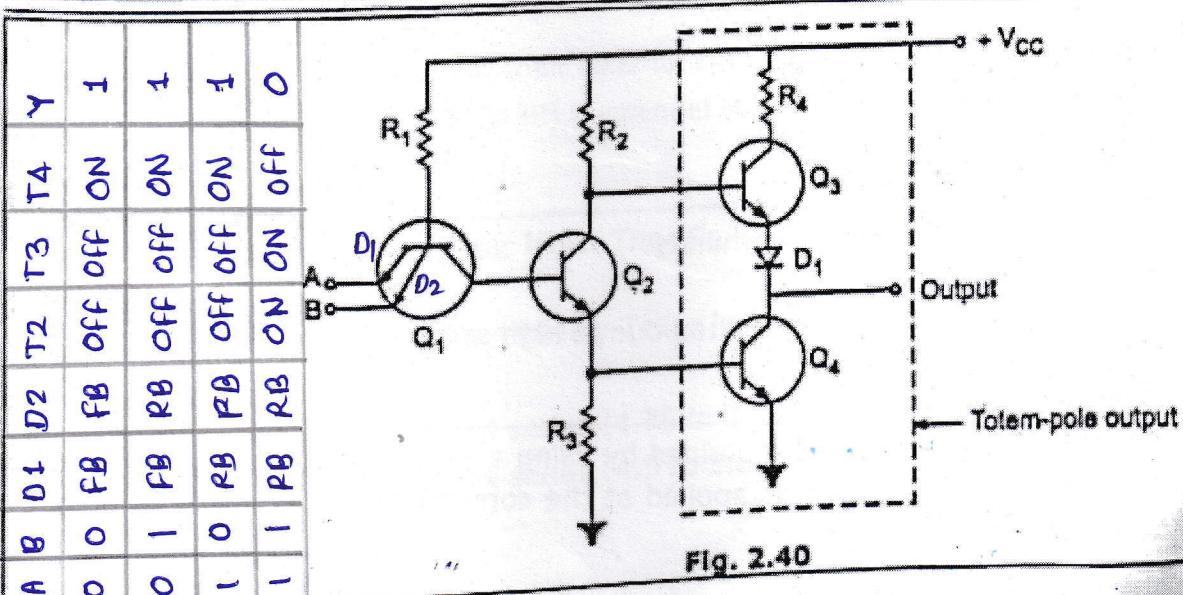


Fig. 2.40

- Totem-pole transistors are used because they produce a low output. Transistors  $Q_3$  and  $Q_4$  form a totem pole. Either  $Q_3$  acts as an emitter follower or  $Q_4$  is saturated.
- The output impedance is low even when  $Q_3$  is conducting or when  $Q_4$  is saturated.
- The output impedance of gate is not purely resistive but is partially capacitive. The capacitive load is contributed by the output capacitance of the transistor, capacitance of fan-out gates and other wiring stray capacitances. Whenever the output changes from low to high, the output transistor of the gate goes from saturation to cut-off and total load capacitance charges exponentially.
- The totem-pole output reduces propagation delay considerably.
- When output is low,  $Q_2$  and  $Q_4$  are in saturation. Diode  $D_1$  is provided to ensure that  $Q_3$  is cut-off when  $Q_4$  is saturated. As the output changes to a high state the transistors  $Q_2$  and  $Q_4$  go into cut-off region. As soon as  $Q_2$  turns off,  $Q_3$  starts conducting because the base of  $Q_3$  is connected to  $V_{CC}$ .
- The high current required to charge the load capacitance causes  $Q_3$  to saturate momentarily and output voltage increases with time constant  $RC$ .
- As the load charges, the output voltage rises and current in  $Q_3$  decreases, bringing the transistor into active region. Thus  $Q_3$  is in active region in steady-state condition and output voltage is 3.6 V.

#### Advantages:

1. Provides low output impedance. With output in logic '1' state,  $Q_3$  acts as an emitter follower with its low output impedance drives current into load. This low output impedance gives a short time constant for charging the capacitive load on the output side. Due to this the output voltage can change quickly from one state to another.
2. Low value of circuit power dissipation.

[W-12]

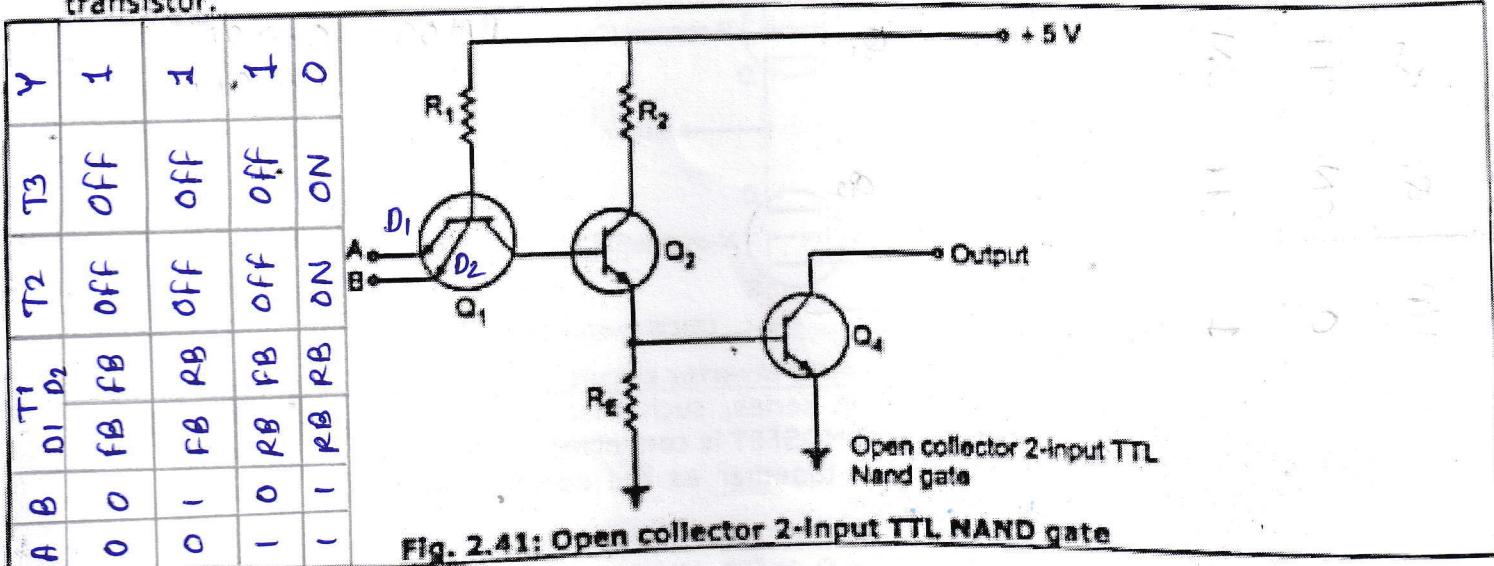
#### Disadvantages:

1. Wired-logic connection is not allowed with totem-pole output circuits.
2. Totem-pole output circuits generate large current spikes during switching.

[W-11, S-12]

### 2.3.8 TTL Open Collector Output

- The totem-pole output has a drawback that two outputs cannot be tied together.
- If the totem-pole outputs of two separate gates are tied together then a high current may cause overheating and deteriorate the performance, resulting in a device failure.
- Some TTL devices provide an open collector output. The outputs of two different gates with open collector output can be tied together. The output is taken from open collector terminal of transistor.



FB - forward bias

RB - Reverse bias

- Since the collector of  $Q_4$  is open, a gate will not work properly until an external pull-up resistor is connected, so that when  $Q_4$  is ON, the output is low and when  $Q_4$  is OFF, the output goes connected to  $V_{cc}$  through an external pull-up resistor. The connection is called a wired AND.

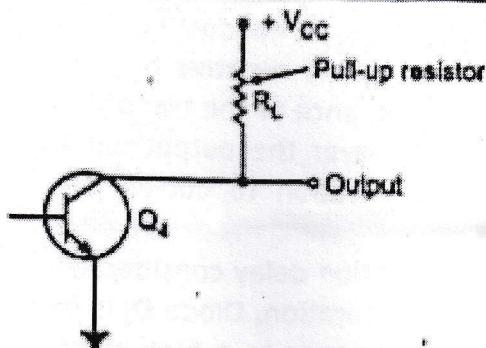


Fig. 2.42: Open collector output with pull-up resistor

#### Advantage:

Output of two gates can be tied together using wired AND technique.

#### Drawback:

Low switching speed, due to high value of pull-up resistor.

#### Comparison between Totem-pole and Open Collector output:

[W-14]

Table 2.4

Totem Pole	Open Collector
1. Output stage consists of transistors $Q_3$ , $Q_4$ and a diode $D_1$ .	1. Output stage consists of only pull-down transistor $Q_4$ .
2. Outputs of two gates cannot be tied together.	2. Outputs of two gates can be tied together using wired AND connection.
3. High switching speed.	3. Low switching speed.
4. Does not require external pull-up resistor.	4. Requires external pull-up resistor for proper operation of gate.

#### 2.3.9 CMOS Inverter

[W-16, 15; S-17]

- CMOS circuits consist of both NMOS and PMOS devices.
- These circuits consume low power and can be operated at high voltages, resulting in improved noise immunity.

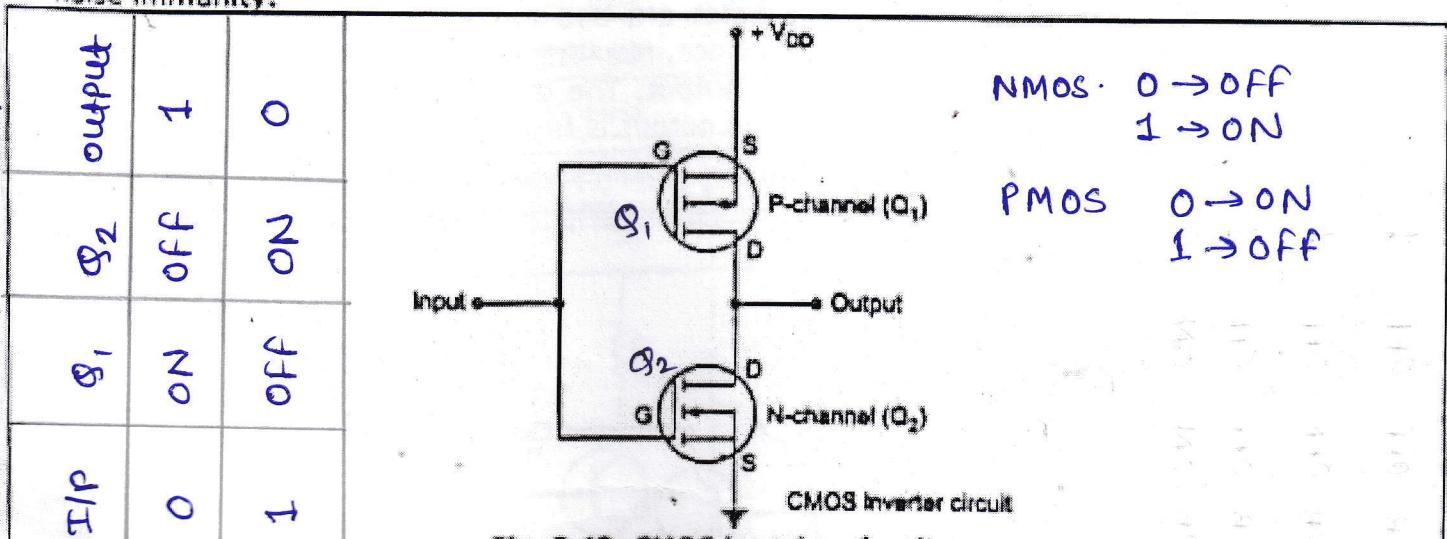


Fig. 2.43: CMOS Inverter circuit

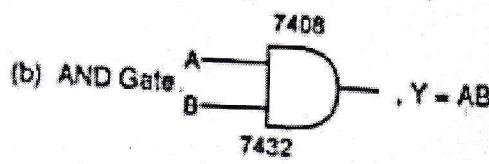
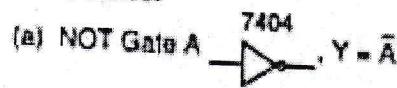
- It consists of two MOSFETs connected in series, such that source of P-channel MOSFET is connected to  $V_{dd}$  and source of N-channel MOSFET is connected to ground.
- The gates of two devices are connected together as the common input and the drains are connected together as the common output.
- When input is high, gate of  $Q_1$  is at 0 V w.r.t. to source of  $Q_1$ . Therefore,  $Q_1$  is OFF whereas gate of  $Q_2$  is at  $+V_{dd}$  w.r.t. its source. Therefore  $Q_2$  is ON. Hence  $V_{out} = 0 \text{ V}$ .

- When Input is low, gate of  $Q_1$  is at negative potential w.r.t. its source and  $Q_2$  has  $V_{DS} = 0$  V. Hence  $Q_1$  is ON and  $Q_2$  is OFF and the output voltage is  $= +V_{DD}$ .

**Table 2.5: Truth Table of Inverter**

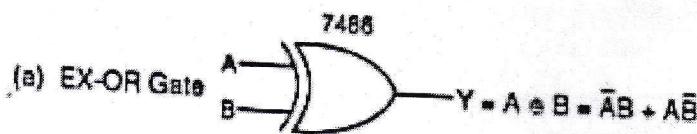
Input	$Q_1$	$Q_2$	Output
0	ON	OFF	1
1	OFF	ON	0

### 1. Basic Gates:



### Important Points

### 2. Derived Gates:



### 3. Universal Gates:

