NURUDEEN AGBONOGA

(972)-330-7430| onagbonoga@gmail.com| onagbonoga.github.io

SKILLS

Programming: C, C++, Python, PHP, CSS, HTML, SQL
Other: MATLAB, Simulink, Multisim, PSPICE, LabView, Verilog, VHDL, ANSYS HFSS (High Frequency Structure Simulator), Solid Edge, Eagle, Cadence Virtuoso, HSPICE

EDUCATION

UNIVERSITY OF TEXAS AT DALLAS Dallas, TX
Master of Science in Computer Engineering **GPA: 3.67/4.00** EXP *GRAD: May 2023*
UNIVERSITY OF TEXAS AT ARLINGTON Arlington, TX
Bachelor of Science in Electrical Engineering **GPA: 3.76/4.00** *GRAD: Dec 2019*

EXPERIENCE

GOOGLE San Francisco, CA
Software Engineering Intern *May 22 – Aug 22*

- Implemented software solutions for automatically detecting how a Fitbit fitness tracker is worn (on a user's wrist or clipped on their hip) to solve issues that led to over $200K in customer service costs by leveraging the device sensors and machine learning algorithms
- Built pipeline for data collection and iterating and optimizing machine learning classifiers to achieve 87% sensitivity and 89% specificity
- Integrated hip detection feature to the Fitbit tracker using techniques and parameters derived from the research phase of the project, with 100% code coverage from unit testing

ONCOR ELECTRIC DELIVERY Dallas, TX
Systems Engineer *Nov 20 – Jun 21*

- Co-ordinated with data team to provide real time power grid asset monitoring in a comprehensive graphical format for grid operators
- Incorporated personnel and public safety procedures into design and operation according to the North American Electric Reliability Corporations Critical Infrastructure Protection's protocols

THE SHOULDERS OF GIANTS Dallas, TX
Technical Mentor/ Research Assistant *Feb 20 – Sep 21*

- Volunteered as a research assistant on multiple engineering projects for STEM outreach. Tasks involved PCB design, project documentation, presenting and assembling projects with school children K-12
- Served as a technical mentor for high school students working on personal projects as well as structured projects offered by organization in various fields of engineering including biomedical and electrical

PROJECTS

Soft 16-Bit Microprocessor

- Designed a 16-bit soft pipelined microprocessor with a load store architecture capable of running user defined programs with a standard instruction set. The processor is implemented in the Zybo Z7-10 FPGA and comprises modules such as general-purpose registers, program and data memory, a stack and ability to handle interrupts

Auto-Carwash State Machine ASIC design

- Realized a state machine ASIC from the logic design and Verilog code to laying out and testing a library of standard cells in cadence virtuoso to placement and routing of final design. The final ASIC was made of 3000+ cells and it described the operation of an automatic car wash system

PUBLICATIONS

- Agbonoga N, Lalwani B, Jones E.C. Development of Affordable Smart Ingestible Pills for Safe Self Medication, International Supply Chain Technology Journal, 2019.