```
#include "STM32F4xx.h"
2
     #include <rtl.h>
 3
     #include <string.h>
 4
     //#include "pdm filter.h"
 5
 6
7
     uint16 t out1 ;
8
9
     /* Exported macros -----
                       ((((uint16_t)(A) & 0xff00) >> 8) | \
10
     #define HTONS(A)
11
                         (((uint16_t)(A) \& 0x00ff) << 8))
12
13
     void gpio config(void) {
14
     RCC->AHB1ENR \mid = ((1UL << 4));
15
16
17
                          ((1UL << 2*12) | // 4x LEDY out
     GPIOE->MODER
                     |=
18
                             (1UL << 2*13) |
19
                             (1UL << 2*14)
20
                             (1UL << 2*15));
21
     GPIOE->OTYPER
22
                    &= ~((1UL << 12) |
23
                             (1UL << 13) |
24
                             (1UL <<
                                       14) |
25
                             (1UL <<
                                      15) );
                                                 // Push - Pull
26
                    &= ~((3UL << 2*12) |
    GPIOE->OSPEEDR
27
                             (3UL << 2*13) |
28
                             (3UL << 2*14)
29
                             (3UL << 2*15));
30
     GPIOE->OSPEEDR
                     | =
                          ((2UL << 2*12) | // 50 Mhz out
31
                             (2UL << 2*13) |
32
                             (2UL << 2*14) |
33
                             (2UL << 2*15));
34
     GPIOE->PUPDR
                     \&= \sim ((3UL << 2*12))
35
                             (3UL << 2*13) |
36
                             (3UL << 2*14) |
37
                             (3UL << 2*15));
38
                          ((1UL << 2*12) | // Pull up
     GPIOE->PUPDR
                     |=
39
                             (1UL << 2*13) |
40
                             (1UL << 2*14)
41
                             (1UL << 2*15));
42
     }
43
44
     void klavesnice_config(void) {
45
     RCC->AHB1ENR \mid = ((1UL << 3));
46
47
48
     GPIOD->MODER
                          ((1UL << 2*6) | // vystup PD6..9
49
                             (1UL << 2*7)
50
                             (1UL << 2*8)
51
                             (1UL << 2*9) );
52
     GPIOD->OTYPER
                     &= ~((1UL <<
                                    6)
53
                             (1UL <<
                                      7) |
54
                             (1UL <<
                                     8) |
55
                                                // Push - Pull
                             (1UL <<
                                     9) );
56
     GPIOD->OSPEEDR
                       \&= ~((3UL << 2*6))
57
                             (3UL <<2*7) |
58
                             (3UL << 2*8) |
59
                             (3UL << 2*9));
                          ((2UL << 2*6) | // 50 Mhz out
60
     GPIOD->OSPEEDR
61
                             (2UL << 2*7)
62
                             (2UL << 2*8) |
```

```
63
                              (2UL << 2*9)
                                            );
 64
      GPIOD->PUPDR
                       \&= \sim ((3UL << 2*6))
 65
                              (3UL << 2*7)
 66
                              (3UL << 2*8)
 67
                              (3UL << 2*9) );
 68
 69
      GPIOD->MODER
                       &=
                           \sim ((3UL << 2*0) | // vstup PD0..2
 70
                              (3UL << 2*1) |
 71
                              (3UL << 2*2))
 72
 73
      GPIOD->PUPDR
                       \&= \sim ((3UL << 2*0))
 74
                              (3UL << 2*1) |
 75
                              (3UL << 2*2));
 76
      GPIOD->PUPDR
                       |= ((1UL << 2*0))|
 77
                              (1UL << 2*1)
 78
                              (1UL << 2*2));
 79
      }
 80
      void LCD config(void) {
      RCC->AHB1ENR \mid= ((1UL << 4)); // PE povolit clock
 81
 82
                    |= ( (1UL << 2*3) | // RS
      GPIOE->MODER
 83
                               (1UL << 2*4) | // R/W
 84
                               (1UL << 2*5) | // E
 85
                              (1UL << 2*6) | // vystup DB4..DB7 data
 86
                              (1UL << 2*7)
 87
                              (1UL << 2*8)
 88
                              (1UL << 2*9)
 89
                               (1UL << 2*10))
 90
      GPIOE->OTYPER
                      &= ~( (1UL << 3) |
 91
                               (1UL << 4)
 92
                               (1UL << 5) |
 93
                              (1UL <<
                                        6) |
 94
                              (1UL <<
                                        7) |
 95
                              (1UL <<
                                        8) |
 96
                                        9) |
                              (1UL <<
 97
                               (1UL << 10)
                                                   // Push - Pull
                                            );
 98
      GPIOE->OSPEEDR
                         \&= ~((3UL << 2*3))
 99
                               (3UL << 2*4)
100
                               (3UL << 2*5)
101
                               (3UL << 2*6)
102
                              (3UL << 2*7)
103
                              (3UL << 2*8)
104
                              (3UL << 2*9) |
                              (3UL << 2*10) ;
105
106
      GPIOE->OSPEEDR |=
                           ((2UL << 2*3) | // 50 Mhz out
107
                              (2UL << 2*4) |
                              (2UL << 2*5) |
108
109
                               (2UL << 2*6)
110
                              (2UL << 2*7) |
111
                              (2UL << 2*8)
112
                              (2UL << 2*9)
113
                             (2UL << 2*10));
114
      GPIOE->PUPDR
                      \&= \sim ((3UL << 2*3))
115
                              (3UL << 2*4)
116
                              (3UL << 2*5)
                               (3UL << 2*6)
117
118
                              (3UL << 2*7)
119
                              (3UL << 2*8)
120
                              (3UL << 2*9)
121
                             (3UL << 2*10)
122
      ; }
123
124
      void ADC_config(void) {
```

```
125
            RCC->AHB1ENR |= ((1UL ) ); // PA povolit clock
126
            RCC->APB2ENR \mid = 0x00000100;
                                          // povolení hodinového signálu k AD
      pøevodníku
127
           GPIOA->MODER \mid= (3UL << 2*1); // PA1 *** Vstup ch1 A/D prevod
128
            ADC1->SMPR2 |= (7UL << 3*1); // nastaveni casu samplovani pro kanal 1: 480
129
      cycles = 111
130
           ADC1->CR1 = 0x00000800; // nastaveni DISCEN do 1 Discontinuous mode
            ADC1->SQR1 = 0x00000000; // nastaveni poctu konvertovanych kanalu na 1
131
            ADC1->SQR3 = 0 \times 000000001; // konvertovat se bude kanal cislo 1
132
133
            ADC1->CR2 |= 1UL ; // PA povolit ADC1 => zapnuti AD prevodniku
134
      // ADC1->CR2 |= 0x08; // resetovani kalibracnich registru
135
      // while ((ADC1->CR2 & 0x08) != 0) {};// cekani na nacteni hodnot po resetu
136
      // ADC1->CR2 \mid= 0x04; // zapnuti autokalibrace
137
138
      // while ((ADC1->CR2 & 0 \times 04) != 0) {} ;// cekani na konec autokalibrace
139
140
     void Buzz config(void) {
141
            RCC->AHB1ENR |= ((1UL ) ); // PA povolit clock
142
              GPIOA->MODER \mid = (1UL << 2*8); // PA8 out
              GPIOA->OTYPER &= \sim (1UL << 8); // Output push-pull
143
              GPIOA->OSPEEDR &= \sim (3UL << 2*8)
144
              GPIOA->OSPEEDR \mid= (2UL << 2*8); // 50 Mhz out
145
146
             GPIOA->PUPDR &= \sim (3UL << 2*8); // No pull-up, pull-down
147
148
      void Mic config(void) {
149
               RCC->AHB1ENR \mid= ((1UL << 1 )); // PB povolit clock
              GPIOB->MODER \mid= (2UL << 2*10); // PB pin 10
150
             GPIOB->AFR[1] \mid= (5UL << 4*2); // AF 5 .... SPI2 SCK alter.f.
151
             GPIOB->OTYPER &= \sim (1UL << 10); // Output push-pull GPIOB->OSPEEDR &= \sim (3UL << 2*10);
152
153
154
             GPIOB->OSPEEDR \mid= (2UL << 2*10); // 50 Mhz out
155
             GPIOB->PUPDR &= \sim (3UL << 2*10); // No pull-up, pull-down
             RCC->AHB1ENR |= ((1UL << 2 ) ); // PC povolit clock
GPIOC->MODER |= (2UL << 2*3); // PC pin 3
156
157
             GPIOC->AFR[0] \mid= (5UL << 4*3); // AF 5 .... SPI2 MOSI alter.f.
158
             GPIOC->OTYPER |= (1UL << 3); // Output OPEN drain
159
             GPIOC->OSPEEDR &= \sim (3UL << 2*3);
160
             GPIOC->OSPEEDR \mid= (2UL << 2*3); // 50 Mhz out
161
162
             GPIOC->PUPDR &= \sim (3UL << 2*3); // No pull-up, pull-down
163
             RCC->APB1ENR \mid= (1UL << 14 ); // SPI2 clock enabled
164
                SPI2->CR1 |= ((1L << 1*1)| // CK to 1 when idle (1L << 1*0 )| // PHA = 1
165
      //
166
      //
                              (1L \ll 1*10) // Bit 10 RXONLY: Receive only
     //
167
                              (1L << 1*6) | // Bit 6 SPE: SPI enable
      //
168
                              (5L << 3) | // BR[2:0]: Baud rate control 101: fPCLK/64
169
     //
170
     //
                              (1L \ll 1*2)); // Bit 2 MSTR: Master selection
171
          SPI2->I2SCFGR |= (
172
                                 (1L << 1*3) | // CKPOL: Steady state clock polarity
                        (2L << 1*4)| // 10: LSB justified standard
173
                        (3L << 1*8) | // 11: Master - receive
174
                         (1L << 1*10) | // Bit 10 I2SE: I2S Enable
175
                        (1L << 11*1)) ; // Bit 11 I2SMOD: I2S mode selection
176
            SPI2->I2SPR |= (16L ) ; // Bit 7:0 I2SDIV: I2S Linear prescaler
177
178
            SPI2->I2SCFGR |=(1L << 1*10); // Bit 10 I2SE: I2S
      Enable
179
      180
181
        RCC->AHB1ENR |= ((1UL ) ); // PA povolit clock
            RCC->APB1ENR |= (1UL << 1*29 ); //DACEN: DAC interface clock enable
182
```

```
183
                                   (3UL << 2*4); // PA4
                                                                *** Vystup D/A prevod ***
            GPIOA->MODER |=
184
            DAC->CR \mid= (1UL << 1*0); // EN1: DAC channel 1 enable
185
                       // (7UL << 1*3 )); // TSEL1[2:0]: DAC channel 1 sw
      trigger
186
187
188
189
190
      void Delay (uint32 t ms) {
191
      os_itv_set (ms);
192
193
          os itv wait ();
194
        }
195
196
197
      uint8 t getkey(){
198
          uint8 t key= 0;
199
          uint16 t temp;
          while (!key) {
200
201
              Delay(1000);
                                 // delay for key
               GPIOD->ODR &= \sim ((15UL << 6));
202
203
               GPIOD->ODR \mid = ((7UL << 6));
204
                 temp = GPIOD->IDR ;
205
                 temp \&= 7;
206
                 switch (temp) {
                   case 6 : key ='.'; break ; // exchange '.'
207
                   case 5 : key ='0'; break ;
208
209
                   case 3 : key ='#'; break ;}
210
211
              GPIOD->ODR &= \sim ((15UL << 6));
212
              GPIOD \rightarrow ODR \mid = ((11UL << 6));
213
                temp = GPIOD->IDR ;
214
                 temp \&= 7;
215
                 switch (temp) {
216
                   case 6 : key ='7'; break ;
217
                   case 5 : key ='8'; break ;
                   case 3 : key ='9'; break ;}
218
219
220
              GPIOD->ODR &= \sim ((15UL << 6));
              GPIOD->ODR |= ((13UL << 6));
221
222
                temp = GPIOD->IDR ;
223
                 temp \&= 7;
                 switch (temp) {
224
225
                   case 6 : key ='4'; break ;
226
                   case 5 : key ='5'; break ;
227
                   case 3 : key ='6'; break ;}
228
229
              GPIOD->ODR &= \sim ((15UL << 6));
230
               GPIOD->ODR \mid = ((14UL << 6));
231
                 temp = GPIOD->IDR ;
232
                 temp \&= 7;
233
                 switch (temp) {
234
                   case 6 : key ='1'; break ;
235
                   case 5 : key ='2'; break ;
236
                   case 3 : key ='3'; break ;}
237
                 }
238
        return key;
239
240
241
      void write nibble res(uint16 t nibble) {
242
        uint16 t x;
243
            GPIOE -> BSRR = ((1UL << (3+16)))
                                                        //
```

```
244
                                   (1UL << (4+16))
                                                            //
245
                                   (1UL << (5+16));
                                                          // E=0
246
             Delay(1); // 100 us
247
             GPIOE->BSRR = (1UL << 5) ;
                                           // E=1 (clk)
248
             nibble &= 0 \times 0 F;
249
             nibble = nibble << 6 ;</pre>
250
             x = GPIOE \rightarrow ODR \& 0xFC3F ; // nuluj data
251
             GPIOE->ODR = nibble | x ; // pridej data
252
             Delay(1); // 100 us
253
             GPIOE->BSRR = (1UL << (5+16)) ;
                                                       E=0
             Delay(1); // 100 us
254
255
      }
256
257
      void write nibble(uint16 t nibble) {
258
        uint16 t x;
259
             GPIOE -> BSRR = ((1UL << (4+16)))
                                                          //
                                                               R/W=0
260
                                   (1UL << (5+16));
                                                          //
                                                               E=0
261
             GPIOE->BSRR = (1UL << 5);
                                            // E=1
                                                      (clk)
262
             nibble &= 0 \times 0 F;
263
             nibble = nibble << 6;</pre>
264
             x = GPIOE \rightarrow ODR \& 0xFC3F ; // nuluj data
265
             GPIOE->ODR = nibble | x ; // pridej data
266
             Delay(1); // 100 us
267
             GPIOE -> BSRR = (1UL << (5+16)) ;
                                                       E=0
268
             Delay(1); // 100 us
269
270
      void LCD ctrlWR(uint16 t cmd) {
             \overline{GPIOE} \rightarrow BSRR = (1UL << (3+16)); //
271
                                                        RS=0
272
             write nibble ( cmd >> 4);
273
             write_nibble (cmd);
274
               Delay(1); // 100 us
275
276
      void LCD dataWR(uint16 t cmd) {
277
             GPIOE -> BSRR = (1UL << 3); //
278
             write nibble ( cmd >> 4);
279
             write nibble (cmd);
280
               Delay(1); // 100 us
281
282
      void LCD ini (void) {
283
      GPIOE -> BSRR = (1UL << (10+16));
                                              // DIR=0
284
             Delay(800); // 80 ms
285
             write nibble res(0x3);
             Delay(50); // 5 ms
286
287
             write nibble res(0x3);
288
             Delay(10); // 1 ms
289
             write nibble res(0x3);
             Delay(10); \frac{1}{1} ms
290
291
             write nibble res(0x2);
292
             LCD ctrlWR(0x28);
293
             LCD ctrlWR(0x28);
294
             LCD ctrlWR(0 \times 0 C);
295
             LCD ctrlWR(0x06);
296
             LCD ctrlWR(0 \times 01);
297
             Delay(20); // 2 ms
298
299
      void puts_LCD(int radek, char* ukaz) {
        uint32_t i, adresa, n = 9;
300
301
        if (radek==1) adresa = 0x80; else adresa = 0xC0;
302
        LCD ctrlWR(adresa);
303
        for (i=0; i < n; ++i) {
304
               LCD dataWR(*ukaz);
305
               ++ukaz ;
```

```
306
               };
307
308
      unsigned char hextoascii(unsigned char cislo ){
309
        unsigned char asci;
310
        asci = cislo&0x0F;
311
        if (asci > 9) asci += 7;
312
        return (asci +='0') ;
313
      }
314
      void putasci(uint16 t cislo1){
315
          LCD dataWR(hextoascii(cislo1 >> 8));
316
          LCD dataWR(hextoascii(cislo1 >> 4));
317
          LCD dataWR(hextoascii(cislo1));
318
        }
319
      uint16 t sample 1( void ){
320
               ADC1->CR2 \mid= (0x40000000); // start mereni AD => SWSTART
321
              while ((ADC1->SR \& 0x02) == 0)\{\}; // cekani na konec mereni AD
322
               return (uint16 t) ADC1->DR;
323
324
      void bzz(uint16 t ms) {
325
      uint16 t i; ms *= 10;
326
         for (i=0; i < ms; ++i ) {
327
             GPIOA->ODR &= \sim (1UL << 8); // bzz off
328
            GPIOA \rightarrow ODR \mid = (1UL << 8); // bzz on
329
330
          Delay(5);
331
          } } ;
332
      void SERIAL ini() {
333
        RCC->APB1ENR |= (1UL << 17); // USART2 CLK ENABLE
334
        RCC->AHB1ENR |= (1UL << 0); // PORT A CLK ENABLE
        GPIOA->AFR[0] \mid = (7U << 4*2) \mid (7U << 4*3);
335
336
        /* Tx Configuration */
337
        GPIOA->MODER &= \sim (3UL << 2*2);
338
        GPIOA->MODER |= (2UL << 2*2); // PA2 Alternate Function
339
        GPIOA->OTYPER &= \sim (1UL << 2); // Pull
        GPIOA->OSPEEDR &= \sim (3UL << 2*2);
340
341
        GPIOA->OSPEEDR \mid= (2UL << 2*2); // 50Mhz
342
        GPIOA->PUPDR &= \sim (3UL << 2*2);
343
        GPIOA->PUPDR |= (1UL << 2*2); // PullUp
344
        /* Rx Configuration */
345
        GPIOA->MODER &= \sim (3UL << 2*3);
346
        GPIOA->MODER \mid = (2UL << 2*3);
                                           // PA2 Alternate Function
347
        USART2->BRR = 0x16D; // 115200 Bd
        USART2->CR1 \mid = (1U << 3) \mid (1U << 2); //Rxen Txen
348
349
        USART2 \rightarrow CR1 \mid = (1U \ll 13); // usart enable
350
      }
351
      void putchar1(char znak ) {
352
        { USART2->DR = (znak);
353
          while((!(USART2->SR & 0 \times 40))); // Transmision Complete
354
        } }
355
356
      void putserial(char* ukaz1 ) {
357
          unsigned char n=strlen(ukaz1) ;
358
        unsigned char i ;
359
          for (i=0; i<n;++i)</pre>
360
        { USART2->DR = (*ukaz1);
361
          while((!(USART2->SR & 0x40))); // Transmision Complete
362
          ++ukaz1;
363
        } }
364
      uint16 t sample1(){
365
          uint16 t znak;
366
         while(!(SPI2->SR & 0x1)){}; // Bit 0 RXNE: Receive buffer not empty
367
          znak = SPI2->DR;
```

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```
368
          return znak ;
369
370
      void read data mic(uint16 t* ukaz1, uint16 t delka) {
371
          uint16 t ind2 ;
372
          for ( ind2=0;ind2< delka; ++ind2 ) {</pre>
373
               while(!(SPI2->SR & 0x1)){}; // Bit 0 RXNE: Receive buffer not empty
                 (*ukaz1) = HTONS(SPI2->DR); // microphone
374
375
                   ++ukaz1 ;
376
377
      }
       void write da (uint16 t* ukaz1, uint16 t delka, uint16 t cas us) {
378
379
          uint16 t ind2, k;
            DAC->DHR12R1= 1500 ;
380
381
          for (ind2=0; ind2< delka; ++ind2 ) {</pre>
382
383
            out1 = (*ukaz1) + 1500;
384
      //
              if (out1 > 3000) \{ out1 = 1500; \}
385
            DAC->DHR12R1 = out1 ;
386
387
              ++ukaz1 ;
388
            for (k=0 ; k < cas us; ++k) {};
      //
389
                Delay(1);
390
               } }
391
392
```