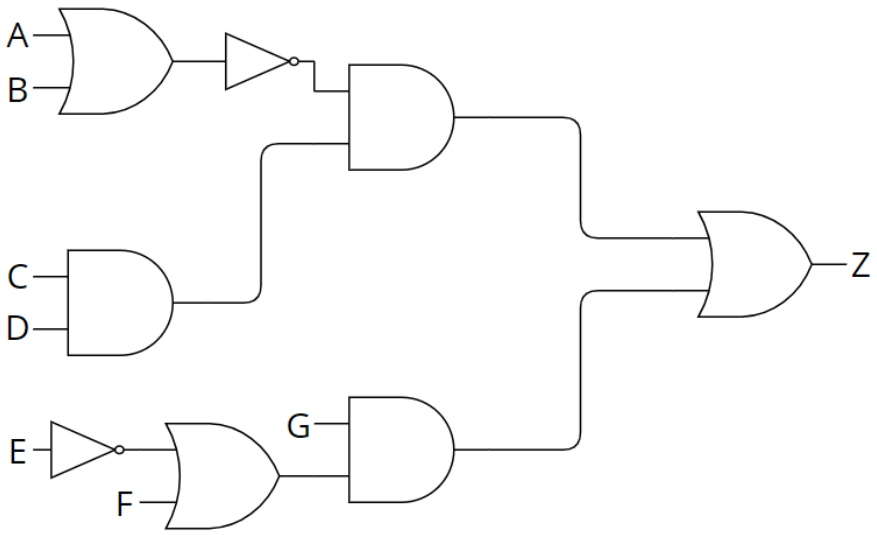
1. Implement the logic gates below.

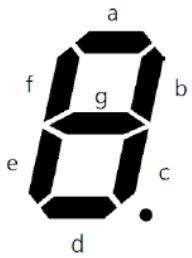


2. Implement the truth table below.

A	B	C	X	Y
0	0	0	1	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

3. Use 1-bit full adder to implement a 4-bit binary adder and convert output to Excess-3 code.

4. Design a Verilog module that takes in a four-digit input signal in 8421-BCD encoding and uses a seven-segment display to output the corresponding decimal value.



Digits	8421-BCD				Individual Segments						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

作要要求:

1. 請使用Gate level 撰寫

2. 每題皆須包含可執行之專案檔，程式中須包含註解

3. 每題皆須是單獨資料夾，全部壓縮成一個壓縮檔上傳

4. Testbench 必須包含至少 8 次以上之運算，時序為 timescale 1ns /1ns

5. 必須包含 Testbench 之 Wave 執行截圖(radix 須為 Unsigned decimal)

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