CS2100 Computer Organization
2022/23 Semester I (2210 Semester)
Assignment 2
SOLUTIONS

PLEASE READ THE FOLLOWING INSTRUCTIONS VERY CAREFULLY.

1. **DEADLINE:** The deadline for this assignment is **SATURDAY 12 NOVEMBER 2021, 11.59 PM**. Submission is **SOFTCOPY** in **PDF ONLY** on **LumiNUS**, NOT on Canvas! **No submissions will be accepted after the deadline.**

2. Fill your answers in the answer book called **CS2100Assg2AnsBk.docx** enclosed in the Assignment 2 ZIP file. Fill all your answers in this file and PDF it. Alternatively you may print out the answer book, write your answers manually, then scan your answers into a PDF file.

3. Name your file "AxxxxxxY.pdf", where AxxxxxxY is your student ID. **3 marks will be deducted if you do not follow this naming convention.**

4. You should complete this assignment on your own without discussing with anyone.

5. All of you should be able to find CS2100 in your LumiNUS. Navigate to Files->Assignment 2 Submissions->Txx, where Txx is your tutorial group number. Submit your PDF file there.

6. Ensure that your submission contains your **tutorial group number, name and student ID. 3 marks will be deducted if you do not fill in this information.**

7. Answers may be typed or handwritten. If it is the latter, please ensure that it is neat and legible. If we can't read your handwriting, we mark based on what we guess you wrote. We will also deduct marks for illegible handwriting.

8. Draw all circuits neatly. The rules in point 7 apply here too.

9. There are FOUR (4) QUESTIONS on FIVE (5) printed pages including this page.

10. You are again reminded to i) Name your PDF file AxxxxxxY.pdf where AxxxxxxY is your student ID, and ii) tutorial group number, name and student ID in your answer book. You may lose up to 6 marks if you fail to do either or both of these.

11. You are likewise reminded to submit on LumiNUS and not on Canvas.

The questions are worth **40 marks** in total.

Question 1 (Boolean Algebra – 8 MARKS)

a. Using the laws and theorems of Boolean Algebra alone, prove the Consensus Theorem. Apply at most one law or theorem on each line and write down the name of the law or theorem that you used. Marks will be deducted if these instructions are not followed. (3 marks)

Consensus theorem: X.Y + X'.Z + Y.Z = X.Y + X'.Z

Proof:

X.Y + X'.Z + Y.Z
= X.Y + X'.Z + 1.Y.Z (Identity Rule)
= X.Y + X'.Z + (X + X').Y.Z (Complement Rule)
= X.Y + X'.Z + X.Y.Z + X'.Y.Z (Distributive Rule)
= X.Y + X.Y.Z + X'.Z + X'.Z.Y (Commutative Rule)
= X.Y + X'.Z (Absorption Rule 1)

b. Prove therefore that (X' + Y).(X + Z').(Y + Z')) = (X' + Y).(X + Z'). Again, use at most one law or theorem on each line and name your law or theorem. Marks will be deducted if these are not done. (1 mark)

By Consensus Theorem:

X'.Y + X.Z' + Y.Z' = X'.Y + X.Z'

By Duality:

(X' + Y).(X + Z') = (X' + Y).(X + Z')

c. Using the laws and theorems of Boolean Algebra alone, find the simplest SOP expression for this function. As before use at most one law or theorem on each line and write down the name of the law or theorem that you used. (4 marks)

f(A, B, C, D) = $\sum m(0, 1, 2, 3, 4, 5, 6, 7, 12, 13, 14, 15)$

We will solve for f'(W, X, Y, Z) = $\sum m(8, 9, 10, 11)$

= A.B'.C'.D' + A.B'.C'.D + A.B'.C.D' + A.B'.C.D
= A.B'.C'.(D' + D) + A.B'.C.(D' + D) (Distributive Rule)
= A.B'.C'.1 + A.B'.C.1 (Complement Rule)
= A.B'.C' + A.B'.C (Identity Rule)
= A.B'.(C' + C) (Distributive Rule)
= A.B'.1 (Complement Rule)
= A.B' (Identity Rule)
f''(A, B, C, D) = (A.B')'
f(A, B, C, D) = A' + B'' (De-Morgan's Theorem)

f(A, B, C, D) = A' + B (Involution)

Question 2 (Combinational Circuits – 7 MARKS)

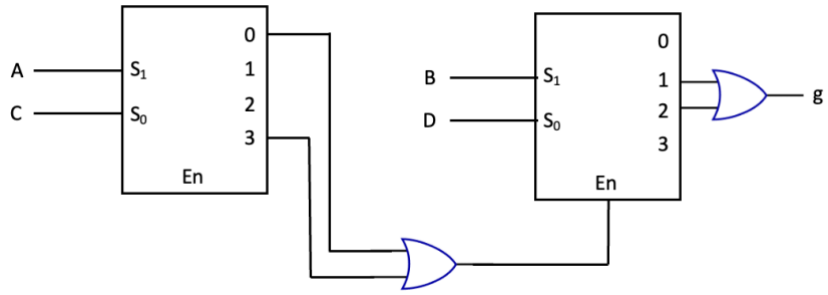
a. Implement the following function using at most two 2x4 decoders with positive (active-high) enable and positive (active high) outputs, and at most 2 OR gates. You are not allowed to use any other gates or devices. (3 marks)

g(A, B, C, D) = $\sum m(1, 4, 11, 14)$

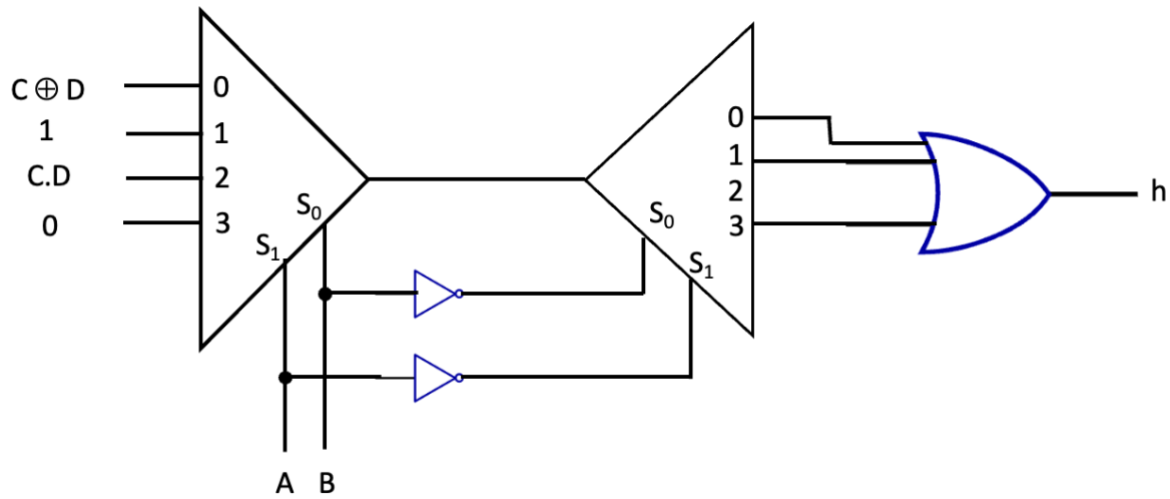
Observation:

m1 = 0001, m4 = 0100, m11 = 1011, m14 = 1110. Here AC = (m1 and m4) or 11 (m11 and m14).

In either case, BD = 01 or 10. So one **possible** circuit is:



b. Write down the simplified SOP of this circuit (4 marks):



Observations:

Input 0 -> Output 3
Input 1 -> Output 2
Input 2 -> Output 1
Input 3 -> Output 0

When AB = 01, output 10 in the DMUX is selected but not connected to the OR gate. So AB=01 is useless.

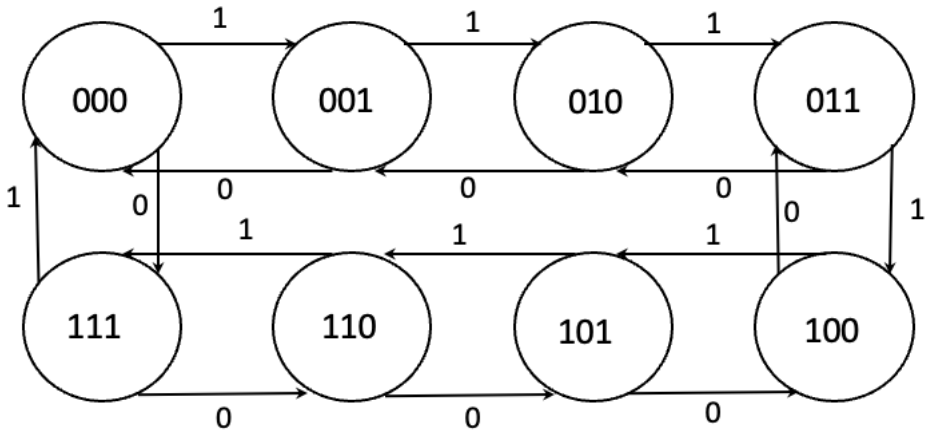
When AB=00, h=1 when C != D. So 0010 and 0001 are in h
When AB=10, h=1 when C=D=1, so 1011 is in h

So minterms in h are 1, 2 and 11.

h(A, B, C, D) = $\sum m(1, 2, 11)$

Question 3 (Sequential Circuits – 15 MARKS)

a. The state diagram below shows a 3-bit up/down counter. When x = 0, the counter counts upwards successively from 000 to 111, then goes restarts again ("rolls over") at 000. Similarly when x = 1, the counter counts backwards from 111 to 000, then rolls over again to 111 and continues counting down. Flipping x (e.g. 0 to 1 or 1 to 0) in between will change the direction of the count.



We want to Implement this counter using three T flip-flops A, B and C, and as few gates as possible.

i. Write down the simplified SOP for TA, TB and TC (3 marks).

A	B	C	x	A+	B+	C+	TA	TB	TC
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	0	0	1	1

0	0	1	1	0	0	0	0	0	1
0	1	0	0	0	1	1	0	0	1
0	1	0	1	0	0	1	0	1	1
0	1	1	0	1	0	0	1	1	1
0	1	1	1	0	1	0	0	0	1
1	0	0	0	1	0	1	0	0	1
1	0	0	1	0	1	1	1	1	1
1	0	1	0	1	1	0	0	1	1
1	0	1	1	1	0	0	0	0	1
1	1	0	0	1	1	1	0	0	1
1	1	0	1	1	0	1	0	1	1
1	1	1	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1

TA

TA =$\sum m(1,6,9,14)$

AB \ Cx	00	01	11	10
00		1		
01				1
11				1
10		1		

TA = B.C.x' + B'.C'.x

TB

TB=$\sum m(1,2,5,6,9,10,13,14)$

AB \ Cx	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

TB = C'.x + C.x'
= C XOR x

TC

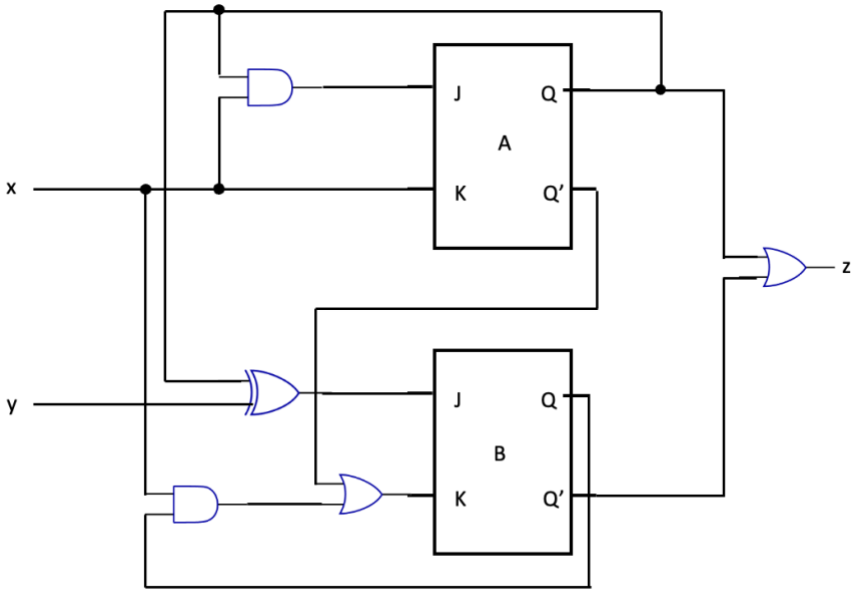
TC = 1

(Marking scheme: -1 mark for each incorrect equation)

ii. Draw the circuit for this counter. **Use as few gates as possible.** (4 marks).

(Omitted)

b. We are given the following circuit with two JK flip-flops A and B, two inputs x and y, and one output z.



i. Write down the expressions for JA, KA, JB and KB (4 marks).

JA = A.x

KA = x

JB = A ⊕ y

KB = A' + B.x

z = A + B'

ii. Draw the state diagram for this circuit (4 marks)

A	B	x	y	JA	KA	JB	KB	A+	B+	z
0	0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	1	0	1	1
0	0	1	0	0	1	0	1	0	0	1
0	0	1	1	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	1	1	0	0	0
0	1	1	0	0	1	0	1	0	0	0
0	1	1	1	0	1	1	1	0	0	0
1	0	0	0	0	0	1	0	1	1	1
1	0	0	1	0	0	0	0	1	0	1
1	0	1	0	1	1	1	0	0	1	1
1	0	1	1	1	1	0	0	0	0	1

1	1	0	0	0	0	1	0	1	1	1
1	1	0	1	0	0	0	0	1	1	1
1	1	1	0	1	1	1	1	0	0	1
1	1	1	1	1	1	0	1	0	0	1

(Diagram omitted)
https://www.cgdirector.com/can-you-mix-ram-brands-memory-modules/

Question 4 (Cache) (10 MARKS)

We have a computer with a 16-bit addressing space and 2-byte words. Consider a cache with a total size of 64 bytes.

We also have read accesses to the following memory locations:

0x14, 0x30, 0x22, 0x10, 0x52, 0x34, 0x56, 0x20, 0x16, 0x4

a. Consider a direct mapped cache with 4-word blocks. How many offset, index and tag bits will we have for this computer system? (1 mark)

1 word = 2 bytes
1 block = 4 words = 4 x 2 = 8 bytes
Total of 64 bytes, # of blocks = 64 / 8 = 8 blocks
# of index bits = 3
# of offset bits = 3
# of tag bits = 16 – 3 – 3 = 10

# of offset bits = 3
# of index bits = 3
# of tag bits = 10

(Marking Scheme: -1 mark for each incorrect answer)

b. What is the hit rate of this cache given the memory accesses above, in percent?. (3 marks)

Block #	Tag	Access
000		
001	0	0x4
010	~~0~~ ~~1~~ 0	~~0x14~~ ~~0x52~~ 0x16
011		
100	0	0x22
101		
110	0	0x30
111		

Addresses

0000000000 010 100 = 0x14 M
0000000000 110 000 = 0x30 M
0000000000 100 010 = 0x22 M
0000000000 010 000 = 0x10 H
0000000001 010 010 = 0x52. M
0000000000 110 100 = 0x34 H

0000000001 010 110 = 0x56 H
0000000000 100 000 = 0x20 H
0000000000 010 110 = 0x16 M
0000000000 001 000 = 0x4 M

Hit rate = 4/10 = 40%

(Marking Scheme: -2 marks if answer is off by +/- 10%, give 1 mark if answer is outside this range but working is shown)

c. If accessing the cache takes 2 ns while accessing the main memory takes 80 ns, what is the average memory access time for this computer system? Express your answer in nanoseconds. (2 mark)

$$0.4 \times 2 + 0.6 \times 82 = 50\ ns$$

(If equation given, give full marks, otherwise check according to answer in b)

d. Now consider a 2-way set associative cache, still with 4-word blocks. How many offset, index and tag bits will we have? (1 mark)

2-way Set Associative

# of bytes per word = 2
# of words per block = 4
# of bytes per block = 8
# of blocks = 64 /8 = 8
# of blocks per set = 2
# of sets = 8 / 2 = 4

# of offset bits = 3
# of index bits = 2
# of tag bits = 16 – 3 -2 = 11

e. What is the hit rate of this cache in percent for the memory accesses above, assuming a least-recently used replacement policy? (3 marks)

Set #	Tag	Access		Tag	Access
00	1	0x22 *			
01	0	0x4 *			

10	~~0~~ ~~1~~ 0	~~0x14~~ ~~0x34~~ 0x16 *		~~1~~ 2	~~0x30~~ 0x52
11					

Addresses

00000000000 10 100 = 0x14 M
00000000001 10 000 = 0x30 M
00000000001 00 010 = 0x22 M
00000000000 10 000 = 0x10 H
00000000010 10 010 = 0x52 M
00000000001 10 100 = 0x34 M

00000000010 10 110 = 0x56 H
00000000001 00 000 = 0x20 H
00000000000 10 110 = 0x16 M
00000000000 01 000 = 0x4 M

Hit rate = 3/10 = 30%.

(-2 marks if answer off by +/- 10%, give 1 mark if answer outside this range but working given)