Godson-T: an Efficient Many-Core Processor Exploring Thread-Level Parallelism
Godson-T: 一个探索线程级并行性的高效的多核处理器

Related
Godson-T series
2012 IEEE Micro (A-class)

- Godson-T an Efficient Many-Core Processor Exploring Thread-Level Parallelism

2013 J. Parallel Distrib. (B-class)

- Comput Scalability study of molecular dynamics simulation on Godson-T many-core architecture

2009 J. Comput. Sci. Technol.

- Godson-T: An Efficient Many-Core Architecture for Parallel Program Executions

2010 J. Comput. Sci. Technol.

- Landing Stencil Code on Godson-T

2010 IEEE FPT

- GVE Godson-T Verification Engine for Many-core Architecture Rapid Prototyping and Debugging

2011 Conf. Computing Frontiers

- Performance analysis and optimization of molecular dynamics simulation on Godson-T many-core processor

Godson series
2009 IEEE Micro

- Weiwu Hu, Jian Wang, Xiang Gao, Yunji Chen, Qi Liu, Guojie Li:Godson-3: A Scalable Multicore RISC Processor with x86 Emulation

2013 HPCC/EUC （C-class）

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- Godson-3B1500: A 32nm 1.35GHz 40W 172.8GFLOPS 8-core processor

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- The Godson Processors: Its Research, Development, and Contributions
- Design for Testability Features of Godson-3 Multicore Microprocessor

- Physical Implementation of the Eight-Core Godson-3B Microprocessor

2011 ISSCC

- Godson-3B: A 1GHz 40W 8-core 128GFLOPS processor in 65nm CMOS

Abstract

GODSON-T是一种用于并行科学计算的研究多核处理器，具有高效的性能和灵活的可编程性。
它还具有许多特性来实现芯片上资源的高效利用，例如

- 基于区域的缓存一致性协议
- 数据传输代理
- 硬件支持的同步机制。

最后，它还具有

- 高效的运行时系统
- 类pthread的编程模型
- 通用的并行库

使这种多核设计具有灵活的可编程性。

Architecture

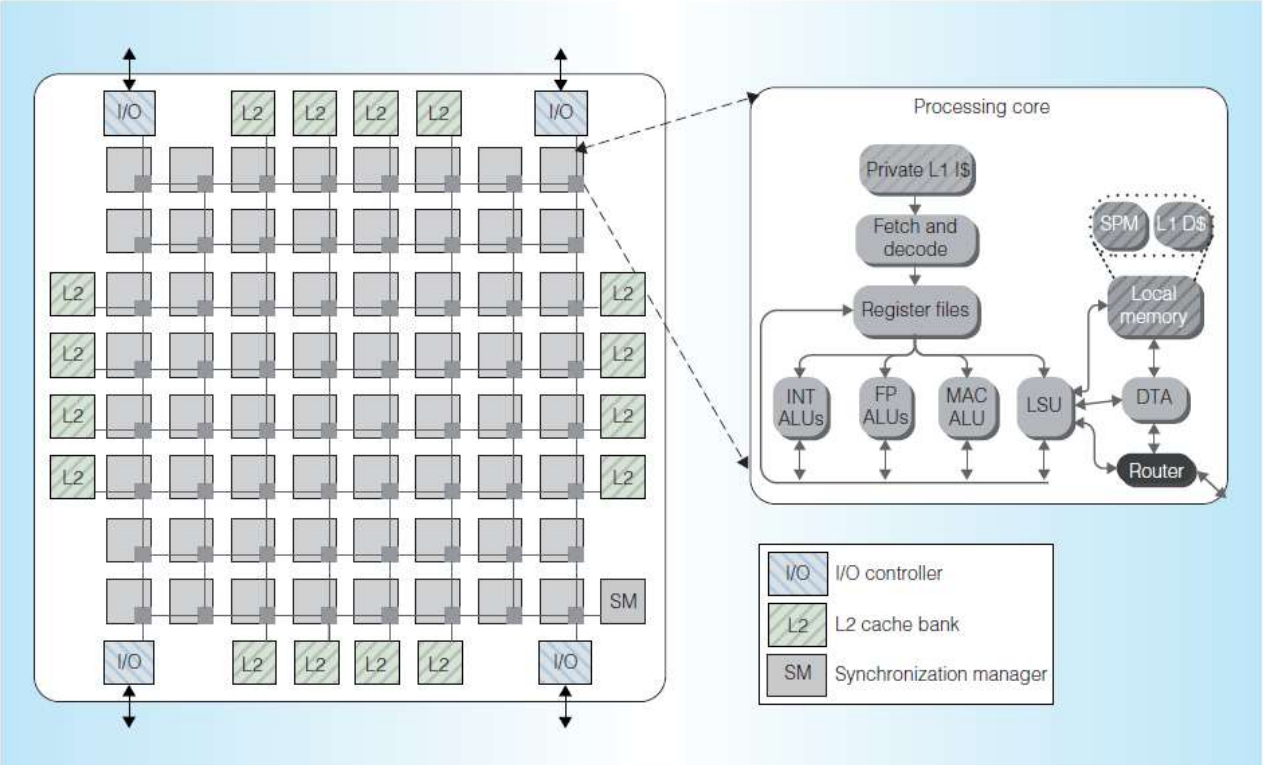
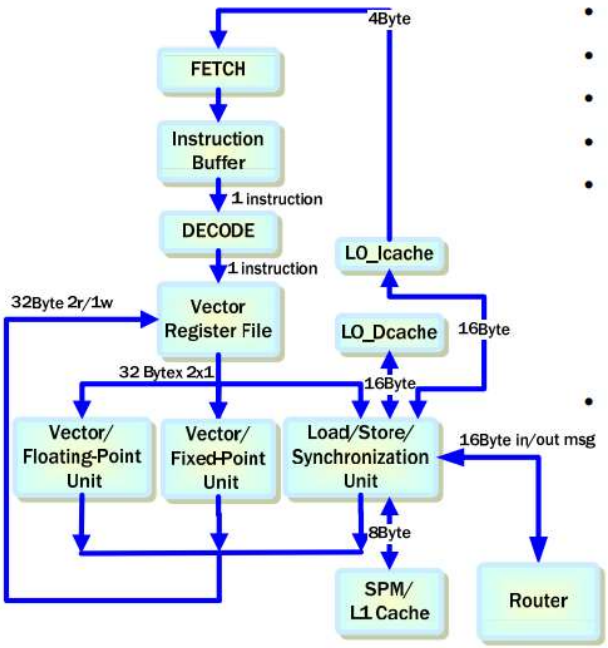


Figure 1. High-level block diagram of Godson-T. (ALU: arithmetic logic unit; D$: data cache; DTA: data transfer agent; I$: instruction cache; INT: integer; FP: floating point; LSU: load-store unit; L1: Level 1; L2: Level 2; MAC: multiply accumulate; SM: synchronization manager; SPM: scratch-pad memory.)

Processing Core



- ISA: MIPS (user), SIMD-ext., sync-ext.
- 8-stage pipeline
- Dual-issue per thread
- Fast level-1 memory
- 16KB private memory
  - Automatically mapped into stack address space
  - Full/empty bit tagged on each 64-bit slot enables efficient producer-consumer style synchronization
- Communication with external modules through message packets

8*8处理单元阵列，顺序双发射，1GHz，8-stage流水
流片原型为4*4=16核
每个核有一级cache，指令和数据各16KB-2路组相连
数据cache可配置为SPM（scratch-pad memory）
L2 cache全部核共享，每个128KB，同边的4个L2共享一个内存控制器
这两级的cache使用基于区域的缓存一致协议（RCC，region-based cache coherence）
每个核有一个数据传输代理（DTA，data transfer agent）
片上同步管理器（SM）支持锁、barrier和signal\wait同步
128-bit 包交换2D mesh网络， 确定X-Y路由，虫洞wormhole交换协议，折半带宽4TB/S

微体系结构特点

流水线
64*64bit 的寄存器堆可以在浮点和定点间转换，灵活性

缓存层次
RCC，数据一致性懒惰保证，区分共享访问和私有访问
region：open-region和closed-region原语之间的代码序列
在region内则认为是共享访问，保证一致性；在region外不保证一致性
让用户声明为粗/细粒度区域
L2支持2条额外原子操作，fetch,add,test,set

SPM
对每个32B cache line 提供8个full/empty位，
每个cache line的8bit写掩膜起到full/empty作用

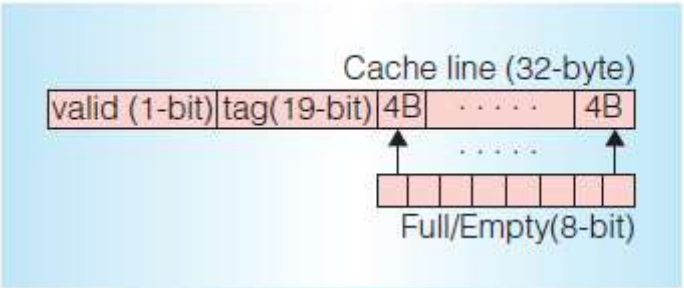


Figure 3. SPM full/empty bit configuration. When an on-chip private memory is configured as SPM, each cache line's 8-bit write mask works as a set of full/empty bits.

数据一致性依靠软件通过新指令保证：
sync_load : 等到full/empty bit设为full(1)后，读，再设empty(0)
sync_store：等到full/empty bit设为empty后，写，再设full
load_future：等full/empty bit设为full(1)
store_future：等full/empty bit设为empty
用于多生产者和多消费者

精心策划数据移动
请求缓存有3个入口项，保存有整个网络信息
流控制记录发送和接受filt数，超过阈值则stall

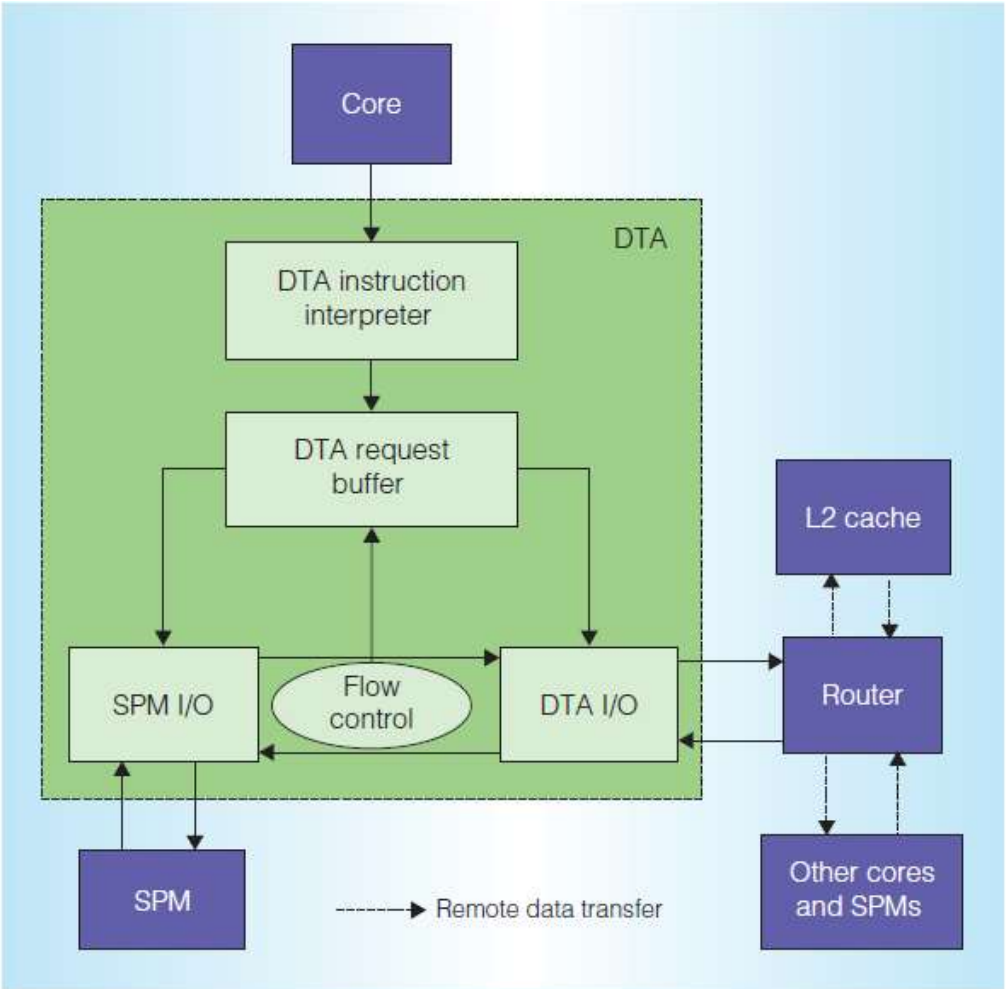
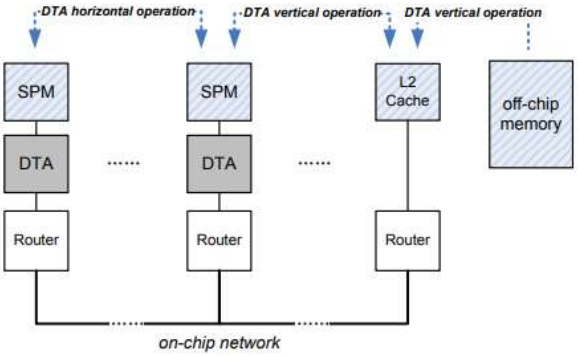
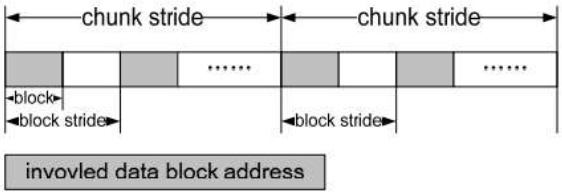


Figure 5. Block diagram of the DTA, which includes five modules: the DTA instruction interpreter, DTA request buffer, SPM I/O, flow controller, and DTA I/O.

Data Transfer Agent (DTA)



(a) vertical and horizontal DTA operations



(b) 2D strided DTA operations

- **Programmable asynchronous data transfer agent**
  - Support vertical and horizontal DTA operations (such as prefetch)
  - Data transfers between multi-dimension addresses (such as matrix inversion)
  - Network load perception, automatically flow control (improve bandwidth-efficiency)
  - Support fine-grain synchronous operations

同步管理器SM有128项，4路组相连，Core_ID和Sync_ID用于索引
State包含 lock_acquired 或者 lock_waiting
Bar_Count 只用来 barrier 同步，记录还未到达barrier的数量
Next指向下一项（等待同一个lock或barrier的另一个core）

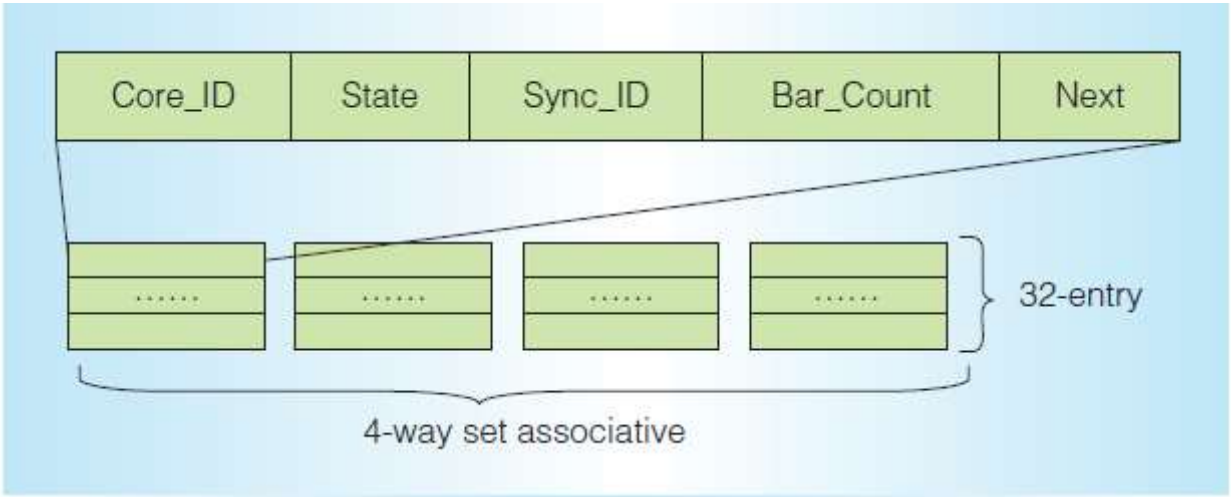


Figure 7. The SM structure. A centric on-chip synchronization manager helps to implement faster synchronization without accessing off-chip shared memory.

片上网络 gMesh
2D mesh
为避免死锁，设计2个网络（请求网络和回复网络）

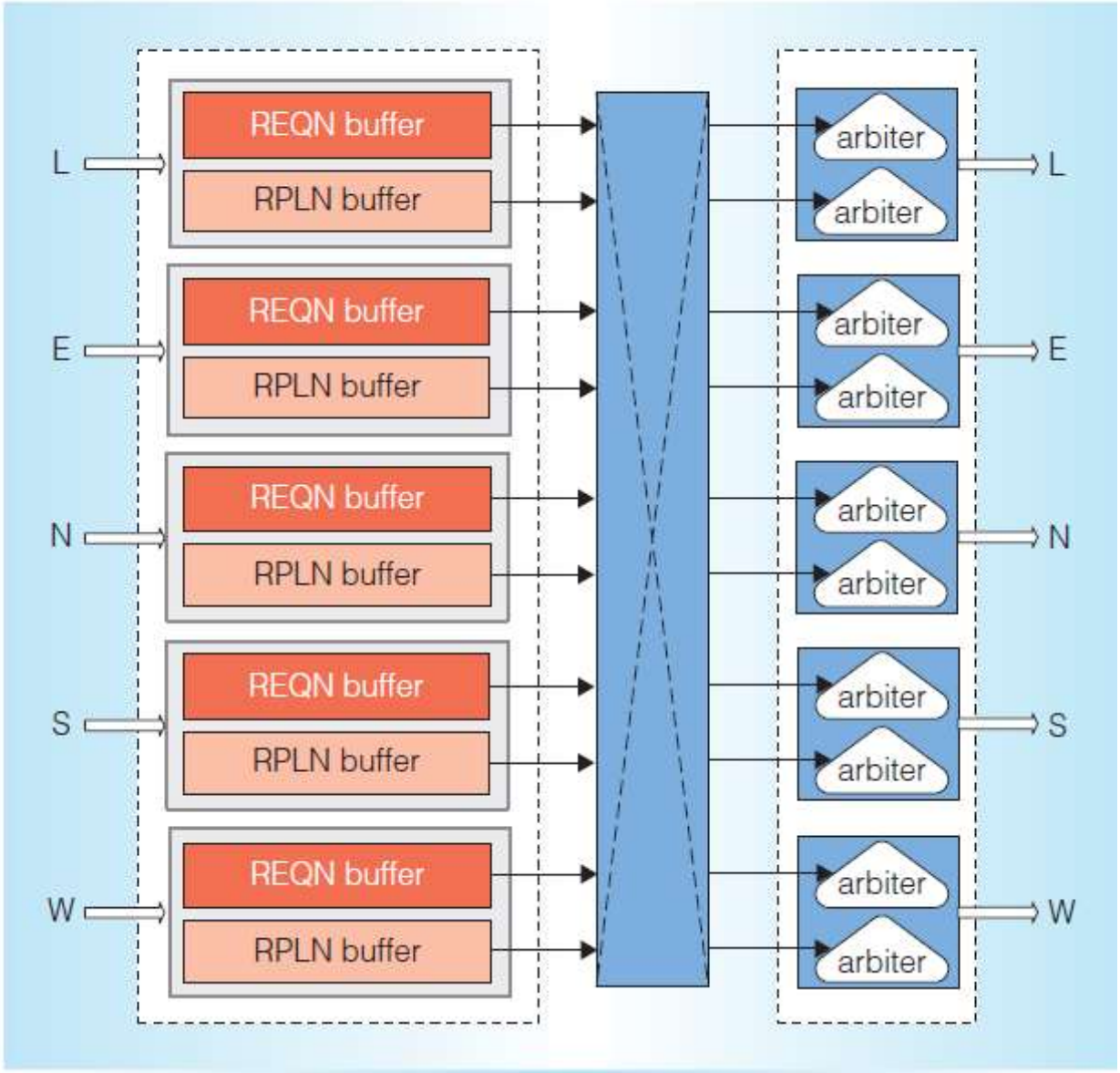


Figure 8. Overview of a wormhole router used in two independent on-chip networks. Each router connects in five directions: east, west, north, south, and to the local core. Each link contains two 128-bit unidirectional links. (REQN: request network; RPLN: reply network; L: local core; E: east; N: north; S: south; W: west; X: crossbar.)

软件环境

类Pthread C库用于任务调度 API

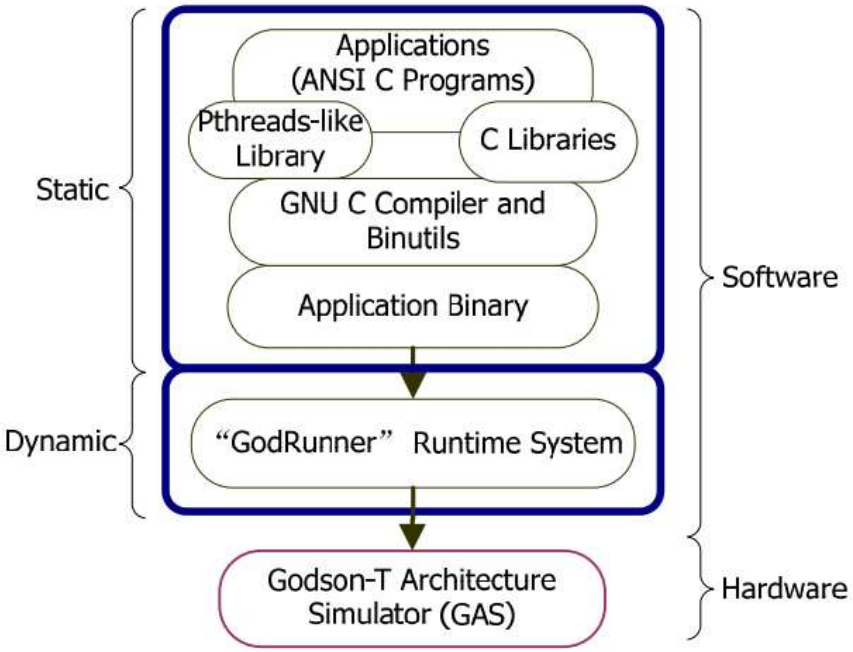
GodRunner 软件运行系统

硬件线程单元的有效抽象和动态负载平衡

上下文切换开销大->非打断式

灵活协助不同任务调度算法：工作窃取和条件生成

GodRunner: Software Runtime System



编译器优化
封装 特定算法优化 到 优化模式， 简单的标记式
可扩展基于模式优化指导框架
EPOD (Extendable Pattern-Oriented Optimization Directives)

多核快速模拟
Godson-T Architecture Simulator (GAS) 时钟精确、时间驱动
并行离散时间模拟方法 parallel discrete event simulation (PDES) method
通过多线程加速模拟：将全局事件队列分割为每个逻辑处理器的独立队列，通过PDES保持队列间的同步
10.9x的加速比

Software

GVE Software Stack

GT-Monitor
Watch GT Running Status

GT-Gcc
Compiler for Godson-T

GT-Debugger
Troubleshooting tools

GT-Loader
Load Runtime/Program

Runtime
Schedule Tasks on Cores

Linux Driver
For PCI-E Communication

物理实现

16核原型芯片 CMOS 65-nm 面积200mm^2