Roll Number: _____

Thapar Institute of Engineering & Technology, Patiala

Department of Computer Science &Engineering

WRITTEN EXAMINATION (2021)

B. E. (COE) (Third Year): Semester-V	Course Code: UCS510/UCS507 Course Name: Computer Architecture and Organization
October 21, 2021	Thursday, 10:20AM – 12:20 Noon
Duration: 2 Hours, Max. Marks: 50	Instructor: AB, SS, RS, SOL

Instructions: Attempt any five questions. Assume missing data, if any, suitably.

Q.1 (a) Write the simplified boolean expression of 3 input variables that generates output 1 if and only if the number of 1's in the input is prime (i.e., 2, 3 or 5). **(5)**

(b) The following bit pattern represents a floating-point number in IEEE 754 single precision format 1 10000011 01000000000000000000000. Determine the value of the number in decimal form. **(5)**

Q.2 (a) Design an adder/subtractor circuit with carry input Cin and two inputs A and B. When Cin=0, the circuit performs A + B. When Cin=1, the circuit performs A – B, Verify the circuit using A=5 and B=2. **(4)**

(b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the block diagram for two stages. **(6)**

S	Cin=0	Cin=1
0	A+B	A-B
1	A+1	A-1

Q.3 (a) Specify the step-by-step micro-operations (Fetch, Decode and Execute) for the BUN and BSA memory reference instructions. **(6)**

(b) The content of AC in the basic Computer is hexadecimal AB98 and the initial value of E is 0. Determine the contents of AC, IR, AR and E in hexadecimal after the execution of instructions at content of IR is 7200 (CMA). Execute the remaining 3 sequence instructions as described in the table below and the starting value of PC is 2FF. **(4)**

	AC	IR	AR	E
CMA				
CME				
CIR				
CIL				

Q.4 (a) The memory unit of a computer has 2K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of nine addressing modes, a register address field to specify one of 61 processor registers, and a memory address. Specify the instruction format and number of bits in each field if the instruction is in one memory word. **(4)**

(b) Perform multiplication of signed 2's complement numbers (-13) x (5) using the Booth's algorithm. Specify the result at each step of the algorithm by clearly taking the value n as 5. **(6)**

Q.5 (a) The two-word instruction at address 300 and 301 is a "load to AC" instruction with an address field equal to 600. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. PC has the value 300 for fetching this instruction. The content of processor register R1 is 500, and the content of an index register XR is 200. The contents of memory at locations 499, 500, 600, 700, 800, 802, 900, 902 are 550, 800, 900, 1000, 650, 350, 400, 700 respectively. Determine the Effective Address and the content of AC for the following addressing modes: **(6)**

(i) Direct address (ii) Immediate operand (iii) Indirect address
(iv) Relative address (v) Indexed address (vi) Register indirect

(b) A computer has 64-bit instructions and 20-bit addresses. If there are 512 two address instructions. How many one address instructions can be formulated? **(4)**

Q.6 (a) A computer uses RAM chips of 4Gx16 bytes capacity. How many chips are needed and how should their address lines to be connected to implement the memory of 16Gx16 bytes. Construct the memory map to show the connections required to implement the 16G X16 RAM. **(7)**

(b) A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. Determine the number of bits for TAG, Set and Word offset fields respectively. **(3)**

Q.7 (a) Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics: **(7)**

Memory level	Access Time	Capacity	Cost/Kbyte	Hit rate
Cache	25 ns	512 Kbyte	₹1.25	0.98
Main memory	903 ns	32 Mbyte	₹0.2	0.9
Disk	4 ms	39.8 Gbyte	₹0.0002	1

(i) To increase the hit rate of main memory from 0.9 to 0.95, we have to double the size of main memory. Calculate the size of disk which we have to sacrifice while increasing the hit rate of the main memory, if the total cost of memory hierarchy will not change.
(ii) Calculate new effective memory access time?

(b) Consider a direct mapped cache of size 256 KB with block size 1 KB. There are 7 bits in the tag field. Consider that the memory is byte addressable and determine the followings: **(3)**

(i) Size of main memory (ii) Tag directory size