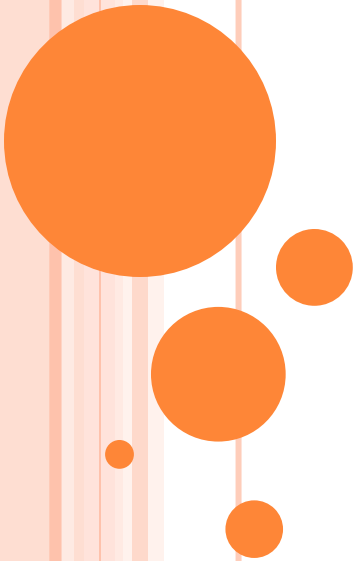
Comparison of Pentium processor with 80386 and 80486 processor's



Limitations of 80286 that lead to 80386

- 80286 has only a 16 bit processor.
- Maximum segment size of 80286 is 64 KB.
- 80286 cannot be easily switched between real mode and protected mode because resetting was required.
- The amount of memory addressable by the 80286 is 16M byte.
- To increase the over all system performance.

The 80386 microprocessor

- A 32-bit microprocessor introduced by Intel in 1985.
- The chip of 80386 contains 132 pins.
- It has total 129 instructions.
- It has 32 bit data bus 32 bit address bus.
- The execution of the instructions is highly pipelined and the processor is designed to operate in a multiuser and multitasking.
- Software written for the 8088, 8086, 80186 and 80286 will also run on 386.

- The address bus is capable of addressing over 4 gigabytes of physical memory.
- Virtual addressing pushing this over 64 terabytes of storage.
- 80387 coprocessor is used.
- The processor can operate in two modes:
  - In the **real mode** physical address space is 1Mbytes and maximum size of segment is 64KB.
  - In the **protected mode** address space is 4G bytes and maximum size of segment is upto entire physical addressing space.

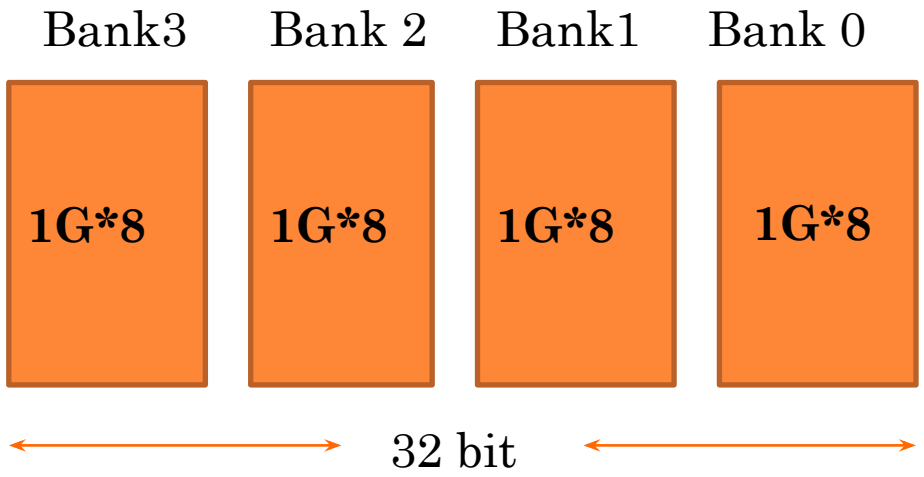
- 80386 processor is available in 2 different versions.
  - **386DX**
    - 32 bit address bus and 32 bit data bus.
    - 132 pins package.
  - **386SX**
    - 24 bit address bus and 16 bit data bus.
    - 100 pin package.
    - The lower cost package and ease of interfacing 8 bit and 16 bit memory and peripherals.
    - But the address range and memory transfer rate are lower than that of 386DX.

Register set-80386

- It included all eight general purpose registers plus the four segment registers.
- The general purpose registers were 16 bit wide in earlier machines, but in 386 these registers can be extended to 32 bit.
- Their new names are EAX, EBX, ECX and so on.
- Two additional 16 bit segment are included FS and GS.

Memory System of the 80386

The memory bank are accessed via four bank enable signals BE0, BE1, BE2 and BE3.



BE0, BE1, BE2 and BE3 are active low signals.

The 80486 microprocessor

- 80486 is the next in Intel's upward compatible 80x86 architecture.
- Only few differences between the 80486 and 80386, but these differences created a significant performance improvement.
- 32 bit microprocessor and same register set as 80386.
- Few additional instructions were added to its instruction set.
- 4 gigabyte addressing space .

Improvements made in 80486 over 80386

- 80486 was powered with a 8KB cache memory.
- This improved the speed of 80486 processor to great extent.
- Some new 80486 instructions are included to maintain the cache.
- It uses four way set associative cache.
- 80486 also uses a co-processor similar to 80387 used with 80386.
- But this co-processor is integrated on the chip allows it to execute instructions 3 times faster as 386/387 combination.

- The new design of 80486 allows the instruction to execute with fewer clock cycles.
- 486 is packed with 168 pin grid array package instead of the 132 pin used for 386 processor.
- This additional pin's made room for the additional signals.
- This new design of 80486 allows the instruction to execute with fewer clock cycles.
- These small differences made 80486 more powerful processor.

The Pentium Processor

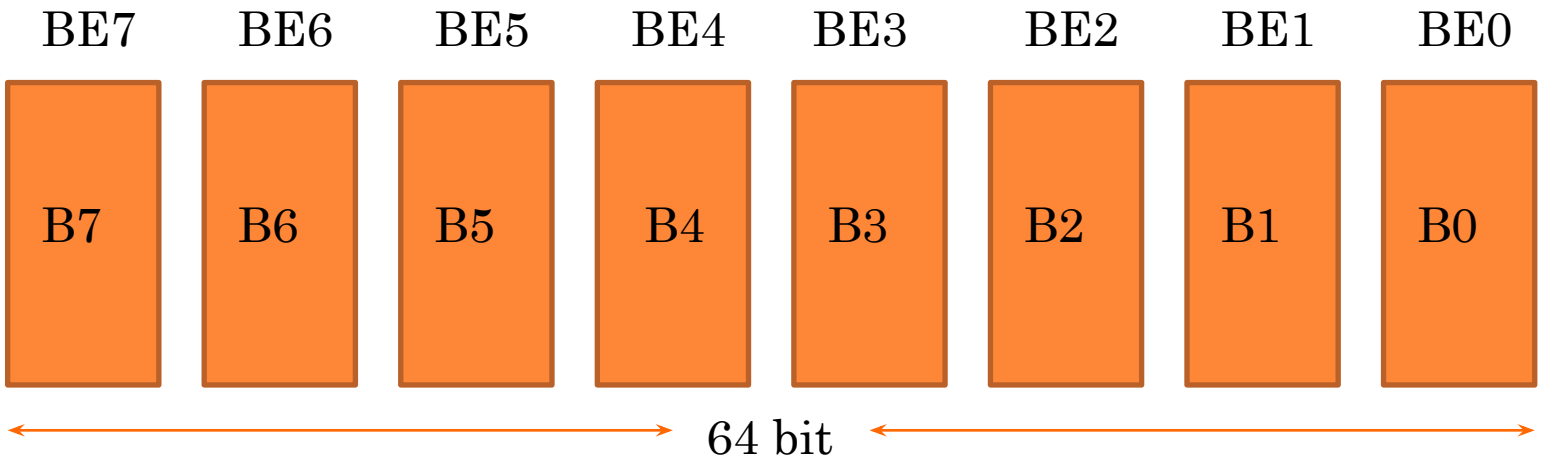
Why the name Pentium ?????

- Intel wanted to prevent their competitors from branding their processors with similar names, as AMD had done with their Am486.
- The name Pentium is originally derived from the Greek word *pente* meaning '**five**' as the series was Intel's 5th generation microarchitecture.

The Pentium Processor

- Upward compatibility has been maintained.
- It can run all programs written for any 80x86 line, but does so at a double the speed of fastest 80486.
- Pentium is mixture of both CISC and RISC technologies.
- All the prior 80x86 processor are considered as CISC processor.
- The addition of RISC aspects lead to additional performance improvement.

- It uses 64 bit data bus to address memory organized in 8 banks, each bank contains 512 MB of data.
- Each bank can store a byte of data.



Memory System of Pentium

- All these bank enable signals are active low.

Improvements of Pentium over 80x86

- **Separate 8KB data** and **instruction** cache memory.
- **Dual Integer pipelines** are present but only single integer pipeline is present in 80486.
- **Branch Prediction Logic.**

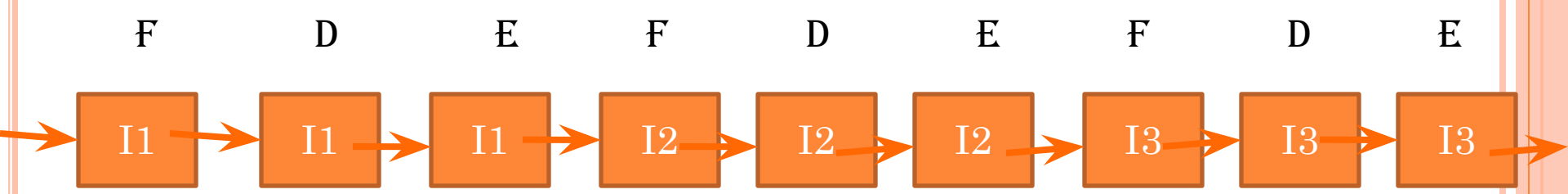
Cache Memory

- The Pentium contains two 8K-byte cache.
- An 8 byte instruction cache, which stores the instruction.
- An 8 byte data cache, stores the data used by the instructions.
- In the 80486 with unified cache, a program that was data intensive quickly fills the cache, allowing less room for instructions.
- In Pentium this cannot occur because of the separate instruction cache.

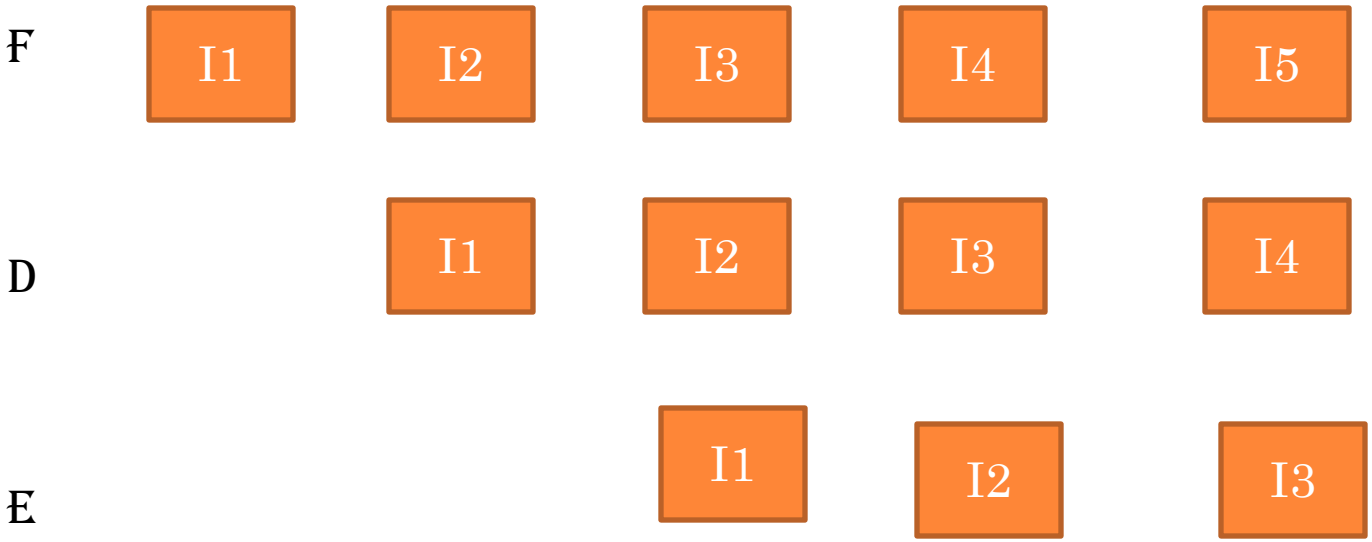
PIPELINING

- It is a technique used to enable one instruction to complete with each clock cycle.
- In Pentium there are two instruction pipelines, the U pipeline and V pipeline.
- These pipelines are responsible for executing 80x86 instructions.
- During Execution the U and V pipelines are capable of executing two integer instructions at the same time and one floating point instructions.

Pipelining



CLOCK CYCLE 1 2 3 4 5 6 7 8 9



CLOCK CYCLE 1 2 3 4 5

- On a non pipelined machine 9 clock cycles are needed for the individual fetch, decode and execute cycle.
- On a pipelined machine fetch, decode and execute operations are performed in parallel only 5 cycles are needed to execute the same three instructions.
- The First instructions needed 3 cycles to complete.
- Additional instructions complete at rate of 1 per cycle.

- The Instruction pipelines are five-stage pipelines and capable of independent operations.

- The **Five-Stages** are,

  PF – Pre Fetch

  D1 – Instruction Decode

  D2 – Address Generate

  EX - Execute Cache and ALU Access.

  WB – Write Back

- The U pipeline can execute any processor instruction where as V pipeline only execute Simple Instruction.

Branch Prediction Logic

- The purpose of branch prediction logic is to reduce the time required for a branch caused by internal delays.
- The microprocessor begins pre-fetch instruction at the branch address.
- The instructions are loaded into the instruction cache.
- When the branch occurs, the instruction are present and allow the branch to execute in one clock period.
- If the branch prediction logic errors, the branch requires an extra three clock cycles.

Speed of Processors

- The 80286 - 25 MHz
- The 80386 - 40MHz
- The 80486 - 60 MHz
- The Pentium -90 MHz

Thank you