Roll Number: _____

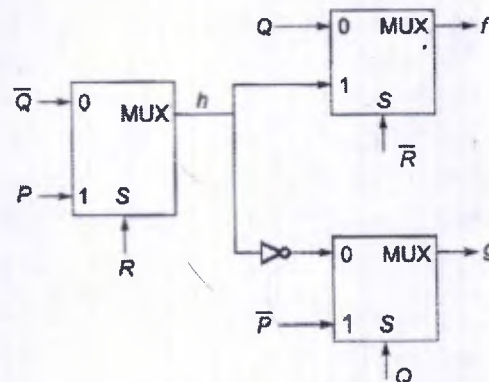|	
B. E. (Second Year): Semester-III (CSE)	Course Code: UCS 510 Course Name: Computer Architecture & Organization
Date: 29 Jan, 2021	Time: 11.00 – 1.00 Hrs
Time: 2 Hours, M. Marks: 50	Name of Faculty: Dr. Rupali Bhardwaj, Vivek Gupta

Note: Attempt any five questions and attempted questions should be in sequence.

Q1 (a) Consider the following multiplexer. Find the value of output function 'g'. (4)

(b) Consider a four variable function $f(A, B, C, D) = \sum (5,7,11,12) + d(3,11,13,15)$. Find the minimal expression. (6)

Q2 (a) Design a 2-bit arithmetic circuit with one selection variable S and two n-bit data inputs A & B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first four stages. (6)

S	$C_{in}=0$	$C_{in}=1$
0	D=A+B	D=A-B
1	D=A+1	D=A-1

(b) Convert $(76.125)_{10}$ into IEEE single precision representation. (4)

Q3 (a) Describe Instruction cycle in brief with flowchart. Specify corresponding micro operations at each stage. (5)

(b) Assume an instruction set that uses a fixed 16-bit instruction length. Operand specifiers are 6 bits in length. There are K two operand instructions and L zero operand instructions. What is the maximum number of one operand instructions that can be supported? (no three-address instruction exists). **P.T.O.** (5)

Q4 (a) ISZ indirect instruction is fetched from memory and executed using registers PC, (4) AR, DR, and IR of the basic computer. The initial content of PC is F2C. The content of memory F2C is E78F. The content of memory at address 78F is 895C. The content of memory at address 95C is FFF0. The value of each register updated at each timing signal recorded in the table given below. Fill the values at position A, B, C, D, E, F, G, and H.

Timing Signal	PC (in hex)	AR (in hex)	DR (in hex)	IR (in hex)
T0		A		
T1	B			C
T2		D		
T3		E		
T4			F	
T5			G	
T6	H			

(b) Let the address stored in the program counter be designated by the symbol X1. The (6) instruction stored at X1 has an address part(operand reference) X2. The operand needed to execute the instruction is stored in memory word with address X3. An index register contains the value X4. Determine the effective address for the following addressing modes: Indirect, PC relative, Direct, Indexed, Autodecrement, Autoincrement

Q5 (a) A four-way set associative cache memory can accommodate a total of 8192 words (2+1) from the main memory. The main memory size is 128 K $\times$ 32, how many bits are there in the tag, index field of the address format?What is the size of the cache memory?

(b) Given x=0101 and y=1010 (already in two's complement notation) compute the (7) product $p = x \times y$ using booth's algorithm by drawing flowchart also.

Q6 (a) A computer has a cache, main memory and a disk used for virtual memory. If a (6) reference word is in the cache, 20 ns are required to access it. If it is in main memory but not in the cache, 60 ns are needed to load it into the cache. If the word is not in main meory, 12 ms are required to fetch the word from the disk, followed by 60ns to copy it to the cache, and then reference is started again. The cache hit ratio is 0.9 and main memory hit ratio is 0.6. What is the average time in nanoseconds required to access a referenced word on this sytem?

(b) Differentiate between the following- (4)
(i) RISC vs CISC   (ii) Paging vs Segmentation

Q7 (a) Consider the following sequence of instructions being processed on the 5- (4+2) stage(Fetch, Decode, Execute, Memory access, Write back) RISC processor.-

```
LOAD   R4, #100(R2)
ADD    R5, R2, R3
SUB    R6, R4, R5
AND    R7, R2, R5
```

Assume that the pipeline does not use operand forwarding. Draw a space time diagram that represents instruction flow through the pipeline during each clock cycle. How long does it take for the instruction sequence to complete?

(b) Explain three input-output modes of data transfer with a suitable example. (4)