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MICROPROCESSORS

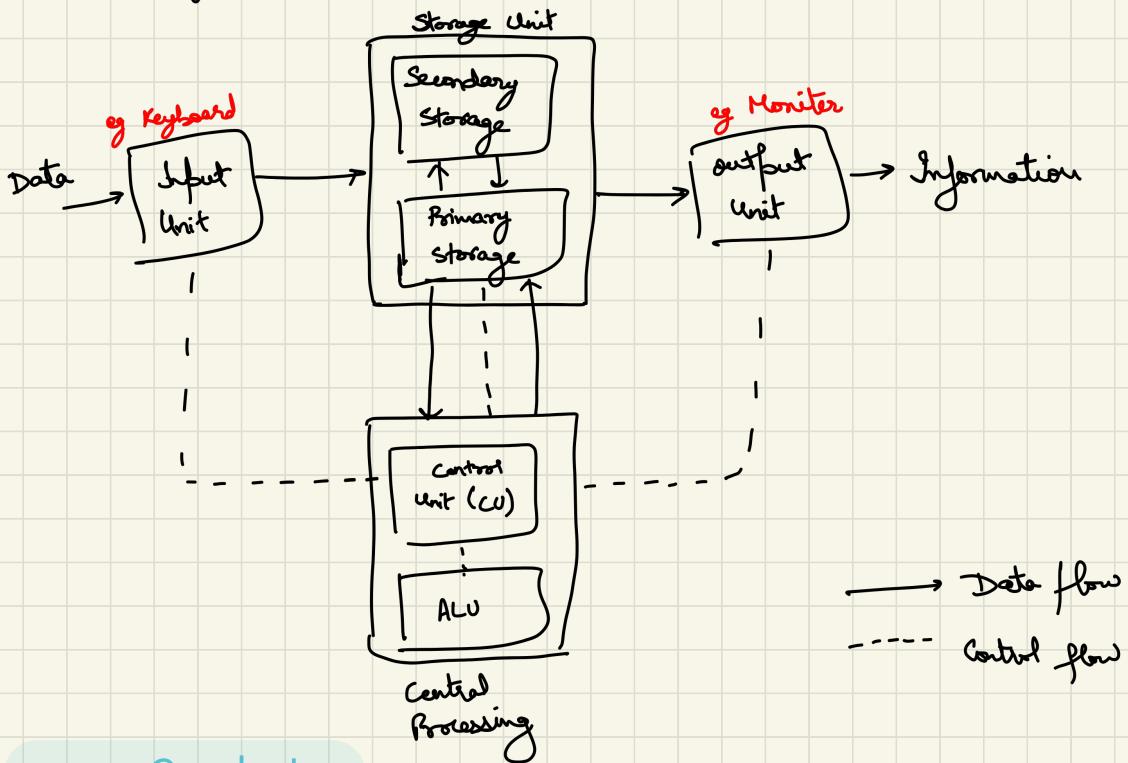
Microprocessors



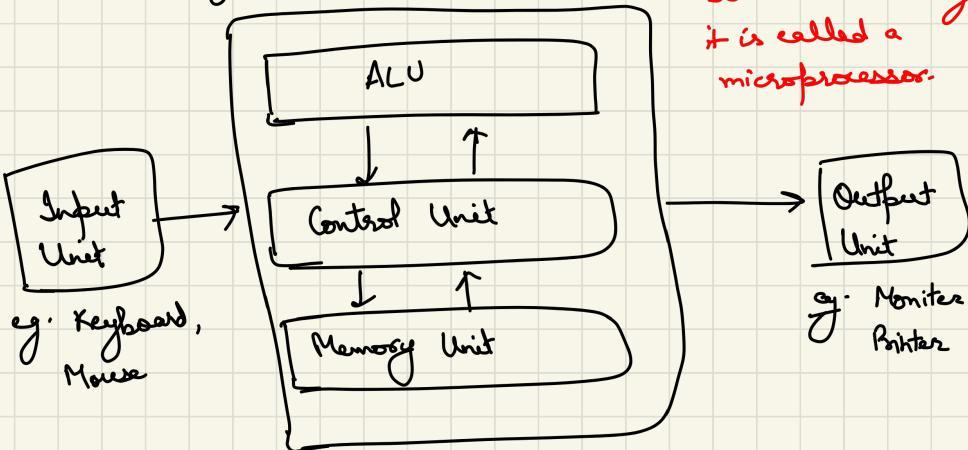
Lec-1 : Microprocessor :

- Microprocessor is a hardware component of computer and it works as brain of computer. It is a chip made of silicon and it has to be responsible to all fns of CPU.
- Microprocessor manages various ALU (Arithmetic Logic unit) operations such as add"/sub, internal processing, device terminal conn & I/O management.
- Block Diagram of digital computer:

① Block diagram of computer



② Central Processing Unit (CPU)

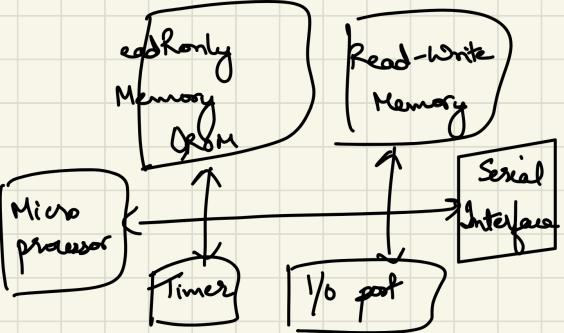


when this CPU is built on a single IC, it is called a microprocessor.

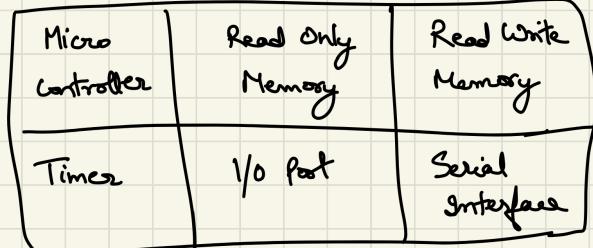
Take input from user using devices such as keyboard, mouse. This set of instruction is processed by CPU after getting the input and then computer produces the output. The computer can show the output to user using monitor, printer.

CPU is brain of computer. It is an electronic hardware device which can perform different types of operations such as arithmetic and logic operation.

Microprocessor



Microcontroller



Microprocessors

- ① Heart of computer system
- ② just a processor. Memory and I/O Components have to be connected externally
- ③ Since memory and I/O has to be connected externally, circuit becomes large.
- ④ Can't be used in compact system and hence inefficient
- ⑤ Cost ↑
- ⑥ Due to external components, the entire power consumption is high. Hence, not suitable to use with devices running on stored power like batteries.
- ⑦ Most of the microprocessors do not have power saving features.
- ⑧ Memory & I/O components are external, each instruction will need ext. operation hence it is relatively slower.

Microcontroller

- Heart of embedded system
- has internal processor along with internal memory and I/O components
- Since memory and I/O has to be connected internally, circuit is small.
- can be used in compact system & hence it is an efficient technique.
- Cost of entire system is low
- Since external components are low, total power consumption is less and can be used with devices running on stored power like batteries.
- Most of microcontrollers have power saving modes like idle mode and power saving mode. This helps to reduce power consumption even further.
- Since components are internal, most operations are internal, speed is fast.

Lee 2 : 8085 Block Diagram

- features of 8085 :

- ① developed by INTEL
- ② 8 bit microprocessor : can accept 8 bit data simultaneously
- ③ operates on single +5V DC supply
- ④ Designed using NMOS technology
- ⑤ 6200 transistors on a single chip
- ⑥ It provides on chip clock generator, hence it does not require external clock generator.
- ⑦ operates on 3MHz clock frequency.
- ⑧ 8 bit multiplexed address/ data bus, which reduce the no. of pins.
- ⑨ 16 address lines, hence it can address $2^{16} = 64\text{ K}$ bytes of memory.
- ⑩ It generates 8 bit I/O addresses, hence it can access $2^8 = 256$ I/O ports.
- ⑪ 5 hardware interrupts i.e. TRAP, RST 6.5, RST 5.5, RST 4.5 and INTR.
- ⑫ It provides DMA (direct memory access).
- ⑬ 40 pin IC package fabricated on a single LSI chip.
- ⑭ Clock cycle is 320 ns.
- ⑮ 80 basic instructions and 246 opcodes.
- ⑯ whenever we are performing any operation , say ADD B , then one value is stored in the accumulator register and other in any general purpose register . $A + B = A$

- INTEL 8085 Architecture :

- ① Register Array
- ② ALU & Logical group
- ③ Instruction decoder and machine cycle encoder, Timing and control circuitry
- ④ Interrupt control group
- ⑤ Serial I/O group

- Register Array : ①

a) General purpose register : (user accessible)

- B, C, D, E, H, L are 8 bit register (can be used singly)
- can also be used for 16 bit register pair - BC, DE & HL
- Used to store the intermediate data and result
- HL & L can be used as data pointer (holds memory address)

b) Special purpose register (A, Instruction Register and Flag)

(b.1) Accumulator (A) : (user accessible)

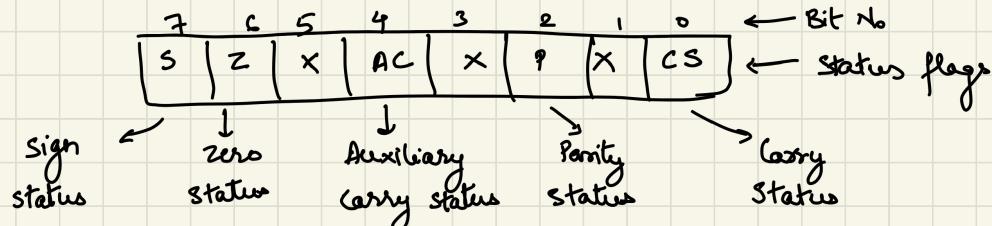
- 8 bit register
- All the ALU operations are performed with reference to contents of accumulator
- Result of an operation is stored in A
- Stores 8 bit data during I/O transfer

(b.2) Instruction Register : (user not accessible)

- When an instruction is fetched from memory, it is loaded in IR. Then transferred to decoder for decoding.
- It is not programmable and can not be accessed through any instruction.

(b.3) Flag Register (f) : (user accessible)

- 8 bit Register
- Indicates the status of ALU operation
- ALU indicates 5 flip flop which are set or reset after an operation according to data conditions of result in the accumulator.



\times = undefined status

Fkg	Significance
$C \text{ or } CY$ (Carry)	CY is set when an arithmetic operation generates a carry out, o/w it is 0 (zero) i.e. reset
P (Parity)	$P=1$, if result of an ALU operation has even number of 1's in A $P=0$, if number of 1 is odd
AC (Auxiliary carry)	Similar to CY $AC=1$, if there is carry from D_3 to D_4 bit $AC=0$, if there is no carry from D_3 to D_4 bit (not available for user)
Z (Zero)	$Z=1$, if result in A is 00F 0 ; otherwise

S (Sign)

| S=1 if D₇ bit of A is 1 (indicate the result is -ve)
| S=0 if D₇ bit of A is 0 (.. .. , +ve)

c) Temporary Register (W, Z, Temporary data register)

- Internally used by the MP (user not accessible)

(c.1) W and Z register :

- 8 bit capacity
- used to hold temporary addresses during execution of some instructions

(c.2) Temporary data register :

- 8 bit capacity
- used to hold temporary data during ALU operations

d) Pointer Register or Special purpose [SP, PC]

(d.1) Stack pointer (SP)

- 16 bit address which holds the address of data present at top of stack memory
- It is a reserved area of memory in RAM to store and retrieve the temporary info.
- Also holds content of PC when subroutines are used
- When there is a subroutine call or an interrupt i.e. pushing the return address on a jump and retrieving it after the operation is complete to come back to its original location.

(d.2) Program Counter (PC)

- 16 bit address used for execution of program
- contain the address of next instruction to be executed after fetching the instruction

- it is automatically incremented by 1
- Not much use in programming, but as an indicator to user only

In addition to register MP contains some latches and buffer

i) Increment and decrement address latch :

- 16 bit register
- used to increment or decrement content of PC and SP

ii) Address buffer :

- 8 bit unidirectional buffer
- used to drive high order address bus (A_8 to A_{15})
- When it is not used under such as reset, hold and halt etc this buffer is used tri-state high order address bus

iii) Data / Address Buffer :

- 8 bit directional buffer
- used to drive low order address (A_0 to A_7) and data (D_0 to D_7) bus
- under certain conditions such as reset, hold and halt etc this buffer is used tri-state low order address bus.

- ② ALU & Logical Group : it consists of ALU, Accumulator, Temp. register & Flag registers

a) ALU :

- performs arithmetic and logical operations
- stores result of arithmetic and logical operations in accumulator

b) Accumulator :

- general purpose register
- stores one of operand before any arithmetic and logical operations & result of operation is again stored back in accumulator
- stores 8 bit data during I/O transfer

c) Temporary Register :

- 8 bit register
- during arithmetic & logical operations , one operand is in A and other is transferred to temporary register

e.g. ADD B - content of B is transferred to Temp. register before actual add

d) Flag Register :

- 5 flags are connected to ALU
- After the ALU operation is performed the status of result will be stored in five flags

③ Instruction decoder and machine cycle encoder, Timing & control circuitry :

a) Instruction decoder and machine cycle encoder :

- decodes the opcode in IR and establishes the sequence of events to follow
- encodes it and transfer to the timing & control unit to perform the execution of instruction

b) Timing and control circuitry :

- works as brain of CPU
- for proper sequence and synchronisation of all operations of MP, this unit generates all the timing and control signals necessary for communication b/w microprocessor and peripherals

④ Interrupt Control Group :

Interrupt : occurrence of an external disturbance

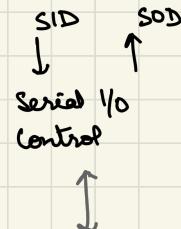
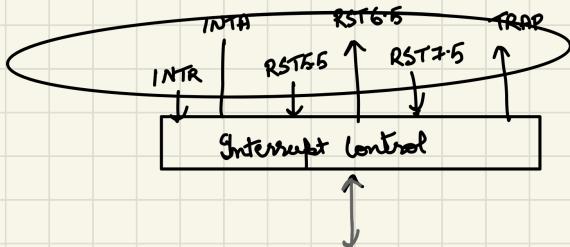
- After servicing interrupt, 8085 resumes its normal working
- Transfer of control to special routines
- Five interrupts - TRAP, RST 7.5, RST 6.5, RST 5.5, INTR

- In response to INTR, it generates INTA signal

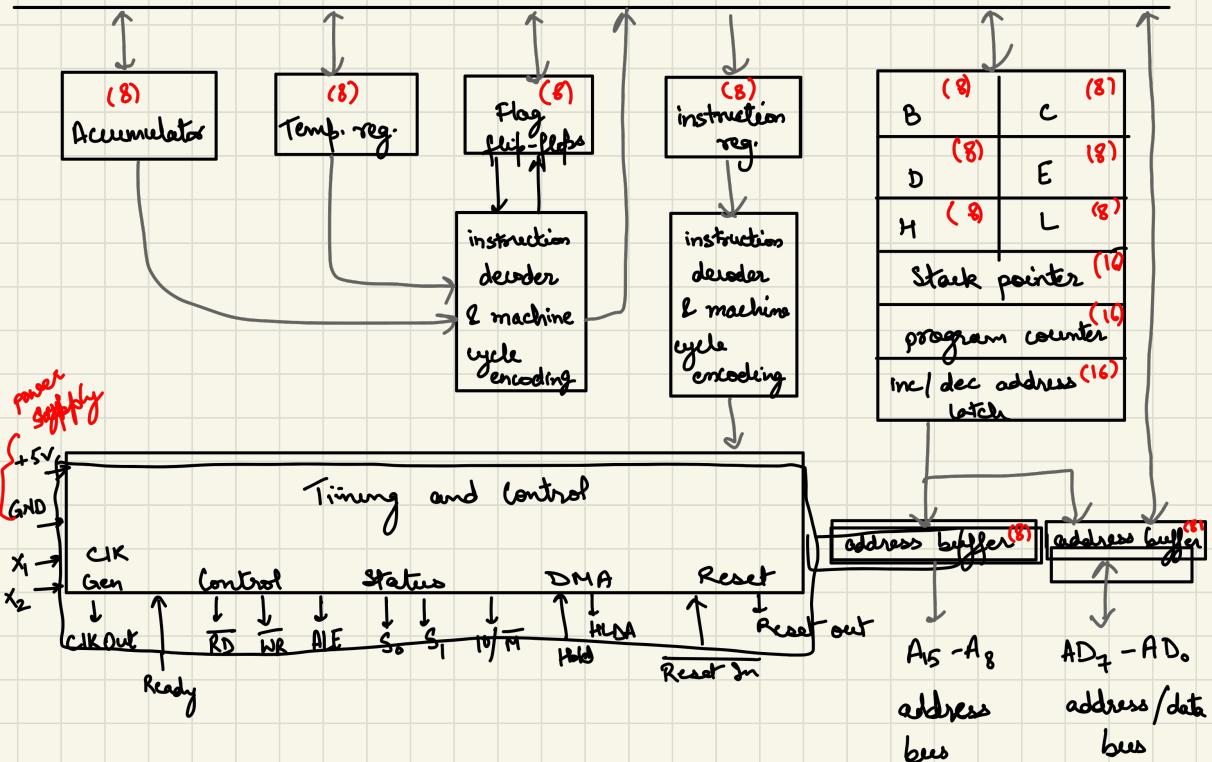
SID = serial input data
SOD = " output "

(b) Serial I/O control group:

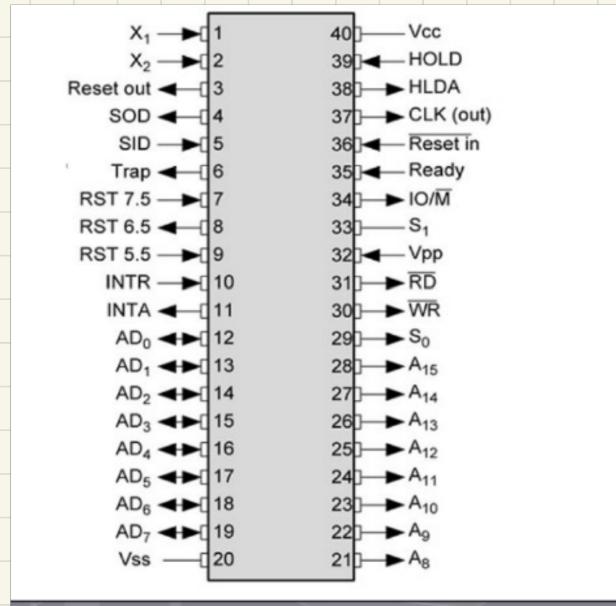
- Data transfer D0-D7 lines is parallel data
- But under some conditions it is used serial data transfer
- Serial data is entered through SID input (received)
- Serial " " output SOD input (send)



8-bit Internal data bus

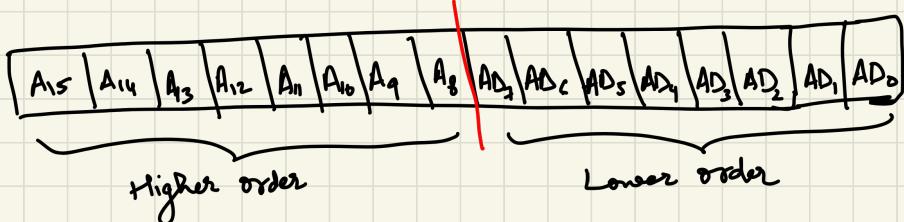


Lee 3 : Pin Diagram of 8085



- It has 40 pins and uses +5 for power. It can run at a max^m frequency of 3 MHz.
- pins on chip can be grouped in 9 groups :
 - i) Address Bus and data bus
 - ii) Status signals
 - iii) Control signals
 - iv) Interrupt Signal
 - v) Power supply and clock signal
 - vi) Reset Signal
 - vii) DMA Request Signal
 - viii) Serial I/O signal
 - ix) Externally initiated signals

- Address and data buses :



Address bus (Pin 21-28) :

- 16 bit address lines A₀ to A₁₅
- The address bus has 6 signal lines A₈-A₁₅ which are unidirectional
- The other 8 address lines A₀ to A₇ are multiplexed with 8 data bits

Data Bus (Pin 19-12) :

- To save the no. of pins lower order address pin are multiplexed with 8 bit data bus (bidirectional)
- Bits AD₀-AD₂ are bidirectional and serve as A₀-A₂ and D₀-D₂ at the same time
- During execution, the bits carry
address part during T₁ (early part)
of data bits during T₂ (later part)

Status Pins - ALE, S₁, S₀

① ALE (Address Latch Enable) : (Pin 30)

used to demultiplex the address and data bus

ALE = 1 → AD₀-AD₂ lines have address

Made with  " " data

This signal can be used to enable a latch to save the address bits from

AD lines

② S₀ and S₁ (Status Signal) : (Pin 33 and 29)

- Status signal to specify the kind of operation being performed

S ₁	S ₀	operation
0	0	HALT
0	1	WRITE
1	0	READ
1	1	Fetch

- Control Signals :

Control Pins - RD, WR, IO/M (active low)

1. RD: Read (Active low) (Pin 32)

- Read Memory or I/O device
- Indicated that data is to be read either from memory or I/P device and data bus is ready for accepting data from the memory or I/O device.

2. WR: Write (Active low) (Pin 31)

- Write Memory or I/O device
- Indicated that data on the data bus are to be written into selected memory or I/P device.

3. IO/M: (Input Output/Memory-Active low) (Pin 34)

- Signal specifies that the read/write operation relates to whether memory or I/O device.
- When (IO/M=1) the address on the address bus is for I/O device
- When (IO/M=0) the address on the address bus is for memory

IO/M(active low)	RD	WR	Control Signal	Operation
0	0	1	MEMR	M/M Read
0	1	0	MEMW	M/M write
1	0	1	IOR	I/O Read
1	1	0	IOW	I/O Write

Control and status Signals

- When S_0, S_1 is combined with IO/M (active low), we get status of machine cycle

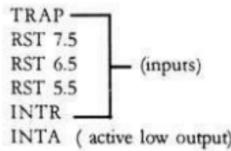
IO/M	S_1	S_0	OPERATION	Control Signal
o	1	1	Opcode fetch	$\overline{RD} = o$
o	1	0	Memory read	$\overline{RD} = o$
o	0	1	Memory write	$\overline{WR} = o$
1	1	0	I/O read	$\overline{RD} = o$
1	0	1	I/O write	$\overline{WR} = o$
1	1	0	Interrupt Acknowledge	$\overline{INTA} = o$
Z	o	o	Halt	
Z	x	x	Hold	$\overline{RD}, \overline{WR} = Z$
Z	x	x	Reset	and $\overline{INTA} = 1$

Z= Tristate, X = don't care condition

7

Interrupts

- They are the signals initiated by an external device to request the microprocessor to do a particular task or work.
- There are five hardware interrupts called, **(Pin 6-11)**
- On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.



Power supply and Clock Signal

- Vcc (Pin 40) : single +5 volt power supply
- Vss (Pin 20) : Ground
- ✓ X₀ and X₁ : (Pin 1-2)
 - Crystal or R/C network or LC network connections to set the frequency of internal clock generator.
 - The frequency is internally divided by two.
 - Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected to the X₀ and X₁ pins.
- ✓ CLK (output) : (Pin 37)
 - Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Reset Signals

- ✓ Reset In (input, active low) (Pin 36)
 - This signal is used to reset the microprocessor.
 - The program counter inside the microprocessor is set to zero (0000H)
 - The buses are tri-stated.
- ✓ Reset Out (Output, Active High) (Pin 3)
 - It indicates microprocessor is being reset.
 - Used to reset all the connected devices when the microprocessor is reset.

DMA Request Signals

- **DMA:**
 - When 2 or more devices are connected to a common bus, to prevent the devices from interfering with each other, the tristate gates are used to disconnect all devices except the one that is communicating at a given instant .
 - The CPU controls the data transfer operation between memory and I/O device.
 - DMA operation is used for large volume data transfer between memory and an I/O device directly.
 - The CPU is disabled by tri-stating its buses and the transfer is effected directly by external control circuits.
- **HOLD (Pin 38)**
 - This signal indicates that another device is requesting the use of address and data bus.
 - So it relinquish the use of buses as soon as the current machine cycle is completed.
 - Microprocessor regains the bus after the removal of a HOLD signal
- **HLDA (Pin 39)**
 - On receipt of HOLD signal, the MP acknowledges the request by sending out HLDA signal and leaves out the control of the buses.
 - After the receipt of HOLD signal the DMA controller starts the direct transfer of data.
 - After the removal of HOLD request HLDA goes low.

Serial I/O Signals

These pins are used for serial data communication

✓ SID (input) Serial input data (Pin 4)

- It is a data line for serial input
- Used to accept serial data bit by bit from external device
- The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

✓ SOD (output) Serial output data (Pin 5)

- It is a data line for serial output
- Used to transmit serial data bit by bit to the external device
- The 7th bit of the accumulator is outputted on SOD line when SIM instruction is executed.

Externally Initiated signal

✓ Ready (input) (Pin 35)

- Memory and I/O devices will have slower response compared to microprocessors.
- Before completing the present job such a slow peripheral may not be able to handle further data or control signals from CPU.
- The processor sets the READY signal after completing the present job to access the data.
- It synchronize slower peripheral to the processor.
- The microprocessor enters into WAIT state while the READY pin is disabled.

Lecture - 4 .

Instruction Formats

Each instruction has two parts:

Opcode (operation code)- The first part is the task or operation to be performed.

Operand - The second part is the data to be operated on.

Data can be given in various forms.

- It can specify in various ways: may include 8 bit/16 bit data, an internal register, memory location or 8 bit /16 bit address

✓ One-byte or one word Instructions: opcode and operand in 8 bits only i.e. one byte. Operand(s) are internal register and are coded into the instruction.

e.g. MOV, ADD, ANA, SUB, ORA etc

✓ Two-byte instructions: first byte is opcode in 8 bits and second byte is operand
either 8 bit data or 8 bit address.

✓ Three-byte instructions: first byte is opcode in 8 bits and second and third byte are
operand either 16 bit data or 16 bit address.
Operand 1 = lower 8 bit data/address
Operand 2 = Higher 8 bit data/address
opcode + data byte + data byte

Types of Addressing Modes

Intel 8085 uses the following addressing modes:

1. Direct Addressing Mode
 2. Register Addressing Mode
 3. Register Indirect Addressing Mode
-

Direct Addressing Mode

In this mode, the address of the operand is given in the instruction itself.

LDA is the operation.

2500 H is the address of source.

Accumulator is the destination

Register Addressing Mode

In this mode, the operand is in one of the general purpose register or accumulator.

MOV is the operation.

B is the source of data.

A is the destination

Register Indirect Addressing Mode

In this mode, the address of operand is specified by a register pair.

MOV is the operation.

M is the memory location specified by H-L register pair.

A is the destination

Immediate Addressing Mode

In this mode, the operand is specified within the instruction itself.

MVI is the operation.

05 H is the immediate data (source).

A is the destination

Implicit Addressing Mode

● If address of source of data as well as address of destination of result is fixed,

then there is no need to give any operand along with the instruction. It means

there are certain instructions which operate on the content of the

accumulator. Such instructions do not require the address of the operand.

● CMA is the operation. A is both source and destination.

With Complements

lecture 5:

- Instruction : command to perform operation on given data

Instruction cycle : steps to fetch an instruction & data from memory & execute it

Instruction cycle = fetch cycle + execute cycle

↓ ↓
fetching time execution time is variable
is constant (depends on type of instruction)

- Fetch : In the beginning of fetch cycle the content of PC is sent to memory.

Memory places opcode on data bus so as to transfer it to the microprocessor.

The entire operation of fetching an opcode takes 3 clock cycles.

The clock cycle for which CPU has to wait (in case of slow memory) is called wait cycle.

- Execute :

opcode fetched from memory goes to the data register then to IR (instruction register)

from the instruction register it goes to the decoder circuitry (which is within the microprocessor)

After instruction is decoded, execution begins.

Made with Goodnotes
If operand is in general purpose registers, execution begins immediately.

Time taken in decoding and execution is one clock cycle.

If an instruction contains data or operand address which are still in the memory, the CPU has to perform some read operations to get the desired data.

After receiving the data it performs execute operation.
A read cycle is similar to a fetch cycle.

- Machine cycle and State :

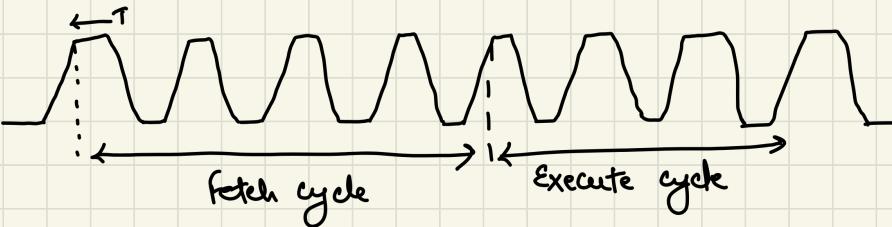
Machine cycle is time for completing the operation of accessing either memory or I/O device. In 8085, the machine cycle may consist of 3 to 6 T states.

The T state is defined as one sub-division of the operation performed in one clock period.

These sub-divisions are internal states synchronised with system clock.

In every machine cycle the first operation is op-code fetch.

So, one clock cycle of the system is referred to as a state.



- Op-code fetch machine cycle :

involves fetching op-code of instruction to be executed and decoding process of that op-code. Usually, it consists of 4 T states

Step 1 → addr placed on addr bus

when $\overline{RD} = 0$, read is done

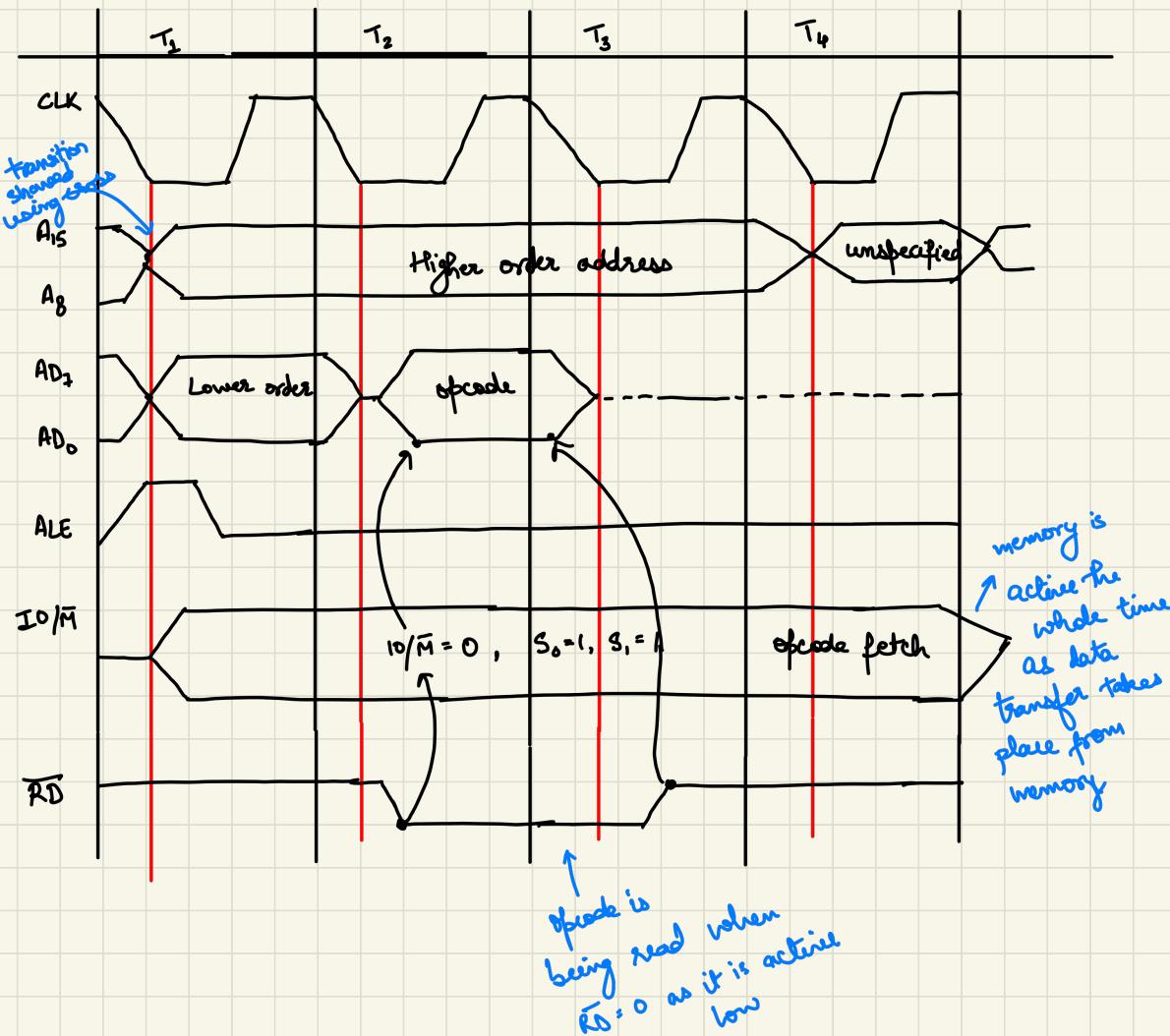
$A_{15} - A_8 \rightarrow$ addr lines (H_0)

$AD_7 - AD_0 \rightarrow$ LO addr lines

ALE → addr latch enable

$= 1 \quad A_7 \text{ to } A_0 \quad (LO)$

$= 0 \quad D_7 \text{ to } D_0$



4th T state:

- fetched opcode is decoded
- 1-byte instructions with STC (set carry flag) are executed.
eg. MOV A,D

5th or 6th T state:

- Some instructions take 5 or 6 states, e.g. DCX, INX, PCHL, SPHL, CALL, RSTN, conditional RET
- Memory Read Machine Cycle: (three T states)

first three states of memory read machine cycle are similar to opcode fetch machine cycle, just one change that values of $S_1 = 1$ & $S_0 = 0$, in first T state.

Memory Write machine cycle: (three T states)

similar to memory read machine cycle, just the values of S_0 and S_1 become $S_1 = 0$ and $S_0 = 1$.

& instead of RD comes WR.

I/O read machine cycle: (three T states)

10/M goes high instead of going low, indicating microprocessor is talking to an I/O device.

$$S_1 = 1, S_0 = 0$$

I/O write machine cycle:

10/M = high, $S_1 = 0, S_0 = 1$, In 3rd T state, WR goes high

Lee 6 : Data Transfer Group :

- Instruction = opcode + operand

Notation	Meaning
M	memory location pointed by HL-register pair
r	8-bit register
SP	16-bit register
rs	source register
rd	destination register
addr	16 bit address

- Data Transfer Instructions : copy data from source to destination while copying, contents of source are not modified.

① MOV r₁, r₂ : move content of 1 register to another

$$[r_1] \leftarrow [r_2]$$

State = 4 → as only fetch is there

Flag = None

Addr = Register

Machine cycle = 1

$$S_1, S_0 = 1$$

RD

LEC 12 : INTERRUPTS

Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. Generally, a particular task is assigned to that interrupt signal. In the microprocessor based system the interrupts are used for data transfer between the peripheral devices and the microprocessor.

After receiving an interrupt signal from the peripheral, the microprocessor executes current instruction completely.

Store the contents of program counter i.e. return address on the stack and then executes interrupt service (ISR) to provide service to the interrupting device.

After servicing the device, the microprocessor transfers program control back to the program where interrupt occurs by reloading the content of program counter which has been stored on the stack when an interrupt occurs.

RIM (Read Interrupt Mask) Instruction

The Read Interrupt Mask, RIM, instruction loads the status of the interrupt mask, the pending interrupts and the contents of the serial input data line, SID, into the accumulator. Thus, it is possible to monitor status of interrupt mask, pending interrupts and serial input. There are number of types of interrupts in 8085. When one interrupt is being serviced, other interrupt requests may occur. If the interrupt requests are of higher priority, 8085 branches program control to the requested interrupt service routines. But when the interrupt requests are of lower priority, 8085 stores the information about these interrupt requests. Such interrupts are called pending interrupts. The status of pending interrupts can be monitored using RIM instruction.

Lec 6-13 are in handwritten notes properly. (pg 1-10)

8086 : Lee 1, Pin diagram :

- features of 8086 :

- ① 16 bit , N-channel , HMOS
- ② CMOS version
- ③ Consumes less power

It is a 16-bit, N-channel, HMOS (High speed metal oxide semiconductor) microprocessor.

- Its CMOS (Complementary MOS) version, 80C86 is also available.
- It consumes less power.
- The 8086 draws 360 mA on 5V whereas the 80C86 draws only 10 mA.
- 8086 is manufactured for standard temperature range 32 F to 180 F as well as extended temperature range (40 F to +225 F).
- Its clock frequencies for its different versions are: 5, 8 and 10 MHz.
- It was introduced in 1978.

- It contains an electronic circuitry of 29000 transistors.
- It is built on a single semiconductor chip and packaged on a 40-Pin IC package.
- The type of package is DIP (Dual In-Line Package).
- 8086 uses 20 address lines and 16 data lines.
- It can directly address up to $2^{20} = 1$ Mbytes of memory.
- The 16-bit data word is divided into a low-order byte and a high order byte.
- The 16 low order address lines are time multiplexed with data, and the 4 high order address lines are time multiplexed with status signals.

AD0-AD15 (Bidirectional) Address/Data bus :

Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A0-A15.

When data are transmitted over AD lines the symbol D is used in place of AD, for example D0-D7, D8-D15 or D0-D15.

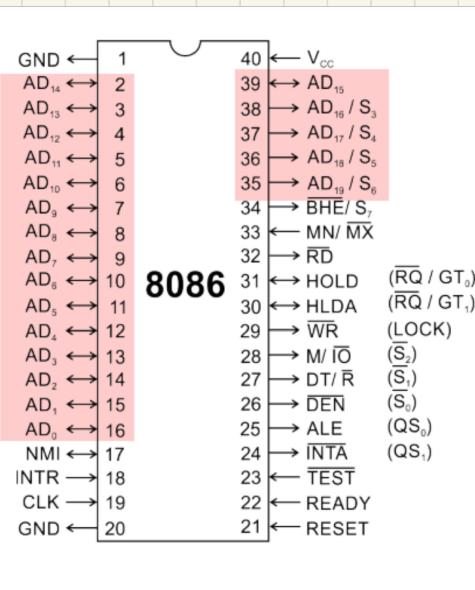
A16/S3, A17/S4, A18/S5, A19/S6

High order address bus. These are multiplexed with status signals.

A16 and A17 are multiplexed with segment identifier signals S3 and S4.

A18 multiplexed with interrupt status S5.

A19 with status signal S6



BHE (Active Low)/S7 (Output)

(T1 is low)It is used to enable data onto the most significant half of data bus, D8-D15. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S7.(S7 available during T3 and T4.)

MN/ MX MINIMUM / MAXIMUM

S3, S4, S5

BHE(low)	A0	
0	0	Whole word is transferred
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

S3	S4	
0	0	ES
0	1	SS
1	0	CS
1	1	DS

TEST

TEST: input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. used to synchronize an external activity to the processor internal operation.

READY

This is the acknowledgement from the slow device(addressed I/O) or memory indicates that peripheral is ready to transfer data. The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086. The signal is active high.

RD (Read) (Active Low)

The signal is used for read operation. It is an output signal. It is active when low.

Min/ Max Pins

In the minimum mode of operation the microprocessor do not associate with any co-processors and can not be used for multiprocessor systems. In the maximum mode the 8086 can work in multi-processor or coprocessor configuration. Minimum or maximum mode operations are decided by the pin MN/ MX(Active low). When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.

RESET (Input)

Causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles.

CLK

The clock input provides the basic timing for processor operation and bus control activity. 5.8 or 10 MHz.

[go to page 11 of handwritten notes](#)

INTR Interrupt Request

This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.

This signal is active high and internally synchronized.

