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Thapar Institute of Engineering & Technology, Patiala

Department of Computer Science and Engineering

MID SEMESTER EXAMINATION

B. E. (Third Year): Semester-VI (2018/19) (COE)

Course Code: UCS617

Course Name: Microprocessor Based Systems Design

March 16, 2019

Saturday 8:00 – 10:00 AM

Time: 2 Hours, M. Marks: 25

Name of Faculty: ANJ, MJU, ANA, HRS, RAH, MKA, RAC, SVS

Note: Attempt all questions in sequence with proper justification. Assume missing data, if any, suitably.

Q1(a) Write an assembly language program to convert a BCD number into its equivalent binary in 8085. (4)

Q1(b) The following program is run on 8085 microprocessor: (2)

Memory address in hex	Instruction
2000	LXI SP, 1000H
2003	PUSH H
2004	PUSH D
2005	CALL 2050H
2008	POP H
2009	HLT

At the completion of the execution of the program, what are the contents of program counter and stack pointer?

Q2(a) Draw and explain the timing diagram for the instruction SHLD 2550H and indicate Total number of T-states and Machine cycles required to execute the instruction. (3+1)

Q2(b) Write a program and show the contents of accumulator for SIM instruction that will mask RST 7.5, 5.5 and unmask RST 6.5. (2)

Q3(a) Determine the maximum time delay that can be generated using 16-bit counters when operating frequency is 2 MHz. (2)

Q3(b) Write the Program Status Word (PSW) for ADD B in 8085 microprocessor when the contents of Accumulator (A) is 9FH and B register is E5H. (2)

Q3(c) Discuss the following 8086 instructions with suitable example: (3)

a) AAD b) DAA c) AAS

Q4(a) Discuss the following pins for 8086 microprocessor: (2+2)

i. $MN/\overline{MX}$ ii. $\overline{TEST}$ iii. $\overline{BHE}$ iv. NMI

How the physical address can be generated in 8086 using segment registers?

Q4(b) Differentiate between Immediate addressing and Based Indexed Addressing mode in 8086 along with example. (2)