Roll Number:_____

Thapar Institute of Engineering & Technology, Patiala

Department of Computer Science and Engineering

AUXILIARY EXAMINATION

B. E. (Third Year)	Course Code: UCS617 Course Name: Microprocessor Based Systems Design
Aug 10, 2019—1715 hrs	
Time: 3 Hours, M. Marks: 100	Name of Faculty: Harpreet

Note: Attempt all questions with proper justification.
Assume missing data, if any, suitably.

Q1(a) Differentiate between the following terms with example:- (4*3)

i. CALL and JUMP Instruction.

ii. Vectored and Non-Vectored Interrupts.

iii. Machine Cycle and Instruction Cycle.

Q1(b) What is the difference between LDA and STA instruction? Illustrate with the help of timing diagrams. (2+8)

Q1(c) Write the contents of accumulator through program for SIM Instruction that will mask RST 7.5, 6.5 and unmask 5.5. (5)

Q2(a) Explain the minimum and maximum mode of 8086 with the help of pin diagram. (4+4)

Q2(b) Write a program in any 8085/8086/ARM assembly language to : (5+5)

i. Subtract two 16-bit numbers using indirect addressing mode.
ii. Perform the division 15/6 using the ASCII codes. Store the ASCII codes of the result in register DX.

Q2(c) Explain different types of Assembler Directives with the help of example. (6)

Q3(a) WAP to Generate a delay of 0.4 sec if the crystal freq is 5 MHz in 8085. (3)

Q3(b) Elaborate the architecture of USART in detail. Why Transmitter and Receiver section called as double buffered system? (10)

Q3(c) How CPSR is different from SPSR in ARM processor? (3)

Q3(d) Write an initialization sequence to define Port A in mode 2, Port B as output in mode 1. The 16 bit address of CWR is 2006h in PPI. (3)

Q4(a) Differentiate between RIM and SIM instruction? (2+2)

Q4(b) Translate the given C code in to ARM programming :- (4)

```
int x,y;
...
if(x >0) {
y=1;
} else
{
y=2;
}
return y;
```

Q4(c) Explain the various addressing modes of 8086 microprocessor? (8)

Q5(a) Differentiate between the following: (3*3)

i. FIQ and IRQ in ARM

ii. Pre-Index and Post-Index Addressing

iii. Thumb and ARM Instructions

Q5(b) How many numbers of registers are present in ARM processor/architecture? Discuss the Register Organization under the ARM's architecture. (1+4)