Cong (Callie) Hao

Postdoctoral Researcher
University of Illinois at Urbana-Champaign, USA
E-mail: congh@illinois.edu

EDUCATION

Postdoc	Electrical & Computer Engineering	University of Illinois at Urbana-Champaign, USA	2017 - present
Ph.D.	Electrical Engineering	Waseda University, Japan	2014 - 2017
M.S.	Electrical Engineering	Waseda University, Japan	2010 - 2012
M.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2011 - 2014
B.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2007 - 2011

RESEARCH AREA

- High-performance reconfigurable computing: FPGA, embedded system, IoT and edge computing
- Machine learning: hardware acceleration, software/hardware co-design, ML algorithms in autonomous driving
- Electronic design automation (EDA): high-level synthesis (HLS), physical synthesis, network-on-chip

HONORS

2019	First place winner (FPGA track, 1/58), IEEE Design Automation Conference (DAC) System Design Contest
	First place winner (GPU track, 1/52), IEEE Design Automation Conference (DAC) System Design Contest
2019	Best Poster Award, ICML Workshop
2018	Student Innovation Award, IEEE HPEC Graph Challenge
2018	Third place winner (FPGA track, 3/62), IEEE Design Automation Conference (DAC) System Design Contest
2018	Distinguished Project Award, Boeing Global Technology
2016	Best Student Paper, IEEE International New Circuits and Systems Conference
2015	Best Student Paper, IEEE International Conference on ASIC
2015	Student travel grant (250 US$), International Workshop on Logic and Synthesis
2015	Young Student Fellow Award, IEEE Design Automation Conference (1K US$ grant)
2015	Excellent Paper Award, ISIPS, Graduate School of IPS, Japan
2013	Best Student Paper, IEEE International Conference on ASIC
2013	Google Anita Borg Memorial Scholarship (1.5K US$)
2013	IEICE VLD Excellent Student Award, Asia and South Pacific Design Automation Conference
2012	Best Paper Nomination, International Symposium on VLSI Design, Automation and Test

PROJECTS

- **NAIS: Neural Architecture and Implementation Search (2018 – present)**
  - **Methodology**: beyond NAS (neural architecture search) – incorporates hardware implementation search into NAS to produce hardware-efficient AI algorithms as well as optimized hardware implementations, within limited hardware resource and performance constraints.
  - **Framework**: an automatic DNN/implementation co-design tool – simultaneously searches for hardware-oriented DNN models and generates optimized hardware implementations.
  - Related Publications: [11] [12] [17] [18] [16]
- **Machine Learning Algorithm Development and Acceleration on FPGA (2018 – present)**
  - DNN algorithm development for object detection; DNN deployment on resource-limited FPGAs targeting real-time frames per second; DNN model acceleration on FPGA.
  - Related Publications: [1] [12] [14] [15]
  - First place winner in both GPU and FPGA track at Design Automation Conference System Design Contest, 2019.
  - Third place winner in FPGA track at Design Automation Conference System Design Contest, 2018.
- **Machine Learning in Autonomous Driving (2019 – present)**
  - Develop a hybrid powerful computing platform for autonomous driving cars, including a GPU-based primary system and an FPGA-based secondary system to improve the platform robustness.
  - 2D object detection in bad condition images such as rainy, foggy or snowy.
  - 3D object detection using monocular/stereo cameras with Lidar/Radar point cloud.
  - Related Publications: [13]

- **Smart Home Scheduling (2016)**
  - Explore low monetary cost scheduling plans for smart home appliances.
  - Related Publications: [22] [26]
- **High Level Synthesis for Approximate Computing using Machine Learning (2016 – 2017)**
  - Explore ASIC/FPGA design solutions for approximate computing applications during High-Level Synthesis; use machine learning algorithms for solution quality control.
  - Related Publications: [21] [28]
- **Low-Power High-Level Synthesis for ASIC (2010 – 2017)**
  - Explore low-power ASIC design solutions during High-Level Synthesis, such as: reducing on-chip interconnection complexity, utilizing multiple supply/threshold voltages to reduce dynamic/leakage power, etc.
  - Related Publications: [5] [6] [7] [8] [31] [29] [30] [32] [33] [34] [36] [35] [37]
- **Topology and Physical Synthesis for 3D Network-on-Chip (2014 – 2017)**
  - Explore 3D Network-on-Chip topology, node clustering and through-silicon via insertion solutions for low power, low routing complexity and low communication latency.
  - Related Publications: [2] [4] [3] [20] [23] [24] [25] [27]

PUBLICATIONS

- **Journals**

[1] Cheng Gong, Ye Lu, Tao Li, **Cong Hao**, Deming Chen, Yao Chen, "VecQ: High Accuracy DNN Model Compression with Vectorized Weight Quantization", *IEEE Transactions of Computers*, 2019, under review

[2] Zhao Yi, **Cong Hao**, and Takeshi Yoshimura. "Thermal and Wirelength Optimization With TSV Assignment for 3D-IC", *IEEE Transactions on Electron Devices*, 2019

[3] Ma Jiayi, **Cong Hao**, and Kundong Wang. "Decomposing and Cluster Refinement Design Method for Application-Specific Network-on-Chips.", *Journal of Shanghai Jiao Tong University (Science)*, 2018

[4] **Cong Hao**, Takeshi Yoshimura. "An Efficient Multi-Level Algorithm for 3D-IC TSV Assignment", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, March 2017

[5] **Cong Hao**, Nan Wang, and Takeshi Yoshimura. "A Unified Scheduling Approach for Power and Resource Optimization with Multiple V-dd or/and V-th in High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2017.

[6] **Cong Hao**, Jianmo Ni, Nan Wang, and Takeshi Yoshimura. "Interconnection Allocation between Functional Units and Registers in High-Level Synthesis", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[7] Wang Nan, Wei Zhong, **Cong Hao**, Song Chen, Takeshi Yoshimura, and Yu Zhu. "Leakage-power-aware scheduling with dual-threshold voltage design.", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[8] Nan Wang, Song Chen, **Cong Hao**, Haoran Zhang, and Takeshi Yoshimura. "Leakage Power Aware Scheduling in High-Level Synthesis.", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, 2014

- **Conferences (peer review)**

[9] Xiaofan Zhang, Haoming Lu, **Cong Hao**, Jiachen Li, Bowen Cheng, Yuhong Li, Kyle Rupnow, Jinjun Xiong, Thomas Huang, Honghui Shi, Wen-mei Hwu, Deming Chen, "SkyNet: a Hardware-Efficient Method for Object Detection and Tracking on Embedded Systems", The Conference on Machine Learning and Systems (SysML), 2020 (to appear).

[10] Pengfei Xu, Xiaofan Zhang, **Cong Hao**, Yang Zhao, Zetong Guan, Yongan Zhang, Yue Wang, Deming Chen and Yingyan Lin, "AutoDNNchip: An Automated DNN Chip Generator through Compilation, Optimization, and Exploration", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2020 (to appear).

[11] **Cong Hao**, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, Junli Gu and Deming Chen, "NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019.

[12] **Cong Hao**, Xiaofan Zhang, Yuhong Li, Sitao Huang, Jinjun Xiong, Kyle Rupnow, Wen-Mei Hwu, and Deming Chen, "FPGA/DNN Co-Design: An Efficient Design Methodology for IoT Intelligence on the Edge", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2019.

[13] **Cong Hao**, Atif Sarwari, Bryan Wu, Zhijie Jin, Junli Gu, and Deming Chen, "FPGA-based Secondary System for Autonomous Driving Cars", Proceedings of IEEE International Workshop on Signal Processing Systems, 2019.

[14] Yao Chen, Kai Zhang, Cheng Gong, **Cong Hao**, Xiaofan Zhang, Tao Li, and Deming Chen, "TDLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA," Proceedings of IEEE Computer Society Annual Symposium on VLSI, 2019.

[15] Cheng Gong, Ye Lu, **Cong Hao**, Xiaofan Zhang, Tao Li, Deming Chen, and Yao Chen, "μL2Q: An Ultra-Low Loss Quantization Method for DNN Compression," Proceedings of International Joint Conference on Neural Networks (IJCNN), 2019.

[16] Xiaofan Zhang, **Cong Hao**, Yuhong Li, Yao Chen, Jinjun Xiong, Wen-Mei Hwu and Deming Chen, "A Bi-Directional Co-Design Approach to Enable Deep Learning on IoT Devices," Joint Workshop on On-Device Machine Learning Compact Deep Neural Network Representations, ICML Workshop, 2019. (Best Poster Award)

[17] Yao Chen, Jiong He, Xiaofan Zhang, **Cong Hao**, and Deming Chen, "Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2019.

[18] **Cong Hao**, Deming Chen, "Deep Neural Network Model and FPGA Accelerator Co-design: Opportunities and Challenges", Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018.

[19] Sitao Huang, Mohamed El-Hadedy, **Cong Hao**, Qin Li, Vikram S Mailthody, Ketan Date, Jinjun Xiong, Deming Chen, Rakesh Nagi, Wen-mei Hwu, "Triangle Counting and Truss Decomposition using FPGA", IEEE High Performance extreme Computing Conference (HPEC), 2018

[20] Yi Zhao, **Cong Hao**, Takeshi Yoshimura, "TSV Assignment of Thermal and Wirelength Optimization for 3D-IC Routing", In 28th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2018

[21] **Cong Hao**, and Takeshi Yoshimura. "Application of on-line machine learning in optimization algorithms: A case study for local search." Computer Science and Electronic Engineering (CEEC), IEEE, 2017

[22] Yangyizhou Wang, **Cong Hao**, and Takeshi Yoshimura. "A Particle Swarm Optimization and Branch and Bound Based Algorithm for Economical Smart Home Scheduling" In 20th IEEE MWSCAS, 2017

[23] Yuxin Qian, **Cong Hao**, and Takeshi Yoshimura. "3D-IC signal TSV assignment for thermal and wirelength optimization" In 27th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2017

[24] Jiayi Ma, **Cong Hao**, Takeshi Yoshimura. "Power-efficient Partitioning and Cluster Generation Design for Application-Specific Network-on-Chip" In 13th IEEE ISOCC, 2016

[25] Hui Zhu, **Cong Hao**, Takeshi Yoshimura. "Thermal-Aware Floorplanning for NoC-Sprinting" In 59th IEEE MWSCAS, 2016

[26] **Cong Hao**, Takeshi Yoshimura. "Economical Smart Home Scheduling for Single and Multiple Users" In 59th IEEE MWSCAS, 2016

[27] **Cong Hao**, Nan Ding, Takeshi Yoshimura. "An Efficient Algorithm for 3D-IC TSV Assignment". In 14th IEEE NEWCAS, 2016 **(Best Student Paper)**

[28] **Cong Hao**, Takeshi Yoshimura. "EACH: An Energy-Efficient High-Level Synthesis Framework for Approximate Computing" In 2nd IEEE WAPCO, 2016

[29] Jian-Mo Ni, Qian Ai, **Cong Hao**, Takeshi Yoshimura, Nan Wang. "Primal-Dual Method based Simultaneous Functional Unit and Register Binding." In 10th ASICON, 2015

[30] **Cong Hao**, Nan Wang, Jian-Mo Ni, Takeshi Yoshimura. "An Efficient Tabu Search Methodology for Port Assignment Problem in High-Level Synthesis." In 24th IWLS, 2015

[31] **Cong Hao**, Jian-Mo Ni, Hui-Tong Wang, Takeshi Yoshimura. "Simultaneous Scheduling and Binding For Resource Usage and Interconnect Complexity Reduction in High-Level Synthesis." In 11th IEEE ASICON, 2015 **(Best Student Paper)**

[32] **Cong Hao**, Song Chen, Takeshi Yoshimura. "Network simplex method based Multiple Voltage Scheduling in Power-efficient High-level synthesis." In 18th IEEE ASP-DAC, 2013 **(IEICE VLD Excellent Student Award)**

[33] **Cong Hao**, Nan Wang, Song Chen, Takeshi Yoshimura, Min-You Wu. "Interconnection allocation between functional units and registers in High-Level Synthesis." In 10th IEEE ASICON, 2013 **(Best Student Paper)**

[34] Wang Nan, **Cong Hao**, Nan Liu, Haoran Zhang, Takeshi Yoshimura. "Timing and resource constrained leakage power aware scheduling in high-level synthesis." In 10th IEEE ASICON, 2013,

[35] **Cong Hao**, Haoran Zhang, Song Chen, Takeshi Yoshimura, Min-You Wu. "Port assignment for multiplexer and interconnection optimization." In 5th IEEE ASQED, 2013

[36] Haoran Zhang, **Cong Hao**, Nan Wang, Song Chen, Takeshi Yoshimura. "Power and resource aware scheduling with multiple voltages." In 10th IEEE ASICON, 2013 (Best Student Paper)

[37] **Cong Hao**, Song Chen, Takeshi Yoshimura. "Port assignment for interconnect reduction in high-level synthesis." In 19th IEEE VLSI-DAT, 2012 (Best Paper Nomination)

TEACHING EXPERIENCE

- **IoT and Cognitive Computing (ECE 498)**
  - *New course design*: revising course syllabus; preparing slides for several lectures; designing three laboratory topics; designing and grading for homework, midterm and final problems
  - Guest lecturer for IoT fundamental and DNN compression
- **System-on-Chip Design (ECE 527)**
  - Guest lecturer for machine learning fundamental

PROFESSIONAL SERVICES

Conference Review:	FCCM, ICCAD, DAC, ASP-DAC, FPGA
Journal Review:	Microelectronics Journal
	IEEE Journal on Selected Areas in Communications
	Engineering Optimization
	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
	IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
	IEEE Design & Test (D&T)
	Multidimensional Systems & Signal Process (MULT)
	ACM Transactions on Design Automation of Electronic Systems (TODAES)

REFERENCES

Deming Chen, Professor
Department of Electrical and Computer Engineering, University of Illinois Urbana-Champaign
410 Coordinated Science Lab MC 228
1308 W. Main St. Urbana Illinois 61801
(217) 244-3922
dchen@illinois.edu
(send.Deming.05A93924E9@interfolio.com)

Wen-mei Hwu, Professor
Department of Electrical and Computer Engineering, University of Illinois Urbana-Champaign
215 Coordinated Science Lab MC 228
1308 W. Main St., Urbana Illinois 61801
(217) 244-8270
w-hwu@illinois.edu
(send.Wenmei.1B2DA71402@interfolio.com)

Jinjun Xiong, Adjunct Research Professor, Program Director
Program Director, Cognitive Computing Systems Research
Thomas J. Watson Research Center, Yorktown Heights, NY USA
216 Coordinated Science Lab MC 228
1308 W. Main St. Urbana Illinois 61801
(914) 588-1515
jinjunx@illinois.edu
(send.Jinjun.62215C3137@interfolio.com)

Takeshi Yoshimura, Professor
Graduate School of Information, Production and Systems, Waseda University
2-7 Hibikino, Wakamatsu-ku, Kitakyushu, Fukuoka 808-0135, Japan
+1-90-2211-7281
t-yoshimura@waseda.jp
(send.Takeshi.A365979F4F@interfolio.com)