

# ONKAR PATIL

Graduate Research Assistant, Visa - F1(India)  
North Carolina State University, Raleigh, North Carolina

February 15, 1990  
3722 Burt Dr Apt 106 Raleigh NC 27606  
opatil@ncsu.edu, +1(669)-265-5086

## Personal Statement

I am a motivated and passionate individual with a zest for research in High Performance Computing. My primary interest lie in Memory architectures, Compilers, Programming Languages and System Software. I aspire to achieve excellence by contributing to my field of interest in every way possible. I wish to work with other aspirants and the stalwarts in Computer Science to gain immense technical expertise and intellect.

## Skills

<b>Programming/Scripting Languages</b>	C, C++, Java, HTML, Python, Perl, Shell
<b>Platforms/Architectures</b>	x86, Power9, Intel Optane DC, KNL, ARM9, NVIDIA Tesla
<b>Tools</b>	MPI, CUDA, OpenMP, OpenACC, MATLAB, GDB, qOp
<b>Compilers</b>	Cetus, OpenARC, LLVM, Clang
<b>Operating Systems</b>	Linux, EV3RT, XINU, ONTAP

## Education

- Ph.D. Computer Science** GPA: 3.182  
*North Carolina State University, Raleigh, NC* 2016 - Current
  - Research: Intelligent Data Placement for hybrid memory systems in HPC
- MS. Computer Science** GPA: 3.125  
*North Carolina State University, Raleigh, NC* 2012 - 2014
  - Thesis: Efficient and Lightweight Inter-process Collective Operations for Massive Multi-core Architectures
- BE. Information Technology** Avg: 69.2%  
*Fr. Conceicao Rodrigues College of Engineering, Mumbai, MH, India* 2008 - 2012
  - Thesis: Design and Implementation of a Parallelized and Distributed Web Crawler

## Publications

- Performance characterization of a DRAM-NVM hybrid memory architecture** MEMSYS 2019
- for HPC applications using Intel Optane DC Persistent Memory Modules**  
*O. Patil, L. Ionkov, J. Lee, F. Mueller, M. Lang* Sept. 2019
- Using Non Volatile Memories to build cost and energy efficient clusters** SC 2019  
*O. Patil, L. Ionkov, J. Lee, F. Mueller, M. Lang* Nov. 2019
- Exploring Use-cases for Non-Volatile Memories in support of HPC Resilience** SC 2017  
*O. Patil, S. Hukerikar, F. Mueller, C. Englemann* Nov. 2017
- Persistent Regions that Survive NVM Media Failure** NVM 2017  
*O. Patil, M. Kuscus, T. Tran, C. Johnson, J. Tucek, H. Kuno* Mar. 2017
- Efficient & Predictable Group Communication Messaging over Manycore NoCs** ISC 2016  
*K. Yagna, O. Patil, F. Mueller* May. 2016
- End-to-end Resilience for HPC Applications (GCS Award)** ISC 2019  
*A. Rezai, H. Khetawat, O. Patil, F. Mueller, P. Hargrove, E. Roman* Jun. 2019
- Sequential memory access on a high performance computing system** USPTO  
*C. Johnson, O. Patil, M. Kuscus, T. Tran, J. Tucek, H. Kuno, M. Chabbi, W. Scherer* Jan. 2020
- Data update of shared fabric memory in a high performance computing system** USPTO  
*C. Johnson, M. Kuscus, O. Patil, J. H. Park, H. Kuno, R. Schreiber* Feb. 2020

## Research/Work Experience

- **High Performance Computing with Heterogeneous memory systems** NCSU, Raleigh, NC  
*Ph.D candidate and Graduate Research Assistant under Dr. Frank Mueller* Aug. 2016 - Current
  - Exploring possibilities for novel software architectures that can take advantage of heterogeneous memory systems to improve resiliency, scalability and performance of HPC applications
  - Performing static code analysis to enable automated memory allocation at compiler level to improve performance and supplement resilience against hard errors
  - Developing framework for front-end and intermediate stage analysis using LLVM and Clang to extract critical code information in order to optimize HPC applications for systems with multiple memory technologies
- **Summer Research Intern** New Mexico Consortium(LANL), Los Alamos, NM  
*Computer Science Research* May. 2019 - Aug. 2019; May. 2018 - Aug. 2018
  - Analyzed the performance characteristics of Intel's Optane DC PMMs in a DRAM-NVM hybrid memory system for HPC applications
  - Developed a Compiler framework to identify critical code information for HPC applications to optimize for hybrid memory systems
- **Summer Research Intern** Oak Ridge National Laboratory, Oak Ridge, TN  
*Computer Science Research* May. 2017 - Aug. 2017
  - Designed, prototyped and evaluated a Runtime system to support Resilience Design Patterns for systems with persistent memory
- **Graduate Teaching Assistant** North Carolina State University, Raleigh, NC  
*Department of Computer Science* Jan. 2018 - May. 2018; Aug. 2016 - Dec. 2016
  - Assisted in organizing curriculum and syllabus for a seminar in Quantum Computing
  - Assisted in organizing and grading Paper reviews and talks for Advanced Distributed Systems
  - Assisted in organizing the Operating systems course for undergraduate students
- **Research Associate** Hewlett Packard Labs, Palo Alto, CA  
*Software and Data Analytics* May 2016 - Aug. 2016
  - Designed and Developed a framework for HPC Stencil applications to survive hardware failures in non-volatile memory systems with large pool of byte-addressable non-volatile memory
- **Member of Technical Staff-II** NetApp Inc., Sunnyvale, CA  
*Engineering Product Support* Aug. 2014 - May 2016
  - Provided solutions and code fixes for existing bugs related to External Authentication, CIFS, WAFL, OS, NAS
- **Pico/micro kernels for a scalable Multi-core Operating System** NCSU, Raleigh, NC  
*Graduate Research Assistant under Dr. Frank Mueller* May. 2013 - May. 2014
  - Developed and implemented pico-kernels for efficient point-to-point and collective inter-process communication avoiding contention and exploiting the shared memory architecture to achieve optimal performance up to 9x times other libraries

## Graduate Course Projects

- **Centre Power Awareness(Independent Study)** Spring 2013  
*Under Dr. Frank Mueller*
  - Developed a dynamic runtime environment for HPC which would provide trade-off between performance, energy and thermal characteristics of the system with the help of monitoring, analysis and feedback
- **Code Optimization for Scalar and Parallel Programs** Spring 2017  
*Under Dr. Xipeng Shen*
  - Implemented a source-to-source compiler using Cetus to allocate data structures in the correct MCDRAM based on the thread location on Intel KNL architecture for OpenMP programs
- **Real-time Operating Systems** Spring 2017  
*Under Dr. Frank Mueller*
  - Implemented different scheduling and resource allocation policies with EV3RT kernel and LEGO Mindstorms to operate a line following robot, segaway and obstacle avoiding robot
  - Created a client-server based IoT-cloud interaction with Nordic nRF51 board and SDK along with Raspberry Pi