Maintask Template

HW/SW Codesign WS2015

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Contents

1 Sources

The template for the main task provides a rough overview over some components that may be used. It consists of 3 main parts:

- **The hardware project** which is located in the folders "quartus" and "vhdl"
- **The NIOS 2 software** project which is located in the folder "software"
- **The PC software** in the folder "pc_software"

This template is only a showcase design and it will be necessary to adapt the design, so that the main task can be implemented! It is up to you to adapt everything needed to implement the main task.
Please make sure, that the whole design flow (compilation and download of the NIOS 2 hard- and software) can still be performed by one (!) target of the main makefile!

2 Hardware

2.1 QSys

The QSys design consists of the following components:

- **An avalon pll** which generates all necessary clock signals for the avalon IP cores, the audio codec and the SDRAM.
- **The NIOS 2 processor**.
- **The main memory** for the NIOS 2 processor where instructions and data are stored.
- **A JTAG UART** for the communication between the NIOS 2 processor and the PC.
- **A Triple-Speed Ethernet controller** which is utilized for the gigabit ethernet link.
- **A SGDMA** for transfering data to and from the Triple-Speed Ethernet controller, respectively (sgdma_rx and sgdma_tx).
- **A SDRAM controller** to utilize the SDRAM.
- **Two clock bridges** for exporting clock signals that are also used within the design.
- **An audio core** that can be used to send audio samples to the audio DAC.

- **The audio and video configuration core** that automatically initializes the audio codec.
- **An audio pll** that generates the input clock for the audio codec.
- **A textmode controller** that can be used to display text on the display.

The textmode controller is basically the same as the one used in the lab course Digital Design and Computer Architecture with a simple memory mapped avalon interface. The audio codec in the template uses a memory mapped interface. Take into consideration, that there is also the option to use a streaming interface!

3 Software

The demo software initializes all devices and then receives audio data via the ethernet interface. This data is than written to the SDRAM. If the specified number of samples was received, the audio codec is initialized and the samples are sent to the codec. After you have downloaded the software to the NIOS 2 processor you should wait for a couple of seconds until the ethernet link is ready to receive data. The reception of the audio data may take some minutes, depending on the number of samples that are specified. The codec in the template operates at a sample rate of 32kHz. Please change this rate to 48kHz for your solution!