Interfacing the LXT971A/972A to the Motorola MPC860T Fast Ethernet Controller

Application Note

February 2001

Order Number: 249401-001

As of January 15, 2001, this document replaces the Level One document known as *AN154*.

Application Note

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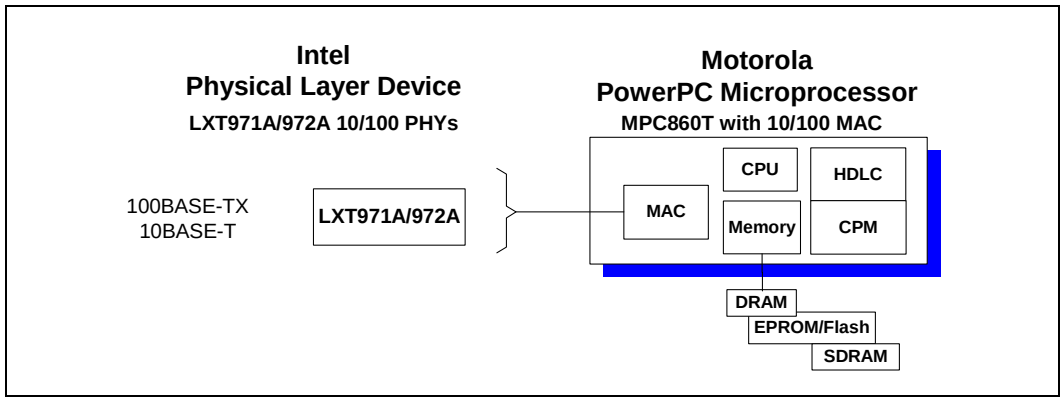
1.0 Simple Integration and Connectivity

The LXT971A or the LXT972A are excellent 10/100Mbps physical layer device choices for designs based on the Motorola MPC860T microprocessor. Either one of these devices can easily be interfaced to the Fast Ethernet Controller (FEC) of the MPC860T as illustrated in Figure 1.

Figure 1. High-Level Device Interface



1.1 Physical Layer Device Interface

The LXT971A/972A are IEEE compliant Fast Ethernet PHY transceivers that directly support both 100BASE-TX and 10BASE-T applications. The Media Independent Interface (MII) feature of the devices allows for easy attachment to the MPC860T Fast Ethernet controller, enabling the microprocessor to support full-duplex operation at 10Mbps and 100Mbps. Both devices' operating condition may be set using auto-negotiation, parallel detection, or manual (forced settings) control. The LXT971A/972A are fabricated with an advanced CMOS process and require only a single 3.3V power supply.

1.2 Microprocessor Interface

The Motorola MPC860T microprocessor includes:

- Highly integrated PowerPC™ Processor
- Serial Communications Channels (SCC)
- Communications Processor Module (CPM)
- 10/100Mbps Fast Ethernet Controller (FEC)

The MPC860T provides protocol processing for 64 time-division-multiplexed channels, multichannel protocol processing, and 10/100Mbps Ethernet in one chip—ideal for high-performance, low-cost networking equipment designs.

2.0 Time-to-Market and Features Advantage

Intel's LXT971A/972A devices, combined with the Motorola MPC860T Fast Ethernet controller, provide a scalable 10/100Mbps solution for value-added networking equipment designs.

For designs based on the Motorola MPC860T microprocessor, where time-to-market and added value are highly regarded, choosing the accompanying 10/100 PHY is a decision that affects both the project schedule and the LAN connectivity features of the product. The LXT971A/972A may yield time-to-market and feature-augmentation advantages by leveraging on the devices' strengths:

- MII (MPC860T compatible) interface with extended register capability.
- Supports auto-negotiation and parallel detection.
- Standard CSMA/CD or full-duplex operation.
- 10BASE-T and 100BASE-TX using a single RJ-45 connection.
- Integrated, programmable LED drivers.
- Robust baseline wander correction performance.
- Configurable via MDIO serial port or hardware control pins.
- Low-power "Sleep" mode (LXT971A only).

3.0 Device Features

3.1 Intel's LXT971A 10/100Mbps Transceiver

- 3.3V Operation.
- Low power consumption (300mW typical).
- Low-power "Sleep" mode
- 10BASE-T and 100BASE-TX using a single RJ-45 connection.
- Supports auto-negotiation and parallel detection.
- MII interface with extended register capability.
- Robust baseline wander correction performance.
- 100BASE-FX fiber optic capable.
- Standard CSMA/CD or full-duplex operation.
- Configurable via MDIO serial port or hardware control pins.
- Integrated, programmable LED drivers.
- 64-pin Plastic Ball Grid Array (PBGA).
  - — LXT971ABC - Commercial (0° to 70°C ambient).
  - — LXT971ABE - Extended (-40° to 85°C ambient).
- 64-pin Low-profile Quad Flat Package (LQFP).
  - — LXT971ALC - Commercial (0° to 70°C ambient).
  - — LXT971ALE - Extended (-40° to 85°C ambient).

3.2 Intel's LXT972A 10/100Mbps Transceiver

The LXT972A is a cost-reduced version of the LXT971A, and does not support the following features:

- Low-power sleep mode.
- 100BASE-FX fiber optic capability.
- Extended temperature capability.

The LXT972A is only available in:

- 64-pin compatible Quad Flat Package (LQFP).
  - LXT972ALC - Commercial (0° to 70° C ambient).

3.3 Motorola's MPC860T Microprocessor

10/100 Ethernet Support:

- Full IEEE 802.3 compliance
- Support for three interfaces:
  - 100Mbps 802.3 MII
  - 10Mbps 802.3 MII
  - 10Mbps 7-wire interface
- Support for half-duplex, 100Mbps operation
- Support for full-duplex, 100Mbps operation
- Large on-chip Tx/Rx FIFOs to support a variety of bus latencies
- Reduced bus utilization due to retransmission from transmit FIFO following a collision
- Automatic internal flushing of the receive FIFO for runts and collision fragments reduces bus utilization
- Off-chip buffer descriptor rings of user-definable size allow flexible transmit and receive buffer memory management

10/100 Media Access Control (MAC) Features:

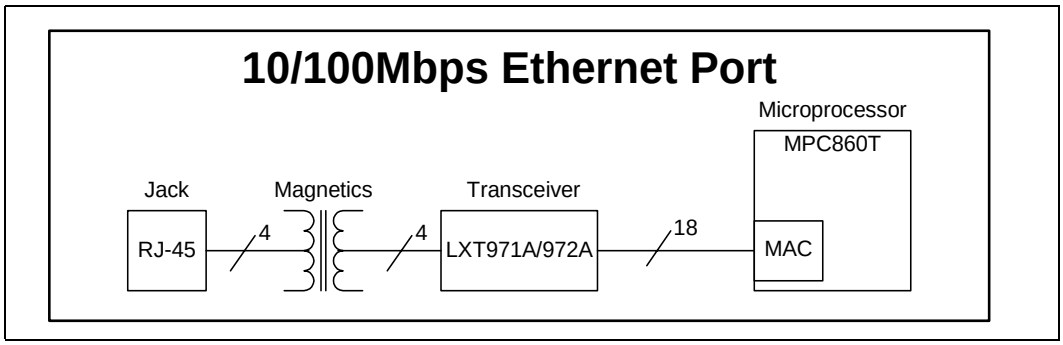
- Address Recognition
  - Broadcast
  - Single station address
  - Promiscuous mode
  - Multicast hashing
- Full support of the MII
- Interrupt modes
  - Per frame
  - Per buffer (optional)

4.0 Device Interfacing

4.1 10/100Mbps Ethernet Port

When combined with the LXT971A/972A, magnetics, and an RJ-45 jack, the Motorola MPC860T provides a complete 10/100Mbps port. The LXT971A/972A transceiver connects directly to the Motorola MPC860T through the 18 signals of the Media Independent Interface (MII). Figure 2 displays this setup.

Figure 2. 10/100Mbps LAN Port



4.2 Selecting the Interface

The MPC860T provides support for MII and 7-pin interfaces. The mode is controlled by bit 29 (MII_MODE) of the Receive Control (R_CNTRL) register.

- Set bit 29 = 1 to select MII mode for 10/100M.

4.3 10/100Mbps MII Connections

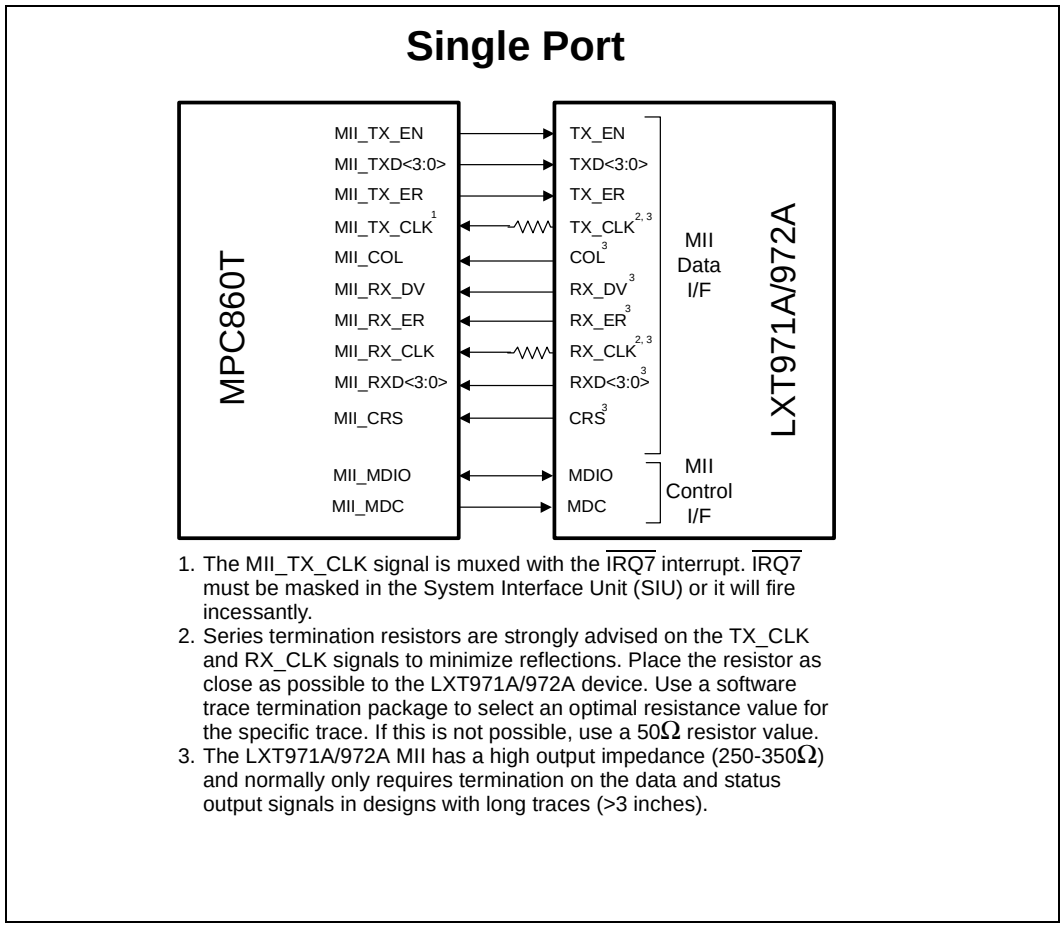
The MII can be used to add a single 10/100Mbps port to the MPC860T illustrated in Figure 3. The LXT971A/LXT972A provide a single MII interface that connects to the MPC860T MII port. Table 1 on page 10 lists signal descriptions, mnemonics and pin assignments for the MII connection between the two devices.

The MPC860T re-maps Port D to support the MII function. To enable the MII interface on Port D, write the following:

0x1fff to PDPAR
0x1fff to PDDIR.

Four additional 860T pins (MII_COL, MII_CRS, MII_TX_EN, and MII_MDIO) are enabled when Port D is set for MII operation and not used in any other application.

Figure 3. Signal-Level Device Interface



1. The MII_TX_CLK signal is muxed with the $\overline{\text{IRQ7}}$ interrupt. $\overline{\text{IRQ7}}$ must be masked in the System Interface Unit (SIU) or it will fire incessantly.
2. Series termination resistors are strongly advised on the TX_CLK and RX_CLK signals to minimize reflections. Place the resistor as close as possible to the LXT971A/972A device. Use a software trace termination package to select an optimal resistance value for the specific trace. If this is not possible, use a 50Ω resistor value.
3. The LXT971A/972A MII has a high output impedance (250-350Ω) and normally only requires termination on the data and status output signals in designs with long traces (>3 inches).

Table 1. 10/100 MII Connections for the LXT971A (LQFP Package)

MPC860T		Flow		LXT971A		Signal Descriptions
Pin #	Signal Name	Flow	Serial R	Pin #	Signal Name	
U17 V19 V18 W18	MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	⇐ ⇐ ⇐ ⇐	No[3] No[3] No[3] No[3]	45 46 47 48	RXD3 RXD2 RXD1 RXD0	**Receive Data.** LXT971A/972A transmits received data to the MPC860T on these lines. The data is driven on the falling edge of MII_RXCLK.
V16	MII_RX_DV	⇐	No[3]	49	RX_DV	**Receive Data Valid.** LXT971A/972A asserts this signal High, synchronous to RX_CLK, to indicate valid data on RXD<3:0>.
W17	MII_RX_CLK	⇐	Yes[2,3]	52	RX_CLK	**Receive Clock.** LXT971A/972A provides this 2.5 or 25 MHz clock derived from the data or from the device's 25 MHz input clock (CLK25).
T15	MII_RX_ER	⇐	No[3]	53	RX_ER	**Receive Error.** LXT971A/972A drives this active High signal, synchronous to RX_CLK, to indicate it is sending invalid data on RXD<3:0>.
T16	MII_TX_ER	⇒	No	54	TX_ER	**Transmit Error.** When the 860T asserts this signal while TX_EN is asserted, the LXT971A/972A drives invalid symbols onto the line.
W15	MII_TX_CLK[1]	⇐	Yes[2,3]	55	TX_CLK	**Transmit Clock.** LXT971A/972A provides this 2.5 or 25 MHz continuous output derived from its 25 MHz input clock (CLK25).
V15	MII_TX_EN	⇒	No	56	TX_EN	**Transmit Enable.** The 860T asserts this signal High when it is presenting valid data on the MII_TXD<3:0> pins.
U15 U16 W16 V17	MII_TXD3 MII_TXD2 MII_TXD1 MII_TXD0	⇒ ⇒ ⇒ ⇒	No No No No	60 59 58 57	TXD3 TXD2 TXD1 TXD0	**Transmit Data.** The 860T sends data to LXT971A/972A on these pins. The LXT971A/972A samples TXD<3:0> on the rising edge of TX_CLK, when TX_EN is High.

1. The MII_TX_CLK signal is muxed with the $\overline{\text{IRQ7}}$ interrupt. $\overline{\text{IRQ7}}$ must be masked in the SIU or it will fire incessantly.
2. Series termination resistors are strongly advised on the TX_CLK and RX_CLK signals to minimize reflections. Place the resistor as close as possible to the LXT971A/972A device. Use a software trace termination package to select an optimal resistance value for the specific trace. If this is not possible, use a 50Ω resistor value.
3. The LXT971A/972A MII has a high output impedance (250-350Ω) and normally only requires termination on the data and status output signals in designs with long traces (>3 inches).

Table 1. 10/100 MII Connections for the LXT971A (LQFP Package) (Continued)

MPC860T		Flow		LXT971A		Signal Descriptions
Pin #	Signal Name	Flow	Serial R	Pin #	Signal Name	
H4	MII_COL	⇐	No[3]	62	COL	**Collision.** LXT971A/972A drives this signal High to indicate that a collision has occurred.
B7	MII_CRS	⇐	No[3]	63	CRS	**Carrier Sense.** LXT971A/972A drives this signal High when it is transmitting or receiving.
H18	MII_MDIO	⇐ ⇒	No	42	MDIO	**Management Channel.** This bidirectional channel provides read/write access to the LXT971A/972A register set.
R16	MII_MDC	⇒	No	43	MDC	**Management Channel Clock.** This 860T provides the clock for the MDIO channel.

1. The MII_TX_CLK signal is muxed with the $\overline{\text{IRQ7}}$ interrupt. $\overline{\text{IRQ7}}$ must be masked in the SIU or it will fire incessantly.
2. Series termination resistors are strongly advised on the TX_CLK and RX_CLK signals to minimize reflections. Place the resistor as close as possible to the LXT971A/972A device. Use a software trace termination package to select an optimal resistance value for the specific trace. If this is not possible, use a 50Ω resistor value.
3. The LXT971A/972A MII has a high output impedance (250-350Ω) and normally only requires termination on the data and status output signals in designs with long traces (>3 inches).

Intel around the world

United States and Canada
Intel Corporation
Robert Noyce Building
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119
USA
Phone: (800) 628-8686

Europe
Intel Corporation (UK) Ltd.
Pipers Way
Swindon
Wiltshire SN3 1RJ
UK

Phone:

England	(44) 1793 403 000
Germany	(49) 89 99143 0
France	(33) 1 4571 7171
Italy	(39) 2 575 441
Israel	(972) 2 589 7111
Netherlands	(31) 10 286 6111
Sweden	(46) 8 705 5600

Asia-Pacific
Intel Semiconductor Ltd.
32/F Two Pacific Place
88 Queensway, Central
Hong Kong, SAR
Phone: (852) 2844 4555

Japan
Intel Kabushiki Kaisha
P.O. Box 115 Tsukuba-gakuen
5-6 Tokodai, Tsukuba-shi
Ibaraki-ken 305
Japan
Phone: (81) 298 47 8522

South America
Intel Semicondutores do Brazil
Rue Florida, 1703-2 and CJ22
CEP 04565-001 Sao Paulo-SP
Brazil
Phone: (55) 11 5505 2296

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