D-PHY Tutorial

PHY Working Group

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Overview

D-PHY >

- **Introduction**
- Architecture
- Electrical
- Timing
- Global Operation
- Interconnect
- PHY-Protocol Interface
- Summary
- Q & A

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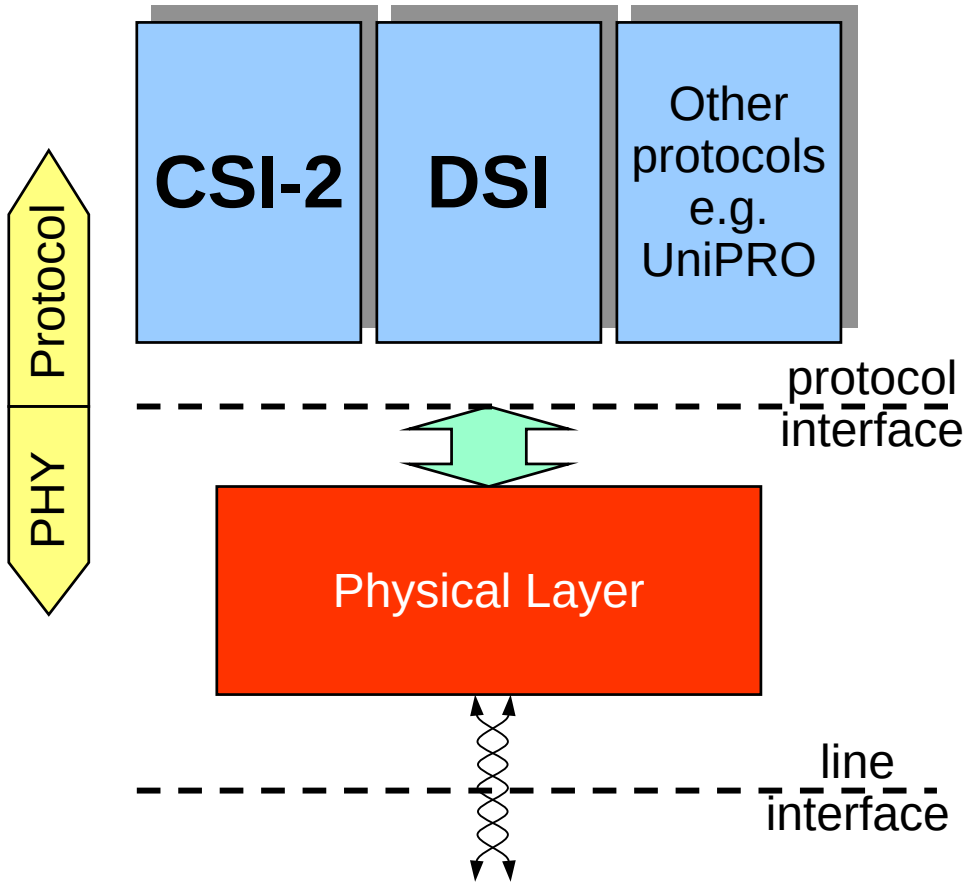
Objectives

- Specify an unified PHY which supports:
  - Display protocol
  - Camera protocol
  - Future MIPI protocols, including UniPRO
- Features
  - High bandwidth
  - Minimal power
  - Supports technology scaling
  - Low implementation complexity



Application Requirement Summary

- Bit rate 80-1000 Mb/s
- Across ‘bad’ channels including flex-foils
- Distance 0-20cm
- Low operational power (mW-range)
- Very low stand-by power (μW-range)
- Low EMI
- Low wire count
- Robustness in a noisy environment
  - noise magnitude: ~10mV$_{dif}$ ~100mV$_{com}$
- Support for bi-directionality
- Ease of integration
- Lane scalability

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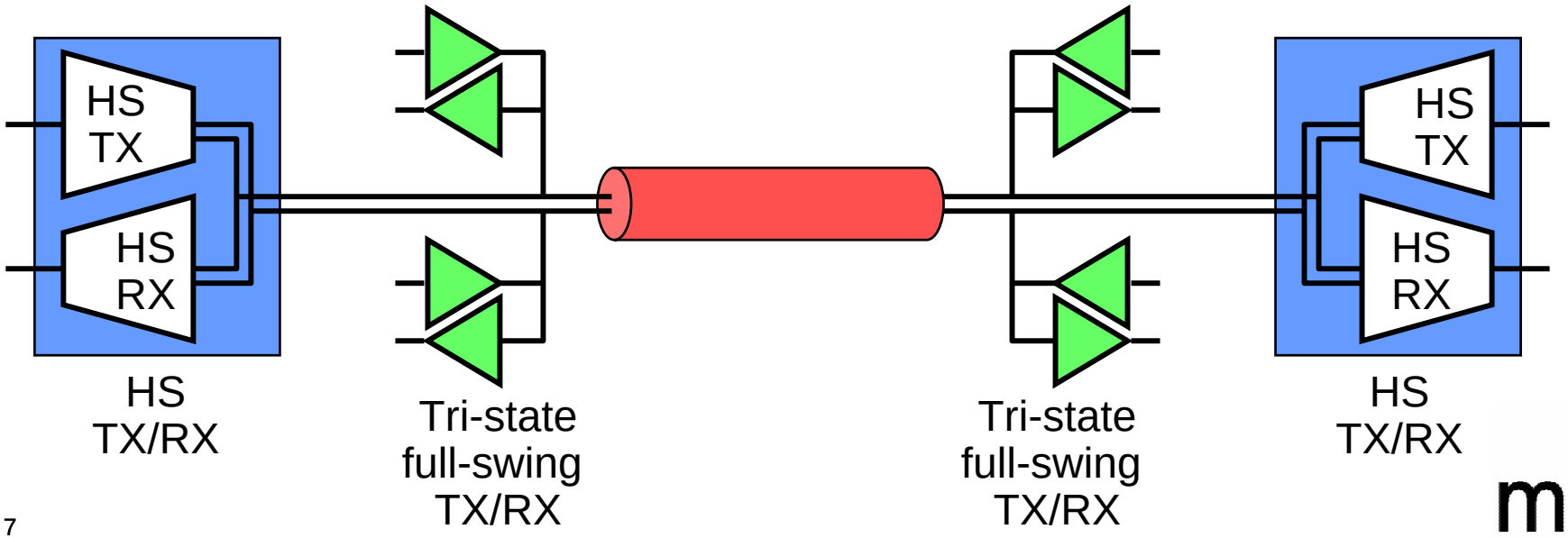
Conceptual choices

- Serial High-speed: Fully terminated differential signaling
- Low-Power: Unterminated 1.2V CMOS-like signaling
- Transmission line interconnect needed
- First generation: Source synchronous & no encoding
- Bi-directionality and contention detection



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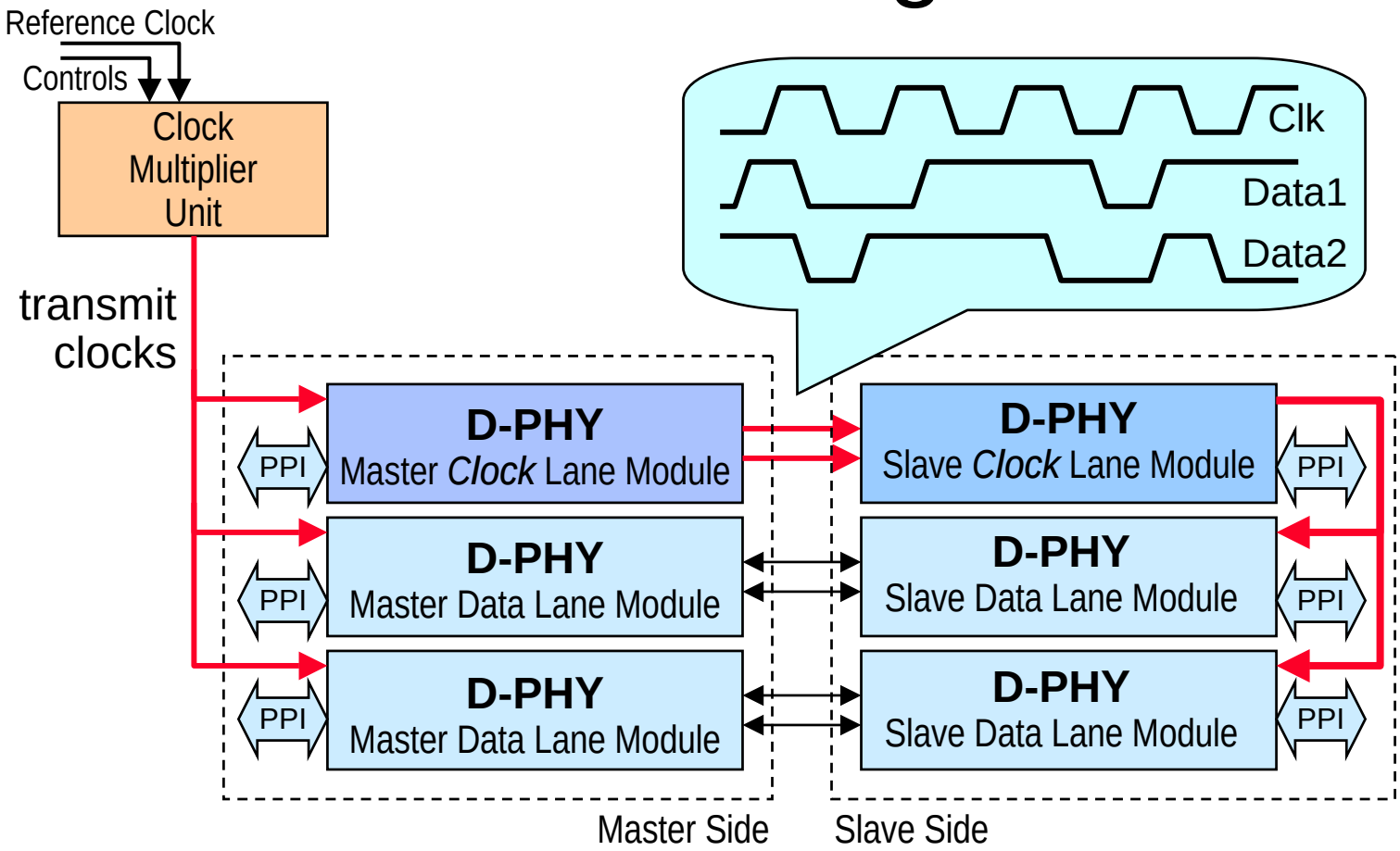
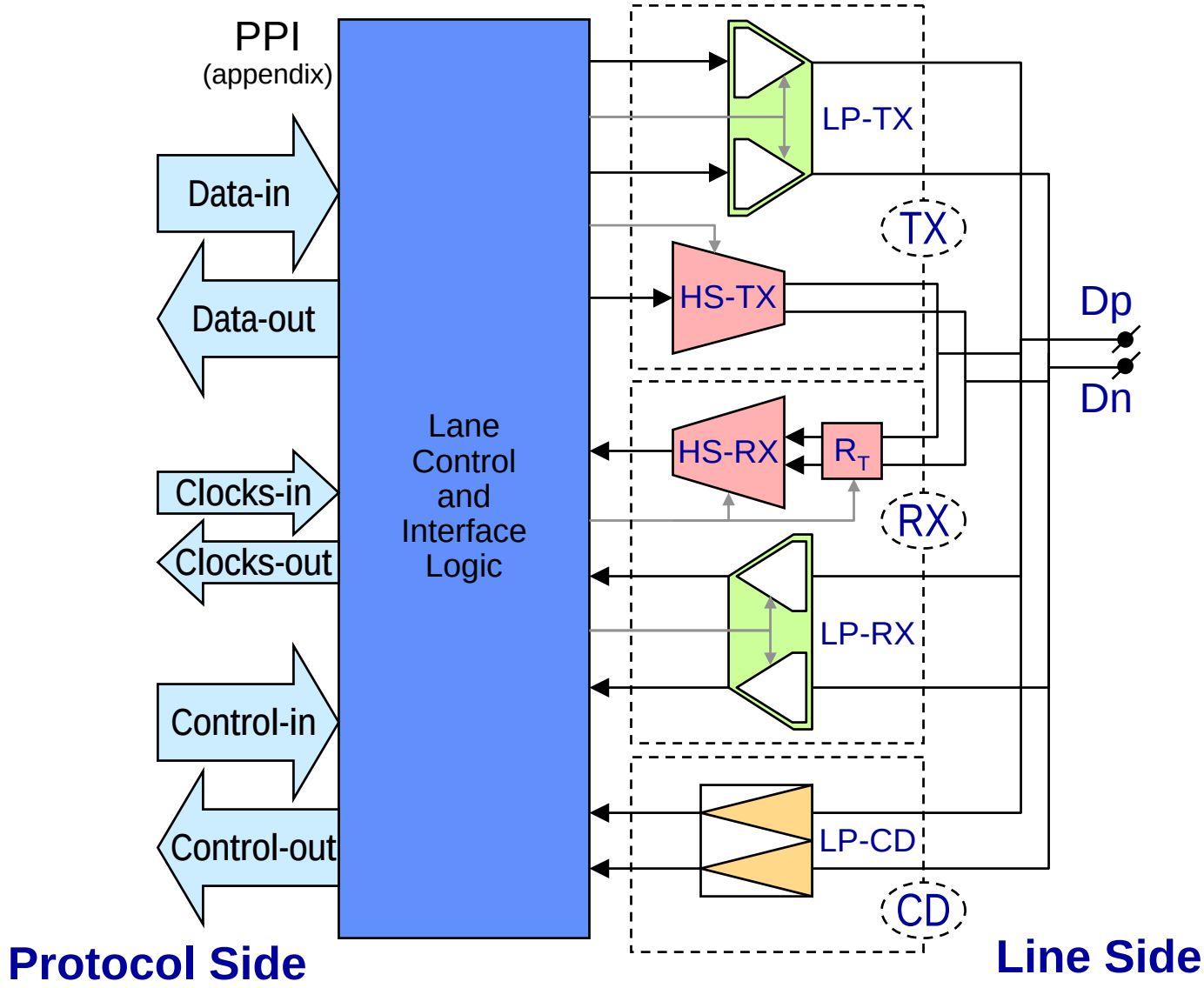
PHY Configuration



- One Clock Lane for one or more Data Lanes
- Source Sync: Clock direction from Master to Slave

Universal Lane Architecture



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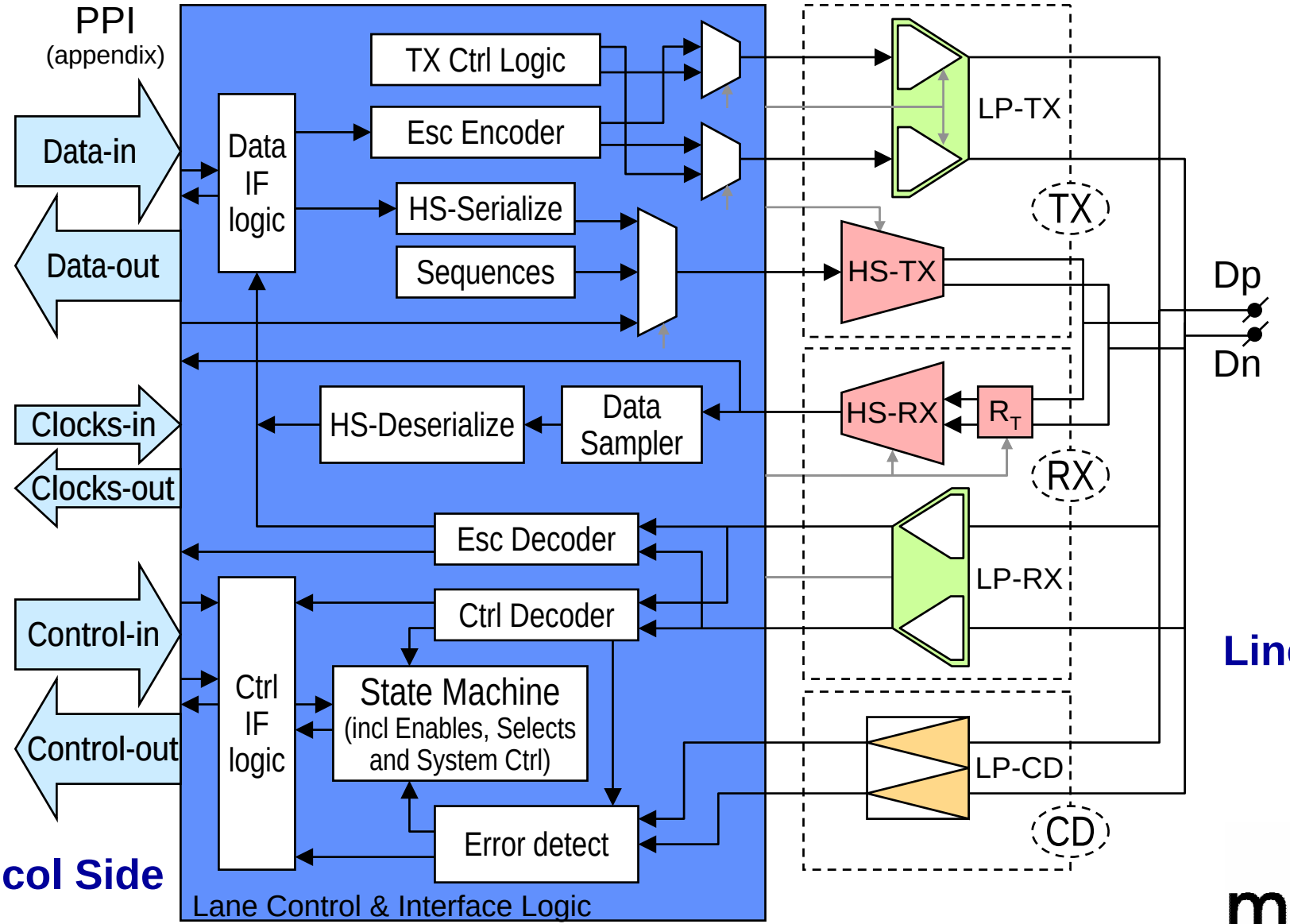
Universal Lane Architecture



Mandatory versus Optional

Mandatory

- High-Speed Forward signaling
- Basic Forward Low-Power Control Capabilities

Optional features

- Escape Mode signaling in Forward direction
- Bi-directionality
  - High-Speed Reverse Signaling
  - Escape Mode signaling in Reverse direction

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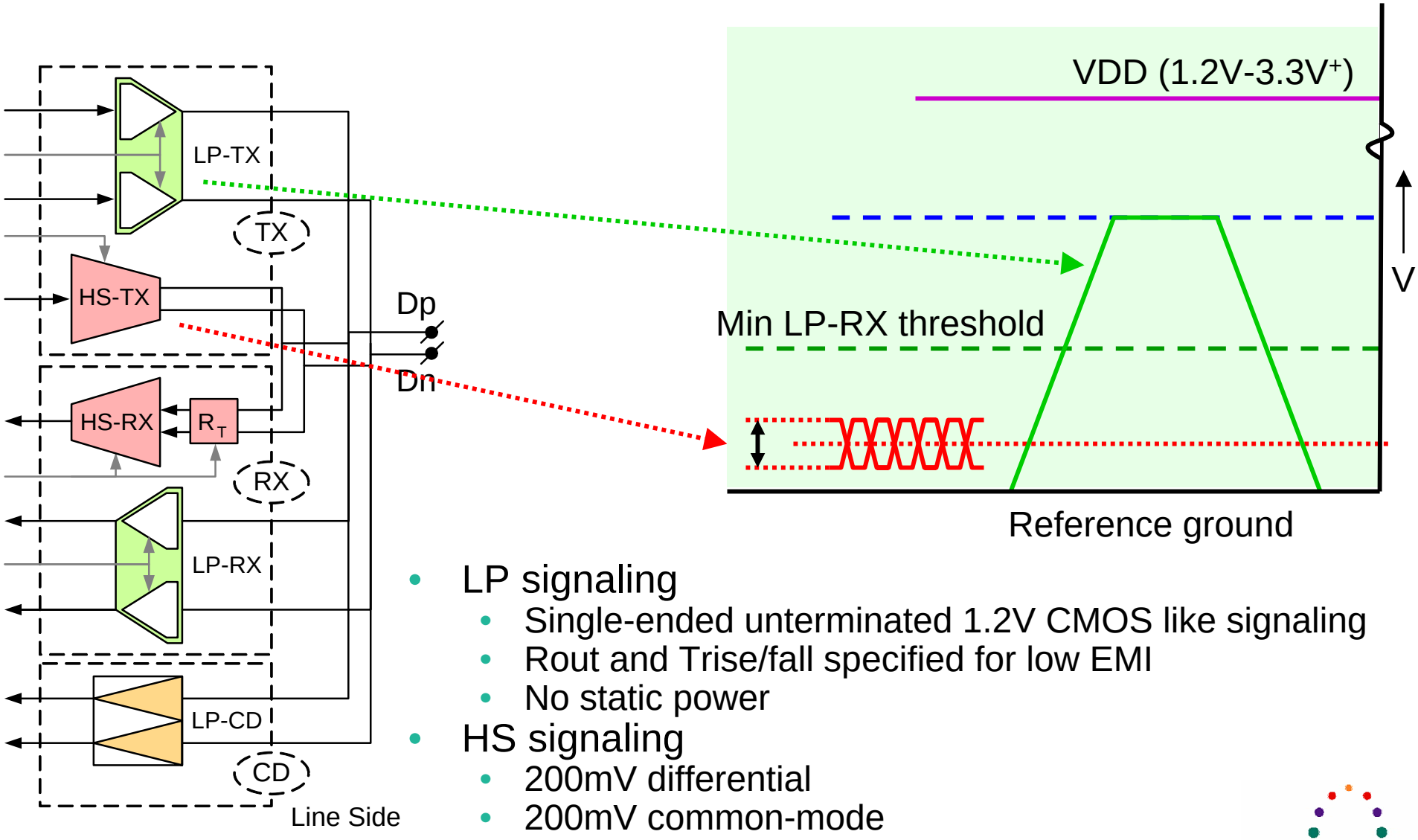
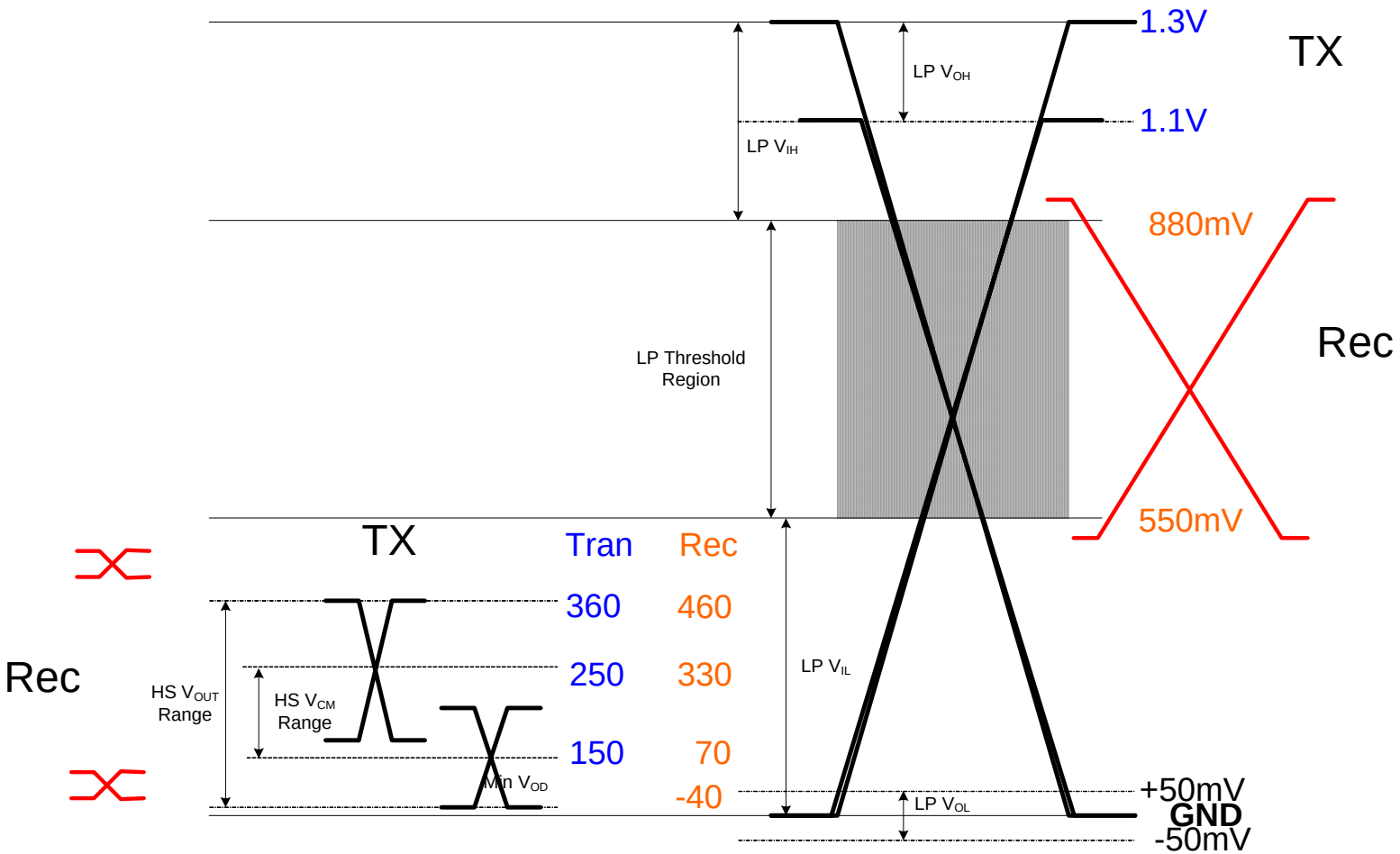
Low Power & Low EMI on 2 Wires



- LP signaling
  - Single-ended unterminated 1.2V CMOS like signaling
  - Rout and Trise/fall specified for low EMI
  - No static power
- HS signaling
  - 200mV differential
  - 200mV common-mode
  - Double terminated

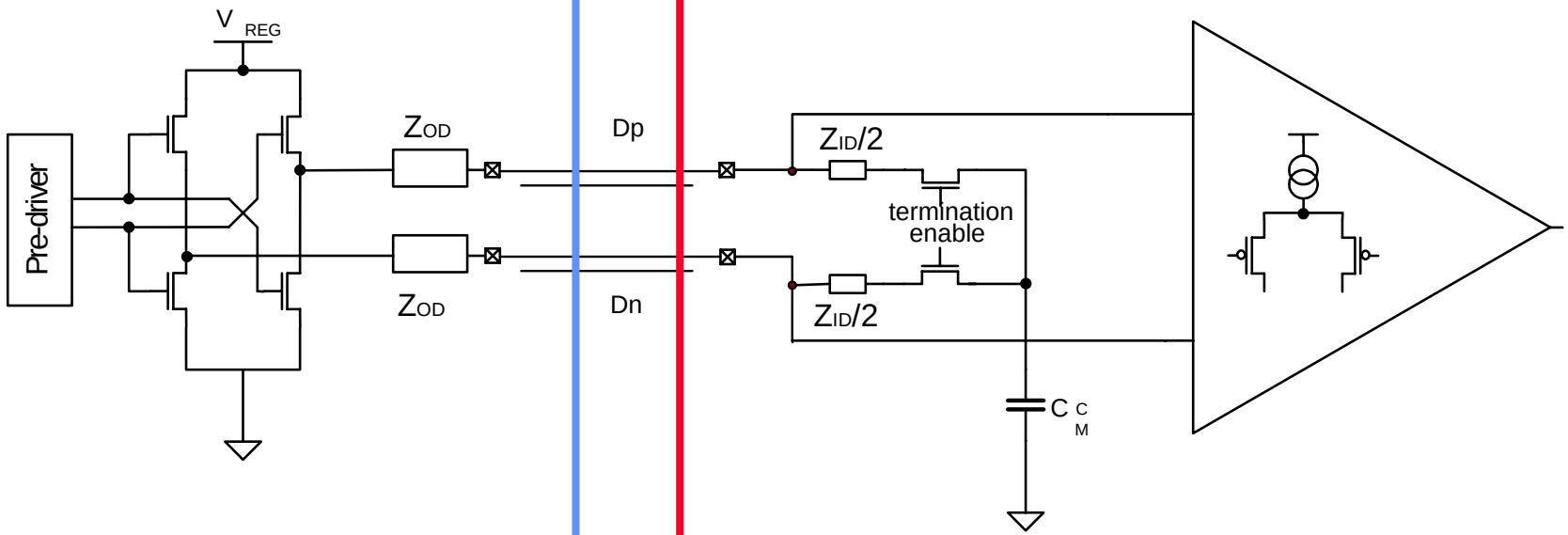
Large Signal Margins



140 mV < |Differential Signal| < 270mV

70mV

HS Driver & Receiver

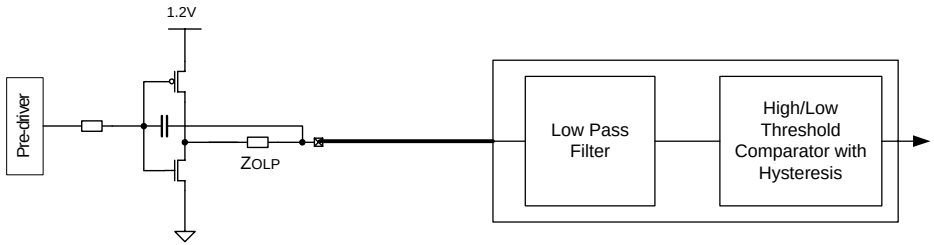


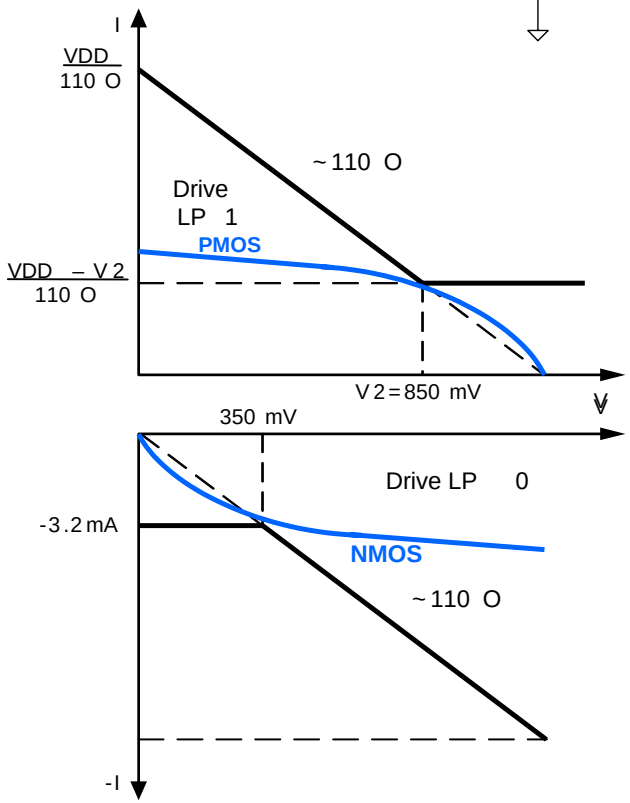
- Voltage or Current Mode Driver
- Z_{OD} = 50 Ω nominal
- Switchable to “Tristate”
- Minimum rise time = 150ps
- Maximum rise time = .3UI_{NOM}

- Differential Receiver
- 100Ω Differential Termination
- Common-mode decap to ground
- Switchable termination
- Common mode AC rejection (200mV at >450MHz)

LP Driver & Receiver

D_P and D_N are two independent single-ended links in LP-mode!



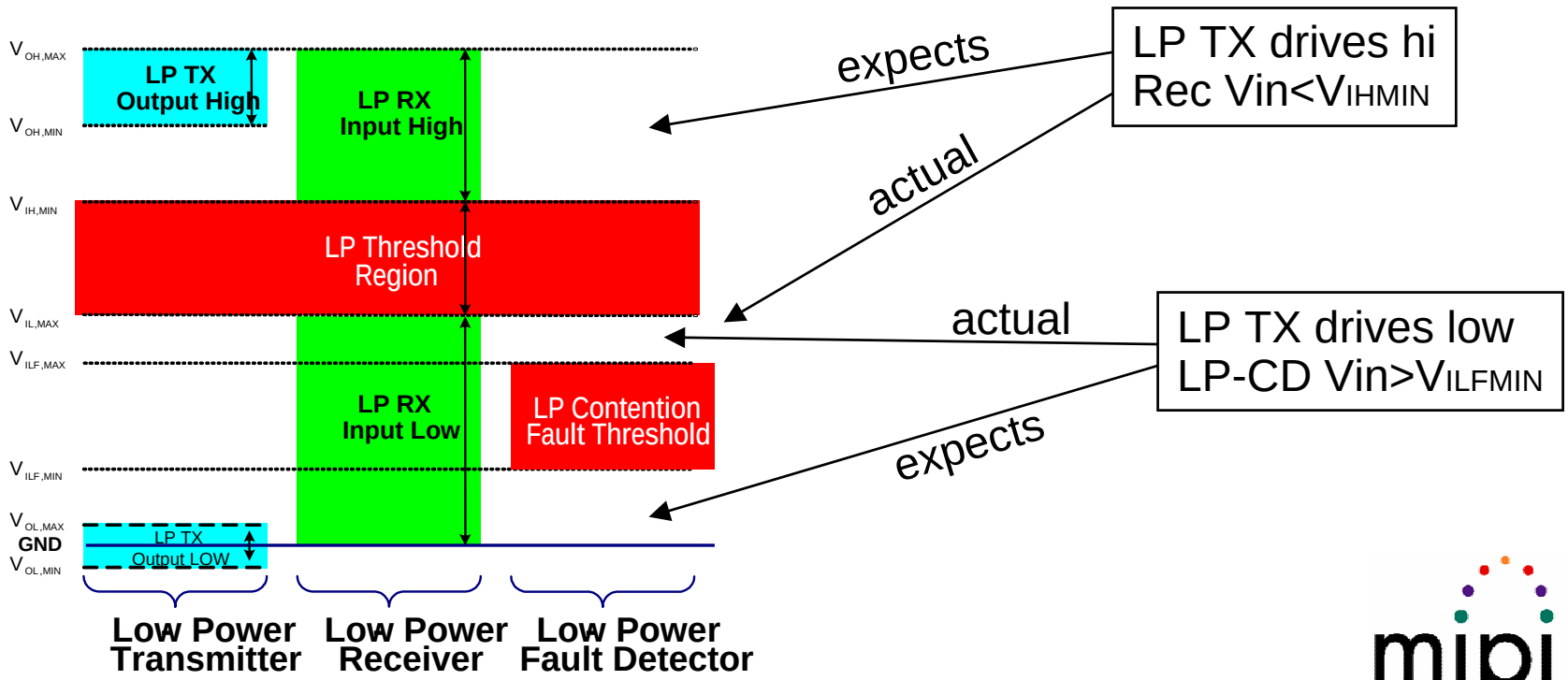


- Driver specified as Thevenin Equivalent V & Z
- Z_{OLP} for low EMI
- Trise/fall <25ns for 70pF load

- Receiver specified for noise rejection, not speed
- LPF input rejects up to 400mV of RF at f > 450 MHz
- Glitches rejection of <300V-psec
- Hysteresis >25mV

Line Contention Detection

- If LP bidirectional functions present in lane, LP contention detection must also exist
  - LP receiver must always be enabled and observed (sampled)
  - LP-CD circuit must be provided
- Two contention situations must be detected by D-PHY hardware
  - 2 LP TX driving opposite levels on same line
  - LP TX drives LP1 while HS TX drives HS0



Electrical Summary

- Electrical specification enables robust sharing of signal pair between High Speed and Low Power mode communication within 1.2V
  - Doubly terminated 50Ω single-ended/100Ω differential in HS
  - High Input noise rejection for LP mode
- Minimizes radiated EMI and EMI susceptibility
- High data transmission rate at low BER, low power in hostile environment
- Low speed channel without DC power
  - Provision made to minimize standby power if 1.2V regulator required (ULPM)
- Optional half-duplex, bidirectional operation

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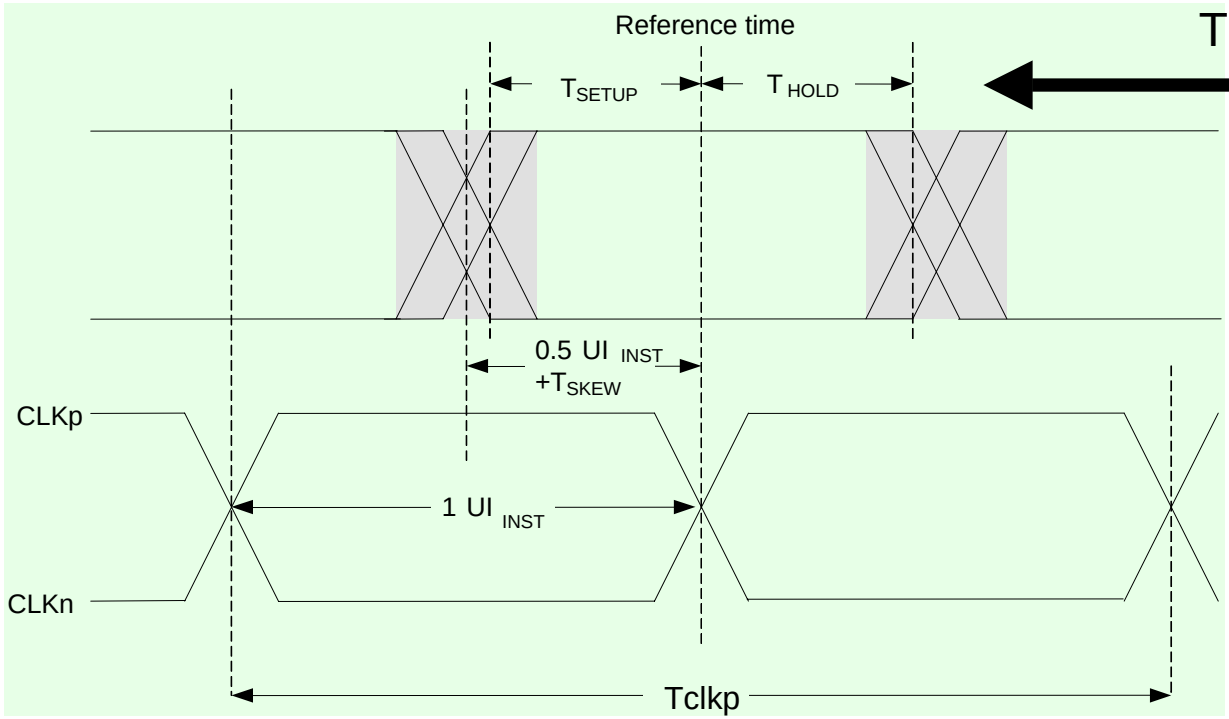
High Speed Clock Timing

- Data are launched and sampled with a DDR clock supplied on the Clock Lane from Master side
- DDR clock generation not part of D-PHY
  - PLL characteristics determine how to meet timing specs
- All D-PHY HS Clock timing specs normalized to UI
  - D-PHY operates in range of 80Mbps to <1Gbps /Data Lane
- Forward data transfers are source synchronous
- Optional reverse data transfers are Master synchronous
- Clock is always in quadrature to data
  - Simplifies slave design

Forward Data Transfer Timing



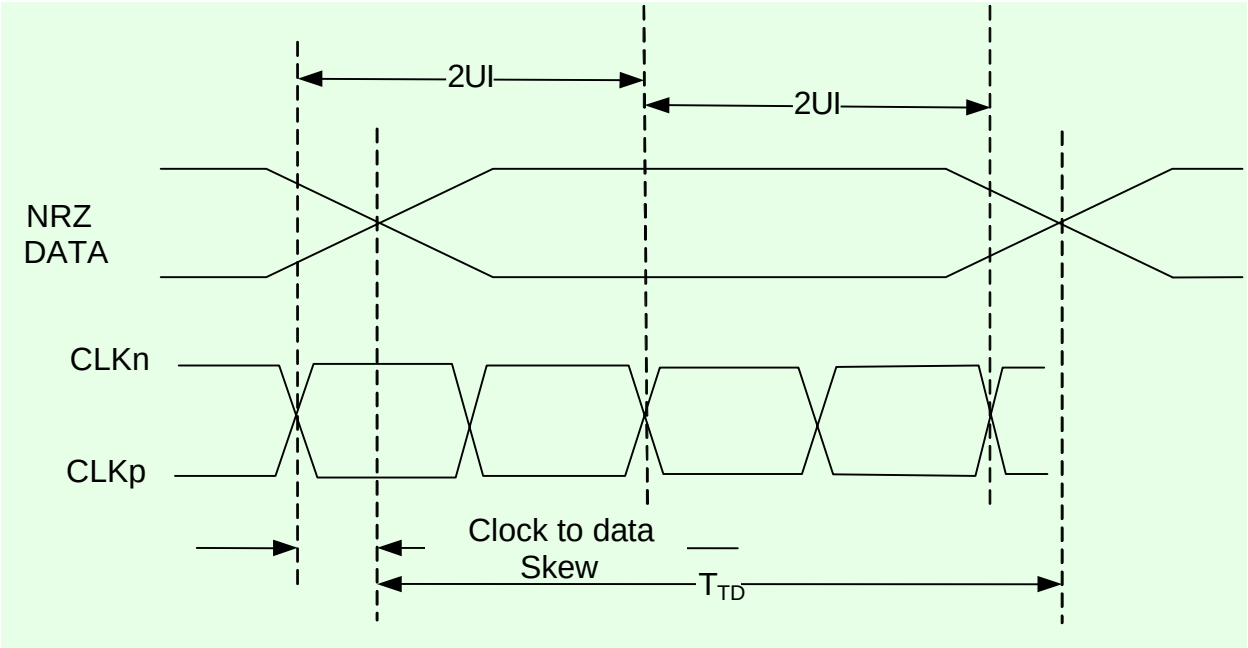
Total .3UI SU+Hld window for receiver

Large Clock and Data Jitter + duty cycle distortion allowed
[referred to 1us average]

All timings referenced to Crossing of clock signal pair

Optional Reverse Data Transfer Timing

- Clock is supplied by master (not Source Synchronous)
- Data rate = ¼ of possible forward rate



- Slave uses any edge of DDR clock to launch data
- Master determines which edge to use to sample received data
- Data to clock skew and round trip delay not specified
- Same UI variation in clock as forward transfer

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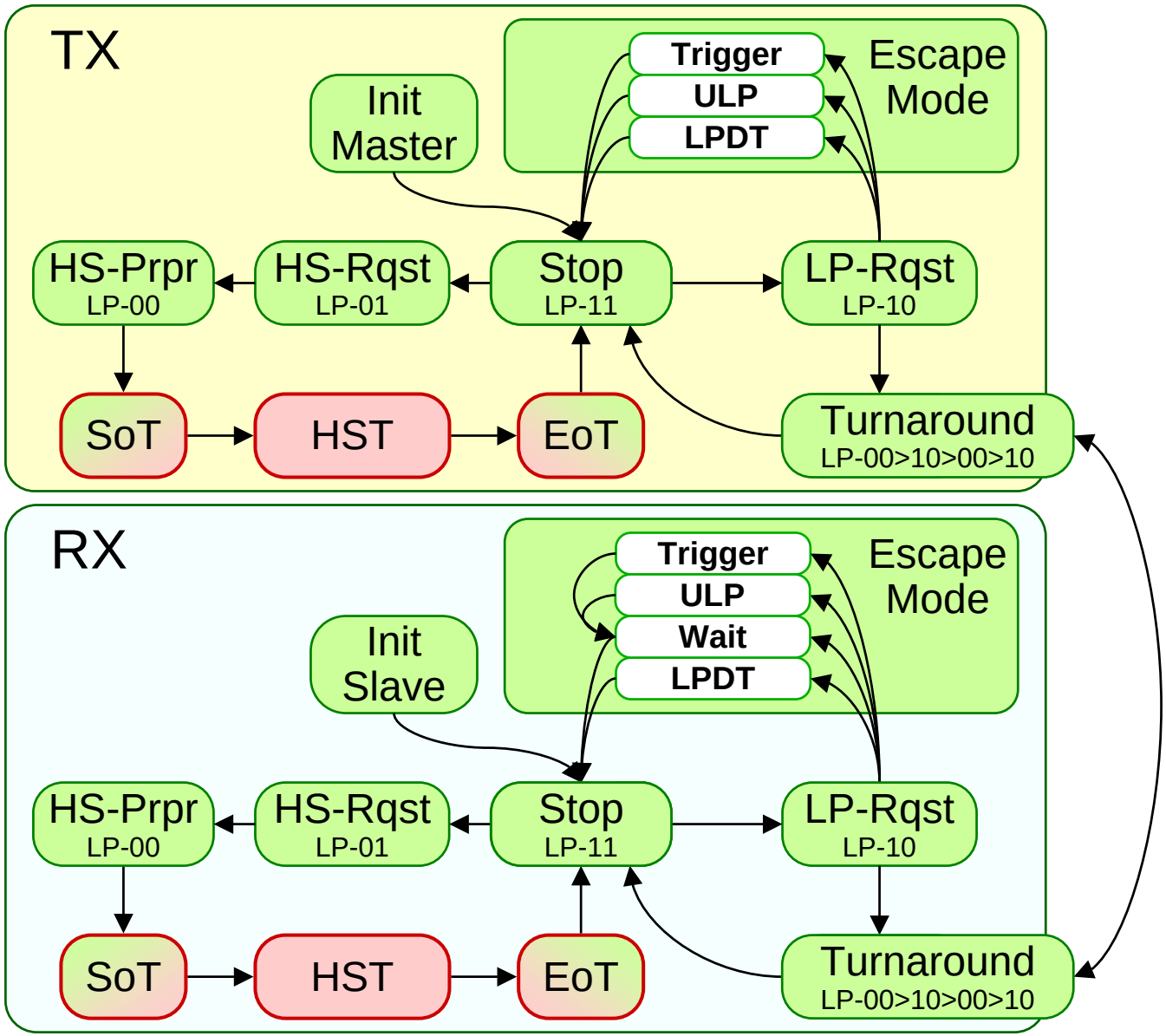
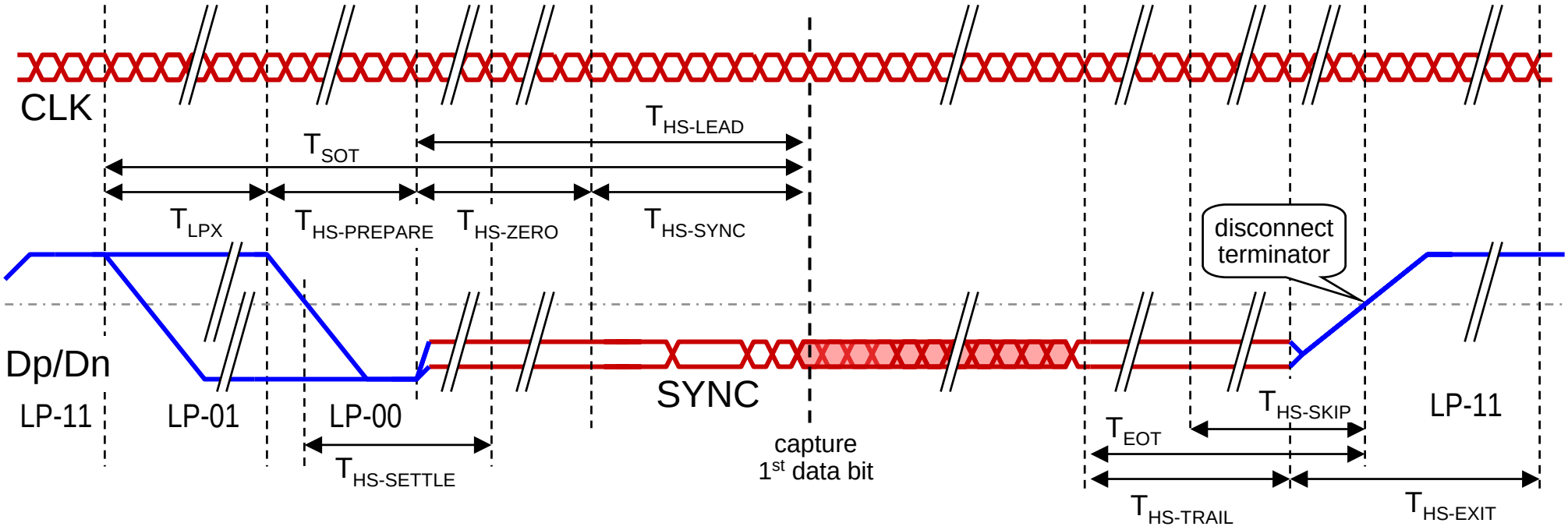
Data Lane Flow Diagram

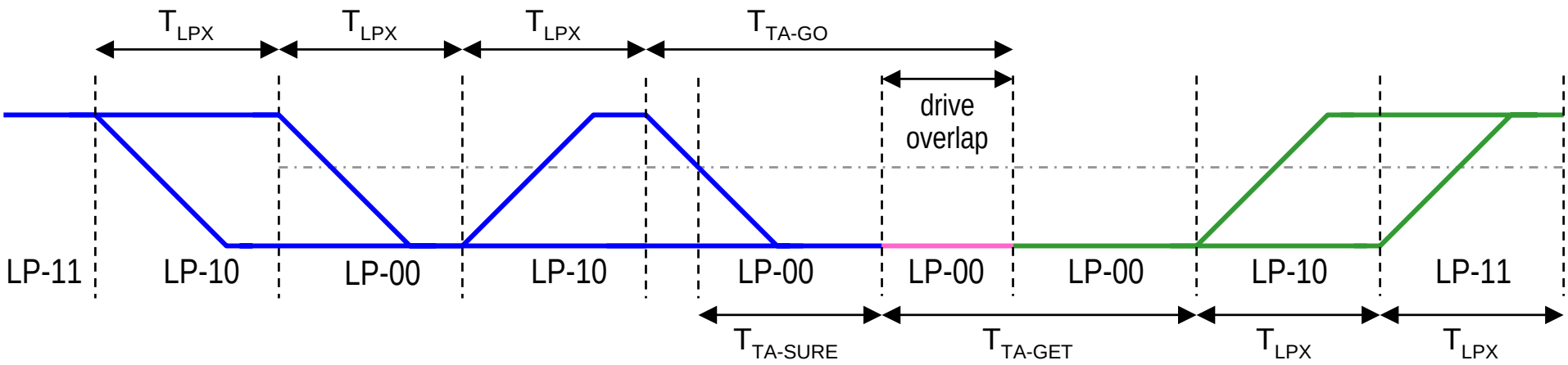


Source Sync: Data Burst



- Clock keeps running and samples data lanes (except for lanes in LPS)
- Unambiguous leader and trailer sequences required to distill real data bits
- Trailer is removed inside PHY (a few bytes)
- Time-out to ignore line-values during line-state transition

Link turnaround

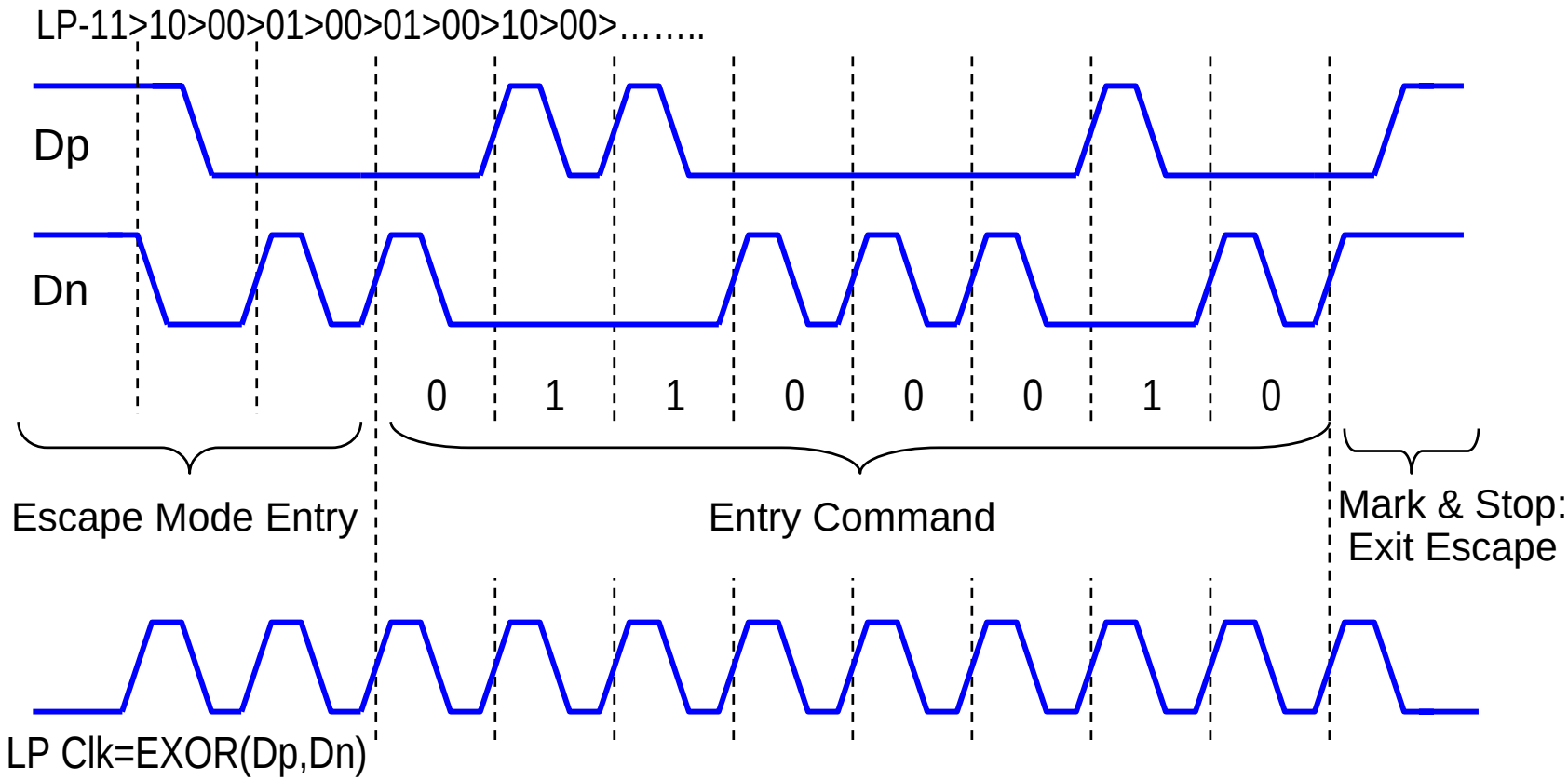


- All during Low-Power mode
- Request sequence (LP11)-LP10-LP00-LP10-LP00…..
- Actual switching of direction during double LP-00 drive: no glitch
- Line levels remain always well-defined

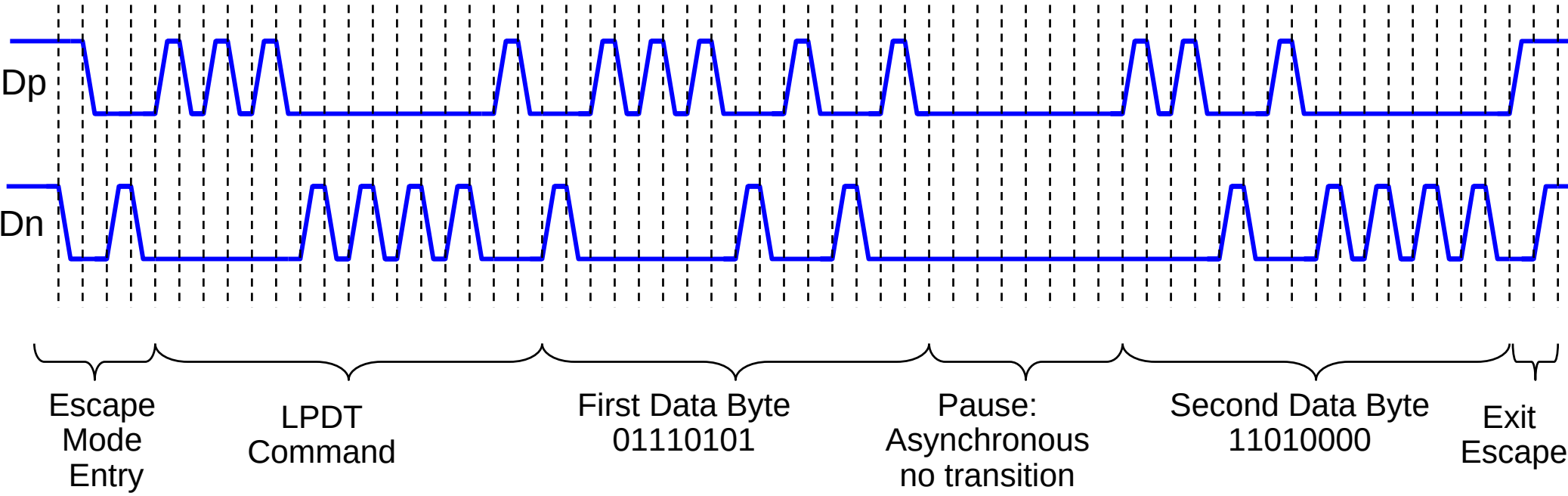
LP Escape Mode

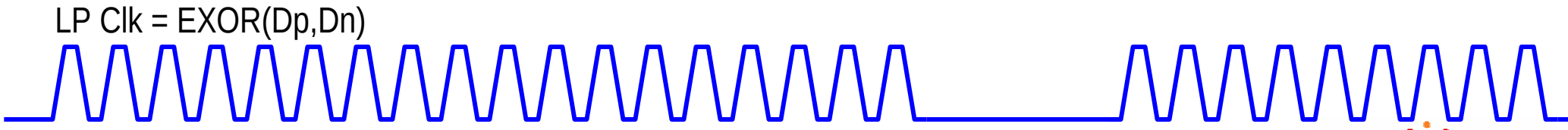
- A special mode of operation for Data Lanes using the low power line states
- Asynchronous communication using two wires
  - Does not depend on clock lane
  - Maximum data rate 10 Mbit/s
- Escape mode commands add extra 8 functions
  - Low power data transfer
  - Ultra low power mode
  - 4 remote triggers
  - 2 reserved functions
- Function selected by Entry codes
  - 8-out-of-256 codes selected for maximum robustness
  - In case of code mismatch everything is ignored till next Stop state

Escape Mode signaling
Trigger Reset Example

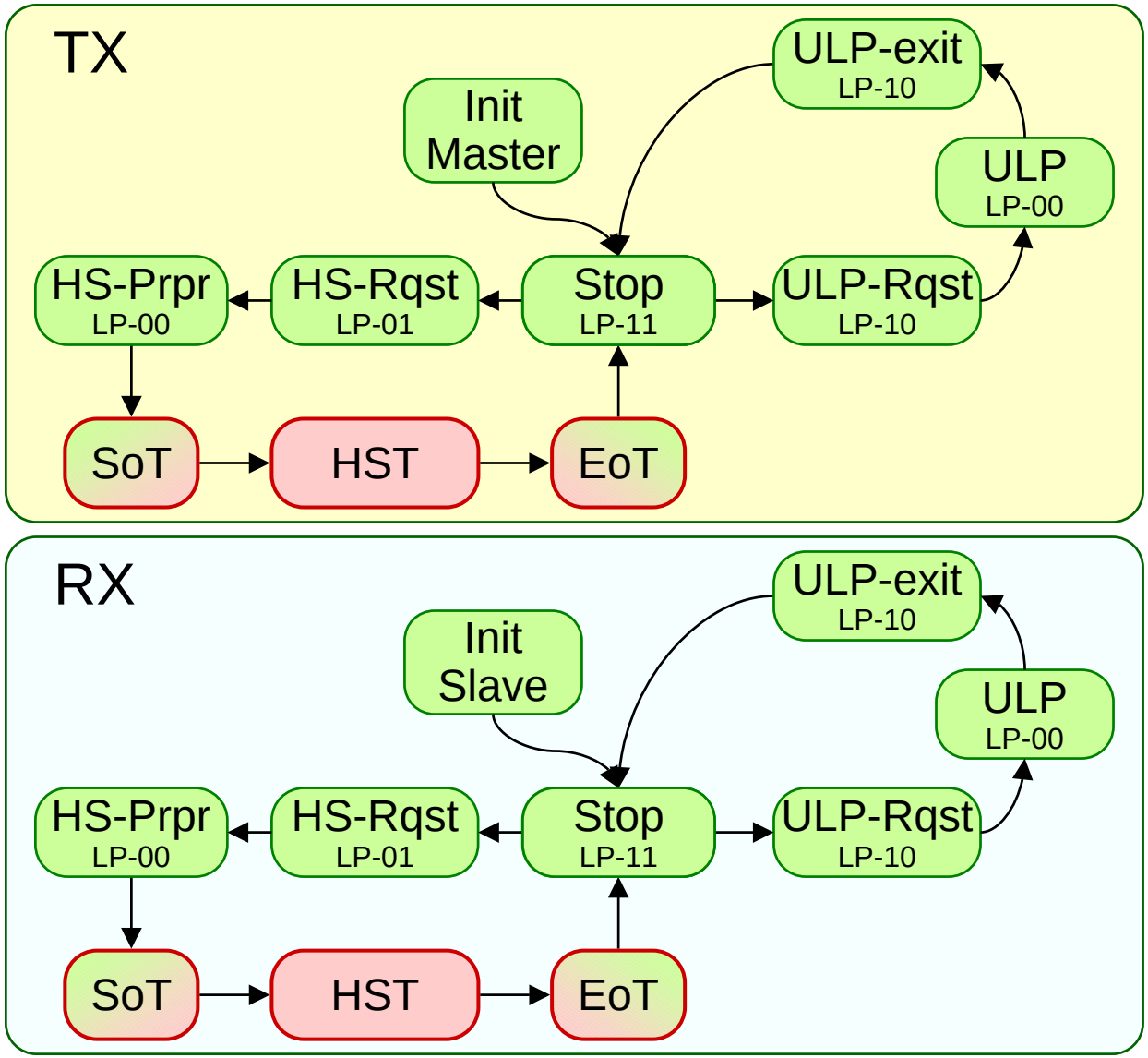


Escape Mode signaling
Two Byte LPDT Example



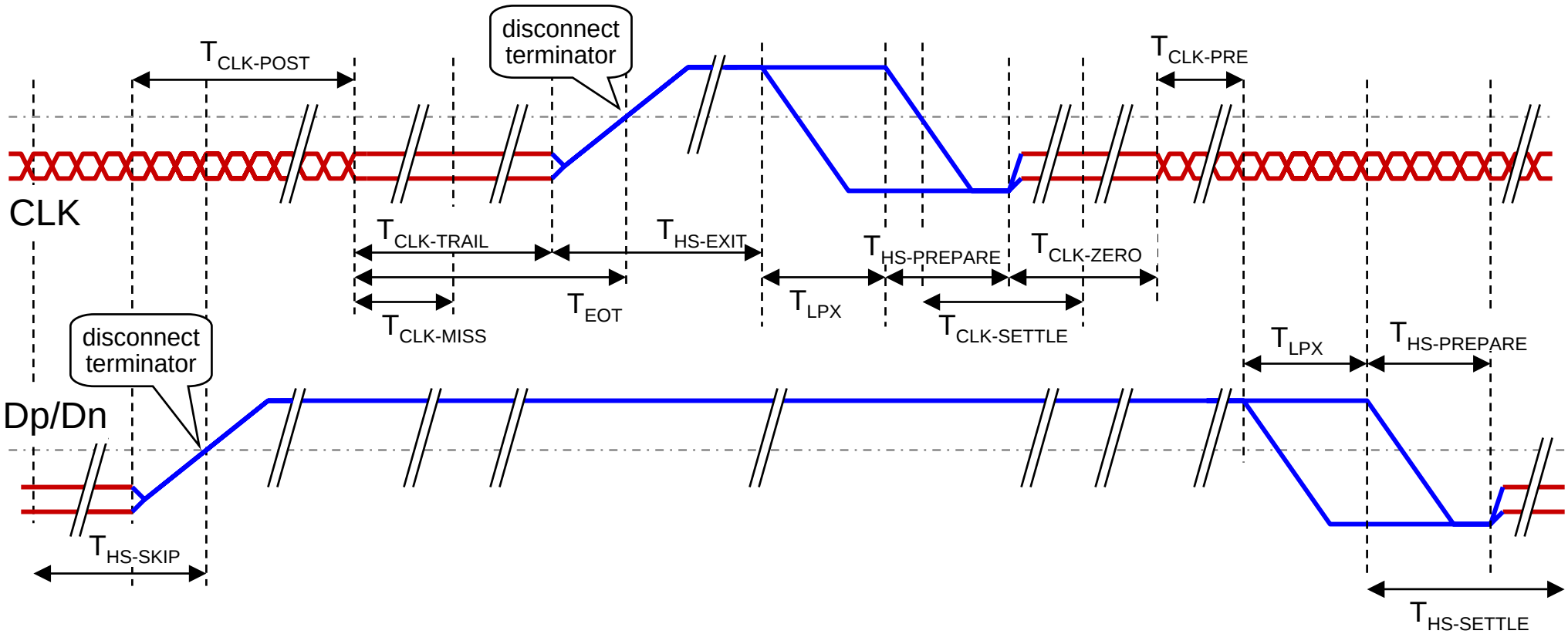


Clock Lane Flow Diagram



- Electrically identical to Unidirectional data lane
- No Escape Mode
- Unidirectional, no Turnaround
- Special short ULP entry (“Sleep mode”)

Clock Lane Low-Power



- Clock must be reliable during HS transmission and mode-switching
- Clock can go to LP only if Data lanes are in LP (and nothing relies on it)
- In Low-Power Data lanes are conceptually asynchronous (independent of the High-Speed Clock)

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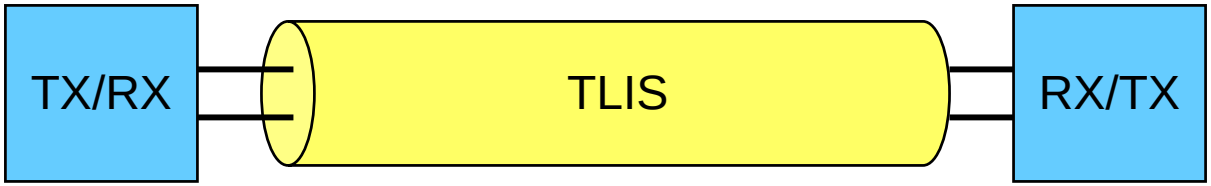
Configuration & Characterization

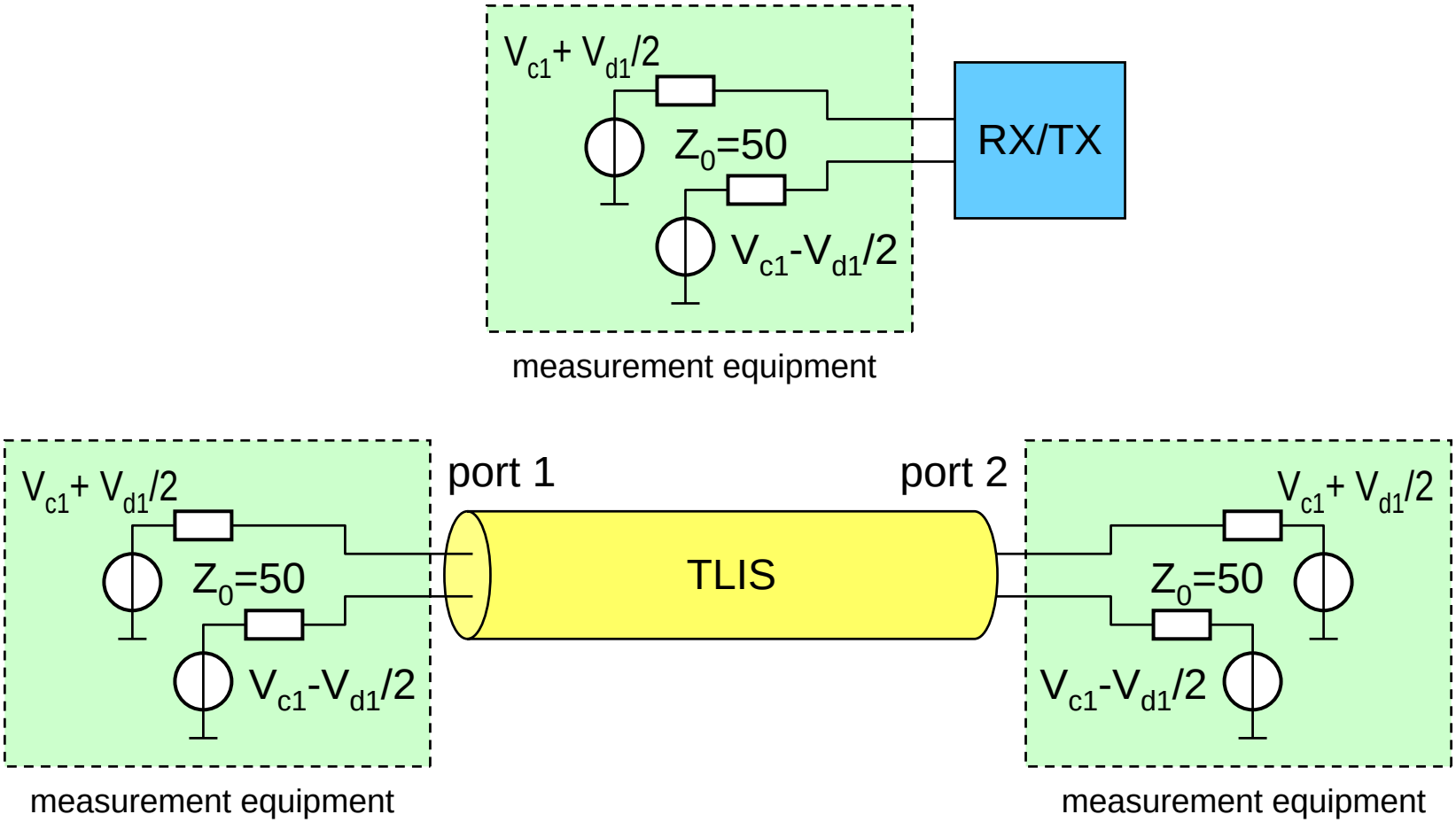


Transmission Line Interconnect Structure

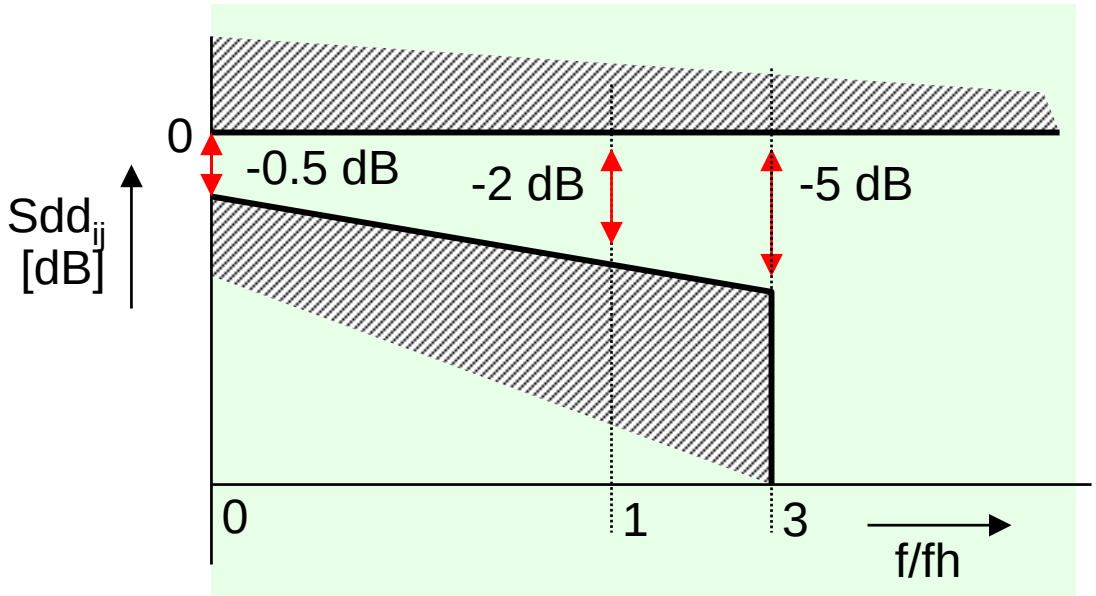
- Split at PHY Modules pins
- Interconnect structure considered as one black box characterized by **S-parameters** over **Frequency**

- **S-parameters**
  - Differential Transfer
  - Differential Reflection
  - Common-mode reflection
  - Mode conversion
- **Frequencies**
  - Low-frequency
  - Fundamental signaling frequency
  - Interference frequencies

Characterization & S-Parameters



Example:
Sdd21 & Sdd12 Interconnect



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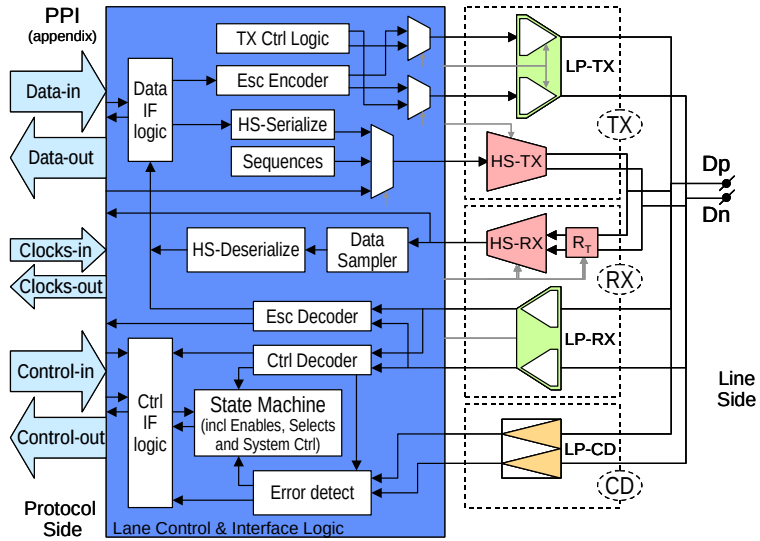
PHY-Protocol Interface (PPI)

- Hides line states and Encodings from Protocol layer
- Byte wide interface
- On-chip interface
  - No sharing of signals
  - No voltage specifications
  - Synchronous interface
- *Informative example* provided in Appendix A
  - Not covered e.g. error behaviour, simultaneous event behaviour
  - Many optional signals regarding optional parts of PHY

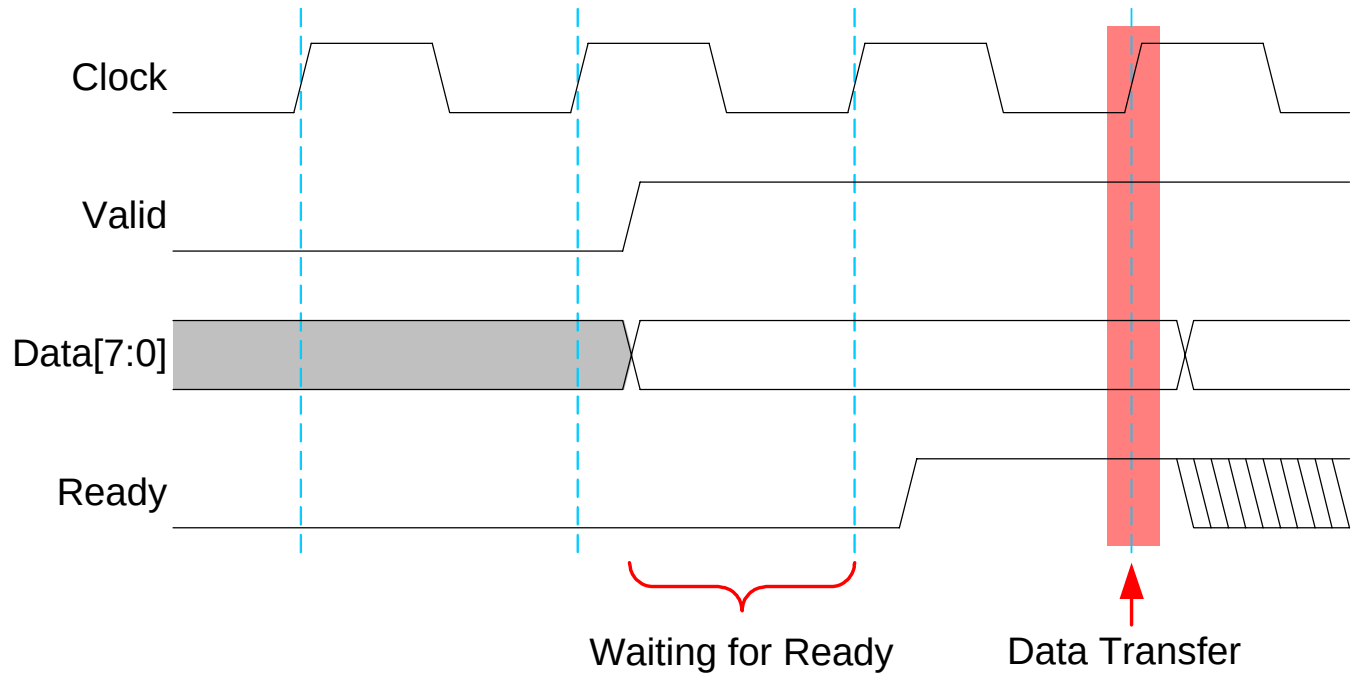


PPI Signals and Clocks

- Almost all signals are synchronous to a clock
  - HS TX Byte Clock
  - HS Receive Byte Clock
  - Esc TX Byte Clock
  - Esc Rec Byte Clock
- No externally supplied clock is assumed on the Slave side for HS transmission in either direction
- High Speed Byte clocks are PHY outputs
- Transmit Escape function requires input clock

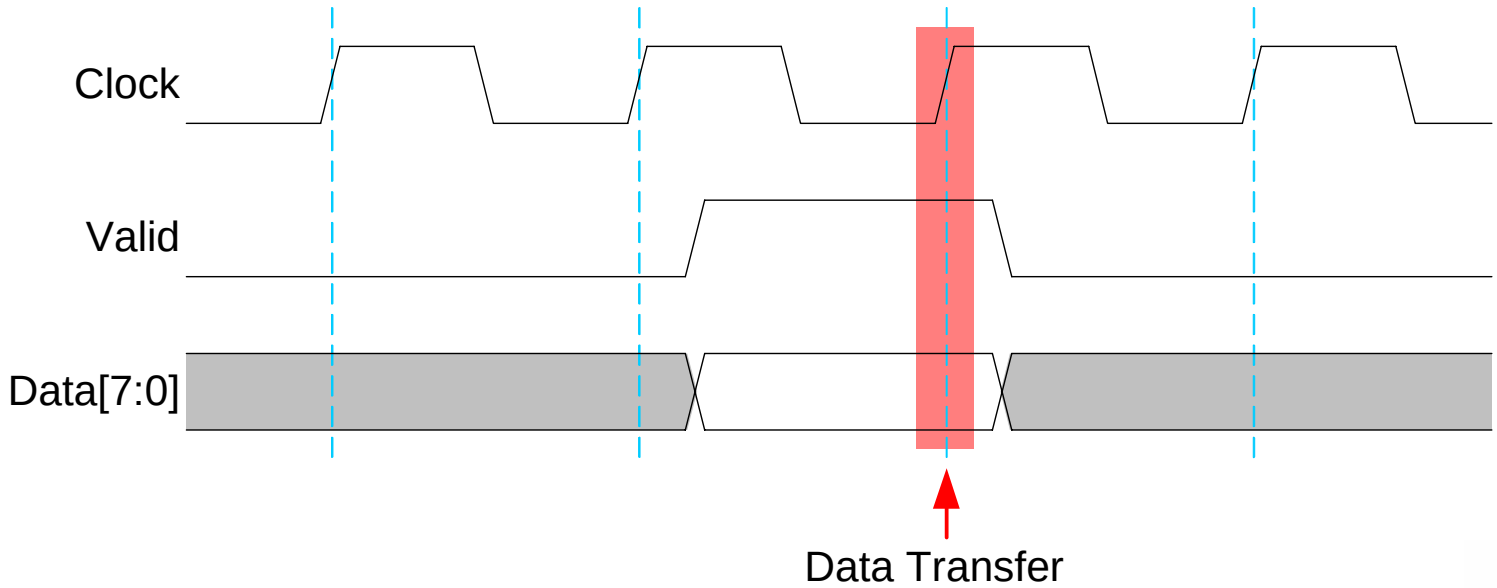
Data Handshaking at Transmit Side

- Ready and Valid (or Request)
  - High-speed request also serves as valid
  - Escape mode uses separate request and valid signal
  - Transfer when both signals are active at a rising clock edge



Data Handshaking at Receive Side

- No “Ready” signal
  - Receive side must always immediately accept the data



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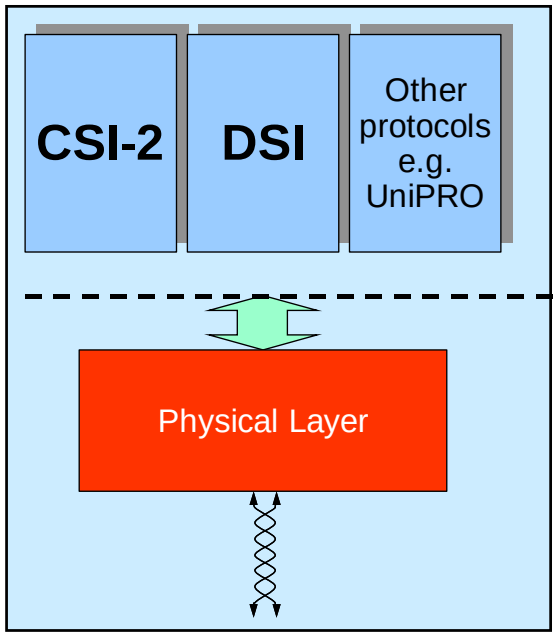

- D- PHY supports:
  - DSI Display Serial Interface
  - CSI2 Camera Serial Interface
  - UniPRO MIPI Universal Protocol

- Meets all of the objectives
  - Scalable bit rate 80-1000 Mb/s
  - Robustness support of ‘bad’ 0-20cm channels
  - Minimal power mW-range for operation, μW-range for standby
  - Easy technology scaling 1.2 Volt signal range
  - Low complexity source-synchronous signalling
  - Low pin count 2 differential pairs
  - Bi-directionality for HS (1/4 forward bit rate) and LP
  - Lane scalability multiple data lanes with a single clock lane

QUESTIONS ?

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IEEE