LXT971A/972A PHY Transceivers

Specification Update

May 2002

Notice: The LXT971A and LXT972A may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 249354-007

Contents

Revision History

Date	Version	Page #	Description
May 17, 2002	007	6	Updated “Affected Documents” Table.
		8	Updated “Codes Used in Summary Table”.
		9	Updated “Errata” Listing.
		14	Added Erratum: “Switching Clocks from 100 Mbps to 10 Mbps Prior to End of Packet”.
		18	Added Addendum: “Increased MII Drive Strength”.
August 17, 2001	006	9	Documentation Changes: Modified to reflect document rev numbers.
		16	Modified Absolute Maximum Ratings table.
June 27, 2001	005	18	Addenda: Clarified Description 1.
June 20, 2001	004	17	Added Product Ordering Information
May 09, 2001	003	9	Errata 7, 9, 10, 11, 12 were fixed in Stepping 2. Removed “Xs” for correct status.
March 20, 2001	002	10	Updated “Markings” table with Manufacturer’s Revision Code information.
		13	Replaced text with “None” for Workaround under Errata 9.
		14	Added BSDL text to Workaround under Errata 11.
January 15, 2001	001	-	Converted to Intel format (no technical or material changes).
August 24, 2000	2.1†	-	Added errata for Stepping 2.
June 27, 2000	2.0†	-	Reformatted and added errata for Stepping 1.
November 5, 1999	1.*n*†	-	Various versions covered silicon Stepping 0.

† Level One document version number. As of January 15, 2001, this document replaces the Level One document.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

As a result of changes, Stepping 2 parts are labeled as LXT971A and LXT972A.

Affected Documents/Related Documents

Title	Order
LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249185
LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249186
LXT971A/972A 3.3V PHY Transceivers Design and Layout Guide Application Note	249016
LXT971A — LXT970A-to-LXT971A Migration Application Note	249028
LXD971B Demo Board for 3.3V 10/100 Applications (Board Rev A1) Development Kit Manual	249246
LXD971L Demo Board for 3.3V 10/100 Applications (Board Rev B2) Development Kit Manual	249247

Nomenclature

Errata are design defects or errors. These may cause the LXT971A and LXT972A Single-Port 10/100 PHY Transceivers' behaviors to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, or specification clarifications which apply to the LXT971A and LXT972A Single-Port 10/100 PHY Transceivers product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in stepping indicated. Specification Change or Specification Clarification does not apply to this stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings†			Page	Status	ERRATA
	0	1	2			
1	X			11	Fixed	"Incorrect Auto-Negotiation Link Partner Base Page Ability Register"
2	X			11	Fixed	"Incorrect Auto-Negotiation Next Page"
3	X			11	Fixed	"Incorrect Remote Fault"
4	X			11	Fixed	"Incorrect Auto-Negotiation Duplex Status"
5	X	X		12	Fixed	"Incorrect JTAG Revision Code"
6	X	X		12	Fixed	"Incorrect Duplex - Collision LED Display"
7	X	X		13	Fixed††	"Incorrect Activity LED Display"
8	X			13	Fixed	"MII Pins Not Tri-Stateable"
9	X	X		13	Fixed††	"100M External Loopback Using Short Cable Length"
10	X	X		14	Fixed††	"10BASE-T Data Inversion"
11	X	X		14	Fixed††	"Power Cycling and JTAG $\overline{\text{TRST}}$ Reset Pin"
12	X	X		14	Fixed††	"Switching Clocks from 100 Mbps to 10 Mbps Prior to End of Packet"

† Refer to "Markings" on page 10 for codes to identify various silicon steppings.

†† As a result of changes, parts for Stepping 2 are labeled as LXT971A and LXT972A.

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

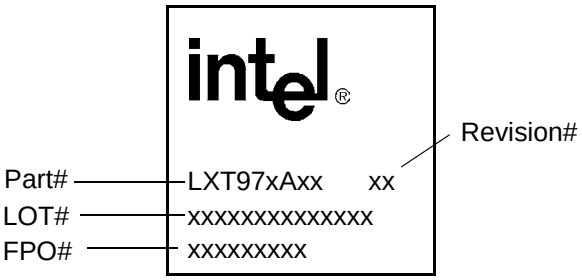
No.	Steppings		Page	Status	SPECIFICATION CLARIFICATIONS
	0	1			
1	X	X	16	Doc	Modified Absolute Maximum Ratings table.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	LXT971A - 001 LXT972A - 002	17	Doc	Added Product Ordering Information.

Identification Information

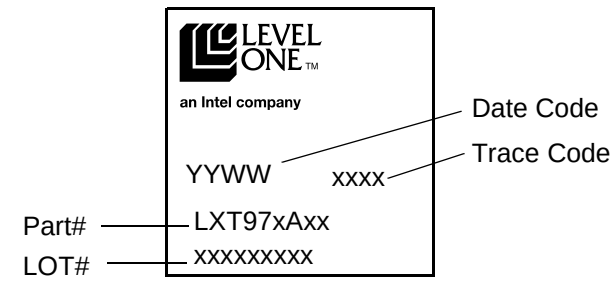
Markings



The silicon stepping in the LXT971A/972A Data Sheet is referred to as "Manufacturer's Revision Number." The silicon stepping number may be read by software from Register 3, bits 3:0 in the LXT971A/972A7 transceivers.

Stepping	Revision Number	Trace Codes[1]	Manufacturer's Revision Number[2]	Notes
0	A1	xxAx	0000	
1	A2	xxBx	0001	
2	A4	xxDx	0010	

1. *x* indicates an insignificant variable.
2. This value is from register bits 3.3:0. Please see the LXT971A/LXT972A data sheets for more information.



Errata

1. Incorrect Auto-Negotiation Link Partner Base Page Ability Register

Problem: Upon completing the parallel detection function, the Auto-Negotiation Link Partner Base Page Ability Register (register 5) should be updated to reflect the link partner's capability. Register 5 is not being updated correctly and always reads 0000h.

Workaround: The Status Register #2 (register 17) is properly updated with the arbitrated link status information and can be used to identify link speed and duplex status.

Status: This erratum has been previously fixed.

2. Incorrect Auto-Negotiation Next Page

Problem: The Auto-Negotiation Next Page state machine functions incorrectly and does not support Next Page operations.

Workaround: Bit 4.15 in the Auto-Negotiation Advertisement Register must be set to 0 (port has no ability to send multiple pages).

Status: This erratum has been previously fixed.

3. Incorrect Remote Fault

Problem: In fiber mode, the Remote Fault bit (1.4) in MII Status Register #1 is used to report receipt of the Far End Fault Indication (FEFI) code to the MAC. Under certain conditions the Remote Fault bit fails to indicate receipt of the FEFI code.

This occurs only when the following conditions are true:

- The device is operating in fiber mode, AND
- The device hardware configuration is set to enable auto-negotiation.

Workaround: Strap the LED/CFG1 pin to ground to disable auto-negotiation.

Status: This erratum has been previously fixed.

4. Incorrect Auto-Negotiation Duplex Status

Problem: The LXT971/972 fails to update the initial control setting for full- or half-duplex operation (bit 0.8) after a link is established. Under certain conditions this can result in incorrect reporting of duplex status and collision events. This problem only occurs under the following conditions:

- The LXT971/972 is initially set for full-duplex operation, AND
- The LXT971/972 establishes a half-duplex link via auto-negotiation or parallel detection

OR

- The LXT971/972 is initially set for half-duplex operation, AND
- The LXT971/972 establishes a full-duplex link via auto-negotiation or parallel detection.

Implication: In the first case (half-duplex link established while control register set for full-duplex), the LXT971/972 will:

- Function as a full-duplex port
- Indicate full-duplex via LED driver and bit 0.8
- Indicate half-duplex via bit 17.9
- Not Indicate collision (via LED driver, MII_COL signal, or bit 17.11) when transmitting and receiving concurrently

In the second case (full-duplex link established while control register is set for half-duplex), the LXT971/972 will:

- Function as a half-duplex port
- Indicate half-duplex via LED driver
- Indicate full-duplex via bit 17.9
- Indicate collision (via LED driver, MII_COL signal, and bit 17.11) when transmitting and receiving concurrently

Workaround: In MDIO Management Interface mode, use Status Register #2 (register 17.9) to update the duplex status in the Control Register. Status Register #2 is updated with the correct duplex status when auto-negotiation is completed. Each time link is established, the duplex status in register 17.9 can be used to update the duplex mode in the Control Register (register 0.8).

Status: This erratum has been previously fixed.

5. Incorrect JTAG Revision Code

Problem: The LXT971/972 (A2) JTAG Device ID is as follows - 0001 03CB 1110 111 1110 1

As per the standard, the Jedec Continuation Character (Bit 11:8) for Level One's devices should have been 0000 instead of 1110.

Implication: Any person performing JTAG operations for boundary scan will receive an incorrect JTAG ID for the Shark device.

Workaround: Use a continuation character of 1110 when addressing an LXT971-Stepping 1 device.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

6. Incorrect Duplex - Collision LED Display

Problem: When the port LED is configured to indicate Duplex and Collision via register 20, the LED does not indicate Collision when transmitting and receiving in a half-duplex link.

Workaround: Configure a separate LED for Collision only, a dedicated LED will properly indicate that a collision is occurring.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

7. Incorrect Activity LED Display

Problem: With Pulse Stretching enabled, Port Activity is indicated with a slow blinking rate on the Activity LED when the port is in full-duplex and the port's transmit and receive traffic has the same packet size and inter-packet gap (IPG) for an extended period of time. Correct indication would be for the Activity LED to remain active when transmitting and receiving continuously.

If either packet size or IPG is altered, the Activity LED resumes normal operation.

Implication: The Activity LED indication will not match the traffic rate at the port. Only the Activity LED behavior is affected. Transmit Status and Receive Status LED functionality are not affected.

The Activity LED operation has no impact on data reliability on the port.

Workaround: Use the following steps for a possible workaround:

1. Use Transmit Status or Receive Status instead of Activity as the LED indication.
2. Logically 'OR' Transmit Status and Receive Status to generate an Activity indicator. This workaround requires external hardware to complete the 'OR' function.
3. Add external pulse stretching via a PLD while disabling on-chip pulse stretching via Register 20 (20.1=0). This workaround requires external hardware and manageability via the MDIO interface. Also, because pulse stretching is global to the device, external logic would need to be added for any LED signal which requires stretching.
4. Display both Transmit Status and Receive Status individually.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

8. MII Pins Not Tri-Stateable

Problem: In the hardware power-down mode, the receive clock MDINT pins do not go into a high-impedance state or are not tri-stated.

Implication: In the hardware power-down mode, the receive clock (RxClk) and the MDINT pins will be continuously driven. The transmit clock will be in a true tri-state condition, however, the device will continue to source a receive clock.

Workaround: None.

Status: Fixed in Stepping 1.

9. 100M External Loopback Using Short Cable Length

Problem: In applications that require a short external looping plug (looping TPFO to TPFI) with cable lengths typically less than 2 feet, a link problem may occur.

Implication: During external loopback operations that require line-loop length less than 2 feet, the LXT971/972 input-receiver reference levels may incorrectly slice the twisted-pair signal, causing a loss of link.

Workaround: None.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

10. 10BASE-T Data Inversion

Problem: If jitter on the twisted-pair data occurs within a certain time window relative internally to the DPLL Reference Clock and remains constant, inverted RxData can occur.

Implication: When the receive twisted-pair data jitters, the LXT971/972 devices may pass errored data to the Reconciliation Sublayer. This errored data would be calculated as CRC errors at the MAC and the RXER signal/bit would be active.

Workaround: None.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A

11. Power Cycling and JTAG $\overline{\text{TRST}}$ Reset Pin

Problem: Power-on cycling may cause the LXT971/972 devices to hang in an unknown state due to the improper reset of some internal JTAG control flip-flops.

Implication: Some internal JTAG flip-flops may not be reset properly, which can cause the input and output steering muxes to be selected incorrectly. This incorrect selection may disable any of the digital, MII signal outputs and inputs.

Workaround: Designs not currently using JTAG should tie the $\overline{\text{TRST}}$ pin directly to GND.

Designs using the 5-signal option should tie the $\overline{\text{TRST}}$ pin to GND through a resistor. Suggested value for this resistor is 20 kΩ. A 20 kΩ resistor to GND is strong enough to pull down the internal, weak pull up to a logic 0 for normal operation. This pull down will also allow a JTAG tap controller to operate successfully and overcome the pull-up and pull-down resistors.

Designs using the 4-signal option and not using the $\overline{\text{TRST}}$ pin for reset should use a 20 kΩ pull-down resistor from $\overline{\text{TRST}}$ to GND and control the JTAG $\overline{\text{TRST}}$ pin accordingly.

Designs using the LXT971A or LXT972A will require a new BSDL file that may be found on the Intel website (www.intel.com).

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

12. Switching Clocks from 100 Mbps to 10 Mbps Prior to End of Packet

Problem: Switching clocks from 100 Mbps to 10 Mbps prior to the end of packet, as the PLL transitions to its reset state, can cause the output to become random and unknown, and result in the corruption of the last nibble of the CRC in the receive packet.

Implication: A CRC error occurs randomly on a small percentage of devices and can result in an error rate up to 10 ppm.

Workaround: None.

Status: This erratum has been previously fixed.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

Specification Changes

There are no specification changes.

Specification Clarifications

This table will replace the Absolute Maximum Ratings table in a future version of the LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet.

Table 1. Absolute Maximum Ratings

Parameter		Sym	Min	Max	Units
Supply voltage		VCC	-0.3	4.0	V
Operating temperature	LXT971A_C (Commercial)	TOPA	-15	+85	ºC
	LXT971A_E (Extended)	TOPA	-55	+100	ºC
Storage temperature		TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

This table will replace the Absolute Maximum Ratings table in a future version of the LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet.

Table 2. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply voltage	VCC	-0.3	4.0	V
Operating temperature	TOPA	-15	+85	ºC
Storage temperature	TST	-65	+150	ºC

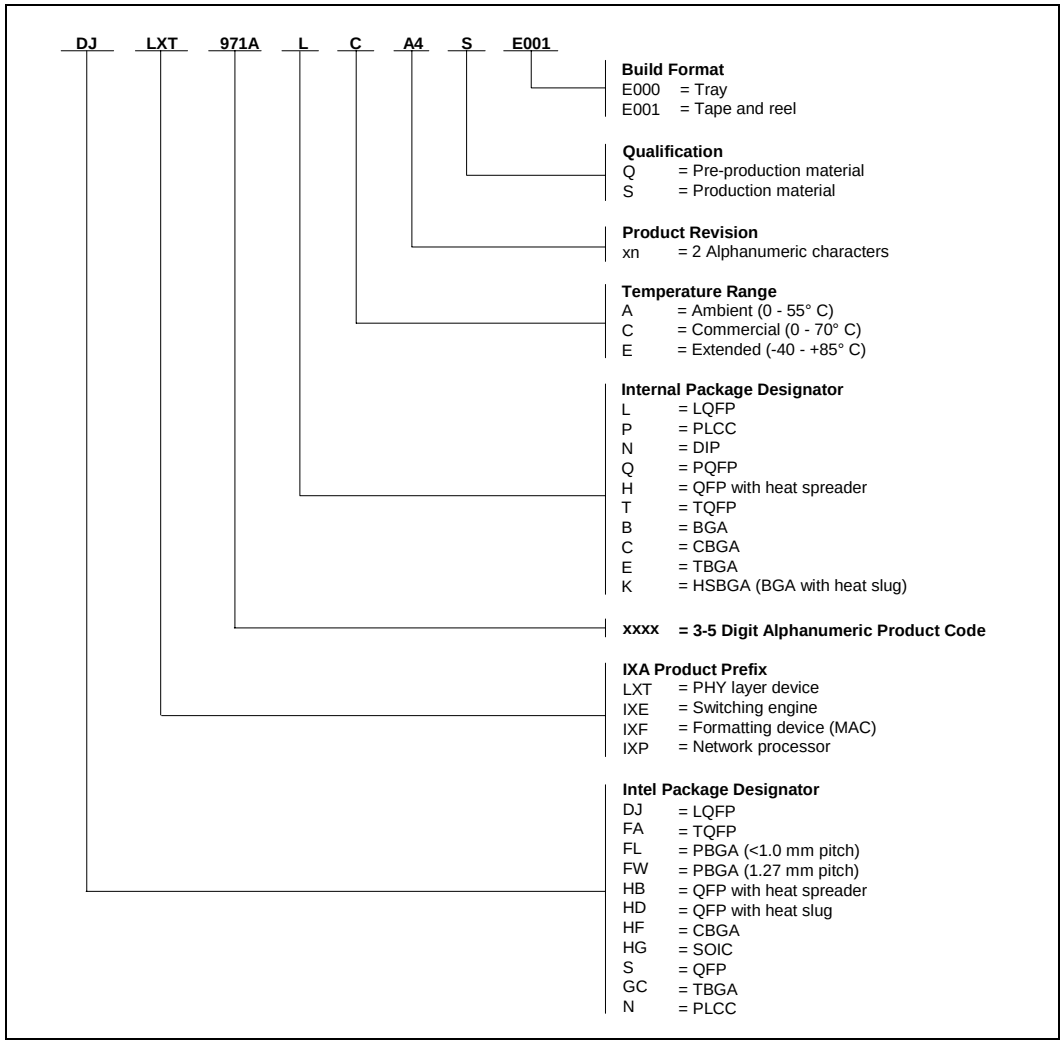
Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Documentation Changes

Table 3. Product Information

Number	Revision	Qualification	Tray MM	Tape & Reel MM
DJLXT971ALC.A4	A4	S	834105	834916
DJLXT971ALE.A4	A4	S	835676	835791
FLLXT971ABC.A4	A4	S	834103	834926
FLLXT971ABE.A4	A4	S	834104	835080
DJLXT972ALC.A4	A4	S	834109	834917

Figure 1. Ordering Information - Sample



Addenda

1. 100BASE-TX Receive Jitter Tolerance

Description: If a receive-link partner operating in 100BASE-TX generates transmit jitter greater than the IEEE standard, the LXT971/972 device may produce errors within the Reconciliation Sublayer, which can result in failure to link or to sustain link. The LXT971/972 devices will be enhanced to allow greater margin to the IEEE standard. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in Stepping 2.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

2. 10BASE-T Jitter Tolerance

Description: In some 10BASE-T input jitter applications, the LXT971/972 device margin may be close to the IEEE standard for input jitter tolerance. The LXT971/972 devices will be enhanced to be optimally centered for 10BASE-T input jitter tolerance. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in Stepping 2.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.

3. Increased MII Drive Strength

Description: A higher Media Independent Interface (MII) drive strength may be desired in some designs to drive signals over longer PCB trace lengths, over high-capacitive loads, through multiple vias, or through a connector. By setting Register 26.11 through software control, the board designer can increase the MII drive strength in the LXT971A/972A. Setting register bit 26.11 to 1 through the MDC/MDIO interface sets the MII pins (RXD[0:3], RX_DV, RX_CLK, RX_ER, COL, CRS, and TX_CLK) to a higher drive strength.

Status: Implemented in Stepping 2.

Note: Parts for Stepping 2 are labeled as LXT971A and LXT972A.