Semiconductors

I²C Logic Selection Guide

Advanced I²C Devices: Innovation in a Mature Technology

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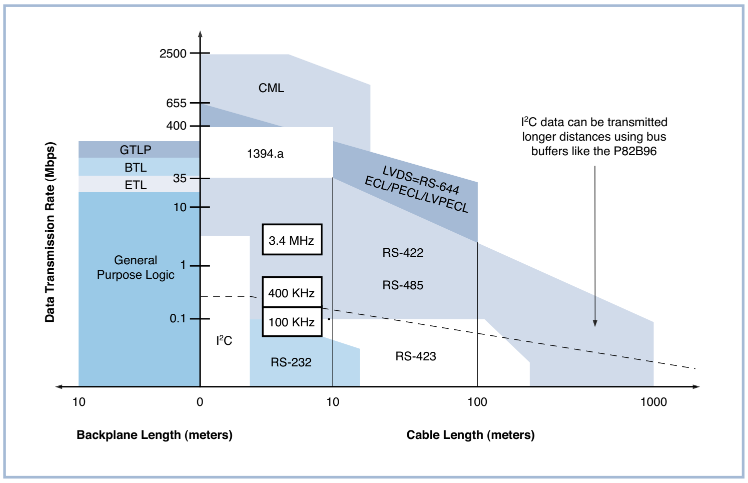
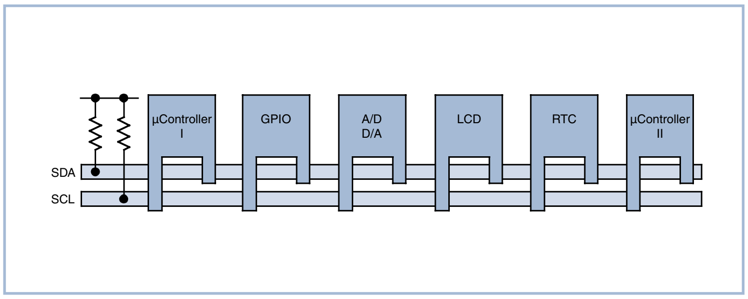
I²C: Mature Technology for Today's Complex Systems

I²C benefits:
- De facto world standard
- Fast time-to-market
- Proven, robust performance
- Very wide range of functions
- Easy to design in
- Simple to debug
- Fast to test and assemble
- Reduces overall cost

Transmission Standards



I²C-bus Structure



The Inter-IC bus, commonly known as the I²C ("eye-squared-see") bus, is a control bus that provides the communications link between integrated circuits in a system. Developed by Philips in the early 1980s, this simple two-wire bus with a software-defined protocol has evolved to become the de facto worldwide standard for system control, finding its way into everything from temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters, CODECs, and microprocessors of all kinds.

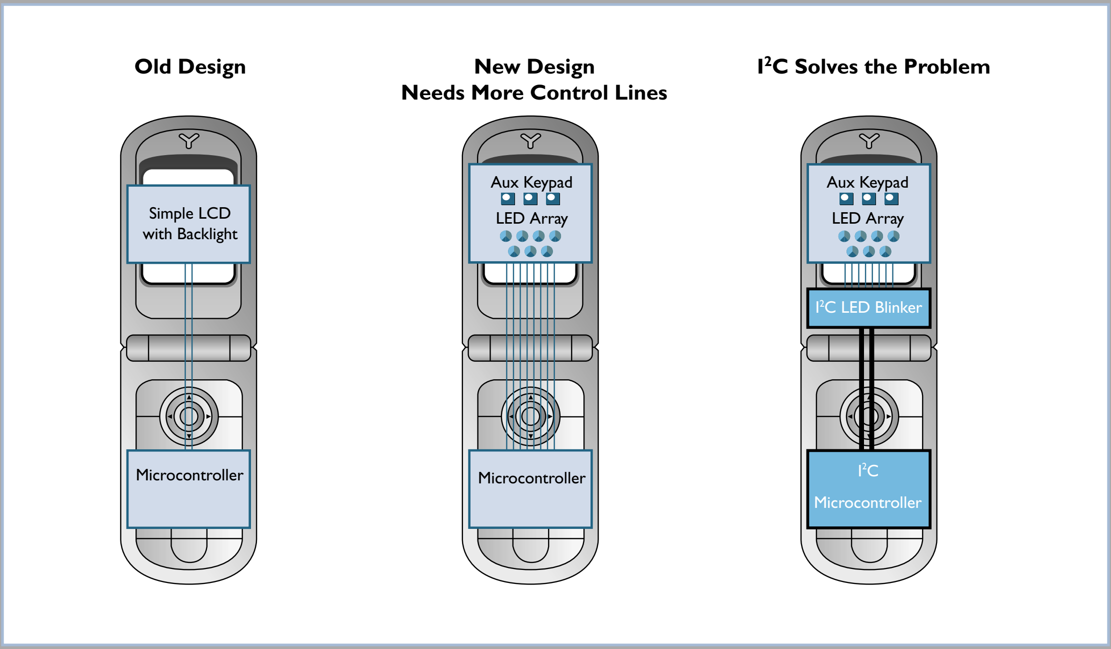
There are several reasons why the I²C-bus has endured for more than 20 years. To begin, the bus has kept pace with performance and today provides three levels of data rate transfer: up to 100 kbps in Standard mode, up to 400 kbps in Fast mode, and up to 3.4 Mbps in High-Speed mode. Recently introduced hubs, bus repeaters, bidirectional switches, and multiplexers have increased the number of devices the bus can support, extending bus capacitance well beyond its original maximum of 400 pF. Also, software-controlled collision detection and arbitration prevent data corruption and ensure reliable performance, even in complex systems.

Beyond performance, though, there is ease of use. Two simple lines connect all the ICs in a system. Any I²C device can be attached to a common I²C-bus, and any master device can exchange information with any slave device. The software-controlled addressing scheme eliminates the need for address-decoding hardware, and there's no need to design and debug external control logic because it's already provided by the I²C protocol. Designers can move quickly from block diagram to final hardware, simply clipping new devices and functions to an existing bus.

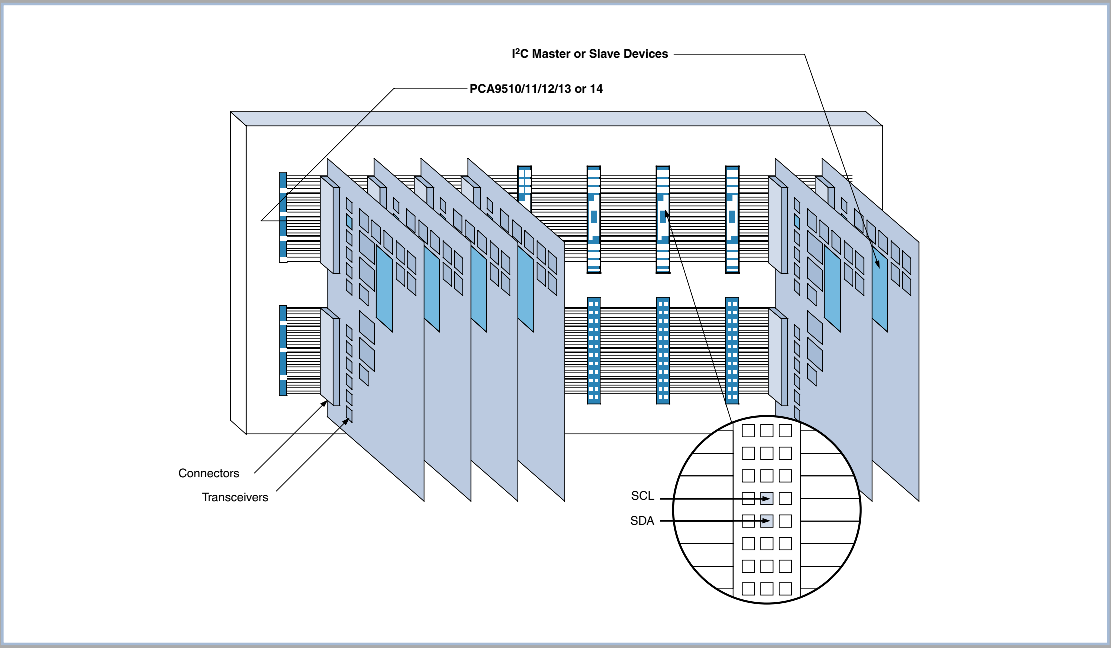
The I²C-bus also saves space and lowers overall cost. The two-line structure means fewer trace lines, so the PCB can be much smaller. Debug and test are easier, too, since there are fewer trace lines and fewer information sources to verify. As the system evolves over several generations, I²C devices can easily be added or removed without impacting the rest of the system.

Innovative Products for Better Designs

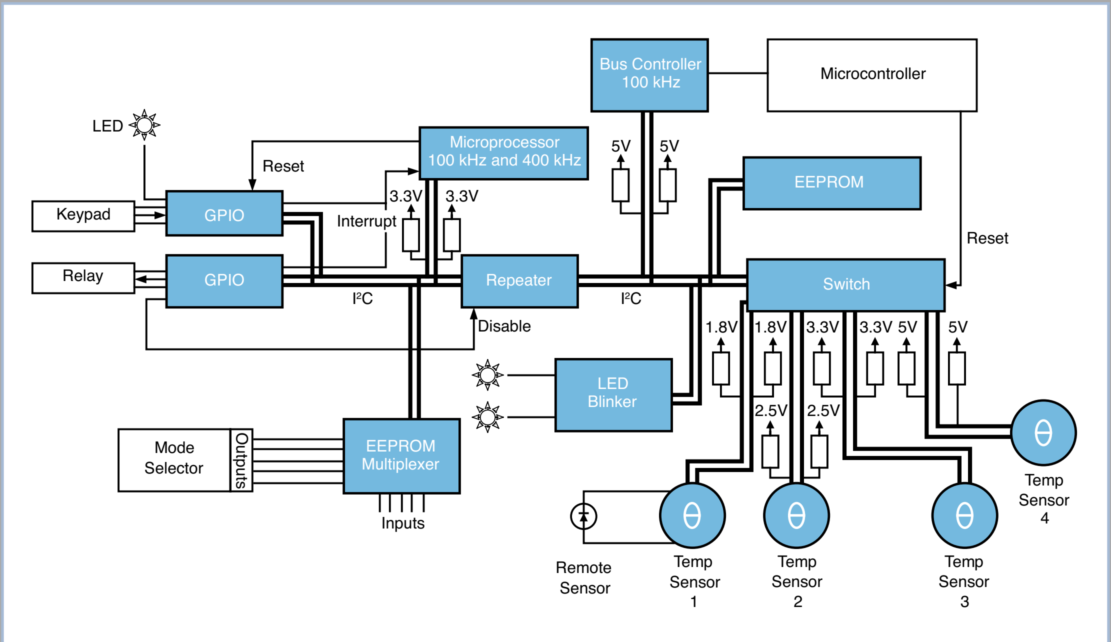
Portable Device Applications



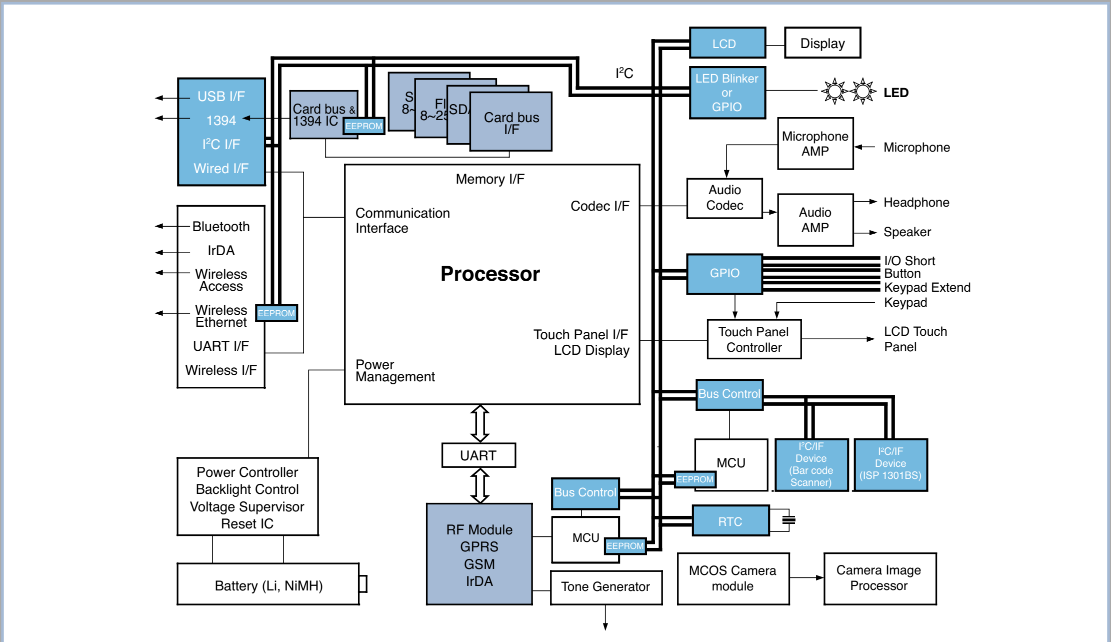
Hot Swap Applications Including cPCI, VME, and Advanced TCA



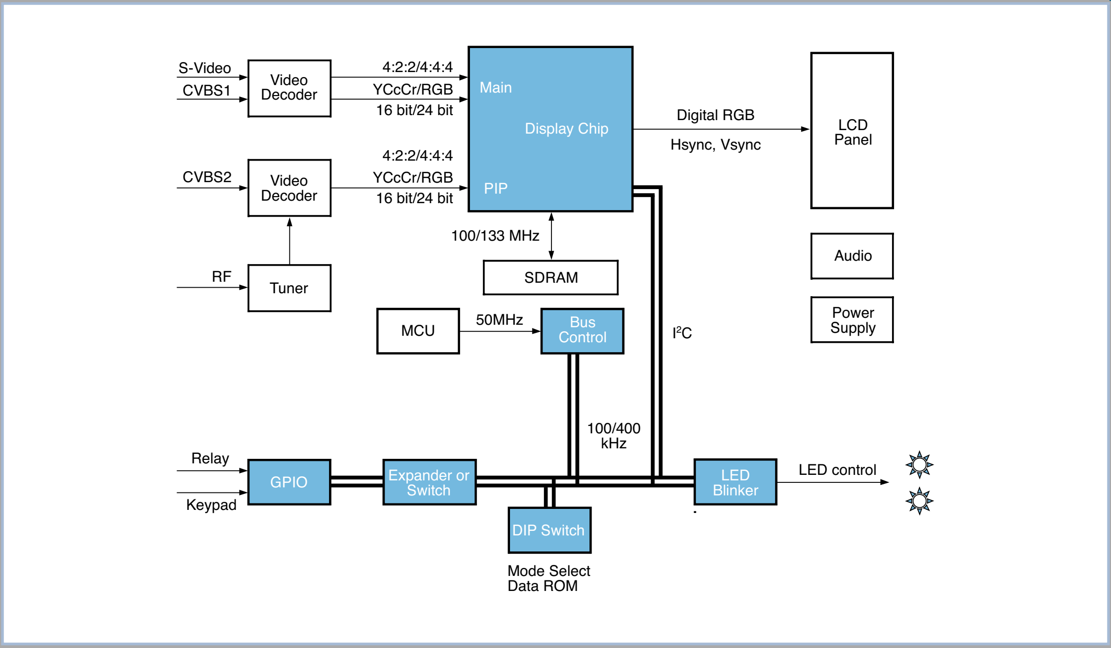
General-purpose Applications



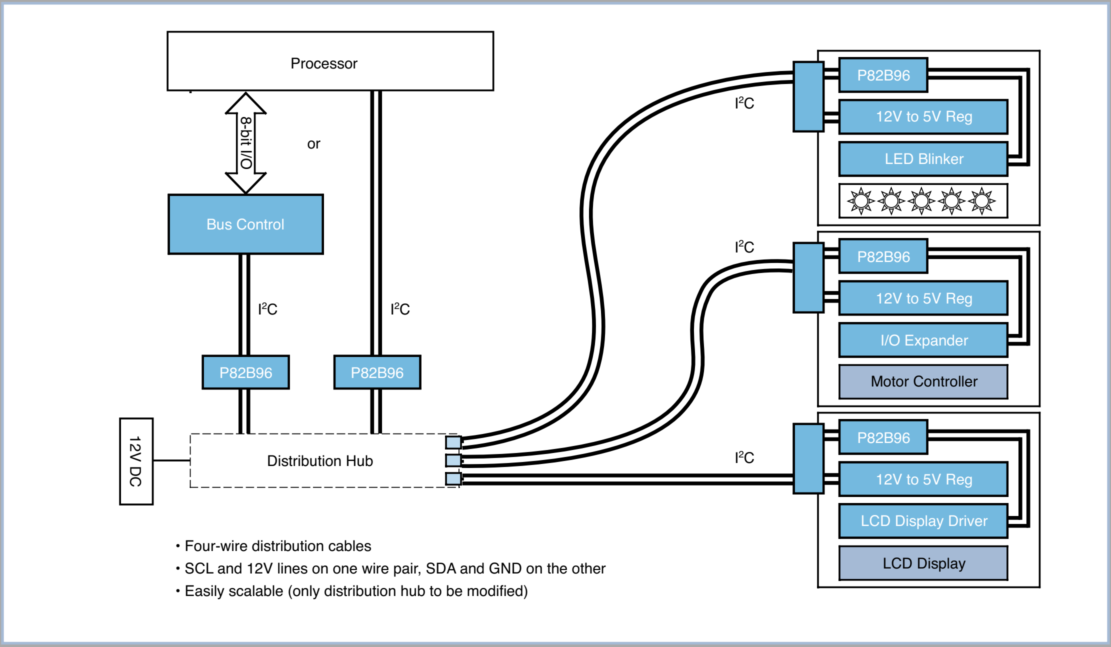
PDA and Smartphone Applications



LCD TV Applications

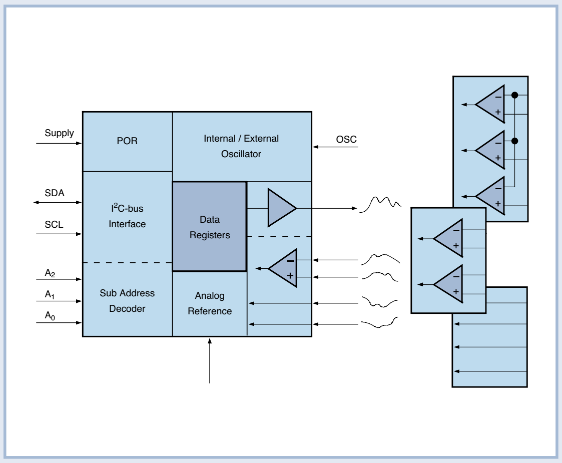


Modular Applications, Medical, Gaming



- Four-wire distribution cables
- SCL and 12V lines on one wire pair, SDA and GND on the other
- Easily scalable (only distribution hub to be modified)

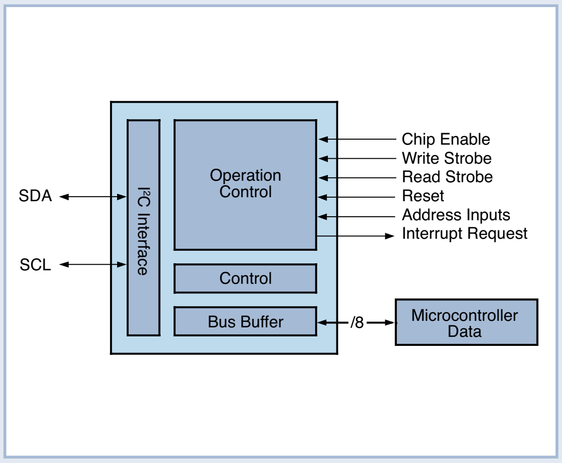
I²C Product Families



I²C Analog-to-Digital Converter

- Converts signals from digital to analog, analog to digital
- Four-channel A/D converter
- One-channel D/A converter
- Internal oscillator
- Power On Reset (POR)

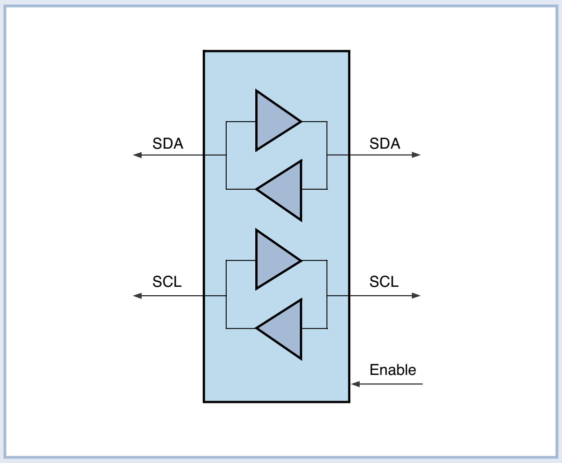
PCF8591	100-kHz 4-channel 8-bit A/D and D/A Converter



Parallel-Bus-to-I²C-bus Controllers

- Interfaces most 8-bit parallel-bus microcontrollers and microprocessors to I²C-bus
- Parallel bus system communicates bi-directionally with I²C-bus
- Provides master and slave functions
- I²C-bus communications carried out on byte-wise basis, using interrupt or polled handshake
- Controls all I²C-bus-specific sequences (protocol, arbitration, timing)
- Internal oscillator (PCA9564)
- Multi-master capable

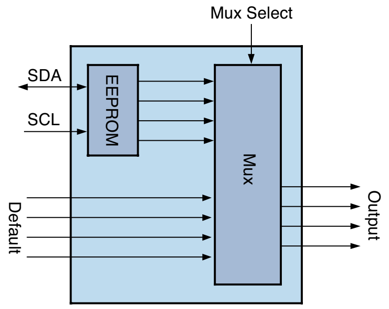
PCA9564	400-kHz 2.3-to-3.6-V I²C-bus Controller
PCA8584	100-kHz 4.5-to-5.5-V I²C-bus Controller



I²C-bus Repeaters, Hubs, and Extenders

- Bi-directional I²C drivers isolate I²C-bus capacitance, accommodating more I²C devices and longer bus length
- Up to 400-pF load on each segment
- Different voltages (3.3 or 5 V) on each segment
- Devices transparent to bus arbitration and contention protocols in multi-master environment
- Twisted pair differential transmission or opto-electrical isolation of I²C-bus (P82B96)

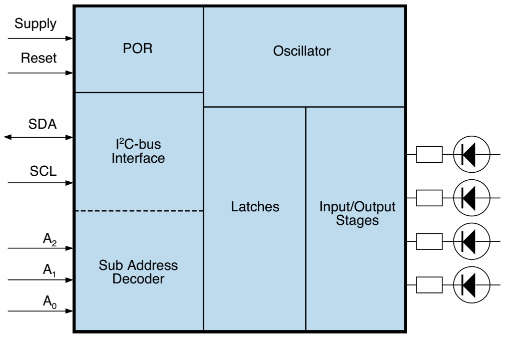
PCA9510/11/12/13/14	I²C Hot Swap Bus Buffers
PCA9515/15A	I²C-bus Repeater
PCA9517	Low-voltage I²C-bus Repeater
PCA9516/16A	5-channel I²C Hub
PCA9518	Expandable 5-channel I²C Hub
P82B96	Dual Bi-directional I²C-bus Buffer
P82B715	I²C-bus Extender



I^{2}C EEPROM-based DIP Switches

- Replace jumpers and DIP switches
- Hands-free manipulation via integrated, I^{2}C-controlled EEPROM and multiplexer
- Program and store settings in I^{2}C-controlled EEPROM register
- Multiplex between default values and stored settings
- Non-volatile memory retains register values, even on power-down

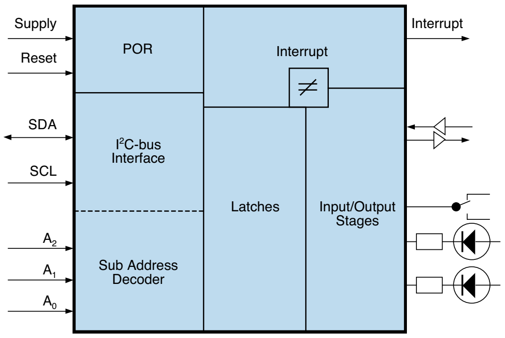
PCA8550	4-bit Multiplexed / 1-bit Latched 5-bit I^{2}C EEPROM
PCA9559	5-bit Multiplexed / 1-bit Latched 6-bit I^{2}C EEPROM
PCA9560	Dual 5-bit Multiplexed / 1-bit Latched I^{2}C EEPROM
PCA9561	Quad 6-bit Multiplexed I^{2}C EEPROM



I^{2}C LED Dimmers/Blinkers

- General-purpose I/O and LED control
- No external components required: internal oscillator provides two (256-step, user-definable) frequency and duty cycles
- Two programmable blink rates
- Single-transmission control of LED on/off/blink
- LED brightness controlled by setting frequency to 152 Hz and changing duty cycle to vary LED's average current
- Extra pins can be used as inputs or outputs
- Hardware reset pin for state machine
- 25-mA, high-current open drain outputs

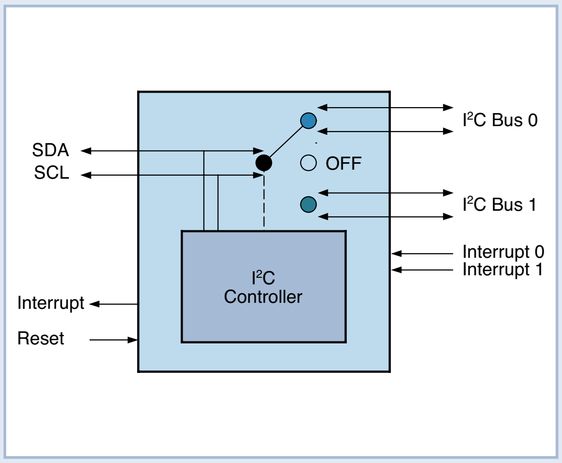
LED Dimmers (Freq. Range: 152 Hz to 1.69 sec.)		LED Blinkers (Freq. Range: 44 Hz to 5.82 sec.)	
PCA9530	2-bit I^{2}C / SMBus LED Dimmer	PCA9550	2-bit I^{2}C / SMBus LED Blinker
PCA9533	4-bit I^{2}C / SMBus LED Dimmer	PCA9553	4-bit I^{2}C / SMBus LED Blinker
PCA9531	8-bit I^{2}C / SMBus LED Dimmer	PCA9551	8-bit I^{2}C / SMBus LED Blinker
PCA9532	16-bit I^{2}C / SMBus LED Dimmer	PCA9552	16-bit I^{2}C / SMBus LED Blinker



I^{2}C General-purpose I/O (GPIO) Expanders

- Extend GPIO from I^{2}C or SMBus
- Connect parallel I/O to serial I^{2}C or SMBus and provide I/O expansion
- Quasi output: upper transistor is on for half a clock cycle and then held up by a weak current source (25-mA sink)
- True Output: configurable as input or output with polarity inversion (push/pull with 25-mA sink and 10-mA source)

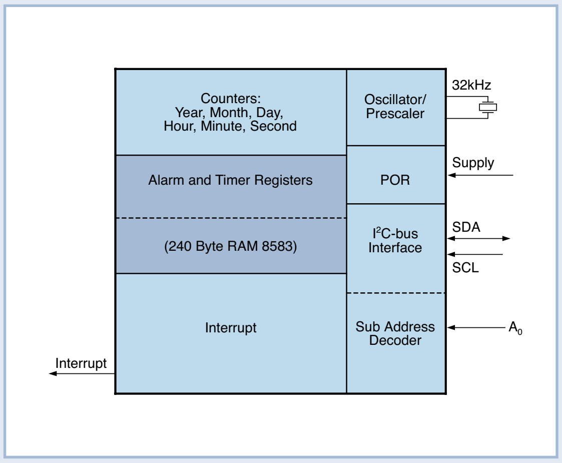
Quasi Output (Weak Current Source)		True Output (Configurable Push/Pull)	
PCA9500	8-bit with 2-kbit EEPROM	PCA9536	4-bit with Interrupt
PCA9501	8-bit with 2-kbit EEPROM, Interrupt	PCA9537	4-bit with Interrupt, Reset
PCA9558	8-bit w/ 5-bit DIP, 2-kbit EEPROM	PCA9538	8-bit with Interrupt, Reset
PCF8574/74A	8-bit with Interrupt	PCA9539	16-bit with Interrupt, Reset
PCF8575/75C	16-bit with Interrupt	PCA9534/54/54A	8-bit with Interrupt
		PCA9535/55	16-bit with Interrupt
		PCA9557	8-bit with Reset



I^{2}C Multiplexers and Switches

- Fans I^{2}C-bus out to multiple I^{2}C-buses
- Buses selected via I^{2}C commands from master
- Multiplexers and switches select one downstream I^{2}C-bus at a time
- Switches can, in broadcast mode, turn on all channels simultaneously
- Interrupts are collected and sent to master
- Reset pin deselects all channels, so master can regain control if bus hangs up
- Designed for address conflict resolution, I^{2}C sub-branch isolation, I^{2}C-bus level shifting, etc.

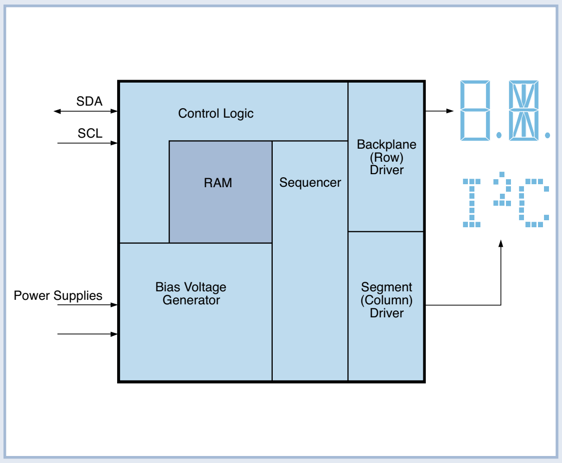
PCA9540B	1-to-2 Multiplexer	PCA9545A	1-to-4 Switch w/ Interrupt, Reset
PCA9541	2-to-1 Master Select w/ Int, Reset	PCA9546A	1-to-8 Switch with Reset
PCA9542A	1-to-2 Multiplexer with Interrupt	PCA9547	1-to-8 Multiplexer with Reset
PCA9543A	1-to-2 Switch w/ Interrupt, Reset	PCA9548A	1-to-8 Switch with Reset
PCA9544A	1-to-4 Multiplexer w/ Interrupt	PCA9549	8-bit Bus Switch with Reset



I^{2}C Real-time Clocks

- 32.768-kHz quartz oscillator
- Year, month, day, hour, minute, second (1/100-sec resolution)
- Alarm and timer functions
- Wide operating supply voltage range (1.0 to 5.5 V)
- Open drain interrupt pin
- Low back-up current (0.25 µA at 3 V)
- Low-voltage detection

PCF8563	Low-power I^{2}C Real-time Clock
PCA8565	High-temperature (125 °C) I^{2}C Real-time Clock
PCF8583	I^{2}C Real-time Clock with 240-Byte RAM
PCF8593	I^{2}C Real-time Clock with 1/100-second Resolution



I^{2}C LCD Segment Drivers

- Low power
- On-chip bias
- Temperature compensation
- Blinking
- No external parts required

PCF8562	32-to-128 I^{2}C LCD Segment Driver
PCF8566	24-to-96 I^{2}C LCD Segment Driver
PCF8577C	32-to-64 I^{2}C LCD Segment Driver
PCF8576(C, D)	40-to-160 I^{2}C LCD Segment Driver
PCF8578/79	>384 I^{2}C LCD Segment / Dot Driver
PCF2113/2119	I^{2}C LCD Character Display
PCF88xx	I^{2}C Color LCD Segment Drivers (consult Internet for full listing)
SAA1064	4 x 7 I^{2}C LED Segment Driver with Decimal

I²C Product Families

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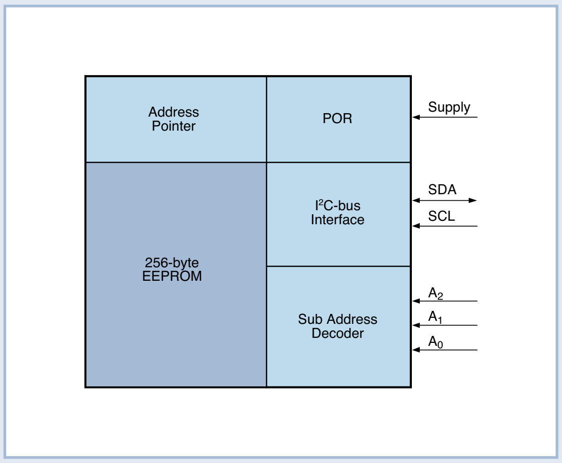
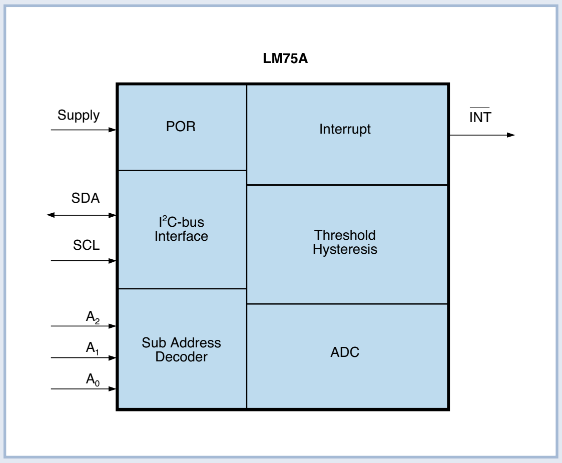


I²C Serial EEPROMs

- Wide voltage range minimizes EEPROM inventory
- I²C-bus reads/writes information to/from memory
- Wide voltage range (2.5 to 5.5 V)
- 1,000,000 read/write cycles
- 10-year data retention

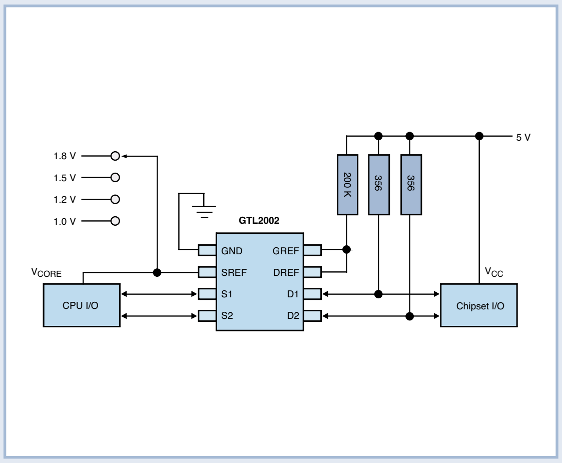
PCA24S08	1024 x 8-bit (8-kbit) I²C Serial EEPROM with Security Features
PCF8570	256 x 8-bit (2-kbit) I²C Static Low-voltage RAM
PCF8581(C)	128 x 8-bit (1-kbit) I²C Serial EEPROM
PCF8582C-2	256 x 8-bit (2-kbit) I²C Serial EEPROM
PCF8594C-2	512 x 8-bit (4-kbit) I²C Serial EEPROM
PCF8598C-2	1024 x 8-bit (8-kbit) I²C Serial EEPROM
PCF85102C-2	256 x 8-bit (2-kbit) I²C Serial EEPROM
PCF85103C-2	256 x 8-bit (2-kbit) I²C Serial EEPROM with Alternate I²C Address
PCF85116-3	2048 x 8-bit (16-kbit) I²C Serial EEPROM



I²C Temperature and Voltage Sensors

- Hardware monitors use I²C-bus to report temperature and/or voltage
- Remote sensor is more accurate than package-mounted sensors (analog input pins let external transistors and diodes – in a processor, for example – perform very precise temperature sensing)

NE1617A	±2 °C Local / Remote I²C Temperature Monitor
NE1618	±1 °C High-accuracy Local / Remote I²C Temperature Monitor
NE1619	±2 °C Local / Remote I²C Temperature and Voltage Monitor
SA56004X	±1 °C Local / Remote Digital Temp Sensor with Over-temp Alarms
LM75A	±2 °C Digital I²C Temperature Sensor and Thermal Watchdog™
SE95	±1 °C Digital I²C Temperature Sensor and Thermal Watchdog



I²C Voltage Level Translators

- Voltage translation between any voltage from 1.0 to 5.0 V
- Open drain on both sides with no drive
- Bi-directional voltage translation with no direction pin
- Reference voltage clamps input voltage with low propagation delay
- Supports bi-directional translation of normal 3.3- and/or 5.0-V I²C-bus signals to low-voltage I²C processor ports
- BiCMOS process for excellent ESD performance

GTL2000	22-bit Bi-directional I²C Voltage Level Translator
GTL2002	2-bit Bi-directional I²C Voltage Level Translator
GTL2010	10-bit Bi-directional I²C Voltage Level Translator

I^{2}C Product Summary

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Type of Function in Device | Features

Data sheets can be downloaded at www.philips.com/i2clogic or www.philips.com/i2c																	Vcc Range (V)						Freq (kHz)		Temp (°C)			Packages							
	I/O Expander (bits)	LED Blinker (bits)	MUX / Latch / EEPROM (bits-latched bits-registers)	MUX / Switch (In/Out channels)	Repeater Hub (In/Out segments)	Bus Controller	Temperature Sensor	Voltage Measurement	RAM / EEPROM (kbits)	Real Time Clock / Calender	Analog / Digital Converter	LCD Driver (segments)	Number of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit / total mA)	1.0	1.8	2.5	3.3	5	5V Tolerant	100	400	0 to 70	-40 to 85	-55 to 125	Pin Count	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
LM75A							2°C						8	0-1					2.8	●	●	●	●	●			●	8		D				DP	
NE1617A							2°C						9	0-1						●	●	●	●		0 to 125			16					DS		
NE1618							1°C						9	0-1						●		●	●		0 to 125			16					DS		
NE1619							2°C	●					2							●	●	●	●	●	0 to 125			16					DS		
P82B715					1-1								NA								●	●	●	●		●		8	PN	TD					
P82B96					1-1								NA						●	●	●	●	●	●		●		8	PN	TD				DP	
PCA8550			4-1-1										1							●		●	●	●	●			16		D		DB		PW	
PCA8565										●			1	0-1			●	●	●	●	●	●	●	●	-40 to 125			8						DP	
PCA8581C									1				8						●	●	●	●	●		-25 to 85			8	PN	TD					
PCA9500	8								2				2-8			25-100				●		●	●	●		●		16			D			PW	BS
PCA9501	8								2				2-64	0-1		25-100				●		●	●	●		●		20			D			PW	BS
PCA9510/11/12/13/14					1-1								NA							●	●	●	●	●		●		8		D				DP	
PCA9515/15A/17					1-1								NA						●	●		●	●	●		●		8		D				DP	
PCA9516/16A					1- 4								NA						●	●		●	●	●		●		16		D				DP	
PCA9518					1-4								NA							●		●	●	●		●		20			D			PW	
PCA9536	4												1			25-50			●	●	●	●	●	●		●		8		D				DP	
PCA9537	4												1	0-1	●	25-50			●	●	●	●	●	●		●		10						DP	
PCA9538	8												4	0-1	●	25-100			●	●	●	●	●	●		●		16		D				PW	
PCA9539	16												4	0-1	●	25-200			●	●	●	●	●	●		●		24			D			PW	
PCA9540B				1-2									1						●	●	●	●	●	●		●		8		D				DP	
PCA9541				2-1									16	1-2	●				●	●	●	●	●	●		●		16		D				PW	BS
PCA9542A				1-2									8	2-1					●	●	●	●	●	●		●		14		D				PW	
PCA9543A				1-2									4	2-1	●				●	●	●	●	●	●		●		14		D				PW	
PCA9544A				1-4									8	4-1					●	●	●	●	●	●		●		20			D			PW	BS
PCA9545A				1-4									4	4-1	●				●	●	●	●	●	●		●		20			D			PW	BS
PCA9546A				1-4									8		●				●	●	●	●	●	●		●		16		D				PW	BS
PCA9547/48A/49				1-8									8		●				●	●	●	●	●	●		●		24			D			PW	BS
PCA9530/50		2											2		●	25-50			●	●	●	●	●	●		●		8		D				DP	
PCA9531/51		8											8		●	25-100			●	●	●	●	●	●		●		16		D				PW	BS
PCA9532/52		16											8		●	25-200			●	●	●	●	●	●		●		24			D			PW	BS
PCA9533/53		4											2			25-100			●	●	●	●	●	●		●		8		D				DP	
PCA9534/54/54A	8												8	0-1		25-100			●	●	●	●	●	●		●		16	N		D	DB/TS		PW	BS
PCA9535/55	16												8	0-1		25-200			●	●	●	●	●	●		●		24	N		D	DB		PW	BS
PCA9557	8												8		●	25-100			●	●	●	●	●	●		●		16		D				PW	BS
PCA9558	8		5-1-1						2				2			25-100				●		●	●	●	●			28						PW	
PCA9559			5-1-1										4			20-80				●		●	●	●	●			20						PW	
PCA9560			5-1-2										4			25-100				●		●	●	●		●		20			D			PW	
PCA9561			6-0-4										4			25-100				●		●	●	●		●		20			D			PW	
PCA9564						●							128	0-1	●				●	●		●	●	●		●		20	N		D			PW	BS
PCA24S08									8				1						●	●			●	●		●		8		D				DP	
PCF2113												24 ch	2					●	●	●	●	●	●	●		●		100			LQFP100				
PCF2119												32 ch	2					●	●	●	●	●	●	●		●					DIE				
PCF85116-3									16				1							●	●	●	●	●		●		8	N	D					
PCF8562												128	3						●	●	●	●	●	●		●		48			LQFP48				
PCF8563										●			1	0-1			●	●	●	●	●	●	●	●		●		8	PN		TD			DP	
PCF8566												96	16						●	●	●	●	●			●		40	PN		VSO40				
PCF8570									2				8						●	●	●	●	●			●		8	PN	TD					
PCF8574/74A	8												4	0-1		20-100			●	●	●	●	●			●		16	PN		TD	TS			
PCF8575/C	16												8	0-1		20-100			●	●	●	●	●	●		●		24				TSDB			
PCF8576C/D												160	16					●	●	●	●	●	●			●		56/64			VSO56/LQFP64				
PCF8577C												64	16						●	●	●	●	●			●		40	PN		VSO40				
PCF8578/79									2			384	2						●	●	●	●	●			●		56/64			VSO56/LQFP64				
PCF8582C-2/102C-2/103C-2									2				8						●	●	●	●	●			●		8	N	D					
PCF8583										●			2	0-1			●	●	●	●	●	●	●			●		8	PN	TD					
PCF8584						●							128	0-1	●						●	●	●			●		20	PN		TD				
PCF8591											8		8						●	●	●	●	●			●		16	PN		TD				
PCF8593										●			1	0-1	●		●	●	●	●	●	●	●			●		8	N		TD				
PCF8594C-2									4				4						●	●	●	●	●			●		8	N	D					
PCF8598C-2									8				2						●	●	●	●	●			●		8	N		D				
SAA1064												4x8	4			21-mA					●	●	●			●		24	P	T					
SA56004							1°C						8	0-2						●	●		●	●	0 to 125			8		D				DP	
SE95							1°C						8	0-1					2.8	●	●		●	●			●	8		D				DP	

I^{2}C Frequently Asked Questions

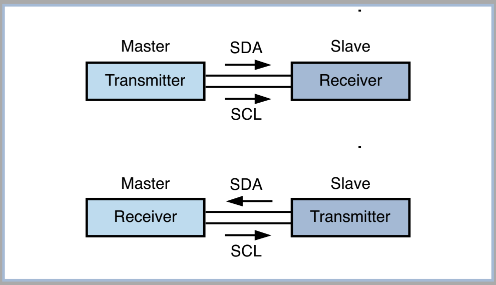
Problem Description	Solution	Suggested Parts
Putting too many of the same devices on the bus causes an address conflict.	Use a multiplexer to break address space into sub-branches. Master selects which sub-branch to address under I²C control. Two to eight sub-branches are available per multiplexer.	PCA9540B, 41, 42A, 43A, 44A, 45A, 46A, 47, 48A
I need more devices than the 400 pF load allows.	Use a multiplexer to break up the capacitance by sub-branch. Sub-branches are addressed individually. Use a repeater or hub to address all devices at the same time (be careful of address conflicts).	PCA9540B, 41, 42A, 43A, 44A, 45A, 46A, 47, 48A PCA9515, 15A, 16, 16A, 17, 18
I have to send I²C through a really long cable.	Use an I²C-bus extender to add high drive to any I²C-bus. Guidelines (80 pF per meter) for 400 kHz are at least 20m and for 30 kHz are at least 1000m.	P82B715, P82B96
I have a mixed-voltage environment that causes conflicts on the open-drain I²C-bus.	Use a switch to dynamically split the bus by pulling downstream channels to different voltages.	PCA9543A, 45A, 46A, 48A GTL2002, GTL2010, GTL2000
I have slow (100 kHz) and fast (400 kHz) parts on the same bus. How can I isolate them to get the most performance from the 400 kHz devices?	Use a bus repeater and have the master disable the 100-kHz segment during 400-kHz communication.	PCA9515, 15A, 16, 16A, 17, 18
I have two masters in my fault-tolerant system, one active at a time. How do I select one master over the other?	Use an I²C master selector to switch from a failing master to its backup. The selector also provides isolation.	PCA9541
I support hot swap in my fault-tolerant system. How can I keep I²C-bus traffic undisturbed during a swap?	Use an I²C hot swap bus buffer to detect bus idle condition, isolate capacitance, and prevent bus glitches.	PCA9510, 11, 12, 13, 14
I need to add a new I²C port to a host.	Use a bus controller to create a new I²C port. You may not need a new port. A multiplexer or a switch may give you the features you need.	PCA9564, PCF8584 PCA954x
The I²C-bus is "multi-drop" and any device can hang the bus. How can I make this bus more fault-tolerant?	Break the bus into different branches to create a "star" configuration. Multi-cast is allowed. The master sets the configuration via I²C.	PCA9543A, 45A, 46A, 48A Simple discrete circuitry with any buffer can detect and isolate failed sections.

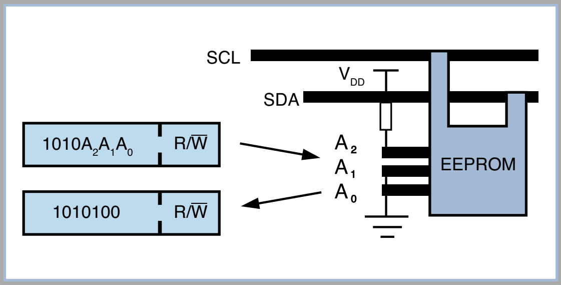
How the I^{2}C-bus Works

I^{2}C-bus Terminology

All the ICs along an I^{2}C-bus are either masters or slaves. A master is an IC that initiates a data transfer, provides the serial clock signal (SCL) during the transfer, and then terminates the transfer. There can be more than one master on the bus at a time – the I^{2}C software protocol uses arbitration and synchronization to prevent collisions and data loss. A slave is any device addressed by the master.

While the master or slave is sending data over the serial data line (SDA), it is referred to as a transmitter. While it's accepting data from the SDA data line, it's called a receiver. A master transmitter can put data onto the SDA data line at any time; a slave transmitter can only do so by request.





Device Addresses

Each device along the I^{2}C-bus has a unique, 7-bit I^{2}C address. The first four bits in the address are typically fixed, indicating device category (e.g. 1010 is assigned to EEPROMs). The last three bits (A_2, A_1, A_0) are set by hardware address pins on the IC package. There are up to eight different address combinations available for each device, so up to eight identical devices can operate on the same I^{2}C-bus. The address pins are held high (1) to Vcc or held low (0) to GND.

The Data Transfer Bitstream

"F" indicates the bus is Free, or available for use. During the Free state the serial data line (SDA) is transferring no data and both the SDA data line and the SCL clock line are high.

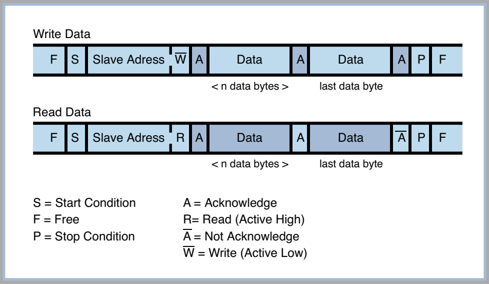
To take control of the bus and initiate a transaction, the master sends out a Start (S) condition. If the master already controls the bus and wants to initiate an additional transaction, it sends out a Repeat Start (Sr) condition. For the start condition, the SDA data line goes from high to low while the SCL clock remains high.

The Start condition is followed by the desired slave address and the instruction to write ($\overline{W}$) or read (R) data.

The slave responds to the master by sending an Acknowledge (A) bit and the transfer begins. During data transfer, the SCL clock line is brought and held low; the SDA data line can be either high or low. The SDA data line only changes state when the SCL clock line is low.

After each byte is sent, the receiver will Acknowledge (A) the transmitter. When the master is the receiver, it will Not Acknowledge ($\overline{A}$) the last byte so it can regain control of the bus to terminate the communication. When the master has completed the transmission, it sends the Stop (P) condition to free the bus. For the stop condition, the SDA data line goes from low to high while the SCL clock line remains high.

With the data transfer complete, the bus returns to the Free state, with both lines high.



I^{2}C vs. SMBus

Developed by Intel in the mid-1990s, the System Management Bus, also known as SMBus, is a popular derivative of the I^{2}C-bus that is, in most cases, compatible with I^{2}C. Both buses use a two-wire communication scheme and have addressable slaves. The SMBus is limited to a maximum data transfer rate of only 100 kbps, requiring special handling in systems that also use the higher transfer rates available with I^{2}C. Other differences include timeout and minimum clock speed, voltage levels, pull-up resistor values, and current levels.

Visit the I^{2}C-bus homepage at
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date of release: January 2005
document order number: 9397 750 13239

Printed in the Netherlands

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