MIPI Alliance Standard for D-PHY
V0.65

MIPI Board approved 29 November 2005

* Caution to Implementers *

This document is a MIPI Specification formally approved by the MIPI Alliance Board of Directors per the process defined in the MIPI Alliance Bylaws. However, the PHY WG has identified certain technical issues in this approved version of the specification that are pending further review and which may require substantive revisions of this document in the near future. Such revisions, if any, will be handled via the formal specification revision process as defined in the Bylaws.

To further assist MIPI companies prior to the conclusion of those formal revisions, the Board has asked the PHY WG to prepare a Release Notes document to accompany this MIPI Specification. The intent of the Release Notes is to provide a list of known technical issues under further discussion with the working group. This may not be an exhaustive list; its purpose is to simply catalog known issues as of this release date. Implementers of this specification should be aware of these facts, and take them into consideration as they work with the specification.

Release Notes for the D-PHY specification are available in the MIPI Alliance secure members website:

Members Home > Specifications > Approved Specifications > MIPI_D-PHY-v065_Notes.pdf

Updates to the D-PHY Release Notes will be posted in this same location as they become available.

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Version 0.65 – 29 November 2005

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Further technical changes to D-PHY are expected as work continues in the PHY Working Group

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MIPI Alliance Standard for D-PHY

1 Overview

This specification provides a flexible, low-cost, high-speed serial interface solution for communication links between components inside a mobile device. Traditionally, these interfaces are CMOS parallel busses with low bit rates for EMI reasons. The D-PHY solution enables significant extension of the interface bandwidth for more advanced applications. The D-PHY solution can be realized with very low power consumption.

1.1 Scope

The scope of this document is to specify the lowest layer of high-speed source-synchronous interfaces to be applied by MIPI application (or protocol) level specifications. This includes the physical interface, electrical interface, low-level timing and the PHY-level protocol. These functional areas taken together are known as D-PHY.

The D-PHY specification shall always be used in combination with a higher layer MIPI specification that references this specification. Initially, this specification will be used for the connection of a host processor to display and camera modules as used in mobile devices. However, this specification can also be referenced by other upcoming higher layer MIPI specifications.

The following topics are outside the scope of this document:

- **Explicit specification of signals of the clock generator unit.** Of course, the D-PHY specification does implicitly require some minimum performance from the clock signals. Intentionally, only the behavior on the interface pins is constrained. Therefore, the clock generation unit is excluded from this specification. and will be a separate functional unit that provides the required clock signals to the D-PHY in order to meet the specification. This allows all kinds of implementation trade-offs as long as these do not violate this specification. More information can be found in section 4.
- **Data encoding.** The D-PHY does not apply line encoding for the Data Payload. Data is transported in bytes. Encoding at the Application Level is allowed as long as the payload data moved through the D-PHY is an integer number of bytes.
- **Test modes, patterns, and configurations.** Obviously testability is very important, but because the items to test are mostly application specific or implementation related, the specification of tests is deferred to either the higher layer specifications or the product specification. Furthermore MIPI D-PHY compliance testing is not yet included in this specification.
- **Procedure to resolve contention situations.** The D-PHY contains several mechanisms to detect Link contention. However, certain contention situations can only be detected at higher levels and are therefore not included in this specification.
- **Ensure proper operation of a connection between different Lane Module types.** There are several different Lane Module types to optimally support the different functional requirements of several applications. This means that next to some base-functionality there are optional features which can be included or excluded. This specification only ensures correct operation for a connection between matched Lane Modules types, which means: Modules that support the same functionality. In case the two sides of the Link are not the same type and these are supposed to work correctly, it shall be ensured by the manufacturer(s) of the Lane Module(s) that the provided additional functionality does not corrupt operation. This can be easiest accomplished if the additional functionality can be disabled by other means independent of the MIPI D-PHY interface, such that the Modules behave as if they were the same type.

- **ESD protection level of the IO.** The required level will depend on a particular application environment and product type.
- **Exact Bit-Error-Rate (BER) value.** The actual value of the achieved BER depends on the total system integration and the hostility of the environment. Therefore, it is impossible to specify a BER for individual parts of the Link. This specification allows for compliant implementations with a BER<10^{-12}.
- **Specification of the PHY-Protocol Interface.** The D-PHY specification includes a PHY-Protocol Interface (PPI) Appendix that provides one possible solution for this interface. This appendix is limited to the essential signals for normal operation in order to clarify the kind of signals needed at this interface. As this interface will be internal for most applications for power reasons, practical implementation might be different without being inconsistent with the D-PHY specification.
- **Implementations.** This specification is intended to restrict the implementation as little as possible. Various sections of this specification use block diagrams or example circuits to illustrate the concept being discussed and are not in any way claimed to be the preferred or required implementation. Only the behavior on the D-PHY interface pins is normative.

Regulatory compliance methods are not within the scope of this document. It is the responsibility of product manufacturers to ensure that their designs comply with all applicable regulatory requirements.

1.2 Purpose

The D-PHY specification is used by manufacturers to design products that adhere to MIPI specifications for mobile device host processor, display and camera interfaces.

Implementing the D-PHY standard reduces the time-to-market and design cost of mobile devices by simplifying the interconnection of products from different manufacturers. In addition, richer feature sets requiring high interface-bitrates can be realized by implementing this standard. Finally, adding new features to mobile devices is simplified due to the extensible nature of the MIPI specifications.

2 Terminology

The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).

The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; must is used only to describe unavoidable situations.

The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.

The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

All sections are normative, unless they are explicitly indicated to be informative.

2.1 Definitions

Back-channel: Communication on a link in the reverse direction from primary communications. For example, a back-channel would refer to communications from Slave to Master in a Master-Slave configuration.

Bi-directional: A single Data Lane that supports communication in both the Forward and Reverse directions.

D-PHY: The source synchronous PHY defined in this document. D-PHYs communicates on the order of ~ 500 Mbit/s hence the Roman numeral for 500 or “D.”

Escape Mode: An optional mode of operation for Data Lanes that allows low bit-rate commands and data to be transferred in a very low power state.

e_{SPIKE}: time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state

Forward Direction: The signal direction is defined relative to the direction of the high-speed DDR clock. Transmission from the side sending the clock to the side receiving the clock is the Forward direction.

Lane: Consists of two complementary Lane Modules communicating via two-line point-to-point Lane Interconnects. Sometimes also used to denote interconnect only. A Lane is used for either Data or Clock signal transmission.

Line: An interconnect wire used to connect a driver to a receiver. Two Lines are required to create a Lane Interconnect.

Link: A complete connection between two devices containing one clock and at least one data lane.

Lane Interconnect: Two-line point-to-point interconnect used for both differential high-speed signaling and low-power single ended signaling.

Lane Module: Module at each side of the Lane for driving and/or receiving signals on the Lane.

Master: The Master side of a Link is defined as the side that transmits the high-speed Clock. The Master side transmits data in the Forward direction.

PHY: The set of Lane Modules on one side of a Link.

PHY Configuration: A set of Lanes that represent a possible link. A PHY configuration consists of a minimum of two Lanes, one clock Lane and one or more Data Lanes.

Reverse Direction: Reverse direction is the opposite of the forward direction. See the description for Forward Direction.

Slave: The Slave side of a Link is defined as the side that does not transmit the high-speed Clock. The Slave side may transmit data in the Reverse direction.

Turnaround: Reversing the direction of communication on a Data Lane.

Unidirectional: A single Lane that supports communication in the Forward direction only.

2.2 Abbreviations

e.g. For example (Latin: exempli gratia)

i.e. That is (Latin: id est)

2.3 Acronyms

BER Bit Error Rate

CIL Control and Interface Logic

DDR Dual Data Rate

EMI Electro Magnetic interference

EoT End of Transmission

HS High-Speed; identifier for operation mode

HS-RX High-Speed Receiver (Low-Swing Differential)

HS-TX High-Speed Transmitter (Low-Swing Differential)

IO Input-Output

229	ISTO	Industry Standards and Technology Organization
230	LMI	Lane Module Interface
231	LP	Low-power: identifier for operation mode
232	LP-CD	Low-Power Contention Detector
233	LPDT	Low-Power Data Transmission
234	LPI	Lane Protocol Interface
235	LP-RX	Low-Power Receiver (Large-Swing Single-Ended)
236	LP-TX	Low-Power Transmitter (Large-Swing Single-Ended)
237	LPS	Low-Power state(s)
238	LSB	Least Significant Bit
239	LSS	Lane Shared Signal
240	Mb/s	Megabits per second
241	MIPI	Mobile Industry Processor Interface
242	MSB	Most Significant Bit
243	PHY	Physical Layer
244	PLL	Phase Locked Loop
245	PI	Protocol Interface (Only used within PHY context)
246	PPI	PHY-Protocol Interface (Equal to PI; can be used within any MIPI context)
247	RF	Radio Frequency
248	RX	Receiver; can be either present at one or both sides of link
249	SE	Single-Ended
250	SoT	Start of Transmission
251	SRC	Slew-Rate Controlled
252	TLIS	Transmission-Line Interconnect Structure: physical interconnect realization between RX and TX
253	TX	Transmitter; can be either present at one or both sides of link
254	UI	Unit Interval, equal to one half the clock period

3 D-PHY Introduction

D-PHY describes a source-synchronous high-speed, low-power, low-cost PHY, especially suited for mobile applications. This D-PHY specification has been written primarily for the connection of camera and display applications to a host processor. Nevertheless, it can be applied to many other applications. It is envisioned that the same type of PHY will also be used in dual-simplex configuration for individual links in a more generic communication network. Operation and available data-rates for a link are asymmetrical due to a master-slave relationship between the two sides of the link. The asymmetrical design significantly reduces the complexity of the link. Some features, like bi-directional, half-duplex operation, are optional. Exploiting this feature is attractive for applications that have asymmetrical data traffic requirements and when the cost of separate interconnects for a back channel is too high. While this feature is optional, it avoids mandatory overhead costs for applications that do not have return traffic requirements or apply separate back-channel interconnects.

3.1 Summary of PHY Functionality

The D-PHY provides a synchronous link between Master and Slave. A Master is primarily a data source and a Slave is primarily a data sink. A practical PHY configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the Master and terminating at the Slave. The data signals can either be unidirectional or bi-directional depending on the selected options. For half-duplex operation, the back-channel bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the link.

The link includes a high-speed mode for fast data-traffic and a low-power mode for control purposes. Optionally, the low-power mode can be used for low-speed asynchronous data communication. High-speed data communication appears in bursts of an arbitrary number of bytes.

The PHY uses two wires per Data Lane plus two wires for the Clock Lane. This gives four wires for the minimum PHY configuration. In high-speed mode each Lane is terminated on both sides and driven by a low-swing, differential signal. In low-power mode all wires are operated single-ended and non-terminated. For EMI reasons the drivers for this mode are slew-rate controlled and current limited.

The actual maximum achievable bit-rate in high-speed mode is determined by the performance of transmitter, receiver and interconnect implementations. Therefore, the maximum bit-rate is not specified in this document. However, this specification is mainly intended to define a solution for a bit-rate range of 80 to 1000 Mb/s per lane. Although PHY configurations are not limited to this range, practical constraints make it the most suitable range for these bandwidths. The effective available data capacity can be increased with more data lanes. The data capacity can be reduced by burst mode communication. The maximum data rate is 10Mb/s in low-power mode. See section 7 for details.

3.2 Selectable Options

In this PHY specification there are several optional features. If any optional feature is selected, it should be implemented according to the specification.

A PHY configuration consists of one Clock Lane and one or more Data Lanes. All Lanes support High-Speed transmission in the Forward direction.

There are two main types of Data Lanes:

- Bi-directional (featuring Turnaround and some Reverse communication functionality)
- Unidirectional (without Turnaround or any kind of Reverse communication functionality)

Bi-directional Data Lanes shall include one or both of the Reverse data communication options:

- High-Speed Reverse communication
- Low-Power Reverse communication (which implies Reverse Escape mode functionality)

For each Lane the Escape mode functionality is optional.

- Applications shall define which Escape Mode functionality is required from the Lanes
- Available options are listed in section 5.6.
- For bi-directional Lanes Escape Mode functionality is selected for each direction

This results in many options for complete PHY Configurations. The degrees of freedom are:

- Single or Multiple Data Lanes
- Bi-directional and/or Unidirectional Data Lane (per Lane)
- Supported types of Reverse communication (per Lane)
- Actions supported by Escape Mode (for each direction per Lane)

Some practical configuration examples can be found in section 4.

3.3 Mandatory Functionality

All functionality that is specified in this document and which is not explicitly stated in section 3.2 shall be implemented for all D-PHY configurations.

4 Architecture

This section describes the internal structure of the PHY including its functions at the behavioral level. Furthermore, several possible PHY configurations are given. Each configuration can be considered as a suitable combination from a set of basic modules.

4.1 Lane Modules

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicate via two interconnect wires to a complementary part at the other side of the link.

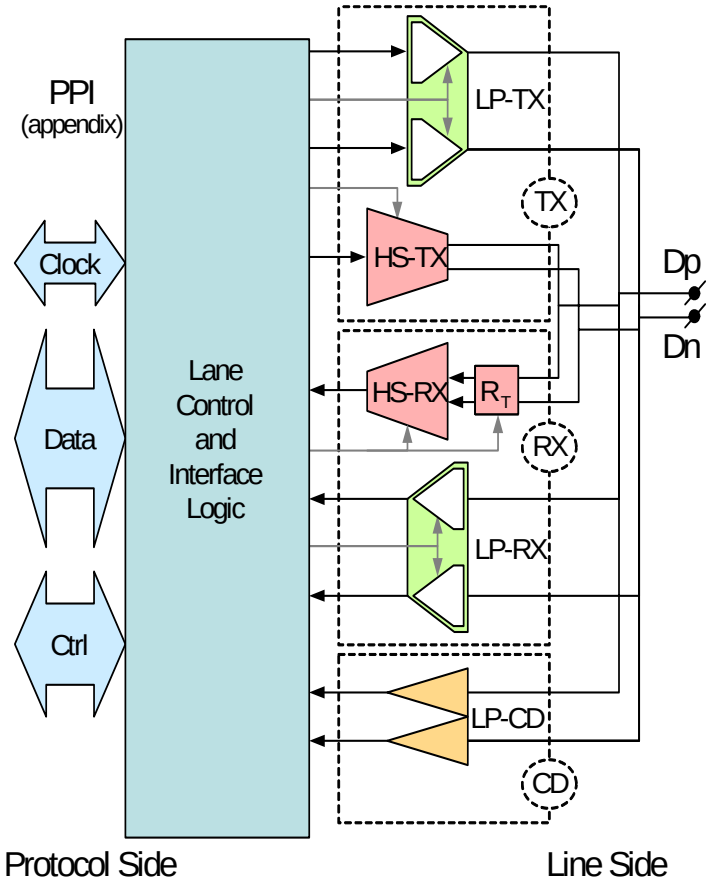


Figure 1 Universal Lane Module Functions

Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. An overview of all functions is shown in Figure 1. High-Speed signals have a low voltage swing, e.g. 200 mV, while Low-Power signals have a large swing, e.g. 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for Control, but have other, optional, use cases. The I/O functions are controlled by a Lane Control and Interface Logic block. This block interfaces with the Protocol and determines the global operation of the Lane Module.

High-Speed functions include a differential transmitter (HS-TX) and a differential receiver (HS-RX).

A Lane Module may contain a HS-TX, a HS-RX, or both. A HS-TX and a HS-RX within a single Lane Module are never enabled simultaneously during normal operation. A High Speed function shall terminate the Lane on its side of the link as defined in sections 8.1.1 and 8.2.1. If no High Speed function in the Lane Module is enabled then the High Speed functions shall be put into a high impedance state.

Low-Power functions include single-ended transmitters (LP-TX), receivers (LP-RX) and Low-Power Contention-Detectors (LP-CD). Low-Power functions are always present in pairs as these are single-ended functions operating on each of the two interconnect wires individually.

Presence of High-Speed and Low-Power functions is correlated. That is, if a Lane Module contains a HS-TX it shall also contain a LP-TX. A similar constraint holds for HS-RX and LP-RX.

The LP-CD function is only required for bi-directional operation. If a Lane Module containing a LP-RX is powered, that LP-RX shall always be active and continuously monitor line levels. A LP-TX shall only be enabled when driving Low-Power states. The LP-CD function is only required for bi-directional operation. If present, the LP-CD function is enabled to detect contention situations while the LP-TX is driving Low-Power states. The LP-CD shall check for contention at least once before driving a new state on the line.

The activities of LP-TX, HS-TX, and HS-RX in a single Lane Module are mutually exclusive, except for some short crossover periods. For detailed specification of the Line Side Clock and Data signals, and the HS-TX, HS-RX, LP-TX, LP-RX and LP-CD functions, see sections 8 and 9.

Obviously, for proper operation the set of functions in the Lane Modules at both sides of the Link has to be matched. This means that the complementary functions of HS and LP functions at one side of the link must be present at the other side. Complimentary functions are RX and TX for each mode of operation. Furthermore, a Contention Detector is needed in any Lane Module that combines TX and RX functions.

4.2 Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. This main direction of communication is denoted as the Forward direction. Communication in the opposite direction is called Reverse traffic. The latter is only available for bi-directional Data Lanes. In that case the Clock Lane remains in the Forward direction, but Data Lane(s) are turned-around, sourcing data from the Slave side. The Reverse traffic arriving at the Master side will not be phase synchronous with the Forward direction clock. Reverse transmission by the Slave side is one-fourth of the Forward direction speed, based on the Forward direction Clock as transmitted via the Clock Lane. This ratio makes it easy to find a suitable phase at the Master Side for Data recovery of Reverse direction traffic.

4.3 High-Speed Clock Generation

In many cases a PLL Clock Multiplier will be needed for the High-Speed Clock generation at the Master Side. The D-PHY specification uses an architectural model where a separate Clock Multiplier Unit outside the PHY generates the required High-Speed Clock signals for the PHY. Whether this Clock Multiplier Unit in practice will be integrated inside the PHY is left to the implementer.

4.4 Clock Lane, Data Lanes and the PHY-Protocol Interface

A complete PHY contains, beside Lane Modules, a PHY Interface Module, which ties all Lanes, the Clock Multiplier Unit, and the PHY Protocol Interface together. Figure 2 shows a PHY configuration example for a Link with two Data Lanes plus a separate Clock Multiplier Unit.

The logical PHY-Protocol interface (PPI) includes, for each individual Lane, a set of signals to cover the functionality of the Lane. Clock signals can be shared for all Lanes. The pilot clock signal and controls for the Clock Multiplier Unit are not within the scope of this specification.

For simplification reasons the interface to each Lane will, in many cases, also be named PPI. There is no essential difference as all signals in the individual LMIs will be represented in the PPI, but shared signals are merged in the PPI.

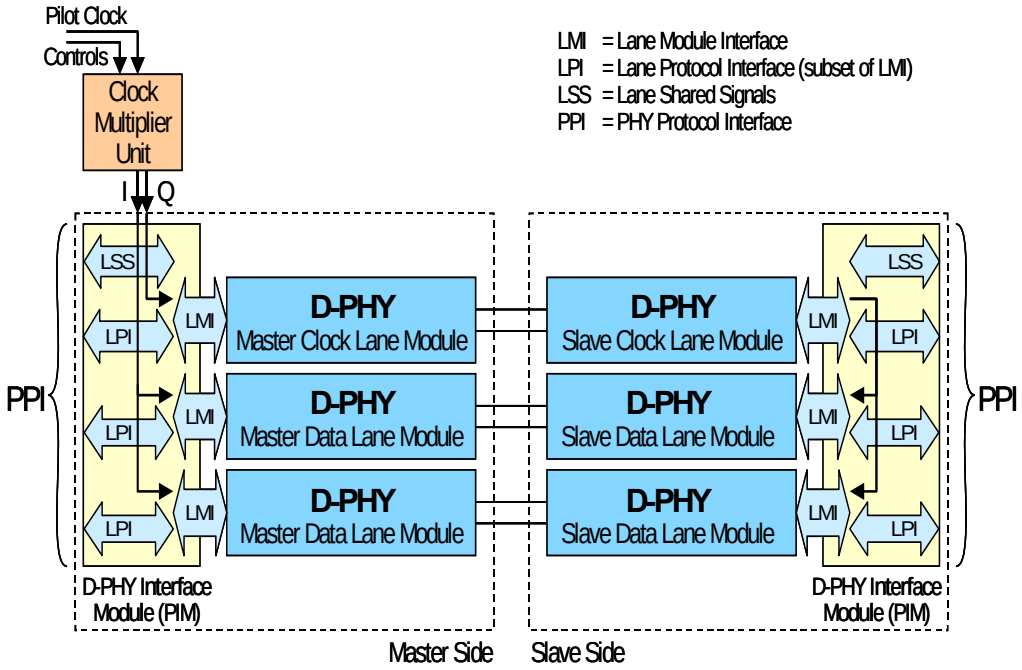


Figure 2 Two Data Lane PHY Configuration

4.5 Lane Module Types

Which functions are required in a Lane Module depends on the Lane Type and on which side of the link the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane without High-speed Reverse Communication. In addition, a fourth Lane type, Bi-directional Data Lane with High-speed Reverse Communication, is possible. Escape mode functionality is optional for each of these Lane types. Several PHY configurations can be constructed with these Lane types.

The requirements for the 'Control and Interface Logic' (CIL) function depend on the Lane type and link side. Figure 3 shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane Types. Section 5 and Annex A implicitly specify the contents of the CIL function. The actual realization is left to the implementer.

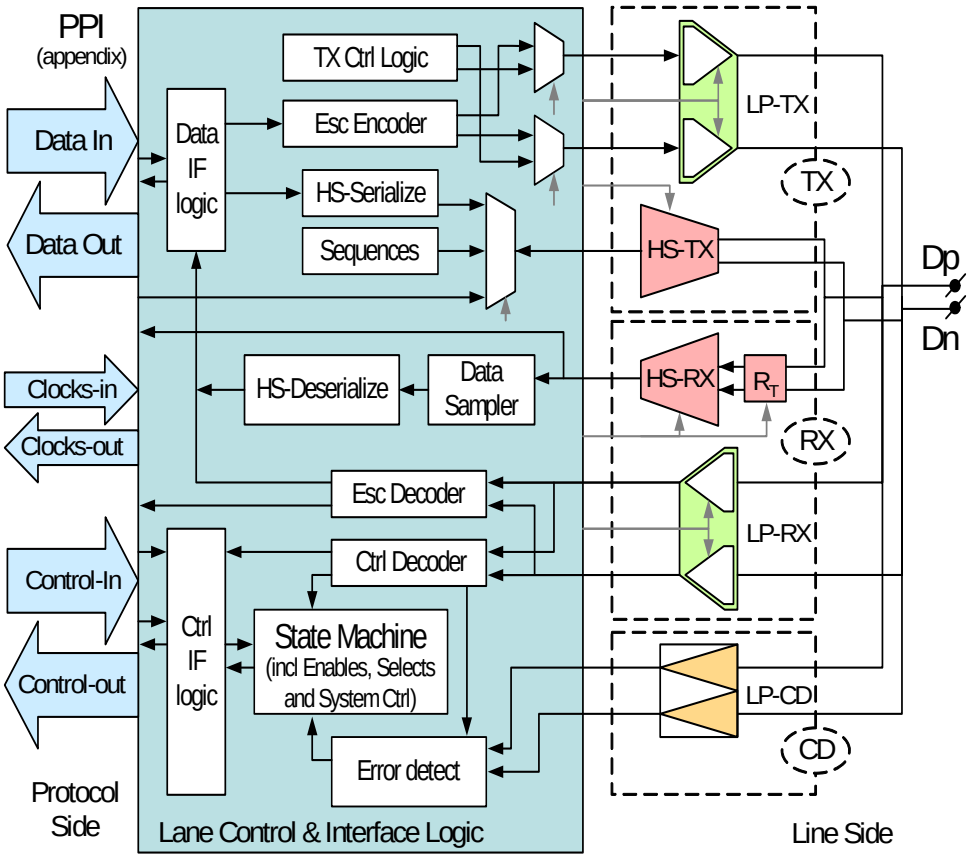


Figure 3 Universal Lane Module Architecture

Of course, stripped-down versions of the Universal Lane Module that just support the required functionality for a particular Lane type are possible. These stripped-down versions are identified by the acronyms in Table 1. For simplification reasons, any of the four identification characters can be replaced by an X, which means that this can be any of the available options. For example, a CIL-MUYN is therefore a stripped-down CIL function for the Master Side of a Unidirectional Link with Escape mode functionality only in the Forward direction. A CIL-SBXX is a CIL function for the Slave Side of a Link with support for Bi-directional High-speed communication and any combination of Escape mode functionality.

Table 1 Lane Type Descriptors

Prefix	Link Side	High Speed Lane Direction	Forward Direction Escape Mode Supported	Reverse Direction Escape Mode Supported
CIL-	M – Master S - Slave	B – Bi-directional C – Clock U – Unidirectional	Y – Yes N – No	Y – Yes N – No
	X – Don't Care			

The PHY Protocol Interface contains Data-in and Data-out in Byte format, Input and/or output Clock signals and Control signals. Control signals include action requests, handshakes, test settings, and initialization. A proposal for a logical internal interface is described in Annex A. Although not a

requirement it might be very useful to use the proposed PPI. For external use on IC's an implementation might multiplex many signals on the same pins. However, for power efficiency reasons, the PPI will normally be always within a PHY module.

4.5.1 Clock Lane

For the Clock-Lane, only a limited set of line states is used. However, for Clock Transmission and Low-Power mode the same TX and RX functions are required as for Unidirectional Data Lanes. A Clock Lane Module for the Master Side therefore contains a HS-TX, LP-TX, and a CIL-MCNN function, while the Slave Side Module includes a HS-RX, a LP-RX and a CIL-SCNN function.

Note that the required functionality for a Clock Lane is very similar to a Unidirectional Data Lane, except that the high-speed DDR clock is transmitted in-quadrature with Data signals instead of in-phase. In addition, Low Power Lane states are defined differently. The Clock signals with the appropriate phases are generated outside the PHY and delivered to the individual Lanes. The realization of the Clock generation unit is outside the scope of this specification. The quality of the Clock signals shall be sufficient to meet the timing requirement for the Line signal as specified in section 9.

4.5.2 Unidirectional Data Lane

For a Unidirectional Data Lane the Master Module shall contain at least a HS-TX, a LP-TX, and a CIL-MUXN function. The Slave side shall contain at least a HS-RX, a LP-RX and a CIL-SUXN.

Notice that a Universal Data Lane Module is also suitable for each side of this Lane type, although not all available functionality will be used in that case.

4.5.3 Bi-directional Data Lane without High-Speed Reverse Communication

A bi-directional Data Lane Module without High Speed Reverse Communication shall include a Reverse Escape mode. This means the Master-side Lane Module includes a HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MBXY. The Slave-side consists of a HS-RX, LP-RX, LP-TX, LP-CD and a CIL-SBXY.

Notice that a universal Data Lane Module is also suitable for each side of this Lane type, although not all functionality available will be used in this case.

4.5.4 Bi-directional Data Lane with High-Speed Reverse Communication

A bi-directional Data Lane Module with High-Speed Reverse communication for either side of the Link contains all the functions of a Bi-directional Data Lane without High-Speed Reverse Communication plus HS-RX for the Master Side or HS-TX for the Slave Side. The CIL shall be CIL-MBXX for the Master Side and CIL-SBXX for the Slave Side. This type of Lane Module might be suitable for both Master and Slave side but because of the asymmetry of the Link one side shall be set as Master and the other side as Slave. See section 5.13 for a description of the operational flow for Master and Slave CILs.

4.6 Configurations

This section outlines several common PHY configurations but should not be considered an exhaustive list of all possible arrangements. Any other configuration that does not violate the operational scheme as specified in section 5 is also allowed.

In order to create an abstraction level, the Lane Modules are represented in this section by Lane Module Symbols. Figure 4 shows the syntax and meaning of symbols.

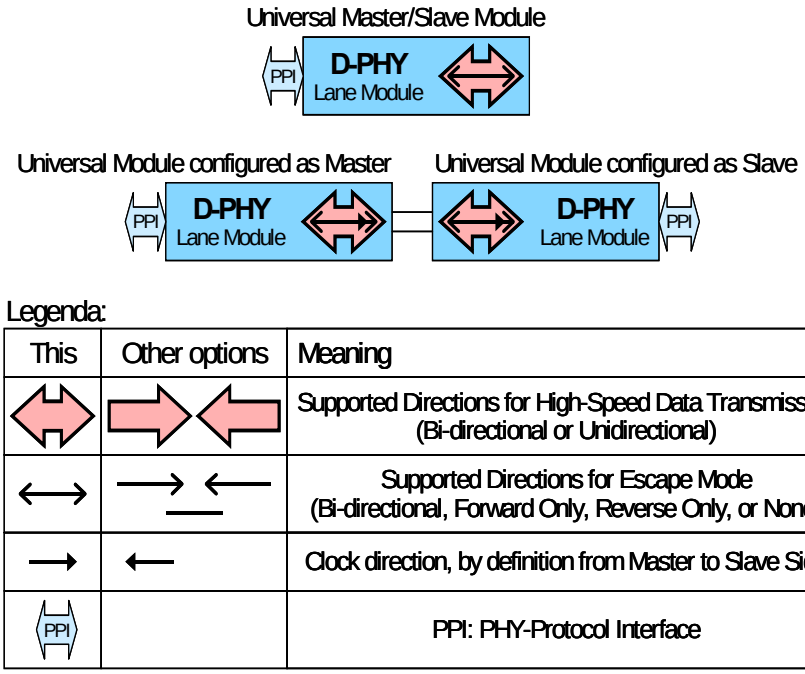


Figure 4 Lane Symbol Macros and Symbols Legend

For multiple Data Lanes a large variety of configurations is possible. Figure 5 shows an overview of symbolic representations for different Lane types. The acronyms mentioned for each Lane type represent the functionality of each module in a short way. This also sets the requirements for the CIL function inside each Module.

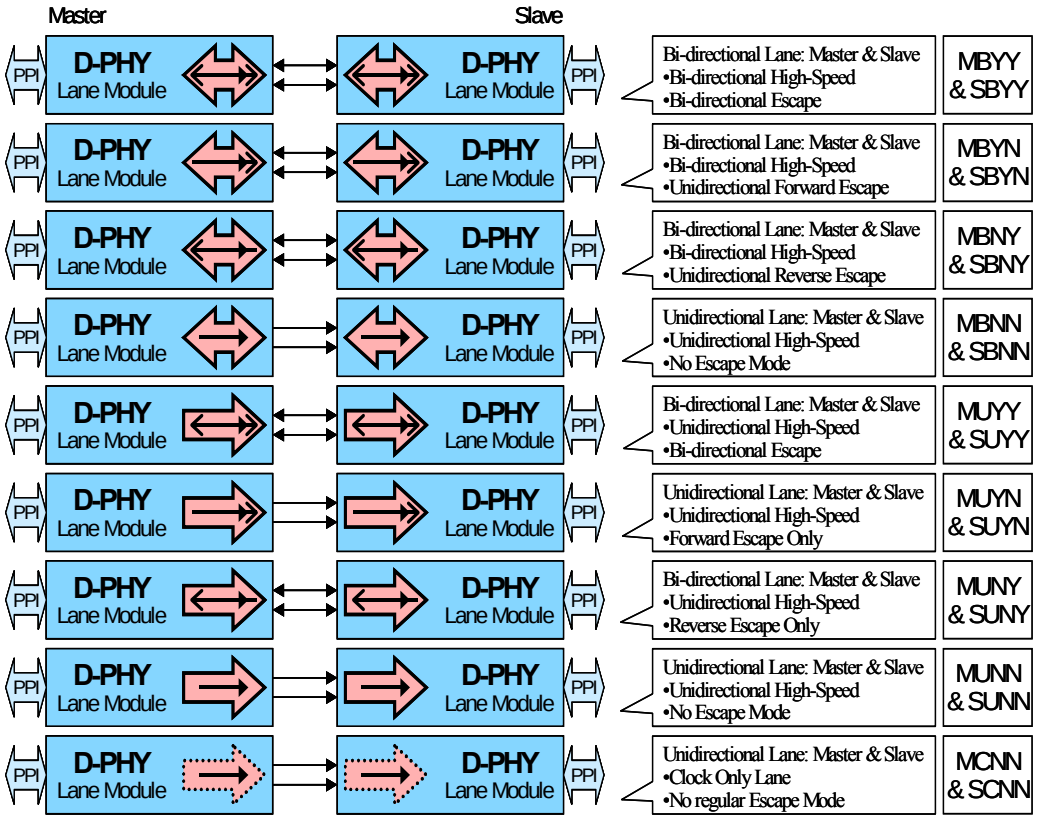


Figure 5 All Possible Data Lane Types and a Basic Unidirectional Clock Lane

4.6.1 Unidirectional Configurations

All unidirectional configurations are constructed with Clock Lanes and one or more Unidirectional Data Lanes. Two basic configurations can be distinguished: Single Data Lane and Multiple Data Lanes. For completeness a Dual-Simplex configuration is also shown. At the PHY level there is no difference between a Dual-Simplex configuration and the other configurations.

4.6.1.1 PHY Configuration with a Single Data Lane

This configuration includes one Clock Lane and one Unidirectional Data Lane from Master to Slave. Communication is therefore only possible in the Forward direction. Figure 6 shows this configuration. This configuration requires four interconnect signal wires.

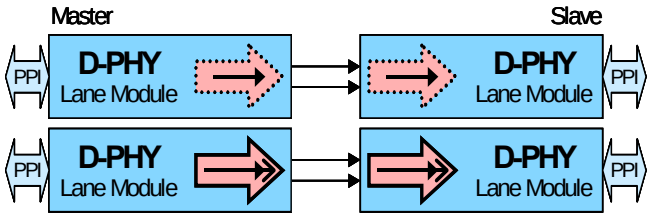


Figure 6 Unidirectional Single Data Lane Configuration

4.6.1.2 PHY Configuration with Multiple Data Lanes

This configuration includes one Clock Lane and multiple Unidirectional Data Lanes from Master to Slave. Bandwidth is extended, but communication is only possible in the Forward direction. The PHY specification does not require all Data Lanes to be active simultaneously. In fact, the Protocol layer controls all Data Lanes individually. Figure 7 shows this configuration for three Data Lanes. If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

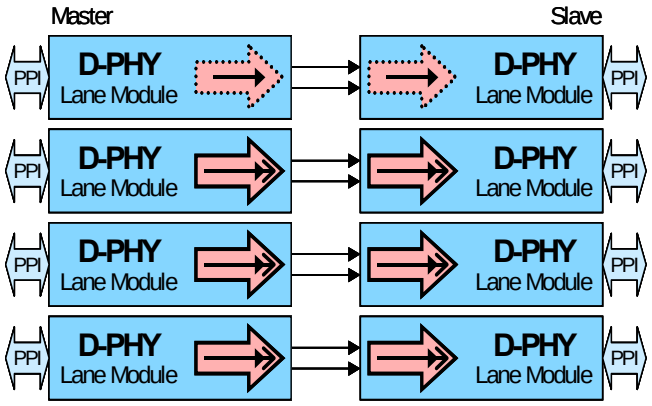


Figure 7 Unidirectional Multi Data Lane Configuration

4.6.1.3 Dual-Simplex (Two Directions with Unidirectional Lanes)

This case is the same as two independent ('dual') unidirectional ('simplex') configurations: one for each direction. Each direction has its own Clock Lane and may contain either a single or multiple Data Lanes. Please note that the Master and Slave side for the two different directions are opposite. The PHY configuration for each direction shall comply with the D-PHY specifications. As both directions are conceptually independent, the bit rates for each direction do not have to match. However, for practical implementations, it is attractive to match rates and share some internal signals as long as both links fulfill all specifications externally. Figure 8 shows this dual PHY configuration.

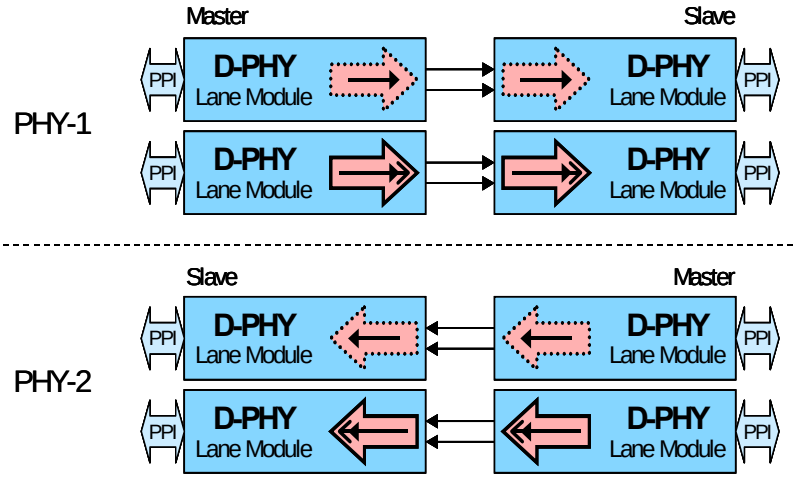


Figure 8 Two Directions Using Two Independent Unidirectional PHY's

4.6.2 Bi-Directional Half-Duplex Configurations

Bi-directional configurations consist of a Clock Lane and one or more bi-directional Data Lanes. Half-duplex operation enables bi-directional traffic across shared interconnect wires. This saves wires compared to the Dual-Simplex configuration. Communication in the Forward direction is similar to a unidirectional Lane, however communication time on the Lane is shared with Reverse traffic. The bit rate in the Reverse direction is one-fourth of the Forward direction. For this reason, this configuration is especially useful for cases with asymmetrical data traffic.

4.6.2.1 PHY Configurations with a Single Data Lane

This configuration includes one Clock Lane and one bi-directional Data Lane. This allows time-multiplexed data traffic in both Forward and Reverse directions. Figure 9 shows this configuration with a Data Lane that supports both High-Speed and Escape communication in both directions. Other possibilities are that only one type of reverse communication is supported. All these configurations require four interconnect wires.

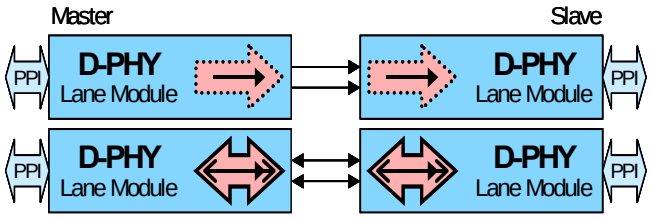


Figure 9 Bidirectional Single Data Lane Configuration

4.6.2.2 PHY Configurations with Multiple Data Lanes

This configuration includes one Clock Lane and multiple bi-directional Data Lanes. Communication is possible in both the Forward and Reverse direction for each individual Lane. The maximum available bandwidth scales with the number of Lanes for each direction. The PHY specification does not require all Data Lanes to be active simultaneously or even to be operating in the same direction. In fact, the Protocol layer controls all Data Lanes individually. Figure 10 shows an example configuration with two Data Lanes. If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

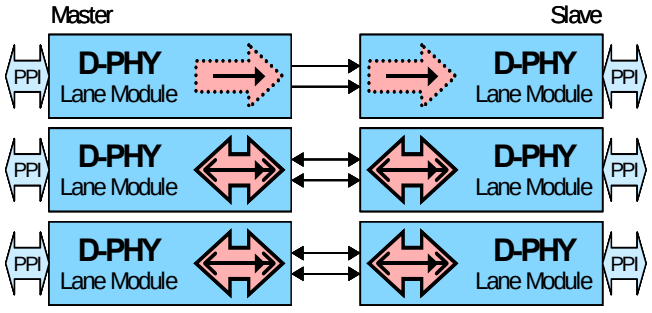
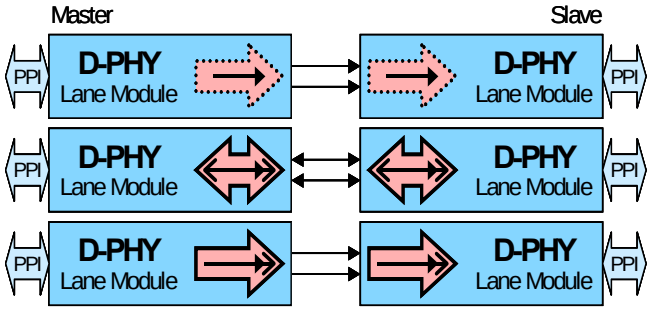


Figure 10 Bi-directional Multi Data Lane Configuration

4.6.3 Mixed Data Lane Configurations

Instead of using only one Data Lane type, PHY configurations may combine unidirectional and bi-directional Data Lanes. In order to share the Clock Lane, the Master and Slave Side should match for these

505 Lanes. Figure 11 shows an example configuration with one bi-directional and one unidirectional Data
506 Lane, while Master and Slave sides match.



507

508 **Figure 11 Mixed Type Multiple Data Lane Configuration**

5 Global Operation

This section specifies operation of the D-PHY including signaling types, communication mechanisms, operating modes and coding schemes. Detailed specifications of the required electrical functions can be found in section 8.

5.1 Payload Data

In some modes, the PHY transports payload data provided by the protocol layer to the other side of the link. This section specifies the restrictions for the transmitted and received payload data.

5.1.1 Data Units

The minimum data unit shall be one byte. Data provided to a TX and taken from a RX on any Lane shall be an integer number of bytes. This restriction holds for both high-speed and low-power data transmission in any direction.

5.1.2 Bit order, Serialization, and De-Serialization

For serial transmission, the bytes shall be serialized in the transmitting PHY and de-serialized in the receiving PHY. The PHY assumes no particular meaning or value of incoming and outgoing data bytes. Therefore, in this specification, the order of bits within bytes is denoted with the transmission order. Wherever bits are numbered (B#), the counter increases with time. An example of bit-order with respect to time is shown in Figure 12; bit 0 is always transmitted first. Whether bit 0 is considered the MSB or the LSB depends on how data is provided by the protocol to the logical PPI.

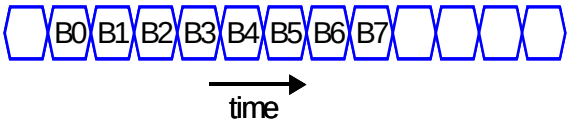


Figure 12 Bit Transmission Order

5.1.3 Encoding/Decoding

The D-PHY specification describes the encoding and decoding of individual bits only. Any higher level encoding and decoding is outside the D-PHY scope. The data stream only contains unprocessed serialized payload data as provided to the transmitter. Therefore, the D-PHY does not impose any limitation on payload data formats.

5.1.4 Data buffering

Data transmission takes place on protocol request. As soon as communication starts the protocol layer at the transmit side shall provide valid data as long as it does not stop its transmission request. The protocol on the receive side shall take the data as soon as delivered by the receiving PHY. The signaling concept, and therefore the PHY protocol handshake, does not allow data throttling. Any data buffering for this purpose shall be inside the protocol layer.

5.2 Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential-0 and Differential-1. Low-Power signaling is used for both Control mode and Escape mode. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

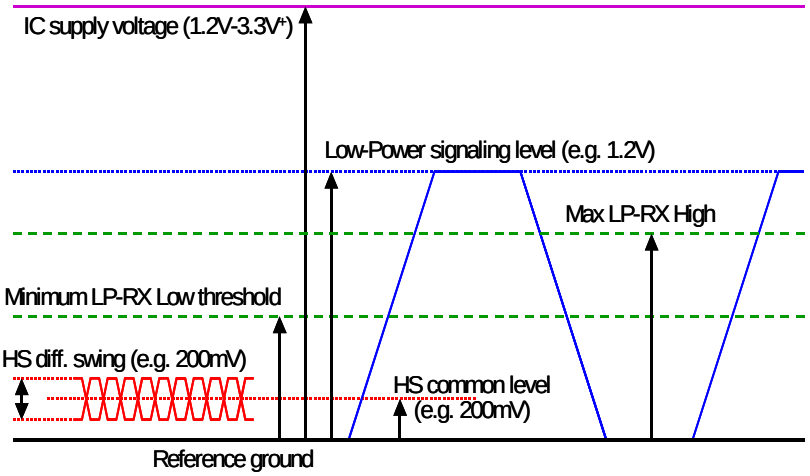


Figure 13 Line Levels

The Stop state has a very exclusive and central function. If a Line level Stop state is observed for the minimum time required the PHY state machine shall asynchronously return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 2 lists all the states that can appear on a Lane during normal operation. Detailed specifications of electrical levels can be found in section 8.

All state transitions shall be smooth and exclude glitch effects, which might cause misinterpretation of signals.

Table 2 Lane State Descriptions

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Turn-around or Escape Mode
HS-0	HS Low	HS High	Differential-0	1	1
HS-1	HS High	HS Low	Differential-1	1	1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Turn-around or Escape Mode
LP-11	LP High	LP High	N/A	Stop	2

Notes:

1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.

2. If LP-11 occurs during Escape Mode the Lane returns to Stop state (Control Mode LP-11)

5.3 Operating Modes: Control, High-Speed, and Escape

During normal operation a Data Lane will be either in Control or High-Speed mode. High-speed Data transmission happens in bursts and starts from and ends at a Stop state (LP-11), which is by definition in Control mode. The Lane is only in high-speed mode during Data bursts. The sequence to enter high speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in high speed mode until a LP-11 is received. The special Escape mode can only be entered via a request within Control mode. The Data Lane shall always exit Escape mode and return to Control mode after detection of a Stop state. If not in High-speed or Escape mode the Data Lane shall stay in Control mode. For Data Lanes and for Clock Lanes the Stop state serves as general standby state and may last for any period of time > T_{LPX}. Possible events starting from and ending in the Stop state are High-Speed Data Transmission burst (LP-11, LP-01, LP-00), Escape mode request (LP-11, LP-10, LP-00, LP-01, LP-00), or Turnaround request (LP-11, LP-10, LP-00, LP-10, LP-00). The Lane shall stay in the Stop state as long as no other state is presented on the Lane.

5.4 High-Speed Data Transmission

High-Speed Data Transmission occurs in bursts. To aid receiver synchronization data bursts shall be extended by the transmitter with a leader and trailer sequence. These sequences shall be eliminated by the receiver. These sequences can therefore be observed on the transmission lines, but shall not be used by the protocol.

Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a Data Lane shall remain in the Stop state, unless a Turnaround or Escape request is presented on the Lane. During a HS Data Burst the Clock Lane shall be in High-Speed mode, providing a Clock to the Slave side.

5.4.1 Burst Payload Data

The payload data of a burst shall always be an integer number of bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and practical BER differs from zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length. See section 8 for details.

5.4.2 Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 3 describes the sequence of events on TX and RX side.

591 **Table 3 Start-of-Transmission Sequence**

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition form LP-01 to LP-00 on the Lines
Enables High-Speed driver and disables Low-Power drivers simultaneously.	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and Line termination
	Waits for Time-out $T_{HS-SETTLE}$ in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	
	Synchronizes Bytes upon recognition of Leader Sequence '011101'
Continues to Transmit High-Speed payload data	
	Receives payload data

592 ### 5.4.3 End-of-Transmission

593 At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by
594 means of an End-of-Transmission (EoT) procedure. Table 4 shows the sequence of events during the EoT
595 procedure.

596 **Table 4 End-of-Transmission Sequence**

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leave LP-00 state and enter Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects

TX Side	RX Side
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

5.4.4 HS Data Transmission Burst

Figure 14 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane. The handshake with the protocol-layer is described in Annex A.

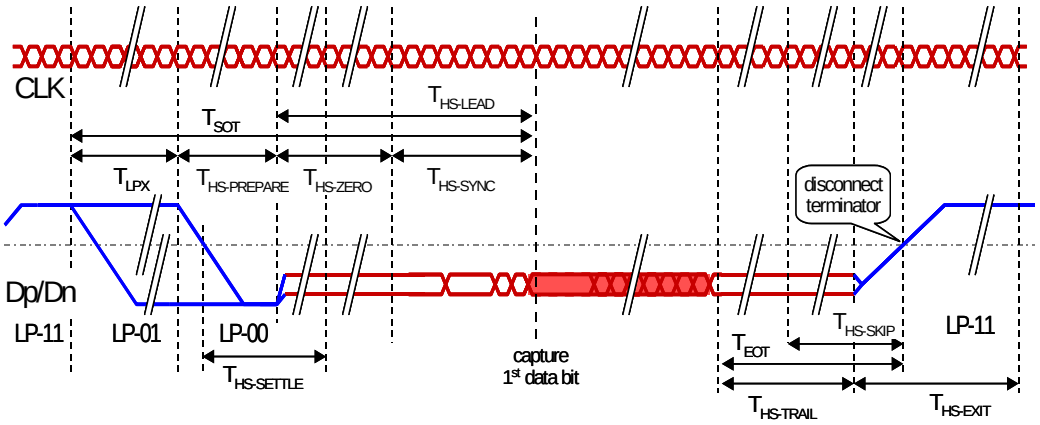


Figure 14 High-Speed Data Transmission in Bursts

Figure 15 shows the state machine for High-Speed data transmission that is described in Table 5.

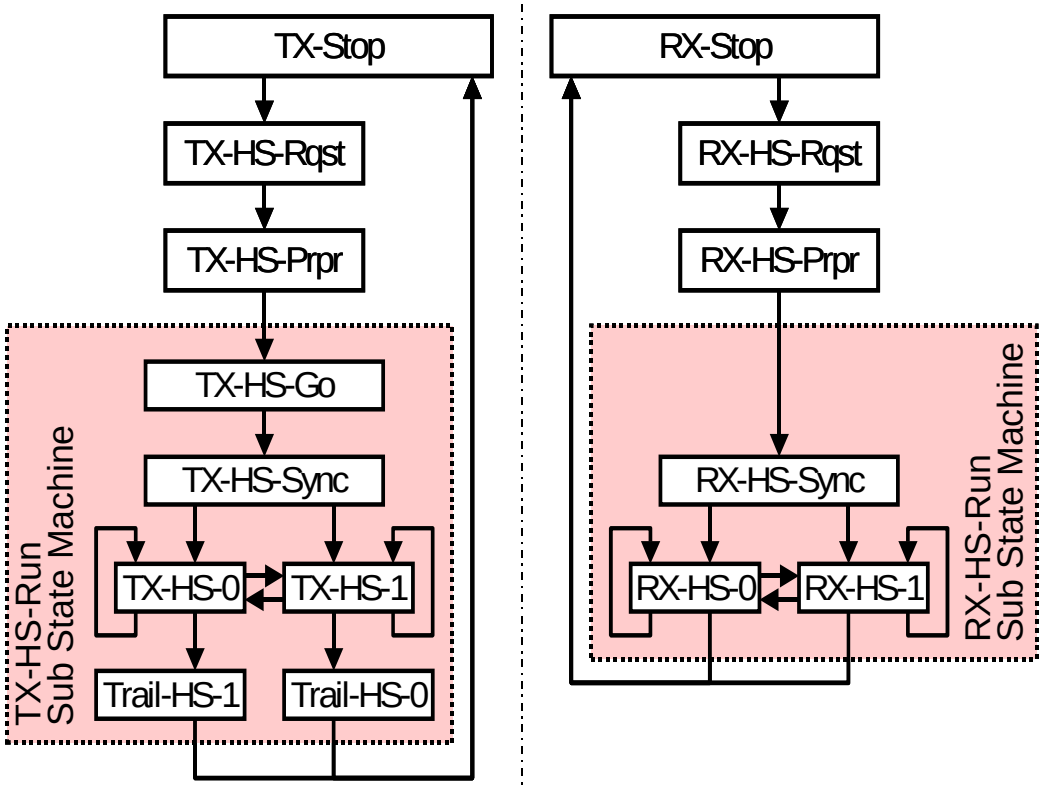


Figure 15 TX and RX State Machines for High-Speed Data Transmission

Table 5 High-Speed Data Transmission State Machine Description

State	Line Event(s)	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-Bridge	End of timed interval T_{LPX}
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{HS\text{-}PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-Sync	End of timed interval $T_{HS\text{-}ZERO}$
TX-HS-Sync	Transmit sequence HS-00011101	TX-HS-0	After Sync sequence if first payload data bit is 0
		TX-HS-1	After Sync sequence if first payload data bit is 1
TX-HS-0	Transmit HS-0	TX-HS-0	Send another HS-0 bit after a HS-0 bit
		TX-HS-1	Send a HS-1 bit after a HS-0 bit
		Trail-HS-1	Last payload bit is HS-0, trailer sequence is HS-1

State	Line Event(s)	Exit State	Exit Conditions
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-1 bit after a HS-0 bit
		TX-HS-1	Send another HS-1 bit after a HS-1
		Trail-HS-0	Last payload bit is HS-1, trailer sequence is HS-0
Trail-HS-0	Transmit HS-0	TX-Stop	End of timed interval $T_{HS-TRAIL}$
Trail-HS-1	Transmit HS-1	TX-Stop	End of timed interval $T_{HS-TRAIL}$
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX- HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS- Prpr	Receive LP-00	RX-HS-Sync	End of timed interval $T_{HS-SETTLE}$
RX-HS-Sync	Receive HS sequence …00000011101	RX-HS-0	Proper match found (any single bit error allowed) for Sync sequence in HS stream, the following bits are payload data.
		RX-HS-1	
RX-HS-0	Receive HS-0	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11
RX-HS-1	Receive HS-1	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11

5.5 Bi-directional Data Lane Turnaround

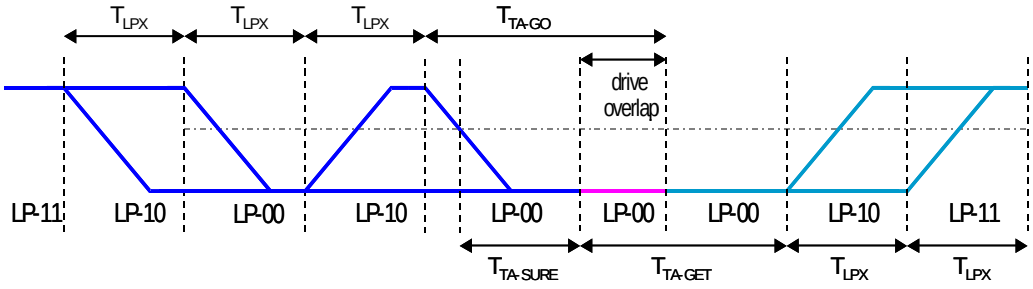
The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround. Lane Turnaround shall be handled completely in Control mode. Table 6 lists the sequence of events during Turnaround.

Table 6 Link Turnaround Sequence

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Drives Stop state (LP-11)	Observes Stop state
Drives LP-Rqst state (LP-10) for a time T_{LPX}	Observes transition from LP-11 to LP-10 states
Drives Bridge state (LP-00) for a time T_{LPX}	Observes transition from LP-10 to LP-00 states

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Drives Mark-1 state (LP-10) for a time T_{LPX}	Observes transition from LP-00 to LP-10 states
Drives Bridge state (LP-00) for a time $T_{TA\text{-}GO}$	Observes the transition from Mark-1 to Bridge state and waits for a time TTA-SURE. After correct completion of this time-out this side knows it is in control.
	Drives Bridge state (LP-00) for a period $T_{TA\text{-}GET}$
Stops driving the Lines and observes the Line states with its LP-RX in order to see an acknowledgement.	
	Drives Mark-1 state (LP-10) for a period $T_{TA\text{-}ACK}$
Observes Mark-1 state (LP-10) on the Lines, interprets that as acknowledge the other side has indeed taken control. Waits for Stop state to complete Turnaround procedure.	
	Drives Stop state (LP-11) for a period T_{LPX}
Observes transition to Stop state (LP-11) on the Lines, interprets this as Turnaround completion acknowledgement, switches to normal LP receive mode and waits for further actions from the other side	

615 Figure 16 shows the Turnaround procedure graphically.



616

617 **Figure 16 Turnaround Procedure**

618 The Turnaround procedure can be interrupted if the Lane is not yet driven into the Bridge state by means of
619 driving a Stop state. Driving the Stop state shall abort the Turnaround procedure and return the Lane to the
620 Stop state. The PHY shall ensure against interruption of the procedure after the start of the Bridge state.
621 Once the PHY drives the Bridge state it shall not abort the Turnaround procedure. The Protocol can take
622 appropriate action if it determines an error has occurred because the Turnaround procedure did not
623 complete within a certain time. See section 6.3.5 for more details. Figure 17 shows the Turnaround state
624 machine that is described in Table 7.

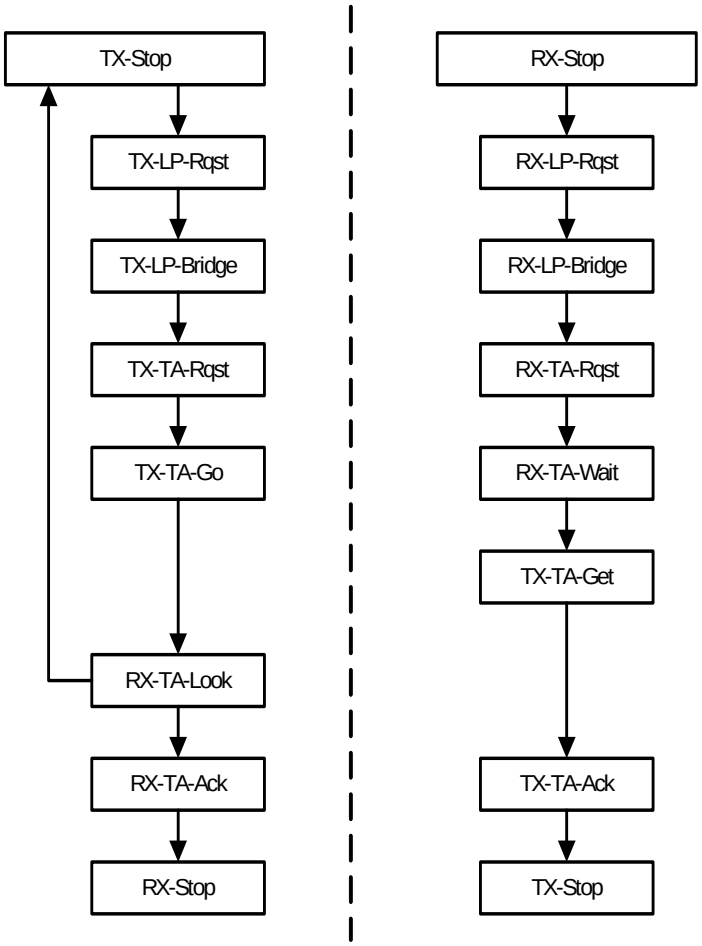


Figure 17 Turnaround State Machine

Table 7 Turnaround State Machine Description

State	Line Signal(s)	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Turnaround (PPI)
TX-LP-Rqst	Transmit LP-10	TX-LP-Bridge	End of timed interval T_{LPX}
TX-LP-Bridge	Transmit LP-00	TX-TA-Rqst	End of timed interval T_{LPX}
TX-TA-Rqst	Transmit LP-10	TX-TA-Go	End of timed interval T_{LPX}
TX-TA-Go	Transmit LP-00	RX-TA-Look	End of timed interval $T_{TA\text{-}GO}$
RX-TA-Look	Receive LP-00	RX-TA-Ack TX-Stop	Line transition to LP-10 On request of Protocol to cancel Turnaround (PPI)
RX-TA-Ack	Receive LP-10	RX-Stop	Line transition to LP-11

State	Line Signal(s)	Exit State	Exit Conditions
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Bridge	Line transition to LP-00
RX-LP-Bridge	Receive LP-00	RX-TA-Rqst	Line transition to LP-10
RX-TA-Rqst	Receive LP-10	RX-TA-Wait	Line transition to LP-00
RX-TA-Wait	Receive LP-00	TX-TA-Get	End of timed interval $T_{TA-SURE}$
TX-TA-Get	Transmit LP-00	TX-TA-Ack	End of timed interval T_{TA-GET}
TX-TA-Ack	Transit LP-10	TX-Stop	End of timed interval T_{LPX}

5.6 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation is optional and, even if supported, does not have to include all available features.

A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state. A Receiver that does not support Escape mode shall ignore any Escape mode Entry Requests.

Once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table 8 lists all currently available Escape mode commands and actions. All unassigned commands are reserved for future expansion.

The Stop state shall be used to exit Escape mode, but should be avoided during Escape mode operation as it immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

The PHY in Escape mode shall implement Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a Data Lane in this mode does not depend on the Clock Lane. The complete Escape mode Action for a Trigger-Reset command is shown in Figure 18.

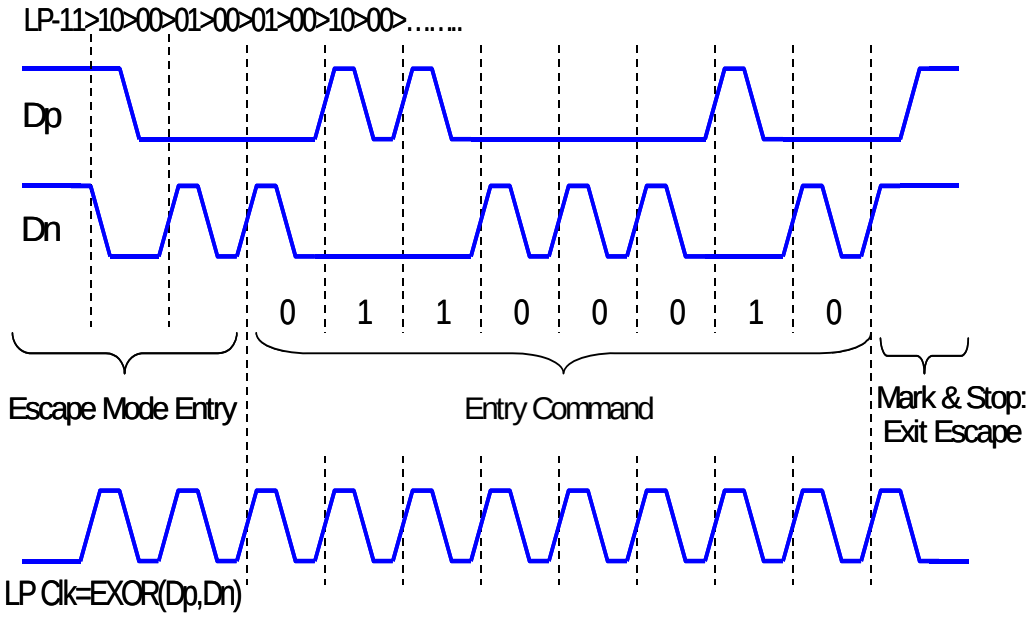


Figure 18 Trigger-Reset Command in Escape Mode

Note that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a 'zero-bit' and it shall send a Mark-1 followed by a Space to transmit a 'one-bit'. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be any Mark state that is not part of the communicated bits. The Clock can be derived from the two Line signals, Dp and Dn, by means of an EXOR function. The length of each individual LP state period shall be T_{LPX}.

Table 8 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Remote Application Reset	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

5.6.1 Remote Triggers

Trigger signaling is the mechanism to send a trigger event to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface.

Figure 18 shows an example of an Escape mode Reset-Trigger action. The Lane enters Escape mode via the Escape mode Entry procedure. If the Entry Command Pattern matches the Reset-Trigger Command a Trigger is flagged to the protocol at the receive side via the logical PPI. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

Note that Trigger signaling including Reset-Trigger is a generic messaging system. The Trigger commands do not impact the behavior of the PHY itself. Therefore, Triggers can be used for any purpose by the Protocol layer.

5.6.2 Escape Sub-Modes

Escape mode also features some Sub-modes, which can extend the capabilities of PHY Lanes. These are currently Low-Power Data Transmission mode and Ultra-Low Power mode. Some additional Sub-modes are reserved for future purposes.

5.6.2.1 Low-Power Data Transmission

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at Low-Speed, while the Lane remains in Low-Power mode.

Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause in LPDT mode by maintaining a Space state on the Lines. A Stop state on the Lines stops Low-Power Data Transmission mode, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark state, which does not represent a data-bit. Figure 19 shows a two-byte transmission with a pause period between the two bytes.

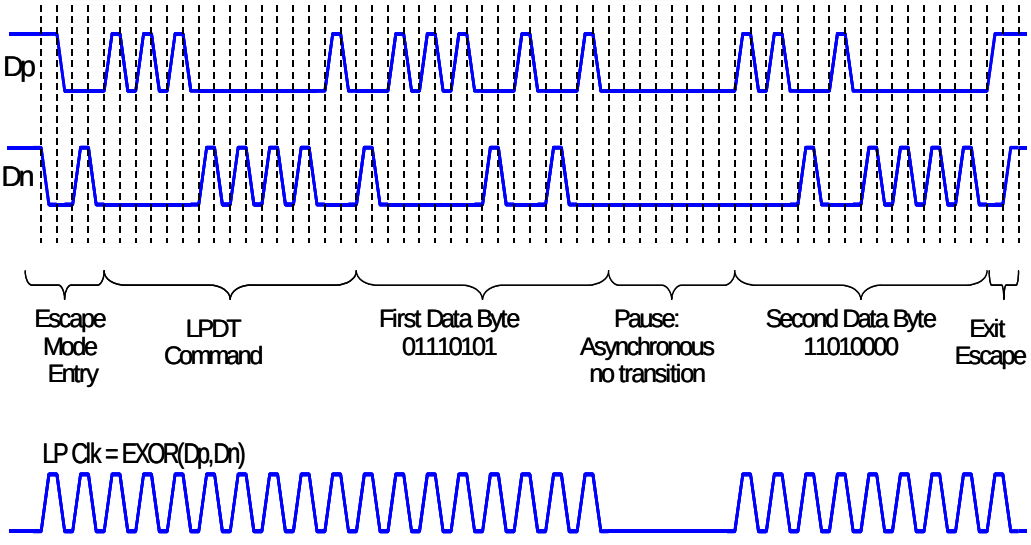


Figure 19 Two Data Byte Low-Power Data Transmission Example

The PPI operates at the byte level. In this Sub-mode a Low-Power (Bit) Clock signal ($f_{MOMENTARY}$<20MHz) provided to the transmit side is used to transmit data. Data reception is self-timed by the bit encoding. Therefore, a variable clock rate can be allowed. A logical handshake in the PPI shall enable asynchronous coding. See Annex A for a possible solution. At the end of LPDT the Lane shall return to the Stop state. If the Data is not byte boundary aligned when exiting Escape mode LPDT, an error has occurred and the last bits may get lost. In this case the receiving PHY Lane shall signal an LPDT Sync Error to the Protocol.

5.6.2.2 Ultra-Low Power Mode

If the Ultra-Low Power Entry Command is sent after an Escape mode Entry command, the Lane shall not exit Low-Power state for a period T_{WAKEUP}. The Protocol that requests this action shall ensure this time requirement. This Command shall be flagged to the receive side Protocol. During this mode the Lines are in the Space state (LP-00). This sub-mode allows the PHY circuitry to be powered down much more quickly than during normal operation. Ultra-Low Power mode is exited by means of a Mark state with a length T_{WAKEUP} followed by a Stop state.

5.6.2.3 Escape Mode State Machine

The state machine for Escape mode operation is shown in Figure 20 and described in Table 9.

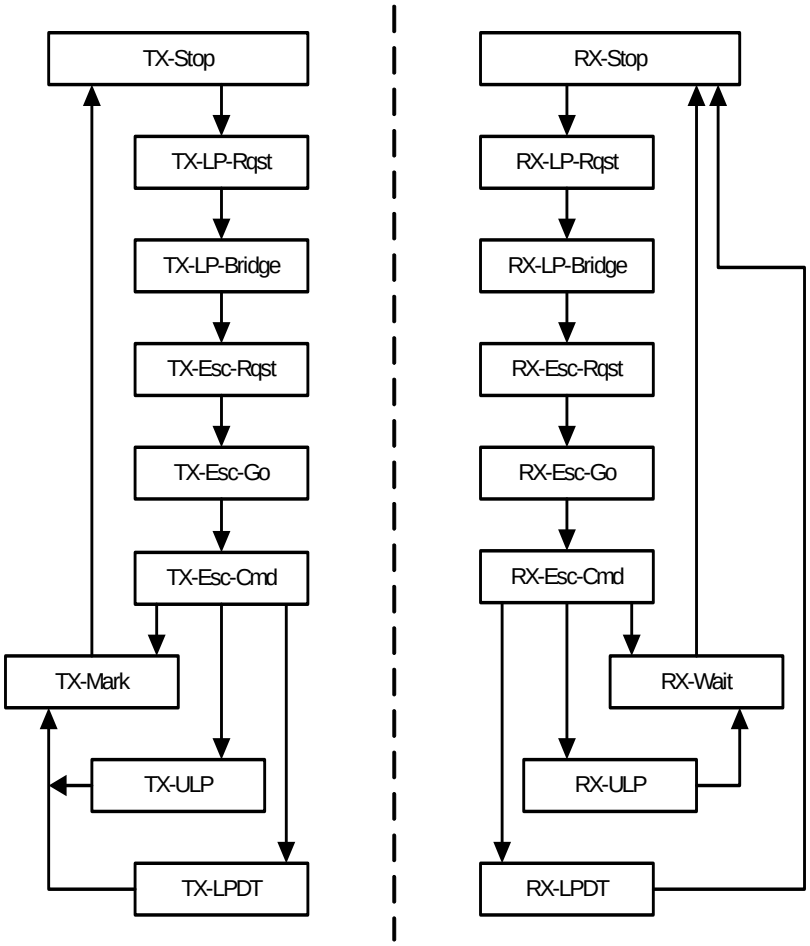


Figure 20 Escape Mode State Machine

704 **Table 9 Escape Mode State Machine Description**

State	Line Signal(s)	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Esc mode (PPI)
TX-LP-Rqst	Transmit LP-10	TX-LP-Bridge	After time T_{LPX}
TX-LP-Bridge	Transmit LP-00	TX-Esc-Rqst	After time T_{LPX}
TX-Esc-Rqst	Transmit LP-01	TX-Esc-Go	After time T_{LPX}
TX-Esc-Go	Transmit LP-00	TX-Esc-Cmd	After time T_{LPX}
TX-Esc-Cmd	Transmit sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	TX-Mark	Next driven state after time T_{LPX}
		TX-ULP	After Ultra Low-Power Command
		TX-LPDT	After Low-Power Data Transmission Command
TX-ULP	Transmit LP-00	TX-Mark	End of ULPM on request of Protocol (PPI)
TX-LPDT	Transmit data bits		After last transmitted data bit
TX-Mark	Mark-1 or Mark-0	TX-Stop	Next driven state after time T_{LPX}, or T_{WAKEUP} if leaving ULPM
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Bridge	Line transition to LP-00
RX-LP-Bridge	Receive LP-00	RX-Esc-Rqst	Line transition to LP-01
RX-Esc-Rqst	Receive LP-01	RX-Esc-Go	Line transition to LP-00
RX-Esc-Go	Receive LP-00	RX-Esc-Cmd	Line transition out of LP-00
RX-Esc-Cmd	Receive sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	RX-Wait	After Trigger and Unrecognized Commands
		RX-ULP	After Ultra Low-Power Command

State	Line Signal(s)	Exit State	Exit Conditions
		RX-LPDT	After Low-Power Data Transmission Command
RX-ULP	Receive LP-00	RX-Wait	Line transition to LP-01 or LP-10
RX-LPDT	Receive data bits	RX-Stop	Line transition to LP-11 (Last state should be a Mark)
RX-Wait	Any, except LP-11	RX-Stop	Line transition to LP-11

5.7 High Speed Clock Transmission

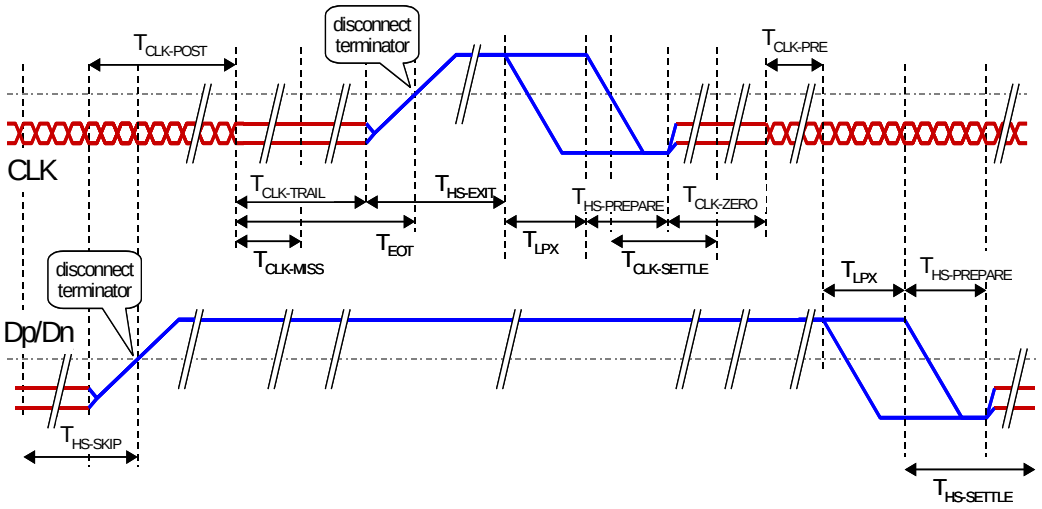
In High-Speed mode the Clock Lane provides a low-swing differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of every Data byte. Details of the Data-Clock relationship and timing specifications can be found in section 9.

A Clock Lane is similar to a Unidirectional Data Lane. However, there are some timing differences and a Clock Lane transmits a High-Speed DDR Clock signal instead of Data bits. Furthermore, the Low-Power mode functionality is defined differently for a Clock Lane than a Data Lane. A Clock Lane shall be unidirectional and shall not include regular Escape mode functionality. Only ULPM is supported via a special entry sequence using the LP-Rqst state. High-Speed Clock Transmission shall be entered from, and exited into, a Stop state.

The Clock Lane mode is controlled by the Protocol via the Clock Lane PPI. The Protocol shall only stop the Clock Lane when there are no High-Speed transmissions active in any Data Lane.

The High-Speed Data Transmission start-up time of a Data Lane is extended if the Clock Lane is in Low-Power mode. In that case the Clock Lane shall first return to High-Speed operation before the Transmit Request can be handled.

The High-Speed Clock signal shall continue running for a period $T_{CLK\text{-}POST}$ after the last Data Lane switches to Low-Power mode and ends with a HS-0 state. The procedure for switching the Clock Lane to Low-Power mode is given in Table 10. Note the Clock Burst always contains an even number of transitions as it starts and ends with an HS-0 state. This implies that the clock provides transitions to sample an even number of bits on any associated data lanes. Clock periods shall be reliable and according to the HS timing specifications. The procedure to return the Clock Lane to High-Speed Clock Transmission is given in Table 11. Both Clock Start and Stop procedures are shown in Figure 21.



729

730 **Figure 21 Switching the Clock Lane Between Clock Transmission and Low-Power Mode**

731 **Table 10 Procedure to Switch Clock Lane to Low-Power Mode**

Master Side	Slave Side
Drives High-Speed Clock signal (Toggling HS-0/HS-1)	Receives High-Speed Clock signal (Toggling HS-0/HS-1)
Last Data lane goes into Low-Power mode	
Continues to drives High-Speed Clock signal for a period $T_{CLK-POST}$ and ends with HS-0 state	
Drives HS-0 for a time $T_{CLK-TRAIL}$	Detects absence of Clock transitions within a time $T_{CLK-MISS}$, disables HS-RX then waits for a transition to the Stop state
Disables the HS-TX, enables LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	
	Detects the Lines transitions to LP-11, disables HS termination, and enters Stop state

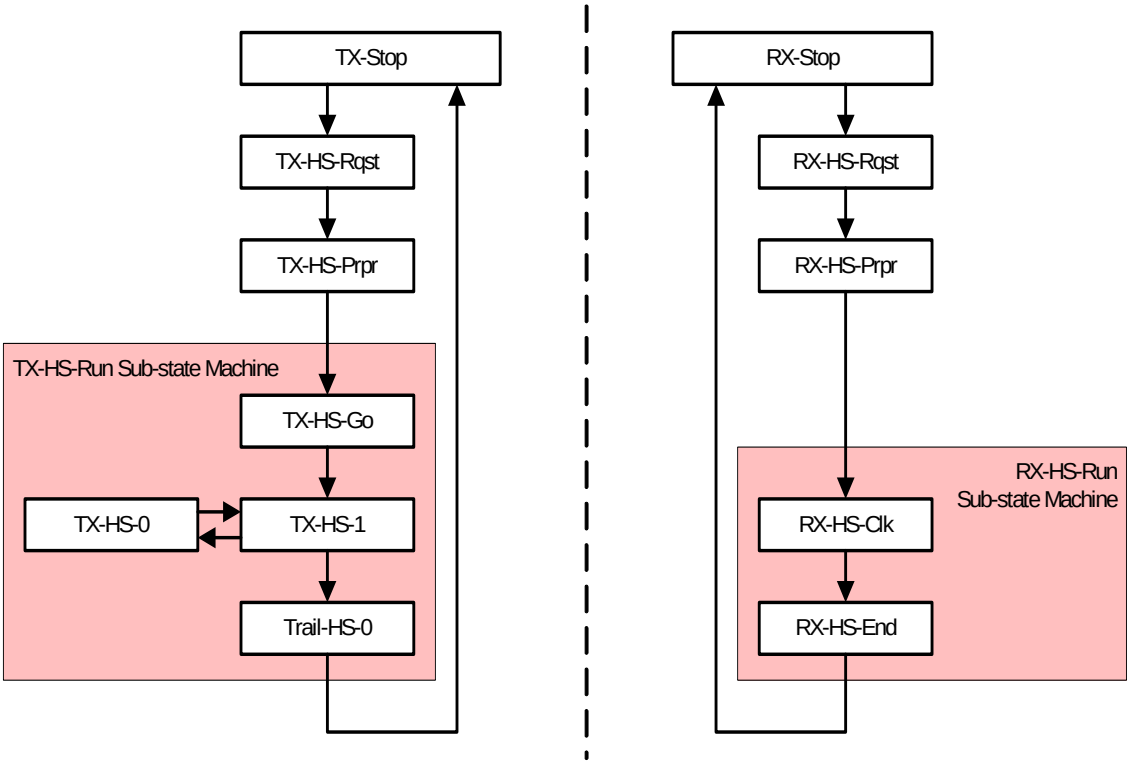
732

733 **Table 11 Procedure to Initiate High Speed Clock Transmission**

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Req state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines. Enables HS-RX and Line termination

TX Side	RX Side
Enables High-Speed driver and disables Low-Power drivers simultaneously. Drives HS-0 for a time $T_{CLK-ZERO}$.	Observes transition form LP-11 to LP-00 on the Lines
	Waits for Time-out $T_{CLK-SETTLE}$ in order to neglect transition effects
	Receives HS-signal
Drives the High-Speed Clock signal for time period $T_{CLK-PRE}$ before any Data Lane might start-up	Receives High-Speed Clock signal

734 The Clock Lane state machine is shown in Figure 22 and is described in Table 12.



735

736 **Figure 22 High-Speed Clock Transmission State Machine**

737 **Table 12 Description of High-Speed Clock Transmission State Machine**

State	Line Event(s)	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-HS-Prpr	End of timed interval T_{LPX}

State	Line Event(s)	Exit State	Exit Conditions
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{HS-PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-1	End of timed interval $T_{CLK-ZERO}$
TX-HS-0	Transmit HS-0	TX-HS-1	Send a HS-1 phase after a HS-0 phase: DDR Clock
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-0 phase after a HS-1 phase: DDR Clock
		Trail-HS-0	On request to put Clock Lane in Low-Power
Trail-HS-0	Transmit HS-0	TX-HS-Stop	End of timed interval $T_{CLK-TRAIL}$
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX-HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS-Prpr	Receive LP-00	RX-HS-Clk	End of timed interval $T_{CLK-SETTLE}$
RX-HS-Clk	Receive DDR-Q Clock signal	RX-Clk-End	Time-out $T_{CLK-MISS}$ on the period on the Clock Lane without Clock signal transitions
RX-HS-End	Receive HS-0	RX-HS-Stop	Line transition to LP-11

5.8 Clock Lane Ultra Low-Power Mode

Although a Clock Lane does not implement any Escape mode, the Clock Lane shall support an Ultra Low-Power mode. The Ultra Low-Power mode shall be entered from a Stop state. When leaving Ultra Low-Power mode, the Clock Lane must go through a Stop state before entering High-Speed Transmission mode.

A Clock Lane shall enter Ultra Low-Power mode via a Clock Lane Ultra Low-Power mode Entry procedure. After a Stop state, the transmit side shall drive LP-Rqst state (LP-10) and then drive Bridge state (LP-00). As soon as the Bridge state is observed on the Lines the Clock Lane shall enter Ultra Low-Power mode. If LP-10 or LP-11 is detected immediately after the LP-Rqst state, the Ultra Low-Power mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state, respectively.

Once the Ultra-Low Power mode Entry procedure is complete, the Lane shall not exit this mode for a period T_{WAKEUP}. The Protocol that requests this action shall ensure this time requirement. The receiving PHY shall flag the appearance of ULPM to the receive side Protocol. During this mode the Lines are in the Bridge state (LP-00). Ultra-Low Power mode is exited by means of a Mark-0 or Mark-1 state with a length T_{WAKEUP} followed by a Stop state.

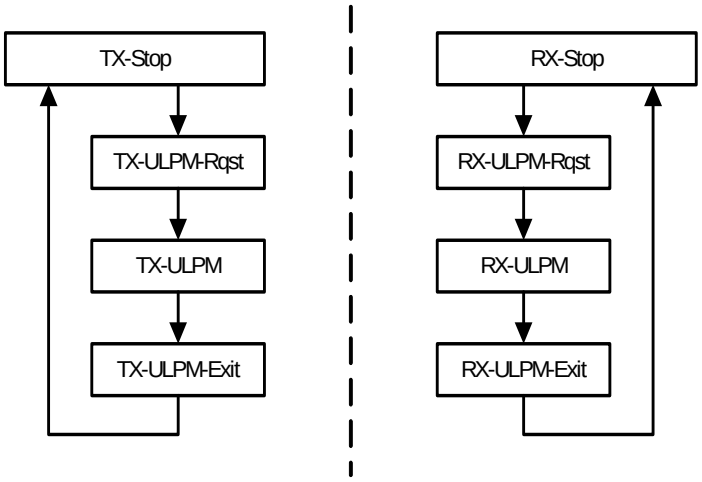


Figure 23 Clock Lane Ultra Low-Power Mode State Machine

Table 13 Clock Lane Ultra Low-Power Mode State Machine Description

State	Line Event(s)	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-ULPM-Rqst	On request of Protocol for Ultra Low-Power mode
TX-ULPM-Rqst	Transmit LP-10	TX-ULPM	End of timed interval T_{LPX}
TX-ULPM	Transmit LP-00	TX-ULPM-Exit	On request of Protocol to leave Ultra Low-Power mode
TX-ULPM-Exit	Transmit LP-10	TX-Stop	End of timed interval T_{WAKEUP}
RX-Stop	Receive LP-11	RX-ULPM-Rqst	Line transition to LP-10
RX-ULPM-Rqst	Receive LP-10	RX-ULPM	Line transition to LP-00
RX-ULPM	Receive LP-00	RX-ULPM-Exit	Line transition to LP-10
RX-ULPM-Exit	Receive LP-10	RX-Stop	Line transition to LP-11

5.9 Global Operation Timing Parameters

Table 14 lists the ranges for all timing parameters used in this section.

Table 14 Global Operation Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	20		50	ns	

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-ZERO}$	Time to drive HS-0 before the Sync sequence	70			ns	
$T_{HS-SETTLE}$	Time-out at RX to ignore transition period of SoT	50		70	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	50		75	ns	
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40		55	ns	
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	
$T_{TA-RQST}$	Time to drive LP-10 to request Turnaround	50			ns	
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	100		150	ns	
$T_{TA-SURE}$	Time-out before new TX side start driving	50		100	ns	
T_{TA-GET}	Time to drive LP-00 by new TX	100			ns	
T_{TA-ACK}	Time to drive LP-10 by new TX for acknowledge	50			ns	
$T_{TA-FINISH}$	Time to drive LP-11 to complete Turnaround	50			ns	
T_{LPX}	Length of any Low-Power state period	50			ns	
T_{WAKEUP}	Recovery time from Ultra-Low Power mode	1			ms	
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	100			ns	
$T_{CLK-MISS}$	Detection time that the clock has stopped toggling			60	ns	1
$T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	150			ns	
$T_{CLK-SETTLE}$	RX time-out on SoT for Clock Lane to ignore transitions	50		150	ns	

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-PRE}$	Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	8			UI	
T_{INIT}	Initialization period (PHY might calibrate)	100			µs	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	

1. The minimum value depends on the bit rate. Realizations should ensure proper operation for all the supported bit rates

5.10 System Power States

Each Lane within a PHY configuration has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power mode. For details on Ultra-Low Power mode see sections 5.6.2.2 and 5.8. The transition between these modes shall be handled by the PHY.

5.11 Initialization

At power-up all Lanes of the PHY shall enter the Stop state in the Forward direction after an unspecified time. This means for the Master Side all Lanes shall be in TX-Stop state (drive LP-11). All Lanes on the Slave Side shall be in RX-Stop state (observe LP-11). The Stop state shall be maintained by the Protocol for a period T_{INIT}. All line states during the unspecified interval prior to Stop state for period of T_{INIT} shall be ignored.

Table 15 Initialization States

States	Entry Conditions	Exit Conditions	Line Levels
Master Init	At Master Module Power-up	Protocol control	Drive Stop state
Slave Init	At Slave Module Power-up	Input Lines exit Stop state	Receive Stop state

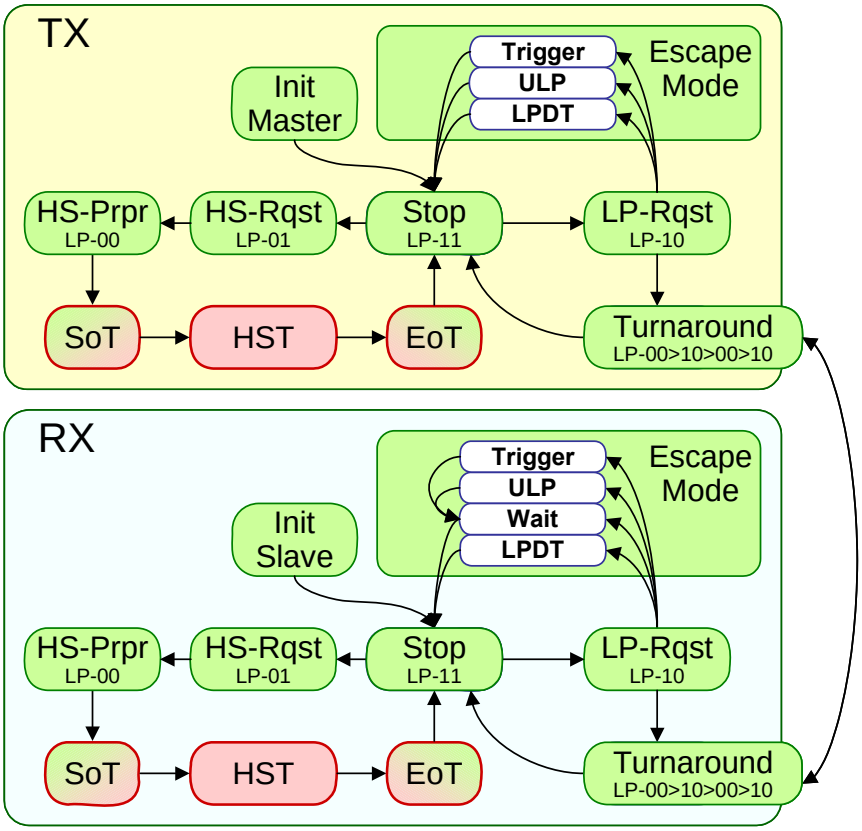
5.12 Calibration

There is no explicit calibration required by the D-PHY specification. If an implementation requires calibration, the calibration can take place off-line during the Initialization period T_{INIT} while the lines are in Stop state. The calibration process should not be visible on the lines. Any further detail on calibration is outside the scope of this specification.

5.13 Global Operation Flow Diagram

All previously described aspects of operation, either including or excluding optional parts, are contained in Lane Modules. Figure 24 shows the operational flow diagram for a Data Lane Module. Within both TX

780 and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround,
781 and Initialization.



782

783 **Figure 24 Data Lane Module Flow Diagram**

784 Figure 25 shows the operational flow diagram for a Clock Lane module. The Clock Lane module has four
785 major operational states: Init (of unspecified duration), Low Power Stop state, Ultra Low Power state, and
786 High Speed clock transmission. The figure also shows the transition states as described previously.

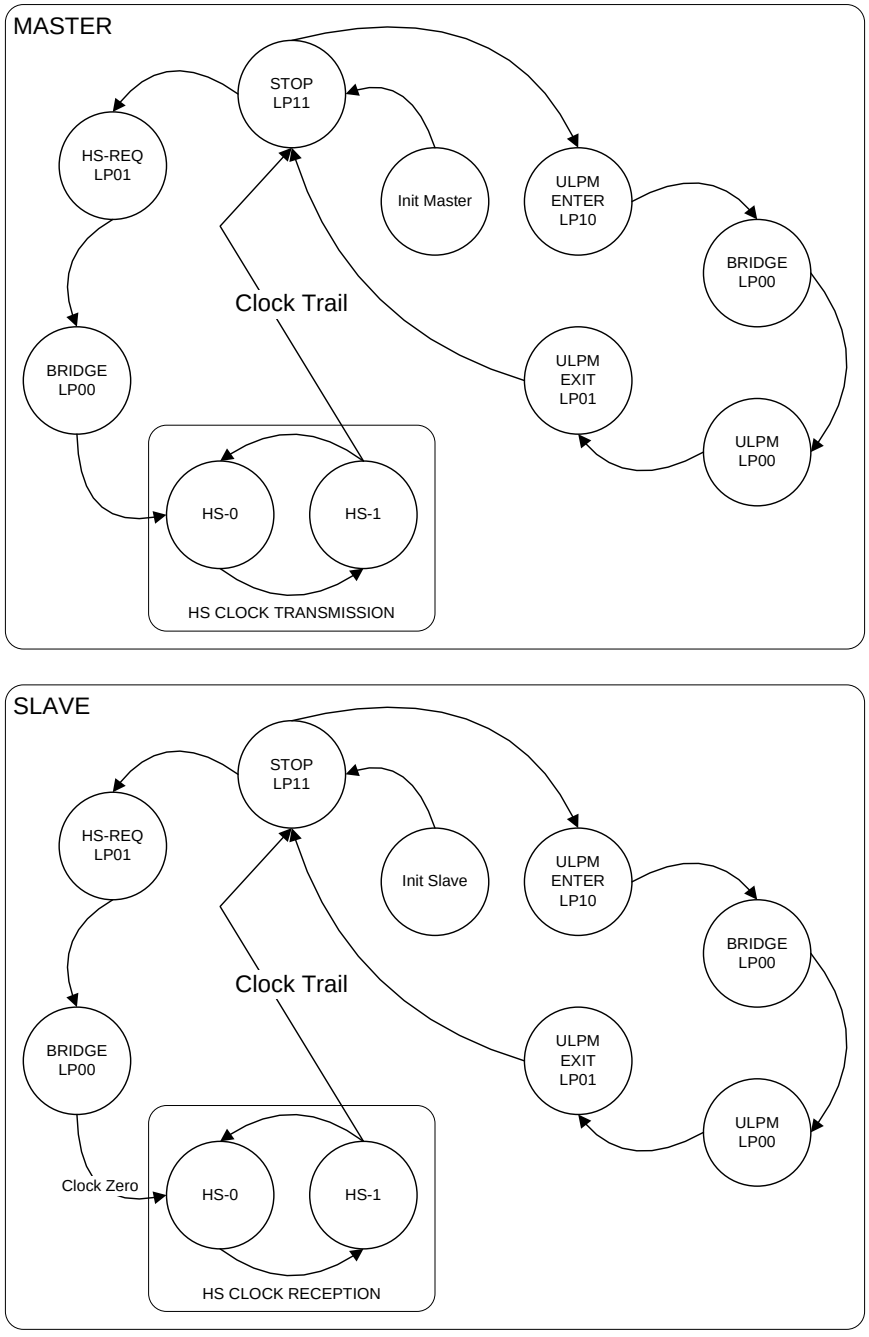


Figure 25 Clock Lane Module Flow Diagram

6 Fault Detection

There are three different mechanisms to detect malfunctioning of the link. Bus contention and error detection functions are contained within the D-PHY. These functions should detect many typical faults. However, some faults cannot be detected within the D-PHY and require a protocol-level solution. Therefore, the third detection mechanism is a set of application specific watchdog timers.

6.1 Contention Detection

This section is important for bi-directional Lanes and Lanes supporting Escape mode. It has no impact on Unidirectional Lanes without Escape mode functionality.

If a bi-directional Lane Module and a Unidirectional Module are combined in one Lane, only unidirectional functionality is available. Because in this case the additional functionality of one PHY Module cannot be reliably controlled from the limited functionality PHY side, the bi-directional features of the bi-directional Module shall be safely disabled. Otherwise in some cases deadlock may occur which can only be resolved with a system power-down and re-initialization procedure.

During normal operation one and only one side of a link shall drive a Lane at any given time except for certain transition periods. Due to errors or system malfunction a Lane may end up in an undesirable state, where the Lane is driven from two sides or not driven at all. This condition eventually results in a state conflict and is called Contention.

The D-PHY module includes contention detection functions that attempt to detect two conditions:

- Modules on both sides of the same line drive opposite LP levels against each other. This implies incorrect signal settling levels. The Contention Detector (LP-CD) specifications ensure that at least one side detects the conflict.
- The Module at one side drives LP-high while the other side drives HS-low on the same Line. This shall be detected at the LP transmitting side.

These cases are detected by the combination of LP-CD and LP-RX functions. The result is checked at the end of every Low-Power bit period when the signals are optimally settled. Details on Contention Detector specifications can be found in section 8.

After contention has been detected the Protocol shall take proper measures to resolve the situation.

6.2 Sequence Error Detection

If for any reason the Lane signal is corrupted the receiving PHY may detect signal sequence errors. Errors detected inside the PHY should be communicated to the Protocol via the PPI. This kind of Error detection is optional, but strongly recommended as it enhances reliability. The following sequence errors can be distinguished:

- SoT Error
- SoT Sync Error
- EoT Sync Error
- Escape Entry Command Error
- LP Transmission Sync Error
- False Control Error

827 ### 6.2.1 SoT Error

828 The Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error and
829 some multi-bit errors. Therefore, the synchronization may be usable, but confidence in the payload data is
830 lower. If this situation occurs this shall be communicated to the Protocol with a SoT Error.

831 ### 6.2.2 SoT Sync Error

832 If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected the SoT
833 Sync Error is set.

834 ### 6.2.3 EoT Sync Error

835 The EoT Sync Error signal shall be set if it is detected that the last bit of a transmission does not match a
836 byte boundary.

837 ### 6.2.4 Escape Mode Entry Command Error

838 If the receiving Lane Module does not recognize the received Entry Command for Escape mode it shall set
839 an Escape Mode Entry Command Error.

840 ### 6.2.5 LP Transmission Sync Error

841 At the end of a Low-Power Data transmission procedure, if data is not synchronized to a Byte boundary the
842 Escape Sync Error signal is set.

843 ### 6.2.6 False Control Error

844 If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape or Turnaround sequence, the PHY
845 sets the False Control Error signal. This is also set if a HS-Rqst (LP-01) is not correctly followed by a
846 Bridge (LP-00).

847 ## 6.3 Protocol Watchdog Timers

848 It is not possible for the PHY to detect all fault cases. Therefore, additional protocol-level time-out
849 mechanisms are necessary in order to limit the maximum duration of certain modes and states.

850 ### 6.3.1 HS RX Timeout

851 In HS RX mode if no EoT is received within a certain period the protocol shall time-out. The timeout
852 period can be protocol specific. While recommended for all links, HS RX Timeout is only required for bi-
853 directional links and unidirectional Links with Escape mode.

854 ### 6.3.2 HS TX Timeout

855 The maximum transmission length in HS TX is bounded. The timeout period is protocol specific. While
856 recommended for all links, HS TX Timeout is only required for bi-directional links and unidirectional
857 Links with Escape mode.

6.3.3 Escape Mode Timeout

A device may timeout during Escape mode. The timeout should be greater than the Escape mode Silence Limit of the other device. The timeout period is protocol specific.

6.3.4 Escape Mode Silence Timeout

A device may have a bounded length for LP TX-00 during Escape mode, after which the other device may timeout. The timeout period is protocol specific. For example, a display module should have an Escape Mode Silence Limit, after which the host processor can timeout.

6.3.5 Turnaround Errors

A Turnaround procedure always starts from a Stop State. The procedure begins with Turn State (LP-10), followed by a Bridge State (LP-00) during which drive sides are swapped. It is finalized by the response including a Turn State followed by a Stop State driven from the other side. If the actual sequence of events violates the normal Turnaround procedure a "False Control Error" is flagged to the Protocol. See section 6.2.6. The Turn State response serves as an acknowledgement for the correctly completed Turnaround procedure. If no acknowledgement is observed within a certain time period the Protocol will time-out and take appropriate action. This period shall be larger than the maximum possible Turnaround time for a particular system. There is no time-out for this condition in the PHY.

7 Interconnect and Physical Link

The Interconnect connecting Transmitter and Receiver carries all signals used in the D-PHY communication. This includes both high-speed, low-voltage signaling I/O technology and low-speed, low-power signaling for control functions. For this reason, the physical link shall be implemented by means of balanced, differential, point-to-point transmission lines referenced to ground. The total link may consist of several cascaded transmission line segments, such as, printed circuit boards, Flex-foils, and cable connections.

Figure 26 Point-to-point Link

7.1 Link Configuration

The complete physical connection consists a Transmitter (TX), and/or Receiver (RX) at each side, with some Transmission-Line-Interconnect-Structure (TLIS) in between. The overall link performance is therefore determined by the combination of these three elements. The split between these elements is defined to be on the Module (IC) pins. This section defines both the required performance of the Transmission-Line-Interconnect-Structure for the signal routing as well as the I/O-cell Reflection properties of TX and RX. This way the correct overall operation of the link can be ensured.

With respect to physical dimensions, the Transmission-Line-Interconnect-Structure will typically be the largest part. Besides printed circuit board and Flex-foil traces, this may also includes elements such as vias and connectors.

7.2 Boundary Conditions

The reference characteristic impedance level is 100 Ohm differential, 50 Ohm single-ended per wire, and 25 Ohm common-mode for both wires together. The 50 Ohm impedance level for single-ended operation is also convenient for test and characterization purposes.

This typical impedance level is required for all three parts of the link: TX, TLIS, and RX. The tolerances for characteristic impedances of the interconnect and the tolerance on line termination impedances for TX and RX are specified by means of S-parameter templates over the whole operating frequency range.

The differential channel is also used for LP single-ended signaling. Therefore, it is strongly recommended to apply only very loosely coupled differential transmission lines.

The flight time for signals across interconnect shall not exceed 2 ns.

7.3 Definitions

The frequency ‘fh’ is the fundamental frequency of the transmission for a certain bit-rate. For example for 600Mb/s fh is 300MHz.

The frequency ‘fh_{MAX}’ is a device specification and indicates the maximum supported fh for a particular device.

The frequency '$f_{LP,MAX}$' is the maximum toggle frequency for Low-Power mode.

RF interference frequencies are denoted by 'f_{INT}', where $f_{INT,MIN}$ defines the lower bound for the band of relevant RF interferers.

The frequency f_{MAX} is defined by the maximum of $(1/3t_{F,MIN}, 1/3t_{R,MIN})$, where t_R and t_F are the rise and fall times of the high speed signaling. These parameters are specified in section 8. For the fastest allowed D-PHY signals f_{MAX} is 2.2GHz.

7.4 S-parameters Specification

The required performance of the physical connection is specified by means of S-parameter requirements for TX, TLIS, and RX, for TLIS by mixed-mode 4-port parameters, and for RX and TX by mixed-mode reflection (return loss) parameters. The S-parameter limits are defined over the whole operating frequency range by means of templates.

The differential transmission properties are most relevant and therefore this specification uses mixed-mode parameters. As the performance needs depend on the targeted bit-rates, most S-parameter requirements are specified on a normalized frequency axis with respect to bit-rate. Only the parameters that are important for the suppression of external (RF) interference are specified on an absolute frequency scale. This scale extends up to f_{MAX}. Beyond this frequency the circuitry itself shall suppress these high-frequency interference signals sufficiently.

Only the overall performance of the TLIS and the maximum reflection of RX and TX are specified. This fully specifies the signal behavior at the RX/TX-module pins. The subdivision of losses, reflections and mode-conversion budget to individual physical fractions of the TLIS is left to the system designer. Annex B includes some rules of thumb for system design and signal routing guidelines.

7.5 Characterization Conditions

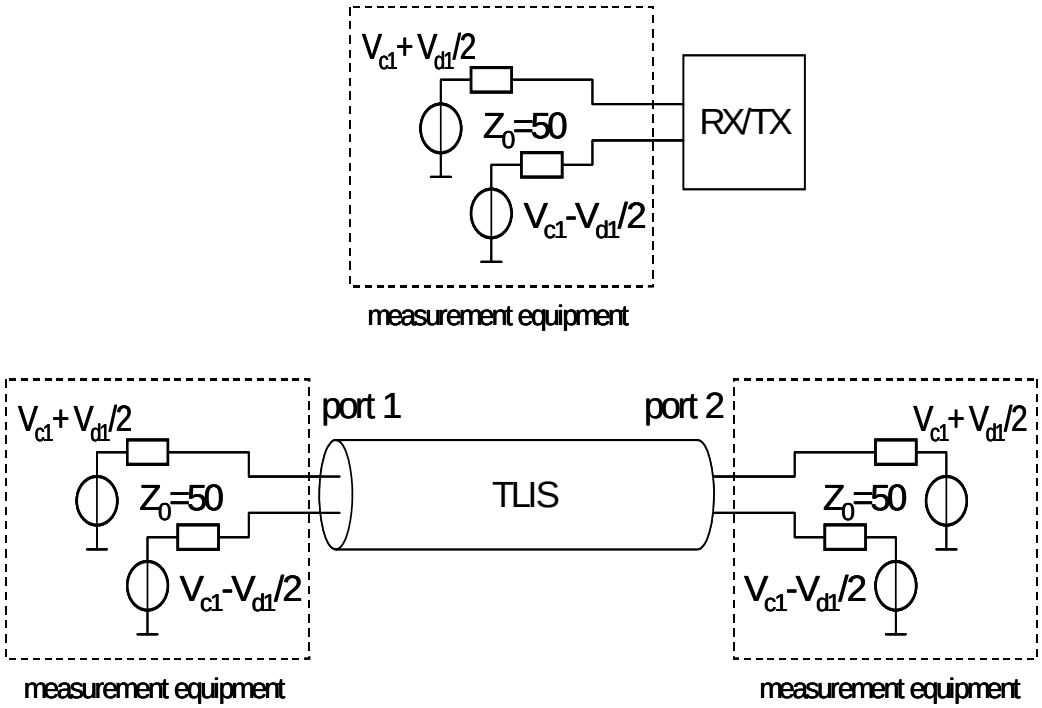


Figure 27 Set-up for S-parameter characterization of RX,TX, and TLIS

All S-parameter definitions are based on a 50 Ohm impedance reference level. The characterization can be done with a measurement system, as shown in Figure 27.

The syntax of S-parameters is S[measured-mode][driven-mode][measured-port][driven-port]. Examples: Sdd21of TLIS is the differential signal at port 2 due to a differential signal driven at port 1; Sdc22 is the measured differential reflected signal at port 2 due to a common signal driven at port 2.

7.6 Interconnect Specifications

The Transmission-Line Signal-Routing (TLSR) is specified by means of mixed-mode 4-port S-parameter behavior templates over the frequency range. This includes the differential and common-mode, insertion and return losses, and furthermore mode-conversion limitations.

7.6.1 Differential Characteristics

The differential transfer behavior (insertion loss) of the TLIS is specified by the Sdd21 and Sdd12 template as shown in Figure 28, where $i \neq j$.

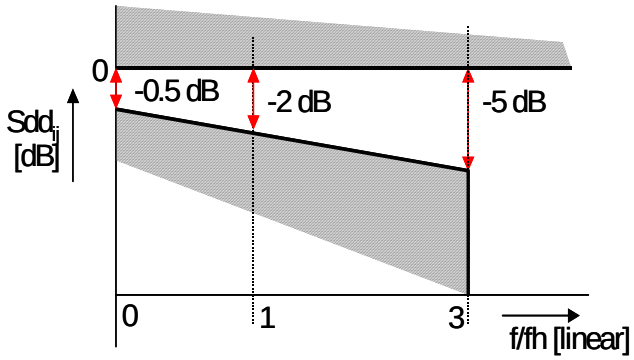


Figure 28 Template for Differential Insertion Losses

The differential reflection for both ports of the TLIS should be less than –20dB for frequencies below $2*f_{LP,MAX}$ and less than –9dB for all frequencies from $8*f_{LP,MAX}$ up to f_{MAX}. See Figure 29.

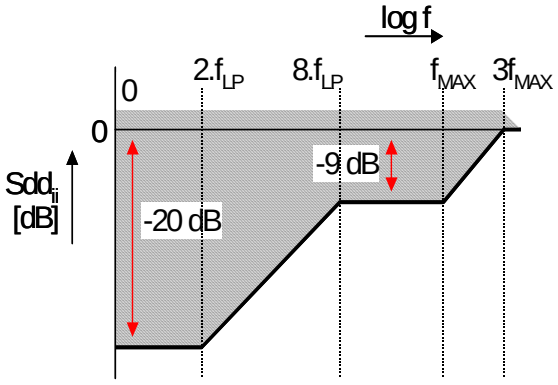


Figure 29 Template for Differential Reflection at Both Ports

7.6.2 Common-Mode Characteristics

The common-mode insertion loss is implicitly specified by means of the differential insertion loss and the Intra-lane cross coupling. The requirements for common-mode insertion loss are therefore equal to the differential requirements.

The common-mode reflection coefficients Scc11 and Scc22 should both be below –20 dB up to $2*f_{LP,MAX}$ and –9 dB for $8*f_{LP,MAX}$ up to f_{MAX}, similar to the differential requirements as depicted in Figure 30.

7.6.3 Intra-Lane Cross-Coupling

The two lines applied as differential pair during HS transmission are also used individually for single-ended signaling during low-power mode. Therefore, the coupling between the two wires shall be restricted in order to limit single-ended cross coupling. This is defined by the difference of the S-parameters: Scc21-Sdd21 (or Scc12-Sdd12). This difference shall not exceed –20dB for any frequency up to $10*f_{LP,MAX}$.

7.6.4 Mode-Conversion Limits

All mixed-mode 4-port S-parameters regarding differential to common-mode conversion and vice-versa shall not exceed –26 dB below f_{MAX}. This includes Sdc12, Scd21, Scd12, Sdc21, Scd11, Sdc11, Scd22, and Sdc22.

7.6.5 Inter-Lane Cross-Coupling

The cross coupling between clock and data pair(s), and between data pairs for multi-lane configurations shall be less than –26 dB up to f_{MAX}.

7.7 Driver & Receiver Characteristics

Besides the TLIS the link consists of two RX-TX modules, one at each side. This paragraph specifies the reflection behavior (return loss) of these RX-TX modules in HS-mode. The signaling characteristics of all possible functional blocks inside the RX-TX modules can be found in the Electrical section. The low-frequency tolerance on line terminations at Transmitter and Receiver is 25% (80-125Ohm).

7.7.1 Differential Characteristics

The differential reflection of a Lane Module in High-Speed TX or RX mode is specified by the template shown in Figure 30.

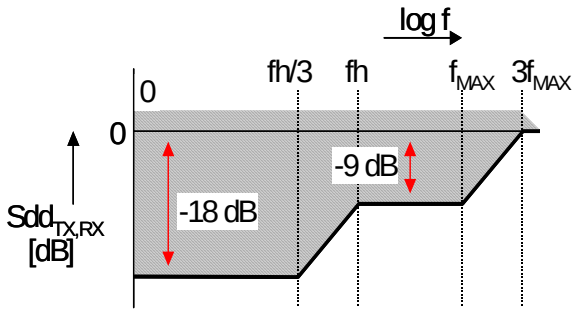


Figure 30 Differential Reflection Template for Lane Modules

7.7.2 Common-Mode Characteristics

The common-mode return loss specification is different for a high-speed TX and RX mode, because the RX is not DC terminated to ground. For an active TX the common-mode reflection shall be less than –6dB over the whole frequency range up to f_{MAX}. For an RX reflection shall be less than –6 dB for the frequency range $f_{INT,MIN}$ – f_{MAX}. Assuming a high DC common-mode impedance this implies a sufficiently large capacitor at the termination center tap. The minimum value allows integration. While the common-mode termination is especially important for reduced influence of RF interferers the RX requirement limits reflection for the most relevant frequency band.

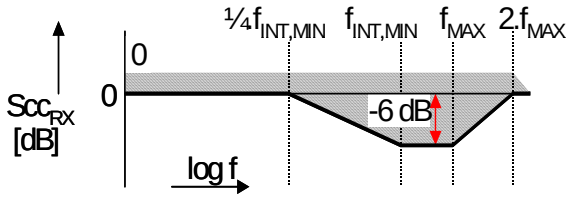


Figure 31 Template for RX Common-Mode Return Loss

7.7.3 Mode-Conversion Limits

The differential to common-mode conversion limits of TX and RX are defined at -26dB up to f_{MAX}.

8 Electrical Characteristics

A PHY may contain the following electrical functions: a High-Speed Transmitter (HS-TX), a High-Speed Receiver (HS-RX), a Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and a Low-Power Contention Detector (LP-CD). A PHY does not need to contain all electrical functions but only the functions, which are required for a certain PHY configuration. The required functions for each configuration are specified in section 4. All electrical functions included in any PHY shall meet the specifications in this section. Figure 32 shows the complete set of electrical functions required for a fully featured PHY transceiver.

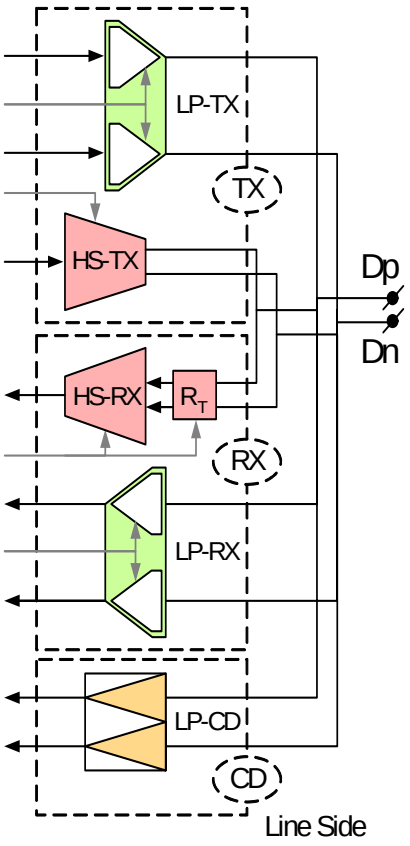


Figure 32 Electrical Functions of a Fully Featured D-PHY Transceiver

The HS transmitter and HS receiver are used for the transmission of the HS data and clock signals. The HS transmitter and receiver utilize low-voltage differential signaling for signal transmission. The HS receiver contains a switchable parallel termination.

The LP transmitter and LP receiver serve as a low power signaling mechanism. The LP transmitter is a push-pull driver and the LP receiver is an un-terminated, single-ended receiver.

The signal levels are different for differential HS mode and single-ended LP mode. Figure 33 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detect low on HS signals.

All absolute voltage levels are relative to the ground voltage at the transmit side.

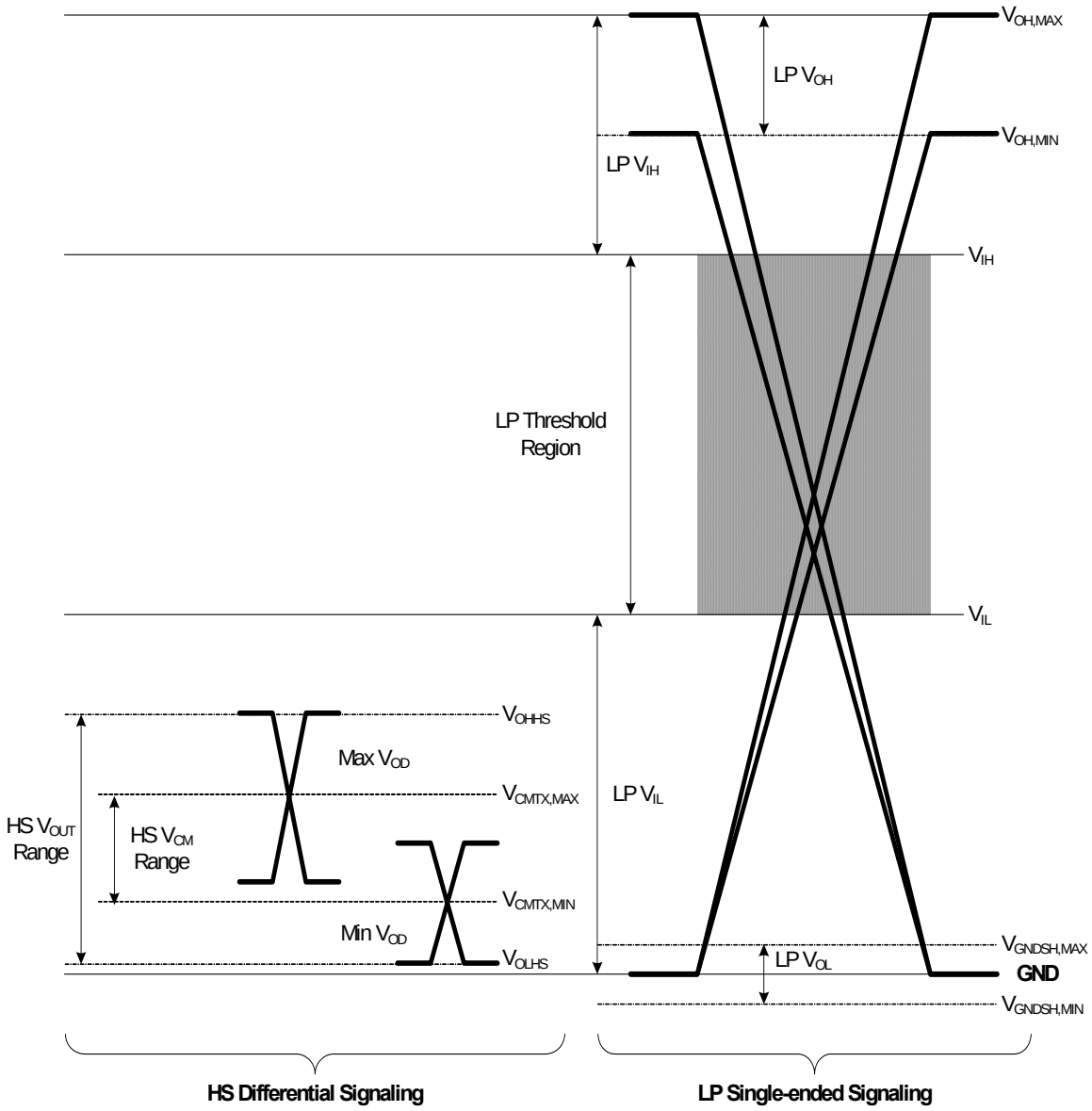


Figure 33 D-PHY Signaling Levels

A Lane switches between Low-Power and High-Speed mode during normal operation. Bidirectional Lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enable and disable events shall not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes shall be smooth to always ensure a proper detection of the Line signals.

8.1 Driver Characteristics

8.1.1 High-Speed Transmitter

A HS differential signal driven on the Dp and Dn pins is generated by a differential output driver. For reference, Dp is considered as the positive side and Dn as the negative side. The Lane state is called Differential-1 (HS-1) when the potential on Dp is higher than the potential of Dn. The Lane state is called

Differential-0 (HS-0), when the potential on Dp is lower than the potential of Dn. Figure 34 shows an example implementation of a HS transmitter.

Note, this section uses Dp and Dn to reference the pins of a Lane Module regardless of whether the pins belong to a Clock Lane module or a Data Lane module.

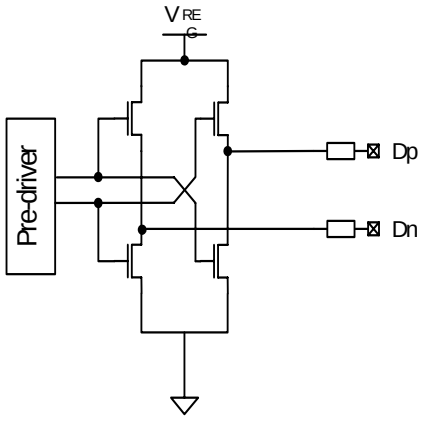


Figure 34 Example HS Transmitter

The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

The output voltages V_{DP} and V_{DN} at the Dp and Dn pins shall not exceed the high-speed output high voltage V_{OHHS}. The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

V_{OD} and V_{CMTX} are graphically shown in Figure 35 for ideal HS signals. Figure 35 shows single-ended HS signals with the possible kinds of distortion of the differential output and common-mode voltages. V_{OD} and V_{CMTX} may be slightly different for driving a Differential-1 or a Differential-0 on the pins. The output differential voltage mismatch ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$. This is expressed by:

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

If $V_{CMTX(1)}$ and $V_{CMTX(0)}$ are the common-mode voltages for static Differential-1 and Differential-0 states respectively, then the common-mode reference voltage is defined by:

$$V_{CMTX,REF} = \frac{V_{CMTX(1)} + V_{CMTX(0)}}{2}$$

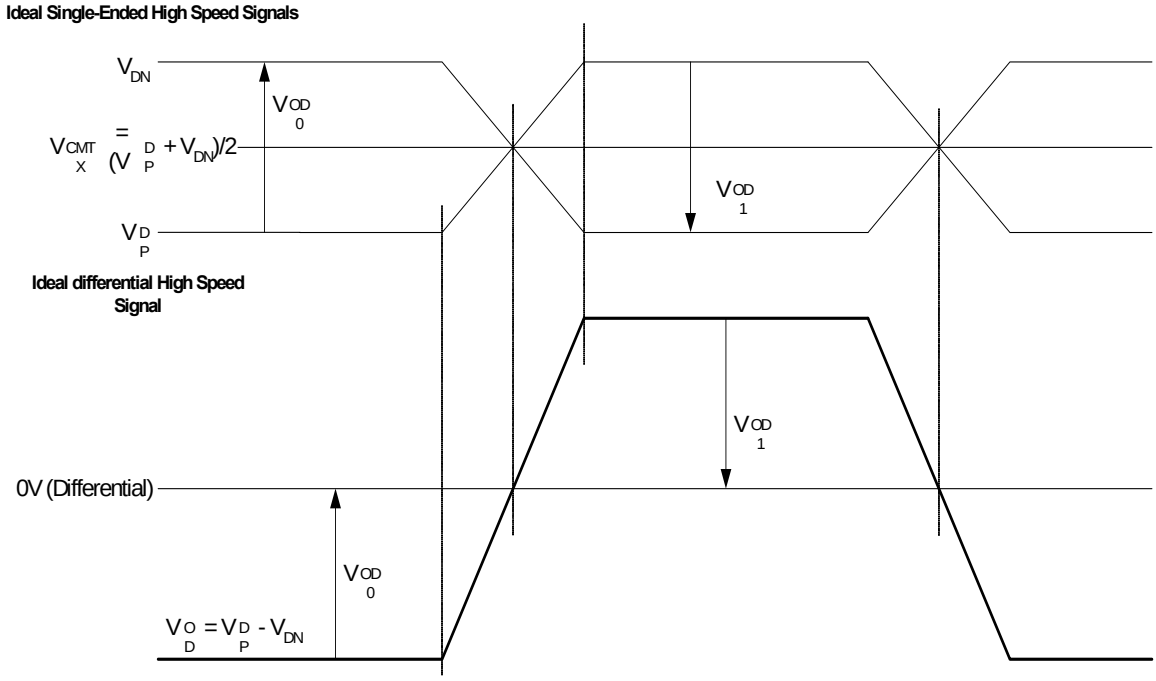
The transient common-mode voltage variation is defined by:

1045 $$\Delta V_{CMTX}(t) = V_{CMTX}(t) - V_{CMTX,REF}$$

1046 The static common-mode voltage mismatch between the Differential-1 and Differential-0 state is given by:

1047 $$\Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

1048 It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and
1049 optimize signal integrity. A test circuit for the measurement of V_{OD} and V_{CMTX} is shown in Figure 36.



1050

1051 **Figure 35 Ideal Single-ended and Resulting Differential HS Signals**

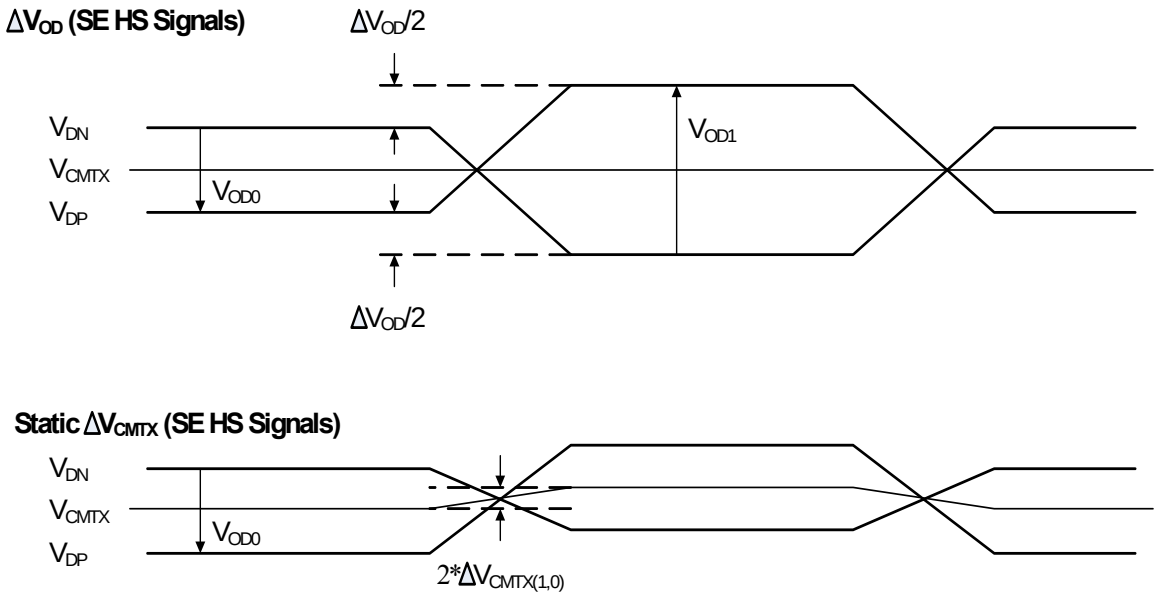


Figure 36 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

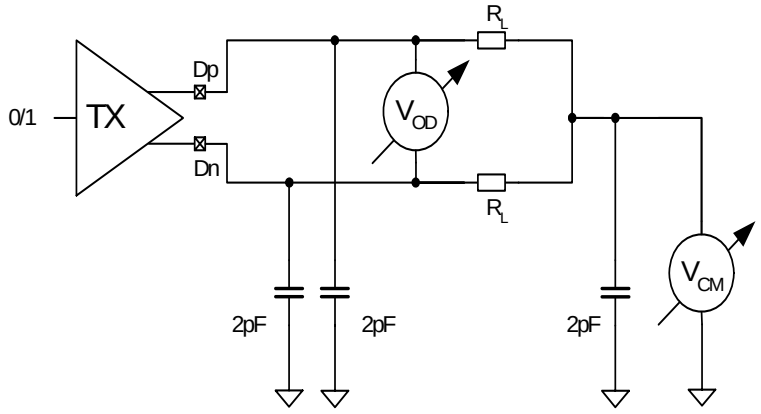


Figure 37 Example Circuit for V_{CMTX} and V_{OD} Measurements

The single-ended output impedance of the transmitter at both the Dp and Dn pins is denoted by Z_{OS}. ΔZ_{OS} is the mismatch of the single ended output impedances at the Dp and Dn pins, denoted by Z_{OSDP} and Z_{OSDN} respectively. This mismatch is defined as the ratio of the absolute value of the difference of Z_{OSDP} and Z_{OSDN} and the average of those impedances:

$$\Delta Z_{OS} = 2\frac{\left|Z_{OSDP} - Z_{OSDN}\right|}{Z_{OSDP} + Z_{OSDN}}$$

The output impedance Z_{OS} and the output impedance mismatch ΔZ_{OS} shall be compliant with Table 17 for both the Differential-0 and Differential-1 states for all allowed loading conditions. It is recommended the design keep the output impedance during state transitions as close as possible to the steady state value. The output impedance Z_{OS} can be determined by injecting an AC current into the Dp and Dn pins and measuring the peak-to-peak voltage amplitude. An example circuit for such a measurement is shown in Figure 38, where R_L are load resistors and $V_{TEST,PP}$ is a test signal applied at the common-mode node via an AC coupling capacitor C_{AC}. The frequency of the test signal is f_{TEST}.

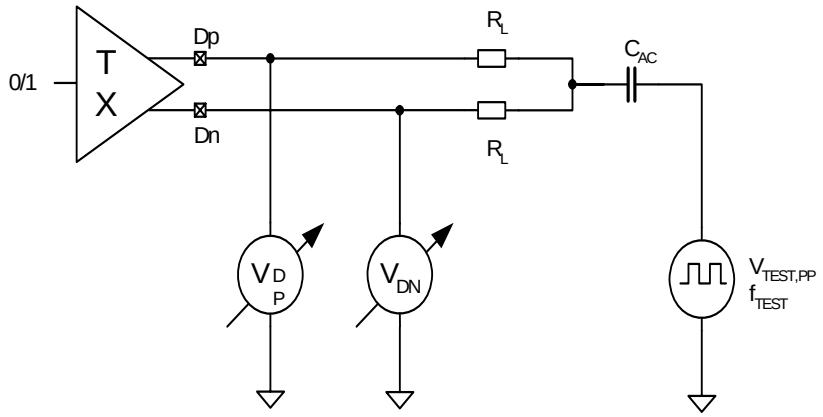


Figure 38 Example Circuit for the Measurement of Output Impedance

Assuming negligible effect of the coupling capacitor, the example circuit gives the following relation between peak-to-peak pin voltage $V_{PIN,PP}$ and Z_{OS}. This equation can be used for both Dn and Dp pins individually.

$$Z_{OS} = \frac{V_{PIN,PP} \cdot R_L}{V_{TEST,PP} - V_{PIN,PP}}$$

Table 16 shows the minimum, nominal, and maximum values of $V_{PIN,PP}$, for R_L values of 40 Ω, 50 Ω, and 62.5 Ω and a test signal peak-to-peak voltage $V_{TEST,PP}$ of 100 mV. These minimum, nominal, and maximum values of $V_{PIN,PP}$ for each value of R_L correspond to the minimum, nominal, and maximum allowed output impedances Z_{OS}, respectively.

Table 16 $V_{PIN,PP}$ for Characteristic Load Resistances R_L

R_L	$V_{PIN,PP,MIN}$ (Z_{OS}=40 Ω)	$V_{PIN,PP,NOM}$ (Z_{OS}=50 Ω)	$V_{PIN,PP,MAX}$ (Z_{OS}=62.5 Ω)
40 Ω	50 mV	56 mV	61 mV
50 Ω	44 mV	50 mV	56 mV
62.5 Ω	39 mV	44 mV	50 mV

The rise and fall times t_R and t_F are defined as the transition time between 20% and 80% of the full HS signal swing while the driver is loaded with a nominal differential load Z_{ID} across the output pins. The specifications for TX common-mode return loss and the TX differential mode return loss can be found in section 7.

It is recommended that a high-speed driver directly terminated at its pins should not generate any overshoot in order to minimize EMI.

Table 17 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV	1
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV	1
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

Notes:

1. Value when driving into load impedance anywhere in the Z_{ID} range.

Table 18 HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 50MHz			15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time	150		$0.3UI_{NOM}$	ps	1

Notes:

1. UI_{NOM} is the long term average Unit Interval: See section 9.

8.1.2 Low Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low. An example of a LP transmitter is shown in Figure 39.

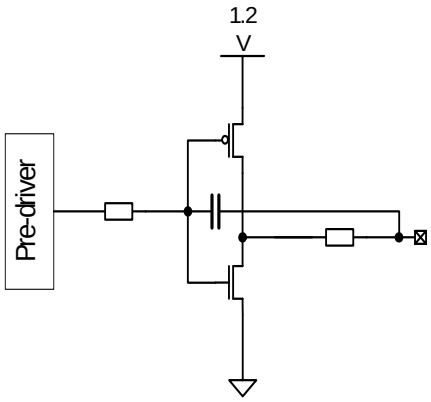


Figure 39 Example LP Transmitter

V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded. The LP transmitter shall not drive the pad pin potential statically beyond the maximum value of V_{OH}. The pull-up and pull-down output impedances of LP transmitters shall be as described in Figure 40 and Figure 41, respectively. The circuit for measuring V_{OL} and V_{OH} is shown in Figure 42.

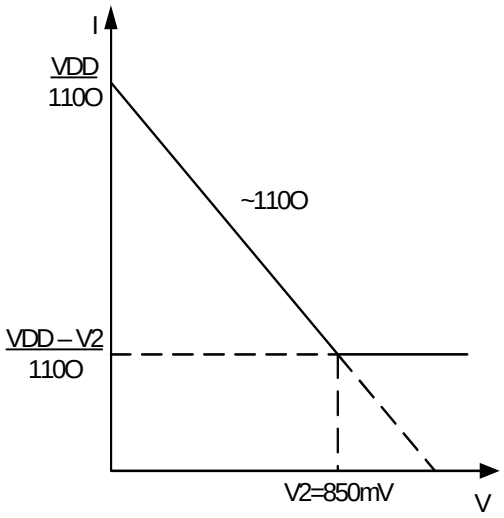


Figure 40 V-I Characteristic for LP Transmitter Driving Logic High

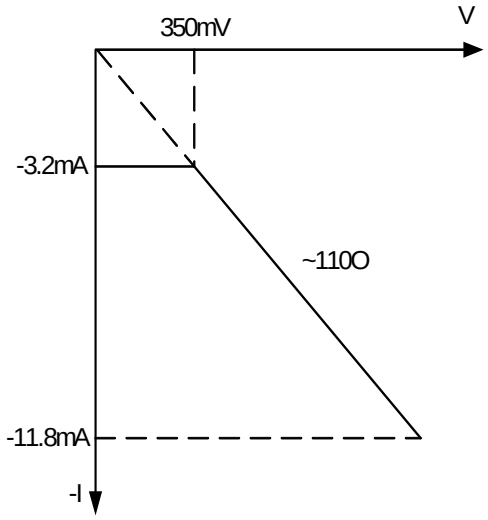


Figure 41 V-I Characteristic for LP Transmitter Driving Logic Low

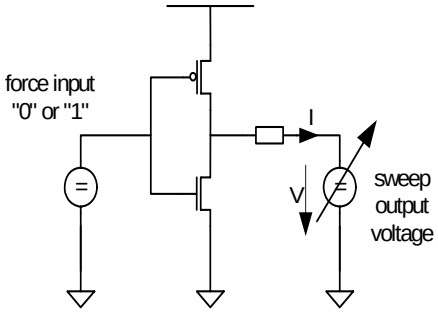


Figure 42 LP Transmitter V-I Characteristic Measurement Setup

The impedance Z_{OLP} is defined by:

$$Z_{OLP} = \left| \frac{V_{THEVENIN} - V_{PIN}}{I_{OUT}} \right|$$

ΔZ_{OLP} is the relative mismatch of the output impedances $Z_{OLP,DP}$ and $Z_{OLP,DN}$ where $Z_{OLP,DP}$ and $Z_{OLP,DN}$ are the output impedances of the LP transmitters driving the Dp and Dn pins, respectively. ΔZ_{OLP} is defined as the ratio of the absolute difference of the output impedances $Z_{OLP,DP}$ and $Z_{OLP,DN}$ and the average of these impedances:

$$\Delta Z_{OLP} = 2 \frac{\left| Z_{OLP,DP} - Z_{OLP,DN} \right|}{Z_{OLP,DP} + Z_{OL,DN}}$$

The LP drivers on Dp and Dn are either driving the same or opposite levels. The mismatch for both cases is denoted by $\Delta Z_{OLP(00,11)}$ and $\Delta Z_{OLP(01,10)}$, respectively.

The times t_{RLP} and t_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage

over time. The slew rate specification shall be met for the 15%-85% range while driving a capacitive load C_{LOAD}. The intention of specifying a maximum slew rate value is to limit EMI. Rather than specifying a minimum slew rate value, maximum rise and fall times are specified, which guarantees that timing requirements are met.

During End-of-Transmission the capacitive load of the LP transmitters can be significantly higher due to the additional capacitance on the common-mode centre tap of the RX termination. With a common-mode termination capacitance C_{CM} the rise time during EoT is specified by t_{REOT}

Table 19 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OL}	Thevenin output low level	-50		50	mV	
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2
$\Delta Z_{OLP(01,10)}$	Dp-Dn output impedance mismatch driving opposite level			20	%	
$\Delta Z_{OLP(00,11)}$	Dp-Dn Output impedance mismatch driving the same level			5	%	

Notes:

1. See Figure 40 and Figure 41.
2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 20 LP Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t_{RLP}/t_{FLP}	15%-85% rise time and fall time			25	ns	1, 5
t_{REOT}	30%-85%			35	ns	4, 5, 6
$\delta V/\delta t_{SR}$	Slew rate			120	mV/ns	1, 2, 3
C_{LOAD}	Load capacitance	0		70	pF	

Notes:

1. When the output is loaded with a capacitive load C_{LOAD}.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50 mV segment of the output signal transition.
4. The rise-time of t_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

5. For capacitive loads from 0-70pF

6. With an additional load capacitance C_{CM} between 0-60pF on the termination centre tap at RX side of the link

8.2 Receiver Characteristics

8.2.1 High Speed Receiver

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. A simplified diagram of an example implementation using a PMOS input stage is shown in Figure 43.

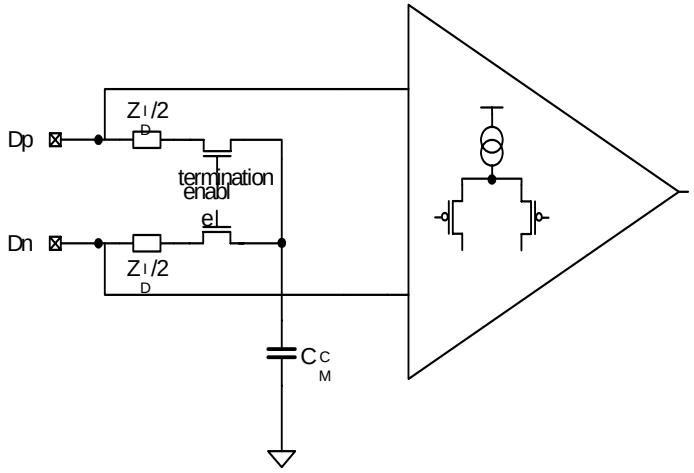


Figure 43 HS Receiver Implementation Example

The differential input high and low threshold voltages of the HS receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{CMRXDC} is the differential input common mode voltage. The HS receiver shall be able to detect differential signals at its Dp and Dn input signal pins when both signal voltages, V_{DP} and V_{DN}, are within the common mode voltage range and if the voltage difference of V_{DP} and V_{DN} exceeds either V_{IDTH} or V_{IDTL}.

During operation of the HS receiver, termination impedance Z_{ID} is required between the Dp and Dn pins of the HS receiver. Z_{ID} shall be disabled when the module is not in the HS receive mode. C_{CM} is the common mode AC termination, which ensures a proper termination of the receiver at higher frequencies.

The RX common-mode return loss and the RX differential mode return loss are specified in section 7. For higher data rates a capacitance C_{CM} is needed at the termination centre tap in order to meet the common-mode reflection requirements.

Table 21 HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{ILHS}	Single-ended input low voltage	-40			mV	1

Parameter	Description	Min	Nom	Max	Units	Note
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{CMRXDC}	Common-mode voltage HS receive mode	70		330	mV	1,2
Z_{ID}	Differential input impedance	80		125	Ω	

Notes:

1. Excluding possible additional RF interference of 200mVPP beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 22 HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz			200	mV_{PP}	2, 4
$\Delta V_{CMRX(LF)}$	Common mode interference 50MHz – 450MHz	-50		50	mV_{PP}	1, 4
C_{CM}	Common mode termination			60	pF	3

Notes:

1. Excluding ‘static’ ground shift of 50mV
2. Common mode variation added to any valid DC common mode level. ΔV_{CMRX} amplitude is defined at the output of a sinusoidal generator loaded by the reference impedance [50 Ohms].
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification
4. V_{PP} is the voltage difference compared to the DC average common-mode potential.

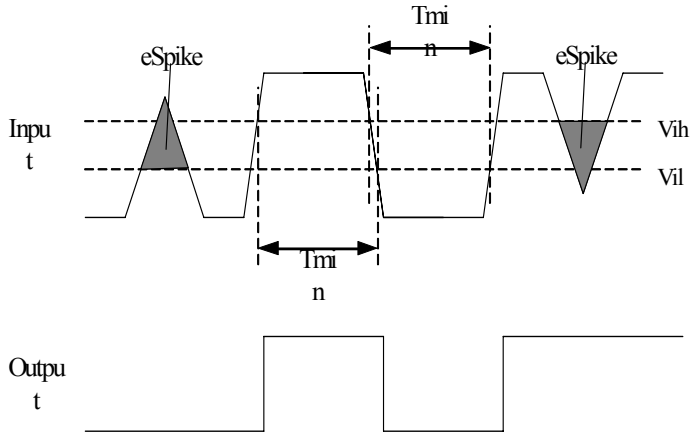
8.2.2 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF-interference. It is recommended the implementer optimize the LP receiver design for low power.

The input low-level voltage, V_{IL}, is the voltage at which the receiver is required to detect a low state in the input signal. V_{IL} is larger than the maximum single-ended Line voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling. The input high-level voltage, V_{IH}, is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}.

The LP receiver shall reject any input glitch when the glitch is smaller than e_{SPIKE}. The filter shall allow pulses wider than T_{MIN} to propagate through the LP receiver.

1185 Furthermore, the LP receivers shall be tolerant of super-positioned RF interference on top of the wanted
1186 Line signals. This implies an input signal filter. The LP receiver shall meet all specifications for
1187 interference with amplitude V_{INT} and frequency f_{INT}. The interference shall not cause glitches or incorrect
1188 operation during signal transitions.



1189

1190 **Figure 44 Input Glitch Rejection of Low-Power Receivers**

1191 **Table 23 LP Receiver DC specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IL}	Logic 0 input threshold			550	mV	
V_{IH}	Logic 1 input threshold	880			mV	
V_{HYST}	Input hysteresis	25			mV	

1192 **Table 24 LP Receiver AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1, 2
T_{MIN}	Minimum pulse width response	50			ns	3
V_{INT}	Peak-to-peak interference voltage			400	mV	
f_{INT}	Interference frequency	450			MHz	

1193 Notes:

1194 1. An impulse less than this will not change the receiver state.

1195 2. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

1196 3. An input pulse greater than this shall toggle the output.

8.3 Line Contention Detection

Contention can be inferred from any of the following conditions:

- An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL}. Refer to Table 23.
- An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{ILF}.

The LP receiver can detect the first condition. The second condition requires an additional contention detector that can detect the input low fault threshold voltage V_{ILF} (LP-CD). The contention voltage V_{ILF} is shown along with the normal signaling voltages in Figure 45. Both contention detectors shall use sufficiently filtered input signals to avoid false triggering on short events.

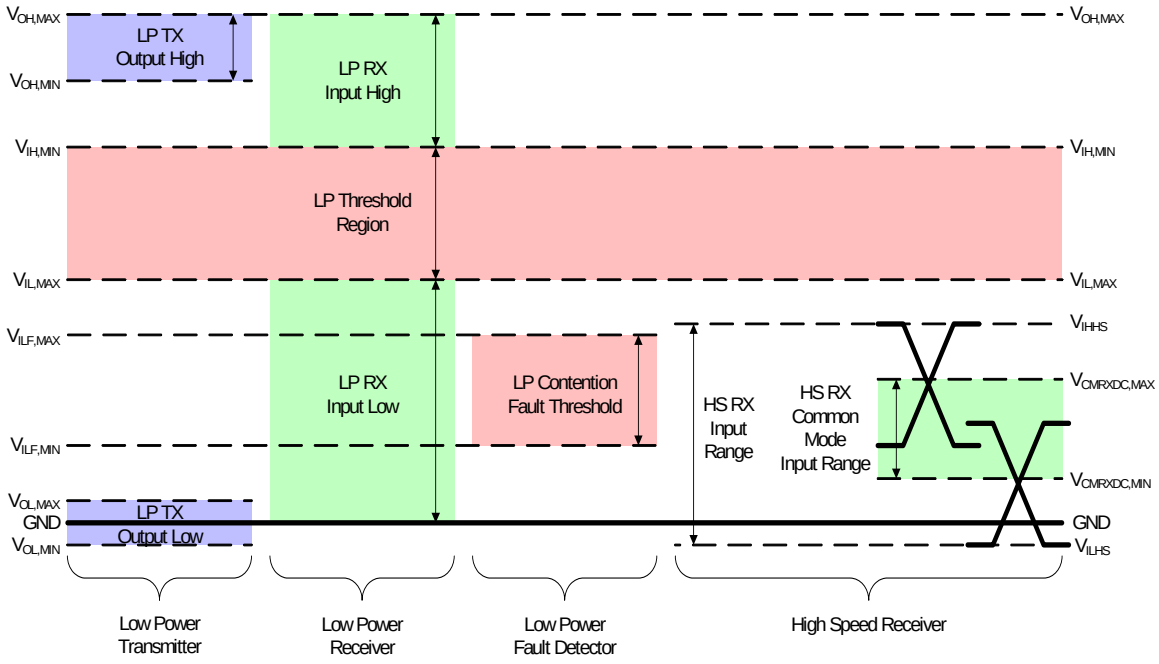


Figure 45 Signaling and Contention Voltage Levels

Table 25 Contention Detector DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{ILF}	Input low fault threshold	200		450	mV	

8.4 Input Characteristics

No structure within the PHY may be damaged when a DC signal that is within the signal voltage range V_I is applied to a pad pin for an indefinite period of time. When the PHY is in the low-power receive mode the pad pin leakage current shall be I_{LEAK} when the pad signal voltage is within the signal voltage range of $V_{GNDSH,MIN}$ to $V_{OH,MAX} + V_{GNDSH,MAX}$. The specification of I_{LEAK} assures interoperability of any PHY in the LP mode by restricting the maximum load current of an LP transmitter. An example test circuit for leakage current measurement is shown in Figure 46.

The ground supply voltages shifts between a Master and a Slave shall be less than V_{GNDSH}.

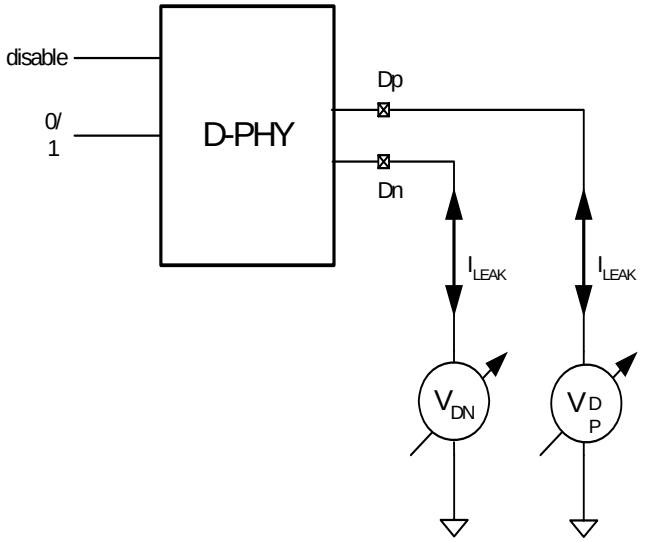


Figure 46 Pin Leakage Measurement Example Circuit

Table 26 Input Characteristic DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_I	Pad signal voltage range	-50		1350	mV	1
I_{LEAK}	Pad pin leakage current	-10		10	µA	2
V_{GNDSH}	Ground shift	-50		50	mV	
$V_{OH(absmax)}$	Maximum transient output voltage level			1.45	V	
$T_{VOH(absmax)}$	Maximum transient time above VOH			20	ns	

Note:

1. The transient voltage range is limited from –300mV to 1600mV
2. When the pad voltage is in the signal voltage range from $V_{GNDSH,MIN}$ to V_{OH} + $V_{GNDSH,MAX}$ and the Lane Module is in LP receive mode.

9 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

This specification allows data transmission at any data bit rate greater than the minimum specified. This data rate maintains a constant long-term average value over a data transmission. It is the intent of this specification that all specified timing values be normalized to the nominal UI of the long-term average data rate.

Figure 47 shows an example PHY configuration including the compliance measurement planes for the specified timings. Note that the effect of signal degradation inside each package due to parasitic effects is included in the timing budget for the transmitter and receiver and is not included in the Interconnect degradation budget. See section 7 for details.

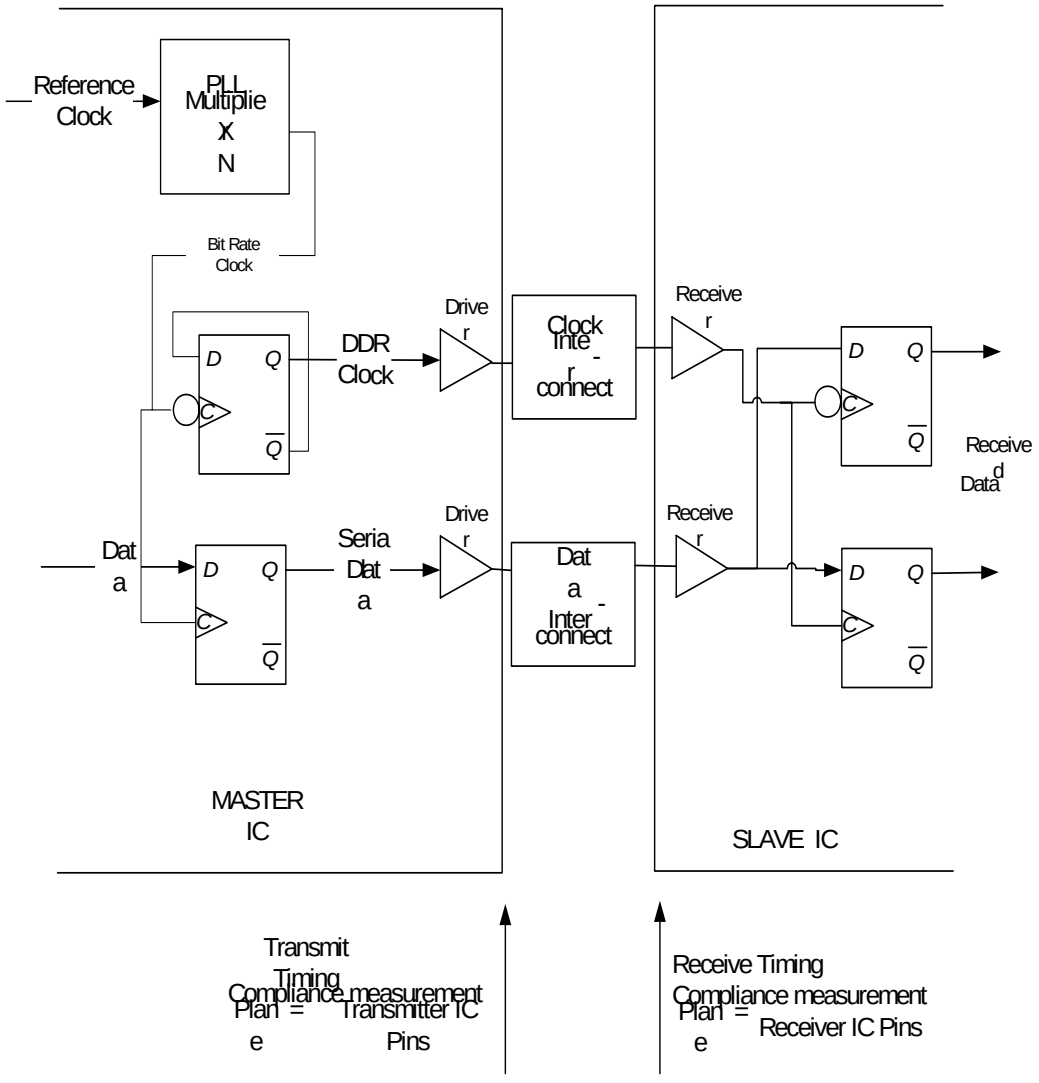


Figure 47 Conceptual D-PHY Data and Clock Timing Compliance Measurement Planes

9.1 High Speed Clock Timing

The Master side of the Link shall send a differential clock to the Slave side to be used for data sampling. This clock is at a fixed nominal frequency and stable for the entire duration of a data transfer. Stability, as defined for this specification, means that all characteristics specified in Table 27 are met. Note that this precludes interrupting the clock for any purpose during the transmission of high-speed data. However, it is the intention of this specification to allow slow variations of instantaneous frequency as long as the resulting signal meets all specified values and relationships with the data signal. Therefore, using a frequency spreading modulation on the clock for purposes of reducing EMI is not precluded.

The DDR [Double Data Rate] Clock signal maintains a quadrature phase relationship to the data signal. Data will be sampled by both the rising and falling edges of the Clock signal. The Clock signal is a differential signal. Use of the term “rising edge” means “rising edge of the signal (CLKp – CLKn) and similarly for “falling edge”. Therefore, the frequency of the Clock signal will be half the desired data rate in bits/second. This relationship is expressed in Figure 48.

Note that the UI indicated in Figure 48 is the instantaneous UI. However, for all specified values with units of UI_{NOM}, the value of UI is 1/[2*Nominal long term average frequency of the DDR Clock]. This is the nominal data, UI_{NOM}. The Clock signal shall have a long term average frequency greater than 40MHz corresponding to a minimum data rate of 80Mbps. A maximum clock frequency is not specified. However, each conforming implementation shall specify a maximum data rate and a corresponding maximum clock frequency, fh_{MAX}. It is assumed that each transmitter, receiver and interconnect combination will have a different maximum effective rate. It is up to the system implementer to determine the maximum operating frequency.

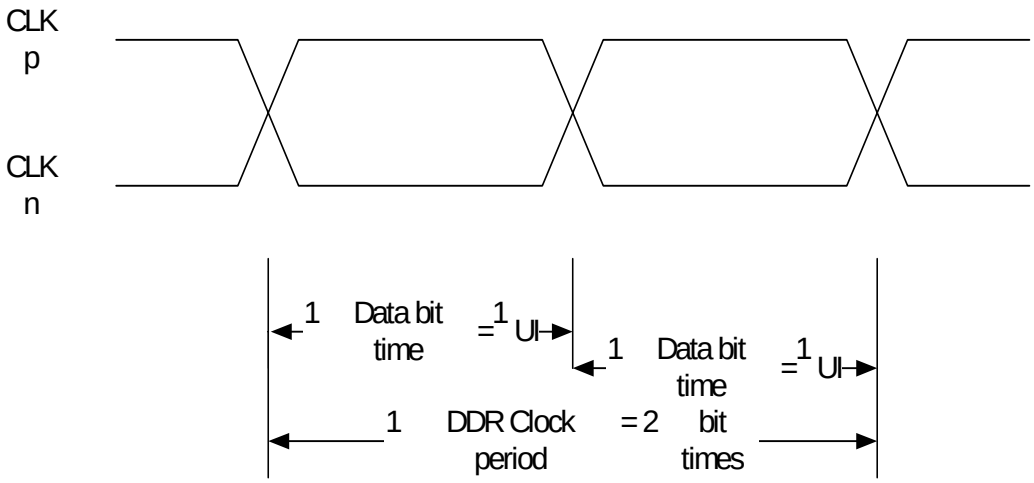


Figure 48 DDR Clock Definition

In order to allow for random frequency variations in the Clock generation circuitry as well as noise-induced variations, a deviation in clock period from one cycle to the next is allowed. As can be seen with reference to Figure 47, the same clock source is used to generate the DDR clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Large instantaneous variations in UI can be accommodated by such a system.

The allowed instantaneous UI variation can cause large instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The specification parameters for the Clock signal are summarized in Table 27.

Table 27 Clock Signal Specification

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
Nominal long term average frequency	f_{AV}	40		fh_{MAX}	MHz	1,2,4
UI instantaneous	UI_{INST}	0.8		1.2	UI_{NOM}	3,4,5

Notes:

1. 80 Mbps minimum. No explicitly specified maximum. Implementations will most likely be practically limited to about 1Gb/s.

2. The average frequency f_{AV} is measured over any 1 µs period of time and shall include all sources of clock variation.

3. Derived from 0.1 UI of clock period jitter and 0.1 UI duty cycle distortion. Period jitter is the deviation between any single period of the clock and the average period of the clock, $1/f_{AV}$. However, the specified instantaneous UI variation may be allocated freely by an implementing D-PHY

4. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

5. $UI_{NOM}=1/(2.fh)$, where fh is fundamental frequency of the DDR Clock. This is equivalent to $0.4 \leq UI_{INST}.fh \leq 0.6$

9.2 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the NRZ Data differential signal is shown in Figure 49. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data. The byte synchronization signaling detailed elsewhere in this document determines which edge of the Clock is used to sample which bit of each byte. The transmitter shall ensure that the rising edge of the DDR Clock is sent during the first bit of each byte, such that the receiver can sample the bits of each byte starting with a rising edge.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

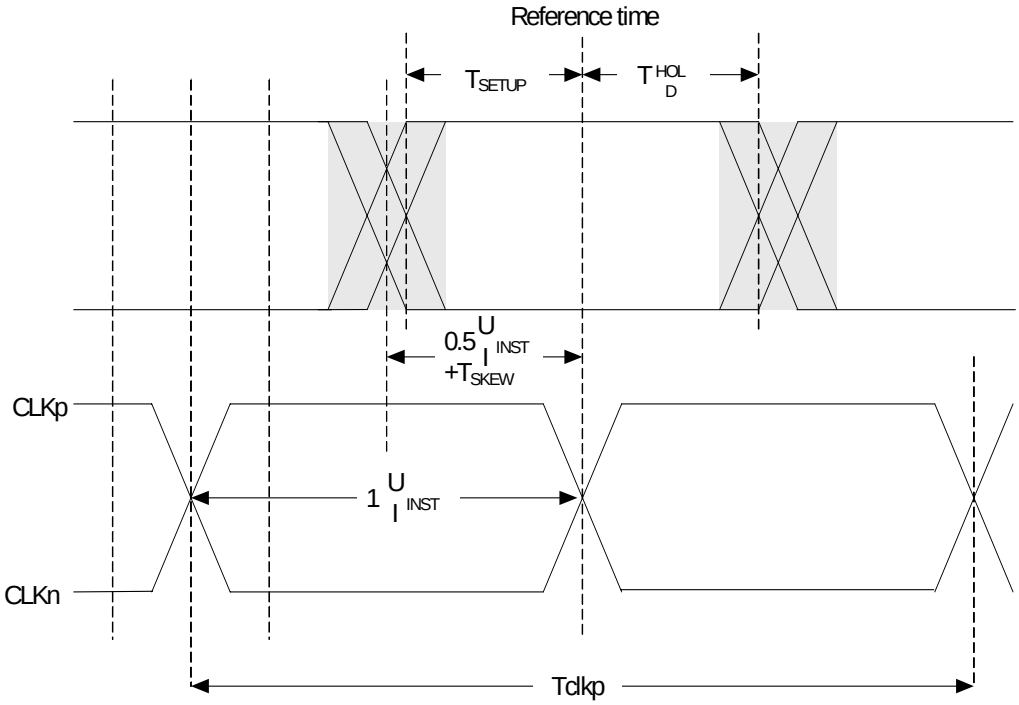


Figure 49 Data to Clock Timing Definitions

9.2.1 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 28. The skew specification is the allowed deviation of the data launch time to the ideal $\frac{1}{2}UI_{INST}$ displaced quadrature clock edge. Specifications of timing budget for receiver represents the minimum budget observable at the receiver for which the receiver will operate at the specified maximum acceptable bit error rate.

The intent in the timing budget is to leave $0.35*UI_{NOM}$ for degradation contributed by the interconnect.

Table 28 Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	$T_{SKEW[TX]}$	-0.075		0.075	UI_{NOM}	1
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UI_{NOM}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UI_{NOM}	2

Notes:

1. Total silicon and package delay budget of .15UI
2. Total setup and hold window for receiver of .3UI

9.3 Reverse High-Speed Data Transmission Timing

This section only applies to Half-Duplex Lane Modules that include Reverse High-Speed Data Transmission functionality.

A Lane enters the Reverse High-Speed Data Transmission mode by means of a Lane Turnaround procedure as specified in section 5.5. Reverse Data Transmission is not source synchronous; the Clock signal is driven by the Master side while the Data Lane is driven by the Slave side. The Slave Side transmitter shall send one NRZ data bit every two periods of the received Clock signal. Therefore, for a given Clock frequency, the Reverse direction data rate is one-fourth the Forward direction data rate.

Note that this specification allows changing the clock source frequency between transmission bursts when all Data Lanes are in a Low-Power state.

The conceptual overview of Reverse HS Data Transmission is shown in Figure 50.

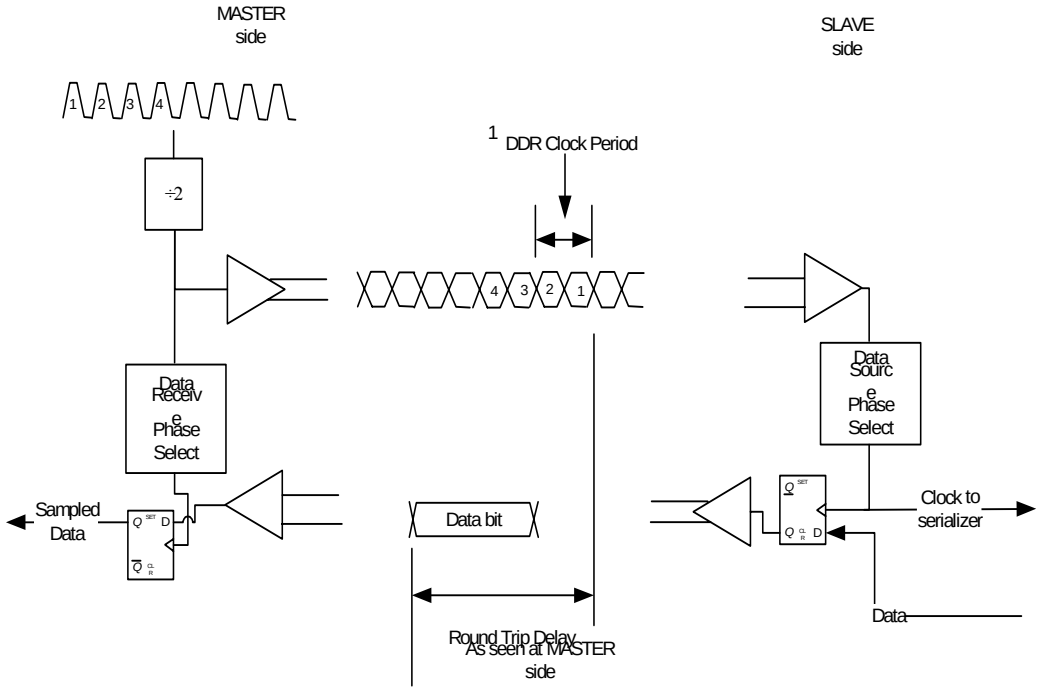


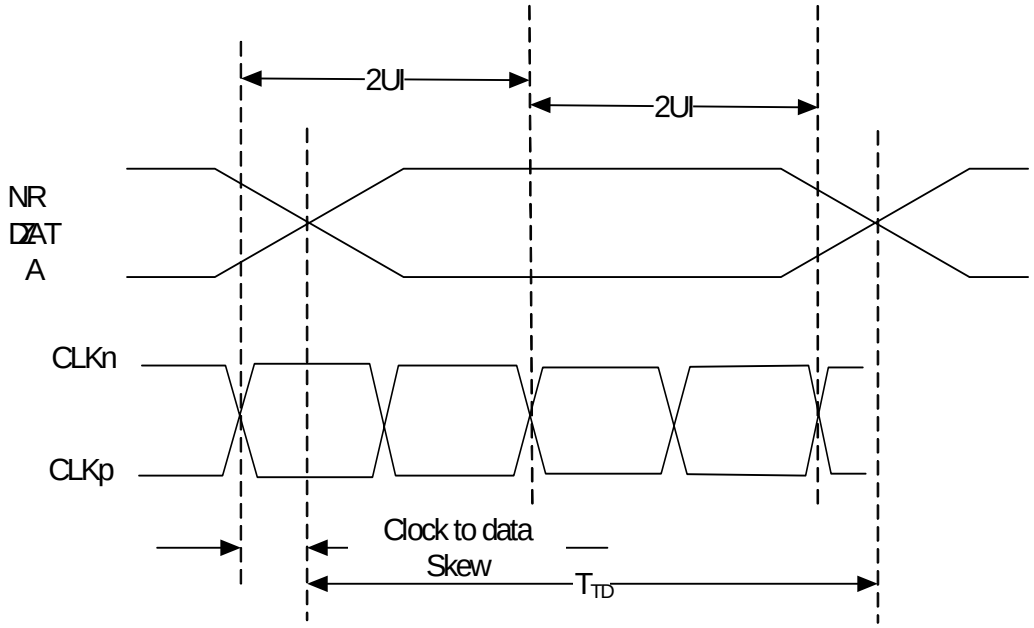
Figure 50 Conceptual View of HS Data Transmission in Reverse Direction

There are four possible phases of data-clock signal in the Reverse direction. The Clock phase used to send data is at the discretion of the Slave side, but once chosen it shall remain fixed throughout that data transmission burst. Signal delays in interconnect together with internal signal delays in the Master and Slave Module cause a fixed but unknown phase relationship between received (Reverse) Data and its own (Forward) Clock in the Master Module.

Synchronization is achieved with the Sync sequence during the Start of Transmission (SoT).

The known transitions of the received Sync sequence shall be used to select an appropriate phase of the clock signal for data sampling. Thus there is no need to specify the round trip delay between the source of the clock and the receiver of the data.

The timing of the Reverse transmission as seen at the Slave side is shown in Figure 51.



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1333 **Figure 51 Reverse High-Speed Data Transmission Timing at Slave Side**

1334 Table 29 summarizes the Reverse HS transmission timing specifications. The UI_{NOM} unit is the equivalent
1335 UI for the full-rate forward transmission.

1336 **Table 29 Reverse HS Data Transmission Timing Parameters**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data bit duration [measured at data transmitter]	$T_{TD[TX]}$	3.2	4	4.8	UI_{NOM}	1,2

1337 Notes:

1338 1. Due to 0.2UI instantaneous clock variation allowed in clock specification.

1339 2. Typical value is the average rate over 50 UI.

10 Structured Tables with all kind of values as described in all other sections

Table 30 DC Electrical Characteristics

Title				
Text				

Table 31 High Speed (HS) Source Electrical Characteristics

Title				
Text				

Table 32 Low Power (LP) Electrical Characteristics

Title				
Text				

11 Regulatory Requirements

All MIPI D-PHY based devices should be designed to meet the applicable regulatory requirements.

Annex A (informative)
Logical PHY-Protocol Interface Description

The PHY Protocol Interface (PPI) is used to make a connection between the PHY lane modules and the higher protocol layers of a communication stack. The interface described here is intended to be generic and application independent.

This appendix is informative only. Conformance to the D-PHY specification does not depend on any portion of the PPI defined herein. Because of that, this section avoids normative language and does not use words like “shall” and “should.” Instead, present tense language has been used to describe the PPI, utilizing words like “is” and “does.” The reader may find it helpful to consider this appendix to be a description of an example implementation, rather than a specification.

This PPI is optimized for controlling a D-PHY and transmitting and receiving parallel data. The interface described here is defined as an on-chip connection, and does not attempt to minimize signal count or define timing parameters or voltage levels for the PPI signals.

A.1 Signal Description

Table 33 defines the signals used in the PPI. For a PHY with multiple data lanes, a set of PPI signals is used for each lane. Each signal has been assigned into one of six categories: high-speed transmit signals, high-speed receive signals, escape-mode transmit signals, escape-mode receive signals, control signals, and error signals. Bi-directional high-speed data lanes with support for bi-directional Escape mode include all of the signals listed in the table. Unidirectional lanes or Clock lanes include only a subset of the signals. The direction of each signal is listed as “I” or “O”. Signals with the direction “I” are PHY inputs, driven from the Protocol. Signals with the direction “O” are PHY outputs, driven to the Protocol. For this logical interface, all clocks are described as being generated outside the PHY, although any specific PHY may implement the clock circuit differently.

The “Categories” column in Table 33 indicates for which Lane Module types each signal applies. The category names are described in Table 1 and are summarized here for convenience. Each category is described using a four-letter acronym, defined as <Side, HS-directions, Escape-Forward, Escape-Reverse>. The first letter, Side, can be M (Master) or S (Slave). The second letter, High-Speed directions, can be B (Bi-directional), U (Unidirectional), or C (Clock). The third and fourth letters indicate Escape mode capability in the Forward and Reverse directions. These letters can be N (Not available) or Y (available). Any of the four identification characters can be replaced by an X to indicate that any of the available options is appropriate. For example, all signals that might be used in a clock lane are identified by codes with a ‘C’ or ‘X’ in the second character. All signals that might be used for a data lane are identified by a ‘B’, ‘U’ or ‘X’ in the second character.

Table 33 PPI Signals

Symbol	Dir	Categories	Description
High-Speed Transmit Signals			
TxDDRClkHS-I	I	MBXX MUXX	Data Lane High-Speed Transmit DDR Clock. This signal is used to transmit high-speed data bits over the Lane Interconnect. All Data Lanes use the same TxDDRClkHS-I (in-phase) clock signal.

Symbol	Dir	Categories	Description
TxDDRClkHS-Q	I	MCNN	Clock Lane High-Speed Transmit DDR Clock. This signal is used to generate the high-speed clock signal for the Lane Interconnect. The TxDDRClkHS-Q (quadrature) clock signal is phase shifted from the TxDDRClkHS-I clock signal.
TxByteClkHS	O	XBXX MUXX	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that all transmitting data lane modules share one TxByteClkHS signal. The frequency of TxByteClkHS should be exactly 1/8 the high-speed bit rate.
TxDataHS[7:0]	I	XBXX MUXX	High-Speed Transmit Data. Eight bit high-speed data to be transmitted. The signal connected to TxDataHS[0] is transmitted first. Data is captured on rising edges of TxByteClkHS.
TxRequestHS	I	XBXX MUXX MCNN	High-Speed Transmit Request and Data Valid. A low-to-high transition on TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the lane module to initiate an End-of-Transmission sequence. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on TxDataHS to be transmitted. The lane module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low.
TxReadyHS	O	XBXX MUXX	High-Speed Transmit Ready. This active high signal indicates that TxDataHS is accepted by the lane module to be serially transmitted. TxReadyHS is valid on rising edges of TxByteClkHS.
High-Speed Receive Signals			

Symbol	Dir	Categories	Description
RxByteClkHS	O	XBXX SUXX	High-Speed Receive Byte Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxByteClkHS is generated by dividing the received high-speed DDR clock.
RxDataHS[7:0]	O	XBXX SUXX	High-Speed Receive Data. Eight bit high-speed data received by the lane module. The signal connected to RxDataHS[0] was received first. Data is transferred on rising edges of RxByteClkHS.
RxValidHS	O	XBXX SUXX	High-Speed Receive Data Valid. This active high signal indicates that the lane module is driving valid data to the protocol on the RxDataHS output. There is no “RxReadyHS” signal, and the protocol is expected to capture RxDataHS on every rising edge of RxByteClkHS where RxValidHS is asserted. There is no provision for the protocol to slow down (“throttle”) the receive data.
RxActiveHS	O	XBXX SUXX	High-Speed Reception Active. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.
RxSyncHS	O	XBXX SUXX	Receiver Synchronization Observed. This active high signal indicates that the Lane module has seen an appropriate synchronization event. In a typical high-speed transmission, RxSyncHS is high for one cycle of RxByteClkHS at the beginning of a high-speed transmission when RxActiveHS is first asserted, and again for one cycle of RxByteClkHS at the end of a high-speed transmission, just before RxActiveHS returns low.
RxClkActiveHS	O	SCXN	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal.
RxDDRClkHS	O	SCXN	Receiver DDR Clock. This is the received DDR clock – it may be used by the protocol if required. This signal is low whenever RxClkActiveHS is low.
Escape Mode Transmit Signals			

Symbol	Dir	Categories	Description
TxClkEsc	I	XBXX MUYX SUXY	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. It is therefore constrained by the normative part of the D-PHY specification. See section 8. Note that this clock is used to synchronize TurnRequest and is included for any module that supports bi-directional high-speed operation, even if that module does not support transmit or bi-directional escape mode.
TxRequestEsc	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Request. This active high signal, asserted together with exactly one of TxLpdtEsc, TxUlpmEsc, or one bit of TxTriggerEsc, is used to request entry into escape mode. Once in escape mode, the lane stays in escape mode until TxRequestEsc is de-asserted. TxRequestEsc is only asserted by the protocol while TxRequestHS is low.
TxLpdtEsc	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Low Power Data. This active high signal is asserted with TxRequestEsc to cause the lane module to enter low-power data transmission mode. The lane module remains in this mode until TxRequestEsc is de-asserted. TxUlpmEsc and all bits of TxTriggerEsc are low when TxLpdtEsc is asserted.
TxUlpmEsc	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Ultra Low Power. This active high signal is asserted with TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpmEsc is asserted.

Symbol	Dir	Categories	Description
TxTriggerEsc[3:0]	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Trigger 0-3. One of these active high signals is asserted with TxRequestEsc to cause the associated Trigger to be sent across the lane interconnect. In the receiving lane module, the same bit of RxTriggerEsc is then asserted and remains asserted until the lane interconnect returns to Stop state. Only one bit of TxTriggerEsc is asserted at any given time, and only when TxLpdtEsc and TxUlpmEsc are both low.
TxDataEsc[7:0]	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Data. This is the eight bit escape mode data to be transmitted in low-power data transmission mode. The signal connected to TxDataEsc[0] is transmitted first. Data is captured on rising edges of TxClkEsc.
TxValidEsc	I	MBYX MUYX SBXY SUXY	Escape mode Transmit Data Valid. This active high signal indicates that the protocol is driving valid data on TxDataEsc to be transmitted. The lane module accepts the data when TxRequestEsc, TxValidEsc and TxReadyEsc are all active on the same rising TxClkEsc clock edge.
TxReadyEsc	O	MBYX MUYX SBXY SUXY	Escape mode Transmit Ready. This active high signal indicates that TxDataEsc is accepted by the lane module to be serially transmitted. TxReadyEsc is valid on rising edges of TxClkEsc.
Escape Mode Receive Signals			
RxClkEsc	O	MBXY MUXY SBYX SUYX	Escape mode Receive Clock. This signal is used to transfer received data to the protocol during escape mode. This “clock” is generated from the two low-power signals in the lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this “clock” may not be periodic.

Symbol	Dir	Categories	Description
RxLpdtEsc	O	MBXY MUXY SBYX SUYX	Escape Low Power Data Receive mode. This active high signal is asserted to indicate that the lane module is in low-power data receive mode. While in this mode, received data bytes are driven onto the RxDataEsc output when RxValidEsc is active. The lane module remains in this mode with RxLpdtEsc asserted until a Stop state is detected on the lane interconnect.
RxUlpmEsc	O	MBXY MUXY SBYX SUYX	Escape Ultra Low Power (Receive) mode. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with RxUlpmEsc asserted until a Stop state is detected on the lane interconnect.
RxTriggerEsc[3:0]	O	MBXY MUXY SBYX SUYX	Escape mode Receive Trigger 0-3. These active high signals indicate that a trigger event has been received. The asserted RxTriggerEsc signal remains active until a Stop state is detected on the lane interconnect.
RxDataEsc[7:0]	O	MBXY MUXY SBYX SUYX	Escape mode Receive Data. This is the eight-bit escape mode low-power data received by the lane module. The signal connected to RxDataEsc[0] was received first. Data is transferred on rising edges of RxClkEsc.
RxValidEsc	O	MBXY MUXY SBYX SUYX	Escape mode Receive Data Valid. This active high signal indicates that the lane module is driving valid data to the protocol on the RxDataEsc output. There is no “RxReadyEsc” signal, and the protocol is expected to capture RxDataEsc on every rising edge of RxClkEsc where RxValidEsc is asserted. There is no provision for the protocol to slow down (“throttle”) the receive data.
Control Signals			

Symbol	Dir	Categories	Description
TurnRequest	I	XBXX XUYY	Turn Around Request. This active high signal is used to indicate that the protocol desires to turn the lane around, allowing the other side to begin transmission. TurnRequest is valid on rising edges of TxClkEsc. TurnRequest is only meaningful for a lane module that is currently the transmitter (Direction=0). If the lane module is in receive mode (Direction=1), this signal is ignored.
Direction	O	XBXX XUYY	Transmit/Receive Direction. This signal is used to indicate the current direction of the lane interconnect. When Direction=0, the lane is in transmit mode (0=Output). When Direction=1, the lane is in receive mode (1=Input).
TurnDisable	I	XBXX SUYY	Disable Turn-around. This signal is used to prevent a (bi-directional) lane from going into transmit mode – even if it observes a turn-around request on the lane interconnect. This is useful to prevent a potential “lock-up” situation when a unidirectional lane module is connected to a bi-directional lane module.
ForceRxmode	I	XBXX SUXX	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a lane module or force a bi-directional lane module into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the lane module immediately transitions into receive control mode and waits for a Stop state to appear on the lane interconnect.
ForceTxStopmode	I	XBXX MUXX	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a bi-directional lane module into transmit mode and Stop state following an error situation (e.g. expired time out). When this signal is high, the lane module immediately transitions into transmit mode and the module state machine is forced into the Stop state.
Stopstate	O	XXXX	Lane is in Stop state. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface.

Symbol	Dir	Categories	Description
Shutdown	I	XXXX	Shutdown Lane Module. This active low signal forces the Lane module into "shutdown", disabling all activity. All line drivers, receivers, terminators, and contention detectors are turned off when Shutdown is asserted. When Shutdown is high, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Shutdown is a level sensitive signal and does not depend on any clock.
TxUlpmClk	I	MCNN	Transmit Ultra Low-Power mode on Clock Lane. This active high signal is asserted to cause a Clock Lane module to enter the Ultra Low-Power mode. The Lane module remains in this mode until TxUlpmClk is de-asserted.
RxUlpmClk	O	SCNN	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpmClk asserted until a Stop state is detected on the Lane Interconnect.
Error Signals			
ErrSotHS	O	MBXX SUXX	Start-of-Transmission (SoT) Error. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxByteClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
ErrSotSyncHS	O	MBXX SUXX	Start-of-Transmission Synchronization Error. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of RxByteClkHS.
ErrEotSyncHS	O	MBXX SUXX	End-of-Transmission Synchronization Error. If a high-speed transmission ends when the number of bits received during that transmission is not a multiple of eight, this signal is asserted for one cycle of RxByteClkHS.

Symbol	Dir	Categories	Description
ErrEsc	O	MBXY MUXY SBYX SUYX	Escape Entry Error. If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.
ErrSyncEsc	O	MBXY MUXY SBYX SUYX	Low Power Data Transmission Synchronization Error. If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the next change in line state.
ErrControl	O	XBXX MUXY SBYX SUYX	Control Error. This signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains high until the next change in line state.
ErrContentionLP0	O	XBXX XUXY	LP0 Contention Error. This signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low.
ErrContentionLP1	O	XBXX XUXY	LP1 Contention Error. This signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line high.

A.2 High-speed Transmit from the Master Side

Figure 52 shows an example of a high-speed transmission on the Master side. While TxRequestHS is low, the lane module ignores the value of TxDataHS. To begin transmission, the protocol drives TxDataHS with the first byte of data and asserts TxRequestHS. This data byte is accepted by the PHY on the first rising edge of TxByteClkHS with TxReadyHS also asserted. At this point, the protocol logic drives the next data byte onto TxDataHS. After every rising clock cycle with TxReadyHS active, the protocol supplies a new valid data byte or ends the transmission. After the last data byte has been transferred to the lane module, TxRequestHS is driven low to cause the lane module to stop the transmission and enter Stop state. The minimum number of bytes transmitted could be as small as one.

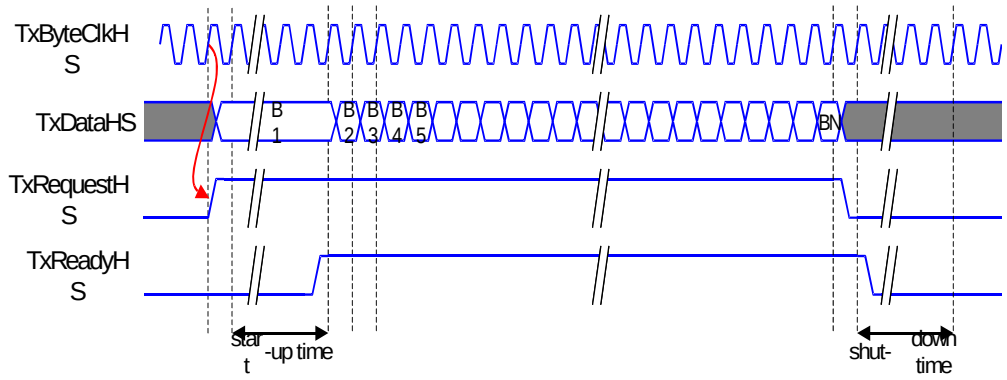

Figure 52 Example High-speed Transmission from Master Side

A.3 High-speed Receive at the Slave Side

Figure 53 shows an example of a high-speed reception at the Slave side. The RxActiveHS signal indicates that a receive operation is occurring. A normal reception starts with a pulse on RxSyncHS followed by valid receive data on subsequent cycles of RxByteClkHS. Note that the protocol shall be prepared to receive all of the data. There is no method for the receiving protocol to pause or slow data reception. When the last data byte has been received, RxSyncHS pulses high for one cycle and then RxActiveHS becomes low.

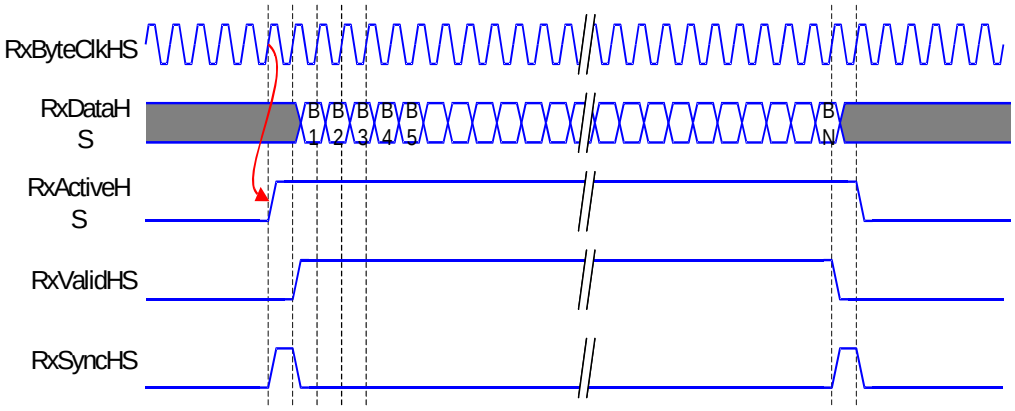

Figure 53 High-speed Receive at the Slave Side

A.4 High-speed Transmit from the Slave Side

A Slave can only transmit at one-fourth the bandwidth of a Master. Because of this, the TxReadyHS signal is not constant high for a transmitting slave. Otherwise, the transmission is very much like that seen at the PPI interface of a transmitting Master-side Lane Module. Figure 54 shows an example of transmitting from the Slave side.

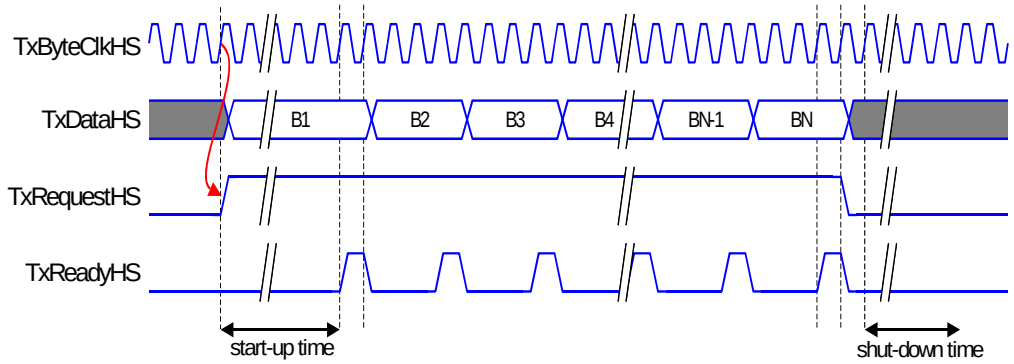

Figure 54 Example High-speed Transmit from the Slave Side

A.5 High-speed Receive at the Master Side

Because a Slave is restricted to transmitting at one-fourth the bandwidth of a Master, the RxValidHS signal is only asserted one out of every four cycles of RxByteClkHS during a high-speed receive operation at the Master side. An example of this is shown in Figure 55.

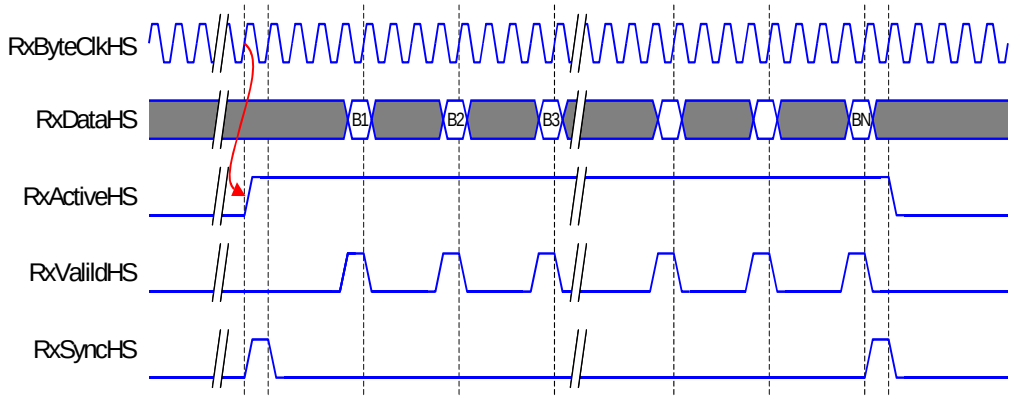

Figure 55 Example High-speed Receive at the Master Side

A.6 Low-power Data Transmission

For low-power data transmission the TxClkEsc is used instead of TxBitClkHS and TxByteClkHS. Furthermore, while the high-speed interface signal TxRequestHS serves as both a transmit request and a data valid signal, on the low-power interface two separate signals are used. The Protocol directs the Data Lane to enter low-power data transmission Escape mode by asserting TxRequestEsc with TxLpdtEsc high. The low-power transmit data is transferred on the TxDataEsc lines when TxValidEsc and TxReadyEsc are both active at a rising edge of TxClkEsc. The byte is transmitted in the time after the TxDataEsc is accepted by the lane module (TxValidEsc = TxReadyEsc = high) and therefore the TxClkEsc should continue running for some minimum time after the last byte is transmitted. The Protocol knows the byte transmission is finished when TxReadyEsc is asserted. After the last byte has been transmitted, the protocol de-asserts TxRequestEsc to end the low-power data transmission. This causes TxReadyEsc to return low, after which the TxClkEsc clock is no longer needed. Whenever TxRequestEsc transitions from high-to-low, it always remains in the low state for a minimum of two TxClkEsc clock cycles. Figure 56 shows an example low-power data transmission operation.

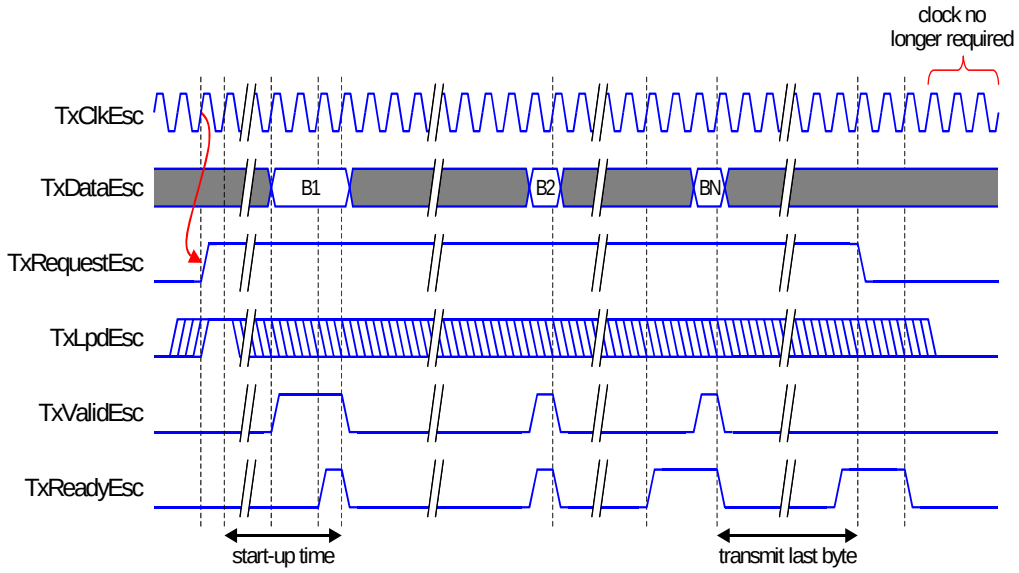

Figure 56 Low-power Data Transmission

A.7 Low-power Data Reception

Figure 57 shows an example low-power data reception. In this example, a low power escape "clock" is generated from the Lane Interconnect by the logical Exclusive-OR of the Dp and Dn lines. This "clock" is used within the Lane Module to capture the transmitted data. In this example, the "clock" is also used to generate RxClkEsc.

The signal RxLpdtEsc is asserted when the escape entry command is detected and stays high until the Lane returns to Stop state, indicating that the transmission has finished. It is important to note that because of the asynchronous nature of Escape mode transmission, the RxClkEsc signal can stop at anytime in either the high or low state. This is most likely to happen just after a byte has been received, but it could happen at other times as well.

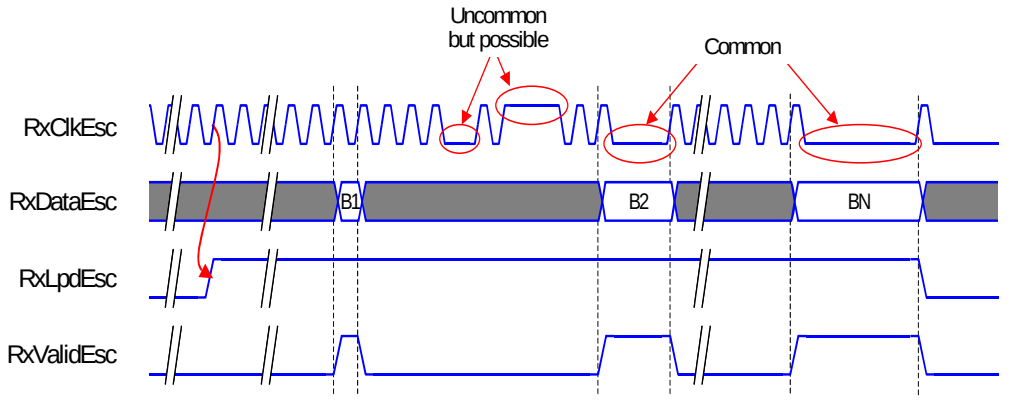

Figure 57 Example Low-power Data Reception

A.8 Turn-around

If the Master side and Slave side Lane Modules are both bi-directional, it is possible to turn around the link for high-speed and/or Escape mode signaling. As explained in section 5.5, which side is allowed to transmit is determined by passing a “token” back and forth. That is, the side currently transmitting passes the token to the receiving side. If the receiving side acknowledges the turn-around request (as indicated by driving the appropriate line state), the direction is switched.

Figure 58 shows an example of two turn-around events. At the beginning, the local side is the transmitter, as shown by Direction=0. When the protocol on this side wishes to turn the lane around (i.e. give the token to the other side), it asserts TurnRequest for at least one cycle of TxClkEsc. This initiates the turn-around procedure. The remote side acknowledges the turn-around request by driving the appropriate states on the Lines. When this happens, the local Direction signal changes from transmit (0) to receive (1).

Later in the example of Figure 58 the remote side initiates a turn-around request, passing the token back to the local side. When this happens, the local Direction signal changes back to transmit (0). It should be noted that there is no prescribed way for a receiver to request access to the Link. The current transmitter is in control of the Link direction and decides when to turn the link around, passing control to the receiver.

If the remote side does not acknowledge the turn-around request, the Direction signal does not change.

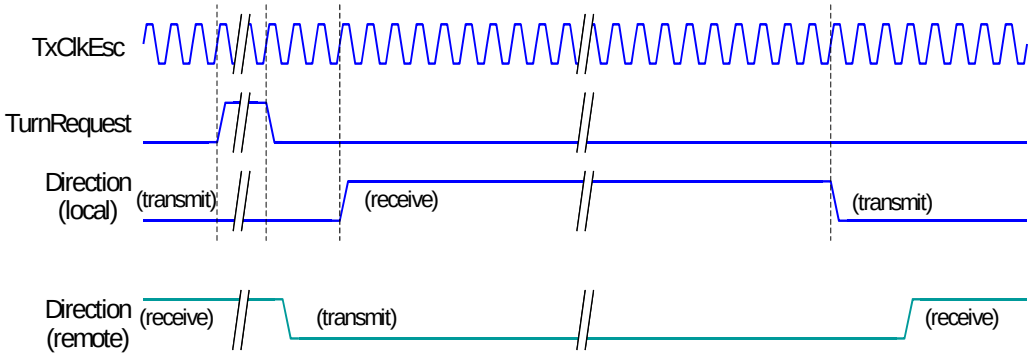

Figure 58 Example Turn-around Actions Transmit-to-Receive and Back to Transmit

Annex B (informative) Interconnect Design Guidelines

This appendix contains design guidelines in order to meet the interconnect requirements as specified in section 7.

B.1 Practical Distances

The maximum link flight time is defined at 2ns. Assuming less than 100ps wiring delay within the RX-TX modules each, the physical distance that can be bridged with external interconnect is around 54cm/√ε. For most practical PCB and flex materials this will correspond to distances around 25-30 cm as a maximum.

B.2 RF Frequency Bands: Interference

On one side there are the RF interference frequencies, which disturb the signals of the link. Most likely the dominant interferers are the transmit band frequencies of wireless interconnect standards. On the other side there are the frequencies for which generated EMI by the link should be as low as possible because very weak signals in these bands must be received by the radio IC. Some important frequency bands are:

Transmit Bands

- GSM 850 (824-849 MHz)
- GSM 900 (880-915 MHz)
- GSM DCS (1710-1785 MHz)
- GSM PCS (1850-1910 MHz)
- WCDMA (450MHz?, 1920-1980 MHz)

Receive Bands:

- GSM 850 (869-894 MHz)
- GSM 900 (925-960 MHz)
- GSM DCS (1805-1880 MHz)
- GSM PCS (1930-1990 MHz)
- WCDMA (2110-2170 MHz)
- GPS (1574-1577 MHz)

It is important to identify the lowest interference frequency with significant impact, as this sets 'f_{INTMIN}'. For this specification $f_{INT,MIN}$ is decided to be 450 MHz, because this frequency will most likely be used as the new WCDMA band in the USA in the future.

B.3 Transmission Line Design

In most cases the transmission lines will either be designed as striplines and/or micro-striplines. The coupling between neighboring lines within a pair is small if the distance between them is >2x the di-electrical thickness. For the separation of multiple pairs it is highly recommended to interleave the pairs with a ground (or supply) line in order to reduce coupling.

B.4 Reference Layer

In order to achieve good signal integrity and low EMI it is recommended that either a ground plane or a ground signal is in the close neighborhood of any signal line.

B.5 Printed-Circuit Board

For boards with a large number of conductor layers the dielectric spacing between layers may become so small that it would be hard to meet the characteristic impedance requirements. In those cases a micro-stripline in the top or bottom layers may be a better solution.

B.6 Flex-foils

Either two conductor layers or a reasonable connected cover layer makes it much easier to meet the specifications

B.7 Series Resistance

The DC series resistance in the interconnect should be less then 5 Ohm in order to meet the specifications. It is strongly recommended to keep the resistance in the ground connection below 0.2 Ohm. Furthermore the DC ground shift shall be less then 50mV, which might require even a lower value if much current is flowing through this ground. The lower this ground series resistance value can be made, the better it is for reliability and robustness.

B.8 Connectors

Connectors usually cause some impedance discontinuity. It is important to carefully minimize these discontinuities by design, especially with respect to the through-connection of the reference layer. Although connectors are typically rather small in size, the wrong choice can mess-up signals completely. Please note that the contact resistance of connectors is part of the total series resistance budget and should therefore be sufficiently low.