Small PCI Specification

Version 1.5a

Final

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Contact the PCI Special Interest Group office to obtain the latest revision of the specification. For more information about the PCI specification or membership in the PCI Special Interest Group contact:

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CONTENTS

Chapter 5 Mechanical Specification

Chapter 6 Configuration Space

Chapter 1
Introduction

1.1. Specification Contents

The Small PCI (SPCI) specification defines an alternative mechanical implementation of the 32-bit PCI Local Bus. It is intended for use as a small form factor interconnect mechanism for highly-integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

The Small PCI Specification, Version 1.5 should be used in conjunction with the *PCI Local Bus Specification,* Revision 2.1 or later. The Small PCI specification uses the same signal protocol, electrical, and configuration definitions as *PCI Local Bus Specification,* Revision 2.1 or later.

Refer to *PCI Local Bus Specification*, Revision 2.1 or later for references on protocol and configuration specification environments.

The Small PCI Specification defines the PCI hardware environment. Contact the PCI SIG for more information on the *PCI System Design Guide* and the *PCI BIOS Specification.* For information on how to join the PCI SIG or to obtain these documents, refer to Section 1.6.

1.2. Motivation

The performance characteristics of the PCI Local Bus, as demonstrated with desktop and server system environments, has generated interest in utilizing it in smaller system platforms. These environments, such as mobile systems, smaller PCs, and settop boxes, have physical characteristics that do not allow them to take advantage of “standard” PCI cards. Small PCI design characteristics address these physical requirements.

The advantages of Small PCI adapters are that they can be utilized in small mechanical packages and can be used to enhance current mechanical designs with additional expansion slots. The Small PCI characteristics will motivate a variety of industry implementations. Thus, it is important to provide a standard to simplify designs, reduce costs, and increase the selection of components and add-in cards.

1.3. Small PCI Local Bus Applications

The Small PCI has been defined with the primary goal of establishing an industry-standard, high-performance local bus architecture that offers low cost implementation and allows differentiation. Consideration for mobile applications via support of 3.3V are well documented in the *PCI Local Bus Specification*, Revision 2.1 and later. The Small PCI characteristics complement the 3.3V design with mechanical and electrical specifications that will enable implementation of PCI expansion slots in these form factors. These design characteristics will optimize size, cost, power consumption, performance, and compatibility.

1.4. Small PCI Overview

Refer to Section 1.4. of the *PCI Local Bus Specification*, Revision 2.1 or later.

Typical PCI Local Bus implementation supports add-in board connectors, although expansion capability is not required. Small PCI expansion boards can be used in ISA-, EISA-, Micro Channel (MC)-, and standard PCI-based systems.

To accommodate the 5V and 3.3V signaling environments and to facilitate a smooth migration path between the voltages, three add-in board electrical types are specified: a "5 volt" board which plugs into only the 5V connector, a "universal" board which plugs into both 5V and 3.3V connectors, and a "3.3 volt" board which plugs into only the 3.3V connector.

1.5. Small PCI Features and Benefits

Small PCI was specified to establish a high performance local bus standard for physically small mechanical environments. The Small PCI specification provides a selection of features that can achieve multiple price-performance points and can enable functions that allow differentiation at the system and component level. Features are categorized by benefit below.

High Performance

- 32-bit data path (132 MB/s).
- Variable length linear and cacheline wrap mode bursting for both read and writes improves write-dependent graphics performance.
- Low latency random accesses (60-ns write access latency to slave registers from master parked on bus).
- Capable of full concurrency with processor/memory subsystem.
- Hidden (overlapped) central arbitration.

Low Cost

- Optimized for direct silicon (component) interconnections (i.e., no glue logic). Electrical/driver (i.e., total load) and frequency specifications are met with standard ASIC technologies and other typical processes.
- Multiplexed architecture reduces pin count (47 signals for target; 49 for master) and package size of PCI components, or provides for additional functions to be built into a particular package size.
- Single PCI add-in card works in ISA-, EISA-, or MC-based systems (with minimal change to existing chassis designs), reducing inventory cost and end user confusion.
- Reduced system board real estate for header connector.
- Reduced add-in card size.

Ease of Use

- Enables full auto configuration support of PCI Local Bus add-in boards and components. PCI devices contain registers with the device information required for configuration.

Longevity

- Increased system board utility by implementation of subsystems on Small PCI add-in cards.
- Increased utility of standard add-in slots (ISA, EISA, MC, and PCI) by moving selected subsystems onto the Small PCI form factor.
- Processor independent. Supports multiple families of processors as well as future generations of processors (by bridges or by direct integration).
- Both 5V and 3.3V signaling environments are specified. Voltage migration path enables smooth industry transition from 5 volts to 3.3 volts.

Interoperability/ Reliability	• Small PCI add-in boards usable across multiple vendors and multiple mechanical packages. • **PRSNT[1:2]#** signals allow power supplies to be optimized for the expected systems usage by monitoring add-in boards that could surpass the maximum power budgeted by the system. • Increased reliability and interoperability of add-in cards by comprehending the loading and frequency requirements of the local bus at the component level, eliminating buffers and glue logic.
Flexibility	• Full multi-master capability allowing any PCI master peer-to-peer access to any PCI master/target.
Data Integrity	• PCI provides parity on both data and address, and allows implementation of robust client platforms.
Software Compatibility	• Small PCI components can be fully compatible with existing driver and applications software. Device drivers can be portable across various classes of platforms.

1.6. Administration

This document is maintained by the PCI SIG. The PCI SIG, an unincorporated association of members of the microcomputer industry, was established to monitor and enhance the development of the PCI Local Bus in three ways. The PCI SIG is chartered to:

- Maintain the forward compatibility of all PCI Local Bus revisions or addenda.
- Maintain the PCI Local Bus specification as a simple, easy-to-implement, stable technology in the spirit of its design.
- Contribute to the establishment of the PCI Local Bus as an industry-wide standard and to the technical longevity of the PCI Local Bus architecture.

SIG membership is available to all applicants within the microcomputer industry. Benefits of membership include:

- Submit specification revisions and addendum proposals.
- Participation in specification revisions and addendum proposals.
- Automatically receive revisions and addenda.
- Voting rights to determine the Steering Committee membership.
- Vendor ID number assignment.
- PCI technical support.
- PCI support documentation and materials.
- Participation in SIG sponsored trade show suites and events, conferences, and other PCI Local Bus promotional activities.

For information on how to become a SIG member or on obtaining PCI Local Bus documentation, please contact:

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Chapter 2
Signal Definition

2.1. Overview

SPCI uses the signals defined in Chapter 2 of the *PCI Local Bus Specification* for 32-bit transactions including the **CLKRUN#** and **PRSNT[1:2]#** signals. **CLKRUN#** can be used by the system and devices to control the frequency of the PCI bus clock (**CLK**). For details on **CLKRUN#** refer to the *PCI Mobile Design Guide*. The current SPCI definition does not support the optional 64-bit transfers and, therefore, does not support the 39 signals of the 64-bit extension. The five JTAG signals are not supported by SPCI.

Note: This SPCI specification has added **CLKRUN#** to the SPCI expansion connector for use in mobile systems. **CLKRUN#** has not been added to the large PCI expansion connector. A significant portion of the benefit of **CLKRUN#** can be obtained (in systems supporting the large expansion connector) by reducing the PCI clock frequency to approximately 1 MHz when the bus is idle. **REQ#** and **INTx#** can be used to increase the clock frequency to 33 MHz when either of these signals are asserted. When **CLKRUN#** is not supported on the SPCI expansion connector, the system grounds the **CLKRUN#** signal.

Chapter 3
Bus Operation

3.1. Overview

SPCI supports all the PCI bus characteristics defined in Chapter 3 of the *PCI Local Bus Specification* with the exception of 64-bit transactions. The optional 64-bit extension signals are not supported.

Chapter 4
Electrical Specification

4.1. Overview

SPCI supports the electrical and timing requirements in Chapter 4 of the *PCI Local Bus Specification.* SPCI supports 5-volt and 3.3-volt keyed small motherboard connectors. A 5-volt keyed Small Board can be inserted into a 5-volt keyed Small Connector. A 3.3-volt keyed Small Board can be inserted into a 3.3-volt keyed Small Connector. A universal keyed Small Board can be inserted into either the 5-volt or 3.3-volt keyed Small Connector. The keying is contained in the shell of the connector (refer to Chapter 5 for details of the keying).

4.2. System (Motherboard) Specification

4.2.1. Power Requirements

All Small PCI connectors require four power rails: +5V, +3.3V, +12V, and -12V. Desktop systems implementing Small PCI are required to provide all four rails in every system with the current budget specified in Table 4-1. Mobile systems typically support small boards that consume 2 watts or less. Support of +12V and -12V is not provided in many current mobile products. Small boards that require +12V or -12V should consider generating it from +3.3V.

Table 4-1: Power Requirements

Power Rail	Small Expansion Cards
5V ±5%	2A max. (system dependent)
3.3V ±0.3V	3A max. (system dependent)
12V ±5%	500 mA max. (system dependent)
-12V ±10%	100 mA max. (system dependent)

4.2.2. Connector Pin Assignments

The pin assignments for the Small Connector are shown in Table 4-2. The pin assignment is the same for the 5-volt and 3.3-volt connectors. The keying for the connector is in the connector shell (refer to Chapter 5 of this document).

Table 4-2: Small Connector Pin Assignments

Pin	5V and 3.3V System Environment		Comments
	Side B	Side A	
1	Ground	Ground	
2	INTB#	+12V	
3	+5V	INTA#	
4	INTD#	INTC#	
5	-12V	+5V	
6	PRSNT1#	Reserved	
7	Reserved	Reserved	
8	PRSNT2#	+5V	
9	CLK	RST#	
10	Ground	GNT#	
11	REQ#	Ground	
12	+5V	CLKRUN#	
13	AD[31]	AD[30]	
14	AD[29]	+5V	
15	Ground	AD[28]	
16	AD[27]	AD[26]	
17	AD[25]	Ground	
18	+V(I/O)	AD[24]	
19	Reserved	+V(I/O)	
20	Ground	Reserved	
	C/BE[3]#	Ground	
22	+3.3V	IDSEL	
23	AD[23]	+3.3V	
24	Ground	AD[22]	
25	AD[21]	AD[20]	
26	AD[19]	Ground	
27	+3.3V	AD[18]	
28	AD[17]	AD[16]	
29	C/BE[2]#	+3.3V	
30	Ground	FRAME#	
31	IRDY#	Ground	
32	+3.3V	TRDY#	
33	DEVSEL#	Ground	
34	Ground	STOP#	
35	LOCK#	+3.3V	
36	PERR#	SDONE	
37	Ground	SBO#	
38	SERR#	Ground	
39	+3.3V	PAR	
40	C/BE[1]#	AD[15]	
41	AD[14]	+3.3V	
42	Ground	AD[13]	

Table 4-2: Small Connector Pin Assignments (continued)

Pin	5V and 3.3V System Environment		Comments
	Side B	Side A	
43	AD[12]	AD[11]	
44	AD[10]	M66EN	
45	+V(I/O)	AD[09]	
46	AD[08]	C/BE[0]#	
47	AD[07]	+V(I/O)	
48	+5V	AD[06]	
49	AD[05]	AD[04]	
50	AD[03]	+5V	
51	+5V	AD[02]	
52	AD[01]	AD[00]	
53	ACK64#	Ground	
54	Ground	REQ64#	

Pins labeled +V(I/O) are connected to the +5V plane on the 5-volt keyed Small Connector and to the +3.3V plane on the 3.3-volt keyed Small Connector.

4.3. Expansion Board Specification

4.3.1. Board Pin Assignment

The **PRSNT1#** and **PRSNT2#** signals are used to indicate a board is physically present in the slot and provide information about the total power requirements of the Small Board. Table 4-3 defines the required setting of the **PRSNT#** pins for the small expansion boards.

Table 4-3: Present Signal Definitions

PRSNT1#	PRSNT2#	Small Board
Open	Open	No expansion board
Ground	Open	10W (max) board
Open	Ground	5W (max) board
Ground	Ground	2W (max) board

The pin assignments for the Small Board are shown in Table 4-4. The pin assignment is the same for the 5-volt and 3.3-volt boards. The keying for the board is in the connector shell (refer to Chapter 5).

Table 4-4: Small Board Pin Assignments

Pin	5V and 3.3V System Environment		Comments
	Side B	Side A	
1	Ground	Ground	
2	INTB#	+12V	
3	+5V	INTA#	
4	INTD#	INTC#	
5	-12V	+5V	
6	PRSNT1#	Reserved	
7	Reserved	Reserved	
8	PRSNT2#	+5V	
9	CLK	RST#	
10	Ground	GNT#	
11	REQ#	Ground	
12	+5V	CLKRUN#	
13	AD[31]	AD[30]	
14	AD[29]	+5V	
15	Ground	AD[28]	
16	AD[27]	AD[26]	
17	AD[25]	Ground	
18	$+V^{(I/O)}$	AD[24]	
19	Reserved	$+V^{(I/O)}$	
20	Ground	Reserved	
21	C/BE[3]#	Ground	
22	+3.3V	IDSEL	
23	AD[23]	+3.3V	
24	Ground	AD[22]	
25	AD[21]	AD[20]	
26	AD[19]	Ground	
27	+3.3V	AD[18]	
28	AD[17]	AD[16]	
29	C/BE[2]#	+3.3V	
30	Ground	FRAME#	
31	IRDY#	Ground	
32	+3.3V	TRDY#	
33	DEVSEL#	Ground	
34	Ground	STOP#	
35	LOCK#	+3.3V	
36	PERR#	SDONE	
37	Ground	SBO#	
38	SERR#	Ground	
39	+3.3V	PAR	
40	C/BE[1]#	AD[15]	
41	AD[14]	+3.3V	
42	Ground	AD[13]	

Table 4-4: Small Board Pin Assignments (continued)

Pin	5V and 3.3V System Environment		Comments
	Side B	Side A	
43	AD[12]	AD[11]	
44	AD[10]	M66EN	
45	+V(I/O)	AD[09]	
46	AD[08]	C/BE[0]#	
47	AD[07]	+V(I/O)	
48	+5V	AD[06]	
49	AD[05]	AD[04]	
50	AD[03]	+5V	
51	+5V	AD[02]	
52	AD[01]	AD[00]	
53	ACK64#	Ground	
54	Ground	REQ64#	

Pins labeled +V(I/O) are special power pins for defining and driving the PCI signaling rail on the universal boards. On these boards, the PCI component's I/O buffers shall be powered from these special power pins, not from the other +5V or +3.3V power pins.

Table 4-5 is a power pin summary of the 32-bit Small Board.

Table 4-5: Power Pin Summary

Pin Type	5V, 3.3V, and Universal Board
Ground	19
+5V	8
+3.3V	8
+12V	1
-12V	1
I/O power	4
Reserved	5

4.3.2. Power Consumption

The maximum power allowed for any PCI Small Board is 10 watts and represents the total power drawn from all four power rails provided at the connector. In the worst case, all power could be drawn from either the +5V or the +3.3V rail.

Many systems will not provide a full 10 watt power budget per Small Connector for each power rail because most boards typically draw much less than this amount. For this reason, PCI Small Boards that consume more than 2 watts should power up in (and reset to) a power-saving state that consumes 2 watts or less, if possible.

Chapter 5
Mechanical Specification

5.1. Overview

The Small PCI expansion card is designed to fit into mobile and small desktop PCs where height restrictions prevent the use of standard PCI expansion cards. The connector has been defined for a 32-bit interface with a total of 108 pins.

The form factor of the Small PCI card is the same as that currently utilized by PCMCIA.

Consequently, keying provisions have been made to exclude any PCMCIA, JEIDA, or DRAM implementations without damage to the connector interface.

5.1.1. Card Dimensions

There are three types of cards listed in this specification: a 5-volt card (Figure 5-1), a 3.3-volt card (Figure 5-2), and a universal card (Figure 5-3), which is capable of running in either a 5-volt or 3.3-volt system. Headers that are mounted to the system board have a set of keys that will prevent the installation of the wrong voltage card.

Additionally, there are two styles of cards that are differentiated only by their height. The Style A card is limited to 5.0 mm total height in the substrate area and Style B to 10.5 mm maximum. The Style A card can be placed in a double-header configuration (see Figure 5-7). Style B is limited to a single stack (see Figure 5-5) or the top layer of a double stack if a Style A card is also to be used.

Connector location and pin numbers for the 5-volt, 3.3-volt, and universal cards are shown in Figures 5-1, 5-2, and 5-3. Card polarization technique and dimensions are also shown in these figures. Polarization keys prevent mismating of a card before pin damage can occur. Keep-out force is 8 kg.

5.1.2. Card Covers

The intent of this specification is to define cards that are installed at the point of manufacture. Hence, card covers are not included as part of this specification. They are not, however, excluded from the specification, and vendors may choose to add them to address specific design needs.

5.1.3. Card Frames

All applications shown in this specification incorporate a card frame. The card frame is an integral part of this package and supplies rigidity to the thin printed circuit board (PCB) as well as supplying the guidance for card insertion. Additionally, the card frame provides polarization to differentiate between the 5-volt, 3.3-volt, and universal card types.

5.1.4. Printed Circuit Board

A typical implementation is shown in Figures 5-9 and 5-9-1, which depict the areas required for clearance for the connector and the card frame on either end of the card.

However, this specification covers only the form factor of the connector interface and the physical size of the entire package. Therefore, the internal details of the card package are the responsibility of the card provider and this section is to be viewed as a reference only.

5.2. Connector

The specified card interconnect system shall be 108 position, two piece pin-and-beam. The beam contacts shall be the connector on the card itself.

5.2.1. Card Connector

The beam contacts are located on the card as shown in Figures 5-1, 5-2, and 5-3. The card connector beam shall be configured as shown in Figure 5-4.

The card connector beam contacts shall make contact with the connector pin for a minimum length of 1.5 mm as shown in Figure 5-4.

5.2.2. Host Connector

The host pin connector shall be a 108-pin connector with opening, polarization, and pin location as shown in Figures 5-5 and 5-5-1. The host connector pin configuration is shown in Figure 5-4. Two different standoff heights as shown in dimension A are available for board component clearance.

The PCB pattern for the 108 host connector is shown in Figure 5-6.

The host pin connector can also be provided in a stacked 216-pin configuration, as shown in Figure 5-7, for inserting two Style A cards or one Style A and one Style B card. Host pin connector polarization is shown in Figure 5-7-1.

The centerline of the lower connector may be 1.8 mm above centerline of the adapter card on the primary component side (see the example in Figure 5-14-1) to 0.72 mm below centerline of the adapter card on the back side (see the example in Figure 5-14-2).

The PCB pattern for the 216-pin configuration is shown in Figure 5-8.

The outermost plating of socket and pin contact area shall be gold or other plated materials compatible with gold, as specified in Section 5.4. (Connector Physical Requirements).

The interconnect system shall meet the requirements specified in Sections 5.4.1. (Connector Performance Specification), 5.4.2. (Connector Electrical Performance Specification), and 5.4.3. (Connector Environmental Performance Requirements).

5.3. Card Guidance

The card shall be guided by the host connector for a minimum distance of 6 mm before the socket connector contacts the host (pin) connector (see Figures 5-4 and 5-5). The Original Equipment Manufacturer (OEM) is responsible for ensuring that the card is properly supported to meet the system requirements. Keep-out areas are defined (see Figures 5-1, 5-2, and 5-3) to assist OEMs. It is recommended that the 3 mm keep-out areas, defined along both lengths of the SPCI card, be used for this purpose.

5.4. Connector Physical Requirements

Table 5-1: Connector Physical Requirements

Part	Materials
Connector Housing	High-temperature plastic. UL flammability rating 94V-0.
Contacts: Receptacle Contacts: Plug	Beryllium copper. Phosphor bronze.
Contact Finish: Receptacle	Gold over nickel in the contact area. Alternate finish: Gold flash over palladium or palladium-nickel in the contact area, nickel underplate.
Contact Finish: Plug	Gold over nickel in the contact area. Alternate finish: Gold flash over palladium or palladium-nickel in the contact area, nickel underplate.

5.4.1. Connector Performance Specification

Table 5-2: Connector Performance

Parameter	Specification
Durability	100 mating cycles without physical damage or exceeding low-level contact resistance.
Total mating force	6.0 kg maximum.

5.4.2. Connector Electrical Performance Specification: 108-Pin Header

Table 5-3: Connector Electrical Performance: 108-Pin Header

Parameter	Specification
Contact Resistance (includes bulk resistance)	Standard height: 40 mΩ maximum initial; 20 mΩ maximum increase through testing. Extended height and double card: 55 mΩ maximum initial; 20 mΩ maximum increase through testing. Contact Resistance, test per Mil-STD-1344, Method 3002.1.
Insulation Resistance	1000 mΩ per MIL-STD-202, Method 302, Condition B
Dielectric Withstanding Voltage	500V ac RMS. per MIL-STD-1344, Method D3001.1, Condition B.
Capacitance	2.3 pF max. at 1 MHz.
Current Rating	0.5A per contact, 30 °C rise above ambient.
Voltage Rating	125V.
Certification	UL Recognition and CSR Certification required.

5.4.3. Connector Environmental Performance Requirements

Table 5-4: Connector Environmental Performance

Parameter	Specification
Operating Temperature	-40 °C to +105 °C.
Thermal Shock	-55 °C to +85 °C, 5 cycles per MIL-STD-1344, Method 1003.1.
Mixed Flowing Gas Test	Battelle, Class II. Connector mated and tested per Battelle method.

5.5. I/O Connector

The selection of two I/O connector types provides physical intermateability in SPCI applications across different system boxes and platforms, while also achieving economy of scale, standardization, and design and performance flexibility at the OEM level.

These I/O connectors are: 2 mm double-row pin headers with 0.5 mm square pins and miniature-ribbon contact connectors with 0.8 mm single- or double-row compliant ribbon contacts. Other connectors, such as miniature coaxial, other card edge, or fiber optic connectors may be employed for unique I/O applications and are not covered by this SPCI I/O specification. Various types of feature connectors that may be required for specific applications are also not specified.

5.5.1. 2 mm I/O

The 2 mm connector is a bare pin header mounted in-line with the printed PCB. This type of "stick" connector is used in small disk drive assemblies. Four to 34 double-row pins fit within the allowable SPCI card dimensions, with three SPCI standard pinouts being specified. These are: 9, 15, and 33, as shown in Figure 5-10 (with pins 10, 16,

and 34 removed for polarization). Frame latching, or other mechanical means of attaching the connector body to the PCB frame is optional, but recommended.

This I/O connector can be specified as either a double-sided straddle mount or single-sided surface mount to the PCB. For straddle-mount applications, PCB pads and double-sided keep-out area are shown in Figures 5-9 and 5-9-1. Depending on the application, these 2 mm MST I/O connectors can be specified as planar or vertically offset from the PCB centerline, depending upon SPCI card clearance requirements. In addition, these connectors are available with locating pins and hold-downs. The 2 mm headers typically mate to discrete wire, standard ribbon, or FE cable assembly via appropriate connectors. See Figure 5-10-1 for connector pin interface dimensions. Pins may be fully or selectively gold or palladium nickel gold-plated.

5.5.2. 0.8 mm Ribbon I/O

The 0.8 mm ribbon connector is a high-performance, high-pin-count-capable I/O system currently applied in various IC card applications. The 0.8 mm ribbon pitch of this connector makes it capable of 41 positions single row or 82 positions double row within the allowable width of the SPCI PCB assembly. For SPCI, the 9, 15, and 33 position connectors are recommended, with the 15 and 33 position devices being available in both shielded and non-shielded versions.

Ribbon contact interface dimensions are as shown in Figure 5-11-2. This type of I/O connector is also compatible with ribbon, FEC, round, discrete wire, or twisted pair cable assemblies. Shielded cable can be employed in RFI/EMI-sensitive applications. The mating cable connector is a 0.8 mm miniature ribbon receptacle with solder tab attachment to a wide dynamic range in conductor size. The 0.8 mm system provides mating polarization via its mechanical interface design. The 2.0 mm and 0.8 mm connectors are in accordance with Connector Environmental Performance Requirements as outlined in Section 5.4.3.

5.5.3. Connector Electrical Performance Specification - I/O

Table 5-5: Connector Electrical Performance Specification - I/O

Parameter	Specification
Contact Resistance	25 mΩ maximum initial; 20 mΩ maximum increase through testing. Contact Resistance, test per Mil-STD-1344, Method 3002.1.
Insulation Resistance	5,000 mΩ per MIL-STD-202, Method 302, Condition B
Dielectric Withstanding Voltage	300V ac RMS. per MIL-STD-1344, Method D3001.1, Condition B.
Current Rating	0.5A per contact, 30 °C rise above ambient.
Voltage Rating	500V.
Certification	UL Recognition and CSA Certification required.

5.6. Printed Circuit Board Attachment

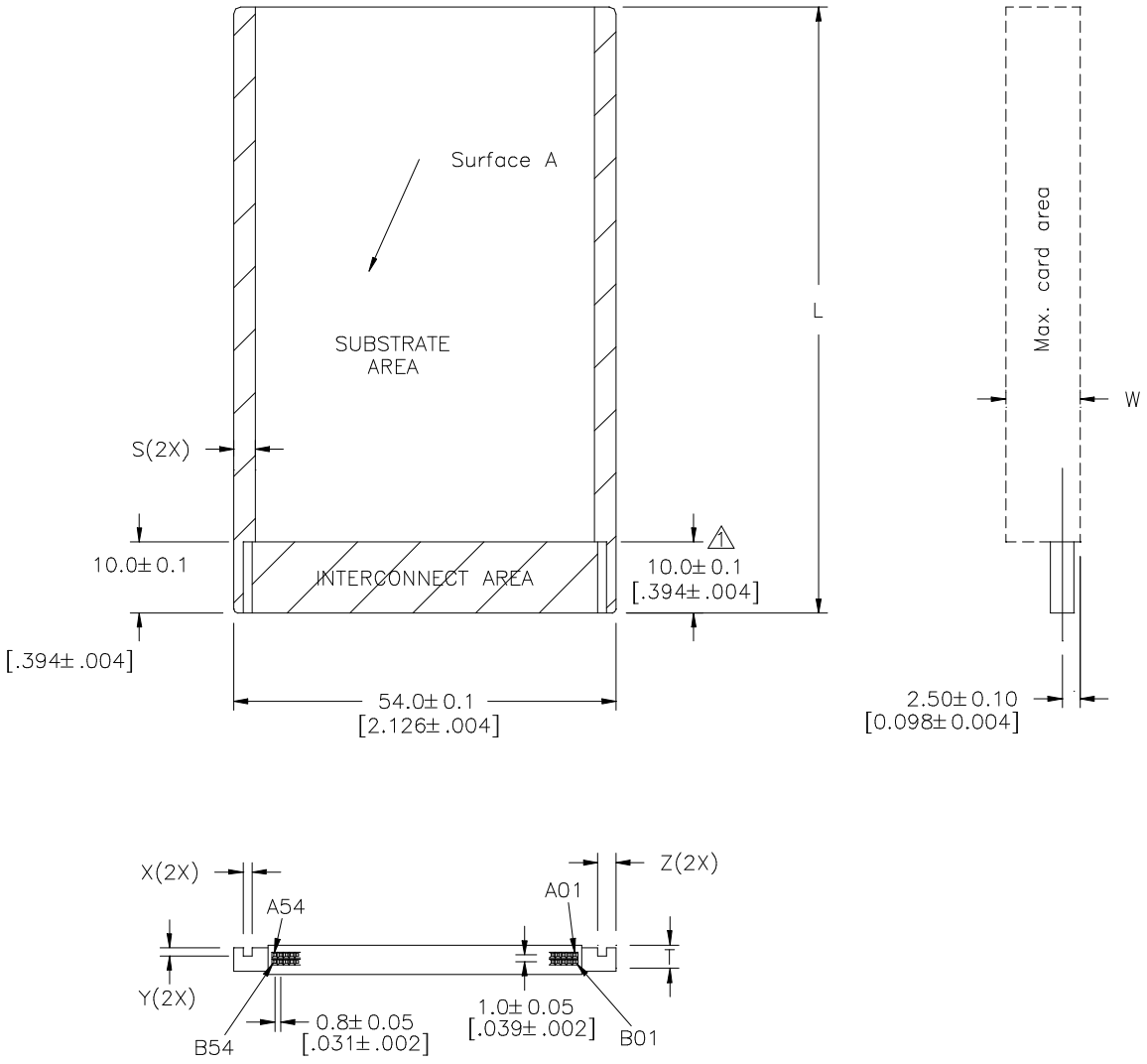
These connector systems are designed to be SMT reflow or hot bar solder attached, with or without alignment pins and hold-downs, depending on the specific part selection. The 2 mm connector can be straddle-mount (without hold-downs) or single-sided surface mount (with alignment pins and hold-downs), depending on the type of assembly operation used by the SPCI card manufacturer. The 0.8 mm connector is single sided surface mount (with alignment pins and optional metal shield tabs) and is designed for application up to and including full pick-and-place SMT automation.

Either I/O connector used in SPCI applications is designed to be applicable to thin laminate multi-layer PCB platforms. Note: Since a wide variety of PCB thickness may be applicable to SPCI applications, care should be taken to specify board thickness and co-planarity of connector pads. Typical board thickness for SPCI is assumed to be thin laminate multi-layer FR-4 in the 0.5-0.9 mm (~20 mils) range with connector pad co-planarity of approximately 0.10 mm. The I/O connector should be centered on the back of the PCB and mounted in proximity to the PCB horizontal plane. This will ensure that insertion/extraction forces do not cause board flexure, solder pad stress, or header misalignment during I/O mating.

5.7. Mechanical Characteristics

This section specifies the mechanical characteristics of the Small PCI bus. The characteristics are shown in the following illustrations:

Characteristic	Figure
5 Volt Small PCI Card Package Dimensions	5-1
3.3 Volt Small PCI Card Package Dimensions	5-2
Universal Small PCI Card Package Dimensions	5-3
Pin Configuration and Socket Contact	5-4
Small PCI Header Options (Single Card)	5-5
Small PCI Header Keying Details (Single Card)	5-5-1
Board Layout (Single Card, Top View)	5-6
Board Layout (Single Card, Top View) With Optional Latching	5-6-1
Small PCI Header Options (Double Card)	5-7
Small PCI Header Keying Details (Double Card)	5-7-1
Board Layout (Double Card, Top View)	5-8
Board Layout (Double Card, Top View) With Optional Latching	5-8-1
Small PCI Card (Surface A) With 2 mm I/O	5-9
Small PCI Card (Surface B) With Straddle Mount I/O	5-9-1
Small PCI Card Assembly With 0.8 mm Bus Connector, 2 mm I/O Connector, and Frame (Surface A Shown)	5-10
Small PCI Card Assembly With 0.8 mm Bus Connector, 2 mm I/O Connector, and Frame (Surface A Shown) With Optional Latching	5-10-1

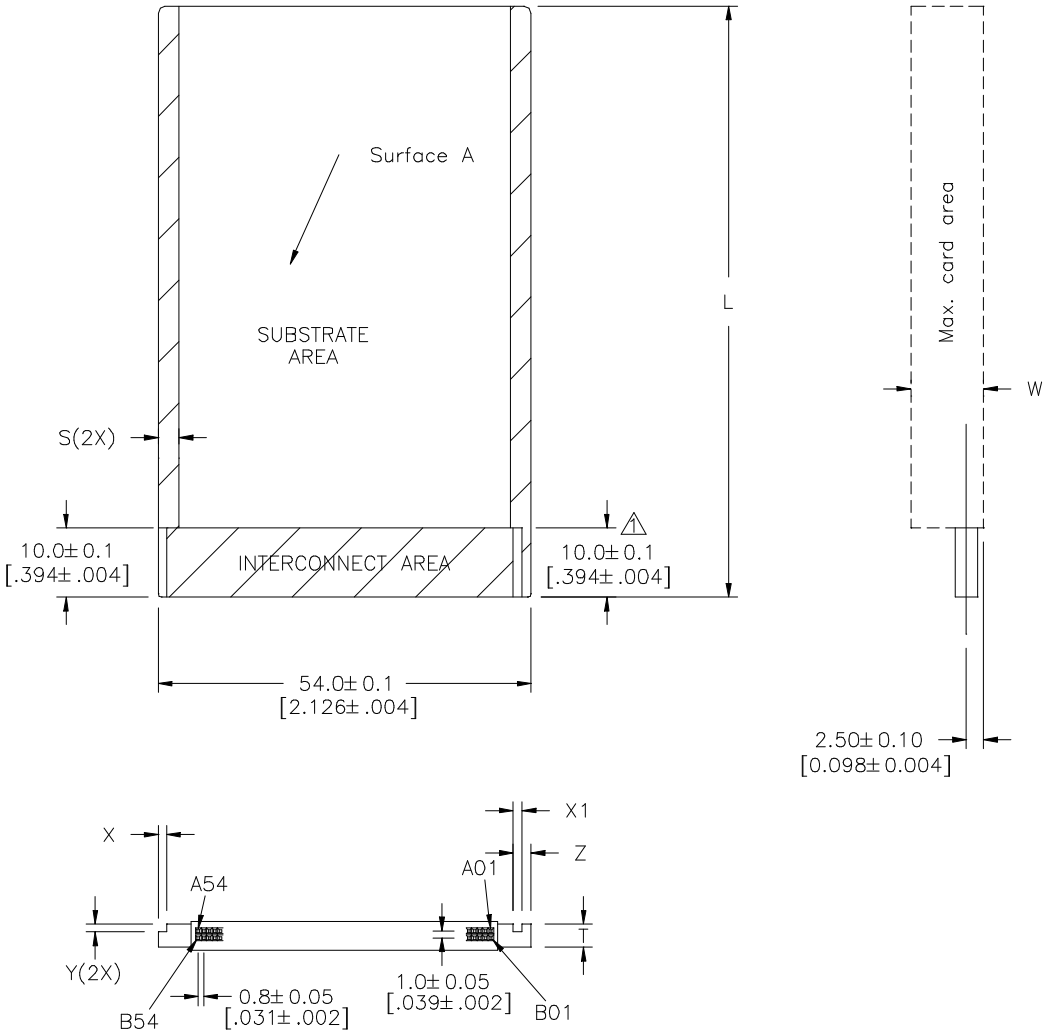


L ± .200 [.008]	S MIN.	T ± .051 [.002]	W ± .10 [.004]	X ± .051 [.002]	Y ± .051 [.002]	Z ± .102 [.004]
85.6 [3.370]	3.0 [.118]	3.3 [.130]	STYLE A: 5.0 [.197]	1.3 [.051]	1.1 [.043]	2.6 [.102]
			STYLE B: 10.5 [.413]			

⚠1 Polarization key length

2 English dimensions are in brackets [ ]

Figure 5-1: 5 Volt Small PCI Card Package Dimensions

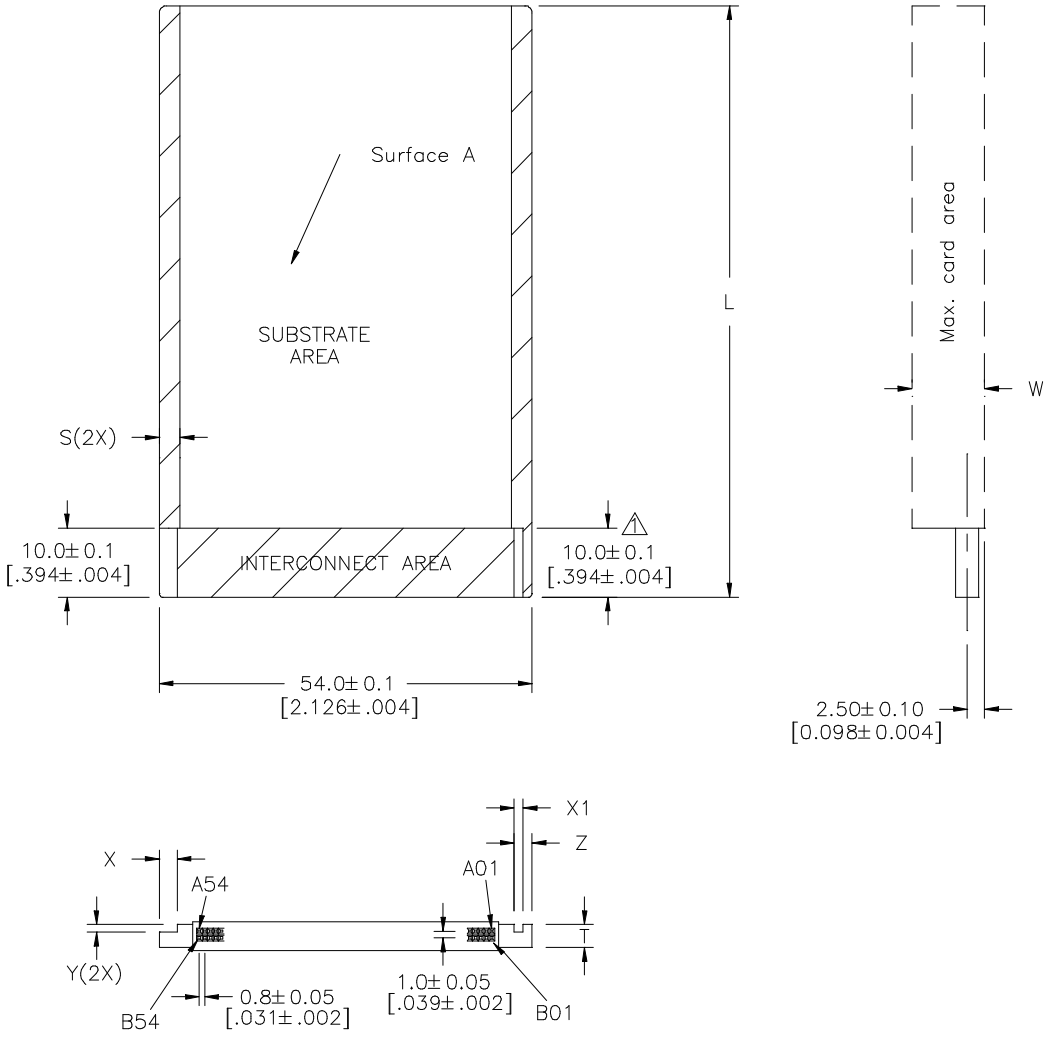


L ± .200 [.008]	S MIN.	T ± .051 [.002]	W ± .10 [.004]	X ± .051 [.002]	X1 ± .051 [.002]	Y ± .051 [.002]	Z ± .102 [.004]
85.6 [3.370]	3.0 [.118]	3.3 [.130]	STYLE A: 5.0 [.197] STYLE B: 10.5 [.413]	1.2 [.047]	1.3 [.051]	1.1 [.043]	2.6 [.102]

1 Polarization key length

2 English dimensions are in brackets [ ]

Figure 5-2: 3.3 Volt Small PCI Card Package Dimensions



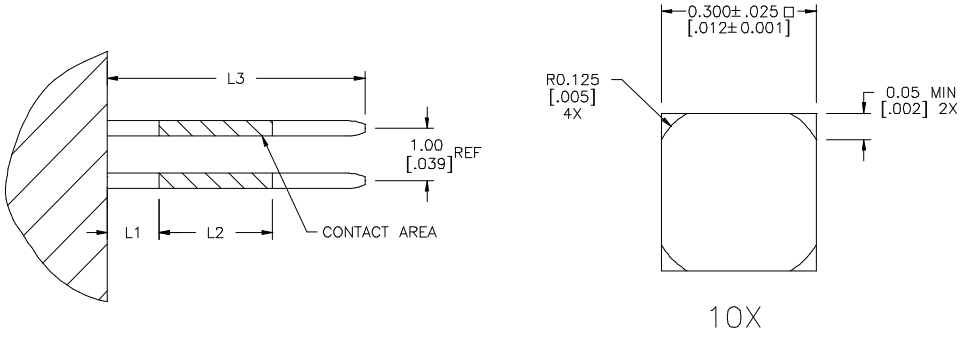
L ± .200 [.008]	S MIN.	T ± .051 [.002]	W ± .10 [.004]	X ± .051 [.002]	X1 ± .051 [.002]	Y ± .051 [.002]	Z ± .102 [.004]
85.6 [3.370]	3.0 [.118]	3.3 [.130]	STYLE A: 5.0 [.197] STYLE B: 10.5 [.413]	2.6 [.102]	1.3 [.051]	1.1 [.043]	2.6 [.102]

⚠1 Polarization key length

2 English dimensions are in brackets [ ]

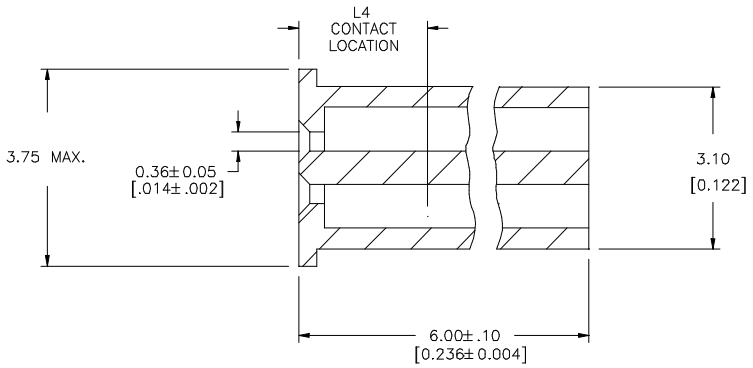
Figure 5-3: Universal Small PCI Card Package Dimensions

PIN CONFIGURATION



L1 MAX.	L2	L3 REF.	L4 MAX.
1.0 [.039]	2.2 [.087]	4.0 [.157]	2.5 [.098]

SOCKET CONTACT



English dimensions are in brackets [ ]

Figure 5-4: Pin Configuration and Socket Contact

CARD TYPE	DETAIL	A DIM	B DIM	C DIM REF	D DIM REF
5 VOLT	E	5.55±0.13 [.219±.005]	11.01±0.13 [.434±.005]	8.28±0.13 [.326±.005]	49.00 (1.929)
3.3 VOLT	F				50.40 (1.984)
5 VOLT	E	10.0±0.13 [.394±.005]	15.46±0.13 [.609±.005]	12.73±0.13 [.501±.005]	49.00 (1.929)
3.3 VOLT	F				50.40 (1.984)
5 VOLT	E	11.01±0.13 [.433±.005]	16.47±0.13 [.648±.005]	13.74±0.13 [.541±.005]	49.00 (1.929)
3.3 VOLT	F				50.40 (1.984)

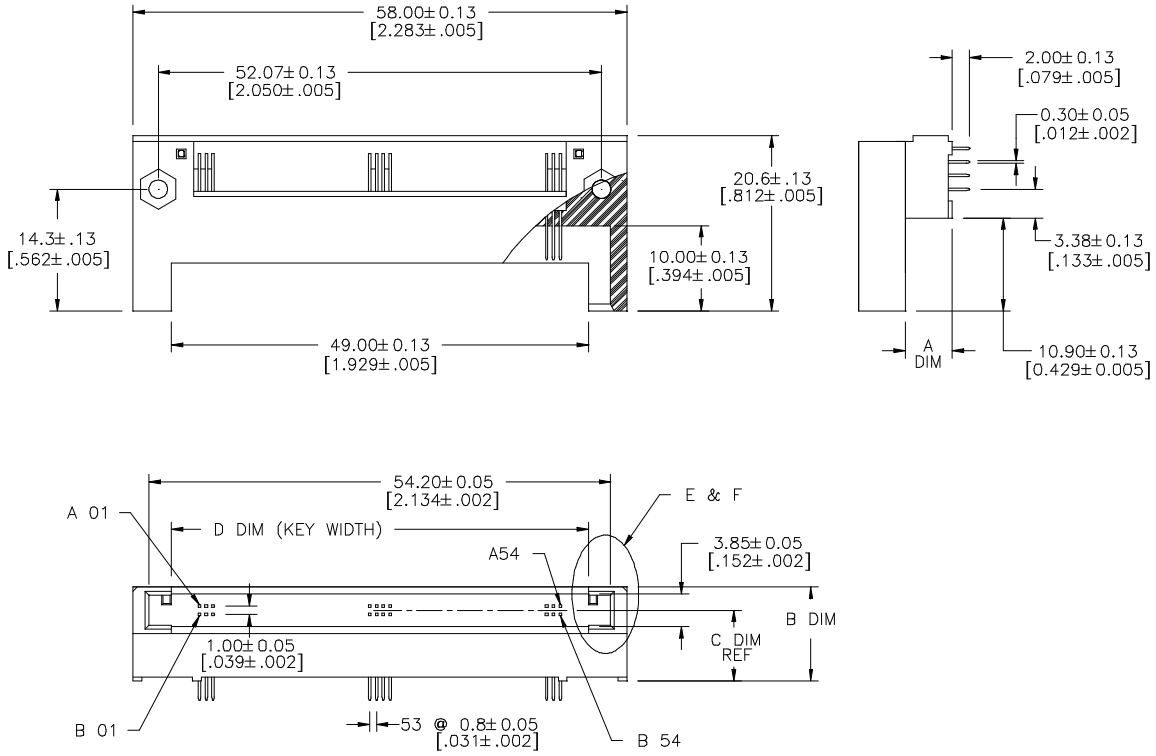


Figure 5-5: Small PCI Header Options (Single Card)

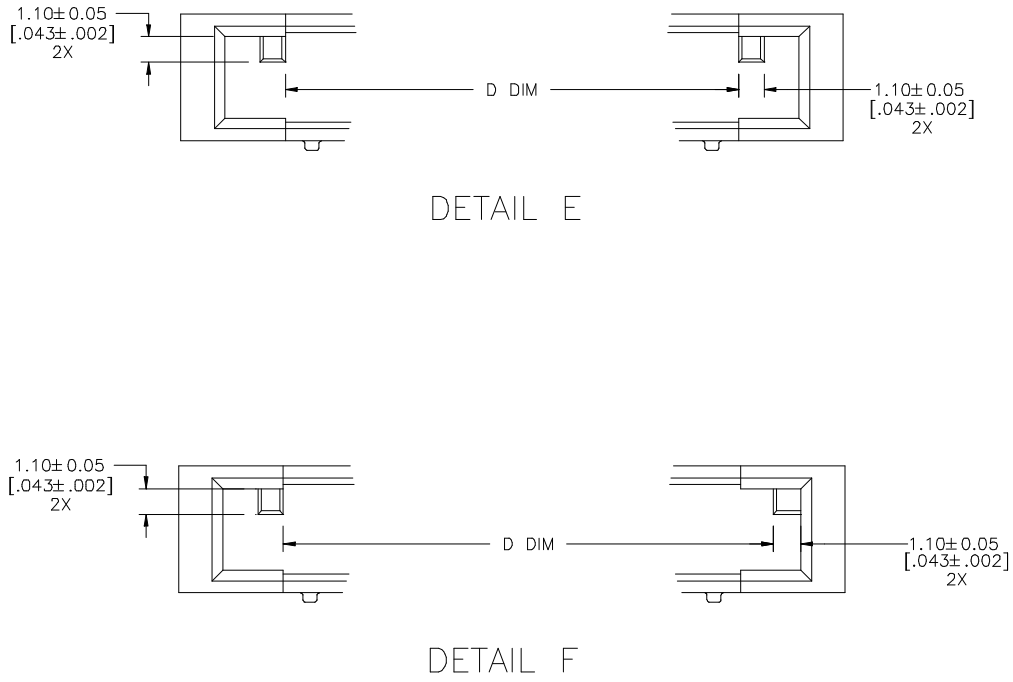


Figure 5-5-1: Small PCI Header Keying Details (Single Card)

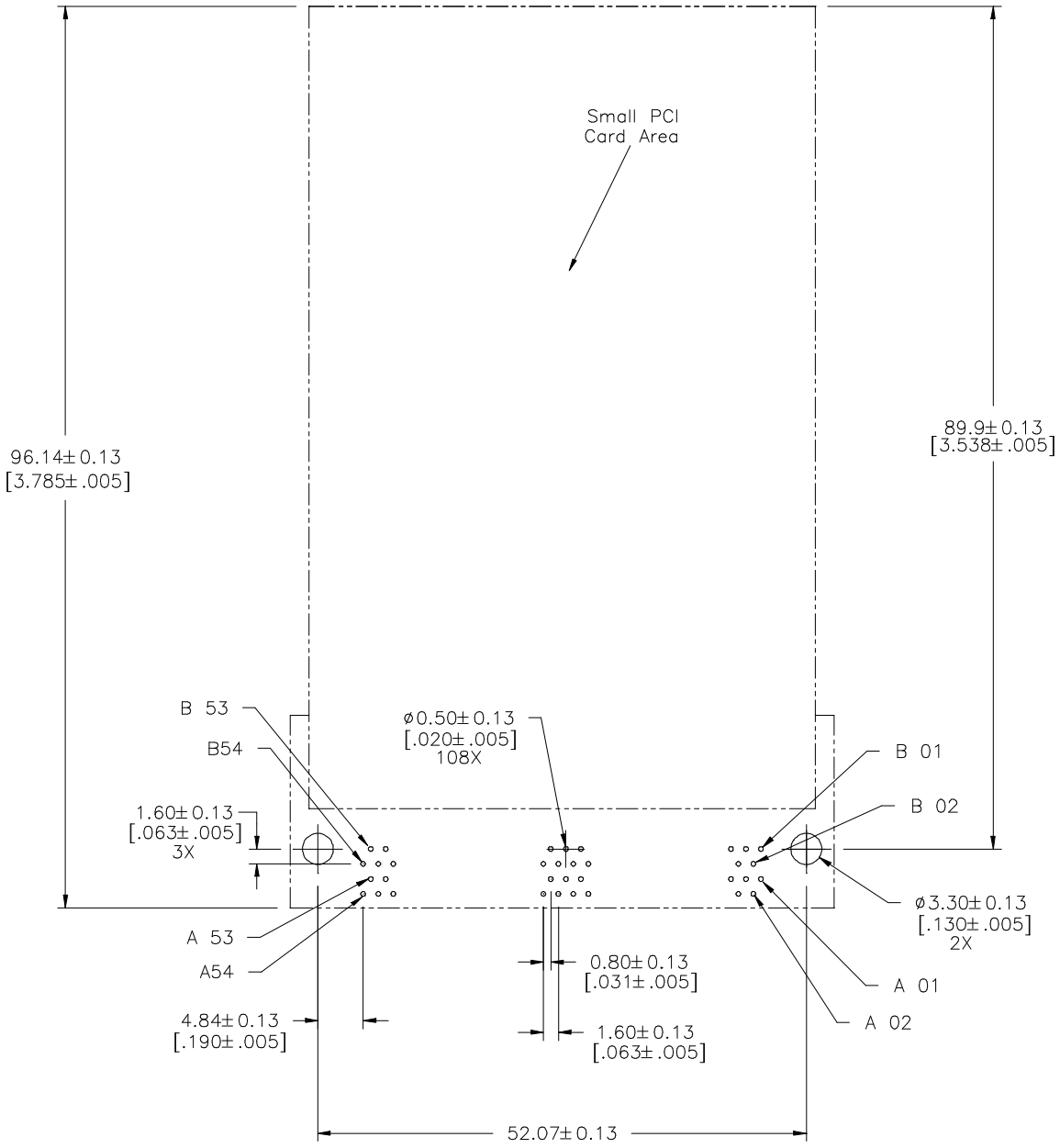


Figure 5-6: Board Layout (Single Card, Top View)

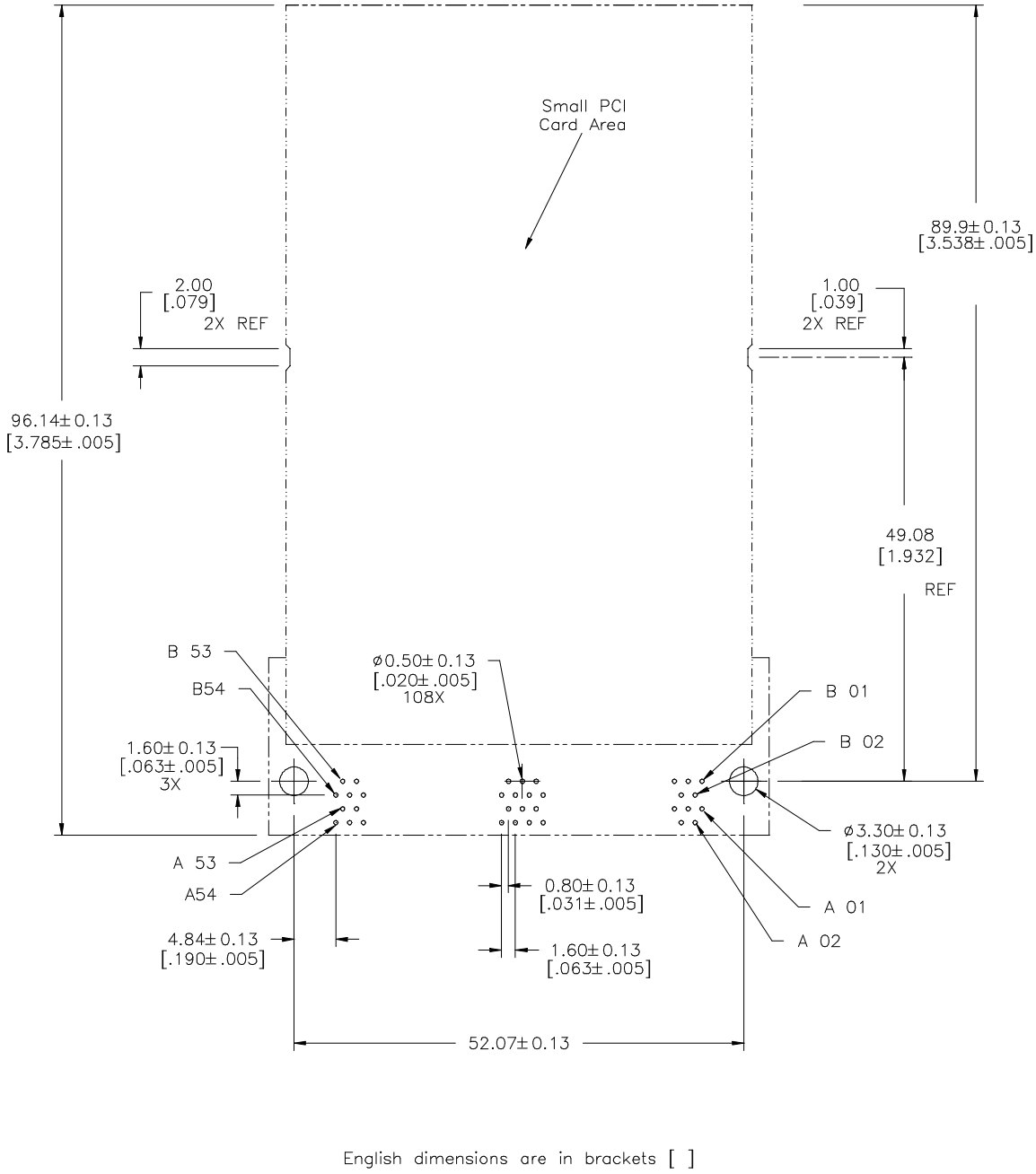


Figure 5-6-1: Board Layout (Single Card, Top View) With Optional Latching

CARD TYPE	DETAIL	A DIM	B DIM	C DIM	C2 DIM	D DIM
5 VOLT	E	5.55±0.13 [.219±.005]	16.47±0.13 [.649±.005]	8.28±0.13 [.326±.005]	13.74±0.13 [.541±.005]	49.00±0.13 (1.929±.005)
3.3 VOLT	F					50.40±0.13 (1.984±.005)

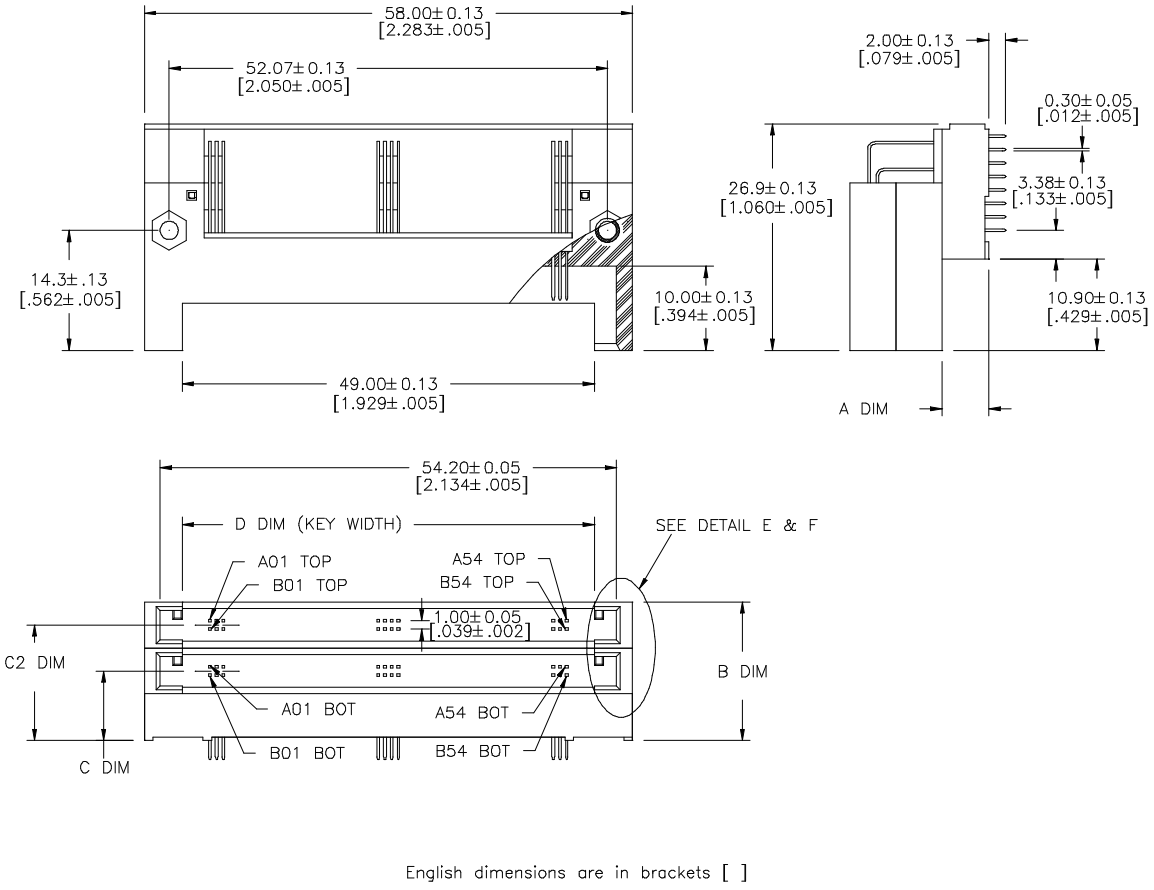


Figure 5-7: Small PCI Header Options (Double Card)

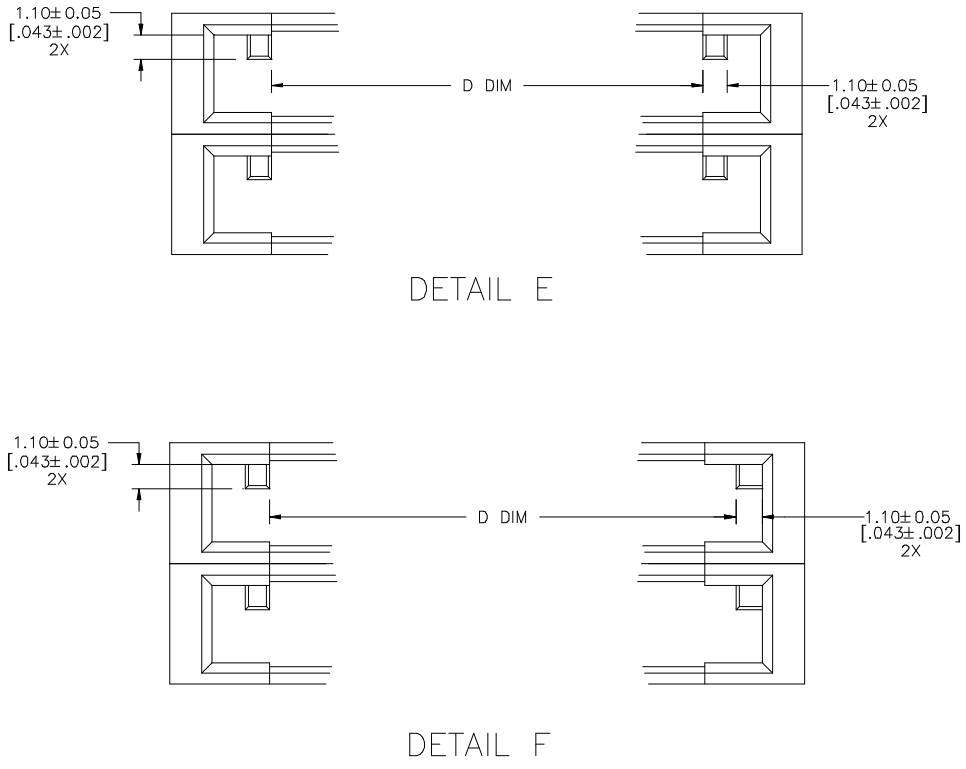


Figure 5-7-1: Small PCI Header Keying Details (Double Card)

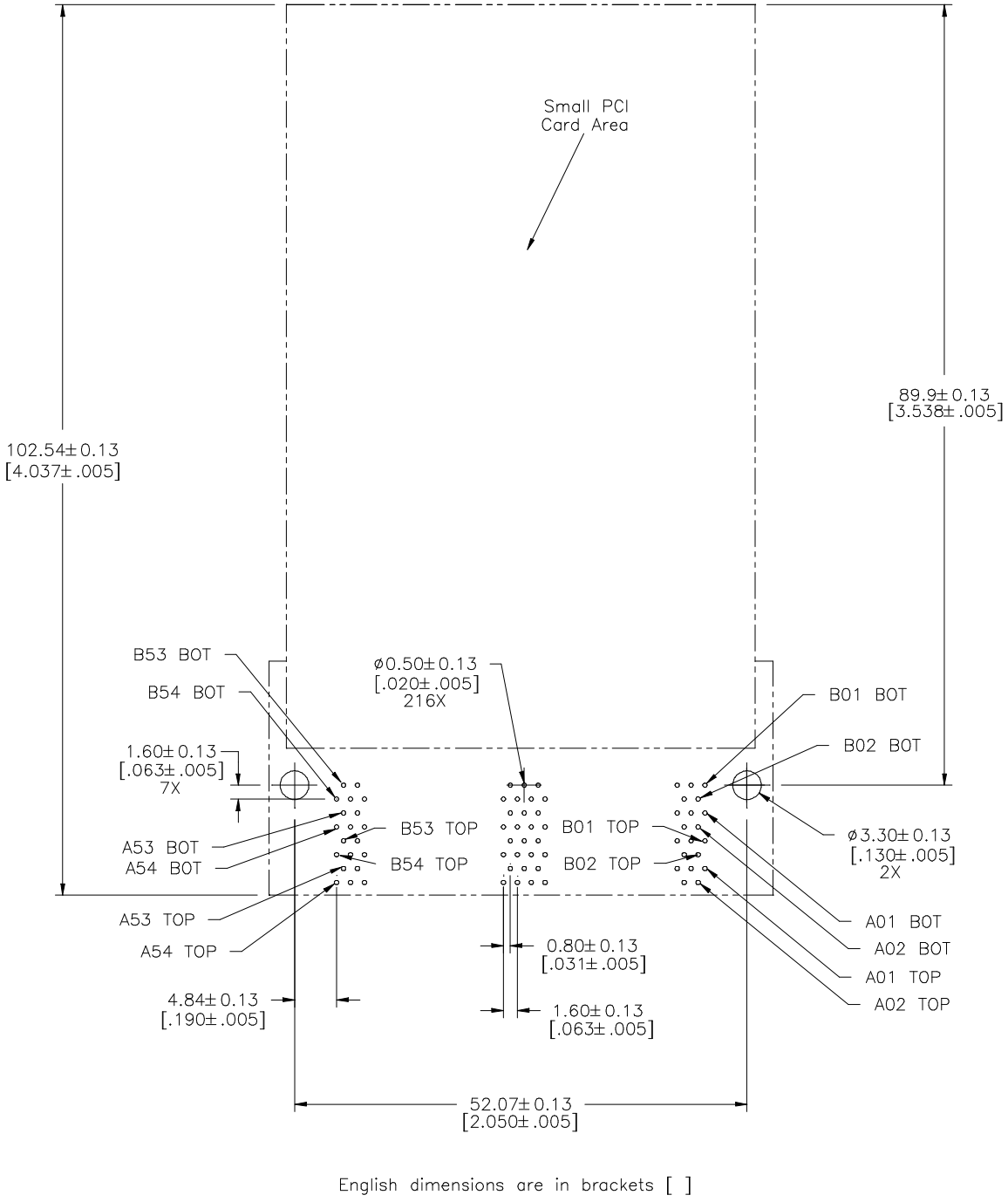


Figure 5-8: Board Layout (Double Card, Top View)

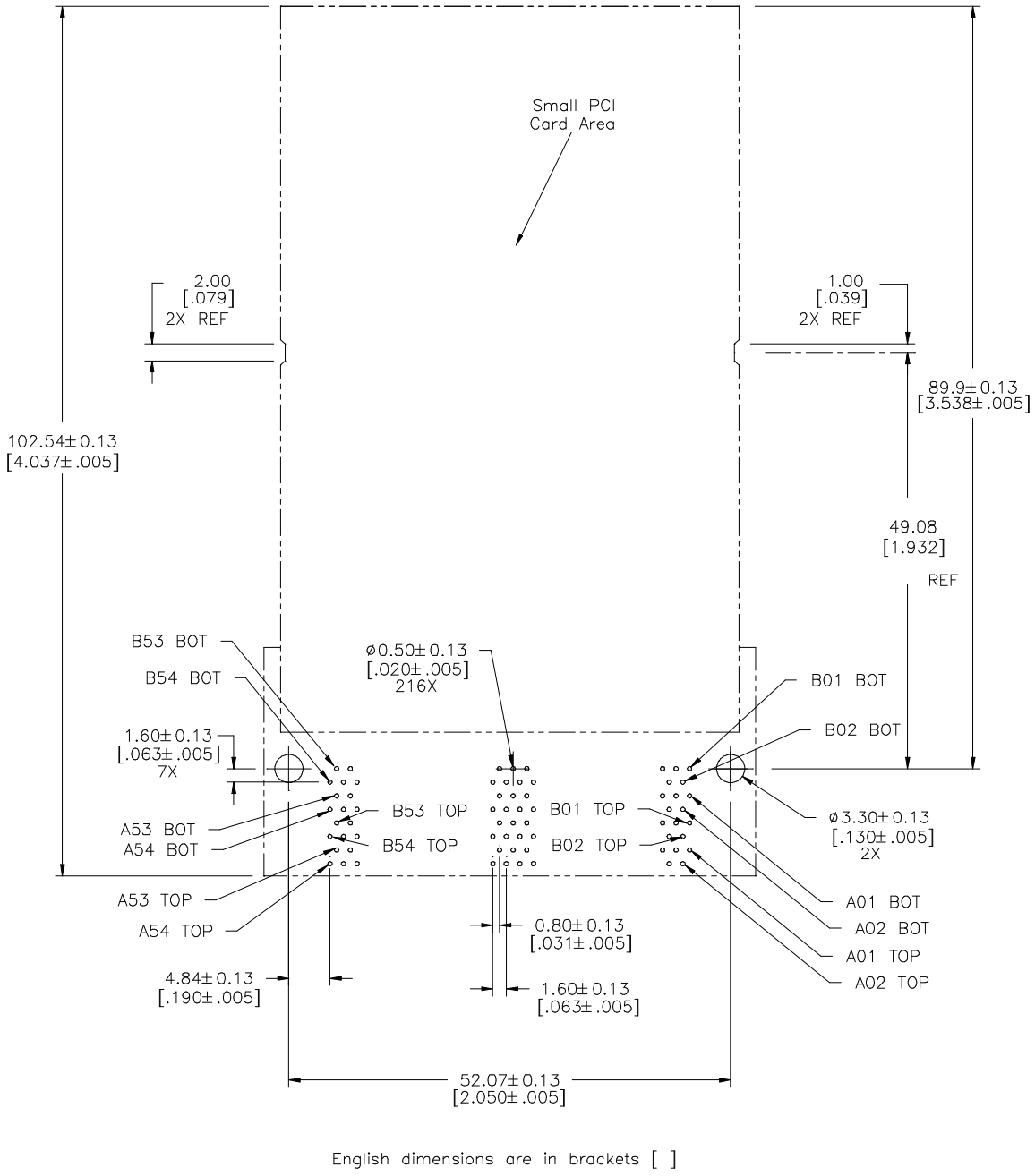


Figure 5-8-1: Board Layout (Double Card, Top View) With Optional Latching

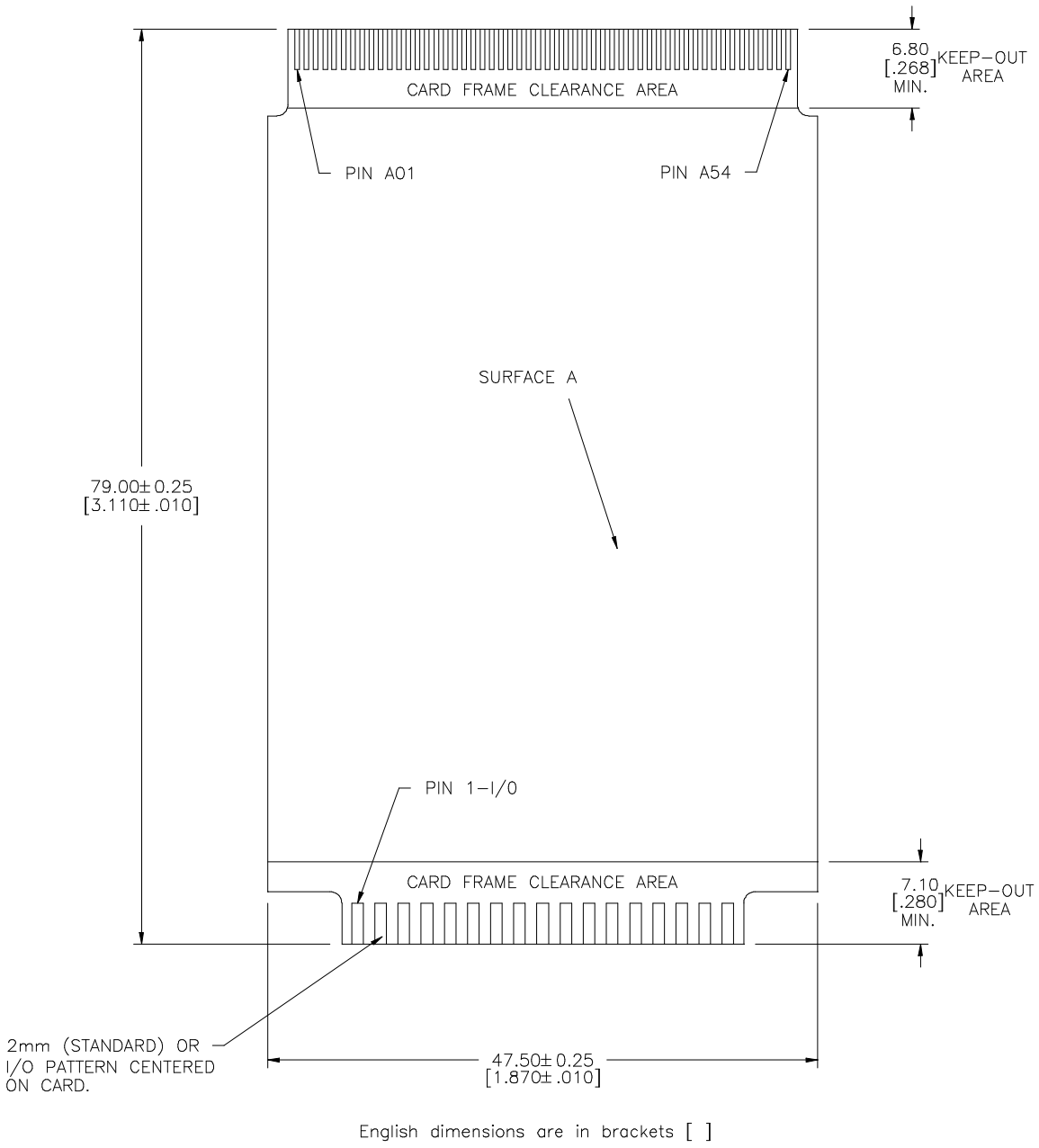


Figure 5-9: Small PCI Card (Surface A) With 2 mm I/O

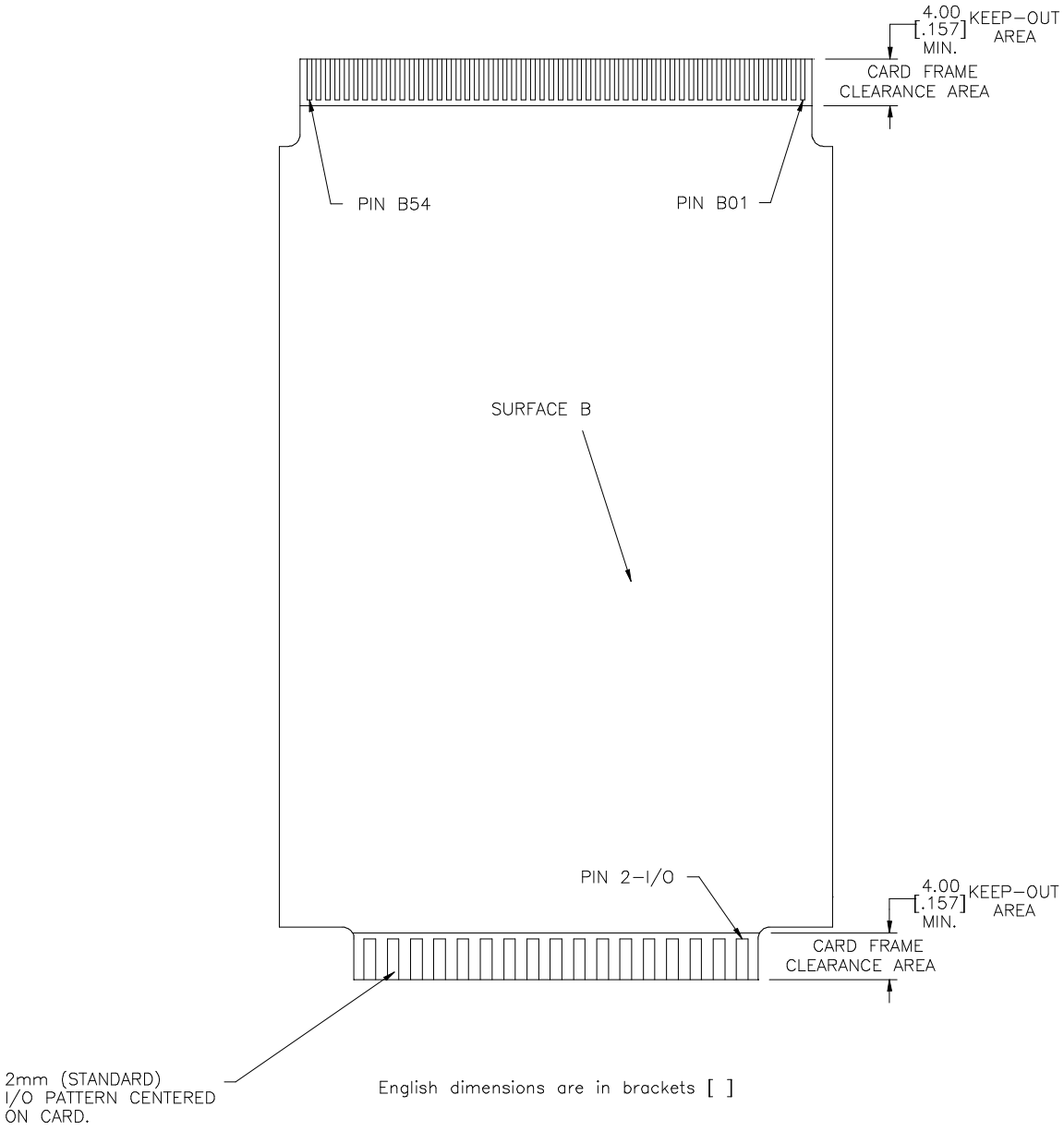
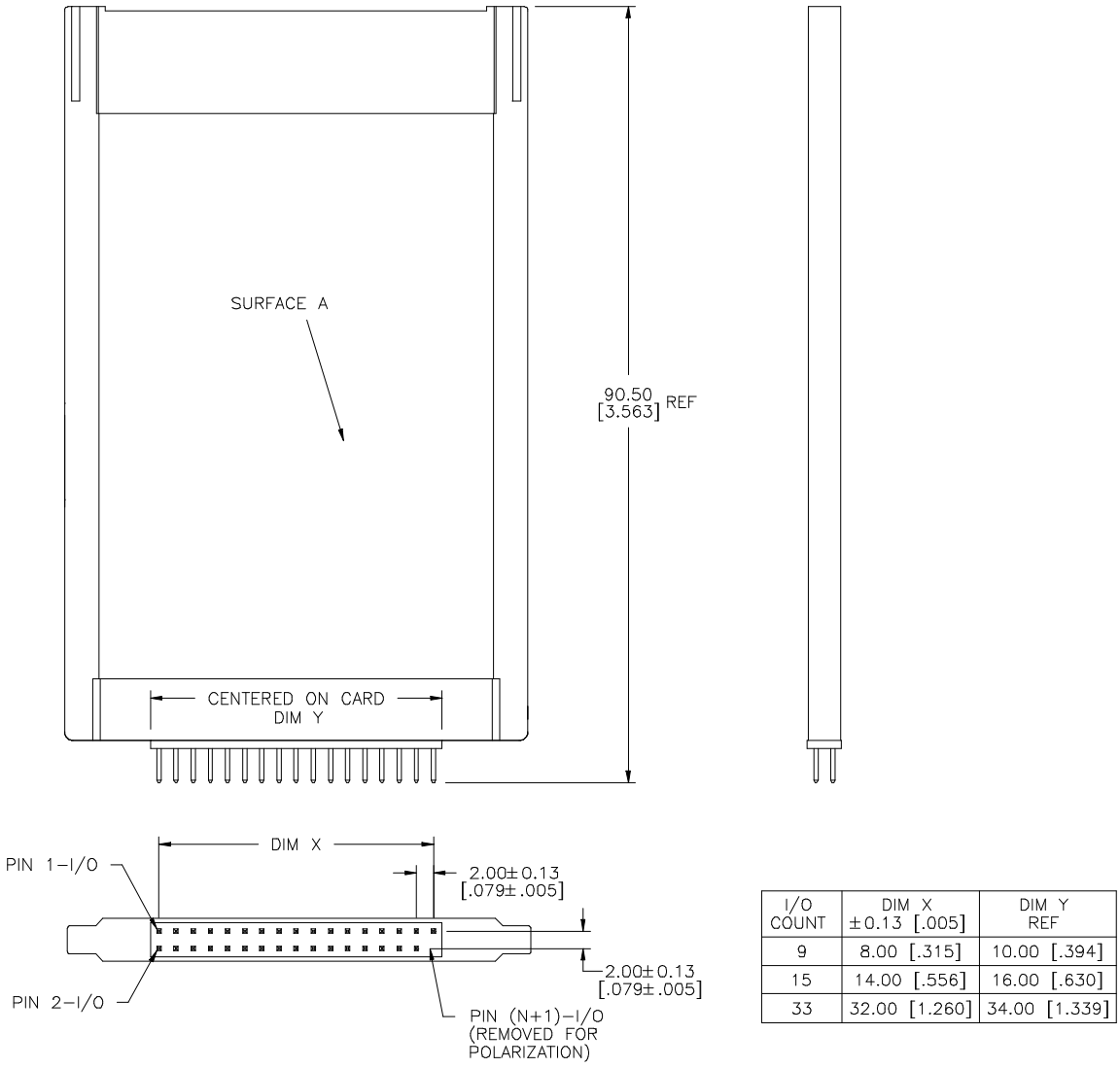
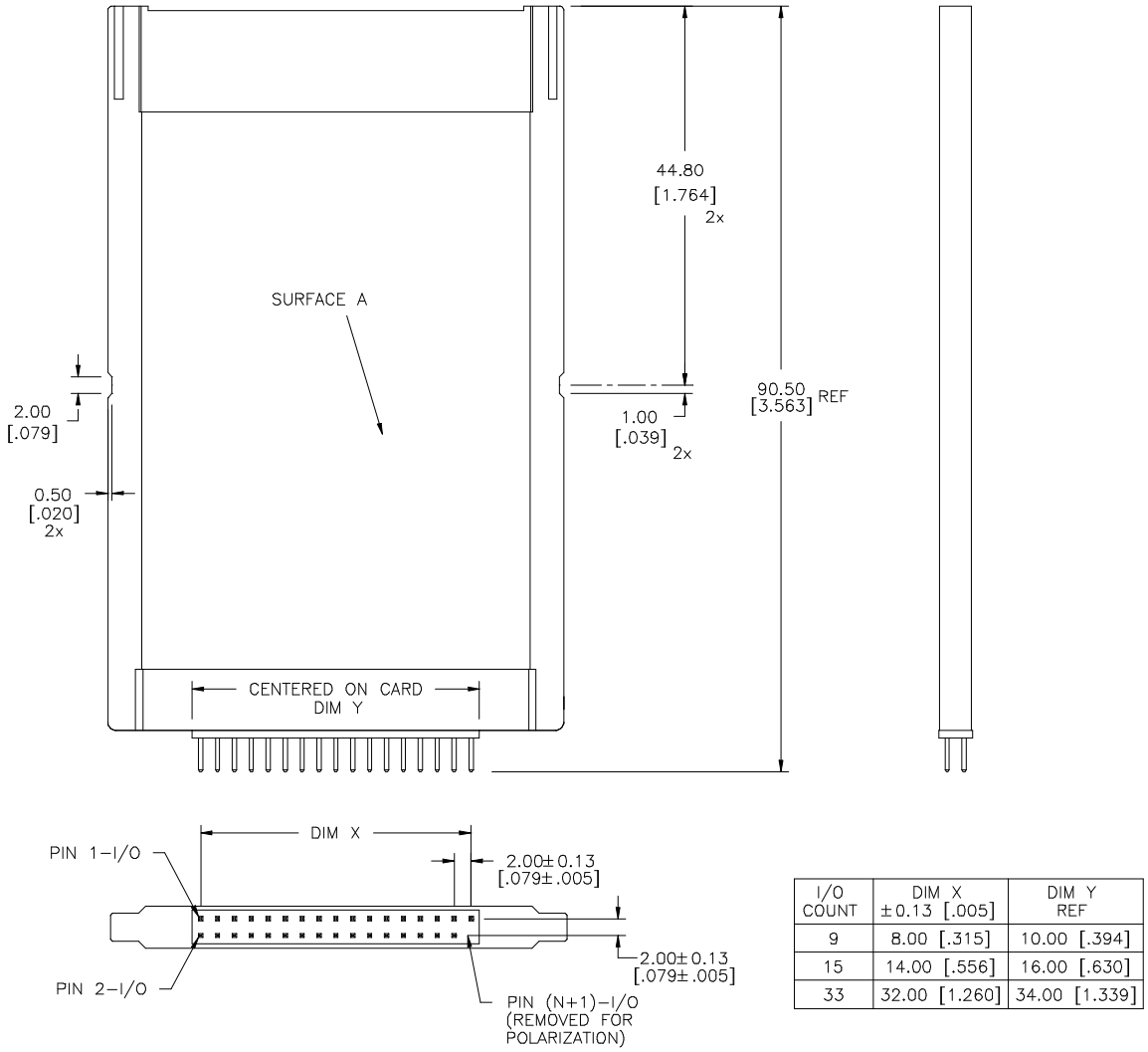


Figure 5-9-1: Small PCI Card (Surface B) With Straddle Mount I/O



I/O COUNT	DIM X ±0.13 [.005]	DIM Y REF
9	8.00 [.315]	10.00 [.394]
15	14.00 [.556]	16.00 [.630]
33	32.00 [1.260]	34.00 [1.339]

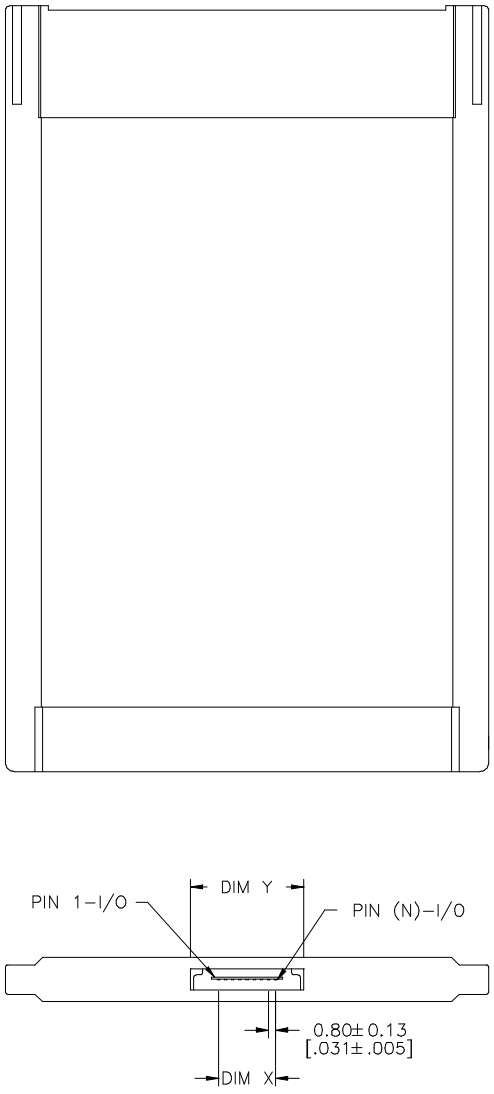
Figure 5-10: Small PCI Card Assembly With 0.8 mm Bus Connector, 2 mm I/O Connector, and Frame (Surface A Shown)



I/O COUNT	DIM X ±0.13 [.005]	DIM Y REF
9	8.00 [.315]	10.00 [.394]
15	14.00 [.556]	16.00 [.630]
33	32.00 [1.260]	34.00 [1.339]

English dimensions are in brackets [ ]

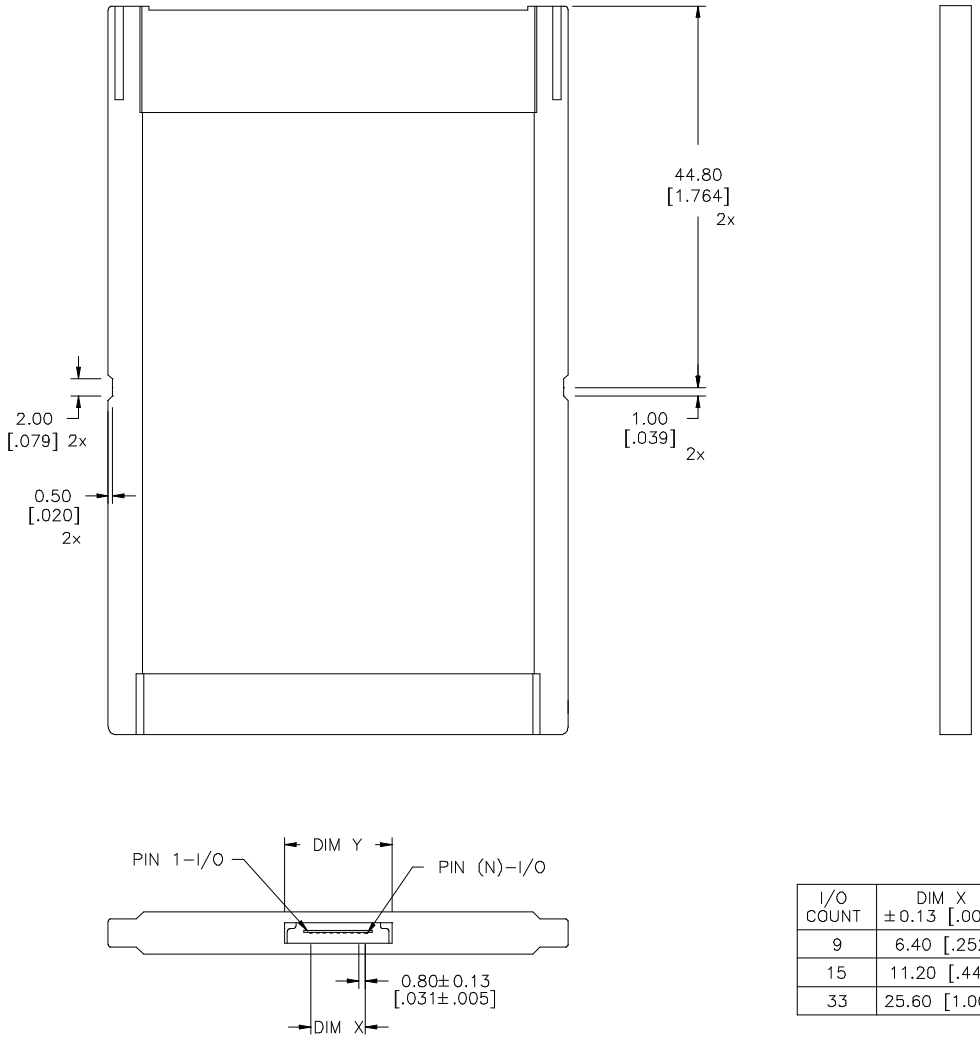
Figure 5-10-1: Small PCI Card Assembly With 0.8 mm Bus Connector, 2 mm I/O Connector, and Frame (Surface A Shown) With Optional Latching



I/O COUNT	DIM X ±0.13 [.005]	DIM Y REF
9	6.40 [.252]	14.26 [.561]
15	11.20 [.441]	19.06 [.750]
33	25.60 [1.008]	33.46 [1.317]

English dimensions are in brackets [ ]

Figure 5-11: Small PCI Card Assembly With 0.8 mm Bus Connector, 0.8 mm I/O Connector, and Frame (Surface A Shown)



I/O COUNT	DIM X ±0.13 [.005]	DIM Y REF
9	6.40 [.252]	14.26 [.561]
15	11.20 [.441]	19.06 [.750]
33	25.60 [1.008]	33.46 [1.317]

English dimensions are in brackets [ ]

Figure 5-11-1: Small PCI Card Assembly With 0.8 mm Bus Connector, 0.8 mm I/O Connector, and Frame (Surface A Shown) With Optional Latching

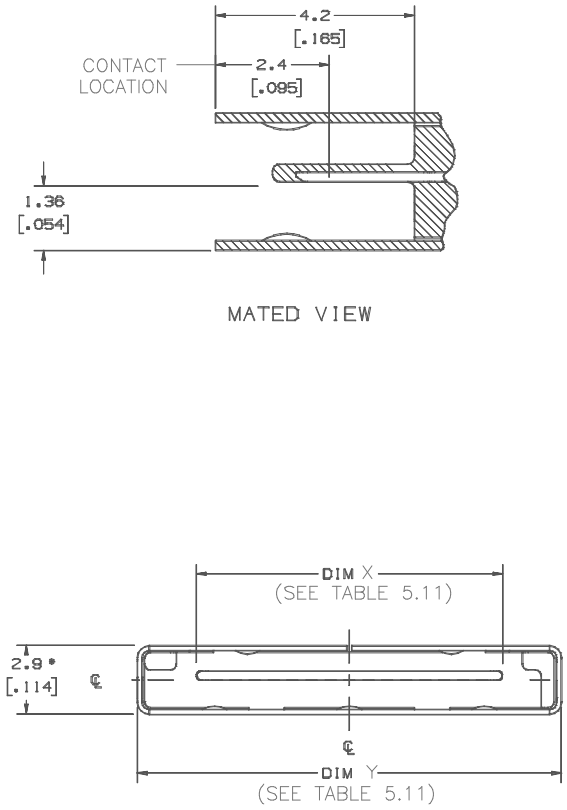


Figure 5-11-2: Small PCI I/O Header, 0.8 mm I/O Connector

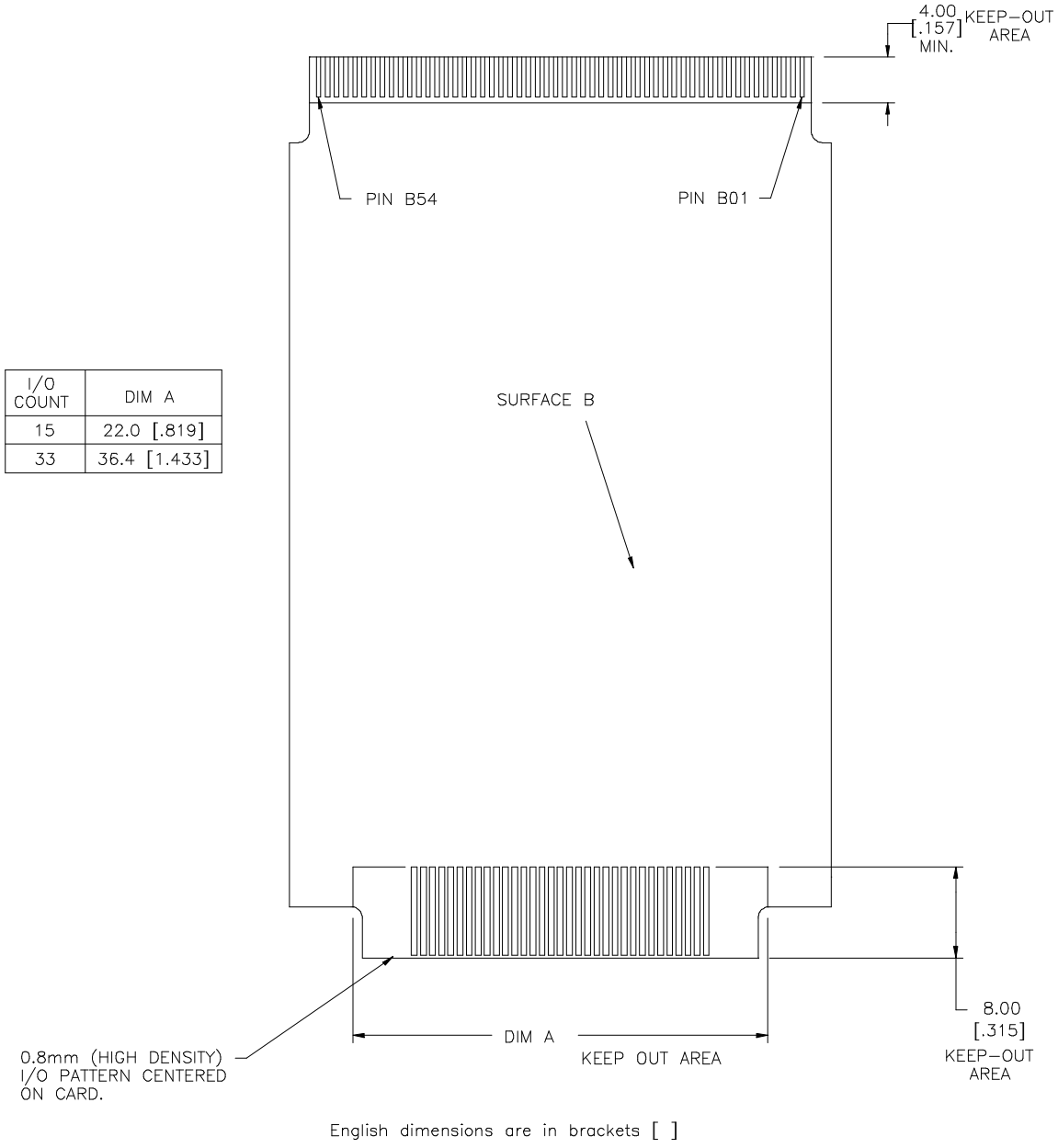


Figure 5-12: Small PCI Card (Surface B) With 0.8 mm SMT I/O

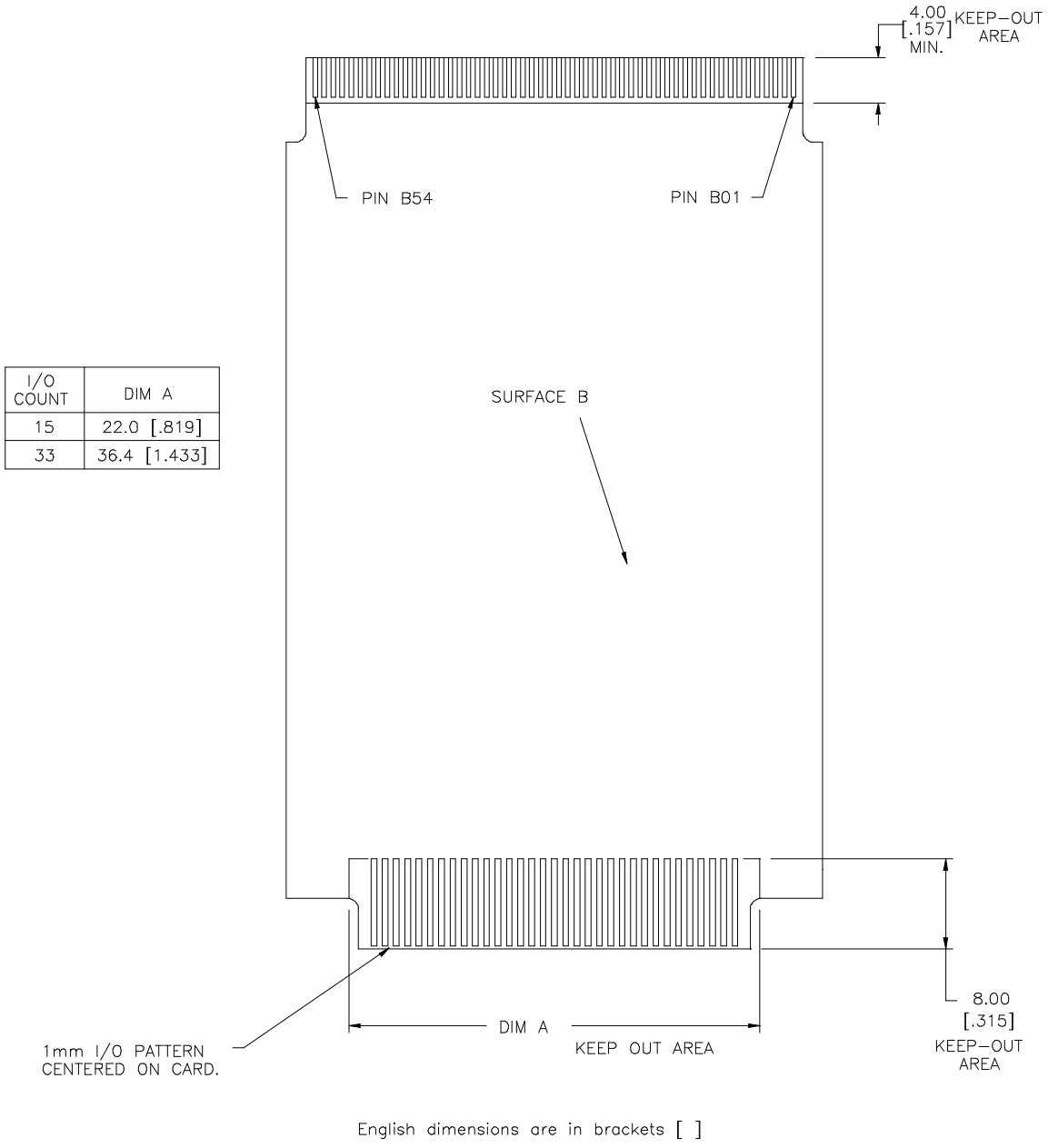


Figure 5-13: Small PCI Card (Surface B) With 2 mm SMT I/O

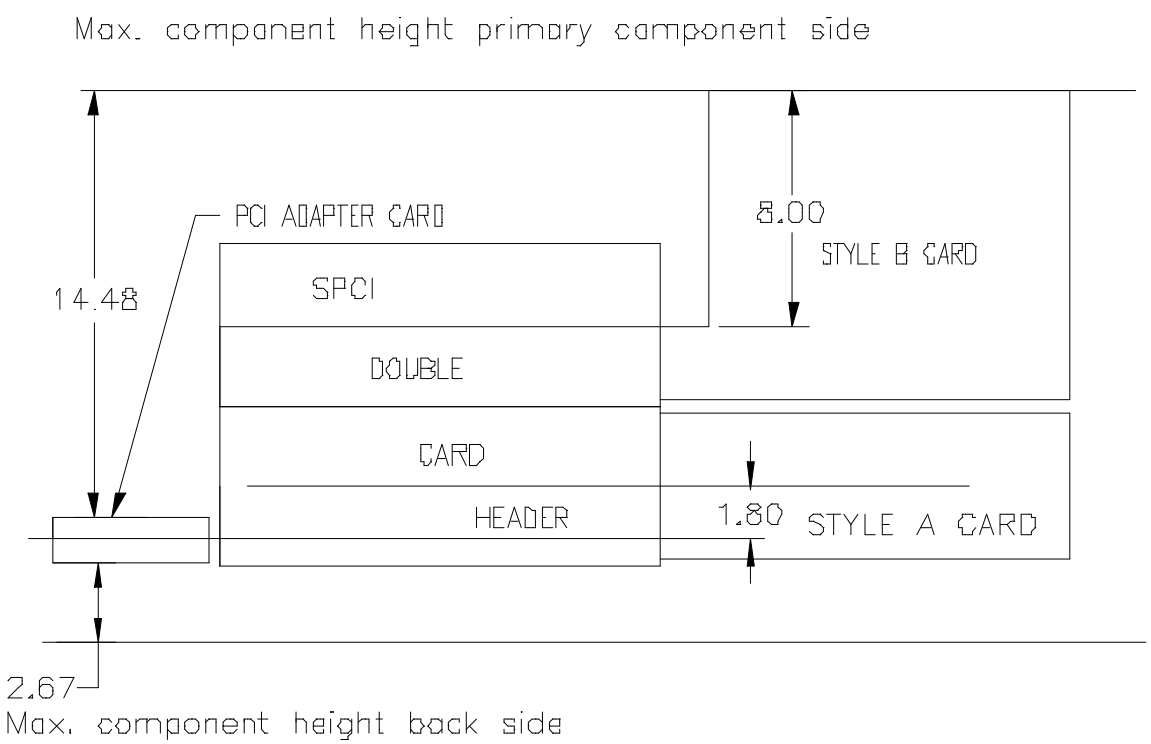


Figure 5-14-1: Example of Boundary Dimensions for PCI Adapter Applications (Style B Card at Max. 14.48 mm Height Restriction

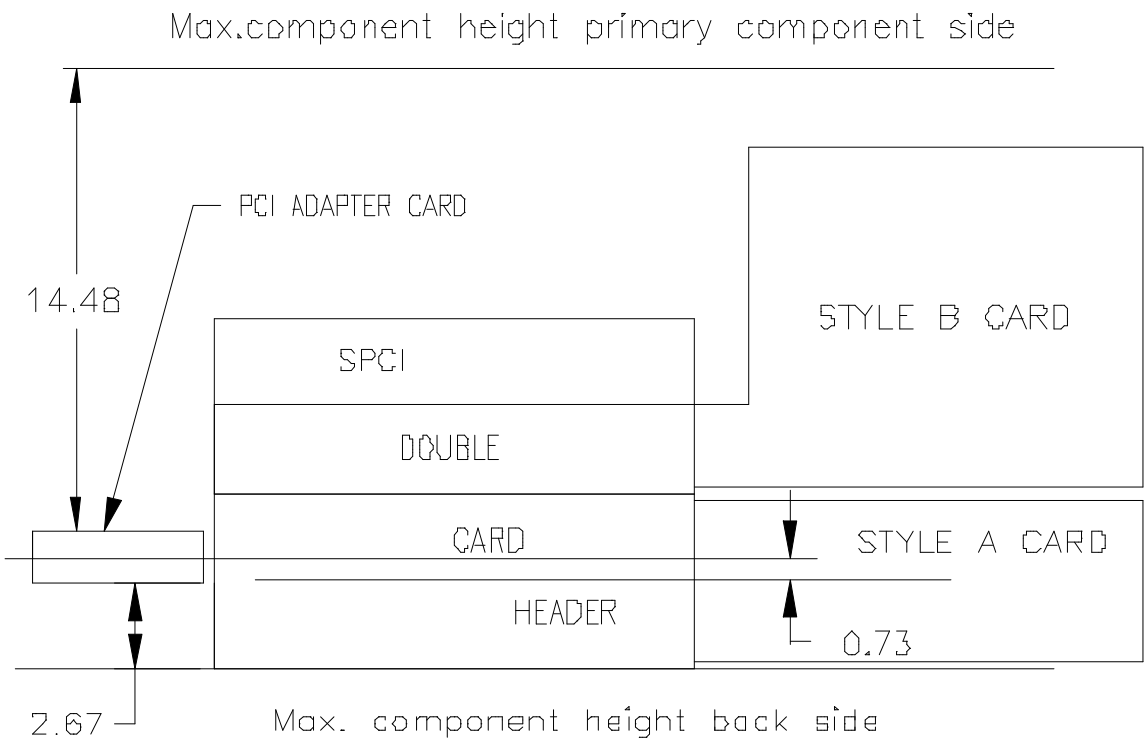


Figure 5-14-2: Example of Boundary Dimensions for PCI Adapter Applications (Header at 2.67 mm Max. Below Board Height Restriction)

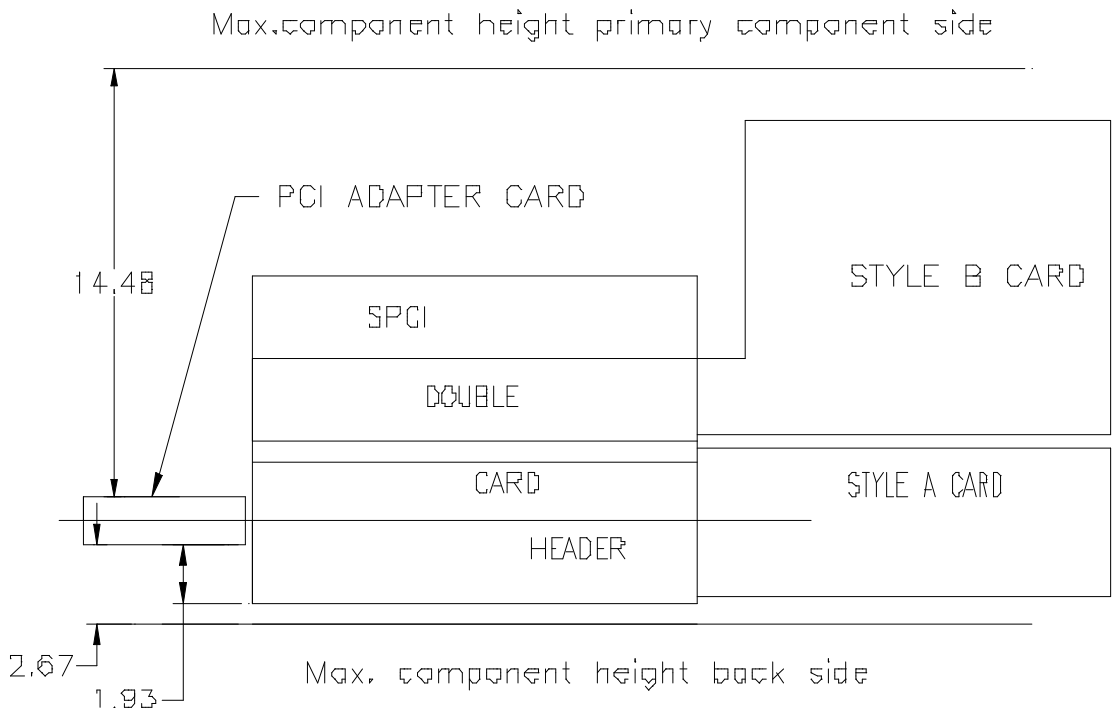


Figure 5-14-3: Example of Boundary Dimensions for PCI Adapter Applications (Center Line of Lower Header Coincident With PCI Adapter Card Center Line)

5.8. Reference Tables for I/O Pinouts

The I/O connector pinout is open to definition by manufacturers who will design this portion of the card to best complement the electrical and mechanical characteristics of their product. The following tables represent recommended I/O pinouts for various subsystems.

5.8.1. Recommended Pinout for Small PCI Ethernet Card (10BASE-T and AUI)

Table 5-6: Recommended Pinout for Small PCI Ethernet Card (10BASE-T and AUI)

No.	Description
1	10BASE-T Receive, Negative Phase
2	10BASE-T Receive, Positive Phase
3	Receive LED
4	AUI Receive, Negative Phase
5	AUI Receive, Positive Phase
6	10BASE-T Link Status LED
7	Cable Activity (Transmit) LED
8	AUI Transmit, Negative Phase
9	AUI Transmit, Positive Phase
10	Power out of PC card to external modules (+12V)
11	AUI Collision Input, Negative Phase
12	AUI Collision Input, Positive Phase
13	Ground
14	10BASE-T Transmit, Negative Phase
15	10BASE-T Transmit, Positive Phase

5.8.2. Recommended Pinout for Small PCI Token Ring (STP or UTP)

Table 5-7: Recommended Pinout for Small PCI Token Ring (STP or UTP)

No.	Description
1	Transmit Negative Phase
2	Transmit Positive Phase
3	Power into PC Card from External Supply
4	STP Receive, Negative Phase
5	STP Receive, Positive Phase
6	Transmit Status LED
7	Receive Status LED
8	Not connected
9	Not connected
10	Power out of PC card to external modules
11	UTP Receive, Negative Phase
12	UTP Receive, Positive Phase
13	Ground
14	STP Transmit, Negative Phase
15	STP Transmit, Positive Phase

5.8.3. Recommended Pinout for Single-Ended 8-bit SCSI

Table 5-8: Recommended Pinout for Single-Ended 8-bit SCSI

No.	Description
1	SCSI Data 0
2	Ground
3	SCSI Data 1
4	Ground
5	SCSI Data 2
6	Ground
7	SCSI Data 3
8	Ground
9	SCSI Data 4
10	Ground
11	SCSI Data 5
12	Ground
13	SCSI Data 6
14	Ground
15	SCSI Data 7
16	Ground
17	SCSI Data Parity
18	Ground
19	Term Power
20	Term Power
21	ATN
22	BSY
23	RST
24	Ground
25	MSG
26	SEL
27	C/D
28	I/O
29	Ground
30	REQ
31	Not connected
32	Ground
33	ACK

5.8.4. Recommended Pinout for Small PCI VGA/SVGA Video

Table 5-9: Recommended Pinout for Small PCI VGA/SVGA Video

No.	Description
1	Red Video
2	Green Video
3	Blue Video
4	Monitor ID Bit 2
5	Ground
6	Red Return
7	Green Return
8	Blue Return
9	Not connected
10	Sync Return
11	Monitor ID Bit 0
12	Monitor ID Bit 1
13	Horizontal Sync
14	Vertical Sync
15	Monitor ID Bit 3

Chapter 6
Configuration Space

6.1. Overview

Small PCI supports all features outlined in Chapter 6 of the *PCI Local Bus Specification*, Revision 2.1 or later.