MF1242-06

S1D15910 Series

Rev.2.2b

Rev.2.2b

Contents

1. DESCRIPTION

S1D15910 series is a color LCD segment driver with 8-gradation RAM incorporated, achieving low power consumption required for a mobile device and high image quality. It is designed to operate in coordination with S1D17C00/S1D17501/S1D17500, a common driver.

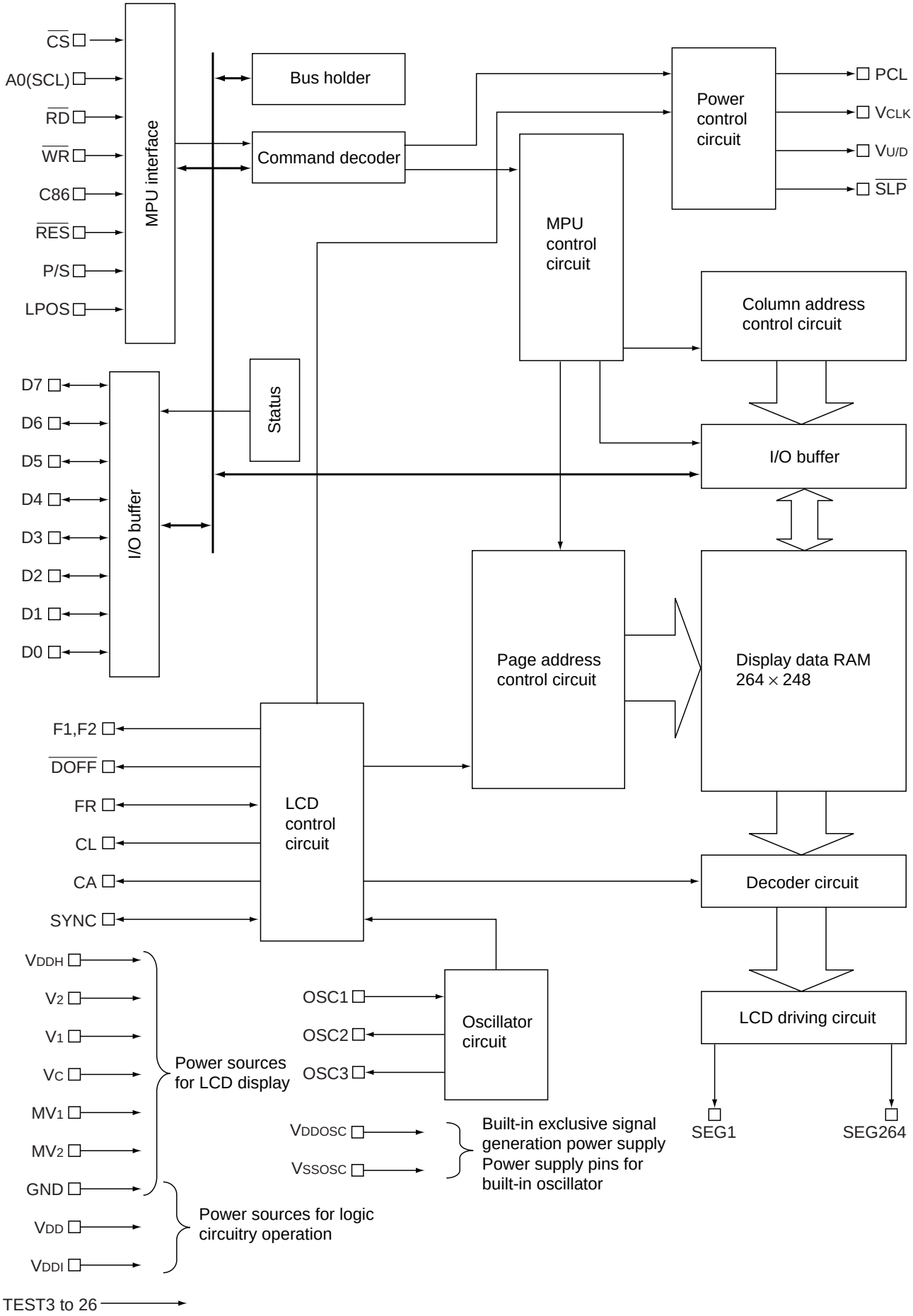
Capable of being directly connected to the MPU buses, it stores parallel or serial gradation display data transmitted from the MPU in the built-in display data RAM, and generates signals for driving the LCD, independent of the display RAM. It incorporates 360 LCD drive outputs and a 360 × 168 × 3-bit display RAM (8 gradations). The display area in the common direction can be set by a command to a multiple of four within the range from 40 to 168. One dot of pixels on the LCD panel is associated with three bits of the built-in RAM, and one chip can display 120 (RGB) ×168 pixels while two chips can display 240 (RGB) × 168 pixels. One pixel (RGB) is input as data of eight bits (RRRGGGBB).

In Write operation from the MPU to the built-in RAM, only minimal power consumption is required since no external operational clock is needed. In addition, adoption of the slim shape for this IC has made it easier to implement a narrow frame on the LCD panel.

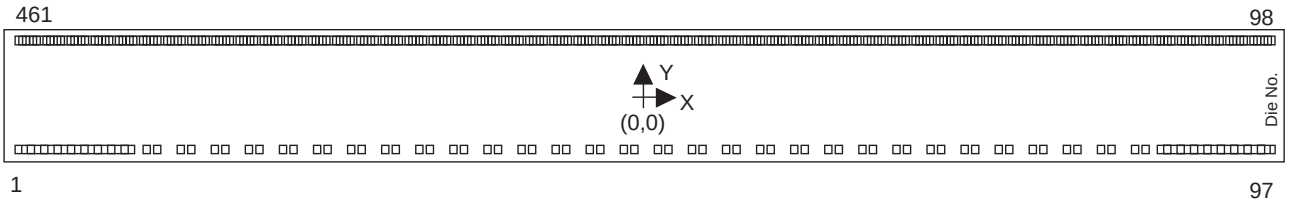
2. FEATURES

- Number of LCD driving outputs: 360
- Driving duty ratio: Variable between 1/40 and 1/168
- Low cross talk achieved by frame-less modulation, and concurrent display of 256 colors.
- Real 3-bit, 8-gradation display is achieved for red and green.
- For blue, intermediate tones can be set by a command, and 4-gradation display is achieved.
  01: Selectable from 001, 010 and 011.
  10: Selectable from 100, 101 and 110.
- Direct data display achieved by the display data RAM (when the LCD is set to normally black).
  RAM bit data: "000" ... OFF (black)
  "111" ... ON
  (RGB maximum luminance)
  (for inverted display)
- Partial display feature: Display can be partially deactivated for power saving. This is best suited for the waiting mode of a mobile device.
- Built-in RAM capacity: 3 × 360 × 168 = 181440 bits
- MPU interface
  Compatible with 80-Series and 68-Series 8-bit parallel microprocessors.
  Serial interface is also possible.
  Data can be input only on three pins: $\overline{CS}$, A0 (SCL) and D0 (data of D/C + 8 bits).
- Fully developed command features (area scroll, page & column automatic increment and power control)
- Continuity of columns when two chips are used:
  As an address in the RAM extends beyond one chip to be continued to the other, it can be accessed as if only one chip were used.
- Logic input signal circuitry: 1.7 to V_{DD}
  Logic output signal circuitry: 2.4 to 3.6 V
  LCD display circuitry: 5.4 to 7.2 V
- Slim shape of chips
- Shipping form: S1D15910D01B*: Au-Bump Chip
  S1D15910T****: TCP
- This product does not incorporate radiation-proof design or intensive light-shielding design.

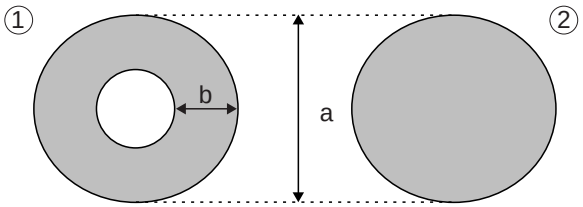
3. BLOCK DIAGRAM



4. PAD LAYOUT



Chip size:	21.01 × 2.16 mm
Chip thickness:	725 ± 25 µm <reference> : S1D15910D01B*
	300 ± 25 µm <reference> : S1D15910D11B*
	525 ± 25 µm <reference> : S1D15910D12B*
Circuit board potential	GND
Die No. name	D159AD1B
Bump size:	Tolerance of ±4 µm
	Upper side: 38 × 102 µm
	Lower side: 92 × 109 µm
Bump pitch:	57 µm on upper side
Bump height:	19.0 ± 5.5 µm <reference>
Alignment coordinates	① (-10156.3, 428.6) µm
	② (10156.3, 428.6) µm
Mark size	a = 80 µm
	b = 20 µm



5. PAD CENTER COORDINATES

Unit: µm

PAD No.	Pin Name	X	Y
1	NC	–10318.5	–916
2	NC	–10208.5	
3	V_{DDH}	–10098.5	
4	V_{DDH}	–9988.5	
5	V_2	–9878.5	
6	V_2	–9768.5	
7	V_1	–9658.5	
8	V_1	–9548.5	
9	V_C	–9438.5	
10	V_C	–9328.5	
11	MV_1	–9218.5	
12	MV_1	–9108.5	
13	MV_2	–8998.5	
14	MV_2	–8888.5	
15	GND	–8778.5	
16	GND	–8668.5	
17	V_{DD}	–8558.5	
18	V_{DD}	–8448.5	
19	FR	–8188.7	
20	CL	–8004.3	
21	PCL	–7626.7	
22	F1	–7442.3	
23	F2	–7064.7	
24	$\overline{DOFF}$	–6880.3	
25	CA	–6502.7	
26	SYNC	–6318.3	
27	$\overline{SLP}$	–5940.7	
28	V_{CLK}	–5756.3	
29	$V_{U/D}$	–5378.7	
30	OSC1	–5194.3	
31	OSC2	–4816.7	
32	OSC3	–4632.3	
33	V_{SSOSC}	–4254.7	
34	V_{DDOSC}	–4070.3	
35	$\overline{CS}$	–3692.7	
36	A0	–3508.3	
37	TEST3	–3130.7	
38	TEST4	–2946.3	
39	TEST5	–2568.7	
40	TEST6	–2384.3	
41	TEST7	–2006.7	
42	TEST8	–1822.3	
43	TEST9	–1444.7	
44	TEST10	–1260.3	
45	TEST11	–882.7	
46	TEST12	–698.3	
47	TEST13	–320.7	
48	TEST14	–136.3	
49	TEST15	241.3	
50	TEST16	425.7	

PAD No.	Pin Name	X	Y
51	GND*2	685.5	–916
52	V_{DDI}*2	795.5	
53	D0	1055.3	
54	D1	1239.7	
55	D2	1617.3	
56	D3	1801.7	
57	D4	2179.3	
58	D5	2363.7	
59	D6	2741.3	
60	D7	2925.7	
61	GND*2	3185.5	
62	V_{DDI}	3295.5	
63	TEST17	3775.3	
64	TEST18	3959.7	
65	TEST19	4337.3	
66	TEST20	4521.7	
67	TEST21	4899.3	
68	TEST22	5083.7	
69	TEST23	5461.3	
70	TEST24	5645.7	
71	GND*2	5905.5	
72	V_{DDI}*2	6015.5	
73	RD	6275.3	
74	WR	6459.7	
75	C86	6837.3	
76	$\overline{RES}$	7021.7	
77	PS	7399.3	
78	TEST25	7583.7	
79	TEST26	7961.3	
80	V_{DD}	8145.7	
81	LPOS	8523.3	
82	GND	8668.5	
83	GND	8778.5	
84	MV_2	8888.5	
85	MV_2	8998.5	
86	MV_1	9108.5	
87	MV_1	9218.5	
88	V_C	9328.5	
89	V_C	9438.5	
90	V_1	9548.5	
91	V_1	9658.5	
92	V_2	9768.5	
93	V_2	9878.5	
94	V_{DDH}	9988.5	
95	V_{DDH}	10098.5	
96	NC	10208.5	
97	NC	10318.5	
98	NC	10345.5	919.5
99	NC	10288.5	
100	SEG360	10231.5	

PAD No.	Pin Name	X	Y
101	SEG359	10174.5	919.5
102	SED358	*1	
457	SEG3		
458	SEG2	–10174.5	
459	SEG1	–10231.5	
460	NC	–10288.5	
461	NC	–10345.5	

1: For Bump No. n, 10231.5-57 (n-100) Pins marked with *2 are those which do not need to be connected.
*2: Those pins which are used to pull-up or pull-down their neighboring pins. Consequently, they cannot be used for power supply purposes.

6. PIN DESCRIPTION

Power Pins

Pin Name	I/O	Description	Number of pins
Substrate Potential		Circuit board potential of IC is GND. Make it GND when circuit board potential is fixed.	
V_{DD}	Power Supply	Connected to V_{CC}, the system power supply. If the system supply voltage is 2.4 V or less, it is required to input power supply of 2.4 V or more.	1
V_{DDI}	Input Power Supply	Connects the power supply for input signals.	1
V_{DDOSC}	Power Supply	V_{DD} power pin for the built-in oscillation circuit	1
V_{SSOSC}	Power Supply	GND power pin for the built-in oscillation circuit	1
GND	Power Supply	Connected to the system ground.	2
V_{DDH}	Power Supply	A power supply for LCD driving. Can be connected to V_2.	2
V_2,V_1,V_C MV_1, MV_2	Power Supply	Multi-level power supplies for LCD driving. Relations of potential magnitudes among different levels: $V_{DDH} \geq V_2 > V_1 > V_C > MV_1 > MV_2 \geq GND$	Two each.

MPU-related Pins (V_{DDI} connection pins)

Pin Name	I/O	Description	Number of pins
D7 to D0	I/O	These are 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses. Pin D0 functions as a data input pin when serial data are input (P/S = LOW).	8
A0(SCL)	I	Typically, connected to the low-order bit of the MPU address bus and used to identify data or commands. LOW : Indicates that D7 through D0 are commands. HIGH : Indicates that D7 through D0 are data. Functions as data capture clock input pin when serial data are input (P/S = LOW). Captures data on the rising edge of the clock.	1
$\overline{RES}$	I	Setting $\overline{RES}$ to LOW initializes the setting. Reset operation is performed on the level of the $\overline{RES}$ signal. See page 36 for the status after resetting.	1
$\overline{CS}$	I	Input pin for the chip select signal. When $\overline{CS}$ is in the non-active status, D7 through D0 are in the high impedance status.	1
P/S	I	Parallel/serial switching input pin. HIGH : Parallel input LOW : Serial input	1
$\overline{RD}$ (E)	I	• When connected to the 80-Series MPU: Active low. This pin connects the signal of the 80-Series MPU. While this signal is LOW, the data bus is in the output status. • When connected to the 68-Series MPU: Active high. Functions as an enable clock input pin for the 68-Series MPU.	1

Pin name	I/O	Description	Number of pins
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to the 80-Series MPU: Active low. This pin connects the $\overline{WR}$ signal of the 80-Series MPU. The signal on the data bus is latched on the rising edge of the $\overline{WR}$ signal. • When connected to the 68-Series MPU: Functions as the input pin for Read/Write control signals. R/$\overline{W}$ = HIGH : Read R/$\overline{W}$ = LOW : Write	1
C86	I	MPU interface switching pin. C86 = HIGH : 68-Series MPU interface C86 = LOW : 80-Series MPU interface	1
LPOS	I	Input pin for IC mounting location. Determines column address assignment and the master/slave status of the display signals for using two of this IC's. Inputs specification for right- or left-side location for the IC, as the chip bump side is placed up while the driver output pin side is placed on the upper side. LPOS = HIGH : Left-side. LPOS = LOW : Right-side. • Column address assignment: Determined by inputs for LPOS and parameter P11 of DATCTL. LPOS : HIGH LOW P11: 0 0 to 119 (master) 120 to 239 (slave) P11: 1 239 to 120 (slave) 119 to 0 (master) • Determining which is master/slave: According to the table above, the chip with column address 0 becomes the master. Caution: Until LPOS:LOW, after resetting, DATCTL becomes P11:0 being in slave condition. Therefore, when switching to the master, it is necessary to set to P11:1 immediately (within 1 ms). FR SYNC When being the master: Output Output When being the slave: Input Input	1

LCD Drive Circuit Signals

Pin name	I/O	Description	Number of pins
OSC1	I	Display clock external input pin. Input external clock signals through this pin. Driven by V_{DDOSC}.	1
OSC2	O	Signal generation clock output pin. When using the internal signal generation circuit, connect this pin to the OSC1 via a capacitor. Keep the connection of this pin open when external clock signals are being input. Driven by V_{DDOSC}.	1
OSC3	O	Signal generation circuit pin. When using the internal signal generation circuit, connect this pin to the OSC1 via a resistor. Keep the connection of this pin open when external clock signals are being input. Driven by V_{DDOSC}.	1
CL	O	Common clock output pin. Driven by V_{DD}. Connected to the CL pin of the common driver.	1
FR	I/O	I/O pin for LCD AC signals. Driven by V_{DD}. Connected to the FR pin of the common driver. Also connected to the other segment driver in order to achieve synchronization of the FR pins between the segment drivers.	1
SYNC	I/O	I/O pin for signals to synchronize the segment drivers. Connected to the SYNC pin of the other segment driver. Driven by V_{DD}.	1
CA	O	Output pin for the field start signal. Driven by V_{DD}. Connected to the YD pins of all the common drivers.	1
$\overline{DOFF}$	O	LCD display blanking control pin. Driven by V_{DD}. Connected to the $\overline{DOFF}$ pin of the common driver.	1
F1 and F2	O	Output pins for driving pattern signals. Driven by V_{DD}. F1 and F2 are connected to the F1 and F2 pins of the common driver.	One each.
SEGn	O	Output pin for LCD segment driving. Driven by V_{DDH}.	360

Control Pins

Pin name	I/O	Description	Number of pins
V_{CLK} $V_{U/D}$	O	Power control output pins. Driven by V_{DD}. Used for controlling electronic volume of the power IC. V_{CLK} outputs counter clocks of the power supply while $V_{U/D}$ outputs counting direction (up or down) of the power counter. This output is controlled by a command.	One each.
$\overline{SLP}$	O	Sleep control pin. When set to the sleep status by the MPU, the sleep mode is entered. Driven by V_{DD}. Connected to the $\overline{SLP}$ pin of the power IC.	1
PCL	O	Power boost clock output pin. Driven by V_{DD}. Connected to the PCL pin of the power IC.	1
TEST3 to 26	HIMP	Pin for LSI test. They are driven by V_{DDI}, so that set it to OPEN or V_{DDI} or GND connection.	24

7. FUNCTIONAL DESCRIPTION

MPU Interface

S1D15910 series transfers data via input to 8-bit bidirectional data buses (D7 to D0) or serial input.

8-bit bidirectional data bus

Set the P/S pin to HIGH.
Setting the C86 pin to HIGH or LOW allows it to be directly connected to either the 80-Sereis or 68-Series MPU, as shown in the table below.

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	68-Series MPU bus	$\overline{CS}$	A0	E	R/W	D0 to D7
LOW	80-Series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

S1D15910 series identifies the data bus signal as shown below, according on the combination of A0, E and R/$\overline{W}$ ($\overline{RD}$, $\overline{WR}$) signals.

With the S1D15910 series, D0 through D7 enter the high impedance status except for the chip select mode and input is disabled for the A0, $\overline{RD}$ and $\overline{WR}$ pins.

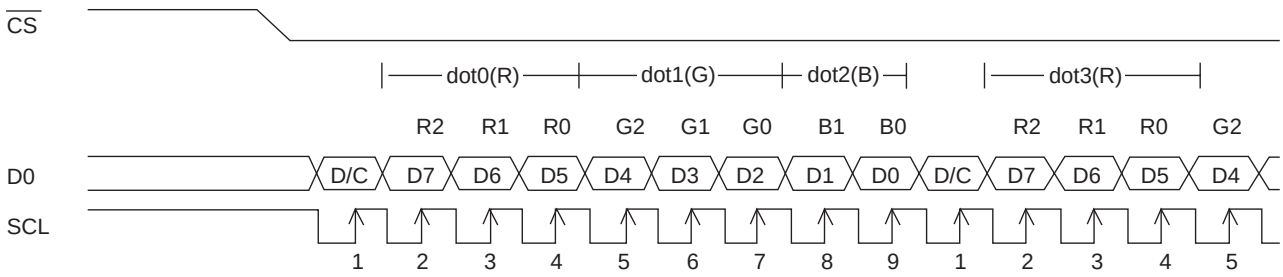
Common	68-Series		80-Series		Function
A0	R/$\overline{W}$	E	$\overline{RD}$	$\overline{WR}$	
1	0	1	1	0	Writes display data.
1	1	1	0	1	Reads display data.
0	1	1	0	1	Reads status.
0	0	1	1	0	Writes control data in the internal register. (Command)

Serial data input

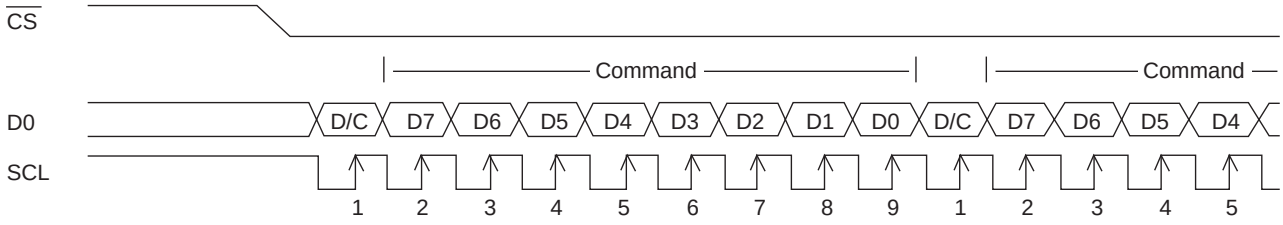
Set the P/S pin to LOW.
Inputting a command and data is enabled using the three pins, $\overline{CS}$, A0 (SCL) and D0 (SI). Data cannot be read. The data input format is D/C + 8-bit data. Follow the input methods below for inputting a command, parameter or gradation data.

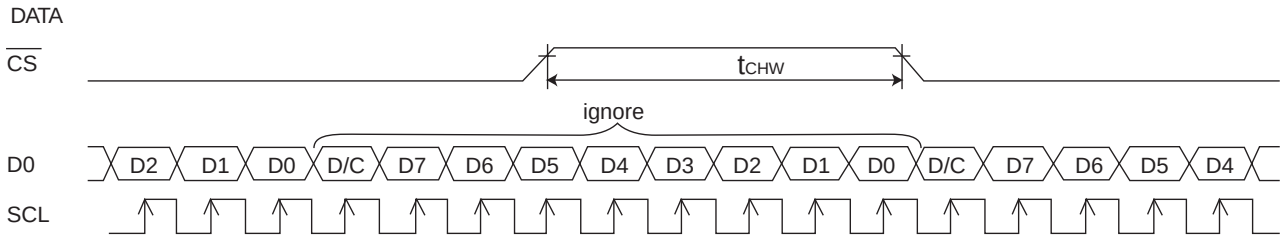
The H pulse width on $\overline{CS}$ is minimum 100 ns. The H pulse width on $\overline{CS}$ is not relative to the SCL cycle..
If $\overline{CS}$ turns to HIGH before all 9 bits are input for D/C through D0, the data become invalid. For continuing to input, re-input the data including input on D/C.
D/C corresponds to the A0 of the parallel data.

For inputting data:



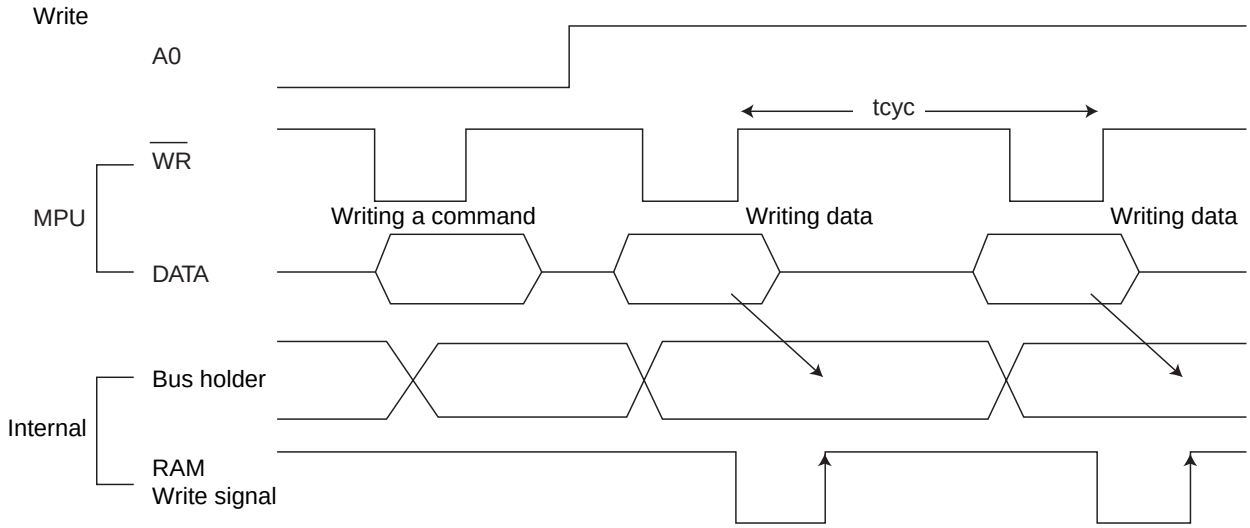
For inputting a command:

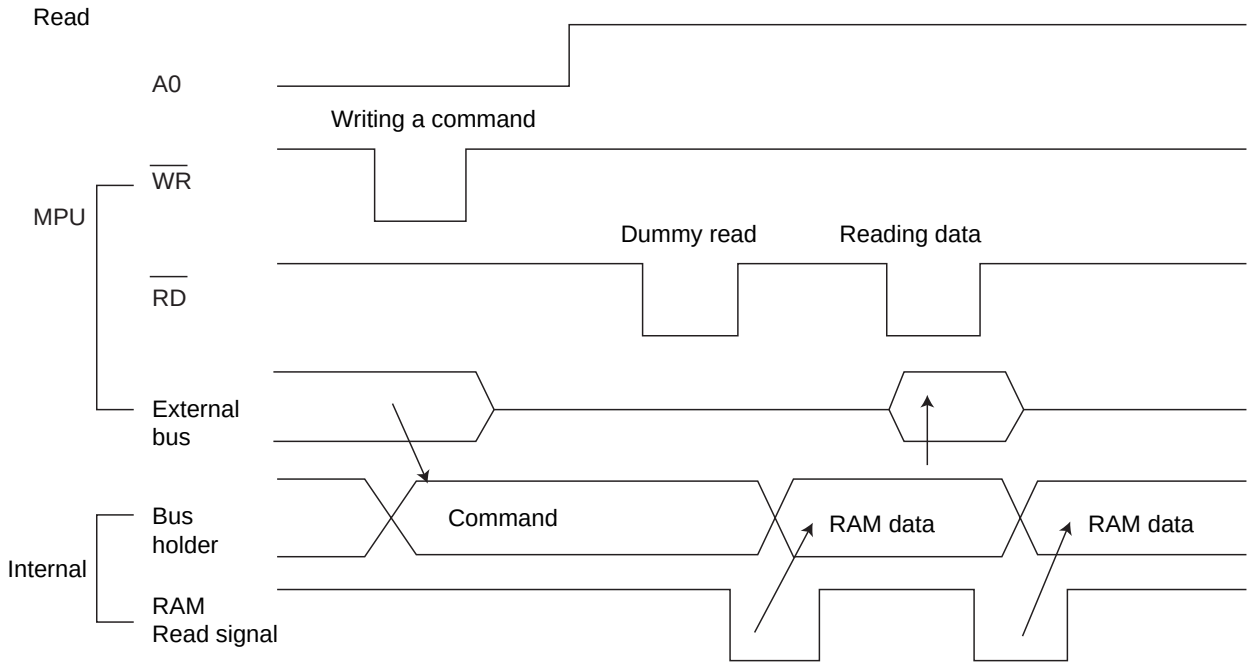




Access to Display Data RAM and Internal Registers

In order to match the operating frequencies of the MPU, the display data RAM and internal registers with each other, the S1D15910 series can perform a series of pipeline processing between LSI's via the bus holder attached to the internal data bus. Therefore, the restrictions on access to the S1D15910 series as viewed from the MPU side is mostly the cycle time rather than the access time of the display data RAM (t_{ACC}). If the cycle time is not satisfied, insert the NOP instruction in the MPU, which is the equivalent of performing wait operation in its apparent effect.





Page Address Control Circuit

This circuit performs address control in the page direction when the display data RAM is accessed from the MPU or the contents of the display data RAM is read for LCD display.

The Page Address Set command can be used to specify the page address area (the start and end pages). If the Scan Direction Select command is used to specify scanning in the page direction, the column address is incremented by one as the address is incremented from the start page to the end page, and the page address returns to the start page.

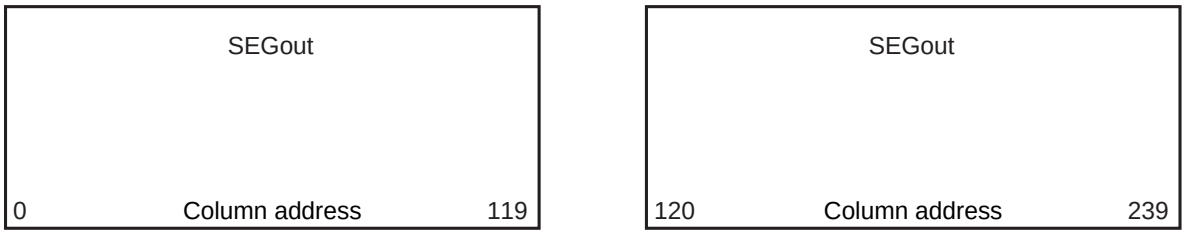
The built-in RAM has a space for 168 lines, that is, for 168 pages.

Also in read operation, the column address is automatically incremented by one when reaching the page specified as the end page, and the page address returns to the start page.

Column Address Control Circuit

This circuit performs address control in the column direction when the display data RAM is accessed from the MPU. The Column Address Set command can be used to specify the column area (the start and end columns). If the Scan Direction Select command is used to specify scanning in the column direction, the page address is incremented by one as the address is incremented from the start column to the end column, and the column address returns to the start column. Also in read operation, the page address is automatically incremented by one when reaching the column specified as the end column, and the column address returns to the start column.

When two IC's are used, the displayable area accommodates 240 (RGB) pixels and the column addresses amount to 240. The column addresses are laid out seamlessly across the two chips as shown below, eliminating the need for recognition of the chip joint.



LPOS=HIGH LPOS=LOW

(P11:0)

I/O Buffer

This is a bidirectional I/O buffer used when the MPU accesses the display data RAM via the internal bus of the S1D15910 series.

Display Data RAM

This is a RAM to store dot data for display, consisting of $3 \times 360 \times 168$ bits. It can be selected by specifying the page and column addresses.

As display data D0 through D7 from the MPU are associated with one RGB pixel, there are not such significant restrictions involved in data transfer for display, which easily achieves display structure with a high level of flexibility. The RAM of the S1D15910 series is divided into blocks by every four lines, and the display system is processed by block.

Read/Write from the MPU side to the display data RAM is controlled via the I/O buffer circuit while Read from the display data RAM for driving LCD is controlled by a separate circuit.

Thus, display data can be overwritten without any regard to the display timing.

See the memory map on page 13 for the structure of the RAM.

Area Scroll Display

Commands can be used to set the area scroll field (start block, end block and specified block) to display the screen by scrolling it within a limited area.

See the description on the scrolling methods on page 14.

Partial Display

Commands can be used to set a partial area (start and end blocks) to obtain partial view of the screen (by line division). With this feature, power consumption can be controlled at a low level, compared to full-screen display, as reading of the display data RAM and the boosting operation of the power IC which is externally connected are terminated during the non-display period, which is best suited for the waiting mode of a mobile device.

Gradation Display

Based on gradation data written in the display data RAM, gradations can be represented by controlling the FRC.

Normally black LC (for inverted display)

Correlation Chart for Gradation Level and Display Color

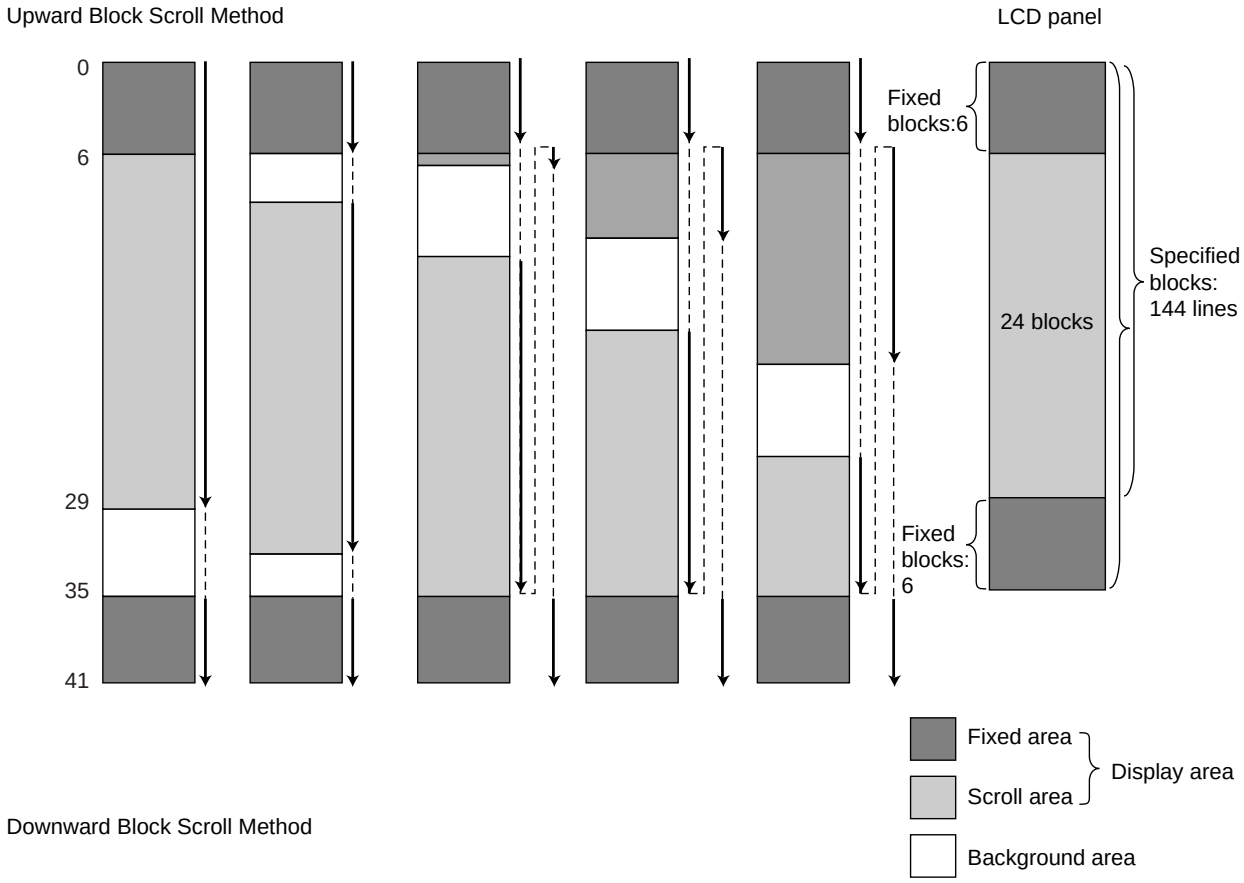
	Black							Red
R(D7,D6,D5)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)
	Black							Green
G(D4,D3,D2)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)
	Black							Blue
E(D1,D0)	(0,0)	(0,1)	(0,1)	(0,1)	(1,0)	(1,0)	(1,0)	(1,1)
		Select one by using a command.			Select one by using a command.			

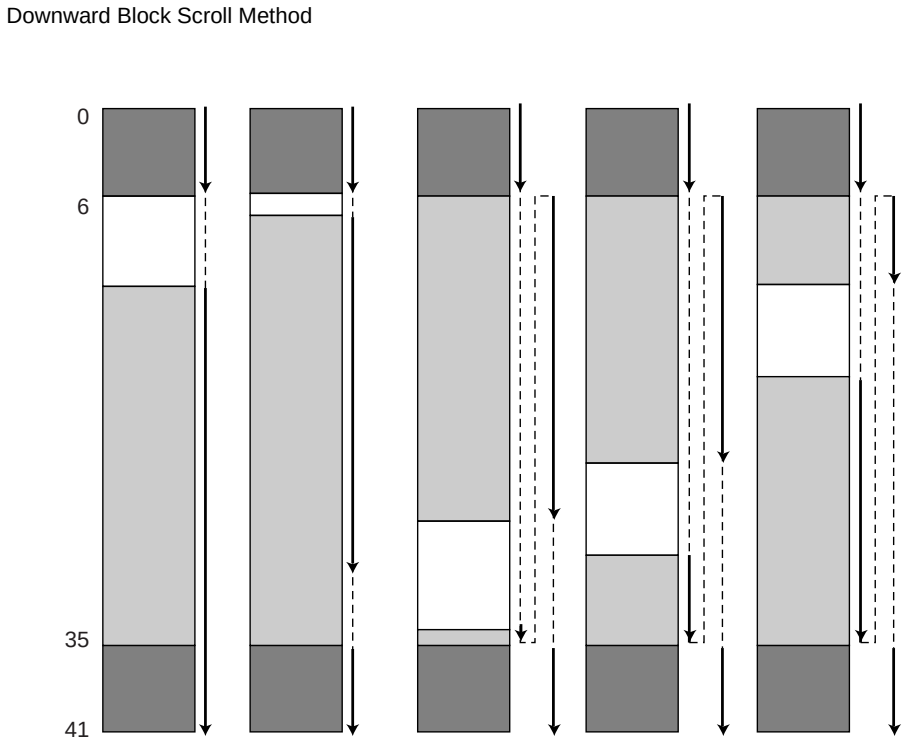
Memory Map Chart

RGB alignment(Command of data control paraametrr2=000)														
			Column											
LCD read direction	LPOS=HIGH P11.0		0			1						119		
	LPOS=LOW P11.0		120			121						239		
	LPOS=HIGH P11.0		239			238						120		
	LPOS=LOW P11.0		119			118						0		
	Color		R	G	B	R	G	B				R	G	B
	Data / Page		D7 D6 D5	D4 D3 D2	D* D* D*	D7 D6 D5	D4 D3 D2	D* D* D*				D7 D6 D5	D4 D3 D2	D* D* D*
Block														
0	0	167												
	1	166												
	2	165												
	3	164												
1	4	163												
	5	162												
	6	161												
	7	160												
2	8	159												
	9	158												
40	160	7												
	161	6												
	162	5												
	163	4												
41	164	3												
	165	2												
	166	1												
	167	0												
SEGout			1	2	3	4	5	6				358	359	360

D* represents data after converting 2-bit data into 3-bit data. Locations of R and G can be altered using the DATCTL command.

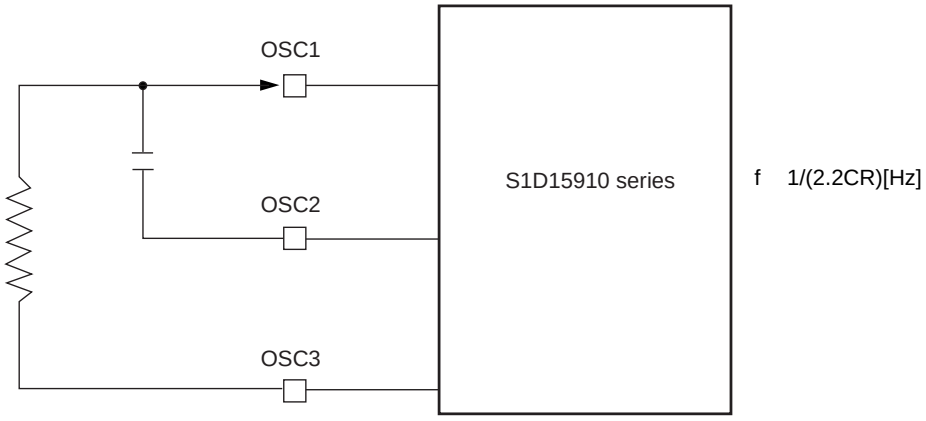
When performing area scrolling at 1/144 duty for lines 25 through 120 (24 blocks) with the background memory in operation, the upper fixed area includes 24/4 = 6 blocks and the lower fixed area includes (144 - 120)/4 = 6 blocks. The scroll area is the area is obtained by subtracting the upper and lower fixed areas (12 blocks) from the total 42 blocks, that is, 30 blocks, and 6 blocks can be used as the background. The specified blocks include 29 blocks (144/4 - 6 lower fixed blocks - 1).





Oscillator Circuit

This is a circuit to generate synchronizing signals for driving LCD. When using the internal oscillation circuit of the S1D15910 series, insert a capacitor between the OSC1 and the OSC2 and a resistor between the OSC1 and the OSC3 as shown below. The values of the "C" and "R" are to be determined on the basis of the oscillation frequency designated below.



When inputting external clock rather than using the internal oscillation circuit, input the external clock through the OSC1. Leave the connections of the OSC2 and OSC3 open.When using twin chips, input external clock signals through the OSC1 of the 2 chips.

	OSC1	OSC2	OSC3
When using the internal oscillation circuit	Refer to the schematic diagram indicated above.		
To input external signals	Input pin	Open	Open

Decoder

Outputs segment driver control signals required for driving LCD. These control signals are determined by display data, driving pattern signals F1/F2 and the LCD AC signal FR.

LCD Driver Circuit

Outputs the LCD driving voltage. For the driving voltage, one of the potential values, V_2, V_1, V_C, MV_1 and MV_2, is output from the driver output.

Internal Timing Generator Circuit

The internal timing generator circuit controls internal Write operation when the display data RAM is accesses by the MPU. It also controls incrementing operation of the column address counter and the page address counter.

Display Control Circuit

The display control circuit generates timing signals SYNC, CL, CA and FR as well as driving pattern signals F1 and F2, referring to the oscillation outputs from the oscillator circuit or external clocks input into OSC1. It also generates the display ON/OFF control signal $\overline{DOFF}$ and the sleep signal $\overline{SLP}$.

8. COMMANDS

Command List

Command Name		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display ON	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Display Invert	A7	None
5	DISCTL	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3bytes
6	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep IN	95	None
7	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep OUT	94	None
8	PASET	0	1	0	0	1	1	1	0	1	0	1	Page Address Set	75	2bytes
9	CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2bytes
10	DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	2bytes
11	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Memory Write	5C	Data
12	RAMRD	0	1	0	0	1	0	1	1	1	0	1	Memory Read	5D	Data
13	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial IN	A8	2bytes
14	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial OUT	A9	None
15	RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read/Modify/Write	E0	None
16	RMWOUT	0	1	0	1	1	1	0	1	1	1	0	End	EE	None
17	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4bytes
18	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1byte
19	VOLCTR	0	1	0	1	1	0	0	0	1	1	0	Volume Control	C6	1byte
20	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None
21	STREAD	0	0	1	Status								Status Read		

Detailed Description of Commands

With the S1D15910 series, interpretation and execution of commands are performed with internal timings alone, without depending on external clocks. With the 80-Series MPU interface, inputting a low pulse in the WR pin activates the command in the Write operation mode. With the 68-Series MPU interface, inputting LOW on the R/W pin activates the Write status, while inputting a high pulse in the E pin activates the command. Therefore, the 68-Series MPU interface differs from the 80-Series MPU interface in that RD (E) in the description of commands and the Command List is replaced with "1" (HIGH) for the Read operation mode. With the serial interface, D/C is used to distinguish data from a command, then the following 8-bit data are used to identify the command. The following describes an example where a command is input with the 80-Series MPU interface.

(1) DISON

Command: 1 Parameter: 0

This command is used for forced control of full-screen display ON. Note that display ON cannot be activated in the sleep mode. Be sure to use this command after resetting the sleep mode.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISON	0	1	0	1	0	1	0	1	1	1	1	Display ON

(2) DISOFF

Command: 1 Parameter: 0

This command is used for forced control of full-screen display OFF. When display is in the OFF mode, set all SEG outputs to the V_C level and DOFF to LOW, and outputs of the common drivers to the V_C level.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF

(3) DISNOR

Command: 1 Parameter: 0

This command is used for normal setting of the lit/unlit display without overwriting the contents of the display data RAM. This is for normal setting for the entire screen and normal setting for partial view is not possible.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display

(4) DISINV

Command: 1 Parameter: 0

This command is used for inverting lit/unlit display without overwriting the contents of the display data RAM. This is for inverting for the entire screen and partial inversion is not possible. The non-display area in the partial view mode is not inverted.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISINV	0	1	0	1	0	1	0	0	1	1	1	Display Invert

(5) DISCTL

Command: 1 Parameter: 3

This command and the accompanying parameters are used for various settings of the display timing.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISCTL	0	1	0	1	1	0	0	1	0	1	0	Display Control
P1	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Test mode, dividing ratio, driving pattern
P2	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Driving duty
P3	1	1	0	*	*	*	*	P33	P32	P31	P30	FR invert setting

* : These are invalid bits that do not affect operations.

Set this command before SLPOUT. Do not switch during display.

P1: Sets the dividing ratio of CL, F1 and F2 driving patterns, test mode and FRC mode, based on which the timing signal for LCD display is generated.

Data	Dividing			
	2 dividings	16 dividings	4 dividings	8 dividings
P13	0	0	1	1
P12	0	1	0	1

The default setting is 2 dividings.

Data	F1/F2 driving pattern switching period			
	8H	4H	16H	Field
P11	0	0	1	1
P10	0	1	0	1

The default setting is 8 H.

Test mode: Used for testing internal features of IC's.

P14 0: Normal operation 1: Test mode (to stop internal F1 and F2 signals)

P15 0: Normal operation 1: Test mode (to stop internal FRC signal)

FRC mode: Alters the pattern delivery method in frame-less modulation.

P16 0: FRC even/odd normal delivery 1: FRC even/odd inverted delivery

P17 0: FRC framed delivery 1: FRC 1H delivery

P2: Sets LCD module duty by block.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Number of displayed lines)/4-1
Example) 1/120 duty	0	0	0	1	1	1	0	1	120/4-1=29
Example) 1/160 duty	0	0	1	0	0	1	1	1	160/4-1=39

P3: Sets the number of inverted lines on the LCD.

Duty	*	*	*	*	P33	P32	P31	P30	(Number of displayed lines)-1
Example) 11 duty	0	0	0	0	1	0	1	0	11-1=10
Example) 13 duty	0	0	0	0	1	1	0	0	13-1=12

The default setting is 11H-inversion.

(6) SLPIN

Command: 1 Parameter: 0

This command causes an LCD module to enter the sleep status. Make sure to input the Display OFF command and turn display off before inputting this Sleep Mode IN command. Also, let the logic power turn off after waiting for the time designated in the specifications for the power IC being used to discharge the electric charge of the power IC, after entering into the sleep status by entry of the sleep IN command. Set SLP to LOW in the sleep status and deactivate the oscillator circuit of the power IC. Also, deactivate the internal oscillator circuit if is has been used.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep IN

(7) SLPOUT

Command: 1 Parameter: 0

This command releases an LCD module from the sleep status. After releasing the sleep status with the Sleep OUT command, wait until the power IC outputs stable voltage. Do so after holding for the time designated in the specifications for the power IC being used.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep OUT

(8) PASET

Command: 1 Parameter: 2

This command and the accompanying two parameters can be used to specify the page address area for accessing the display data RAM from the MPU side. If scanning is set to be performed in the page direction, the column address is incremented by one as the address is incremented from the start page to the end page, and the page address returns to the start page. Make sure to set the start page and the end page as a pair. Make sure that the setting is as follows: start page value < end page value.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Address Set
P1	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start page
P2	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End page

* : These are invalid bits that do not affect operations.

(9) CASET

Command: 1 Parameter: 2

This command and the accompanying parameters can be used to specify the column address area for accessing the display data RAM from the MPU side. If scanning is set to be performed in the column direction, the page address is incremented by one as the address is incremented from the start column to the end column, and the column address returns to the start column. Make sure to set the start column and the end column as a pair. Do not invert the relationship between the settings for the start and the end columns.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set
P1	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start address
P2	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End address

(10) DATCTL

Command: 1 Parameter: 2

This command and the accompanying parameters are used for various settings required when the MPU processes the display data in the built-in RAM.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Control
P1	1	1	0	*	P16	P15	P14	P13	P12	P11	P10	Scan Column Page (B)
P2	1	1	0	*	*	*	*	*	P22	P21	P20	RGB arrangement

P1:

Location of page 0 for the page address

Determines if the location of page 0 relative to the physical location of the display RAM should be inverted or not from the location of page 167.

P10: Location of page 0 for the page address

0: Line 1

1: Line 168

Location of column 0 for the column address

Using two of the S1D15910 series makes it possible to control up to 240 columns. The following section describes the column locations when 2 chips are used. Column locations vary depending on which side the chips are placed, right or left. (The location is determined with the chips placed with their active surface up and the SEG output on the upper side.)

If the chips are placed on the left-hand side (LPOS = HIGH)

P11: 0

The location of column 0 corresponds to SEG1, 2 and 3.

The location of column 119 corresponds to SEG358, 359 and 360.

P11: 1

The location of column 120 corresponds to SEG358, 359 and 360.

The location of column 239 corresponds to SEG1, 2 and 3.

If the chips are placed on the right-hand side (LPOS = LOW)

P11: 0

The location of column 120 corresponds to SEG1, 2 and 3.

The location of column 239 corresponds to SEG358, 359 and 360.

P11: 1

The location of column 0 corresponds to SEG358, 359 and 360.

The location of column 119 corresponds to SEG1, 2 and 3.

Changing the locations of column 0 and page 0 makes it possible to use any desired corner such as the top left corner of the panel as the reference address (address 0) despite the location where IC is connected, top, bottom, right or left section on the panel. The directions for incrementing columns and pages can be selected from leftward, rightward, upward or downward on the panel as desired.

Scanning direction

When the MPU is to access the display memory successively, the direction is determined to be either page or column direction.

P12: Scanning direction 0: Column direction

1: Page direction

Converting blue data

Blue display data are input in 2 bits. You can convert the data into 3-bit data. When the RAM is read, the 2-bit data are restored for output.

BB: 01			
P14, P13	00	01	10
Data after conversion	001	010	011

BB: 10			
P16, P15	00	01	10
Data after conversion	100	101	110

Data after conversion when BB = 00 is fixed to 000 while data after conversion when BB = 11 is fixed to 111. Data after conversion is 000 when P14 and P13 are set to 11 and P16 and P15 to 11.

P2: RGB arrangement

The arrangement of RGB for segment output can be changed according to the RGB arrangement on the LCD panel. This changes the location where data are written in the memory.

P22,P21,P20	line	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	• • •	SEG 360
000	1 2	R R	G G	B B	R R	G G	B B	R R	G G	• • • • • •	B B
001	1 2	B B	G G	R R	B B	G G	R R	B B	G G	• • • • • •	R R
010	1 2	R R	G G	B B	B B	G G	R R	R R	G G	• • • • • •	R R
011	1 2	B B	G G	R R	R R	G G	B B	B B	G G	• • • • • •	B B
100	1 2	R B	G G	B R	R B	G G	B R	R B	G G	• • • • • •	B R
101	1 2	B R	G G	R B	B R	G G	R B	B R	G G	• • • • • •	R B
110	1 2	R B	G G	B R	B R	G G	R B	R B	G G	• • • • • •	R B
111	1 2	B R	G G	R B	R B	G G	B R	B R	G G	• • • • • •	B R

The default setting is 000. (When LPOS = HIGH, P10 = “0” and P11 = “0” , the SEG360 series is a chip to be placed on the right-hand side and LPOS = LOW)

(11) RAMWR

Command: 1 Parameter: Number of data written

When the MPU writes data in the display memory, this command is used to set the data entry status. Inputting this command always sets the page and the column addresses to be set to the start addresses. Writing data following this command overwrites the contents of the display data RAM as well as incrementing the page or column address. Inputting another command (excluding NOP and STREAD) automatically releases the data entry status.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Memory Write
Data written	1	1	0	Data written								Data Write

(12) RAMRD

Command: 1 Parameter: Number of data read

When the MPU reads data from the display memory, this command is used to set the data read status. Inputting this command always sets the page and the column addresses to be set to the start addresses. Reading data following this command causes the contents of the display data RAM as well as incrementing the page or column address. Inputting another command (excluding NOP and STREAD) automatically releases the data read status.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Memory Read
Data read	1	0	1	Data read								Data Read

(13) PTLIN

Command: 1 Parameter: 2

This command and the following two parameters set the partial area. This command is used to obtain a partial view of the screen (line division) for the purpose of controlling power consumption. The smallest unit for LCD display is 4 lines. Accordingly, the numbers of lines in the display and non-display areas are multiples of 4. When lines 1 through 4 are specified as block 0 and lines 5 through 8 block 1, the entire screen consists of blocks 0 through 41. You can specify the range to be displayed by specifying blocks among those.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PTLSET	0	1	0	1	0	1	0	1	0	0	0	Partial Set
P1	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block
P2	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block
Example) BIGIN	1	1	0	0	0	0	0	0	0	0	0	Block 0
Example) END	1	1	0	0	0	0	0	1	0	0	1	Block 9

* : These are invalid bits that do not affect operations.

Block addresses that can be specified for partial view must be selected from the displayed addresses. (Do not specify any of the non-display addresses in the scrolling mode.)

The S1D15910 series enters the following status in the non-display area in the partial display mode.

$\overline{DOFF}$ output: LOW (Fixes the common driver output to V_C.)

Terminates PCL output and stop boosting operation of the power IC.

Sets all SEG pins to V_1 or MV_1.

The FR status of the line displayed last determines to which SEG output is set, V_1 or MV_1. V_1 is output when FR = HIGH. MV_1 is output when FR = LOW. For FR, the phase is inverted each time a frame is started.

(14) PTOUT

Command: 1 Parameter: 0

With this command, the partial display status is exited.

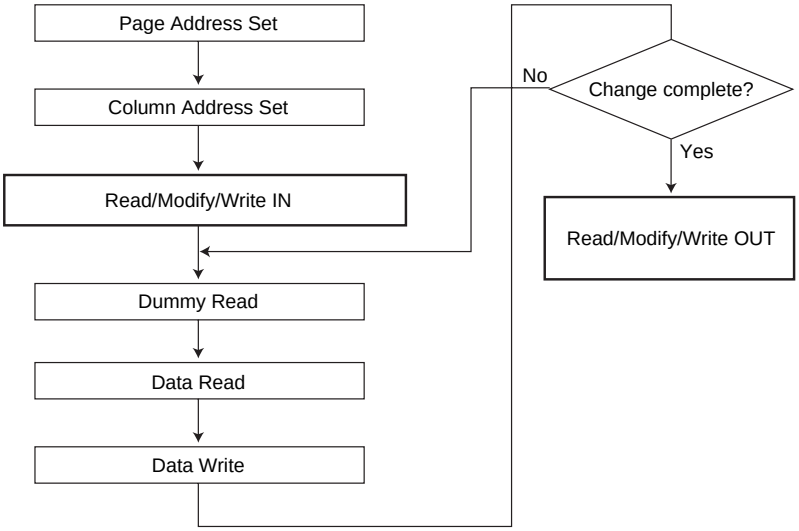
Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial clear

(15) RMWIN

Command: 1 Parameter: 0

This command is used together with the Column Address Set command, Page Address Set command and Read/Modify/Write OUT command. This feature is used to repeatedly modify data in a certain display area such as that specified by the blinking cursor. Set the specific display area with the Column and Page Address commands. Then input this command to set the column and page addresses to the start addresses of the specified area. The Display Data Read command can no longer modify the column (page) address and the address is incremented only with the Display Data Write command. This status is reset with the Read/Modify/Write OUT command or some other command (excluding NOP and STREAD) is input.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read/Modify/Write



(16) RWOUT

Command: 1 Parameter: 0

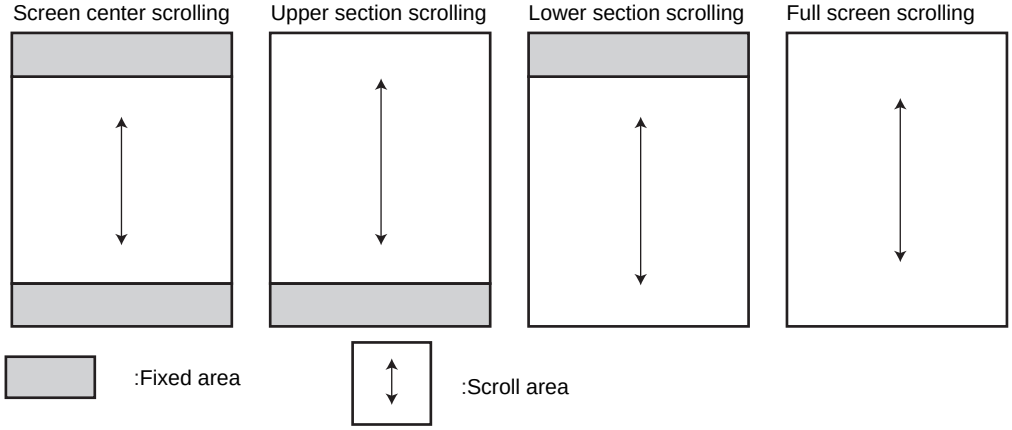
Inputting the Read/Modify/Write OUT command resets the read/modify/write mode.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW OUT

(17) ASCSET

Command: 1 Parameter: 4

This command is used for inputting settings for partially scrolling the screen (by line division). This command and the following four parameters are used to the type of area scrolling, presence or absence of background RAM, area scrolling range and data required for area scrolling. The area scrolling type can be selected from the four patterns below:



The smallest unit for LCD display is 4 lines. Accordingly, the numbers of lines in the display and non-display areas are multiples of 4. Specify the scroll area and the number of specified blocks by block on the RAM. Do not invert the relationship of magnitudes between values of the start and end blocks. *: Invalid bit.

*: Invalid bit.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set
P1	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block
P2	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block
P3	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Number of specitied blocks
P4	1	1	0	*	*	*	*	*	*	P41	P40	Scroll Mode Set

P1: Sets the start block for area scrolling.
Always specify block 0 for the upper section and full-screen scrolling modes.
This is also used as the scroll start block until it is set with the Scroll Start Block Set command.
P2: Sets the end block for area scrolling.
Input (42 = the total number of blocks in RAM - the number of lower fixed blocks - 1).
In the lower section scrolling and full-screen scrolling modes, set 41 if the background RAM is present.
P3: Sets the number of specified blocks.
Input (the number of display duty blocks - the number of lower fixed blocks - 1).
In the lower section scrolling and full-screen scrolling modes, set the same value as for P2.
P4: Input the type of area scrolling.

Data	Screen center scrolling	Upper section scrolling	Lower section scrolling	Full-screen scrolling
P41	0	0	1	1
P40	0	1	0	1

[Example Area Scrolling Setting]
For scrolling the area from line 25 through line 120 on the 1/144 duty screen in the screen center scrolling mode:
P1: Start block is (25 -1)/4 = 6.
P2: The lower fixed area is (144 - 120)/4 = 6 and the end block is 42 - 6-1 = 35.
P3: The number of specified blocks is 144/4 - 6 - 1 = 29.

Example) Screen center scrolling	1	1	0	0	0	0	0	0	0	0	0	Screen center scrolling
Example) BIGIN	1	1	0	0	0	0	0	0	1	1	0	Block 6
Example) END	1	1	0	0	0	1	0	0	0	1	1	Block 35
Example) Block 43	1	1	0	0	0	0	1	1	1	0	1	Block 29

The parameters above assign the upper and lower fixed areas to the upper and lower ends of the RAM. For the display RAM area for area scrolling, the area scrolling display area plus the background area are assigned. Writing data in the background area beforehand facilitates smooth scrolling. For the background, an area containing 2 blocks (8 pages) in the full-screen display at 1/144 duty can be secured. See the description on the scrolling methods on page 14.
[When the background area is not used]
Set the end block as described below.
1) For the upper section and screen center scrolling modes:
Display lines/4 - lower fixed blocks - 1
2) For the lower section and full-screen scrolling modes:
Number of display lines - 1
According to the above example, the end block is 144/4 - 6 - 1 = 29.

(18) SCSTART

Command: 1 Parameter: 1

This command and the accompanying parameter are used to set the first block for scrolling in the scroll area. Do not set a block outside the scroll area. Execute this command after executing the Area Scroll Set command. Scrolling is enabled upon setting the start block for display.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Start Block Set
P1	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block
Example) Block 12	1	1	0	0	0	0	0	1	1	0	0	Block 12

* : These are invalid bits that do not affect operations.

(19) VOLCTR

Command: 1 Parameter: 2

This command is used to set the clock number to control the electronic volume of the external LCD power source and to specify Up/Down. S1D15910 outputs the specified values from the V_{CLK} and $V_{U/D}$ outputs immediately after this command is input.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
VOLCNT	0	1	0	1	1	0	0	0	1	1	0	Power supply control
P1	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Number of volume level steps, U/D

P14 - P10: Input number of stepping volume levels of electronic volume. As the electronic volume of the external power supply has 32 levels, you can specify the level within the stepping range between 0 and 32.

P15: Specifies to step up or down the electronic volume from the current level.

P15 1: UP

P15 0: DOWN

For example, if the number of steps for P14 through P10 is set to 3 and 1 for P15, S1D15910 sets the $V_{U/D}$ output to level “H” and causes 3 clocks to be generated from the V_{CLK} output. Clocks from V_{CLK} are output in the same clock cycle as those from the CL output. If P14 through P10 are set to 0, no clock is output.

The power IC is provided with the limiter feature, which fixes the number of clocks to 31 if a number of clocks beyond the set range or to 0 or a negative number is input as the number of clocks.

To input this command successively, provide a cycle interval of (3 + number of steps) x YSCL between instances of inputting the command.

(20) NOP (Non-operating)

Command: 1 Parameter: 0

This command does not affect operations.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP

(21) STREAD

This read operation enables monitoring of the internal operations of S1D15910. Dummy read is not required for the status read mode. However, when setting the LPOS:LOW master chip, status read is enabled by entering RAMRD command and executing the dummy read after canceling the reset.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
STREAD	0	0	1	O	O	O	O	O	O	O	O	Status Read

D7: Area scroll mode	P41 (see ASCSET)	
D6: Area scroll mode	P40 (see ASCSET)	
D5: Read/Modify/Write	0: OUT	1: IN
D4: Scanning direction	0: Page	1: Column
D3: Display ON/OFF	0: OFF	1: ON
D2: Sleep IN/OUT	0: OUT	1: IN
D1: Normal display/display invert	0: Display invert	1: Normal display
D0: Partial display	0: OFF	1: ON

9. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +4.6	V
Oscillator supply voltage	V_{DDOSC}	–0.3 to +4.6	V
Input supply voltage	V_{DDI}	–0.3 to +4.6	V
Supply voltage (2)	V_{DDH}	–0.3 to +8.0	V
Supply voltage (3)	V_2, V_1, V_C, MV_1, MV_2	–0.3 to +V_{DDH}	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.5	V
Output voltage	V_{OUT}	–0.3 to +0.5	V
Operating temperature	Topr	–40 to +85	°C
Storing temperature 1	Tstg1	–65 to +150	°C
Storing temperature 2	Tstg2	–55 to +100	°C

[Note 1] Voltages are all represented in values relative to GND = V_{SSOSC} = 0V.

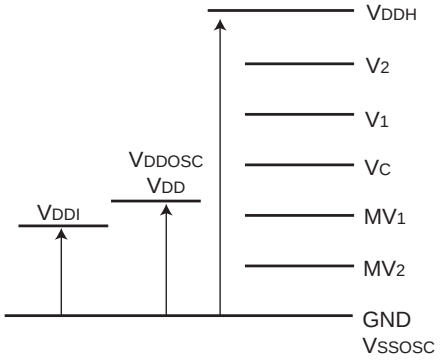
[Note 2] The storing temperature 1 defines the bare chip and the storing temperature 2 defines the populated condition of TCP.

[Note 3] For the relationships between voltage levels at V_2, V_1, V_C, MV_1 and MV_2, maintain the following: $V_{DDH} \geq V_2 > V_1 > V_C > MV_1 > MV_2 \geq GND$

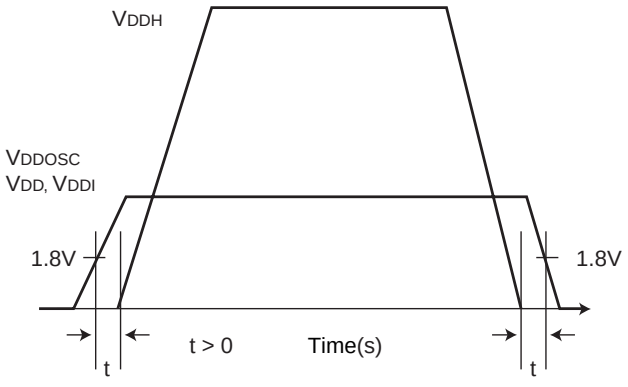
[Note 4] The V_{DD} and V_{DDOSC} and the GND and V_{DDOSC} should be at the same electric potential respectively.

[Note 5] Operating LSI beyond the absolute maximum rating may lead to permanent destruction of LSI. Additionally, it is recommended to maintain the conditions for the electrical characteristics under normal operation. Operating the LSI beyond those characteristics may cause malfunction as well as adverse effect on reliability of the LSI.

Charge Correlation Chart



Power ON/OFF sequence



10. ELECTRICAL CHARACTERISTICS

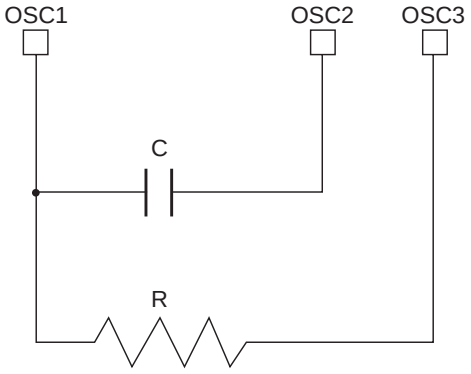
DC Characteristics

Unless otherwise specified, V_{DDH} = V_2 = 6.0 V, V_{DD} = 3.0 V, GND = V_{SSOSC} = MV_2 = 0 V, MV_1 = 1.5 V, V_C = 3.0 V and V_1 = 4.5 V. Ta = 20°C to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Supply voltage (1)	V_{DD}		2.4	2.75	3.6	V	V_{DD}
Oscillator supply voltage	V_{DDOSC}		2.4	2.75	3.6	V	V_{DD}
Input supply voltage	V_{DDI}		1.7	1.8	V_{DD}	V	V_{DDI}
Supply voltage (2)	V_{DDH}		5.4	6.0	7.2	V	V_{DDH}
Supply voltage (3)	V_2		–	–	V_{DDH}	V	V_2
Supply voltage (4)	V_1		–	0.75V_{DDH}	–	V	V_1
Supply voltage (5)	V_C		–	0.50V_{DDH}	–	V	V_C
Supply voltage (6)	MV_1		–	0.25V_{DDH}	–	V	MV_1
Supply voltage (7)	MV_2		GND	–	–	V	MV_2
High level input voltage 1	V_{IHC1}		0.7V_{DDI}	–	V_{DDI}	V	*1
Low level input voltage 1	V_{ILC1}		0.0	–	0.3V_{DDI}	V	*1
High level input voltage 2	V_{IHC2}		0.7V_{DD}	–	V_{DD}	V	*2
Low level input voltage 2	V_{ILC2}		0.0	–	0.3V_{DD}	V	*2
High level output voltage 1	V_{OH1}	I_{OH}=–0.6mA	V_{DDI}–0.4	–	V_{DDI}	V	*3
Low level output voltage 1	V_{OL1}	I_{OL}=+0.6mA	0.0	–	0.4	V	*3
High level output voltage 2	V_{OH2}	I_{OH}=–0.6mA	V_{DD}–0.4	–	V_{DD}	V	*4
Low level output voltage 2	V_{OL2}	I_{OL}=+0.6mA	0.0	–	0.4	V	*4
High level output voltage C2	V_{OHC2}	I_{OH}=–0.02mA	V_{DD}–0.4	–	V_{DD}	V	OSC2
Low level output voltage C2	V_{OLC2}	I_{OL}=+0.02mA	0.0	–	0.4	V	OSC2
High level output voltage C3	V_{OHC3}	I_{OH}=–0.1mA	V_{DD}–0.4	–	V_{DD}	V	OSC3
Low level output voltage C3	V_{OLC3}	I_{OL}=+0.1mA	0.0	–	0.4	V	OSC3
Input leak current 1	I_{LI1}	GND≤V_{IN}≤V_{DDI}	–	–	5.0	µA	*1
Input leak current 2	I_{LI2}	GND≤V_{IN}≤V_{DD}	–	–	5.0	µA	*2
Driver output resistance	RON	ΔV=0.5V	–	0.8	1.4	kΩ	SEG1 to 360
Static power consumption	I_{DDQ}	V_{DD}=V_{DDI},Ta=25°C	–	–	25.0	µA	V_{DD}
Static power consumption	I_{LCDQ}	V_{DDH}=6.0V, Ta=25°C	–	–	25.0	µA	V_{LCD}
Dynamic power consumption	I_{DDOP1}	MPU access *6	–	4.8	33	µA	V_{DDI}
			–	2.0	3.0	µA	V_{DD}
Dynamic power consumption	I_{DDOP2}	MPU no access *7	–	0	25	µA	V_{DDI}
			–	101	170	µA	V_{DD}
Dynamic power consumption	I_{LCDOP}	V_{DDH}=6.0V, Ta=25°C	–	13	45	µA	V_{LCD}
Input pin capacity	CI	Freq.=1MHz	–	–	15	pF	*1,*2
Output pin capacity	CO	Ta=25°C single chip	–	–	15	pF	*3,*4
Oscillating frequency	Fosc	Ta=25°C	–	24	–	kHz	*5

DC Characteristics (supplementary description)

* 1 Input (V_{DDI} connection pin)
  - D[0:7] (I/O input mode)
  - A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, P/S, LPIS
* 2 Input (V_{DD} connection pins)
  - FR, SYNC (I/O input mode)
  - OSC1
* 3 Input (V_{DDI} connection pins)
  - D[0:7] (I/O)
* 4 Output (V_{DD} connection pins)
  - FR, SYNC (I/O output mode)
  - CL, CA, $\overline{DOFF}$, F1, F2, PCL, V_{CLK}, $V_{U/D}$, $\overline{SLP}$
* 5
  - Oscillation circuit using the external “C” and “R”



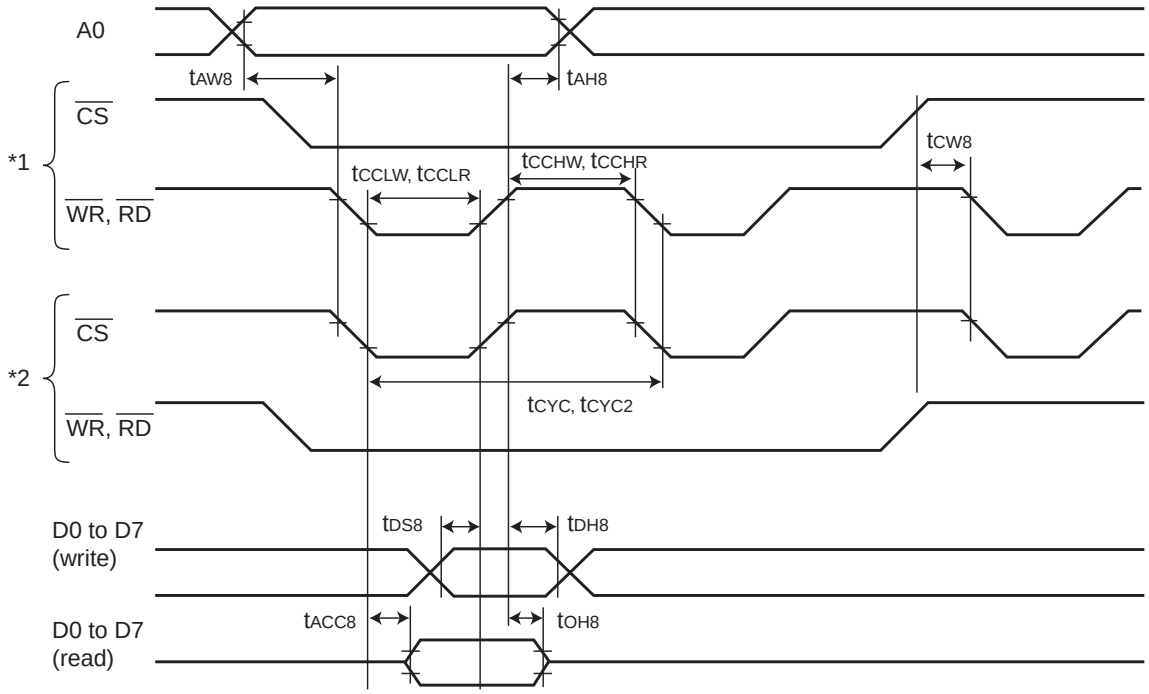
Oscillation frequency f ≒ 1/(2.2 CR)

* 6
  - The conditions, frame frequency = 60 Hz, duty = 1/160. CR oscillation = 19.2 kHz from the external clock is used in two dividings.
  - Access by the MPU is to successively write display data at a cycle time of 1333 ns (750 kHz).
  - The indicated data are of repetitions of AA_H (10101010) and 55_H (01010101).
* 7
  - When using the built-in oscillation circuit, the C-R oscillation should be made using a “C” of 100pF and using a variable “R” to adjust to 25KHz.
  - Frame frequency = 60Hz., Duty = 1/160 and the internally oscillation should be divided by 2.
  - The display data is repetitions of black and white at every 4 lines.

AC Characteristics

System bus

Read/Write characteristics I (80-Series MPU)



*1 is set when $\overline{CS}$ is LOW and access is made with $\overline{WR}$ and $\overline{RD}$.
*2 is used when $\overline{WR}$ and $\overline{RD}$ are LOW and accessed with $\overline{CS}$.

Ta = –40 to 85°C, V_{DD} = 2.6 to 3.6V V_{DDI} = 2.6 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0	t_{AH8}	Address hold time	5	–	ns	
	t_{AW8}	Address setup time	5	–	ns	
$\overline{WR}$, $\overline{RD}$ $\overline{CS}$	t_{CYC}	Write cycle	190	–	ns	
	t_{CYC2}	Read cycle	220	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	150	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	70	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	140	–	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	10	–	ns	
D0 to D7	t_{DS8}	Data setup time	10	–	ns	–
	t_{DH8}	Data hold time	20	–	ns	
	t_{ACC8}	Read access time	–	140	ns	CL=10 to 100pF
	t_{OH8}	Output disable time	5	60	ns	

• Define the rise and fall times (tr and tf) of the input signal as 15 ns or less.
• The reference values for defining all timings are 30% and 70% of V_{DD} – GND.
• t_{CCLW} and t_{CCLR} are defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.
• The timing of A0 is defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.

Ta = –40 to 85°C, V_{DD} = 2.6 to 3.6V V_{DDI} = 1.7 to 2.6V

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0	t_{AH8}	Address hold time	5	–	ns	–
	t_{AW8}	Address setup time	5	–	ns	
$\overline{WR}$, $\overline{RD}$ $\overline{CS}$	t_{CYC}	Write cycle	190	–	ns	–
	t_{CYC2}	Read cycle	250	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	150	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	70	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	170	–	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	10	–	ns	
D0 to D7	t_{DS8}	Data setup time	10	–	ns	–
	t_{DH8}	Data hold time	20	–	ns	
	t_{ACC8}	Read access time	–	170	ns	CL=10 to 100pF
	t_{OH8}	Output disable time	5	60	ns	

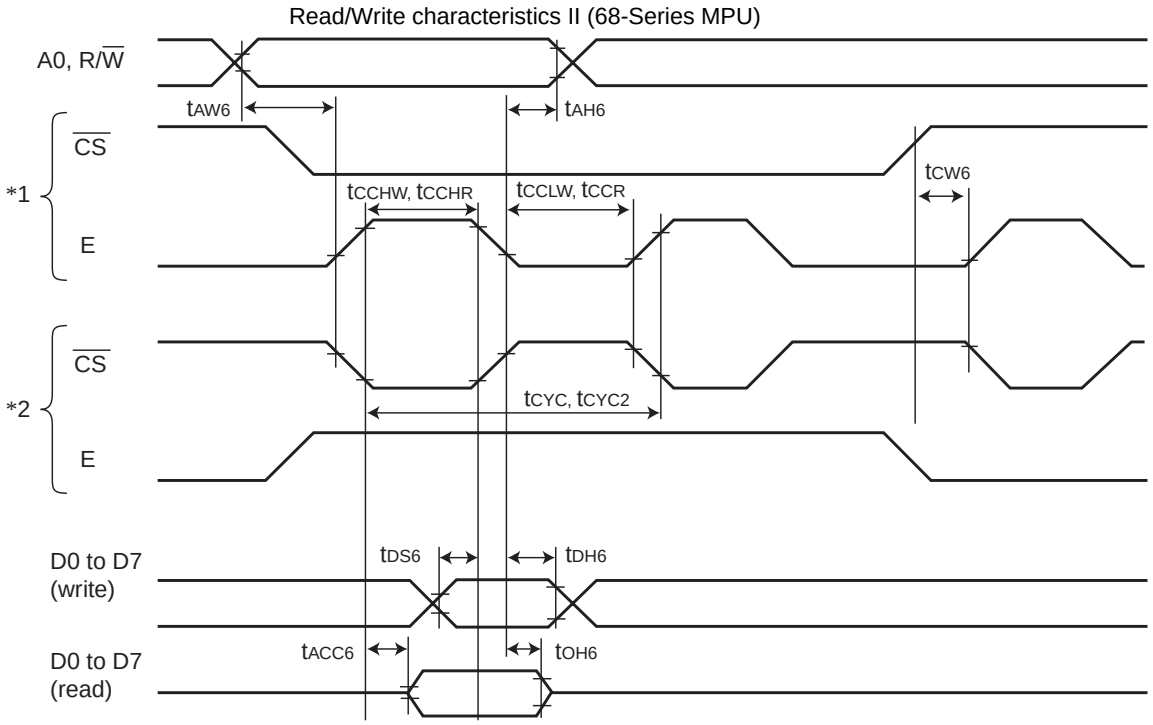
• Define the rise and fall times (tr and tf) of the input signal as 15 ns or less.
• The reference values for defining all timings are 30% and 70% of V_{DD} – GND.
• t_{CCLW} and t_{CCLR} are defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.
• The timing of A0 is defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.

Ta = –40 to 85°C, V_{DD} = 2.4 to 2.6V V_{DDI} = 1.7 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0	t_{AH8}	Address hold time	5	–	ns	–
	t_{AW8}	Address setup time	5	–	ns	
$\overline{WR}$, $\overline{RD}$ $\overline{CS}$	t_{CYC}	Write cycle	210	–	ns	–
	t_{CYC2}	Read cycle	270	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	170	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	80	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	180	–	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	10	–	ns	
D0 to D7	t_{DS8}	Data setup time	10	–	ns	–
	t_{DH8}	Data hold time	20	–	ns	
	t_{ACC8}	Read access time	–	180	ns	CL=10 to 100pF
	t_{OH8}	Output disable time	5	70	ns	

• Define the rise and fall times (tr and tf) of the input signal as 15 ns or less.
• The reference values for defining all timings are 30% and 70% of V_{DD} – GND.
• t_{CCLW} and t_{CCLR} are defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.
• The timing of A0 is defined within the overlap period when $\overline{CS}$ is level LOW and $\overline{WR}$ and $\overline{RD}$ are level LOW as well.

• Read/Write characteristics II (68-Series MPU)



*1 is set when $\overline{CS}$ is LOW and access is made with E.
*2 is used when E is HIGH and access is made with $\overline{CS}$.

Ta = –40 to 85°C, V_{DD} = 2.6 to 3.6V V_{DDI} = 2.6 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0, R/$\overline{W}$	t_{AH6}	Address hold time	5	–	ns	
	t_{AW6}	Address setup time	5	–	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	190	–	ns	
	t_{CYC2}	Read cycle	220	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	150	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	70	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	140	–	ns	
	t_{CW6}	$\overline{CS}$–E time	10	–	ns	
D0 to D7	t_{DS6}	Data setup time	10	–	ns	
	t_{DH6}	Data hold time	20	–	ns	
	t_{ACC6}	Read access time	–	140	ns	CL=10 to 100pF
	t_{OH6}	Output disable time	5	60	ns	

• Define the rise and fall times (tr and tf) of the input signal as 15 ns or less.
• The reference values for defining all timings are 30% and 70% of V_{DD} – GND.
• t_{CCLW} and t_{CCLR} are defined within the overlap period when $\overline{CS}$ is level LOW and E is level HIGH.
• The timing of A0 is defined within the overlap period when $\overline{CS}$ is level LOW and E is level HIGH.

Ta = –40 to 85°C, V_{DD} = 2.6 to 3.6V V_{DDI} = 1.7 to 2.6V

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0, R/$\overline{W}$	t_{AH6}	Address hold time	5	–	ns	–
	t_{AW6}	Address setup time	5	–	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	190	–	ns	–
	t_{CYC2}	Read cycle	250	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	150	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	70	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	170	–	ns	
	t_{CW6}	$\overline{CS}$–E time	10	–	ns	
D0 to D7	t_{DS6}	Data setup time	10	–	ns	–
	t_{DH6}	Data hold time	20	–	ns	
	t_{ACC6}	Read access time	–	170	ns	CL=10 to 100pF
	t_{OH6}	Output disable time	5	60	ns	

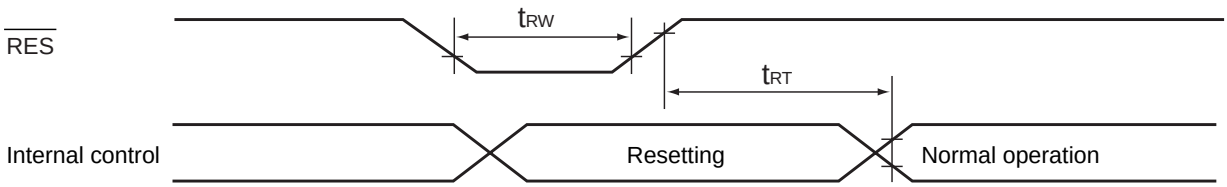
- The rise time and fall time (tr and tf) of input signals should be limited within 15ns.
- All the timings should be set up on the basis of 30% and 70% of the V_{DD}–V_{SS}.
- The "t_{CCHW}" and "t_{CCHR}" should be prescribed by the overlapping period when the $\overline{CS}$ is at the LOW level and when the "E" is at the HIGH level.
- The A0 timing and R/$\overline{W}$ timing should be prescribed by the overlapping period when the $\overline{CS}$ is at the LOW level and when the "E" is at the HIGH level.

Ta = –40 to 85°C, V_{DD} = 2.4 to 2.6V V_{DDI} = 1.7 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
A0, R/$\overline{W}$	t_{AH6}	Address hold time	5	–	ns	–
	t_{AW6}	Address setup time	5	–	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	210	–	ns	–
	t_{CYC2}	Read cycle	270	–	ns	
	t_{CCLW}	LOW width of control pulse ($\overline{WR}$)	170	–	ns	
	t_{CCLR}	LOW width of control pulse ($\overline{RD}$)	80	–	ns	
	t_{CCHW}	HIGH width of control pulse ($\overline{WR}$)	30	–	ns	
	t_{CCHR}	HIGH width of control pulse ($\overline{RD}$)	180	–	ns	
	t_{CW6}	$\overline{CS}$–E time	10	–	ns	
D0 to D7	t_{DS6}	Data setup time	10	–	ns	–
	t_{DH6}	Data hold time	20	–	ns	
	t_{ACC6}	Read access time	–	180	ns	CL=10 to 100pF
	t_{OH6}	Output disable time	5	70	ns	

- The rise time and fall time (tr and tf) of input signals should be limited within 15ns.
- All the timings should be set up on the basis of 30% and 70% of the V_{DD}–V_{SS}.
- The "t_{CCHW}" and "t_{CCHR}" should be prescribed by the overlapping period when the $\overline{CS}$ is at the LOW level and when the "E" is at the HIGH level.
- The A0 timing and R/$\overline{W}$ timing should be prescribed by the overlapping period when the $\overline{CS}$ is at the LOW level and when the "E" is at the HIGH level.

• Reset timing

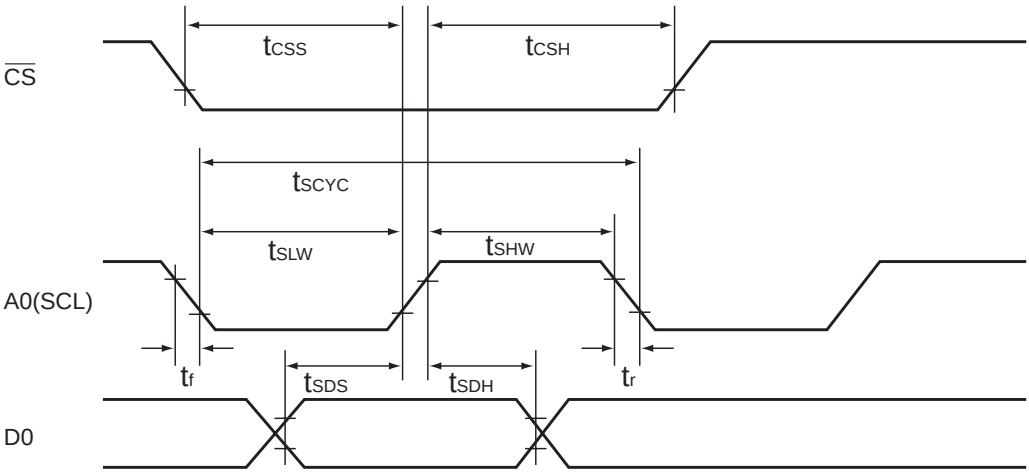


Ta = –40 to 85°C, V_{DD} = 2.4 to 3.6V V_{DDI} = 1.7 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
$\overline{RES}$	t_{RW}	Reset pulse width	100	–	ns	*1
	t_{RT}	Reset release	1000	–	ns	

*1 Define the rise and fall times (tr and tf) of the input signal as 15 ns or less.
The reference values for defining all timings are 30% and 70% of V_{DD} – V_{SS}.

• Serial input characteristics



Ta = –40 to 85°C, V_{DD} = 2.6 to 3.6V V_{DDI} = 1.7 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
$\overline{CS}$	t_{CSS}	$\overline{CS}$ setup time	10	–	ns	*1, *2
	t_{CSH}	$\overline{CS}$ hold time	30	–	ns	
SCL	t_{SCYC}	Clock cycle	150	–	ns	
	t_{SLW}	LOW pulse width	40	–	ns	
	t_{SHW}	HIGH pulse width	40	–	ns	
D0	t_{SDS}	Data setup time	10	–	ns	
	t_{SDH}	Data hold time	10	–	ns	

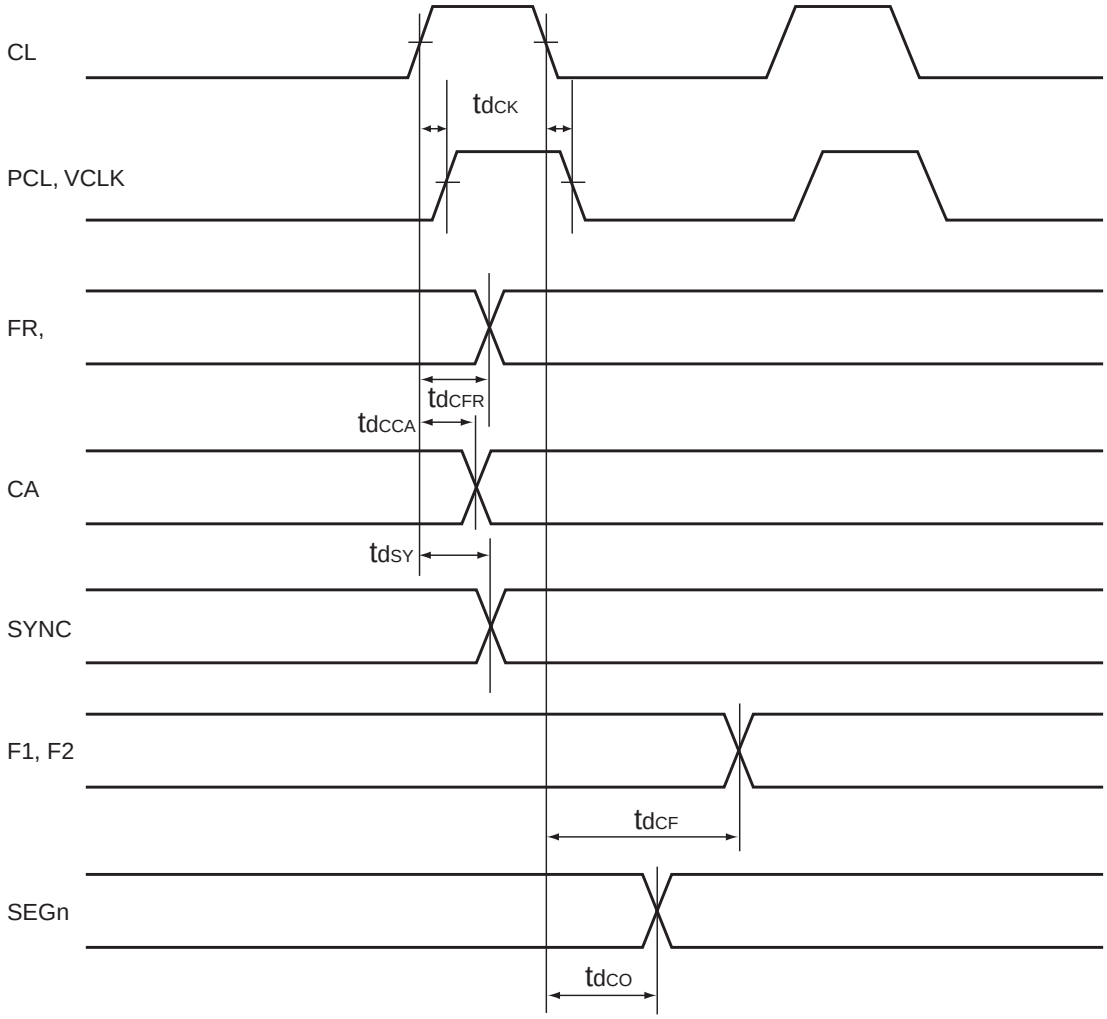
*1 Define the rise and fall times (tr and tf) of the input signal as 10 ns or less.
*2 The reference values of the timings of all input signals are 30% and 70% of V_{DDI}.

Ta = –40 to 85°C, V_{DD} = 2.4 to 2.6V V_{DDI} = 1.7 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and other description
$\overline{CS}$	t_{CSS}	$\overline{CS}$ setup time	10	–	ns	*1, *2
	t_{CSH}	$\overline{CS}$ hold time	40	–	ns	
SCL	t_{SCYC}	Clock cycle	170	–	ns	
	t_{SLW}	LOW pulse width	40	–	ns	
	t_{SHW}	HIGH pulse width	40	–	ns	
D0	t_{SDS}	Data setup time	10	–	ns	
	t_{SDH}	Data hold time	20	–	ns	

*1 Define the rise and fall times (tr and tf) of the input signal as 10 ns or less.
*2 The reference values of the timings of all input signals are 30% and 70% of V_{DDI}.

Output timing characteristics



Ta = –40 to 85°C, V_{DD} = 2.4 to 3.6V V_{DDI} = 1.7 to V_{DD}

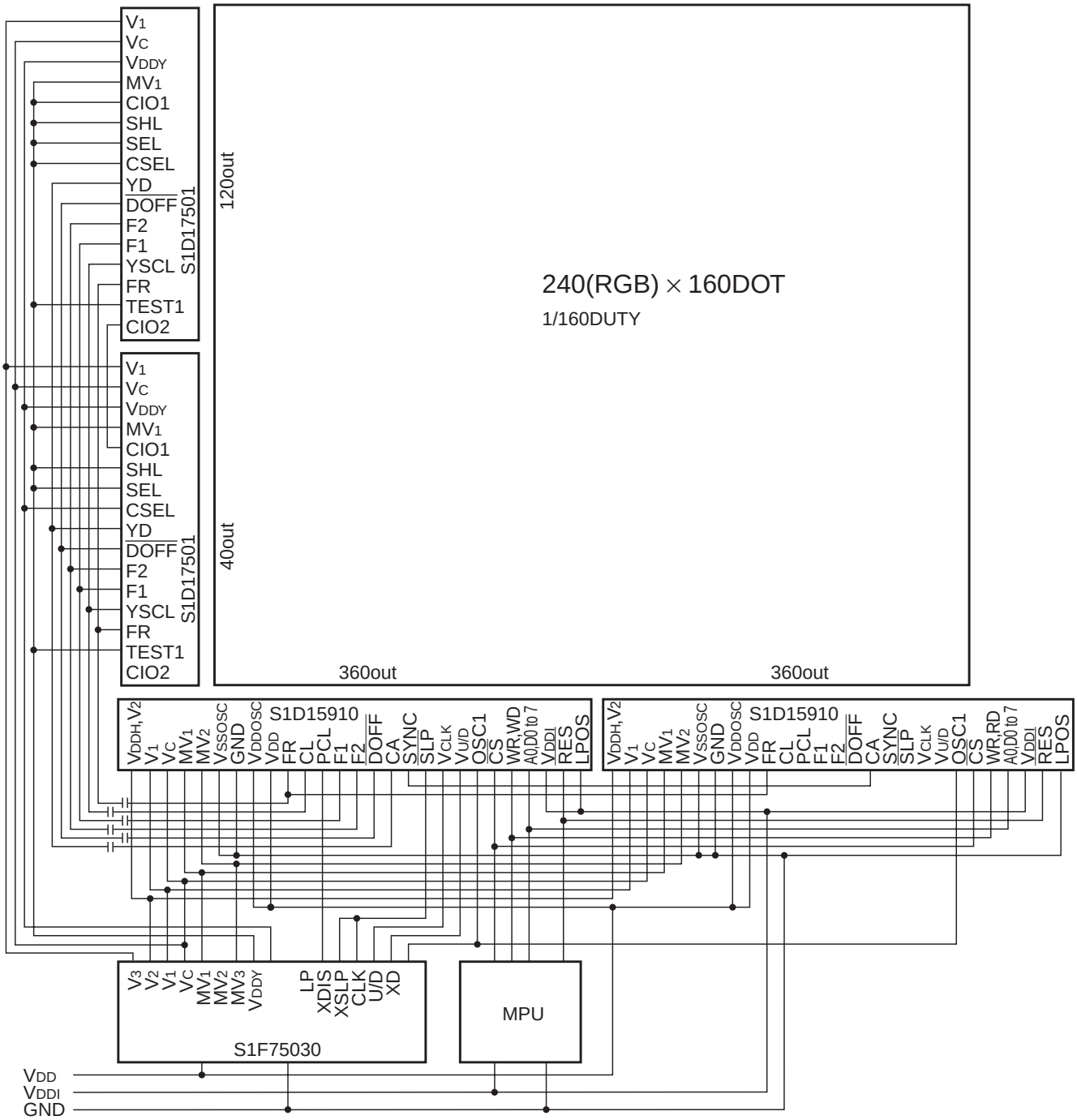
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measuring conditions and other description
PCL,VCLK	t_{dCK}	PCL, VCLK output delay	–	–	1000	ns	CL=100pF
FR	t_{dCFR}	FR output delay	–	–	1000	ns	
CA	t_{dCCA}	CA output delay	–	–	1000	ns	
SYNC	t_{dSY}	SYNC output delay	–	–	1000	ns	
F1,F2	t_{dCF}	F1/F2 output delay	–	–	1000	ns	
SEG n	t_{dCO}	SEG n output delay	–	–	500	ns	

11. APPLICATIONS

Connection examples: Explanations will be made on examples of the LPOS and DATCTL settings for the display, a reference example and practical example of the MPU interface.

Example of Connection

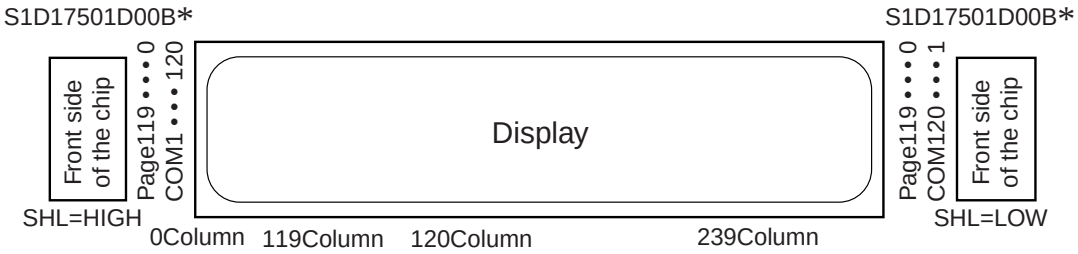
Conditions: 1/160 duty (160-line display)

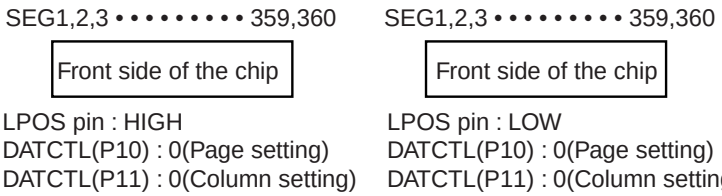


Examples of the LPOS pin and DATCTL (P10 and P11) settings for the display

Conditions: 1/120duty, 240RGB × 120 pixels, setting the upper left corner as the page "0" and the column "0" and using the S1D17501D00B∗ as the Y driver.

① When installing the S1D15910D series on the lower side of the panel showing the active surface up

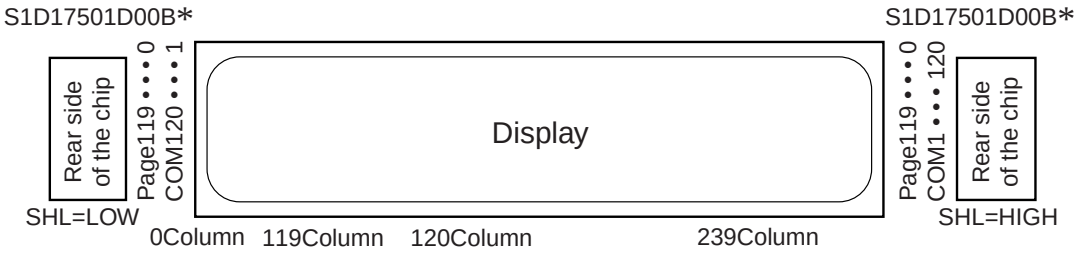


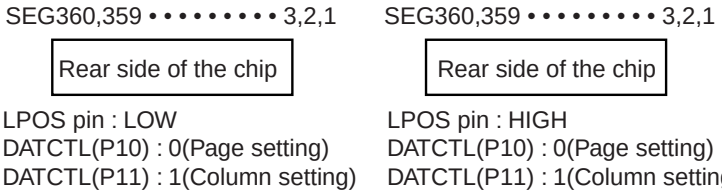


LPOS pin : HIGH
DATCTL(P10) : 0(Page setting)
DATCTL(P11) : 0(Column setting)

LPOS pin : LOW
DATCTL(P10) : 0(Page setting)
DATCTL(P11) : 0(Column setting)

② When installing the S1D15910D series on the lower side of the panel hiding the active surface down

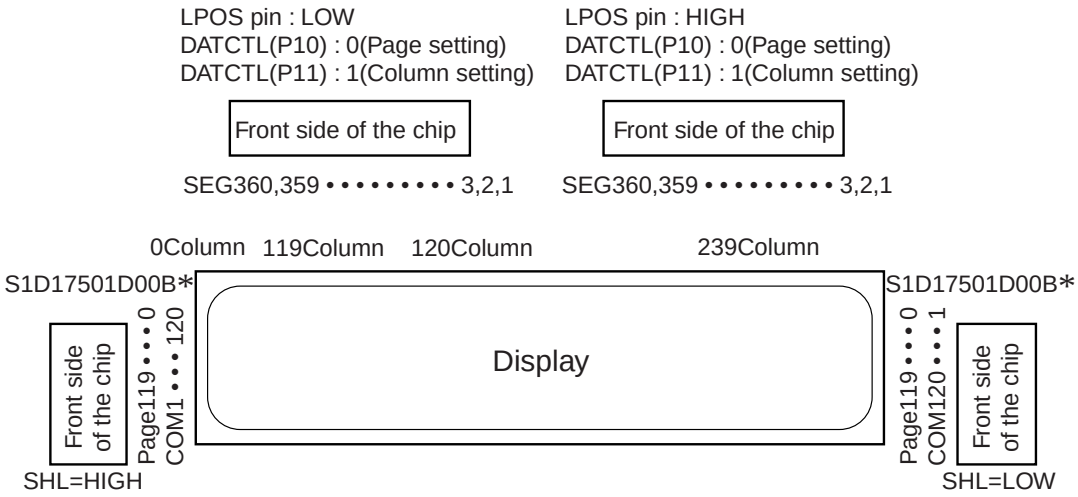




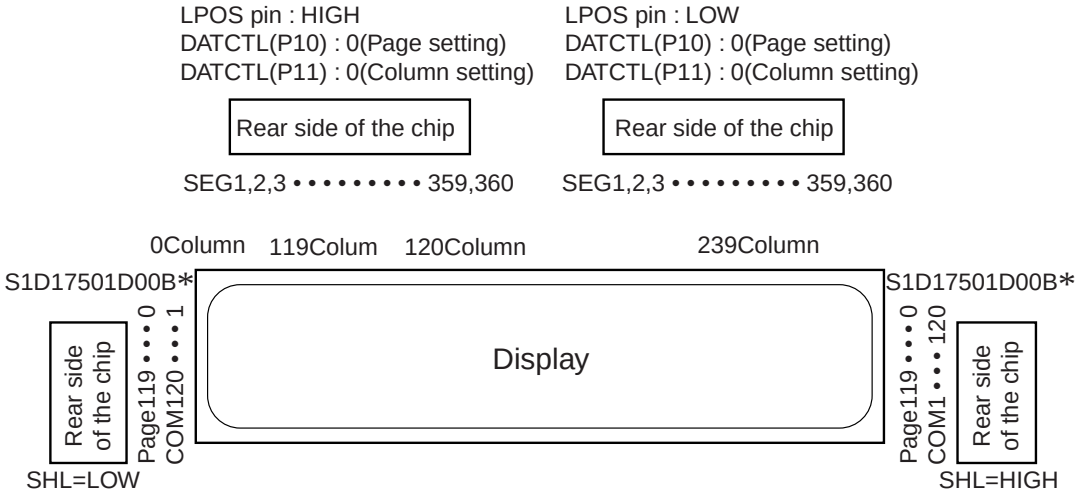
LPOS pin : LOW
DATCTL(P10) : 0(Page setting)
DATCTL(P11) : 1(Column setting)

LPOS pin : HIGH
DATCTL(P10) : 0(Page setting)
DATCTL(P11) : 1(Column setting)

③ When installing the S1D15910D series on the upper side of the panel showing the active surface up



④ When installing the S1D15910D series on the upper side of the panel hiding the active surface down

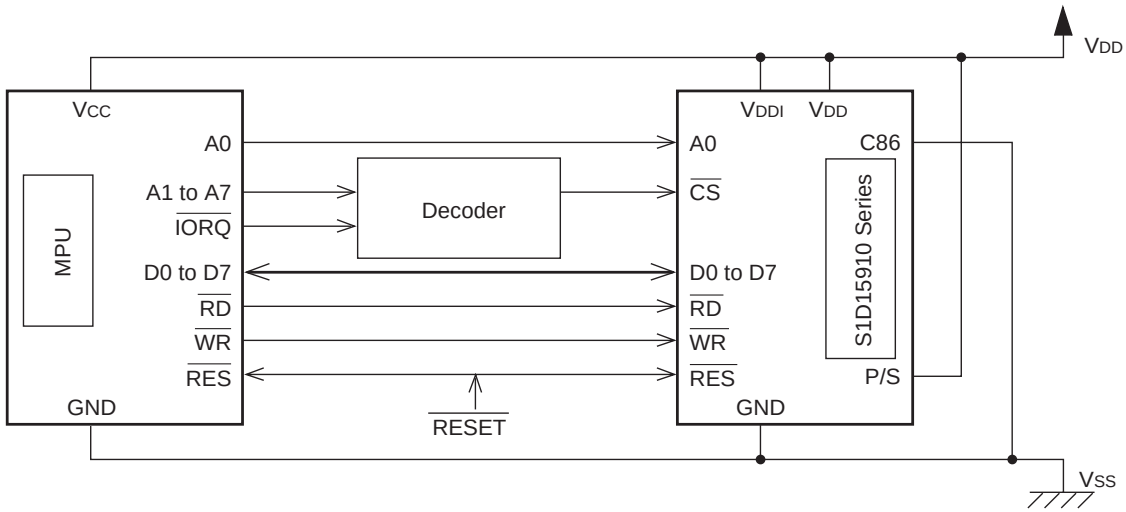


When using 2 chips of the S1D15910D series, the one involving the column “0” is to become the master chip. For signal (CL, CA, etc.) connection between the S1D15910D series and the Y-driver, either the master chip or the slave chip can be used. Make connection to either one of these chips.

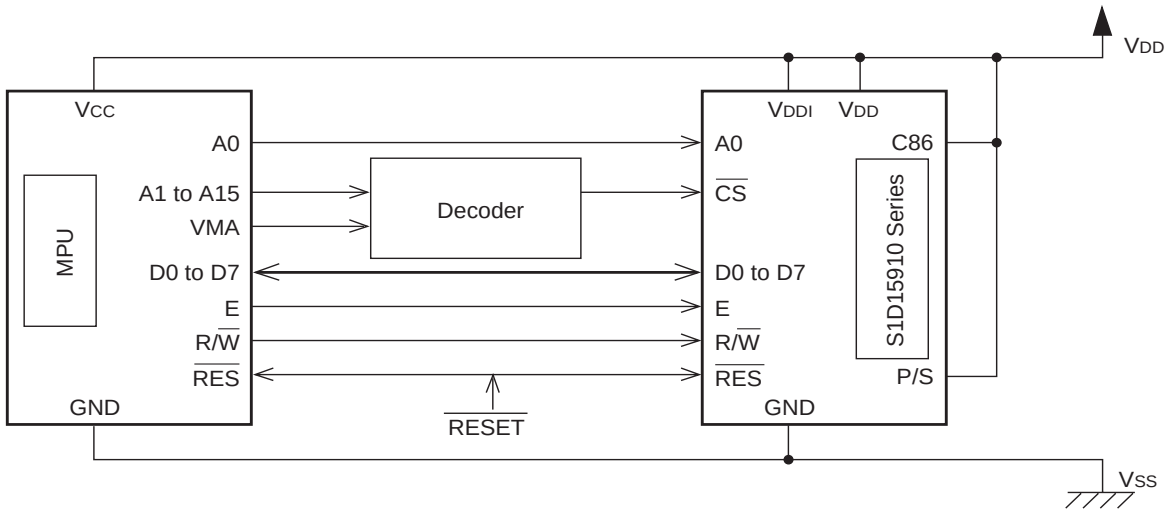
MPU interface (For reference)

The S1D15910D series devices can be directly connected to the 80-type and 68-type MPU's. Furthermore, by use of a serial interface, they can be operated by use of fewer signal lines.

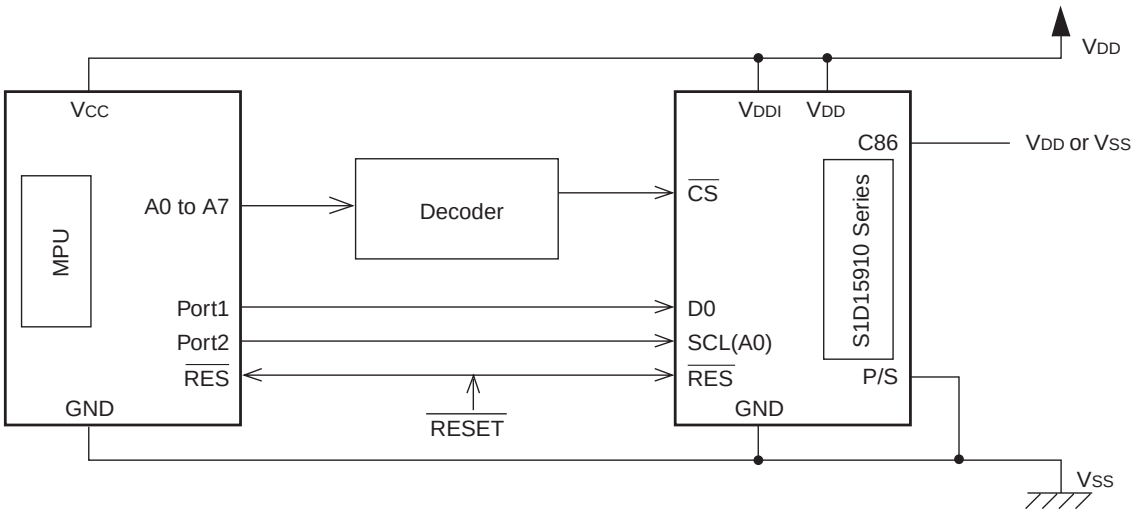
80-type MPU interface



68-type MPU interface



Serial interface



Actual Application Examples

Power start-up

Input system power (V_{DDI}, V_{DD}, V_{DDH}).

↓

Always perform reset operation after turning power on. (RES = LOW)

The following shows the default settings to be restored upon resetting.

Sleep status:	Sleep IN
DISON/DISOFF status:	DISOFF
Normal display/display invert:	Normal display
Driving duty:	1/160 (set to 160 lines)
FR frequency:	11 h-inversion
Page address field:	page 0 (start), page 167 (end)
Column address field:	column 0 (start), column 239 (end)
Location of page 0 address:	line 1
Location of column 0 address:	SEG 0, 1 and 2 pins (when LPOS = HIGH)
Scanning direction:	column direction
F1/F2 driving pattern:	Fluctuates every 8 hours.
V_{CLK}, $V_{U/D}$:	LOW
Two clock dividings:	00h
No partial display provided.	
Area scroll:	full-screen scrolling, with background memory.

Input initial command.

DATCTL: Setting scanning direction and master slaves.

DISCTL: Setting driving duty, FR frequency, F1 and F2 driving patterns.

Caution: When LPOS:L, after resetting, DATCTL becomes P11:0 being in slave condition. Therefore, when switching to the master, it is necessary to set to P11:1 immediately (within 1 ms).

↓

Sleep OUT

↓

Setting the power supply volume control.

↓

Input display data.

Example: To start Write.

Input write data. ← + the number of data desired to be displayed

↓ | Repeat.

↓

Display ON (Let the indication turn on after waiting for the time designated in the specifications for the power IC being used, namely, until the power IC starts outputting stable voltage after sleep OUT.)

↓

Being on display

Rewrite some part of the displayed contents.

↓

Example. Page Address Set

Column Address Set

Write start

Input write data. ← + the number of data desired to be overwritten

| Repeat.

↓

Electronic volume control

↓

etc.

Power OFF

↓

Display OFF

↓

Sleep IN (Let the power fall after waiting for the time designated in the specifications for the power IC being used to discharge the electric charge of the power IC, after the sleep IN.)

↓

Power OFF (V_{DDI}, V_{DD}, V_{DDH})

Cautions:

1) In partial overwriting, do not overwrite the same section repeatedly in one frame (which is 16.6 ms at 60 Hz).

2) Follow the specified sequence for sleep OFF and display ON/OFF. (Refer to the Paragraph (6) SLPIN and Paragraph (7) SLPOUT in the “Explanations of the Commands”.)

12. CAUTIONS

Please be advised on the following points in the use of this development manual.
1. This development manual is subject to change for improvement without prior notice.
2. This development manual does not guarantee or furnish any industrial property right nor its execution.

Any application examples in this manual are intended to ensure your better understanding of the product. Thus, the manufacturer shall not be liable for any trouble with your circuits arising from using such application examples.

In handling the S1D15910 Series, your attention is required to the following points:
[Precautions on Light]
Any semiconductor device is prone to changes in its characteristics when exposed to light, following the general principles inherent in any solar cell. Therefore, exposure to light may lead to mal-function of this IC.
(1) Give considerations to design and mounting layout so that the IC is implemented in a light-shielded structure in its actual application.
(2) Give considerations to design and mounting layout so that light-shielding protection is given to the IC in the test process.
(3) Extend the above considerations for light-shielding protection to the front, rear and side faces of the IC chip.

Precautions for Handling against External Noise
(1) Although the S1D15910 Series retain the operating status and display data achieved with commands, excessive external noise may alter its internal status. Measures should be taken to control noise or to protect the product from the effect of noise in the process of installation and in design of the system.
(2) We recommend that you should configure software so that the operating status is periodically refreshed (resetting of commands and retransfer of display data) in order to cope with unexpected noise.