Prelab 3 : 52%
Prelab 4 : 94%
LabRep 3 : 69%

Jacobs University Bremen

Electronics Laboratory Course
Spring Semester 2019

Lab Experiment: Bipolar Junction Transistor

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Place of execution	: Teaching Lab EE
Date of execution	:

Introduction:

The few main objects of this experiments were:

- To become familiar with bipolar junction transistors (BJTs).
- The output characteristics of a common-emitter based BJT circuits will be obtained.
- The voltage gain (AV), the frequency response, the phase relation between the input voltage and the output voltage of

a common-emitter amplifier circuit will be investigated

A BJT is a three terminal semiconductor device. It is widely used in discrete circuits as well as in integrated circuits. The main applications of BJTs are analog circuits. For example, BJTs are used for amplifiers in particular for high-speed amplifiers. BJTs can be used for digital circuits as well, but most of the digital circuits are nowadays realized by field effect transistors (FETs). There are three operating modes for BJTs, the active mode (amplifying mode), the cut-off mode and the saturation mode. To apply a BJT as an amplifier, the BJT has to operate in the active mode. To apply a BJT as a digital circuit element, the BJT has to operate in the cut-off mode and the saturation mode.

6.1 Prelab BJT

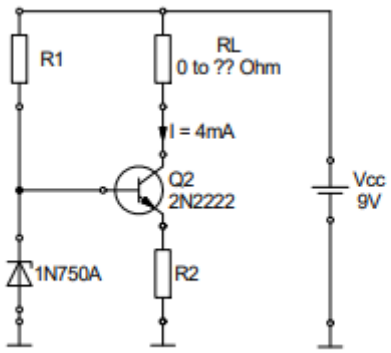
6.1 Problem 1: Biasing of Bipolar Junction Transistors

1) Calculate VB, VE, VCE, and VC.
   Ve=3.84V
   Vb=3.14V
   Vce=0V
   Vc=8.16V
   Calculate IB, IE, and IC.
   Ib=0.9mA
   Ie=8.1mA
   Ic=8.1mA
2)

the values are wrong! Show the calculation!!

6.2.3 Problem 2: Constant Current Source

1) Given is following constant current circuit:



$V_{BE} = 0.7V$

2) Find the values for R1 and R2 to get a constant current of IC ≈ 4mA. Hint: The 1N750A diode is a Zener diode! See data sheet for electrical Properties

   The voltage of the 1N7504 Zener diode in the active mode operates at a voltage V_Z=4.7V. We also know that

$$I_E = I_C + I_B$$
$$I_C = \beta I_B$$
$$I_C = \alpha I_E$$
$$I_C \approx I_E \approx 4mA$$

   From the mesh equation:

$$I_{R1} = IE = \frac{V_Z - V_{BE}}{R_2} \rightarrow R_2 = \frac{V_Z - V_{BE}}{I_E} = \frac{4.7 - 0.7}{4 \times 10^{-3}} = 1000\Omega$$

Iz should be lower!! 10mA are enough!

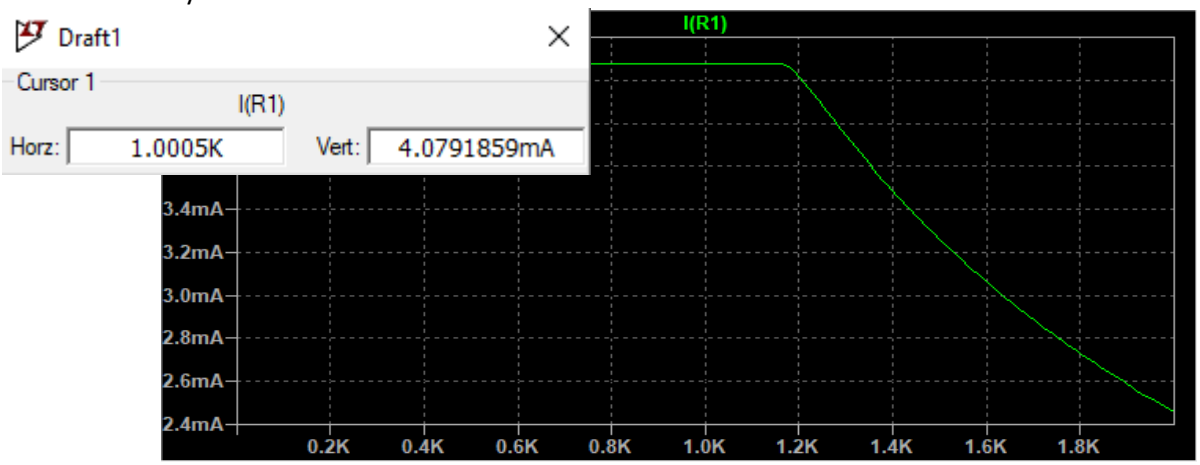
At Vz= 4.7, I_Z = 100 mA:

$$R_1 = \frac{V_{CC} - V_Z}{I_Z + I_B} = \frac{9 - 4.7}{100 \times 10^{-3}} = 43\Omega$$

3) What is the maximum value for RL to still get IC ≈ 4mA?
The max value of R_L is found when we consider having V_{CC} with its largest value and V_{CE} as approximately 0.7V, and we solve accordingly.

$$R_L \times I_C = V_{CC} - V_{CE} - V_E \rightarrow R_L = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{9 - 0.7 - 4}{4 \times 10^{-3}} = 1075\Omega$$

4) Implement the circuit in LTSpice and verify your calculations! Use the .step command to vary RL.



The value for 1000ohm R1 is obviously still something close to 4mA, and after it we see a decrease from the graph.

LTSpice circuit with all commands??

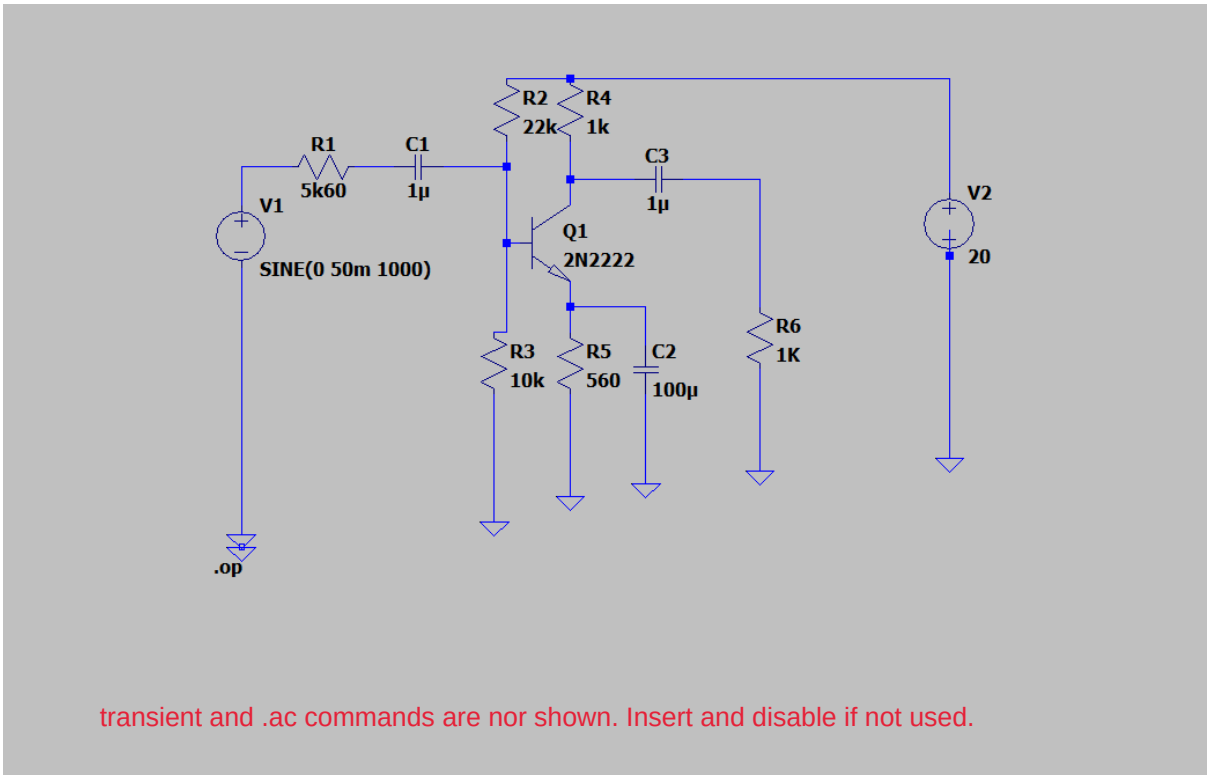
5) Explain the function principle of the circuit!

We have three values that stay constant over the circuit, that being the voltage V_E, current, and I_C is also approximately constant. For the voltage V_E to remain constant we must satisfy the equation $V_B = V_E + V_{BE}$. And if that is constant the current over it is also constant. As for I_C, V_{CE} should also be high enough for the current to remain constant.

The circuit works as a constant current source that goes into the collector is kept the same independent from a range of resistors. This is done with the help of a Zener diode which keeps the voltage at base constant at a value of 4.7V. Also, the current is kept the same. By selecting values of R2 it is easily to change the current value of the emitter which is nearly that of the collector. By this means we also have a way to change the output current just by changing the value of the R2.

5.2.3 Problem 3: Amplifier Circuit

1. Use 'LTSpice IV' to implement the following circuit



2. The DC operation point for the values of Vb, Vc, Vce, Ve, Ic and Ib was found using the following output table from LTSpice.

--- Operating Point ---

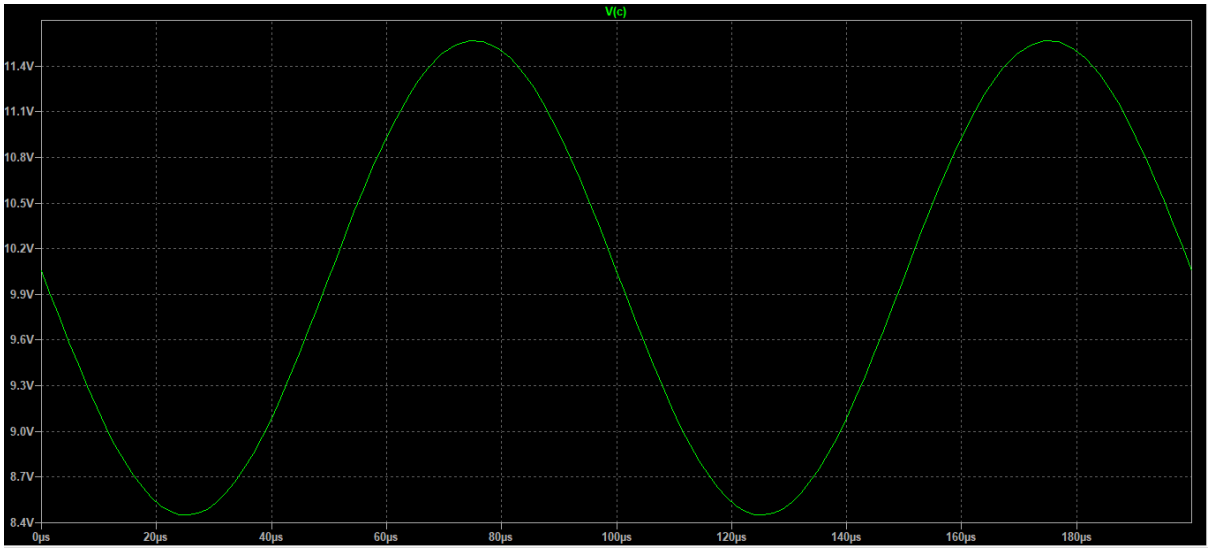
V(n002):	0	voltage
V(n003):	3.32449e-014	voltage
V(n004):	5.93659	voltage
V(n005):	10.7206	voltage
V(n007):	5.22198	voltage
V(n001):	20	voltage
V(n006):	1.07206e-014	voltage
Ic(Q1):	0.00927939	device_current
Ib(Q1):	4.55866e-005	device_current
Ie(Q1):	-0.00932497	device_current
I(C3):	-1.07206e-017	device_current
I(C2):	5.22199e-016	device_current
I(C1):	5.93659e-018	device_current
I(R6):	1.07206e-017	device_current
I(R5):	0.00932497	device_current
I(R4):	0.00927939	device_current
I(R3):	0.000593659	device_current
I(R2):	0.000639246	device_current
I(R1):	5.93659e-018	device_current
I(V2):	-0.00991863	device_current
I(V1):	5.93659e-018	device_current

From above table, we can see that Vc =10.72. The Vc recorded by the LTSpice is the voltage experienced at the collector pin of the transistor. The voltage at base is Vb= 5,9V. If the voltage drop over R4 is needed then we have to compute Vr4=Vcc-Vc=20-10.72 =9.9831V. The voltage drop on the emitter is given at the table an the value is 5.94V. We can now calculate $V_{CE} = V_C - V_E = 10.72 - 5.94 = 4.39$V. The current at the collector is recorded as 0.00998A and the one at the base was $4.9689 * 10^{-5} A$.

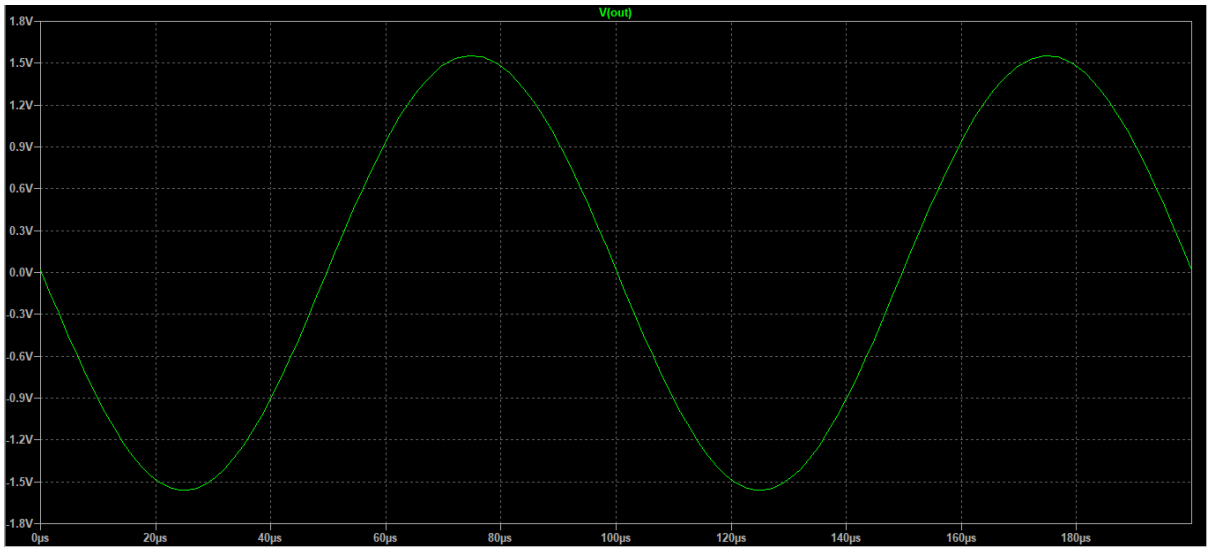
a table would be better!!

3. Perform a transient analysis for about 2 cycles of a sinusoidal input signal. The input signal Vs exhibits a frequency of 10KHz and an amplitude 50mV peak. Display the voltage at the base and across the load resistance RL. Determine the voltage gain VC/VB and VC/VS.

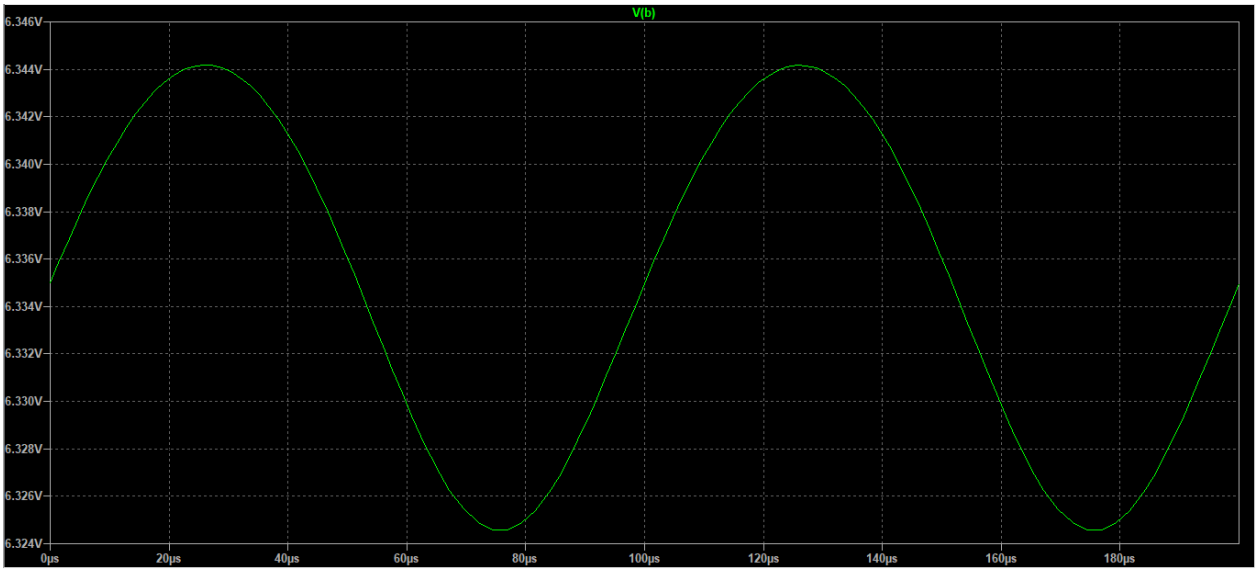
Vc:


V(c)
11.4V
11.1V
10.8V
10.5V
10.2V
9.9V
9.6V
9.3V
9.0V
8.7V
8.4V
0µs
20µs
40µs
60µs
80µs
100µs
120µs
140µs
160µs
180µs

Vrl:


V(out)
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
-0.3V
-0.6V
-0.9V
-1.2V
-1.5V
-1.8V
0µs
20µs
40µs
60µs
80µs
100µs
120µs
140µs
160µs
180µs

Vb:

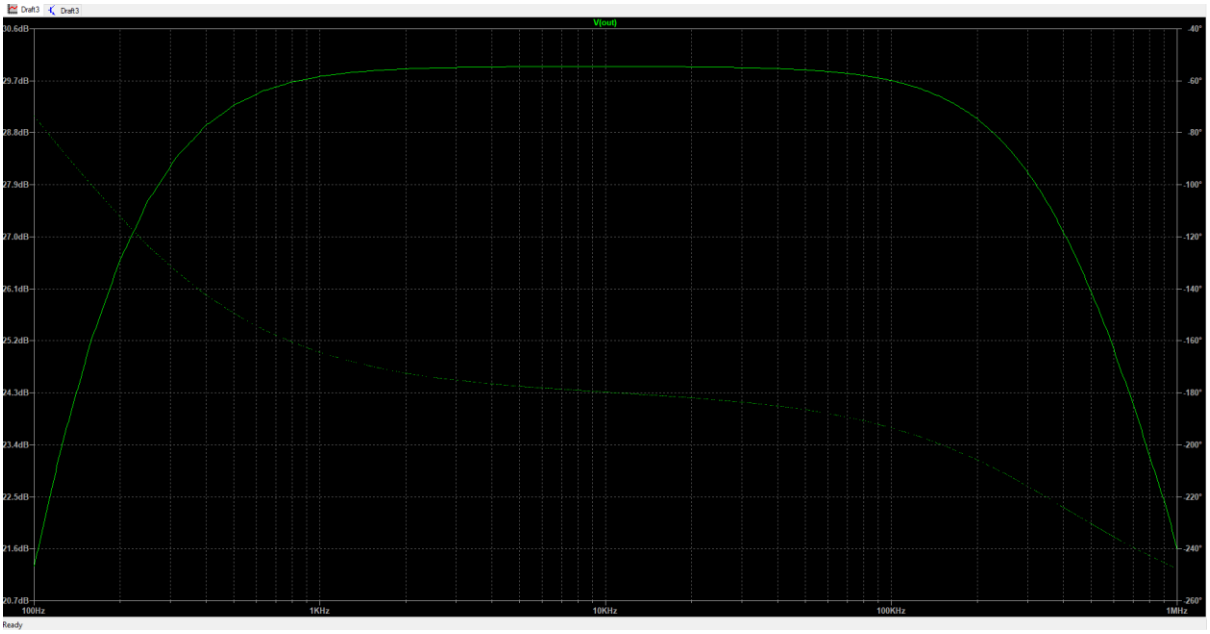


$$G_{CB} = \frac{V_C}{V_B} = \frac{3.116}{0.0197} = 158.17$$

$$G_{CS} = \frac{V_C}{V_S} = \frac{3.116}{0.050} = 62.32$$

Quality ouf output signal??

4. Perform an AC analysis. Keep the amplitude of the input signal constant at 50mV . Vary the frequency from 100Hz to 1MHz with 10 points per decade and display the voltage across the load resistance RL.



5. Use the LTSpice '.MEASURE' command (see help file and example 'MeasureBW.asc') to determine the lower and upper −3dB frequencies and the bandwidth.

The bandwidth was found using the following directives

.measure tmp max mag(V(out))

command in the simulation file?? show it in the circuit

.measure BW trig mag(V(out))=tmp/sqrt(2)rise=1 targ mag(V(out))=tmp/sqrt(2) fall=last

Which yielded

$$f_{lower} = 215.786Hz, f_{upper} = 414.421KHz$$

2

values should be different.. did you really check the error log after simulation??? You can copy paste the result from there..

Bandwidth = Fupper – Flower = 414.421KHz-215.786= 414.205214KHz

Execution & Evaluation

The goal of the experiment is to investigate the reverse/forward and forward/reverse transition behavior of a rectifier and a signal diode.

Workbench No. 11

Instruments and tools used:

- Breadboard
- Function Generator/oscilloscope
- Resistors
- Capacitor
- Wires
- Q22N2222 transistor

5.3.1 Problem 1: Determine Type and Pin Assignment of a Bipolar Transistors

1. First task is to find the base terminal

Multimeter Leads connected to BJT		Diode Check value(reading or .OL)
+ Terminal	Gnd Terminal	-
1	2	.OL

do not split tables

2	1	0.719
1	3	.OL
3	1	.OL
2	3	0.714
3	2	.OL

Over load is between 1 and 3, so pin 2 is base.

2. Second task is to determine the type of the transistor.

The negative or common terminal of the multimeter is connected to the base terminal which we found above, and we get 2 readings after connecting the +terminal to the other two remaining pins. The table below shows our lab results.

Pin the +Terminal is connected to	Value at the multimeter
1	.0L
3	.0L

3. Last task is to determine the emitter and collector terminals

First thing we had to do is to change the + terminal of the multimeter and connect it to the base(pin2) as it is the only way we can see voltage readings from the multimeter if the other two pins are connected with the common terminal of the multimeter each time. The voltages were recorded and are shown below:

Pin the Common terminal is connected to	Value at the multimeter
1	0.715V(emitter)
3	0.704(lower is collecter)

The following table shows the results of this Problem.

Transistor Type	NPN
Base Terminal	Pin 2
Emitter Terminal	Pin 1

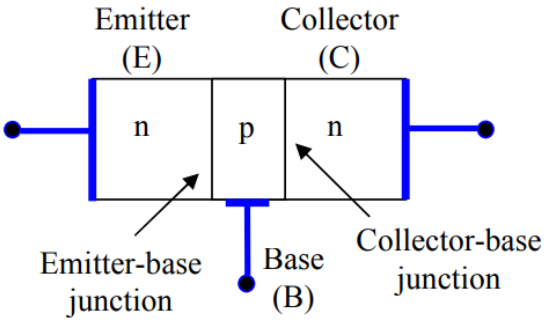
Collector terminal Pin 3

Evaluation:

1. In Problem 5.3.1.(1), explain why the remaining terminal is the base when the other two terminals give overload .0L with both polarities of the multimeter applied?

The transistor consists of two diodes with opposite polarities in series. When the positive polarity is applied to the emitter, it is in reverse bias while the other diode is forward bias. When a negative polarity is applied, the diode is forward biased and the other one would be reverse bias. In both cases, no current passes through terminals which is why multimeter reads OL. When the positive lead of the multimeter is connected to the base and the ground lead to any other terminal, there will be current flow and we will get a voltage reading. In this case, the base-emitter and base-collector diodes would be forward biased.

2. Explain why Problem 5.3.1.(2) can be used to determine whether the transistor is 'NPN' or 'PNP'.

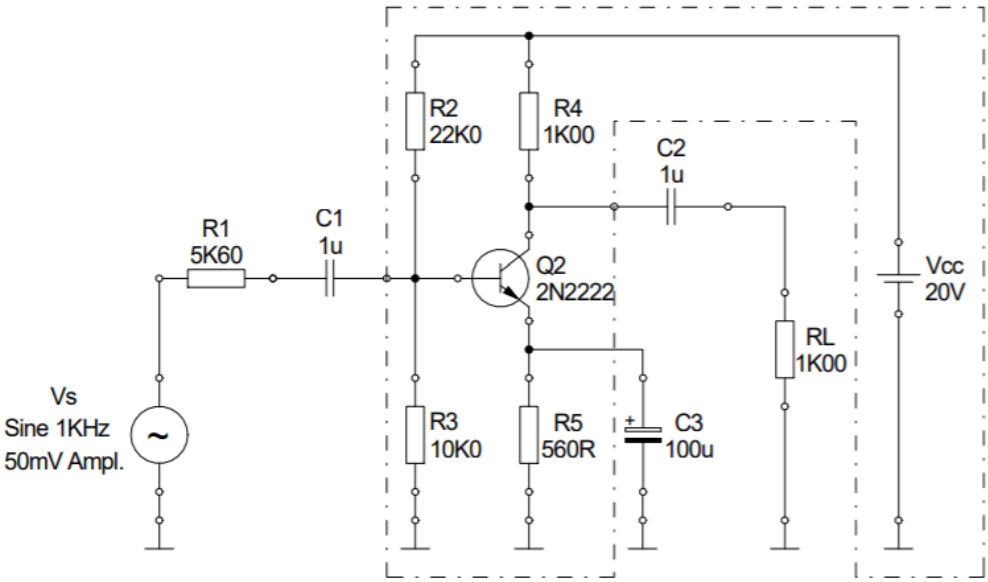


The transistor is NPN. It could be proved from the picture above. We can say when we connect the negative lead of multimeter to the base of NPN transistor and the positive lead to other two pins, the current path will be block due to diodes being reverse biased diode and we will get .OL in each case. If the transistor was PNP we would get a reading rather than .OL.

3. Explain why Problem 5.3.1.(3) can be used to determine the collector and the emitter terminals.

The multimeter was set to diode testing function. This means that the emitter-base junction has a greater forward voltage drop than the collector base junction. This is due to difference in doping concentration between the collector and emitter regions of the transistor. The emitter is more heavily doped than the collector, making the junction with the base provoke a higher voltage drop.

5.3.2 Problem 2: Operating point of BJTs



RESULTS:

Vcc	20.01
Vb	6.03
Ve	5.39
Vc	10.46
Vce	5.06
Vbe	0.65

Evaluation:

	Measured Value	Theoretical Value
Vcc	20.01	20V
Vb	6.03	6.3354V
Ve	5.39	5.61838V
Vc	10.46	10.0169V
Vce	5.06	4.39852V
Vbe	0.65	0.71702 V

Both the measured and the theoretical values are very close to each other. The small differences can be seen due to the tolerances of the equipment used. Also the Beta is different for the theoretical and the real measurements.

what does equipment mean??

2. Calculate the common emitter current gain β. Use only measured values!

$$\alpha = \frac{I_C}{I_E} \text{ and } \beta = \frac{\alpha}{1-\alpha}$$

By considering that the values of the resistor are the same as the measured one we can easily calculate I_C and I_E.

$$I_C = \frac{V_{CC} - V_C}{R4}$$

*(note that Vc is not the voltage drop over the resistor R4 but that at the collector pin)

$$I_C = \frac{20.01 - 10.46}{1000} = 9.55mA$$

To calculate Ie we use the following relationship:

$$I_E = \frac{V_E}{R5} = \frac{5.39}{560} = 9.625\ mA$$

From the two-above values alpha can be calculated.

$$\alpha = \frac{I_C}{I_E} = \frac{9.55mA}{9.625mA} = 0.9922$$

Therefore, the value of β is:

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9922}{1 - 0.9922} = 127.2$$

3. Determine the error sources with approximate values and -CALCULATE- the relative error of the calculated β. Check the plausibility of your previous calculated value by comparing it to the simulation. If the error is to high what is the reason and is there a way to avoid it?

The errors are due to accuracy of the measuring devices and the resistors tolerance. Assume $The\ known\ tolerance\ of\ resistor\ is\ \pm 1\%\ and\ \pm 0.25\%\ for\ accuracy\ of\ voltage.\ Using\ the\ formula\ below, we\ can\ see\ that\ \alpha \approx \pm 2.5\%$

$$\alpha = \frac{I_C}{I_E} = \frac{V_{R4} * R_5}{R_5 * V_5} = 1 + 1 + 0.25 + 0.25 = 2.5\%$$

For calculating β error we differentiate the formula below.

$$\beta = \frac{\alpha}{1-\alpha}$$
$$= \frac{d\beta}{d\alpha} = \Delta E_\beta = \left|\frac{1}{(1-\alpha)^2} * \Delta\alpha\right|$$

$$\Delta E_\beta = \left|\frac{1}{(1-0.9922)^2} \times 0.9922 \times 0.025\right| = 407.7087442$$
$$\%E_\beta = \frac{\Delta E_\beta}{\beta} \times 100 = \frac{407.7087442}{127.21} \times 100 = 320.5005457\%$$

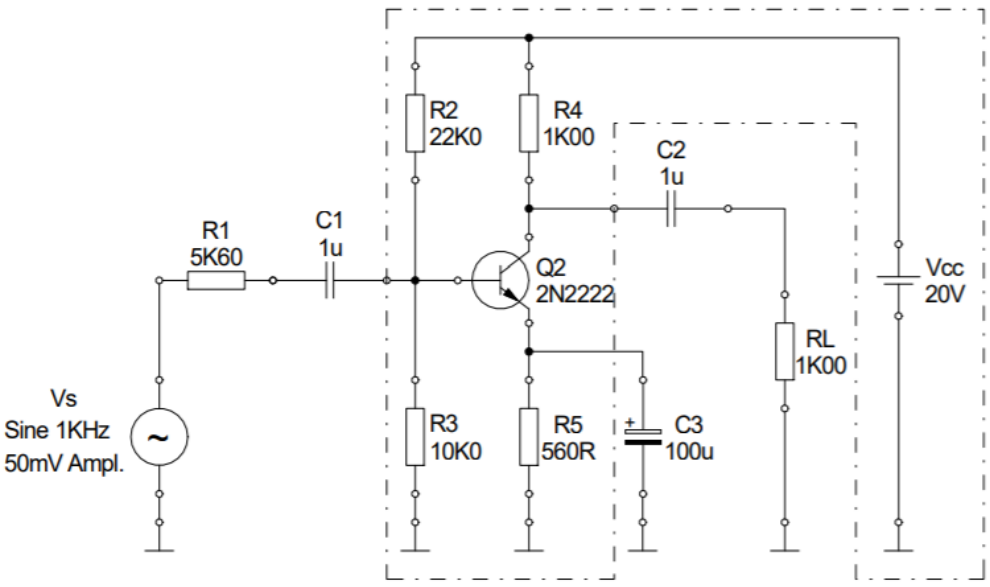
When the value of α increases towards 1, we obtain a larger error value meaning that the error of β also increases. In this, case however we see the error of the gain is even higher than 100% meaning that the error is very high, and the value is highly deviated from the actual one.

5.3.3 Problem 3: Common emitter Circuit

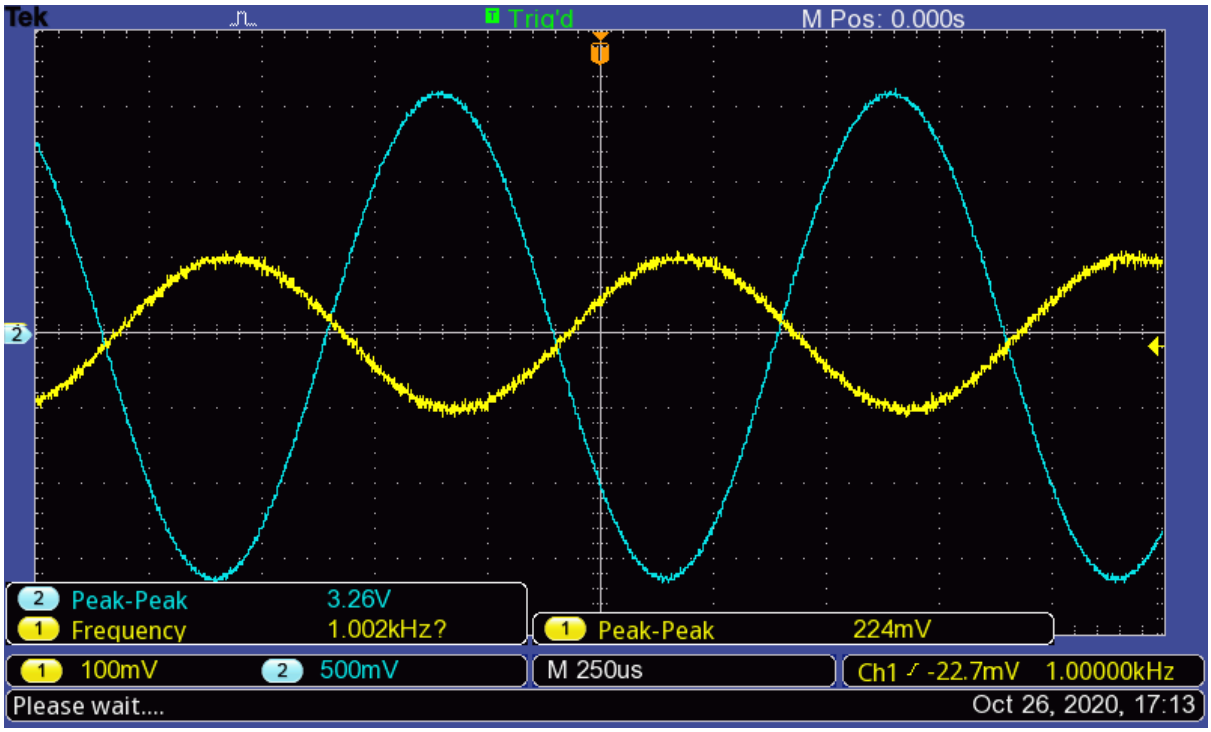
The purpose of this problem is to show the BJT amplification of small signals when it is correctly biased to work in the active mode of operation. The same circuit as before is used but now the all the components are assembled.

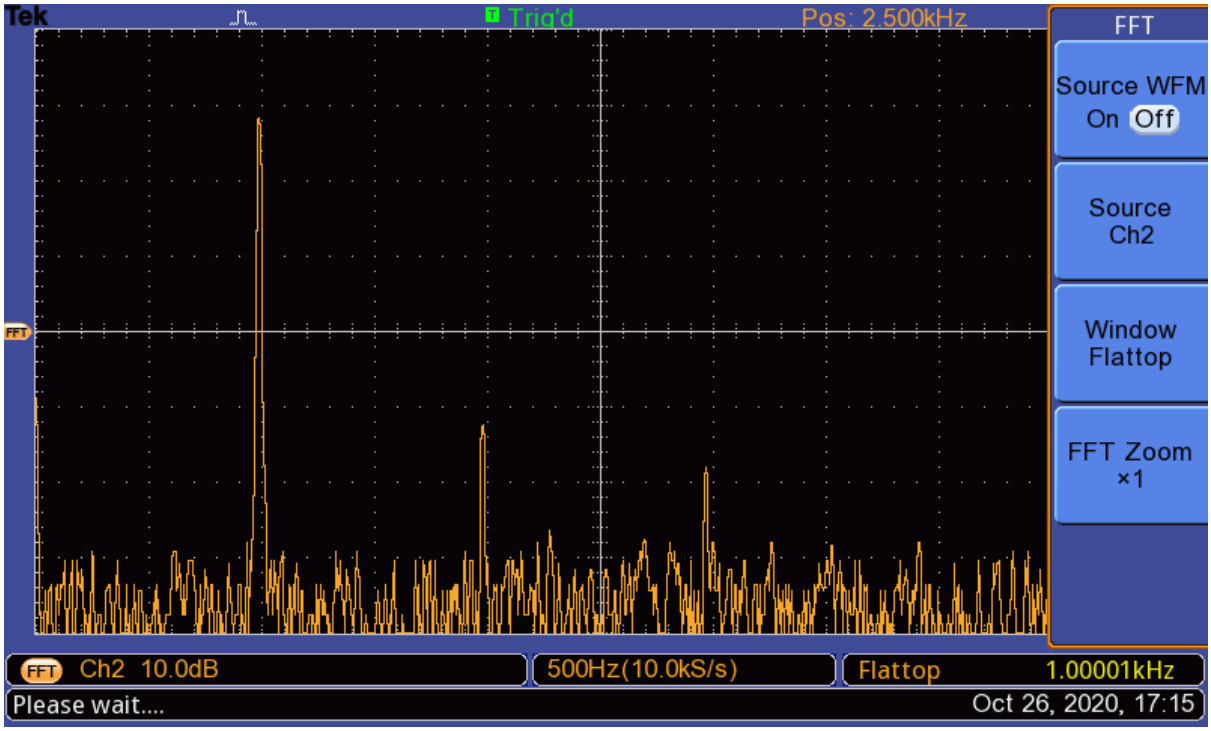
As input signal a 10KHz 50mV amplitude sine wave was used. The value of the amplitude was increased to see the clipping effect of amplifier. A hardcopy of this state is shown below.

Following circuit was assembled:



2. Connect the oscilloscope to the base and over RL of the circuit. Use f = 10KHz. Starting from 50mV amplitude(!), slowly increase VS. You can observe the clipping of the output signal at some value. Take a hardcopies showing the distorted state and measure the peak-to-peak voltages.

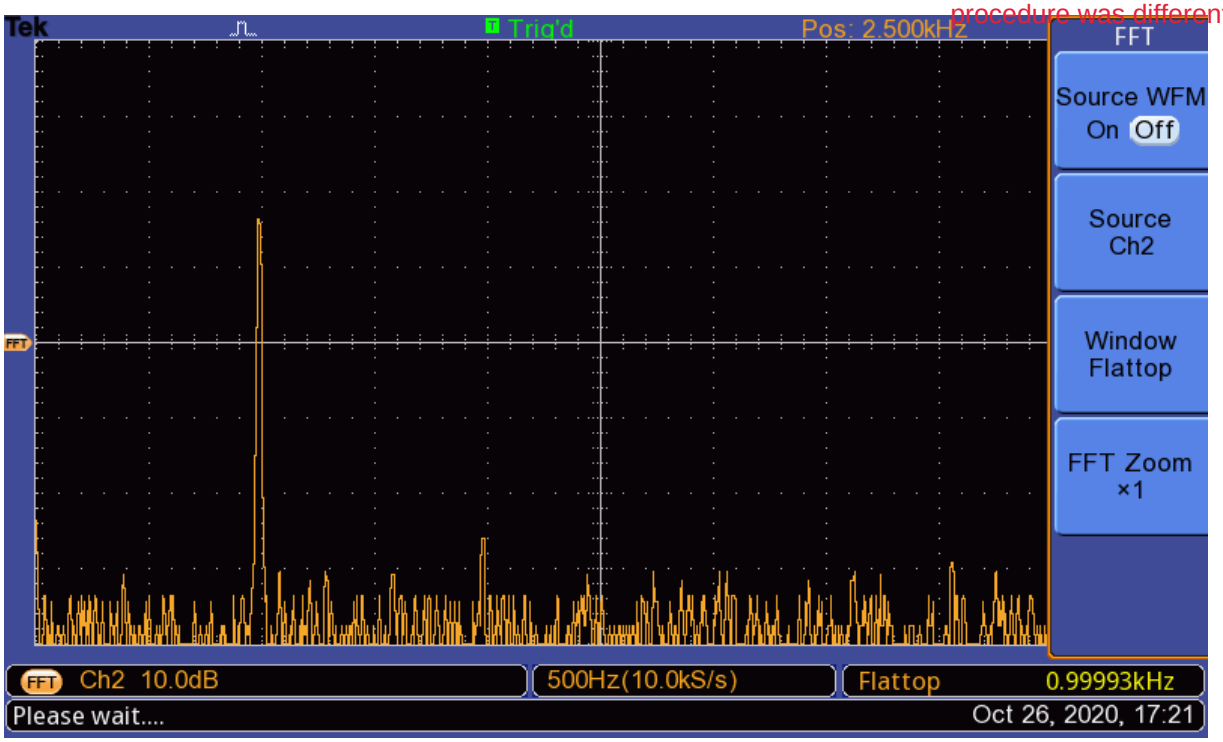




As we can see from the FFT, there is no point in increasing for Vs as it distorts more.

3. Slowly reduce VS for maximum undistorted output signal. Again take a hard copies at this state and measure the peak-to-peak voltages.

where did you find this request?? procedure was different!!



The value we obtained is V_{PP} = 50m

Evaluation:

1. In what region of the output characteristic is the circuit for a distorted positive or negative amplitude? Explain! What is the condition in your case?

At first, Vs = 50mV the input signal was amplified without any distortion because the BJT was biased in the active operating region. An increase in Vs yielded clipping in the negative part of the output signal, something that was very noticeable for us at Vs =340. It could also be seen in the frequency spectrum that we had extra peaks. Since the clipping occurs the negative part of the output signal, this means that the transistor changes the operation mode from the active region to the saturation region (in our case we do not enter the cut off region). Due to non linear amplification we have distortion. The current IB becomes really large, forcing the operation to the upper end of the output load line. Also when decreasing Vs to obtain maximum undistorted output signal we found it to be when Vs=167mV, which was also proven by checking the frequency spectrum.

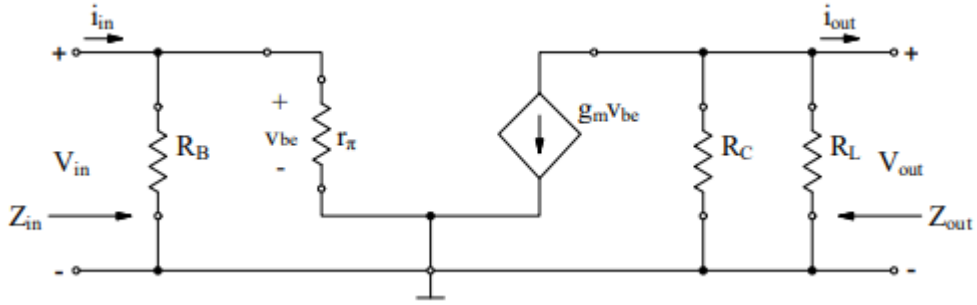
2. Using the measurements taken in the lab, calculate the voltage gain AV of the amplifier.

Voltage Gain = VOUT/VIN= 3.72/41.6*10e-3= 89.423

3. Determine from the hard copies, what is the phase relationship between the input and the output signals?

4. Explain the reason for such a relation.

We see that the amplitudes of the inputs and output signals are inversely related. Therefore the phase shift between both signal is 180 degrees. The reason is very well explained in lab manual with hybrid pi model.



This is an equivalent circuit of a BJT.

$$A_i = \frac{i_o}{i_{in}} = -g_m \frac{R_C(R_B||r_\pi)}{R_C + R_L}$$

The negative signin the voltage gain expression means that Vin and Vout are 180 degress out of phase. In the other words, signal was amplified and inverted by amplifier.

Also, this can be understood very simple as it is the principle of the BJT amplifier. When the current at the base increases (as the voltage increases) the current value of the collector increases which makes the voltage drop over bigger leading to a smaller Vc value.

5.3.4 Problem 4: Bandwidth of amplifier circuit

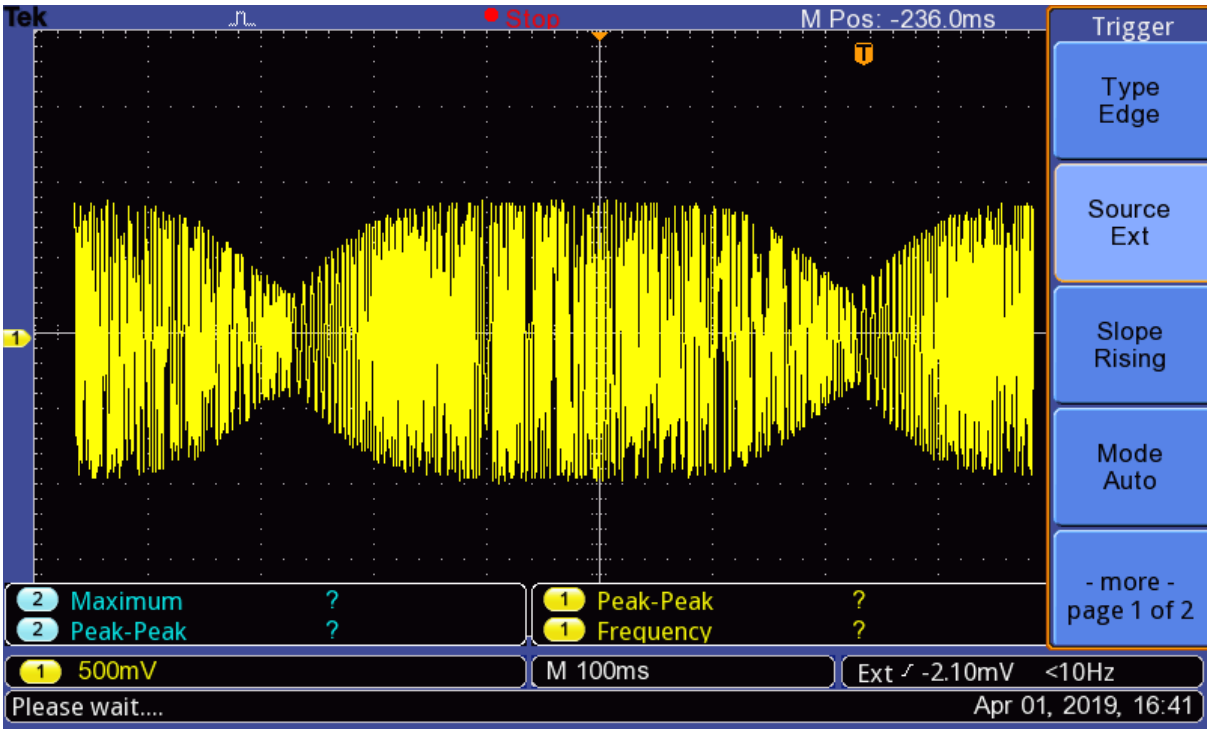
1. Using 50mV peak for VS. Enable the sweep mode of the function generator for the following settings:

The purpose of this problem is to determine the bandwidth of the BJT amplifier circuit and to observe how the voltage gain of a BJT is affected with changing the frequency of the input signal.

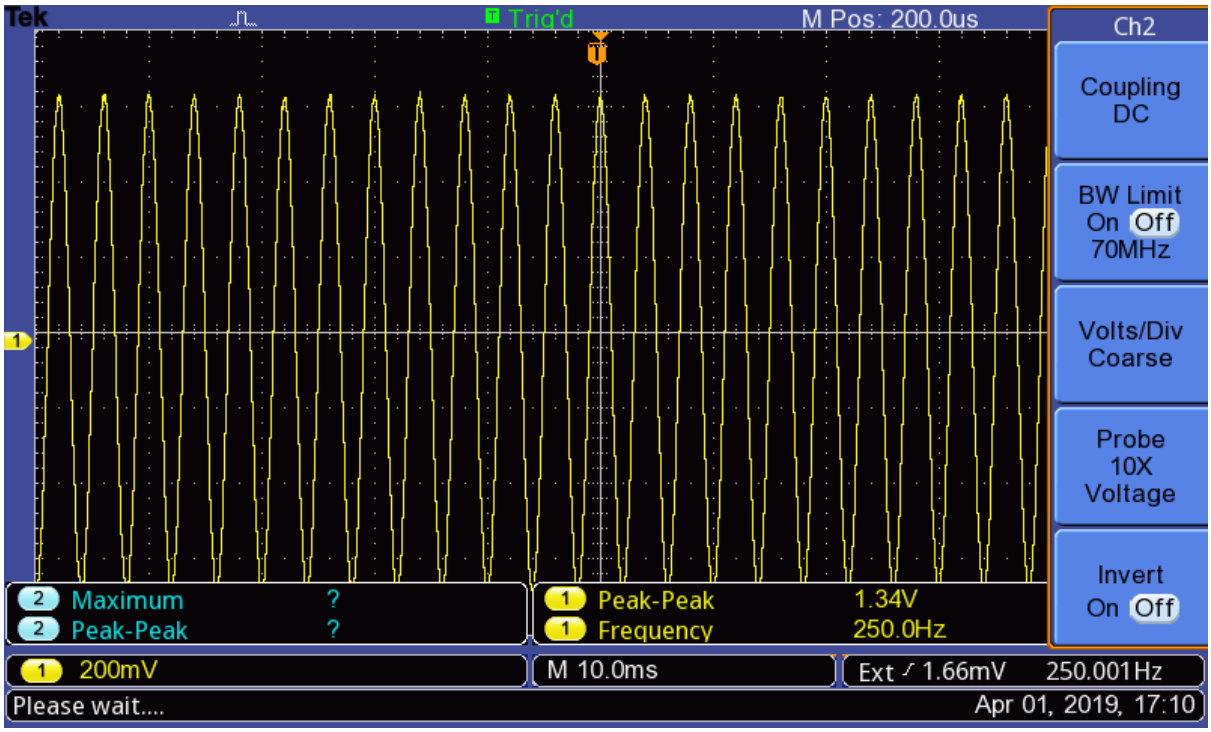
- START F : 100Hz
- STOP F : 1MHz
- SWP TIME : 500ms
- SWP MODE : logarithmic

Note: Use the SYNC output of the generator as trigger source for the oscilloscope.

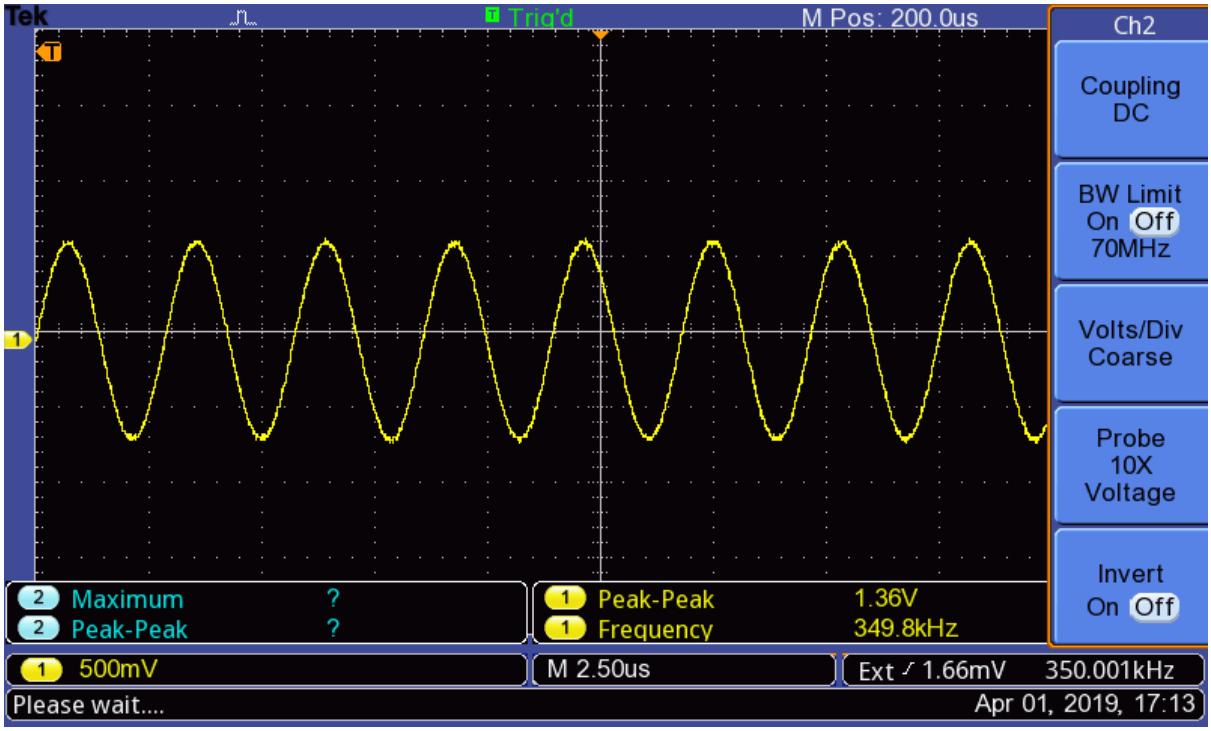
2. Adjust the oscilloscope to observe the output signal across the load resistor RL and take hard copies.



3. Disable the sweep mode of the function generator. Without changing the amplitude of VS, manually change the frequency of the function generator to obtain the lower −3dB cut-off frequency.



4. Without changing the amplitude of VS, manually change the frequency of the function generator to obtain the upper −3dB cut-off frequency.



Obtained Value = 349.8 KHz

Evaluation:

1. In Problem 5.3.4.(2), explain your observation.

We see that with the increase of frequency in our scope, the amplitude starts out low and then keeps increasing until a certain frequency, and then the amplitude decreases again. The bode plot of this system acts the same way in terms of the amplitude plot. In addition, the capacitor filters out lower frequency components and for high frequencies we observe that the transistor can't follow the deviation in the base current. Therefore, we conclude that we have a bandpass filter.

2. Using the measurements taken in the lab, calculate the amplifier bandwidth

BW=349.8kHz-250Hz=349550Hz

3. Compare to the simulation!

In the one simulated we have a bandwidth of ---, and we see that the value obtained is much smaller. There are many errors that could cause this deviation, such as the transistor's ability to withstand higher frequency's property may be lost to a certain extent. In addition, we have all instrumental errors in the experimental process which also contribute in this deviation of the value.

simulation is not complete I guess??

Conclusion:

Throughout this lab, we learned several applications of a BJT transistor, how it is used, its pins, and type defining. In the first part of the lab, I was able to learn how to identify the pins and type by observing voltage drops or overloads on my multimeter such that what is obtained defines our pins and type. The beta current amplification factor was also handled, such that we saw that a lot of errors came along, from the transistor and other instruments that were used. In the second part, we added the use of a Zener diode along with the BJT transistor such that it is paired with a constant current source. Throughout this part, we were able to compare the values obtained in the prelab and see how our theoretical and experimental values deviate from one another. Lastly, the bandpass characteristics of the amplifier were observed in the last part of the lab where the cut off frequencies were considered to find the bandwidth. In conclusion, this lab experiment was pretty interesting as we got to observe the use of a transistor and how its bias is a key factor in order to obtain an output which is not distorted and get information such as the current gain factor and the output voltage/current. However, during this experiment it was also evident that experimental and systematic errors could play a key role in affecting our values.

References:

Lab Manual, Datasheet

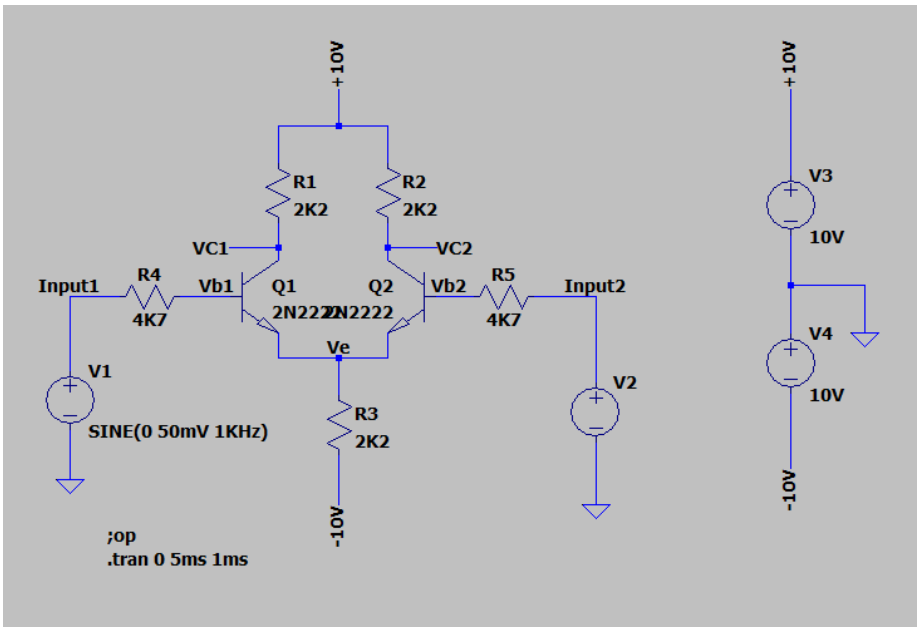
I guess you forgot at least one lab report from 2019!!!

APPENDIX:

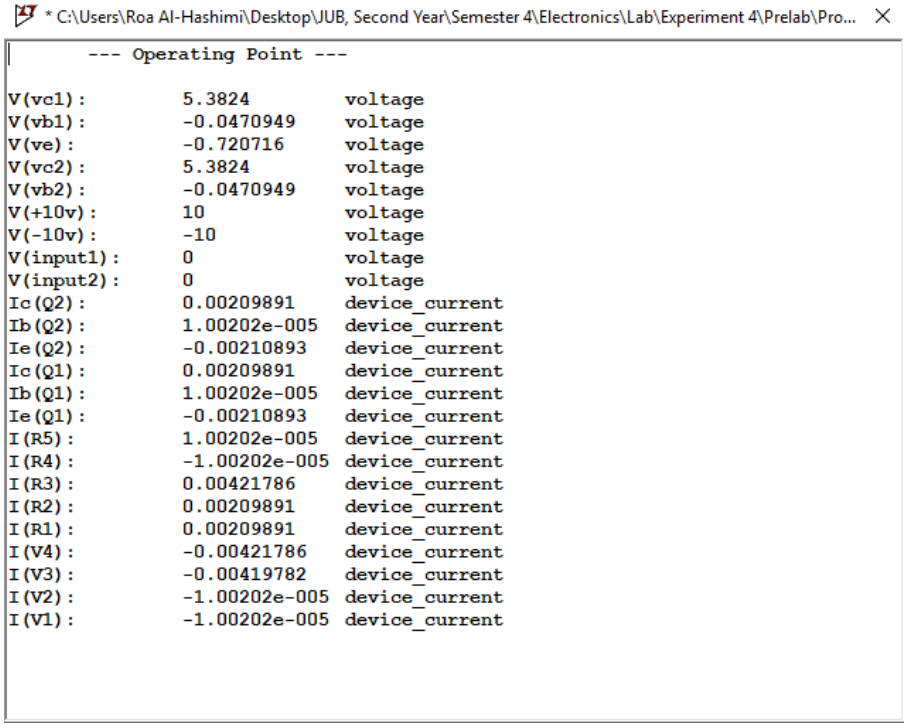
Prelab of OpAmps:

Problem 1: Simulate a differential Amplifier

1) **Perform a dc operation point analysis for the above circuit.**



Values obtained from LTSpice:

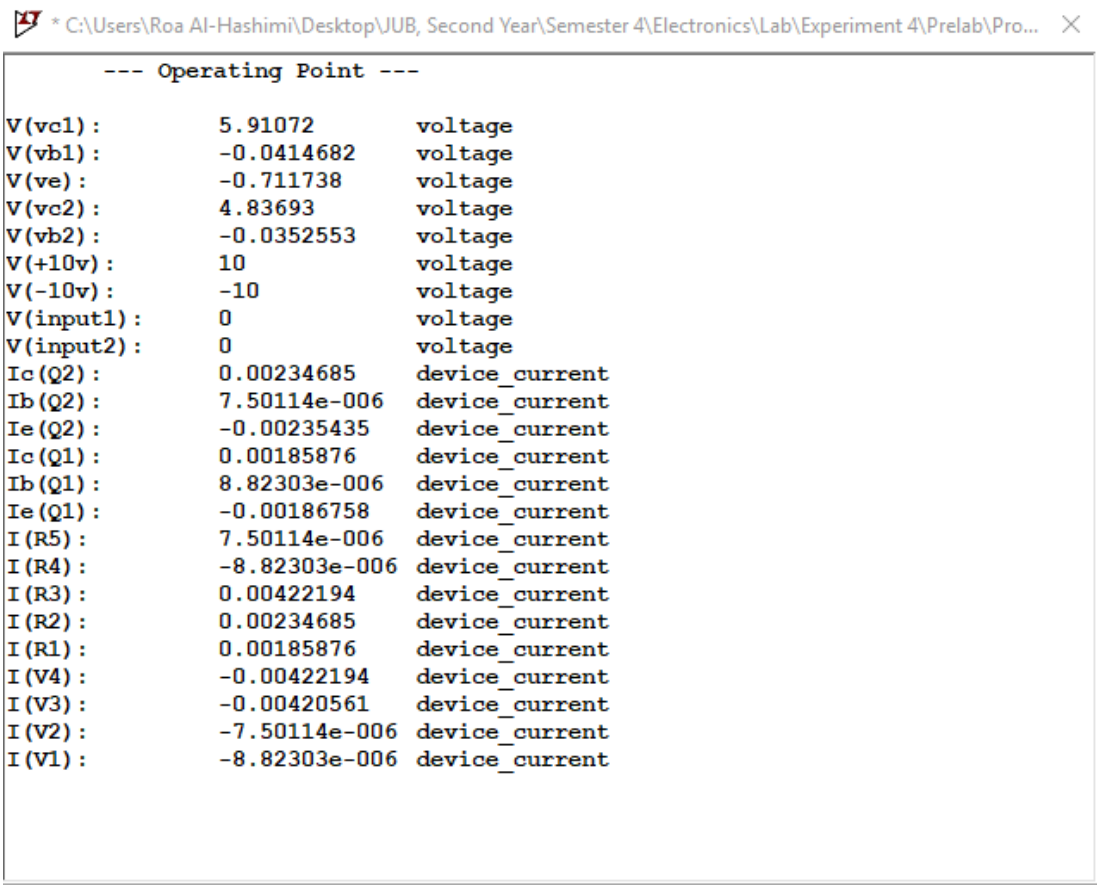


Required values	Value
V_{BE1}	V(vb1)-V(ve)=-0.0470949+0.720716= 0.6736 V
V_{BE2}	V(vb2)-V(ve)=-0.0470949+0.720716= 0.6736 V
V_{C1}	5.3824 V
V_{C2}	5.3824 V
I_{C1}	2.09891 mA
I_{C2}	2.09891 mA
I_{E1}	2.10893 mA
I_{E2}	2.10893 mA
I_{RE}	4.21786 mA

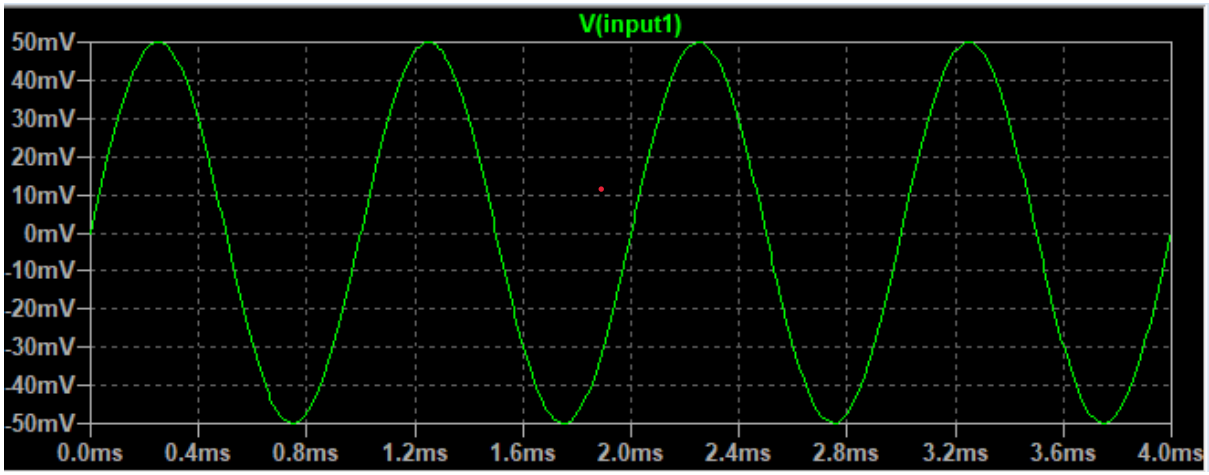
Changing transistor to 2N3904:

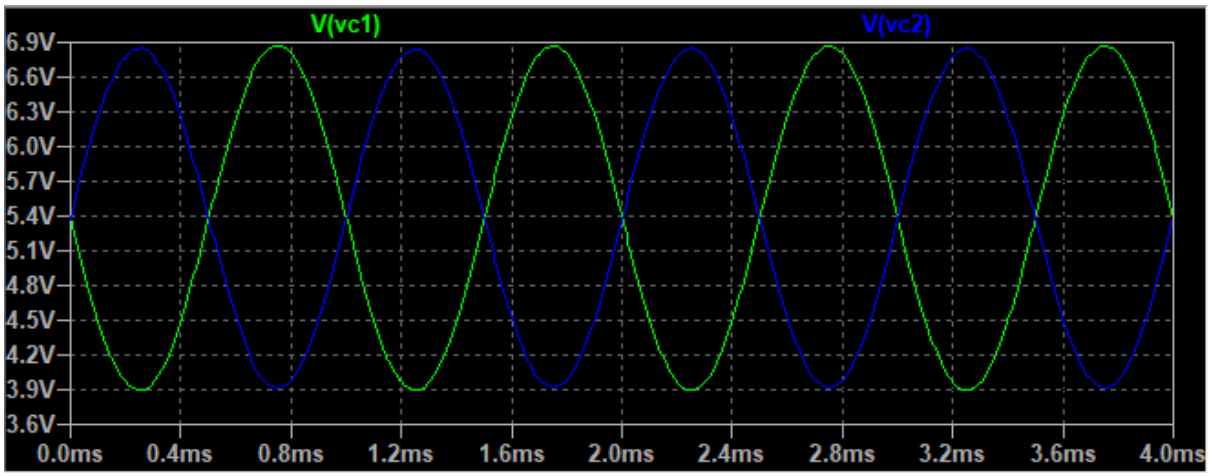
When we perform this change of transistor, we see that the values of the two branches are not the same and it is only true that they are identical when they are identical. Voltages and currents change due to having a different β in our case.

(Values from LTSpice):


* C:\Users\Roa Al-Hashimi\Desktop\JUB, Second Year\Semester 4\Electronics\Lab\Experiment 4\Prelab\Pro...
--- Operating Point ---
V(vc1): 5.91072 voltage
V(vb1): -0.0414682 voltage
V(ve): -0.711738 voltage
V(vc2): 4.83693 voltage
V(vb2): -0.0352553 voltage
V(+10v): 10 voltage
V(-10v): -10 voltage
V(input1): 0 voltage
V(input2): 0 voltage
Ic(Q2): 0.00234685 device_current
Ib(Q2): 7.50114e-006 device_current
Ie(Q2): -0.00235435 device_current
Ic(Q1): 0.00185876 device_current
Ib(Q1): 8.82303e-006 device_current
Ie(Q1): -0.00186758 device_current
I(R5): 7.50114e-006 device_current
I(R4): -8.82303e-006 device_current
I(R3): 0.00422194 device_current
I(R2): 0.00234685 device_current
I(R1): 0.00185876 device_current
I(V4): -0.00422194 device_current
I(V3): -0.00420561 device_current
I(V2): -7.50114e-006 device_current
I(V1): -8.82303e-006 device_current

2) **Perform a transient analysis.**

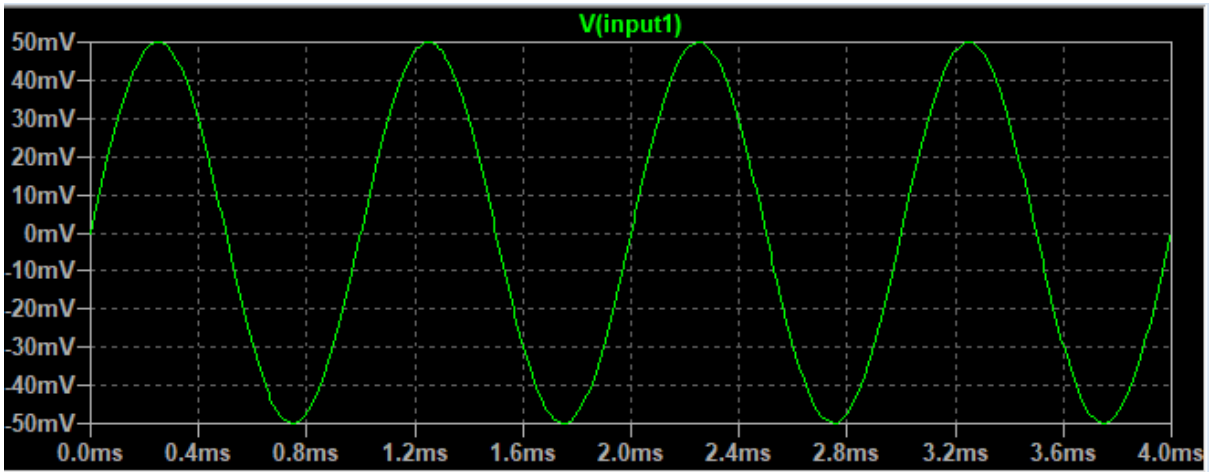


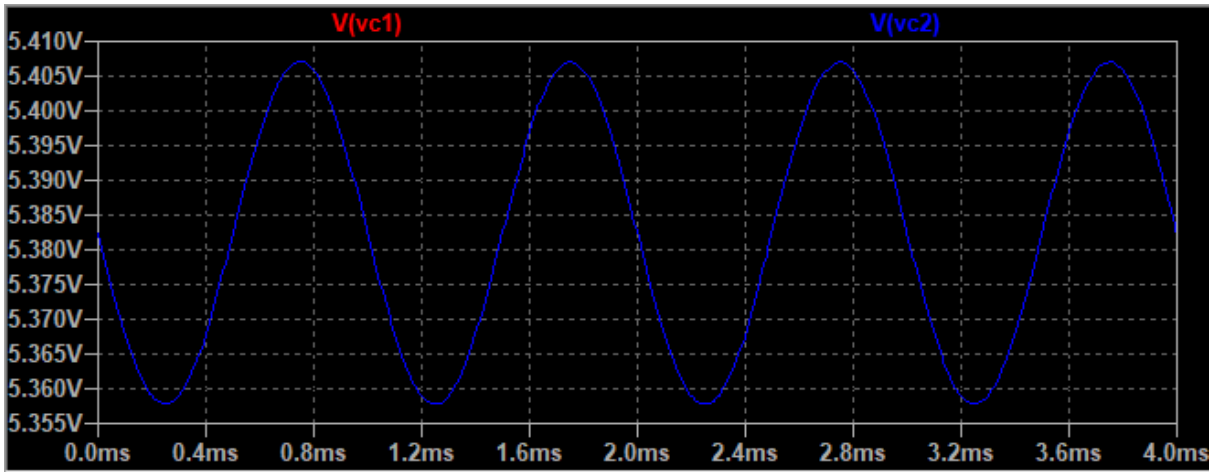


The two plots will have the same Vpp since they are only shifted by 180 degrees with respect to each other, where Vpp=2.97436V in our case.

$$A_{vdiff} = 20\log\left(\frac{Vc}{Vi}\right) = 20\log\left(\frac{2.97436}{100mV}\right) = 29.46787064 \text{ dB}$$

3) Perform a simulation with common mode input.





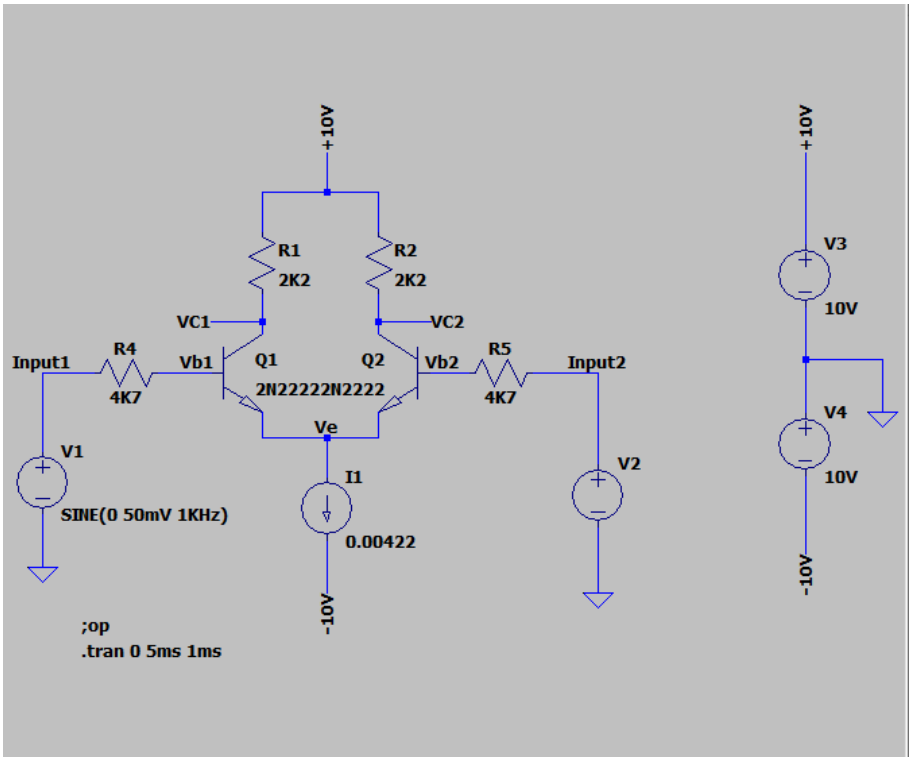
The two plots are on top of each other, you can see on the legend that we have V(vc1) and V(vc2). Therefore, they also share the same peak to peak value. In our case that is Vpp=49.26138 mV.

$$A_{vdiff} = 20\log\left(\frac{Vc}{Vi}\right) = 20\log\left(\frac{49.226138\text{mV}}{100mV}\right) = -6.156084703\ dB$$

4) Calculate the common-mode rejection ratio in dB!

$$A_{common} = Av_{diff} - Av_{comm} = 29.46787064 - -6.156084703 = 35.62395534\ \text{dB}$$

5) **Replace the resistor R3 by a current source.**



Values from LTSpice:

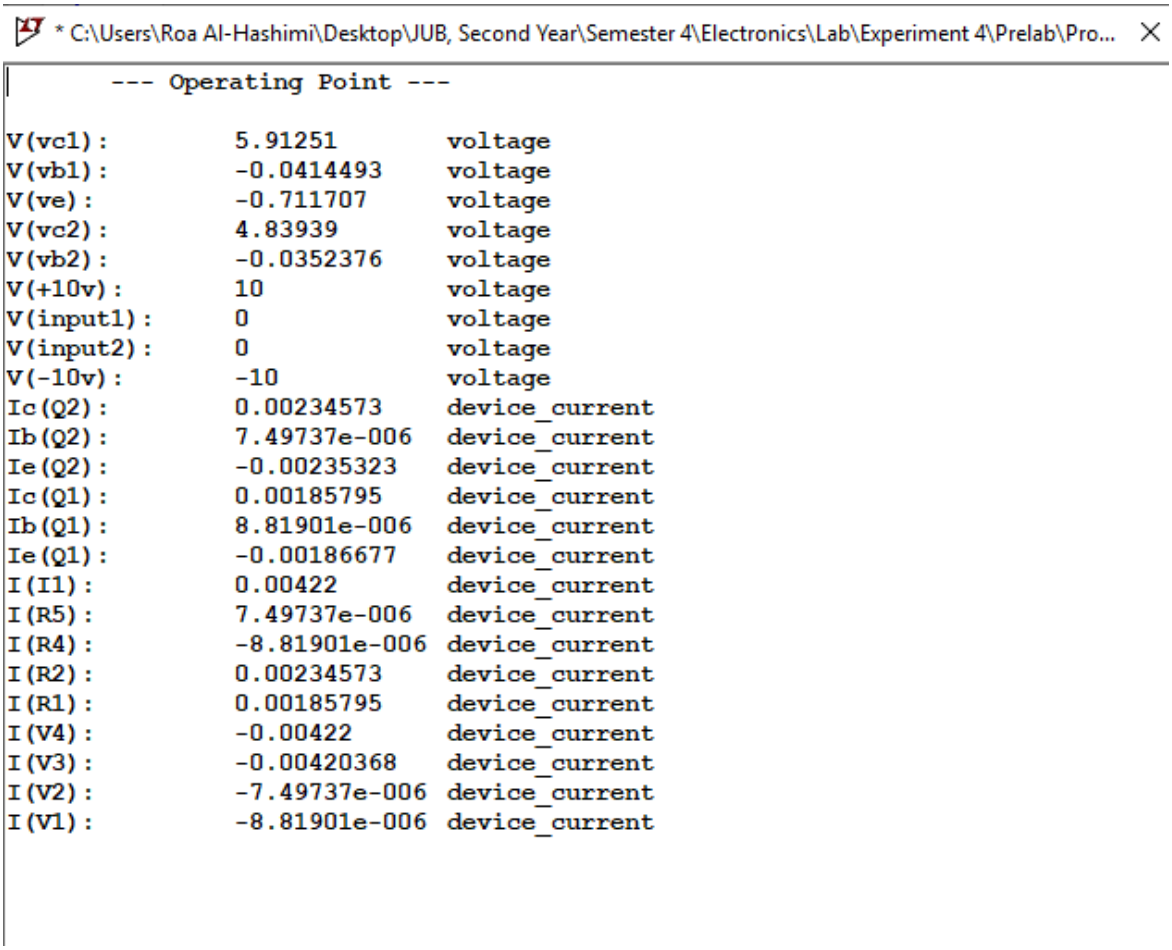
```
        --- Operating Point ---

V(vc1):         5.38006         voltage
V(vb1):         -0.04712        voltage
V(ve):          -0.720756       voltage
V(vc2):         5.38006         voltage
V(vb2):         -0.04712        voltage
V(+10v):        10              voltage
V(input1):      0               voltage
V(input2):      0               voltage
V(-10v):        -10             voltage
Ic(Q2):         0.00209997      device_current
Ib(Q2):         1.00255e-005    device_current
Ie(Q2):         -0.00211        device_current
Ic(Q1):         0.00209997      device_current
Ib(Q1):         1.00255e-005    device_current
Ie(Q1):         -0.00211        device_current
I(I1):          0.00422         device_current
I(R5):          1.00255e-005    device_current
I(R4):          -1.00255e-005   device_current
I(R2):          0.00209997      device_current
I(R1):          0.00209997      device_current
I(V4):          -0.00422        device_current
I(V3):          -0.00419995     device_current
I(V2):          -1.00255e-005   device_current
I(V1):          -1.00255e-005   device_current
```

Required values	Value
V_{BE1}	V(vb1)-V(ve)= -0.04712+0.720756= 0.6736 V

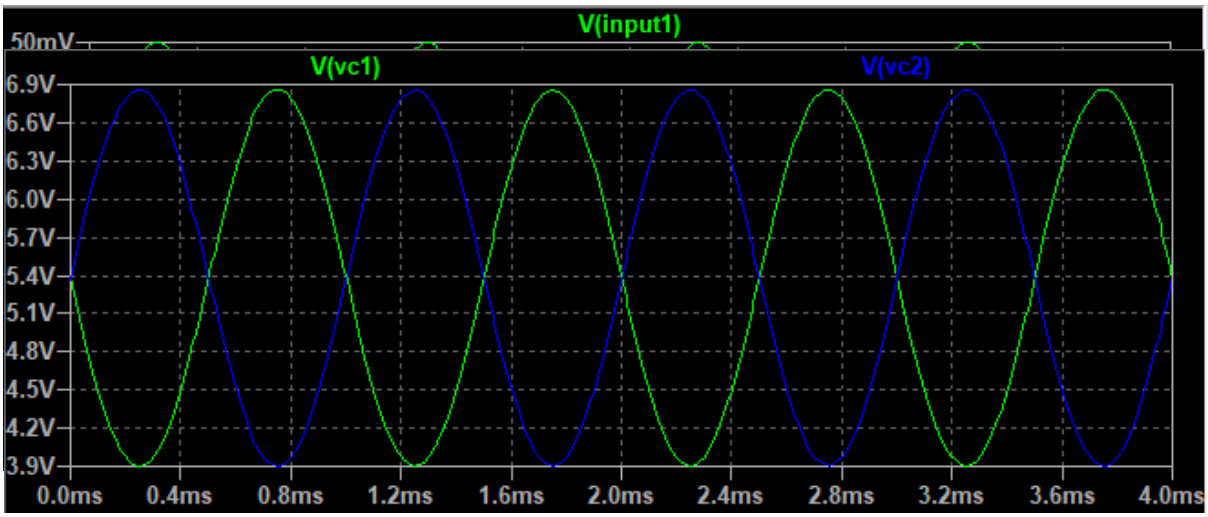
V_{BE2}	V(vb2)-V(ve)= -0.0470949+0.720716= 0.6736 V
V_{C1}	5.38006 V
V_{C2}	5.38006 V
I_{C1}	2.0909997 mA
I_{C2}	2.0909997 mA
I_{E1}	2.111 mA
I_{E2}	2.111 mA
I_{RE}	4.22 mA

Changing transistor to 2N3904:

We see that the values are very similar in this case and the previous one. If one of the transistors is also changed in this case, we also see a variation in the values as explained previously. (Values from LTSpice listed below):



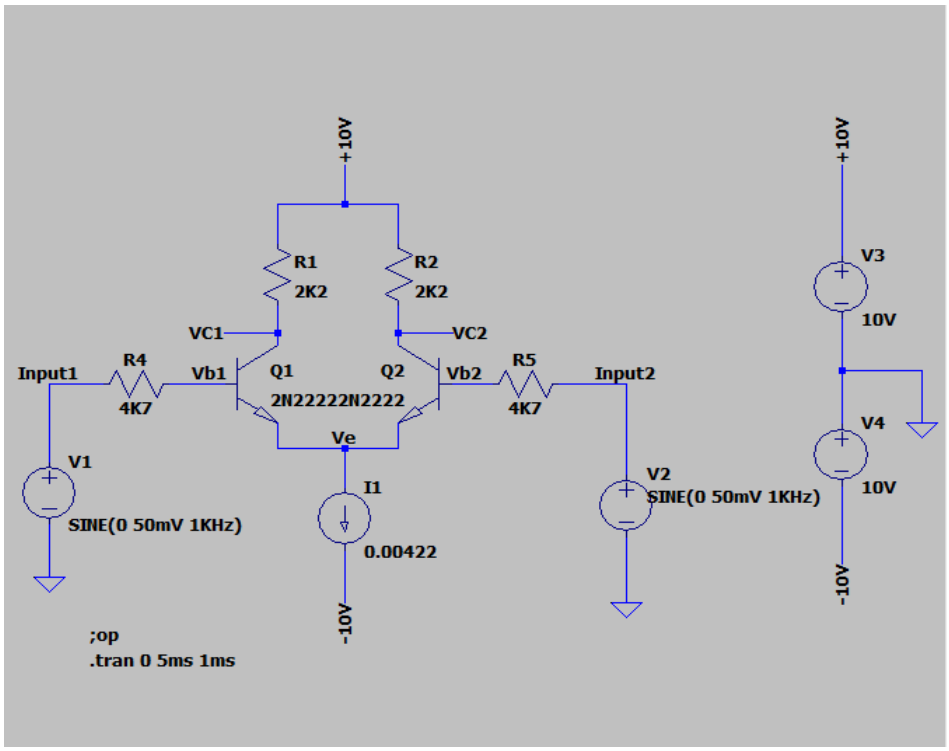
6) **Repeat steps 1-4.**



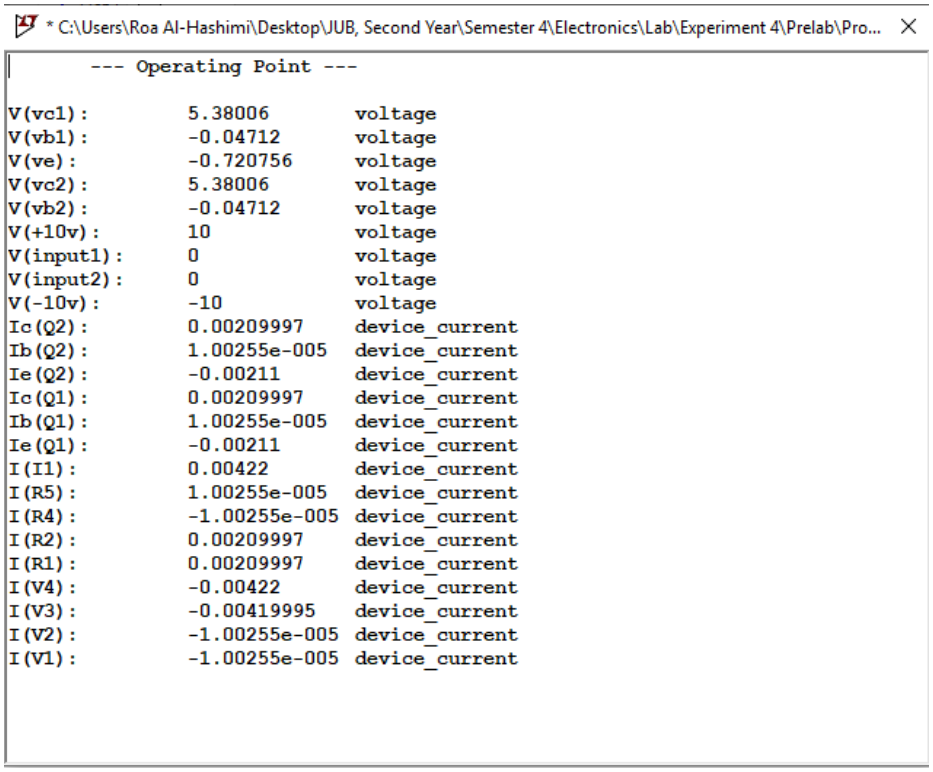
The two graphs will have the same Vpp since they are only shifted by 180 degrees with respect to each other, where Vpp=-2.9511577V in our case.

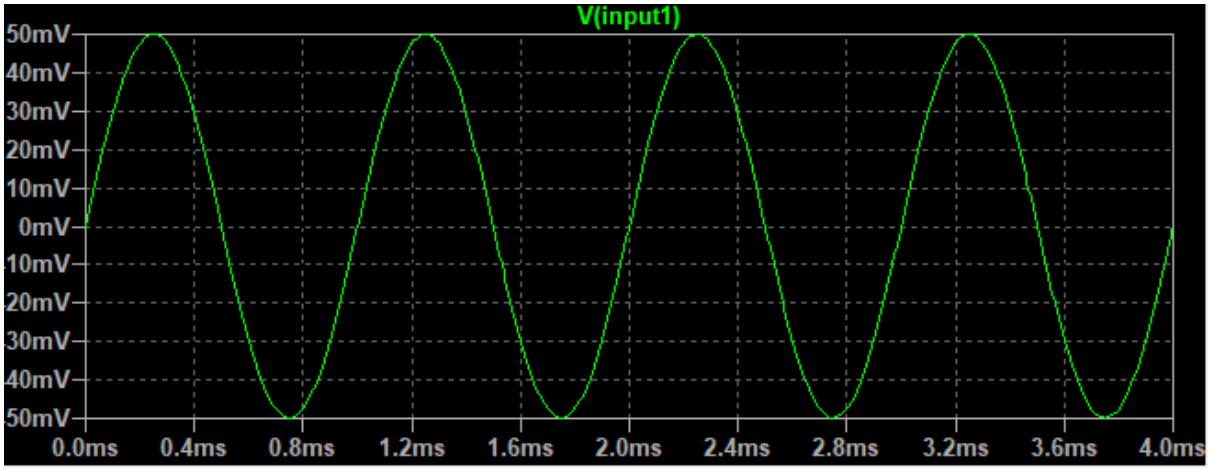
$$A_{vdiff} = 20\log\frac{Vc}{Vi} = 20\log\left(\frac{2.9511577V}{100mV}\right) = 29.39984835\ \text{dB}$$

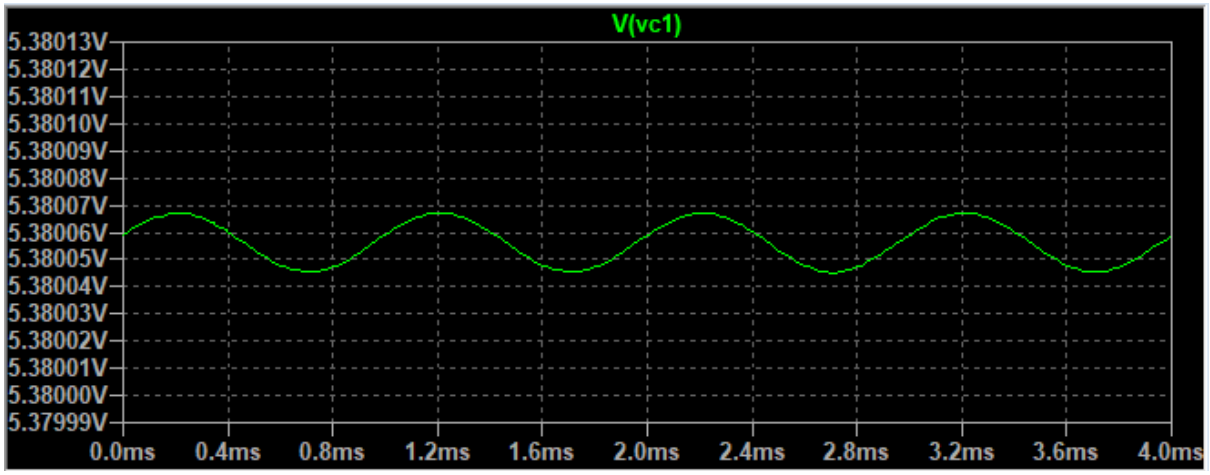
Now changing V2 voltage source, as a sinusoidal as well:

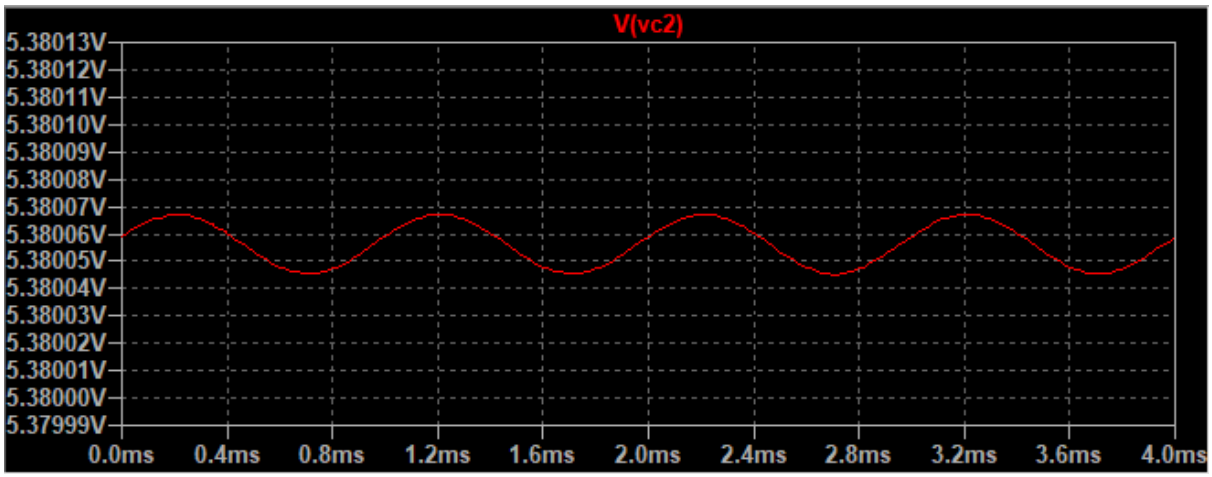


LTSpice values listed below:


* C:\Users\Roa Al-Hashimi\Desktop\JUB, Second Year\Semester 4\Electronics\Lab\Experiment 4\Prelab\Pro...
--- Operating Point ---
V(vc1): 5.38006 voltage
V(vb1): -0.04712 voltage
V(ve): -0.720756 voltage
V(vc2): 5.38006 voltage
V(vb2): -0.04712 voltage
V(+10v): 10 voltage
V(input1): 0 voltage
V(input2): 0 voltage
V(-10v): -10 voltage
Ic(Q2): 0.00209997 device_current
Ib(Q2): 1.00255e-005 device_current
Ie(Q2): -0.00211 device_current
Ic(Q1): 0.00209997 device_current
Ib(Q1): 1.00255e-005 device_current
Ie(Q1): -0.00211 device_current
I(I1): 0.00422 device_current
I(R5): 1.00255e-005 device_current
I(R4): -1.00255e-005 device_current
I(R2): 0.00209997 device_current
I(R1): 0.00209997 device_current
I(V4): -0.00422 device_current
I(V3): -0.00419995 device_current
I(V2): -1.00255e-005 device_current
I(V1): -1.00255e-005 device_current







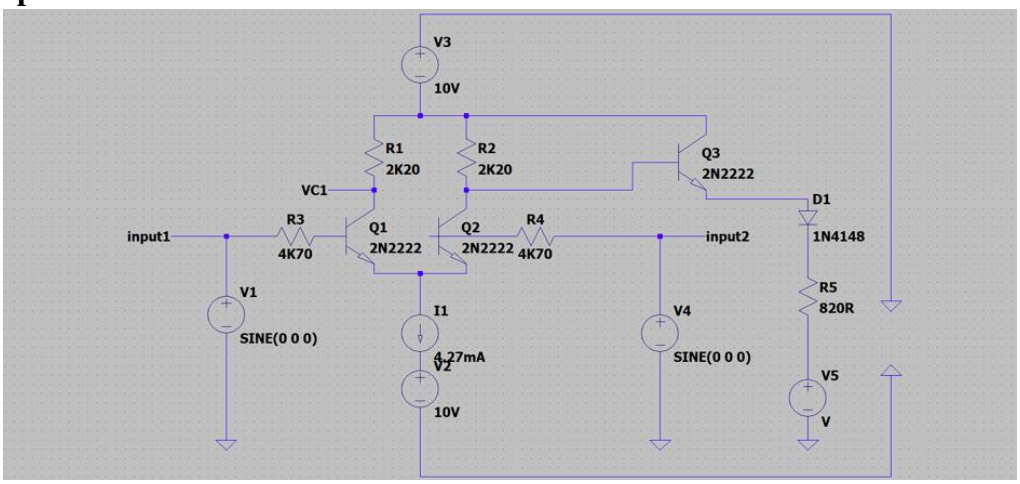
The two plots are on top of each other, however this time I plotted V(vc1) and V(vc2) on two different plots, but the same concept applies. Therefore, they also share the same peak to peak value. In our case that is Vpp=21.453832µV.

$$A_{vdiff} = 20\log\frac{Vc}{Vi} = 20\log\left(\frac{21.453832\mu V}{100mV}\right) = -73.36990249\ dB$$

$$A_{common} = Av_{diff} - Av_{comm} = 29.39984835 - -73.36990249 = 102.7697508 dB$$

Problem 2: Construct on OP-Amp

1) **Calculate the voltage at the output of the emitter follower when both inputs are connected to ground. Assume β = 200 and UBE = 0.7V. The forward voltage drop of the diode is 0.7V.**



simulation commands?? without incomplete

From the Simulation we can see that the current we got it 0.0042Amp = 4.22mA. For the current at T2, we will divide the result/2 hence 4.22/2 = 2.11mA.
To calculate voltage at

$$R_2 = 10V - R_2 \times 2.11mA = 10V - (2200) \times 2.11 \times 10^{-3} = 5.36V$$

To calculate $Vout = 10V + 10V - 20.7V - 4.64V - V_x = 0$
$V_x =$ 13.96V.
Now we will calculate the total resistance = 820Ω +2200Ω = 3020Ω.
To calculate the current, we will = $I = \frac{V_x}{R} = \frac{13.96}{3020} = 0.00462Amp = 4.62mA$.
Now we will calculate the voltage at R = 2200, $V = 2200 \times 0.00462A = 10.164V$
Hence, $V_{out} = 10.164 - 10V = 0.164$.

2) **Perform a dc operation point analysis. Determine the output voltage and compare to your calculation.**

```
--- Operating Point ---

V(vc1):         -10.241         voltage
V(n004):        -9.51955        voltage
V(n006):        -10.2495        voltage
V(n002):        -10.241         voltage
V(n005):        -9.51955        voltage
V(n001):        -10             voltage
V(input1):      0               voltage
V(input2):      0               voltage
V(n008):        10              voltage
V(n003):        -0.000184535    voltage
V(n009):        0               voltage
V(n007):        -8.39754e-009   voltage
Ic(Q3):         2.42769e-013    device_current
Ib(Q3):         -1.04853e-011   device_current
Ie(Q3):         1.02409e-011    device_current
Ic(Q2):         0.000109563     device_current
Ib(Q2):         0.00202544      device_current
Ie(Q2):         -0.002135       device_current
Ic(Q1):         0.000109563     device_current
Ib(Q1):         0.00202544      device_current
Ie(Q1):         -0.002135       device_current
I(D1):          -1.02409e-011   device_current
I(I1):          0.00427         device_current
I(R5):          -1.02409e-011   device_current
I(R4):          0.00202544      device_current
I(R3):          -0.00202544     device_current
I(R2):          0.000109563     device_current
I(R1):          0.000109563     device_current
I(V5):          -1.02409e-011   device_current
I(V4):          -0.00202544     device_current
I(V3):          0.000219127     device_current
I(V2):          0.00427         device_current
I(V1):          -0.00202544     device_current
```

Voltage at Output	184.5mV

3) Determine AV diff , AV cm, and the common-mode rejection ratio in a similar way like in problem 1. 4. What is the inverting and what the non-inverting input?

And then we have $V_{id} = V_{in1} - V_{in2} = 100\,mV$

Using this we get $A_{vdiff}[dB] = 20 \log\left(\frac{V_{od}}{Vid}\right) = 26.54dB$

Now for A_{Vcm}: $Voc = Vpp = 16.41\mu V$

and for V_{IC} we have

$V_{IC} = V_{IN1} - V_{IN2} = 100\,mV$

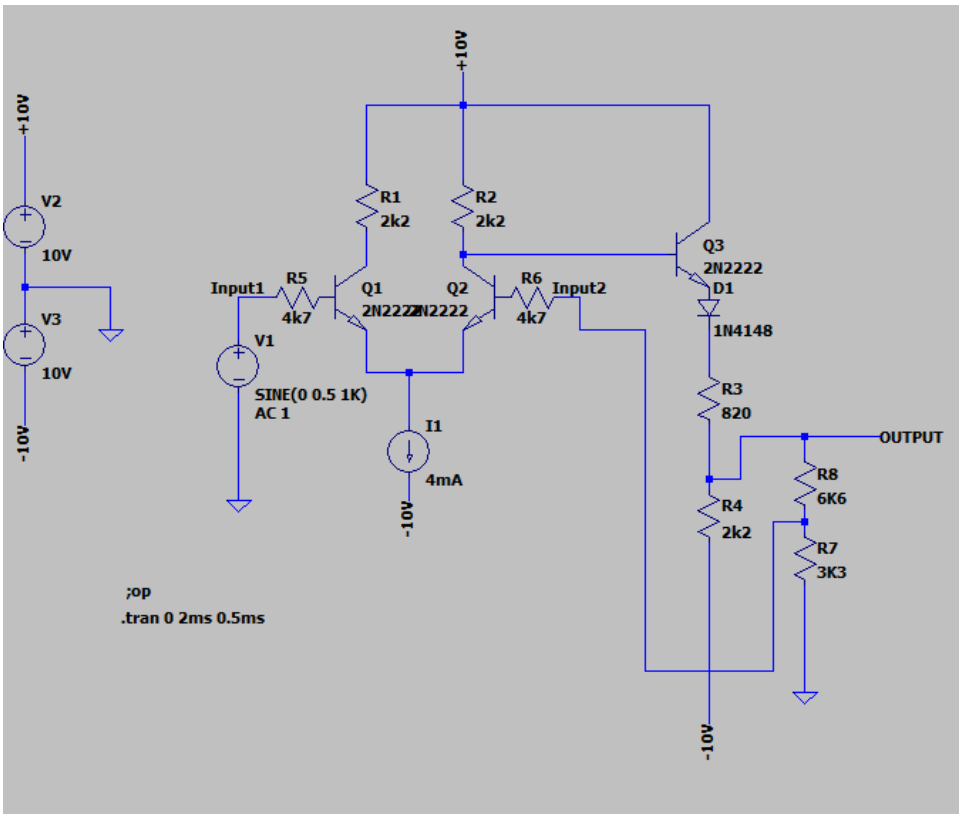
$-A_{vcm}[dB] = 20\,log\left(\frac{V_{OC}}{V_{IC}}\right) = -75.71\,dB$

$-A_{CMRR}[dB] = 26.54 - -75.71 = 102.24\,dB$

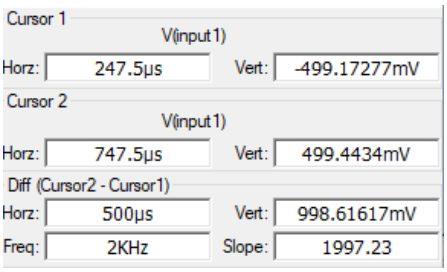
Problem 3: Designing a non-inverting amplifier

1) **Design a non-inverting amplifier using the circuit from problem 2. Calculate the resistance of R1. The gain should become 3. The value of R2 = 3K30Ω.**

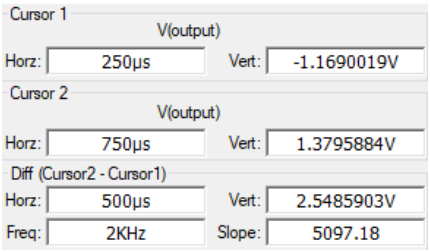
$$A = \frac{R_1 + R_2}{R_2} \rightarrow \quad 3 = \frac{R_1 + 3300}{3300} \rightarrow R_1 = 6600 = 6K60\Omega$$



2) **Use PSpice to simulate your design. Display and measure input and output signal. For Uin use ˆu = 500mV. Determine the gain.**



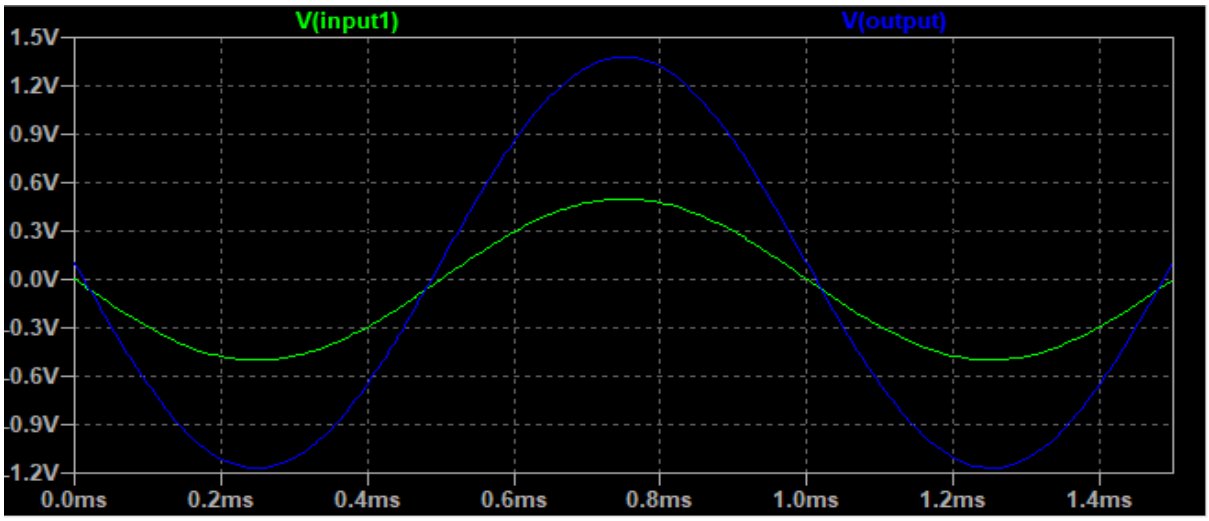
Input



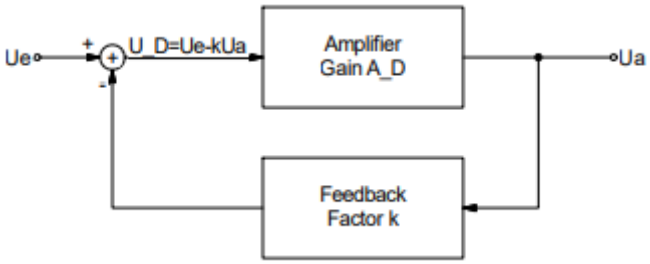
Output

$$A = \frac{V_{out}}{V_{in}} = \frac{2.549}{998.6 \times 10^{-3}} \approx 2.5526$$

3) **What is the reason why the measured gain is smaller than the theoretical gain.**



Hint: Think of the principles of feedback!



From the above diagram we can see obtain the following function:

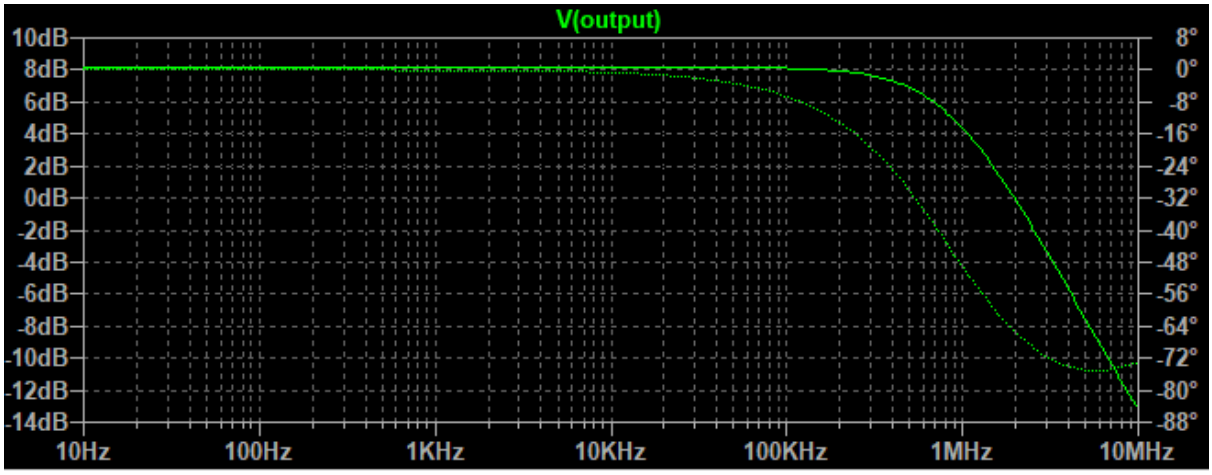
$$U_a = U_D \times A_D = A_D(U_e - kU_a)$$

$$A_D = A_{Vdiff} = 2.5526 \;\&\; k = \frac{1}{3}$$ ~20!!

$$A = \frac{U_a}{U_e} = \frac{A_D}{1 + kA_D} = \frac{2.5526}{1 + \frac{1}{3} * 2.5526} = 1.379$$ ~2.6

This value obtained is comparable to measured one.

4) Plot the gain as a function of frequency (10Hz to 10MHz).



Problem 4: Properties from Data Sheet

	Value from Data Sheet	Our Values
Input Offset Current	30nA	-
Slew Rate	$0.5\mu s$	-
Input Bias Current	100nA	$0.0100225nA$
Input Offset Voltage	5mV	186.334mA
Voltage Gain	$20\log(200000) = 106.021dB$	228.15mV
CMRR	90dB	96.8dB