Jacobs University Bremen

Electronics Laboratory Course
Fall Semester 2020

Lab Experiment: Metal Oxide Field Effect Transistor

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Place of execution : Teaching Lab EE

Introduction:

The few main objects of this experiments were:

- To become familiar the characteristics and applications of Field Effect Transistors (MOSFETs)
- Investigation of the I-V characteristics and the implementation of MOSFETs as amplifiers and switches.

The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). BJTs based circuits dominated the electronics market in the 1960's and 1970's. Nowadays most electronic circuits, particularly integrated circuits (ICs), are made of MOSFETs. The BJTs are mainly used for specific applications like analog circuits (e.g. amplifiers), high-speed circuits or power electronics.
There are two main differences between BJTs and FETs. The first is that FETs are charge-controlled devices while BJTs are current or voltage controlled devices. The second difference is that the input impedance of the FETs is very high while that of BJT is relatively low.
As for the FET transistors, there are two main types: the junction field-effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET based circuit would be simply too high. MOSFETs became the most popular field effect device in the 1980's. The combination of n-type and p-type MOSFETs allow for the realization of the Complementary Metal Oxide Semiconductor (CMOS) technology, which is nowadays the most important technology in electronics. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors on a single chip. In this experiment, we will concentrate on the MOSFET transistor. We will investigate its characteristics and study it's behaviour when used as an amplifier or a switch.

8.2 Prelab Field Effect Transistor

8.2.1 Problem 1: Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

1. Explain the differences between an enhanced and depletion MOSFET.

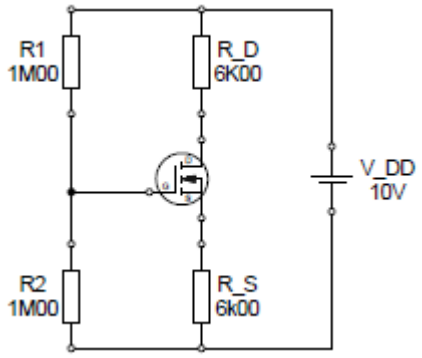
An enhanced MOSFET is a normally off device. It does not conduct when $V_{GS} = 0$ because it normally does not have a channel to conduct but one can be induced by applying a sufficiently large V_{DS} matching the polarity of the base. This creates a depletion region and when there are enough free carriers to connect the source and drain terminals of the MOSFET, a current can flow.

However, a depletion MOSFET has the channel allowing it to conduct when $V_{GS} = 0$. This channel is a thin layer of doped silicon of the same type as the drain and the source which connects terminals and creates a depletion zone. In both cases, when both devices are in the ON state, their conductance can be modified by varying the applied V_{DS} of the right bias, up to the pinch off.

2. Explain the differences between an NMOS and PMOS transistor.

In NMOS transistor, the drain and the source terminals are made from an N-type material and are collocated on a P-type base. While for the PMOS transistors, the terminals are P-type and the base is N-type. This makes it such that NMOS transistor needs a positively biased gate to source voltage, while the PMOS needs a negatively biased gate to source voltage.

8.2.2 Problem 2: MOSFET as Amplifier



$$I_{DS} = \mu_n C_G \frac{W}{2L}(V_{GS} - V_{th})^2 = k * (V_{GS} - V_{th})^2$$

Pre-factor k is given by $k = \frac{0.5mA}{V^2}$,$V_{th} = 1V$

1. Determine the gate-source and drain-source voltage and the drain current for the MOSFET amplifier.

From the circuit we can see that the V_G is defined by the voltage divider circuit where:

$$V_G = \frac{R2}{R1 + R2} V_{DD} = \frac{1 \times 10^6 \Omega}{1 \times 10^6 \Omega + 1 \times 10^6 \Omega} 10V = 5V$$

Then from the given equation above we can see that:

$$I_{DS} = k * (V_{GS} - V_{TH})^2$$

$$I_{DS} = k * (V_G - V_S - V_{TH})^2$$

$$I_{DS} = 0.5 \times 10^{-3}(4 - V_S)^2 \quad (i)$$

But from the circuit and saying that $I_D = I_S$ we can say that:

$$V_S = R_S * I_D$$

Replacing (i) in the equation:

$$V_S = 6000 * 0.5 * 10^{-3}(4 - V_S)^2$$

$$V_S = 3(16 - 8V_S + V_S^2)$$

$$V_S = 48 - 24V_S + 3V_S^2$$

$$48 - 25V_S + 3V_S^2 = 0$$

Two values of V_S:

$$V_{S1} = 5.333\ V$$

$$V_{S2} = 3V$$

As $I_D = I_S$ and $R_S = R_D$ then this means that $V_S = V_D$.

For the first case V_{S1}we can say that that if we try to computer V_{DS} we will see that it will be negative which makes no -sense this case. So, the value of $V_S = 3V$.

Finding V_{GS} and V_{DS}

$$V_{GS} = V_G - V_S = 5 - 3 = 2V$$

$$V_{DS} = V_{DD} - V_S - V_D = 10 - 3 - 3 = 4V$$

To find drain current I_D we have at the $V_S = I_D * R_S$

$$I_D = \frac{V_S}{R_S} = \frac{3V}{6 * 10^3\Omega} = 0.5mA$$

$$I_{D2} = \frac{V_S}{R_S} = \frac{5.333V}{6 * 10^3\Omega} = 0.8889mA$$

2. Show that the MOSFET indeed operates in the saturation region.

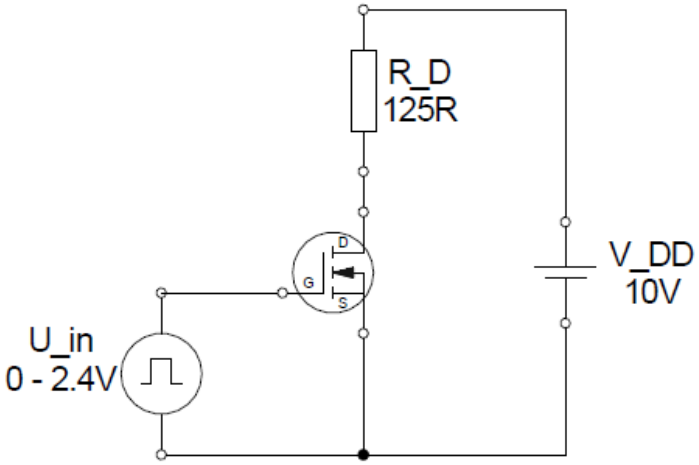
To show that the MOSFET is in the saturation region and operating we show that

$\rightarrow V_{DS} \geq V_{GS} - V_{TH} \longrightarrow 4V \geq 2V - 1V \longrightarrow 4V \geq 1V$

Hence MOSFET is in saturation region and hence operates in saturation region.

8.2.3 Problem 3: MOSFET as Switch

1. Determine the operating points of the MOSFET circuit shown.



The transistor works with two different V_{GS} values

When $V_{GS} = 2.4V$

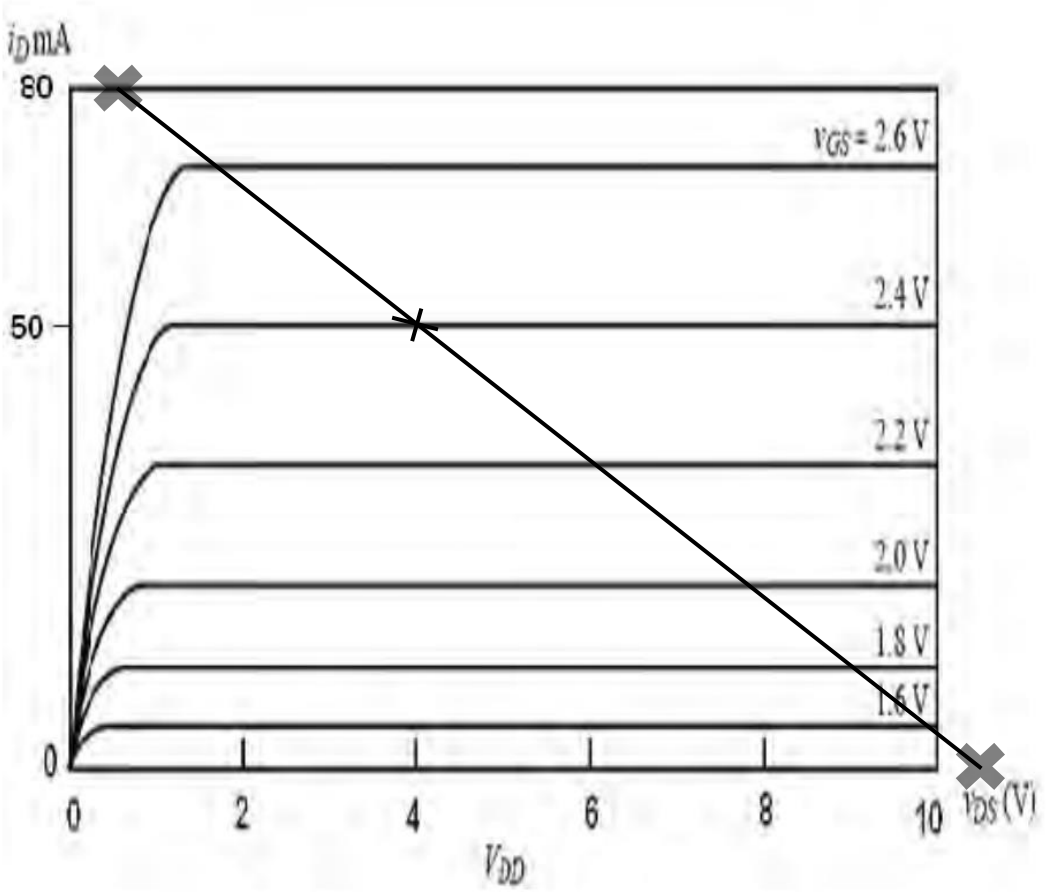
In this case, $V_{DS} = 0$ where we get that $I_{DS} = \frac{V_{DD}}{R_D} = \frac{10V}{125\Omega} = 0.08A = 80mA$

When $V_{GS} = 0$

In this case, $I_{DS} = 0$ therefore $V_{DS} = V_{DD} = 10V$

Now we have two coordinates from the graph which are **(**10V,0) and (0, 80mV)

We draw a straight line through these points and slope of this line is $\frac{1}{R_D}$. The line passes through a point which is the operating point where $I_D = 50mA \; and \; V_D = 3.6V$(**quiescent** point)



Execution & Evaluation

Workbench No. 11

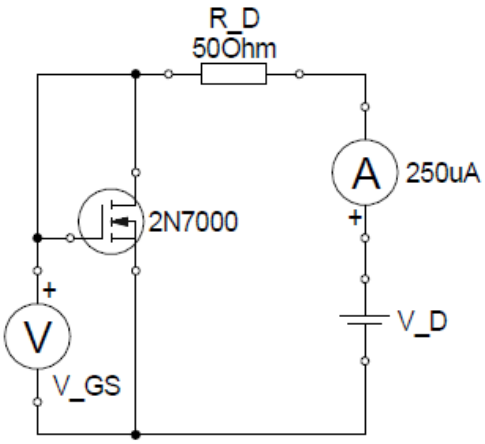
Instruments and tools used:

- Breadboard
- Function Generator/oscilloscope
- Resistors
- Capacitor
- Wires
- 2N7000 MOSFET Transistor
- CD40007 integrated circuit

8.3.1 Problem 1: Current/Voltage Characteristic of a MOSFET

The purpose of this problem is to measure the current/voltage characteristics of a NMOS Field Effect Transistor.

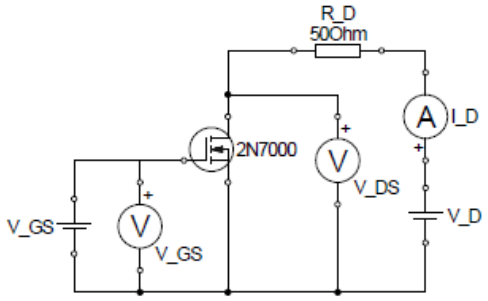
1. Use the following circuit to determine U_{th}.



Uth = UGS = UDS when ID = 250_A. Measure and record Uth and ID.

$U_{th}(V)$	$I_D(uA)$
2.041	244.9

2. Use the following circuit to measure the transfer characteristic.



The gate source voltage should be scanned from 0V to 3V. Ensure that the drain voltage source U_{DS} is kept constant at 5V while changing U_{GS}

V_{DS}	V_{GS}	I_{DS}
5.006	0.0	0.0000003
5.006	0.5	0.0000003
5.006	1.0	0.0000003
5.006	1.5	0.0000004
4.990	2.0	0.0001078
5.003	2.2	0.0029
5.003	2.4	0.0107
5.006	2.5	0.0184
4.996	2.7	0.0356
4.999	3.0	0.0749

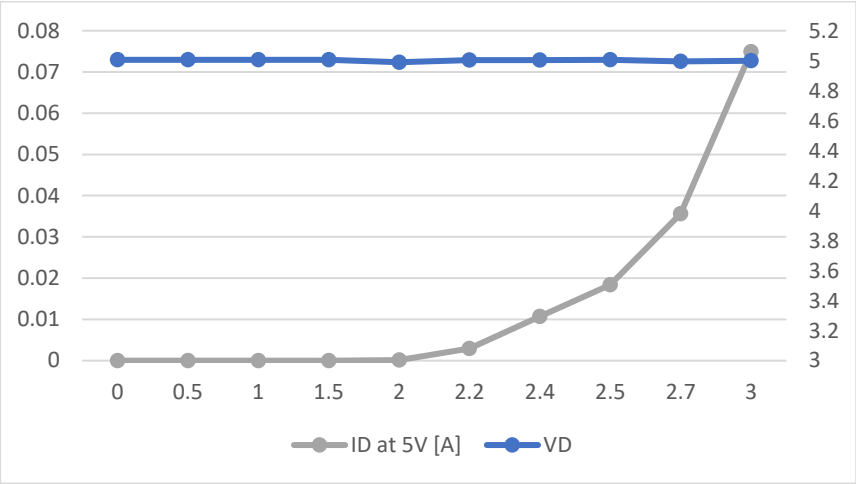
3. Use the circuit from before and measure the output characteristic for gate source voltages of 2V , 2:2V , 2:4V , and 2:6V . The drain source voltage should be scanned from 0V to 4V .
(Recordings Take From Mohammed Mahfoud)

$V_{GS} = 2V$		$V_{GS} = 2.2V$		$V_{GS} = 2.4V$		$V_{GS} = 2.6V$	
$V_{DS}(V)$	$I_{DS}(A)$	$V_{DS}(V)$	$I_{DS}(A)$	$V_{DS}(V)$	$I_{DS}(A)$	$V_{DS}(V)$	$I_{DS}(A)$
0.004	0.0000212	0.00	0.0000438	0	0.0000502	0	0.0000583
0.509	0.000181	0.506	0.000017	0.522	0.0073	0.525	0.0116
0.994	0.00015	1.013	0.0000186	1.016	0.00966	1.016	0.0129
2.004	0.00015	1.495	0.00189	1.507	0.0131	1.538	0.0161
		2.00	0.00192	2.014	0.0167	2.017	0.0197
		2.518	0.00195	2.506	0.0205	2.509	0.0234
		3.08	0.0000198	3.001	0.0244	3.002	0.0273
		3.506	0.00201	3.5	0.0285	3.496	0.0313

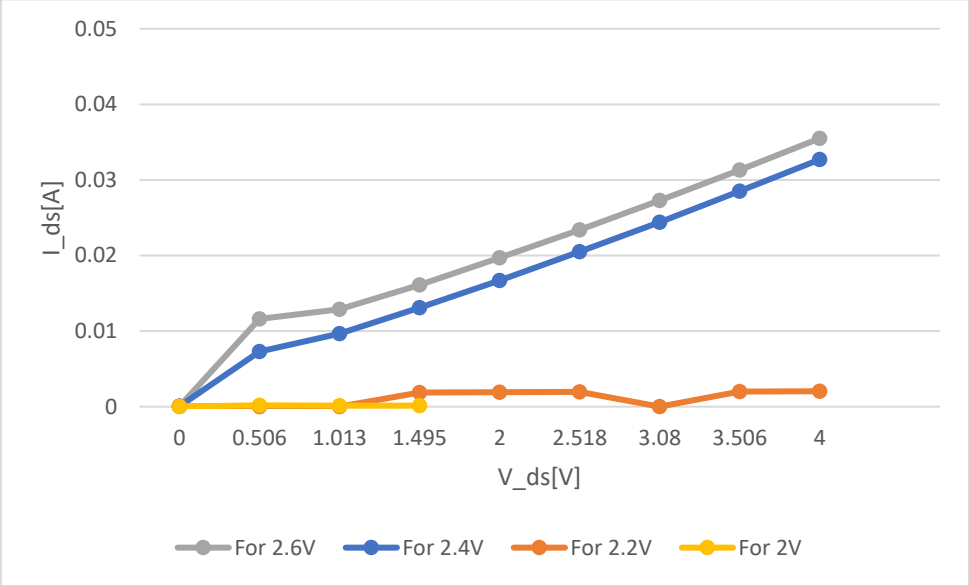
		4.00	0.00204	4.007	0.0327	3.997	0.0355

Evaluation:

1. Plot the measured transfer characteristic.



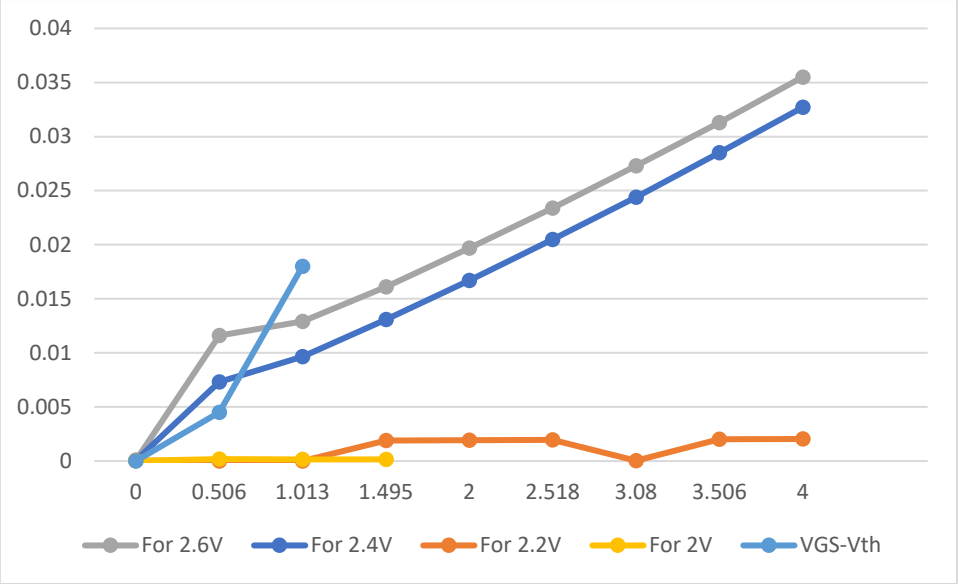
2. Plot the measured output characteristic for the different gate source voltages.



An almost linear behavious can be observed in values VGS of 2.4V and 2.6V. This can be attributed to the effects of the components heating up because the increased applied voltage.In order to obtained desired behaviuor one must take measurements quickly. This is a methodical error.

For the first few values taken past pinch off, the expected behavior of an almost horizontal line can be observed in graphs for VGS=2V and VGS=2.2V

3. Insert the VDS = VGS - Vth line into the output characteristic.

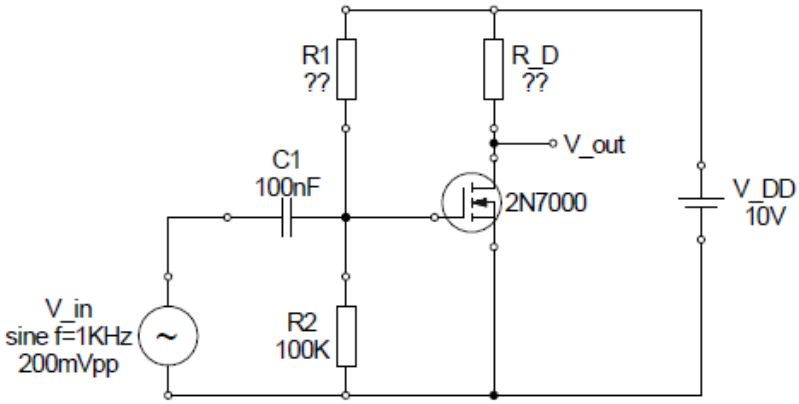


When connecting wires at the pinch off all the cureves, aline with behavior pf a parabola can be observed which is predicted from the equation discussed in lab.

8.3.2 Problem 2: MOSFET as Amplifier

Goal of the problem is to design and realize an amplifier circuit using a MOSFET.

1. We want to use the following circuit



$V_{GS} = 2.7V$, $V_{DS} = 5V$, $k = 72.2mA/V^2$, U_{th} = use measured value!

Determine the values for R1 and RD.

$$V_{GS} = 2.7V = \frac{R2 * V_D}{R2 + R1}$$

Making R1 the subject of the formula, where V_D = 10 and R2=100K Ω we obtain

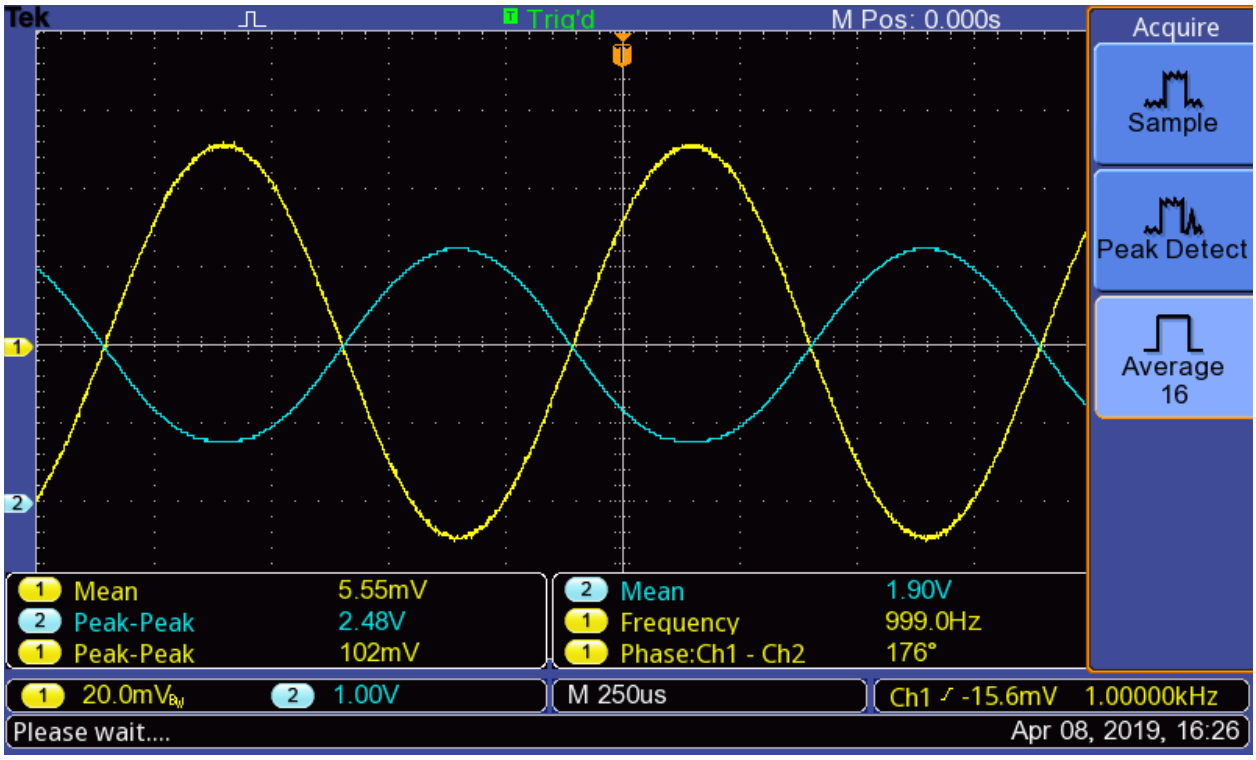
$$2.7(100000 - R1) = 1000000$$
$$270000 + 2.7R1 = 1000000$$
$$R1 = 270.370K\Omega$$

For R_D

$$I_D = k(U_{GS} - U_{th})^2 \; and \; R_D = \frac{U_{RD}}{I_D}$$
$$substituting \; I_D \; gives = R_D = \frac{U_{RD}}{k(U_{GS} - U_{th})^2} = \frac{5}{\frac{72mA}{V^2(2.7V - 2.041V)^2}} = 159.9\Omega$$

Therefore we used 220 Ohm which was better.

2,3,4. Take hard copies showing the input and the output signals and the phase relation between them.



Evaluation:

1. In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.

The amplifier works only in the saturation of the MOSFET, this is because it is desired for all the possible range of input voltages to be amplified by the same amount. Since in this mode of the MOSFET we have a source-drain current which is independent of the source-drain voltage and

instead we have the gate-source voltage. Therefore, we will obtain a current source which is voltage-controlled.

2. If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.

In order to stay inside the active region, we need to take care to stay between the triode and cutoff regions. It is known that the minimum VDS to stay in active region is $V_{DSmin} = V_{GS} - V_{TH}$ and at the same time one must be lying in the load line $V_{DS} = V_{DD} - I_D R_D$ and $I_D = k.(V_{DS})^2$in the triode region.

$$\frac{k * (V_{DS})^2 * R_D}{2} + V_{DS} - V_{DD} = 0$$

$$V_{DSmin1} = -1.03353\,; V_{DSmin2} = 0.85649$$

The negative solution is discarded. Now, in order to stay out of the cutoff zone, VDS<VDD. Meaning that from the quiescent point VDSQ=5, it can swing 4.14V in the negative direction and 5V in the positive. Since we are thinking of waves with symmetric maxima and minima, the maximum amplitude would be Amax=4.14. From the hardcopy, we can see that the gain is $\frac{2.48}{0.102} = 24.313$

From which we can take maximum input amplitude.

$V_{in} = \frac{V_{out}}{Gain}$=170mV giving maximum point of 340.5mV

3. Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.

$$V_{out} = V_{DS} \quad \& \quad V_{in} = V_{GS}$$
$$\rightarrow V_{out} = V_{DS} = V_{DD} - I_D \times R_D \quad \& \quad I_D = k(V_{GS} - V_{th})^2$$
$$\rightarrow V_{out} = V_{DD} - kk(V_{GS} - V_{th})^2 \times R_D$$
$$\rightarrow g(V_{in}) = \frac{dV_{out}}{dV_{in}} = 2 \times k \times R_D(V_{GS} - V_{th})$$

The assumptions here is that the DC bias signal that may be observed is ignored and the slope of the equation is what gives us the relationship between the input and output. In addition, we observe that the gain is dependent on V_{GS}.

4.*Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.*

The gain could be written as $Gain = -g_m R_D \frac{R1||R_2}{R1||R_2} = -g_m R_D$

Where $gm = \frac{\partial I\_D}{\partial V_{GS}} = \frac{\partial (k*(V_{GS}-V_{th})^2)}{\partial V_{GS}} = 2k * (V_{GS} - V_{th}) = 95\,\frac{mA}{V}$

Therefore Gain: $R_D * -g_m = 159.9 * -0.09515 = -15.22$

The observed negative sign in the calculated gain reflects the phase difference of 18 that is present in the hard copies. The reason for this sign not to be reflected in the measured gain is because that value was calculated disregarding phase by just taking peak values of two signals.

5. Explain the phase relation between the input and the output.

In the hardcopy that was taken, we observe that we have a phase difference of approximately 180°, this property is visible due to the properties of the transistor. The first explanation is that the gain is negative meaning that the output sign will change, thus causing the 180-degree shift to be visible. In addition, we know when the input signal is increased then the drain source current is increased, and the result will be a voltage drop over R_D which is bigger and thus leaving V_{DS} to be smaller → keeping in mind that $V_{DS} = V_{DD} - R_D \times I_D$. Therefore, this is the second reason why we may observe this shift.

Conclusion:

Throughout this experiment the main goal was to focus on the use and properties of a MOSFET. It is important for us to keep in mind that is one of the most used transistors, and its FET part signifies the fact that is charged, however if we compare it to what we previously studied, BJT, is it current or voltage controlled. Therefore, in this case we are able to see a different transistors property and explore how it works. We mostly worked on the NMOS enhancement types of a MOSFET, where we firstly explored its main properties by making different measurements on the drain-source current and by changing and recording values of the drain source and gate source voltages. Once we plotted these results, we were able to obtain an idea of the saturation mode and its dependence on the voltages. Later on, we were able to use the MOSFET as an amplifier as we where we focused on using it in the saturation range. At the end of the experiment we faced some accuracy issues when it came to peak to peak voltages and choosing which resistor to use in order to obtain a somewhat accurate solution. It was due to resolution of instruments used and the internal errors they possess.

References:

Lab Manual

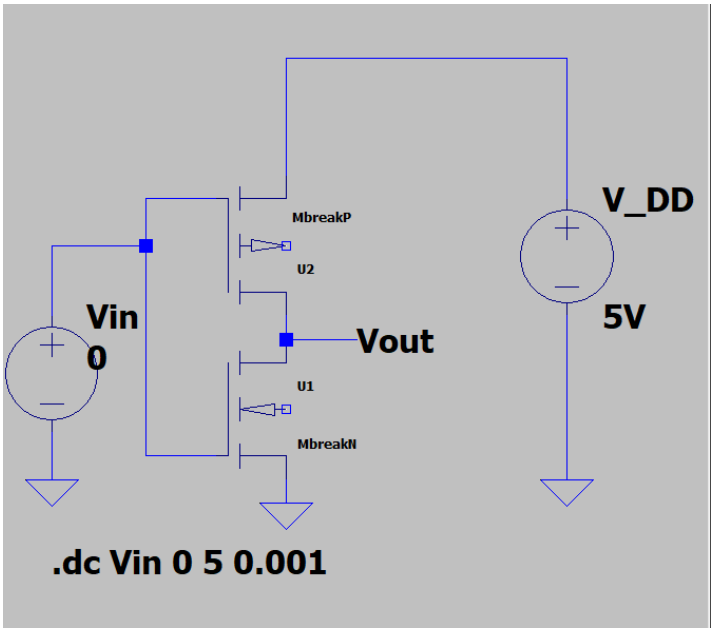
Signal Diode Data Sheet

Appendix:

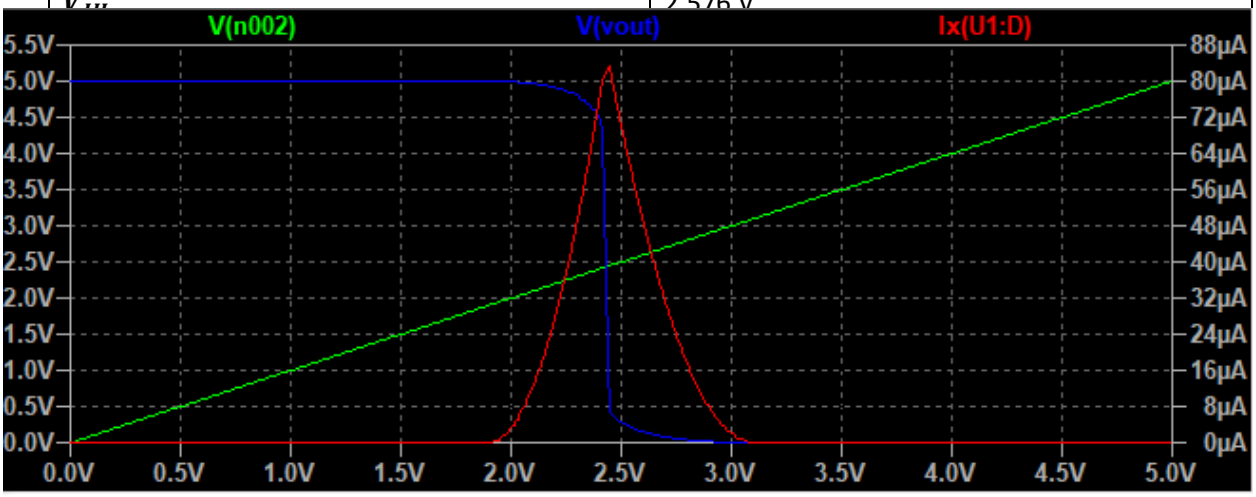
Prelab of CMOS Inverters and Logic Gates:

Problem 1: Voltage Transfer Characteristic of a CMOS

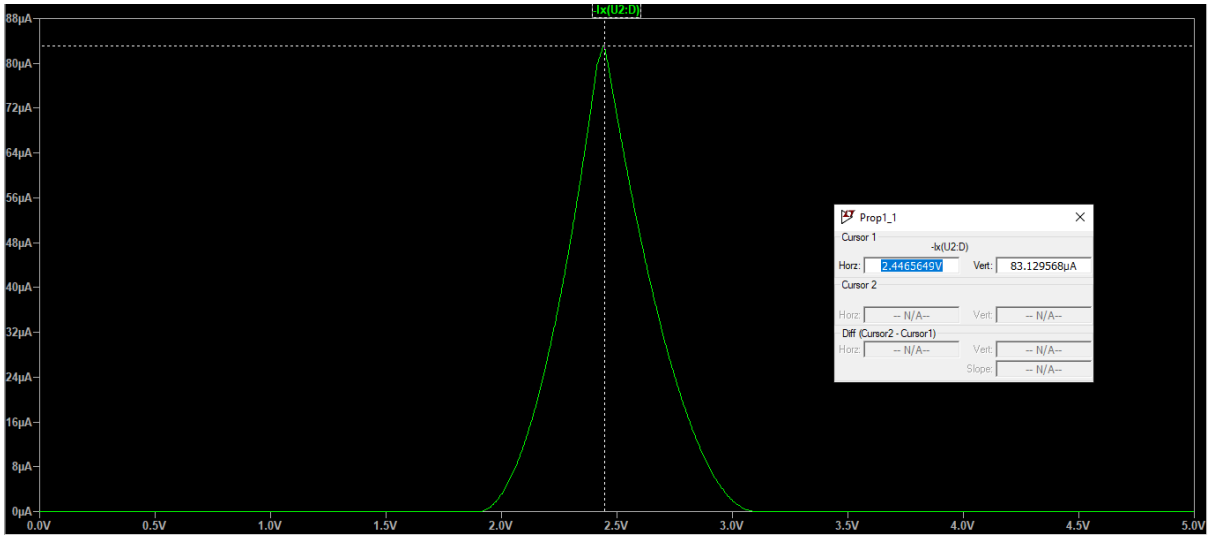
1. Use 5V for the power supply VDD. Simulate the voltage transfer curve (VTC) of the CMOS inverter and extract the values of VOH, VOL, VIH, VIL, NML, NMH, and Vth. Hint: Use the d() function of LTSpice to determine VIH, VIL!!



Name	Value
V_{OH}	4.872 V
V_{OL}	160.394 mV
V_{IH}	2.576 V



2. Simulate the current flowing through the inverter as a function of the input voltage.

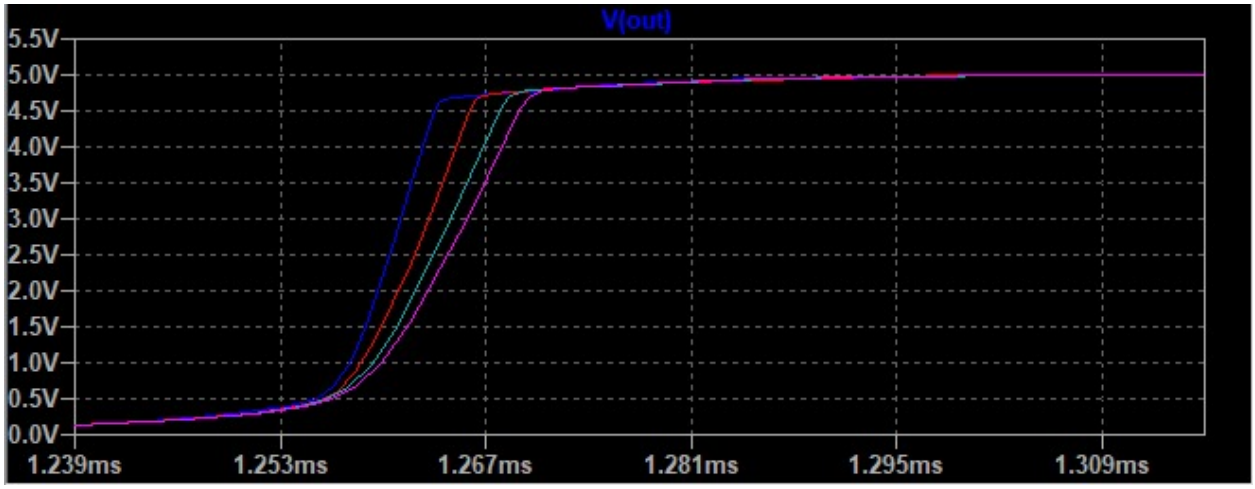


3. For what input level the current reaches its maximum. Provide an explanation.

The current reaches its maximum value with an input of 2.446V. This value assimilates the one obtained previously for Vth=2.431V. This is because at Vth both MOSFETs are in the on state, specifically in the saturation region. This creates an equilibrium point where the current is maximized. At this value the dissipated power is also maximized.

Problem 2: CMOS Inverter with Capacitive Load

1. The capacitive load should be varied from 25pF to 100pF in 25pF steps. Determine the propagation delay (tP LH = tP HL) if the input signal is given by a 1KHz square wave with a 20ns rise and fall time. Use 5V for the power supply VDD.



Using the cursor at Vdd/2 we obtain

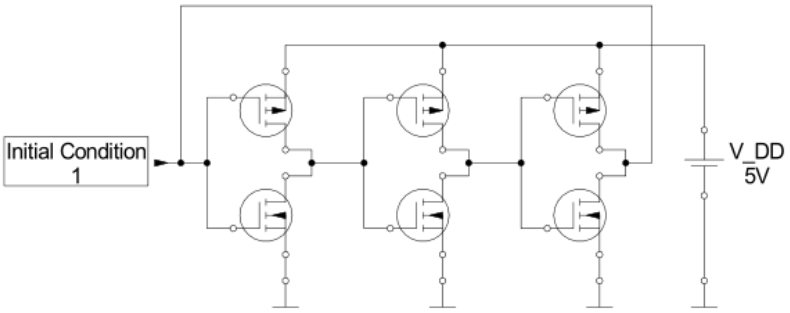
Capacitance/pF	$t_{PLH} = t_{PLH}/ns$
25	46.8
50	63.6
75	83.7
100	108.5

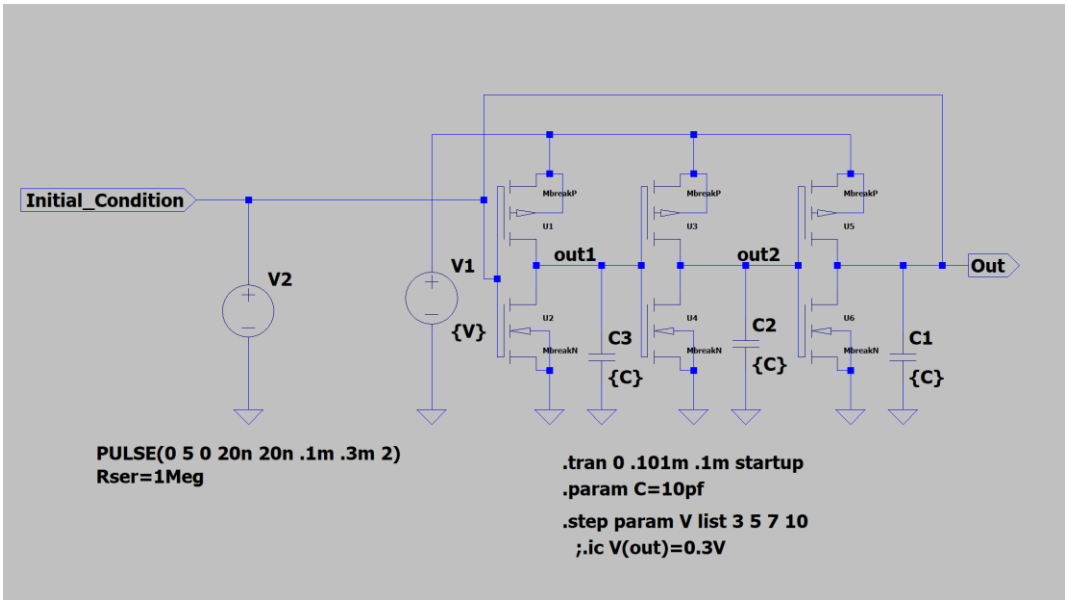
2. Obtain the dynamic power dissipation of the CMOS inverter for the different load capacitors.

The dynamic power dissipation is given by : $P_D = f * C * V_{DD}^2$

Capacitance/pF	DPD/W
25	6.25×10^{-7}
50	$1.25 * 10^{-6}$
75	$1.875 * 10^{-6}$
100	$2.5 * 10^{-6}$

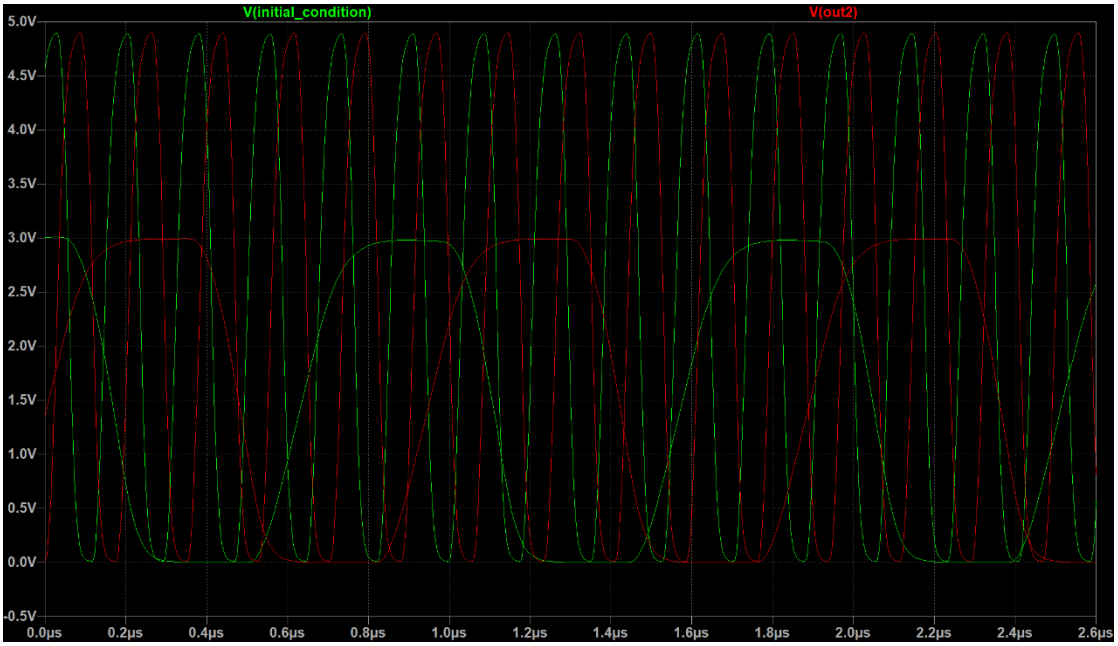
Problem 3: Propagation Delay of an Inverter Stage(Reference From Sheikh Usman Ali)



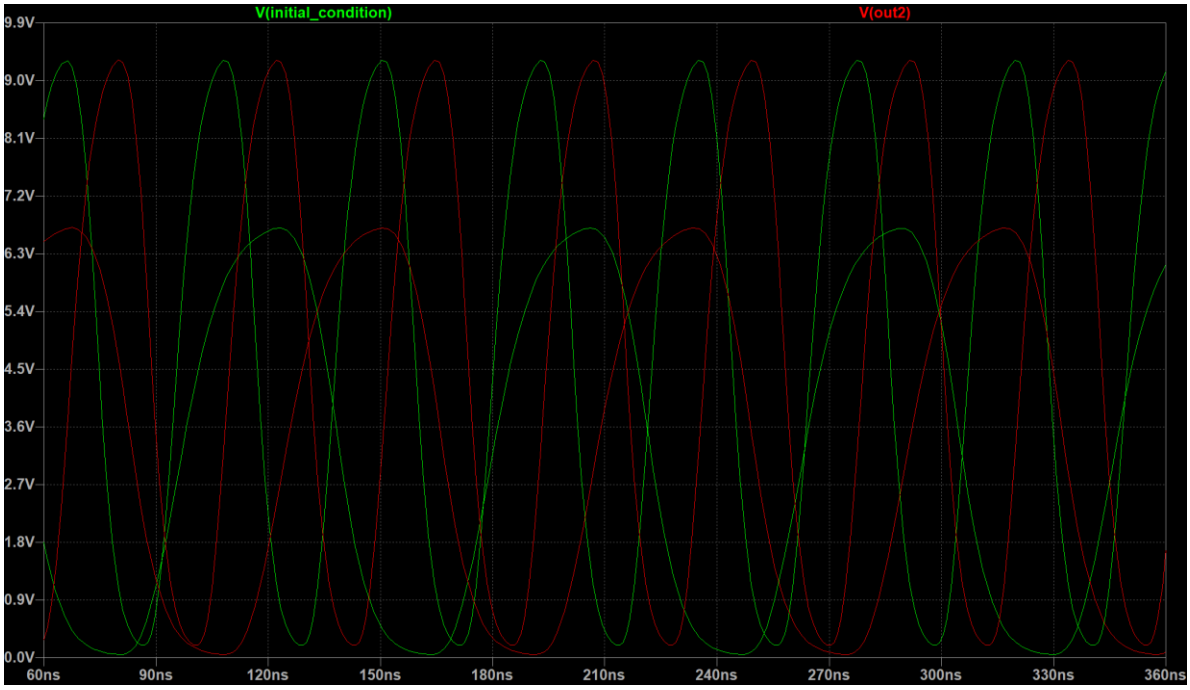


1. Determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of $3V$, $5V$, $7V$ and $10V$, respectively.
   Note: It might be necessary to apply a single pulse to the input of the ring oscillator to start it!

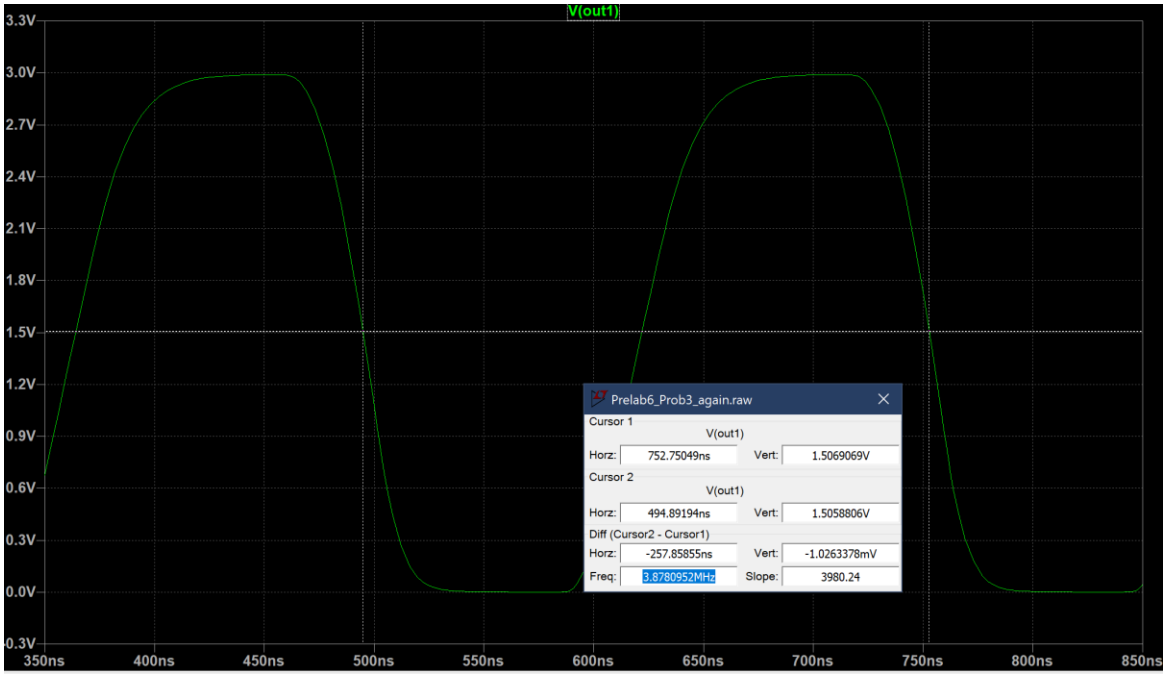
3 and 5V:



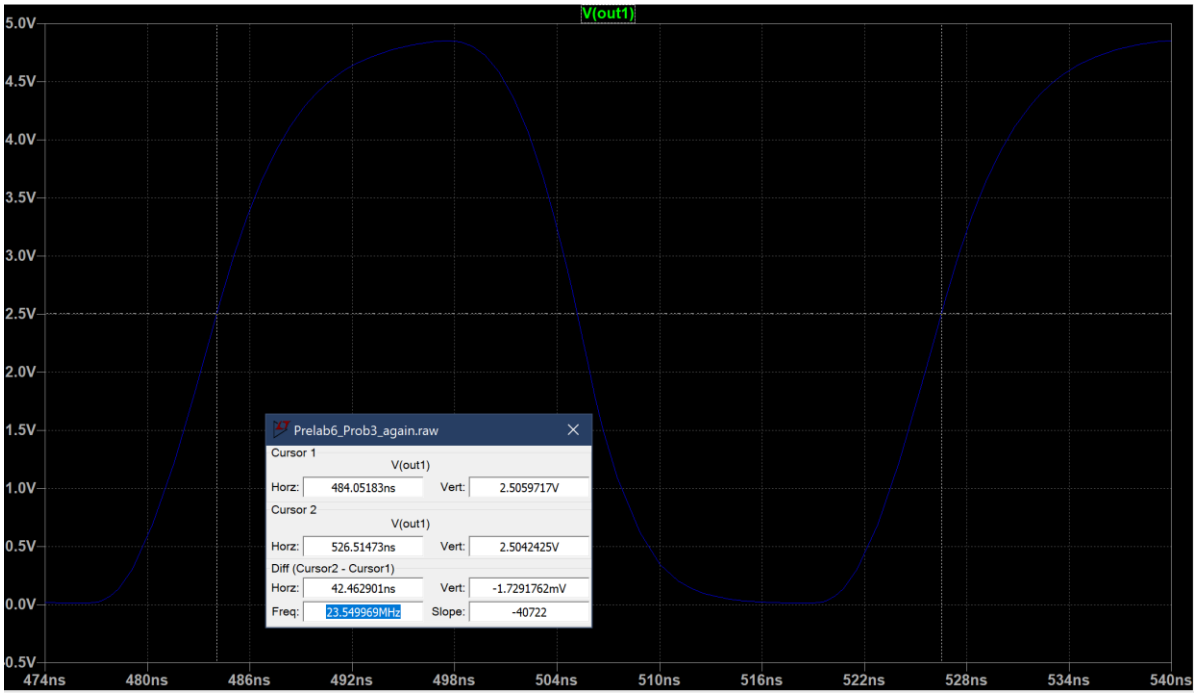
7 and 10V:



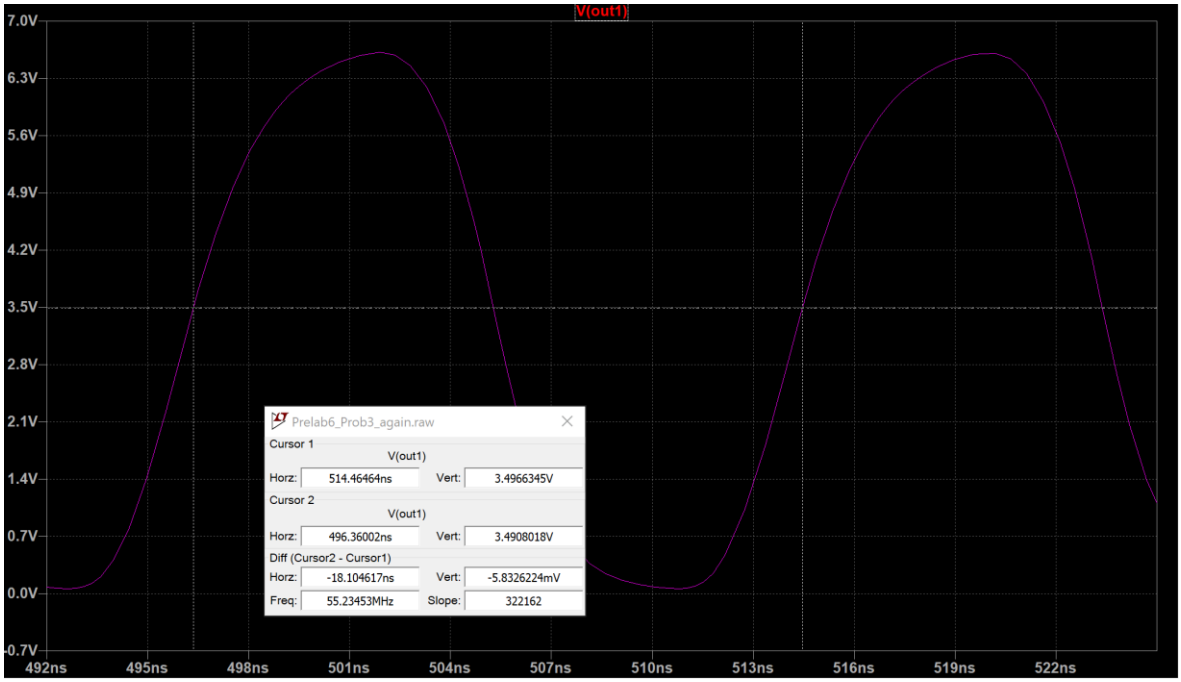
3V:


V(out1)
3.3V
3.0V
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
-0.3V
350ns
400ns
450ns
500ns
550ns
600ns
650ns
700ns
750ns
800ns
850ns
Prelab6_Prob3_again.raw
Cursor 1
V(out1)
Horz: 752.75049ns
Vert: 1.5069069V
Cursor 2
V(out1)
Horz: 494.89194ns
Vert: 1.5058806V
Diff (Cursor2 - Cursor1)
Horz: -257.85855ns
Vert: -1.0263378mV
Freq: 3.8780952MHz
Slope: 3980.24

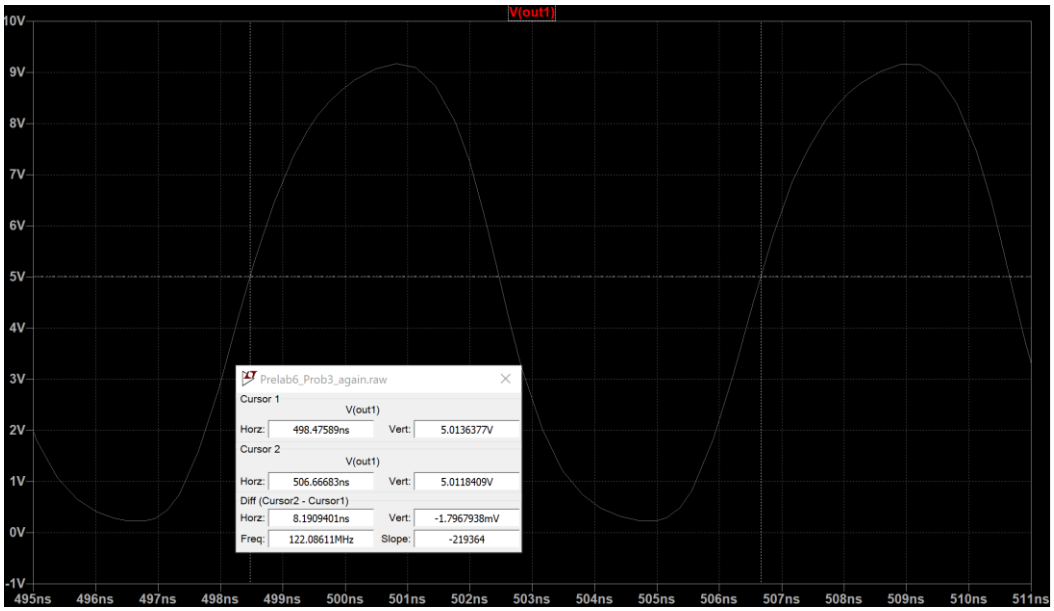
5V:


V(out1)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
474ns
480ns
486ns
492ns
498ns
504ns
510ns
516ns
522ns
528ns
534ns
540ns
Prelab6_Prob3_again.raw
Cursor 1
V(out1)
Horz: 484.05183ns
Vert: 2.5059717V
Cursor 2
V(out1)
Horz: 526.51473ns
Vert: 2.5042425V
Diff (Cursor2 - Cursor1)
Horz: 42.462901ns
Vert: -1.7291762mV
Freq: 23.549969MHz
Slope: -40722

7V:


V(out1)
7.0V
6.3V
5.6V
4.9V
4.2V
3.5V
2.8V
2.1V
1.4V
0.7V
0.0V
-0.7V
492ns
495ns
498ns
501ns
504ns
507ns
510ns
513ns
516ns
519ns
522ns
Prelab6_Prob3_again.raw
Cursor 1
V(out1)
Horz: 514.46464ns
Vert: 3.4966345V
Cursor 2
V(out1)
Horz: 496.36002ns
Vert: 3.4908018V
Diff (Cursor2 - Cursor1)
Horz: -18.104617ns
Vert: -5.8326224mV
Freq: 55.23453MHz
Slope: 322162

10V:


V(out1)
10V
9V
8V
7V
6V
5V
4V
3V
2V
1V
0V
-1V
495ns
496ns
497ns
498ns
499ns
500ns
501ns
502ns
503ns
504ns
505ns
506ns
507ns
508ns
509ns
510ns
511ns
Prelab6_Prob3_again.raw
Cursor 1
V(out1)
Horz: 498.47589ns
Vert: 5.0136377V
Cursor 2
V(out1)
Horz: 506.66683ns
Vert: 5.0118409V
Diff (Cursor2 - Cursor1)
Horz: 8.1909401ns
Vert: -1.7967938mV
Freq: 122.08611MHz
Slope: -219364

2. Calculate the dynamic power dissipation per inverter stage for the different supply voltages.

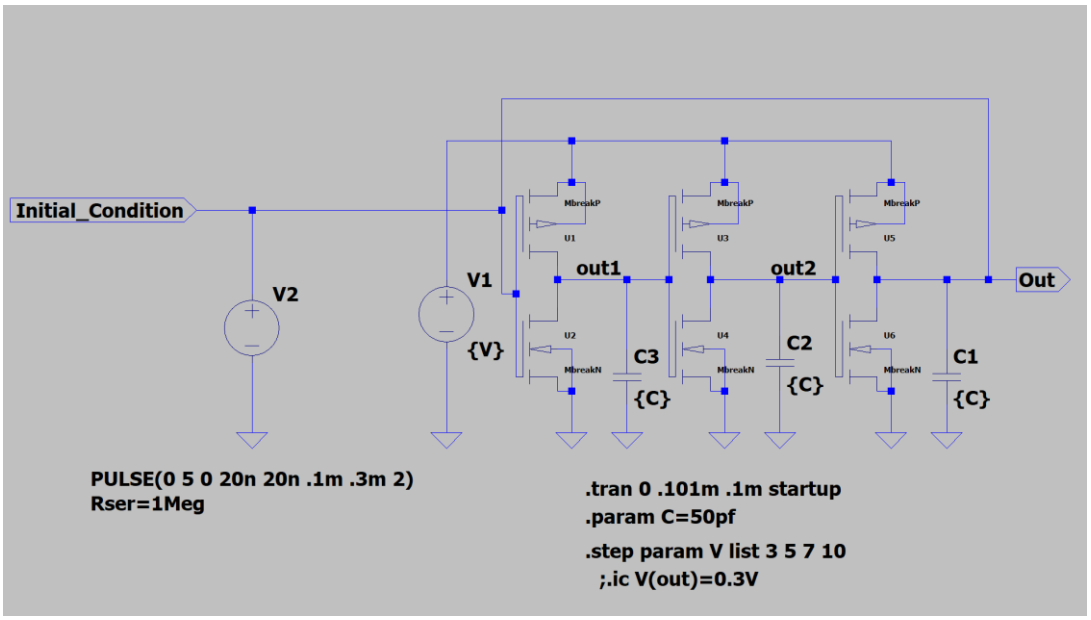
$P = fCV_{DD}^2$ using C=10pF

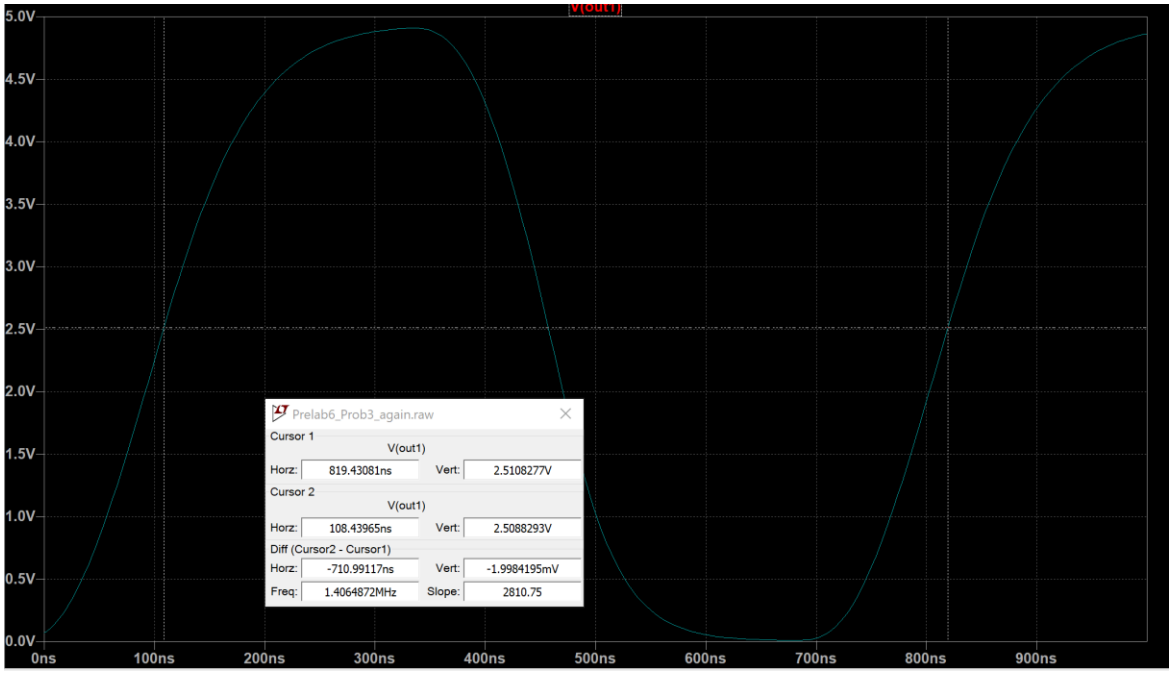
V_{DD}/V	f/MHz	tPLH/ns	tPHL/ns	P/W
3	3.87	41.60	43.77	3.483E-4
5	23.55	7.2058	6.924	5.8875E-3
7	55.23	3.135	2.864	0.02706
10	122.08	1.4788	1.2324	0.12208

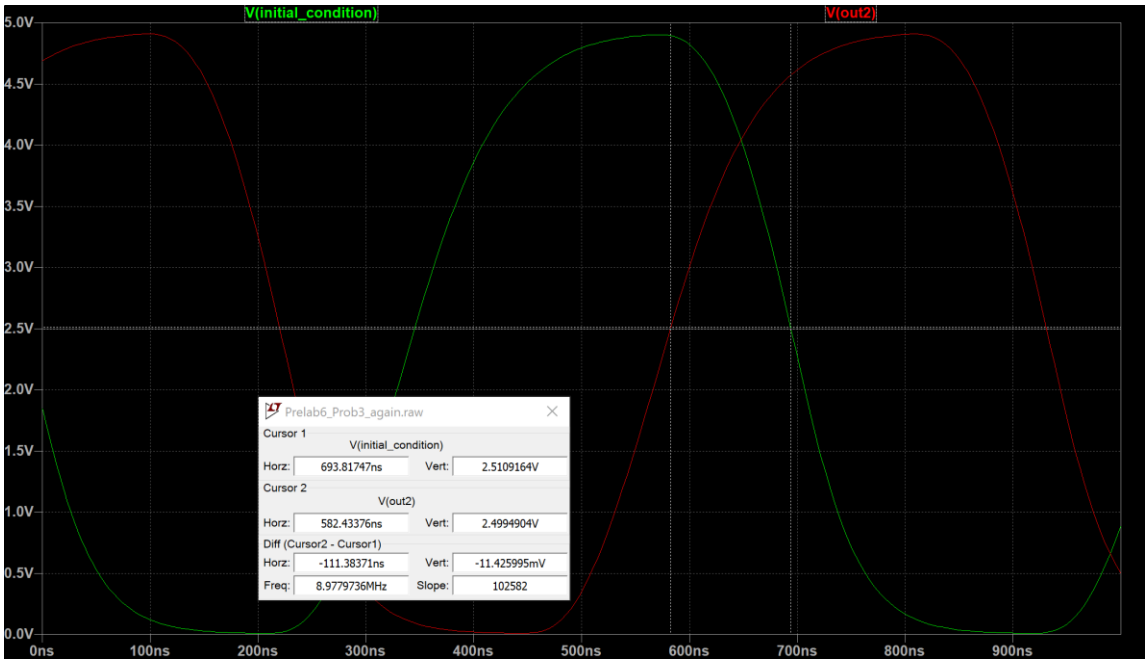
3. Add a $50pF$ load capacitor to each inverter of the 3-stage ring oscillator and measure the oscillation frequency and determine the propagation delay per inverter for a power supply of $V_{DD} = 5.0V$

$P = fCV_{DD}^2$ using C=50pF

V_{DD}	f/MHz	tPLH/ns	tPHL/ns	P/W
5	1.40687	126.10402	111.87439	1.7585E-3







What is the effect of the capacitive load on the propagation delay and the oscillation frequency?

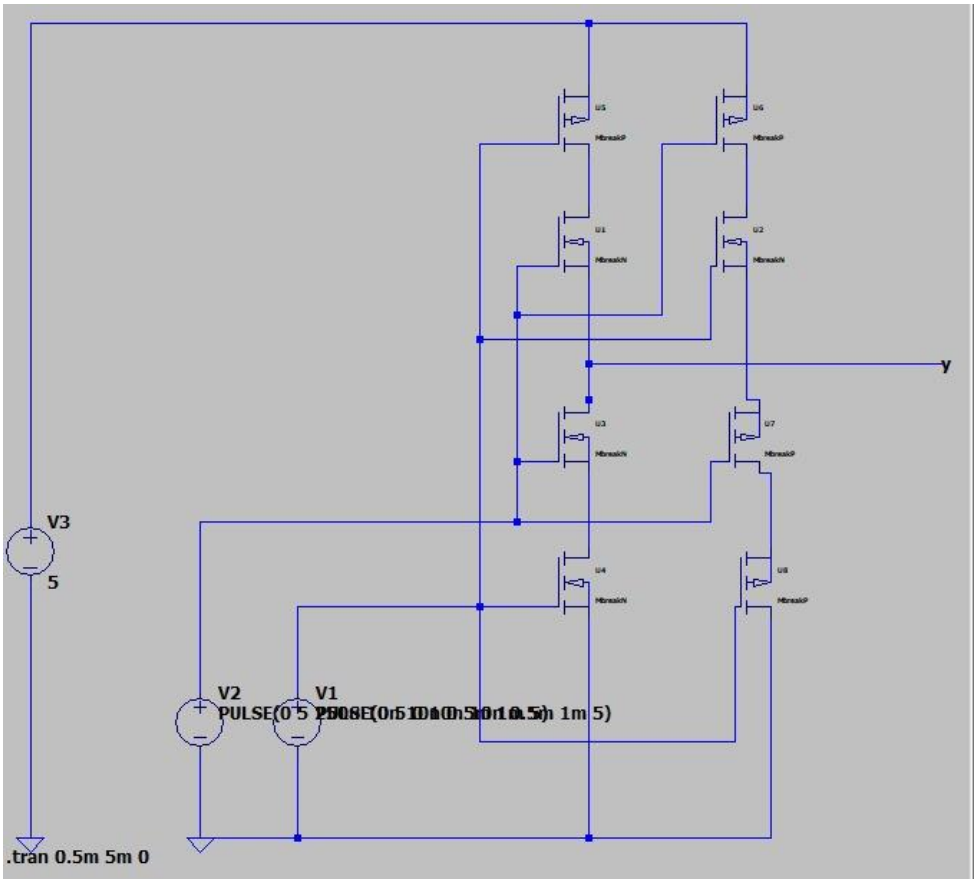
The capacitive load increases resulting a higher RC constant, which means we have reduced speed. Then, the frequency decreases and the propagation delay times are longer. It is due to discharge time of capacitor.

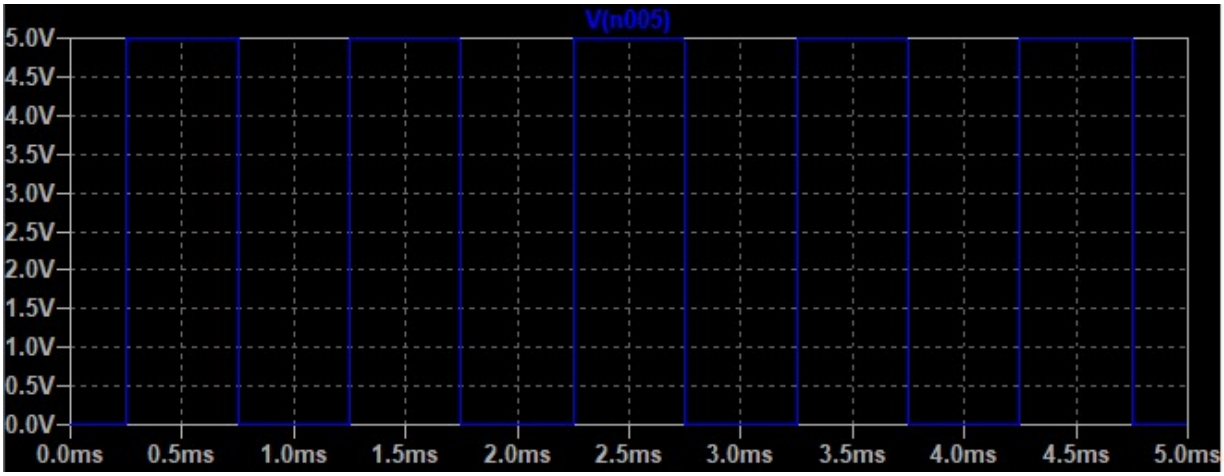
What is the effect of the capacitive load and the power supply on the power dissipation?

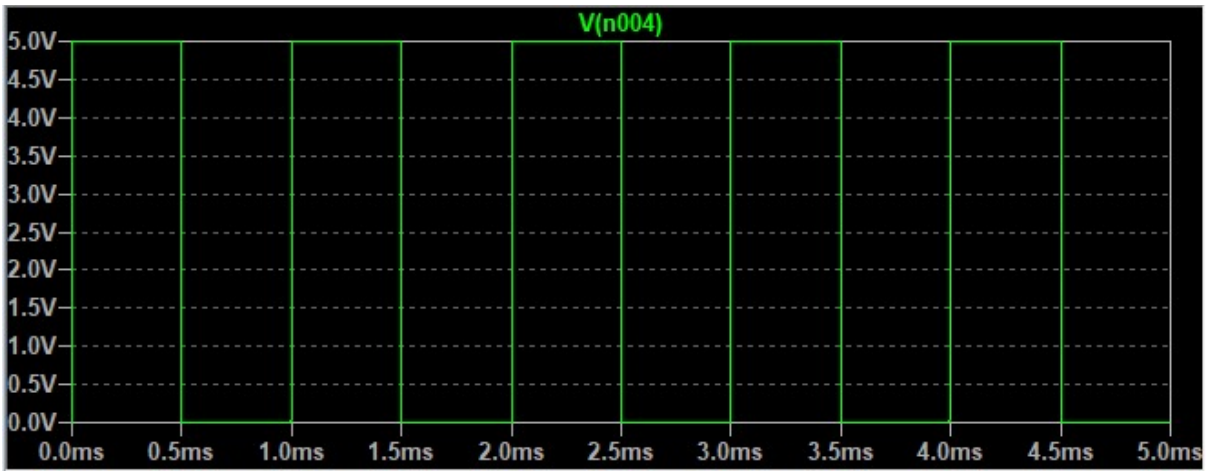
There is a decrease in power dissipation because the frequency of oscillation is greatly decreased, which therefore lowers the power dissipation.

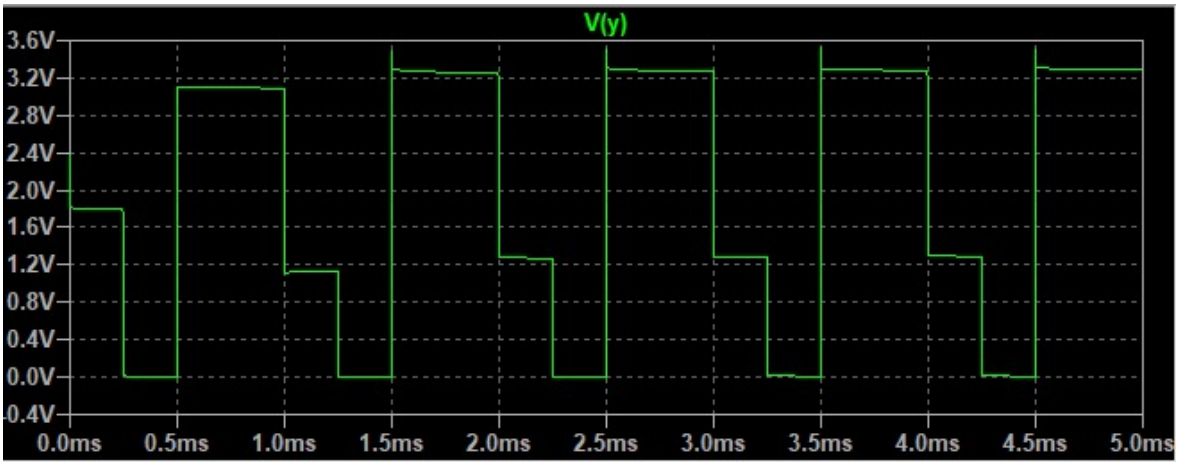
Problem 4: Logic Gate

Design a XOR (exclusive OR) logic gate. The gate should be realized by using a pull-up and a pull-down network. Only if one of the input signals is getting high the output signal is getting high. If both input signals are getting high the output signals is getting low. Use LTSpice to show the circuit. Simulate to verify the function.




V(n005)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms


V(n004)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms


V(y)
3.6V
3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms