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CONCLUSION

In this paper, we study logic synthesis and defect tolerance of memristor based crossbar arrays. We propose two-level and multi-level logic synthesis techniques. In addition, we devise a defect model and propose a hybrid defect tolerant logic mapping method. We show that in spite of defective components, securing a valid mapping is achievable with an appropriate algorithm. As a future direction, we plan to integrate multi-level logic design with our defect tolerant logic mapping meth-ods.

ACKNOWLEDGEMENT

REFERENCES

1. Tunali O and Altun M, "A survey of fault-tolerance algorithms for reconfigurable nano-crossbar arrays," *ACM Comput. Surv.*, vol. 50, pp. 79:1–79:35, Nov. 2017.

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