EXPERIMENT NO.

Finite State Machine

AIM: To write VHDL code, synthesis, implement Mealy machine for given example

SOFTWARE TOOL:

KIT:

THEORY: This experiment is about implementing a finite state machine. Finite state machine is a graphical model/representation of sequential activities or events. After representing and modeling the events they can be implemented easily in case of sequential logic designs.

Finite state machines can be utilized in many fields of study e.g. neural networks, artificial intelligence, mathematics, games, robotics and sequential flow of data. Since we are dealing with the sequential circuits so i will explain their use in sequential circuit design in this tutorial.

Types of finite state machines

There are many fsm (finite state machines) in existence. The two most popular used in digital combinational and sequential circuits are

- **Mealy Machine**
- **Moore Machine**

Difference between Mealy vs Moore machine

The main difference between mealy and moore is the computation of the next state. In mealy machine the output depends on the current state and the input variables. Where as in moore machine the output depends on the current state only. There are also other differences which are hardly highlighted anywhere.

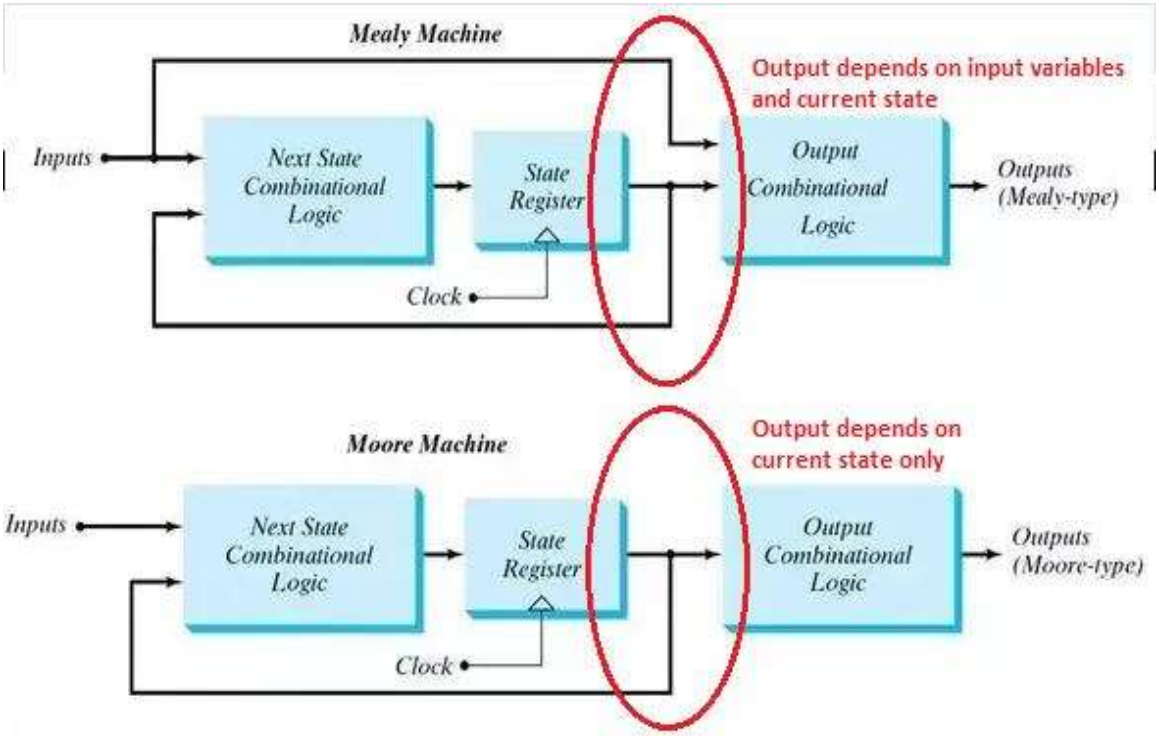
Moore Machine

1. More number of states in moore compared to mealy for same fsm.
2. States change after 1 clock cycle. Latency = 1.
3. Synchronous output. Because the states are determined in a process.
4. States are output.

Mealy Machine

1. Less number of states in mealy compared to moore for same fsm.
2. State transition on the same clock cycle. Latency = 0.
3. Asynchronous output.

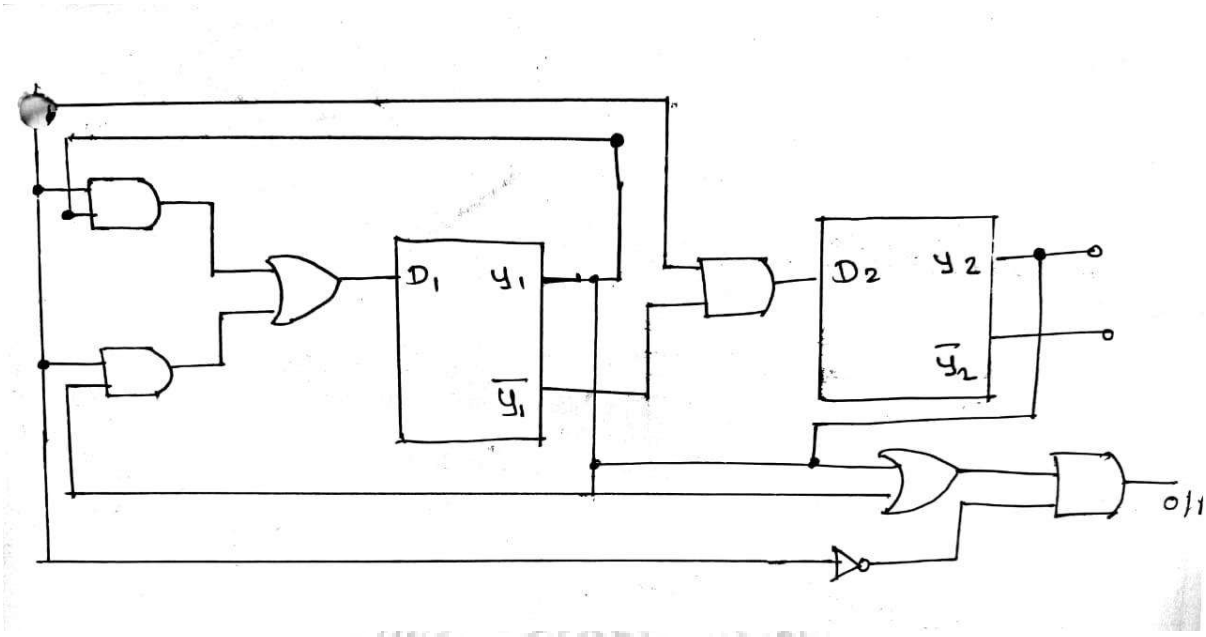
4. Transition are output.



Mealy Machine	Moore Machine
Output depends both upon the present state and the present input	Output depends only upon the present state.
Generally, it has fewer states than Moore Machine.	Generally, it has more states than Mealy Machine.
The value of the output function is a function of the transitions and the changes, when the input logic on the present state is done.	The value of the output function is a function of the current state and the changes at the clock edges, whenever state changes occur.
Mealy machines react faster to inputs. They generally react in the same clock cycle.	In Moore machines, more logic is required to decode the outputs resulting in more circuit delays. They generally react one clock cycle later.

Problem Statement:

Implement the Mealy Machine for following diagram using VHDL language.



PIN CONFIGURATION

Sr No	Input/ Output	Pin No	Sr No	Input/ Output	Pin No

Conclusion:

