EXPERIMENT NO. 7

NAND Gate using CMOS

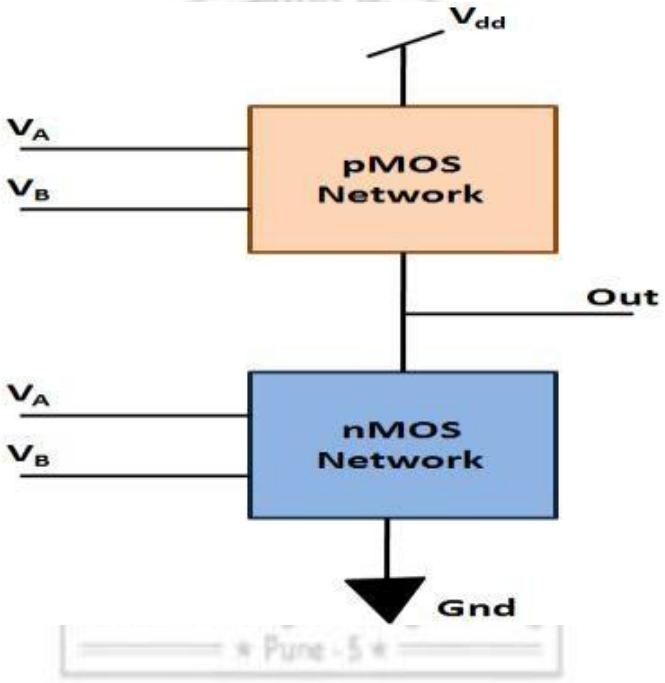
AIM: To simulate two input NAND Gate Circuit using CMOS technology

SOFTWARE TOOL: Microwind version 3.1

KIT:

THEORY:

For the design of any circuit with the CMOS technology; We need parallel or series connections of nMOS and pMOS with a nMOS source tied directly or indirectly to ground and a pMOS source tied directly or indirectly to Vdd. A basic CMOS structure of any 2-input logic gate can be drawn as follows:



2 Input NAND Gate

TRUTH TABLE

V_A	V_B	V_{out}
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

CIRCUIT

Circuit Diagram of two input NAND gate:

The above drawn circuit is a 2-input CMOS NAND gate. Now let's understand how this circuit will behave like a NAND gate. The circuit output should follow the same pattern as in the truth table for different input combinations.

Case-1 : VA – Low & VB – Low

As VA and VB both are low, both the pMOS will be ON and both the nMOS will be OFF. So the output Vout will get two paths through two ON pMOS to get connected with Vdd. The output will be charged to the Vdd level. The output line will not get any path to the GND as both the nMOS are off. So, there is no path through which the output line can discharge. The output line will maintain the voltage level at Vdd; so, High.

Case-2 : VA – Low & VB – High

VA – Low: pMOS1 – ON; nMOS1 – OFF

VB – High: pMOS2 – OFF; nMOS2 – ON

pMOS1 and pMOS2 are in parallel. Though pMOS2 is OFF, still the output line will get a path through pMOS1 to get connected with Vdd. nMOS1 and nMOS2 are in series. As nMOS1 is OFF, so Vout will not be able to find a path to GND to get discharged. This in turn results the Vout to be maintained at the level of Vdd; so, High.

Case-3 : VA – High & VB – Low

VA – High: pMOS1 – OFF; nMOS1 – ON

VB – Low: pMOS2 – ON; nMOS2 – OFF

The explanation is similar as case-2. Vout level will be High.

Case-4 : VA – High & VB – High

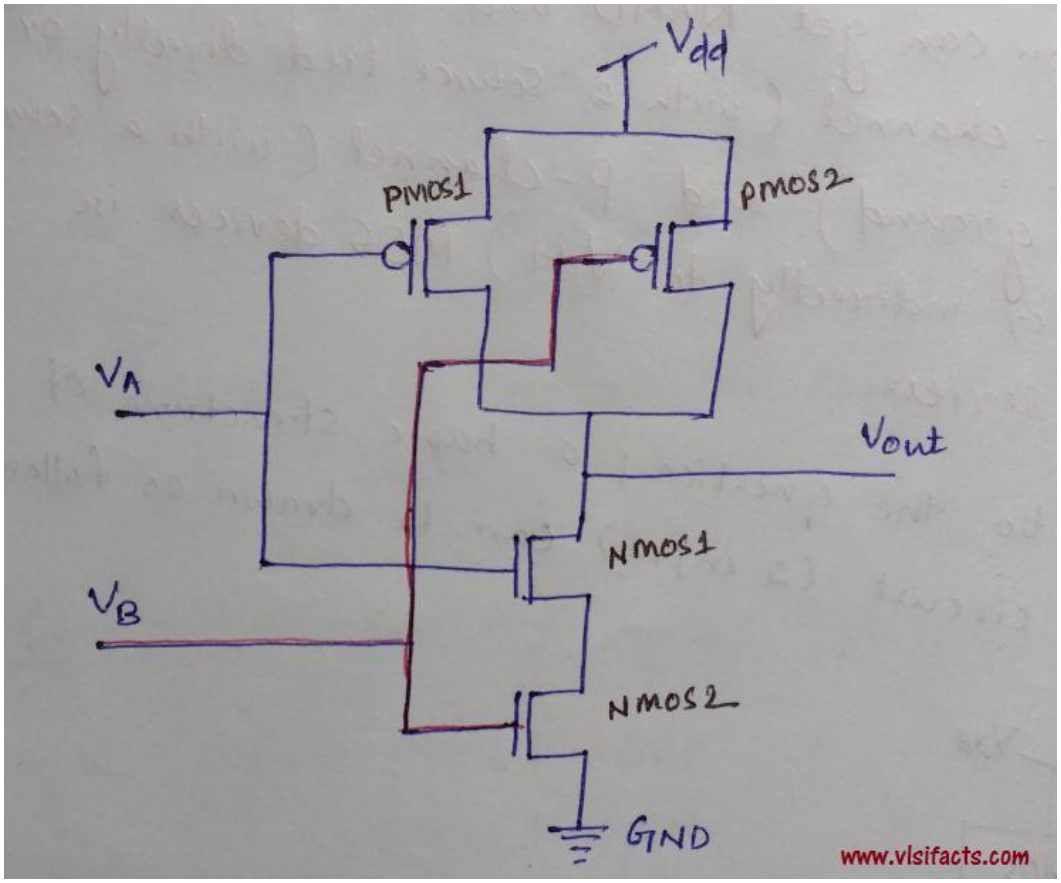
VA – High: pMOS1 – OFF; nMOS1 – ON

VB – High: pMOS2 – OFF; nMOS2 – ON

In this case, both the pMOS are OFF. So, Vout will not find any path to get connected with Vdd. As both the nMOS are ON, the series connected nMOS will create a path from Vout to GND. Since, the path to ground is established, Vout will be discharged; so, Low.

In all the 4 cases we have observed that Vout is following the exact pattern as in the truth table for the corresponding input combination.

Simulation on Microwind:



Conclusion:

EXPERIMENT NO. 8

2:1 Multiplexer Using NAND Gate

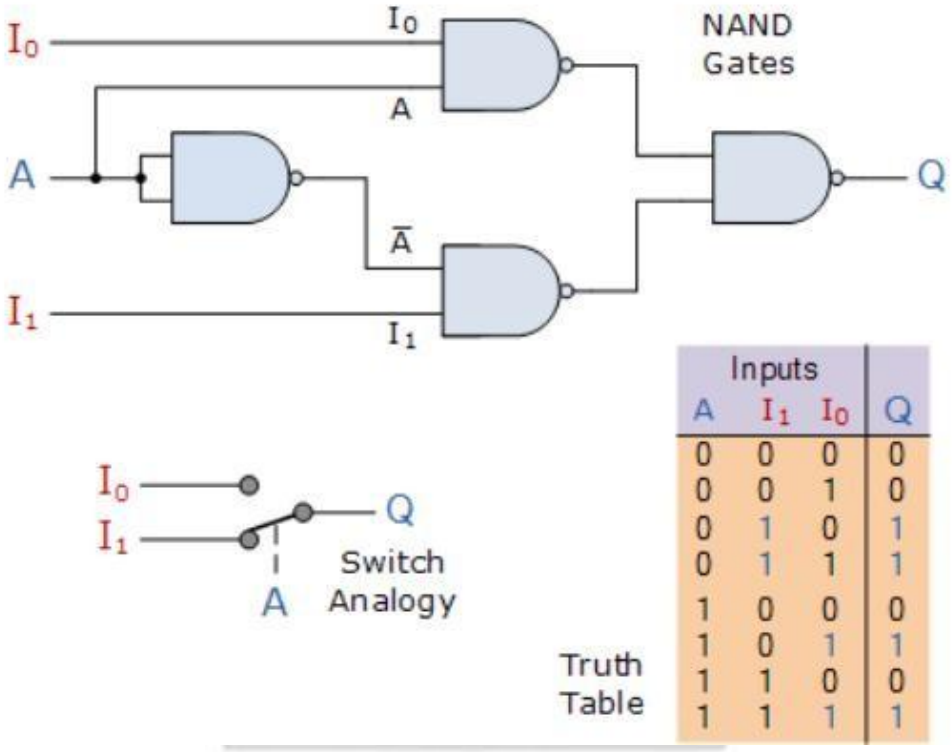
AIM: Ti design and simulate 2:1 Mux using Two inpute NAND gate

SOFTWARE TOOL: Microwind version 3.1

KIT:

THEORY:

Input Multiplexer Design



The input A of this simple 2-1 line multiplexer circuit constructed from standard NAND gates acts to control which input (I0 or I1) gets passed to the output at Q.

From the truth table above, we can see that when the data select input, A is LOW at logic 0, input I1 passes its data through the NAND gate multiplexer circuit to the output, while input I0 is blocked. When the data select A is HIGH at logic 1, the reverse happens and now input I0 passes data to the output Q while input I1 is blocked.

So by the application of either a logic “0” or a logic “1” at A we can select the appropriate input, I0 or I1 with the circuit acting a bit like a single pole double throw (SPDT) switch.

As we only have one control line, (A) then we can only switch 21 inputs and in this simple example, the 2-input multiplexer connects one of two 1-bit sources to a common output, producing a 2-to-1-line multiplexer. We can confirm this in the following Boolean expression

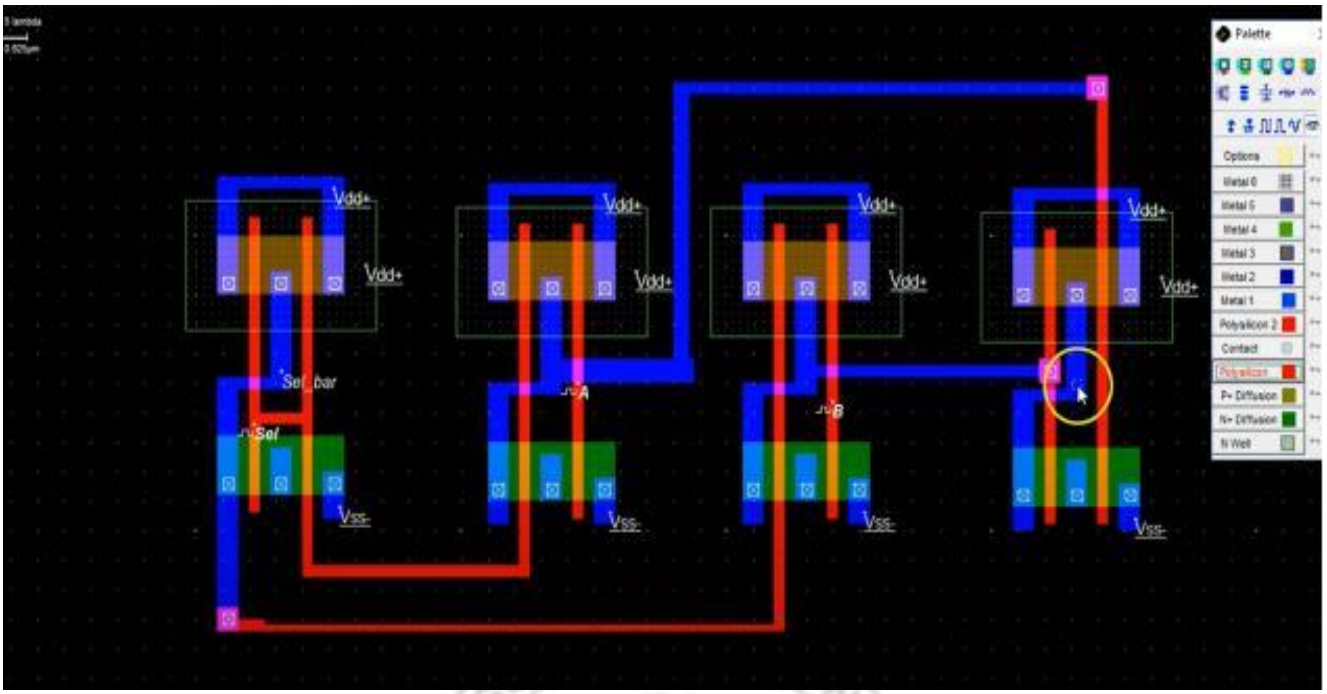
$$Q = A.I0.I1 + A.I0.I1 + A.I0.I1 + A.I0.I1$$

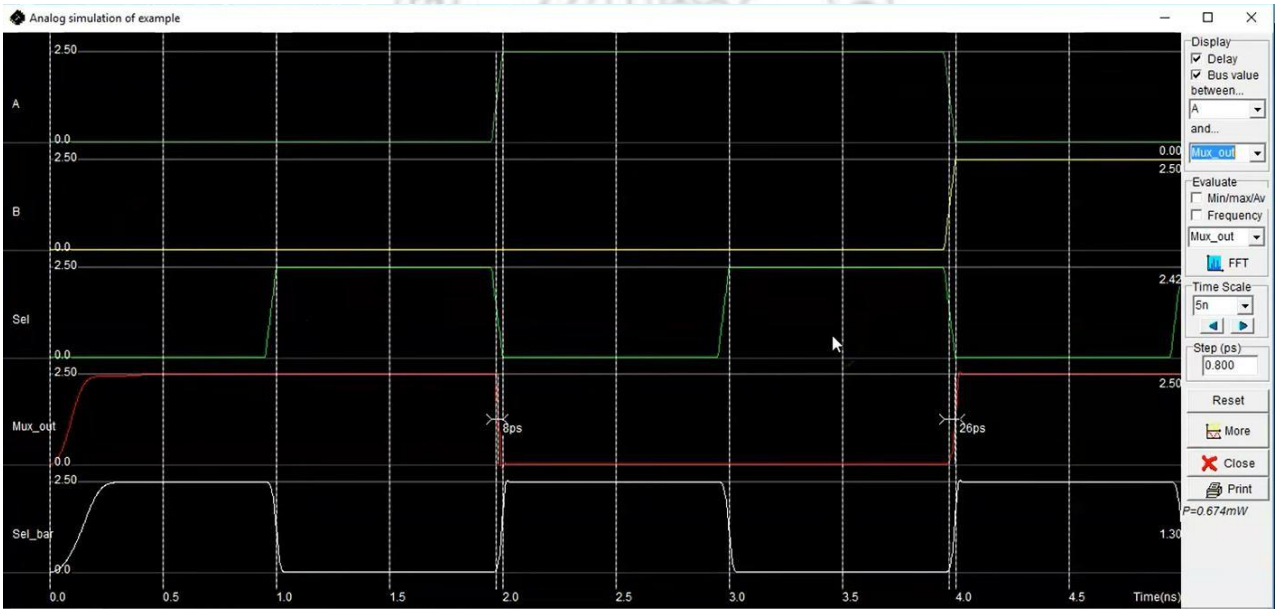
and for our 2-input multiplexer circuit above, this can be simplified too:

$$Q = A.I1 + A.I0$$

We can increase the number of data inputs to be selected further simply by following the same procedure and larger multiplexer circuits can be implemented using smaller 2-to-1 multiplexers as their basic building blocks. So for a 4-input multiplexer we would therefore require two data select lines as 4-inputs represents 22 data control lines give a circuit with four inputs, I0, I1, I2, I3 and two data select lines A and B

Conclusion:


Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Vdd+
Vss-
Sel_bar
Sel
A
B


Analog simulation of example
A
B
Sel
Mux_out
Sel_bar
2.50
0.0
8ps
26ps
Time(ns)
Display
Delay
Bus value between...
and...
Evaluate
Min/max/Av
Frequency
FFT
Time Scale
5n
Step (ps)
0.800
Reset
More
Close
Print
P=0.674mW