Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices

Giorgio Ferrari, *Member, IEEE*, Fabio Gozzini, *Member, IEEE*, Alessandro Molari, and Marco Sampietro

***Abstract*—The paper presents a very high sensitivity transimpedance amplifier in standard CMOS 0.35 μm technology suited for sensing current signals from molecular and nanodevices systems. The circuit, based on an integrator followed by a differentiator configuration, features i) a low-noise time-continuous feedback loop to cope with possible standing currents from the device under test as high as few tens of nA without limiting the signal dynamic range; ii) active current-reducers to implement very high value equivalent resistances of hundreds of GΩ with high linearity irrespective to the current direction and characterized by a shot noise current level $(2qI)$ which is, for low standing current, few orders of magnitude smaller than a physical resistor of equal value and iii) nested-Miller compensation networks to ensure strong stability over a bandwidth of few MHz. Thanks to the ability to draw large standing currents, the circuit is suitable for a use in biological systems where physiological medium is co-present. The measured input equivalent noise of 4 fA/$\sqrt{\text{Hz}}$ at about 100 kHz, recorded when the input dc current is lower than 10 pA, allows the chip to be used, among others, in impedance spectroscopy measurements at the nanoscale with a capability of detecting capacitance variations in sub-attofarad range to cope with the challenges of single-chip instrumentation.**

***Index Terms*—Active resistor, high sensitivity instrumentation, instrument-on-chip, transimpedance amplifier.**

I. Introduction

TRANSIMPEDANCE amplifiers, used to sense the signal current made available by an input device (a sensor or others) and to convert it into a voltage with maximum signal-to-noise ratio ready for further processing, are gaining increasing importance in the domain of single molecules and nano-scaled devices characterization [1], [2]. Thanks to the input virtual ground, the current flowing in the device under test (DUT) can be measured with high accuracy irrespective of the overwhelming stray capacitances introduced by the connections. This peculiarity is for example essential when the impedance of a nanosample is under investigation (see Fig. 1): by applying a sinusoidal input voltage across the nanosample and by sensing the current, the impedance information can be extracted by processing the in-phase and in-quadrature current components. Indeed, impedance spectroscopy is an essential tool to study the frequency response of a variety of systems and to obtain characteristic parameters of devices such as dielectric constant, charge carrier density, junction capacitance, as well as to study interface adsorption and charge transfer reaction in electrochemistry [3], [4]. The utilization of impedance measurement is not limited to the characterization of nanosamples, but can be extended to the realization of affinity molecular biosensors, where the binding of a target molecule with an high specific biological macromolecule such as antibodies, receptors and DNA strands is detected by measuring an impedance change [5], [6].

The miniaturization offered by the integrated technologies gives two key advantages with respect to discrete-components realizations: i) it reduces the total input capacitance, improving the signal to noise ratio and the impedance matching with the nanodevices; ii) it makes possible to obtain high density systems to measure many devices in parallel. The design of a single-chip integrated transimpedance amplifier deserves special care if very high sensitivity and wide bandwidth are desired. The classic configuration of transimpedance amplifier having a simple resistor R_f in the feedback path of an Operational Amplifier (opamp), cannot be adopted. Since the feedback resistor defines the sensitivity of the transimpedance amplifier, as it sets the current noise $(4\ \text{kT}/R_f)$ at the input node, and also defines the precision of the instrument as it sets the current-to-voltage conversion factor, the classic configuration requires a stable and linear resistor of very high value (GΩ values are currently used in discrete realizations) that cannot be directly integrated.

The lack of high-value and linear resistors in standard integrated technologies has solicited the design of transimpedance amplifier having an integrator-differentiator architecture, as shown in Fig. 1. In this case the feedback resistor of the opamp is substituted by a well defined and stable in value capacitor obtaining a large bandwidth integrating amplifier which will be followed by a differentiating amplifier to recover the desired relationship between input current and output voltage. Such a pure architecture offers a unique cocktail of very low noise (besides the opamp, no noisy elements are added to the input node along the signal path), of current-to-voltage stability (the gain being given by the ratio of two capacitors) and of wide bandwidth practically approaching the gain-bandwidth product of the opamp. It has the strong disadvantage of being prone to saturation of the integrator stage caused by the leakage currents flowing to the input node from the DUT and/or the opamp. A simple switch in parallel to C_i operated when the integrator output voltage reaches a defined threshold, would set a limit to the time interval available to measure the DUT current [7], [8]. This time would depend both on the impinging leakage current and on C_i and can become easily insufficient

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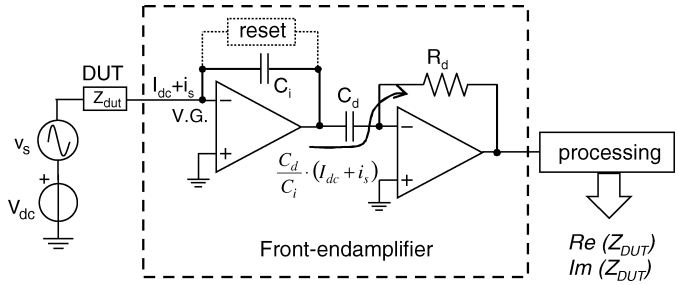

Fig. 1. Impedance spectroscopy experimental setup. The input voltage $V_{\rm dc}+v_s$ is applied across the D.U.T and the parasitic capacitances of the connections of the DUT toward the voltage source on the left and toward the amplifier on the right do not affect the measurement. The amplitude and phase shift of the sinusoid at the amplifier output give the DUT impedance information. A reset network should be added to prevent the saturation of the integrator induced by the dc input current.

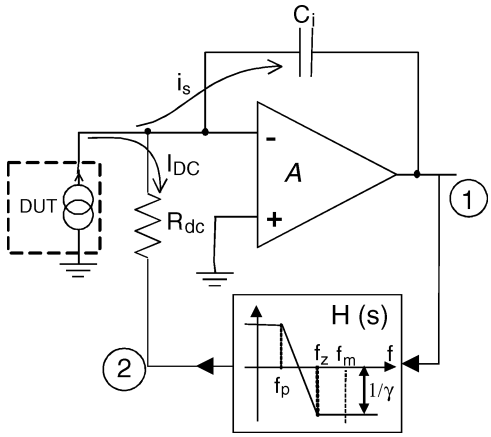

Fig. 2. Schematic of the feedback network to discharge the standing current from the DUT connected to the integrator stage.

for many applications. For example, biomolecules kept in physiological liquid may have a leakage current in the range of tens of nA: assuming a C_i of 100 fF a measurement period of only few tens of μs would result! A continuous reset using a MOS transistor as pseudoresistor in parallel to the feedback capacitance, as applied in voltage sensing [9] and capacitive sensing [10] circuits, cannot be used to realize transimpedance amplifier with a wide dynamic range. The equivalent resistance of the pseudoresistor, and consequently the frequency response, is proportional to the stationary input current introducing an unacceptable signal-dependent behavior. Active systems that continuously reset the dc current have to work only up to very low frequencies (hundreds of Hz or less) to leave untouched the signal over a large bandwidth. Because of this requirement, the successful solutions available in the literature to reset the feedback capacitance of charge preamplifiers [11], [12] cannot be directly transferred to transimpedance amplifiers. Those architectures are not conceived to have poles at such low frequencies and to have a frequency response independent from the leakage current. The circuit presented in this paper is specifically designed to solve these problems and to ensure an operating bandwidth up to 4 MHz when connected to devices having from zero up to $\pm$25 nA of input steady current, with a noise floor as low as 3 fA/$\sqrt{\rm Hz}$ at low currents. To reach these goals a specifically conceived feedback architecture and new circuit solutions to obtain very high value linear and low-noise resistors are presented.

II. Feedback Architecture

The continuous discharge architecture [13] is schematically shown in Fig. 2 where the integrator stage has a second feedback loop made of an amplifier $H(s)$ and a resistance $R_{\rm dc}$. The loop gain of the new feedback loop can be written as

$$G_{loop} = -H(s)\frac{A}{1+s(1+A)C_iR_{\rm dc}} \tag{1}$$

where A is the gain of the operational amplifier. The amplifier $H(s)$ has a gain from node 1 to node 2 which is large at very low frequency and strongly attenuated elsewhere. Therefore, at low frequency the feedback is strong enough to control the voltage across $R_{\rm dc}$ and to draw the DUT current, $I_{\rm DC}$ into the resistor. For higher frequencies, instead, the feedback is inactive and consequently not affecting the input signal, i_s, that is integrated in the capacitance C_i. The frequency f_m at which $|G_{loop}(f_m)| = 1$ defines the lowest signal frequency amplified by the integrator-differentiator path, 100 Hz in our case. Note that by choosing $|H(0)| \gg 1$ the dc value of the integrator output (node 1 in Fig. 2) is kept almost at zero irrespective of the dc input current, thus ensuring the maximum ac dynamic range for the signal and a high linearity of the integrator in any bias condition.

Since the integrator introduces a pole at very low frequency, $f_{\rm int} = 1/[2\pi(1+A)C_iR_{\rm dc}]$, the stability of the new feedback loop depends on $H(s)$ and the phase margin can be written as $\varphi_m = 90^\circ - \angle H(f_m)$. By using an amplifier $H(s)$ with one pole at the frequency f_p and one zero at the frequency $f_z > f_p$, as reported in Fig. 2, a phase margin greater than 45° is ensured just providing that $f_z < f_m$. In this condition, the minimum frequency amplified by the integrator-differentiator is given by the following expression:

$$f_m = \frac{1}{2\pi R_{\rm dc}C_i\gamma}\frac{A}{1+A} \tag{2}$$

where γ is the attenuation of $H(s)$ for frequencies greater than f_z and is a free parameter that can be tuned to obtain the desired value of f_m. In our case we have chosen $\gamma = 400$, so to shift f_m by a factor of 400 lower in frequency with respect to the case of $H(s)$ not present.

The challenges solved to implement an integrated solution using a low-noise high value resistance $R_{\rm dc}$ and an amplifier $H(s)$ with pole and zero frequencies well below 100 Hz are discussed in the following section.

III. Feedback Network Implementation

A. Design of Active Resistance $R_{\rm dc}$

As the current noise of the resistor $R_{\rm dc}(4\,{\rm kT}/R_{\rm dc})$ is injected directly into the input node (see Fig. 2), to have it as low as few fA/$\sqrt{\rm Hz}$ it would be necessary to use very large value resistors, in the GΩ range. Since technological limits prevent the integration of such high value resistor, we have implemented

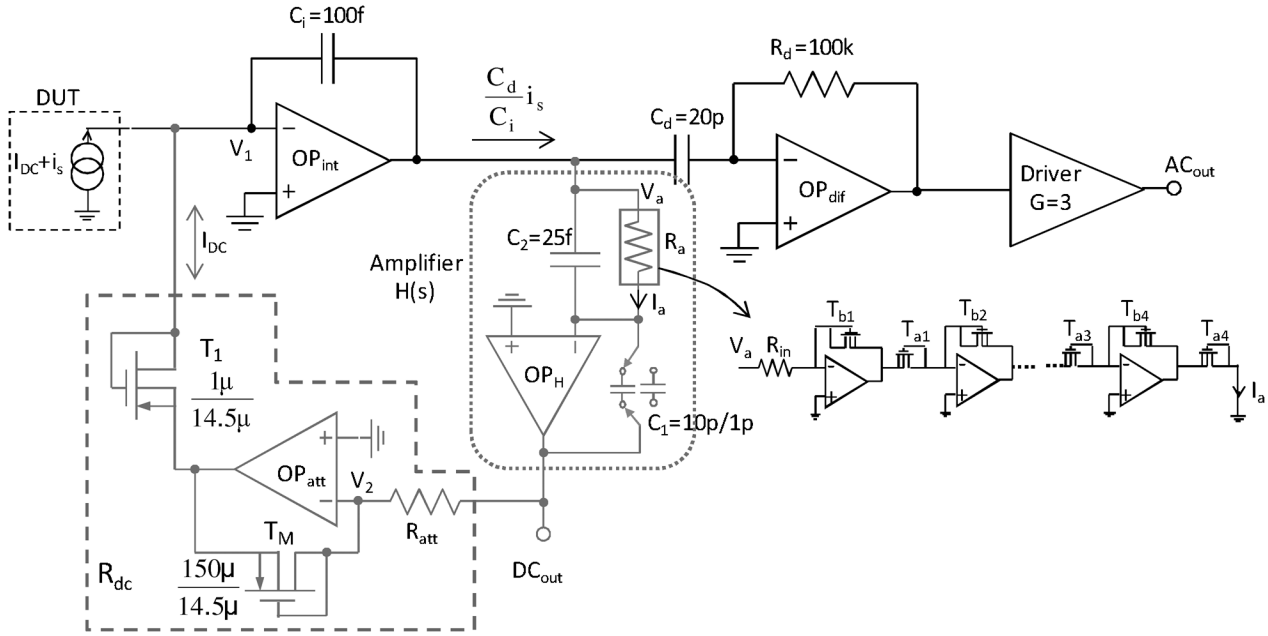

Fig. 3. Schematics of the transimpedance amplifier prototype with active network to drain the dc input current. The $R_{\rm dc}$ resistor of Fig. 2 is implemented by the current reducer reported inside the dashed box on the lower left, while the large resistor R_a is implemented by cascading 4 current reducer systems.

it with an active low-noise circuit. Note that although the linearity of element $R_{\rm dc}$ does not affect directly the signal path, a non-linear element such as a simple transistor would give a frequency f_m (and consequently also a loop stability) dependent on the input dc current. Our solution for "$R_{\rm dc}$" uses a linear transconductor as shown in the dashed box on the left-side of Fig. 3. The core of this system are the matched MOS transistors T_1 and T_M connected with source-well short circuited: with negative gate-source voltage (V_{GS}), the devices operate as a pMOS-diode; with positive V_{GS}, the parasitic drain-well $(p-n)$ junctions are forward biased, and the transistors act as a $p-n$ junction diode [14]. The matched MOSFETs have the same channel length and are biased with the same voltage, thus the current density in the MOSFET T_M is the same as in T_1, irrespective to the sign of the leakage current $I_{\rm DC}$ flowing in T_1. By designing T_M M-times larger than T_1, the overall system acts as a linear and accurate current reducer by a factor M. A physical resistor $R_{\rm att}$ is used to convert linearly the $H(s)$ output voltage into a current subsequently reduced to obtain an equivalent resistance of $M \cdot R_{\rm att}$. Fig. 4 shows the measured *I–V* characteristic of the $R_{\rm dc}$ block, when a reducing factor $\mathrm{M} = 150$ and a resistor $R_{\rm att}$ of 300 kΩ is chosen, certifying an equivalent resistance of $R_{\rm dc} = M \cdot R_{\rm att} \cong 45$ MΩ with good linearity over the full input current range.

The noise at the output of the implemented scheme is given by two fundamental components: the thermal noise of the physical resistor $R_{\rm att}$, which reaches the input of the transimpedance amplifier reduced by the factor M^2, and the shot noise of MOSFET T_1. Hence, the noise injected into the input is equivalent to a very large resistance of 6.5 GΩ, although the *I–V* characteristic (equivalent to a resistor of only 45 MΩ) ensures a dc current range of ±25 nA using a ±1.5 V power supply. This low noise condition is valid for currents less than the few pA. For greater $I_{\rm DC}$ currents, the shot noise $(2qI_{\rm DC})$ of the T_1 transistor operating in subthreshold regime or as $p-n$ junction diode becomes dominant. The flicker noise of T_1 in the signal band has been made negligible by using a non-minimal MOSFET area.

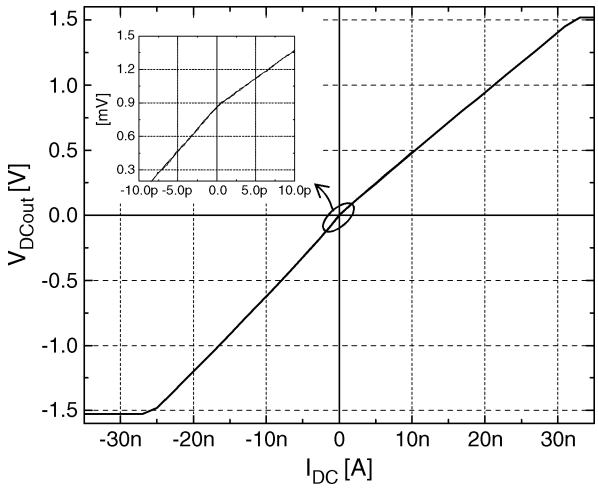

Fig. 4. Measured *I–V* characteristic of the active $R_{\rm dc}$ made with matched MOSFETs, certifyng an equivalent resistance of about 45 MΩ.

B. Amplifier $H(s)$ Design

A second critical aspect of the project is the realisation of the feedback network $H(s)$ having: i) zeros and poles at frequencies well below the signal bandwidth (100 Hz in our case); ii) a high dc gain, $H(0)$, to keep the output of the integrator close to zero irrespective of the dc current. We adopted the first order circuit showed in the dotted box in the center of Fig. 3. The transfer function of this network up to the first pole of the operational amplifier OP_H is

$$H(s) = -\frac{A_0(1+sC_2R_a)}{1+sR_a\left[C_2+C_1(1+A_0)\right]} \tag{3}$$

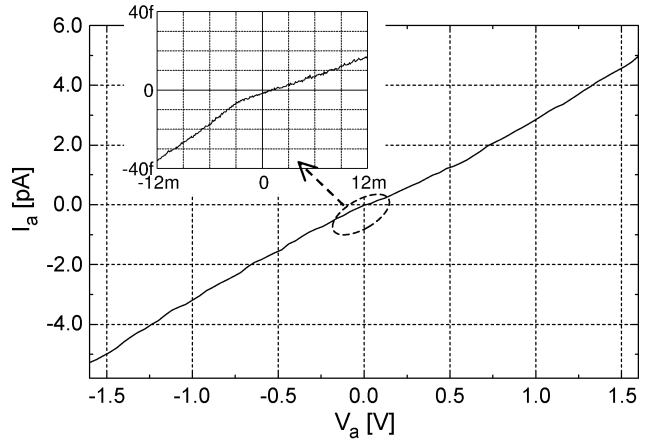

Fig. 5. I-V characteristic curve of a cascade of 4 current reducers realized with the matched MOSFET scheme. In the inset the magnification around zero shows the ability to drive current in the fA range.

where A_0 is the dc gain of the amplifier OP_H. Technological aspects play an important role in defining the values of C_1, C_2 and R_a. Taken a maximum practical value of the differentiator resistor R_d at 100 kΩ and a maximum practical value of C_d of 20 pF, to make negligible the thermal noise of R_d with respect to the noise of the integrator stage, a ratio $C_d/C_i > 100$ is required, thus setting $C_i \approx 100$ fF. Given these values, to set the minimum frequency f_m at 100 Hz the γ factor in the (2) must be equal to 400. Fixing $C_1 = 10$ pF to limit the die area, the capacitor C_2 must be of 25 fF. Then, the feedback stability condition $(1/2\pi C_2 R_a < f_m)$ imposes a resistor R_a in the order of hundreds GΩ. Such a large value has been implemented using a cascade of 4 current reducers similar to that discussed in the previous section. Fig. 5 reports the measured *I–V* characteristic and shows that with this technique it is possible to make transconductance as low as $1/300$ G$\Omega = 3.3$ pA/V with a good linearity and capable to drive very small current down to fA. Parasitic currents are not present in the input/output current because all MOSFET terminals are actively controlled by the operational amplifier used in the current reducer and the leakage current of n-well-substrate is driven directly by the amplifier output. The linearity in the full range of the input voltage ensures the stability of the dc feedback loop in every bias conditions.

IV. Operational Amplifiers Design

A. Integrator opamp

The forward amplifier of the integrator stage plays a major role in the performance of the instrument as it sets i) the noise of the system, ii) the high frequency bandwidth limit of the full transimpedance and iii) the dc voltage of the input node. This latter point leads to the use of a differential input configuration, powered at ± 1.5 V, to control the voltage of the virtual ground of the integrator and to apply an accurate dc signal across the DUT without introducing an external voltage source. For this reason the simple common source configuration, typical in many low noise applications [15], [16], has not been used. To lower flicker noise, pMOS transistors are preferable to nMOS in the input differential stage even if they have a slightly larger white noise. The high input impedance together with the low gate bias current make negligible the parallel (current) noise of the differential pair. Its voltage noise $\overline{e_{n,i}^2}$, instead, would be amplified by the overall capacitance at the inverting input of the opamp, giving an equivalent input current noise of

$$\overline{i_{\mathrm{eq}}^2} = (2\pi f)^2 (C_i + C_{\mathrm{DUT}} + C_{\mathrm{gate}})^2 \overline{e_{n,i}^2} \tag{4}$$

where C_{gate} is the capacitance of the input transistor, C_{DUT} is the capacitance related to the device under test (DUT) including the wire connection. Because of the frequency dependence, this noise would become dominant in the high frequency region of the signal bandwidth and must be minimized. Consequently, special care must be kept in sizing the differential input transistors as they set both C_{gate} and $\overline{e_{n,i}^2}$ through the following expressions:

$$\overline{e_n^2} = 2 \cdot 4kT \frac{2}{3} \frac{1}{g_m} = 2 \cdot \frac{4kT}{3\mu_p} \frac{2L^2}{C_{\mathrm{gate}} V_{od}} \tag{5}$$

$$C_{\mathrm{gate}} = C'_{ox} W L \tag{6}$$

where the factor 2 in $\overline{e_{n,i}^2}$ reflects the presence of two MOSFETs in the differential pair, $k$is the Boltzman constant, μ_p is the hole mobility in the channel, $V_{od} = V_{GS} - V_T$ is the overdrive voltage, C'_{ox} is the gate capacitance for unit area and W, L are respectively the channel width and length. Since in our project we have not power consumption constraints, the minimization of the (4) has been done by fixing the overdrive voltage to the maximum possible value that would maximize the dynamic range that is at about 350 mV. Taking into account (5), (6), the following condition for the gate capacitance is obtained [17], [18]:

$$C_{\mathrm{gate}} = C_i + C_{\mathrm{DUT}}. \tag{7}$$

In our case, with C_i already set at 100 fF and C_{DUT} estimated in the range of 0.5 pF (dominated by the chip interconnection and by the bonding pad), we obtained $C_{\mathrm{gate}} = 600$ fF leading to $\mathrm{W} = 220$ μm and $\mathrm{L} = 0.6$ μm, the minimum value to achieve a good matching of the differential pair and a good drain resistance together with the desired minimum $\overline{e_n^2}$. In this way the additional small capacitance of the real nanometer-scale devices which will be connected to the bonding pad would not alter this choice and the amplifier can be used in many different applications without the need of a re-design.

The integrator's opamp schematic, without bias circuits, is reported in Fig. 6. The differential input stage is purely resistively loaded because the white noise component and 1/f noise of the resistances are lower than the noises of an active load using a nMOS current mirror. The second stage of the operational amplifier is again a differential pair with active load that injects its current in a multipath nested Miller compensation stage [19], [20] to obtain high gain with strong feedback stability. The overall gain–bandwidth product of the opamp is about 100 MHz. The output stage uses a complementary common-source topology [21] to provide a rail-to-rail output swing.

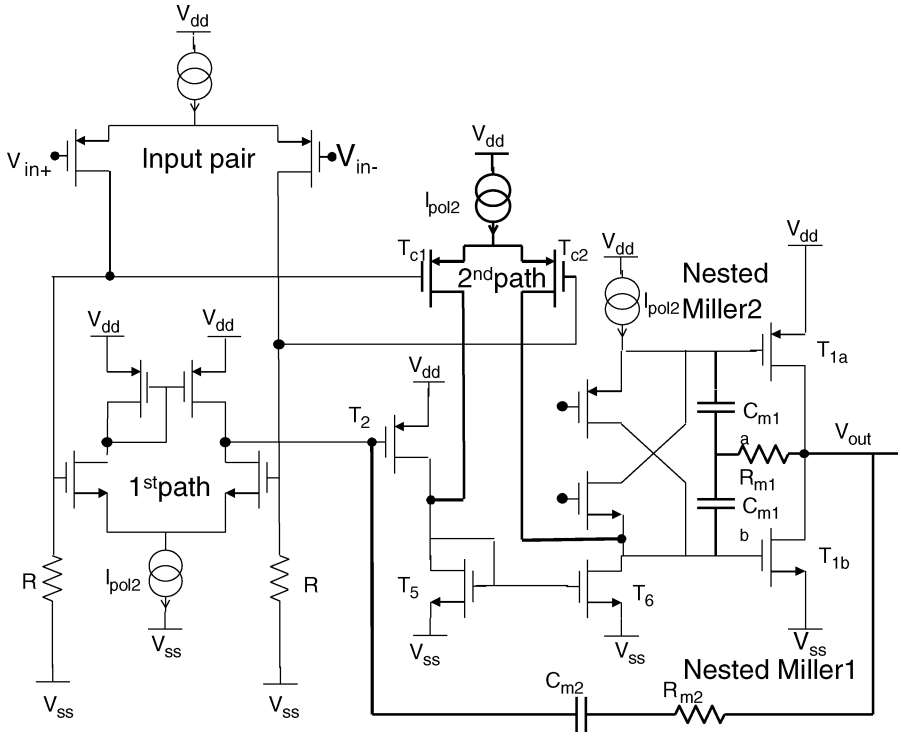

Fig. 6. Schematic of the integrator opamp. A pMOSFET input pair with resistive load has been used to reduce the effect of the flicker noise.

B. Differentiator Opamp

As previously discussed, noise constraints impose high values of R_d and C_d (respectively 100 kΩ and 20 pF) that introduce a pole in the loop gain of the differentiator stage at frequency of $1/2\pi R_d C_d = 80$ kHz, thus affecting the feedback stability. A standard compensation, achieved by adding a feedback capacitance C_{fd} in parallel to the resistance R_d, would require to place the pole $1/2\pi R_d C_{fd}$ at a frequency greater than the differentiator bandwidth (10 MHz in our case) and consequently to have a gain-bandwidth product of the operational amplifier greater than 10 MHz $\cdot\, (C_d + C_{fd})/C_{fd} \cong 1.25$ GHz. Alternatively, without affecting the closed-loop transfer function, we introduced a zero directly in the frequency response of the operational amplifier by adding in the Miller compensation network a second active feedback as reported in Fig. 7. In the signal bandwidth, the open loop frequency response of the opamp can be approximated with the expression

$$A(s) \cong A_0 \frac{1 + sC_f R_f}{1 + sC_f R_f A_0 g_{mf}/g_{m1}} \tag{8}$$

where $A_0 = g_{m1}R_1 g_{m2}R_2$ is the dc gain of the opamp. By choosing $R_f = 400$ kΩ and $C_f = 5$ pF, the zero $1/2\pi R_f C_f$ compensates the pole $1/2\pi R_d C_d$ in the loop gain of the differentiator stage ensuring stability and wide bandwidth. Since the compensation depends only on passive elements, an excellent robustness to temperature variations or process variability is guaranteed. This solution is achieved with a small amount of silicon area: the required area for the feedback network is in fact almost totally given by the reduction of the Miller capacitance C_m which is only 1 pF instead of tens of pF in most common solutions.

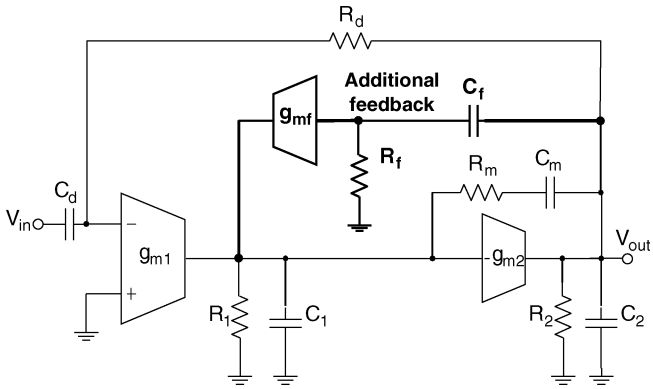

Fig. 7. Block diagram of the differentiator stage. An additional feedback network (C_f, R_f, g_{mf}) introduces a zero to compensate the external pole $1/2\pi R_d C_d$.

V. Circuit Performance

A. Experimental Results

The Fig. 8 shows the chip micrograph of the overall circuit. The chip, fabricated in a 0.35 μm CMOS technology, dissipates 45 mW and operates with a dual supply voltage of ± 1.5 V. To guarantee a good driving capability on a rail-to-rail output voltage swing, an additional driver stage with gain 3 has been added to the output of the circuit in Fig. 3 ensuring a total transimpedance of about $C_d/C_i \cdot R_d \cdot 3 = 60$ MΩ.

The amplifier has an additional output, $\mathrm{DC_{out}}$ in Fig. 3 whose input-output characteristic is given by the equivalent resistance $R_{\mathrm{dc}} = M \cdot R_{\mathrm{att}}$ of Fig. 4, that can be used to perform measurements also in the low frequency range. Fig. 9 shows the

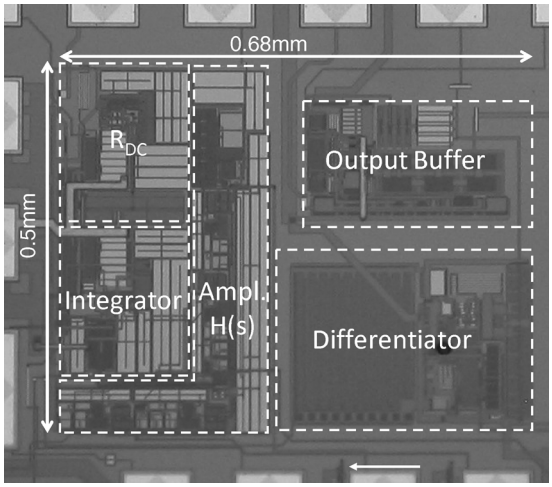

Fig. 8. Chip micrograph. The silicon area is 0.5×0.68 mm^2 without the bonding pads.

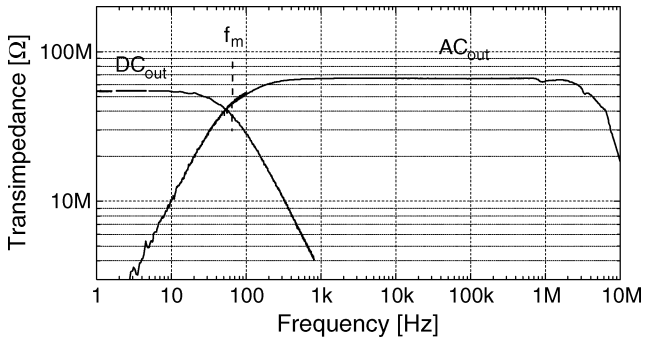

Fig. 9. Experimental frequency response of the transimpedance amplifier taken at both available outputs. In this case $C_1 = 10$ pF (see Fig. 3) giving $f_m \cong 100$ Hz.

measured bandwidth from both the outputs: the transition frequency f_m can be selected among two values, about 100 Hz or 1 kHz, depending on the needs of a specific application (this feature has been implemented by using two switches to select the capacitor C_1 in the amplifier $H(s)$, as sketched in Fig. 3, in order to change the attenuation γ of the amplifier $H(s)$ in agreement with (2)); the maximum frequency, 4 MHz, is limited only by the feedback loop of the integrator, i.e., $f_{\max} = \mathrm{GBP} \cdot C_i/(C_i + C_{\mathrm{gate}} + C_{\mathrm{DUT}})$ with a testing capacitor of $C_{\mathrm{DUT}} = 1$ pF. The signals from the two outputs can be easily combined to perform for example impedance spectroscopy measurements: by previously measuring both "gains" the impedance up to 100 Hz is extracted from $\mathrm{DC_{out}}$, while the impedance from 100 Hz onward is extracted from $\mathrm{AC_{out}}$.

Fig. 10 shows the measured equivalent input noise in the case of low input dc current ($I_{\mathrm{DC}} < 10$ pA), that is when the shot noise of the MOSFET T_1 is negligible with respect to the thermal noise of the resistors. The experimental noise current density is in agreement with the theoretical prediction (dashed line) discussed in the previous sections and summarized here taking into account the major contributions of the entire system:

$$\overline{i_n^2} \cong \frac{4kT}{R_{\mathrm{att}}M^2} + \overline{i_{T1}^2} + \frac{4kT}{R_d}\left(\frac{C_i}{C_d}\right)^2 + \overline{e_{n,i}^2}\omega^2(C_i + C_{\mathrm{gate}} + C_{\mathrm{DUT}})^2 \quad (9)$$

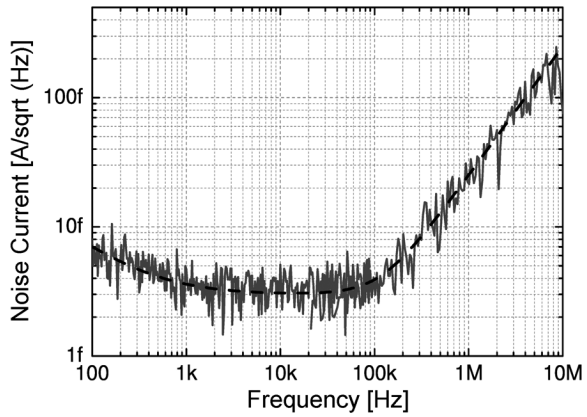

Fig. 10. Equivalent input current noise of the prototype shown in Fig. 3 operating with zero input current ($I_{\mathrm{DC}} = 0$) obtained by measuring the output voltage noise and dividing it by the measured frequency response. The dashed line is the theoretical prediction based on eq. (9). At low frequency a tail of flicker noise, due to the differentiator opamp, is present; the raise in the spectrum at higher frequencies is due to the total input capacitances.

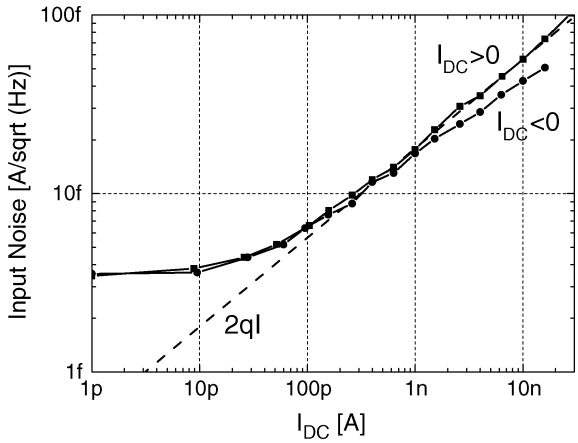

Fig. 11. White noise of the amplifier as a function of the dc input current measured at 3 kHz. The dashed line is the theoretical shot noise.

where $\overline{i_{T1}^2}$ is the current noise of the MOSFET T_1, $\overline{e_n^2}, \overline{i} \simeq (3\ \mathrm{nV})^2/\mathrm{Hz}$ is the noise voltage source of the operational amplifier $\mathrm{OP_{int}}$. The measured white noise is equivalent to the thermal noise of a 2 GΩ resistor; the 1/f noise at frequencies lower than 1 kHz is added by the differentiator stage and therefore is independent from the input bias; at high frequency the noise increases as ω (rms), as previously discussed.

Fig. 11 shows how the lower limit of input noise in the white region of the spectrum is modified when I_{DC} increases over 10 pA due to the dc reset system. In this case the noise of transistor T_1 becomes dominant and increases with current, following the theoretical shot noise expected for a MOSFET operating in subthreshold regime or as a $p-n$ junction diode. For large negative input current instead, the transistor T_1 operates in inversion regime and the noise is correspondingly less than the shot noise. Note that, despite the increase of the noise level, when $I_{\mathrm{DC}} > 10$ pA the amplifier still has a better sensitivity than an opamp with a simple feedback resistor: only in the worst case, i.e., with the maximum input current ($I_{\mathrm{DC}} = 10$ nA), the noise level ($60\ \mathrm{fA}\sqrt{(\mathrm{Hz})}$) would become comparable to the thermal

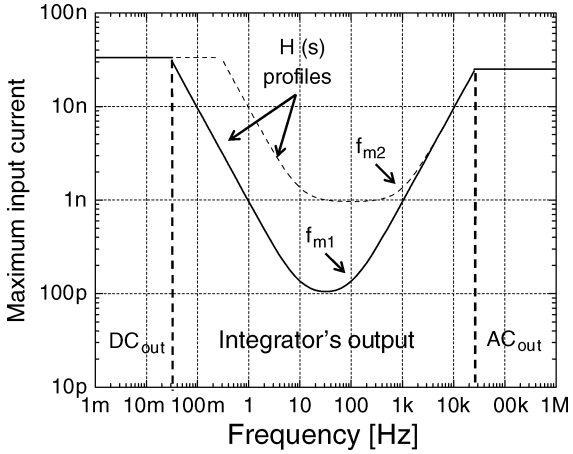

Fig. 12. Maximum input current that can be accepted by the transimpedance input node as a function of the frequency of the input signal for a transition frequency of $f_{m1} = 100$ Hz (continuous line) and for $f_{m2} = 1$ kHz (dashed line).

noise of the maximum physical resistor that can be integrated on a chip (that is some MΩ).

B. Dynamic Range

The maximum amplitude of the input current, reported in Fig. 12, depends on the frequency and is limited by three different nodes: the output of the amplifier $H(s)$ ($\mathrm{DC_{out}}$ in Fig. 3), the signal output $\mathrm{AC_{out}}$ or the integrator's output. To maximize the dynamic range all these nodes have been designed with a rail-to rail ($V_{\mathrm{supply}} \pm 1.5$ V) voltage swing. At very low frequencies, where the amplifier $H(s)$ has an high gain, both the integrator's output and the $\mathrm{AC_{out}}$ are insensitive to the input current and the input dynamic range is limited by the saturation of the $\mathrm{DC_{out}}$ node at the value $1.5\ \mathrm{V}/R_{\mathrm{dc}} \cong 25$ nA. This condition holds as long as the gain of the amplifier $H(s)$ is larger than 1, that is up to few tens of mHz. Above this limit the integrator output node becomes the limiting node. The maximum input current first decreases with frequency reaching the minimum value of $1.5\ \mathrm{V}/(R_{\mathrm{dc}}\gamma) \cong 100$ pA when the attenuation γ of $H(s)$ is maximum, i.e., for frequencies greater than the zero f_z (10 Hz) of the amplifier $H(s)$. Then, for frequencies greater than 100 Hz, the dc feedback network of the integrator stage is no longer active and the maximum input current is limited by the frequency response of the integrator at the value $|I_{\mathrm{max}}| = 1.5\ \mathrm{V} \cdot (2\pi f C_i)$. Finally, when the differentiator gain becomes larger than 1, the saturation of the transimpedance output voltage ($\mathrm{AC_{out}}$) becomes dominant and the maximum input current is given by $1.5\ \mathrm{V}/60\ \mathrm{M\Omega} = 25$ nA, where 60 MΩ is the total transimpedance gain. Note that a higher value of V_{supply} ($V_{\mathrm{supply}} > 1.5$ V) would proportionally increase the dynamic range of the input current, so as would do an increase of C_i. This latter would also produce an extension of the integrator-differentiator bandwidth (f_m) at low frequency (see (2)) at the expense of a reduced signal gain.

The dashed line reported in Fig. 12 is instead the maximum input amplitude when the transition frequency f_m is set at 1 kHz. The reduced attenuation of the amplifier $H(s)$ leads to an increased maximum input current.

VI. Conclusion

The paper has presented a transimpedance amplifier based on integrator-differentiator scheme featuring a feedback network to drain standing currents from the DUT as high as ±25 nA. This feedback network is advantageous with respect to a fixed value resistor in the integrator stage as it adapts its noise contribution to the amount of standing current: when $I_{\mathrm{DC}} = 25$ nA the noise introduced is equivalent to that of a resistor of 1.6 MΩ and correspondingly decreases as I_{DC} decreases, until it reaches a level of few $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ (up to 100 kHz) as would be obtained by a resistor of 1.8 GΩ. The key element of the feedback network is a topological solution to implement very high value resistors up to 300 GΩ, showing good linearity, noise limited by the shot noise, and bidirectionality of the current. The high sensitivity of the transimpedance amplifier combined with a bandwidth extending from 100 Hz to few MHz with highly stable gain and an auxiliary output to monitor also the DC-100 Hz frequency range, show the flexibility and suitability of the circuit in measuring current signals from nanodevices with high resolution. In particular, the chip can replace a standard discrete-components transimpedance amplifier in the applications where the submillimeter size can be beneficial to reduce the stray capacitance of the input connection, such as in the case of mounting the circuit directly on the probe of a current-sensing atomic force microscope [22], or to increase the number of parallel measurements, such as in the ion-channel experiments using an array of planar electrodes [23].

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