A 170-dBΩ CMOS TIA With 52-pA Input-Referred Noise and 1-MHz Bandwidth for Very Low Current Sensing

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***Abstract*— A fully integrated current sensing interface chip employing a capacitive-feedback transimpedance amplifier (TIA) is presented. A robust dc current removal block is proposed to prevent the dc portion of the input current from saturating the output voltage. This block allows the TIA to operate in the presence of a wide range of input dc currents, and the cancellation loop is designed to enhance its stability. The TIA is fully integrated in a standard 0.13 μm CMOS technology, and a gain of 170 dBΩ is achieved without requiring any off-chip resistors. The integrated input-referred current noise of the interface circuit is 0.4, 3.8, and 52 pA_{RMS} within 0.01, 0.1, and 1 MHz integration bandwidths, respectively.**

***Index Terms*— Biomedical, DNA sequencing, medical, Transimpedance amplifiers.**

I. Introduction

VLSI silicon chips are widely used in various sensor applications. Among them are many biomedical applications that require sensing of nanoamp and subnanoamp currents. These applications range from spectroscopy, electrophysiology, and life sciences [1], [2] to, more recently, nanopore-based integrated systems for DNA analysis [3], [4]. Ultralow noise transimpedance amplifiers (TIAs) are a key block in these current-sensing applications. Moreover, such TIAs have also been widely utilized to study the characteristics of ion channels in living cellular membranes [2], and are also well suited to other applications such as in the detection of single molecules using nanopores, the electrical characterization of nanosamples by means of atomic force microscopes, or the electrical read-out of quantum bits [5].

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For such applications, where small signal currents must be precisely recorded, shunt-shunt feedback TIAs have been widely used due to their relatively simple circuit architecture, low input-referred noise, and small input capacitance [6]. In this topology, the feedback circuit can be resistive or capacitive in nature. Additionally, it can be implemented by a more complex hybrid circuit. In the resistive feedback configuration, the resistance must be large enough (i.e., gigaohm range) in order to ensure high gain and low input-referred current noise. In order to be integrated within the circuit, such a resistor consumes a large chip area and usually becomes a fabrication limited parameter, leading to the wide use of a pseudo-resistive structure that employs an active device as the feedback network [3]. This approach, however, results in a resistance value that is inversely proportional to the input dc current, resulting in a variable TIA gain and bandwidth that are undesirably input dependent. An additional linearization circuit for the pseudo-resistor is presented in [3] to mitigate this issue. Alternatively, the capacitive feedback architecture [7] contributes less noise, is independent of input dc current conditions, and does not require a significant chip area. However, the capacitor voltage must be reset regularly to mitigate the integration of the input dc current that can saturate the TIA. This resetting results in clock feedthrough and discontinuous measurements [8], [9]. To avoid the reset phase, a dc current removal block is presented in [8] to remove the dc portion of the input current. However, the feedback loop implemented with this block includes several poles due to the presence of many nodes and stages in the loop. This complicates loop design because of stability issues. In [10], a semi-digital technique using digital-to-analog converters (DACs) is used to remove the dc portion of the input current, but this method requires a large off-chip resistor.

An emerging current sensing application that requires an ultralow noise TIA with robust dc cancellation is nanopore-based DNA analysis. This application has the potential to increase the sequencing speed and reduce the cost in comparison with conventional electrochemical DNA analysis techniques [11]. In this technique, a dc command voltage, V_{CMD}, is applied across a nanopore placed in an ionic solution, as depicted in Fig. 1. This command voltage is the difference between a dc nanopore bias voltage V_C and V_{CM}, the common-mode voltage of the TIA's input. Due to the negative charge of the DNA backbone, the command voltage results in a DNA strand passing

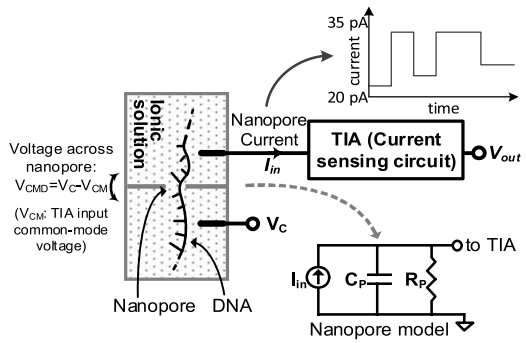

Fig. 1. Conceptual diagram of current sensing using the proposed TIA in a nanopore-based DNA analysis application. In this application, the electrical current I_{in} depends on the DNA base passing through the nanopore, and enables the reading of the DNA sequence.

through the nanopore. Notably, it also generates a constant (i.e., dc) ionic current of ∼100 pA in biological nanopores and up to a few nanoamps in solid-state nanopores when no DNA passes through [3]. The current flowing through the nanopore, I_{in}, is altered depending on the DNA base passing through it [12]. This is due to the DNA-base-specific change in the nanopore resistance. Thus, measuring the variation in I_{in} enables the reading of the DNA sequence. Since this current variation is very small, typically in the subnanoamp range, an ultralow noise and very high gain TIA is required to provide an amplified voltage with sufficient SNR. Moreover, the translocation rate of the DNA going through the nanopore is of about 1–5 μs per base [13], [14]. Therefore, a relatively high circuit bandwidth of the order of 1 MHz is needed to detect the current variations.

Accordingly, this paper introduces a fully integrated ultralow-noise TIA architecture for biomedical applications that is fabricated in IBM standard 0.13 μm CMOS technology. The architecture is optimized to meet the stringent bandwidth and noise performance requirements of the emerging nanopore-based DNA analysis application [15]–[17]. To demonstrate the advantages of the proposed architecture for this emerging biomedical application, an equivalent *RC* nanopore model is used to characterize the performance of the TIA. In order to minimize the TIA noise, capacitive feedback is used, as opposed to resistive feedback [18]. However, as mentioned earlier, the resulting integrating response requires an input dc current removal block to prevent the TIA from saturating. Thus, a robust low-complexity dc current removal block is proposed. In addition, the design is optimized for ultralow noise performance and optimally matches the nanopore model capacitance to improve supply noise rejection.

This paper is organized as follows: Section II presents the proposed TIA, Section III describes the noise minimization strategy for the proposed TIA, and Section IV presents the measurement results of the fabricated integrated circuit.

II. Proposed Transimpedance Amplifier

Fig. 2 shows the block diagram of the proposed TIA, composed of a capacitive feedback integrator, a resistive feedback differentiator, and a dc current removal block. The differentiator must be cascaded after the capacitive feedback integrator in order to obtain a flat frequency response. An *RC* network is used to model the nanopore, which can represent either a biological or a solid-state nanopore, as described in [3] and [19]. This nanopore model features a resistor that increases when the diameter of the pore is reduced [20]. As shown in Fig. 2, a capacitor C_B is added on-chip to balance the inputs of the integrator such that it matches the modeled nanopore capacitance, C_P. This input balancing improves the supply rejection of the integrator. Based on simulation results, removing C_B degrades supply rejection by 12 dB. Moreover, omitting C_B causes the noise of the tail transistor in the opamp of the integrator to noticeably increase the total input-referred noise of the TIA by 25%. Details pertaining to the impact of C_B on noise are given in Appendix I. In addition, a large resistor R_B is implemented as an on-chip pseudo-resistor to bias the input of the integrator to the common-mode voltage, V_{CM}.

It is worth mentioning that, as shown in Fig. 2, the gain of the TIA is (20 pF/100 fF) · 2 MΩ. Here, both of the 20 pF and 100 fF capacitors are on-chip and realized using factory-available metal-insulator-metal (MIM) capacitors that are matched in the layout. Hence, any drift that occurs on-die will affect both capacitors similarly and their ratio will not vary significantly. The reported mismatch value between capacitors is less than 1% in this technology. However, the absolute value of the resistor can have a 20% error, and hence, the gain value of the TIA is mostly sensitive to the absolute value of the 2 MΩ resistor.

A. Integrator and Differentiator Opamps

Fig. 3 presents a schematic of the opamp used to implement the integrator, labeled as Amp1 in Fig. 2. The opamp is composed of two stages with the first stage using matched kxres resistors (BEOL thin film resistors) loads in order to reduce the flicker noise, and the second stage using an active load to provide a single-ended output. As the first stage of the opamp has relatively low output impedance, the dominant pole of this opamp is generated at the output of the second stage as it is connected to the large differentiator capacitor. Both the poles are well split and, accordingly, no frequency compensation is required. Fig. 4 shows the loop gain and loop phase of the integrator opamp, Amp1, when used with a 100 fF feedback capacitor and a nanopore capacitance of 6 pF. Here, the loop gain is the open-loop gain of Amp1 multiplied by the feedback factor (β) given by $\beta \approx C_F/(C_{\text{Amp1}} + C_P) \approx 0.01$, where C_{Amp1} is the input capacitance of Amp1. Considering a 560 V/V simulated open-loop gain for Amp1, this results in a 15.1 dB loop gain at midband frequencies. A stable phase margin (PM) of 99° can be observed for this configuration.

The outputs of the first stage of Amp1, V_{O+} and V_{O-}, can exhibit a dc mismatch because of the low loop gain of the dc feedback loop. This will be further detailed in the following section. As a result, 10 pF decoupling capacitors between the two stages of Amp1 are utilized to prevent these mismatches from saturating the second stage. The second stage of this opamp is biased separately, using two large pseudo-resistors. The pole introduced by the decoupling capacitor and the pseudo-resistor is set to be at 10 Hz since the low frequency cutoff of this TIA is usually set at 100 Hz [8].

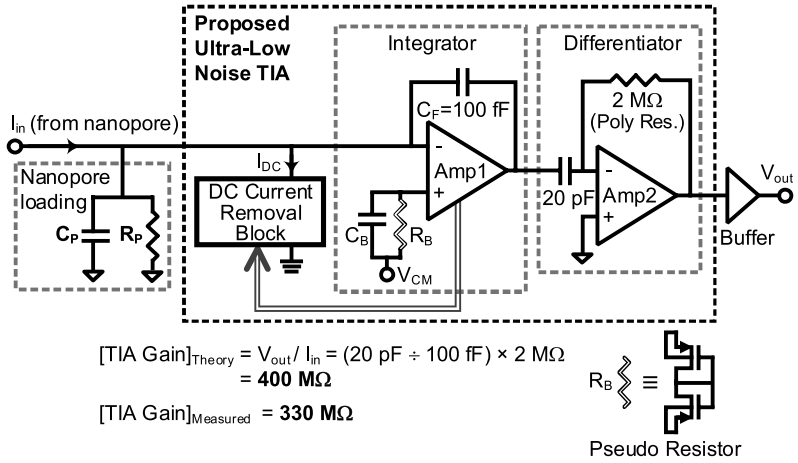

Fig. 2. Proposed ultralow noise TIA architecture consisting of an integrator cascaded with a differentiator. The dc current removal block sinks the input dc current and prohibits the integrator from saturation. The on-chip buffer stage has a gain of 5 V/V in order to reduce the input-referred noise of the oscilloscope used to measure V_{out}. The reported TIA gain of 330 MΩ does not include this added gain.

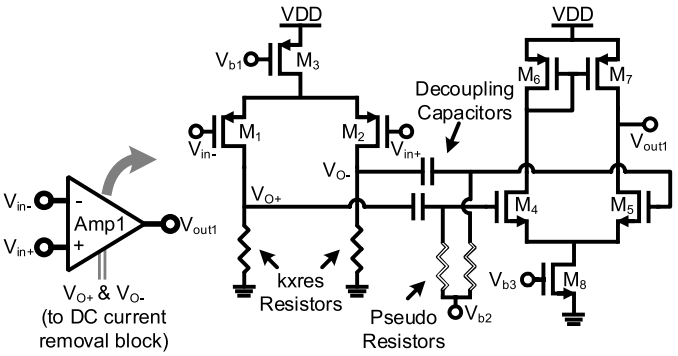

Fig. 3. Op-amp circuit used within the integrator (labeled Amp1). Here, V_{O+} and V_{O-} are inputted to the dc current removal block to achieve a robust low-frequency feedback loop.

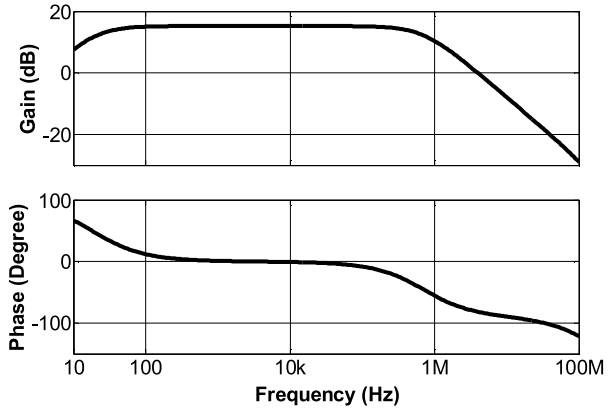

Fig. 4. Loop gain and loop phase of the integrator opamp, Amp1.

This margin allows to compensate for process variation of the decoupling capacitors or pseudo-resistor values.

The simulated Amp1 power consumption is 24 mW, including its bias circuit. Its gain, slew-rate, and unity gain bandwidth are of 560 V/V, 25 V/μs, and 190 MHz, respectively. Here, the first stage of Amp1 has a gain of 13 V/V and the second stage has a gain of 43 V/V. Note that, similar to other opamps in feedback, the value of the gain, *SR*, and bandwidth of Amp1 should be maximized to guarantee the proper input-current integration on C_F. Here, the minimum bandwidth requirement such that a 1 MHz input signal is not deteriorated by the opamp bandwidth is 1 MHz / β (i.e., 100 MHz). The minimum value of *SR* such that no slewing occurs for a full-swing 1 MHz sinewave at the output of the integrator is $2\pi A$ 1 MHz (i.e., 9.5 V/μs), where A is the maximum amplitude of the signal at the output of the integrator.

The differentiator is realized using an opamp with a 20 pF capacitor at its input, and a 2 MΩ resistor in its feedback, as shown in Fig. 2. The opamp used in the differentiator, labeled as Amp2, is a conventional two-stage opamp with a differential pair as its first stage and a common source as its second stage. The opamp bias current can be changed off-chip to control its bandwidth as will be discussed in Section IV. Note that, in this TIA, the main source of noise is the integrator opamp (Amp1), as the noise of the differentiator is effectively divided by the gain of the integrator.

B. DC Current Removal Block

In order to prevent the saturation of the integrator stage from an input dc current, a dc current removal block is required. Typically, dc current removal blocks are designed using a low-frequency feedback path that senses the output dc value and sets it to a reference value [8]. However, when connected to the opamp output, such a feedback path can have a very high loop gain and several poles resulting in instability or stability that may not be robust. In [8], this low-frequency feedback path is implemented using several amplifiers, a large capacitor, and a large linear resistor which contribute several poles to the feedback path, rendering its design more complex. In order to noticeably simplify this block while maintaining its robustness, Fig. 5(a) shows the proposed dc current removal block that is composed of a differential pair with diode-connected loads, a low-pass filter (LPF), and an output transistor, M_C. In contrast to sensing the output voltage of Amp1, this circuit senses the outputs of its first stage, V_{O+} and V_{O-}, differentially, and ensures that their dc biases are identical. Thus, the loop gain and the number of loop poles

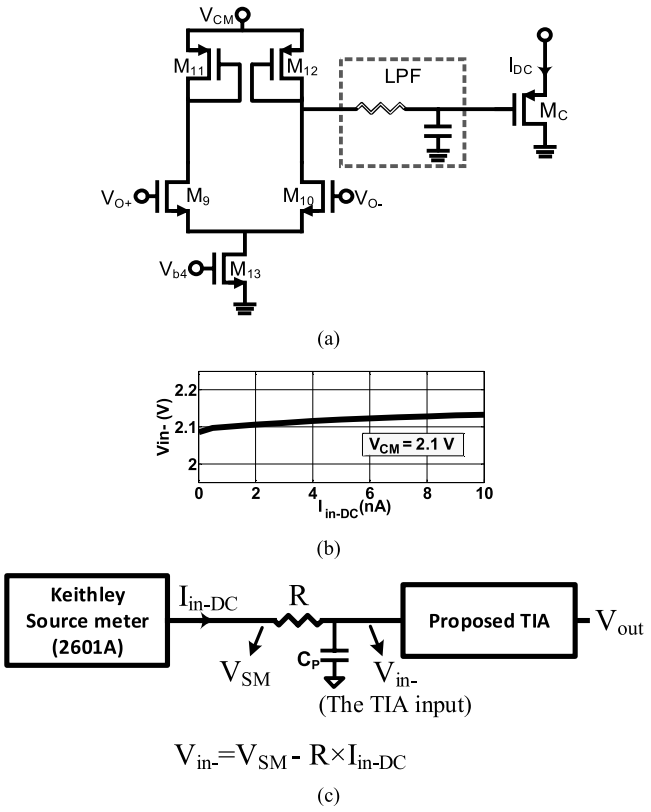

Fig. 5. (a) DC current removal block (not showing the first stage of Amp1). (b) Measured negative input of the TIA in response to a relatively wide range of injected input dc currents, $I_{\text{in-dc}}$, outlining the robustness of the dc current removal block. (c) Required test setup and the relation used to calculate V_{in} for different values of $I_{\text{in-dc}}$.

of the low-frequency feedback loop are reduced, and stability conditions are improved. Additionally, the differential nature of the dc current removal block does not require a reference common-mode value to be generated in order to compare with. The dc current removal block itself has no additional gain since the load of its first stage is diode connected and PMOS transistor M_C serves as a source follower. Thus, the gain of this dc feedback loop is of the order of the gain of the first stage of Amp1. Specifically, the dc current removal block has a gain of 0.5 V/V and the first stage of Amp1 has a gain of 13 V/V. The resulting low loop gain of 6.5 V/V further improves the loop stability. Note that M_C could be designed using an NMOS in a common source architecture, however, it would increase the loop gain which results in instability.

The very low bandwidth (i.e., a few Hz) of this dc feedback loop is controlled by the on-chip *RC* LPF implemented by a 1.2 pF capacitor and a large pseudo-resistor, as shown in Fig. 5(a). Transistor M_C sinks a dc current to set the negative input voltage level of the integrator to V_{CM}.

The power supply of the dc current removal block is set to V_{CM}, in order to simplify its biasing. Here, the current of M12 is mirrored to M_C. As the source of transistor M_C is biased at V_{CM}, the sources of M11 and M12 must be biased at V_{CM} as well. This ensures symmetric mirroring from M12 to M_C. A minimum size transistor is used for M_C (0.5 μm/0.4 μm) and, hence, its loading on the TIA input is negligible.

Fig. 5(b) shows the TIA negative input voltage that is measured for different relatively large dc current values of up to 10 nA injected at the input, $I_{\text{in-dc}}$. For all tested currents, the dc current removal block prevents the saturation of the integrator by holding its negative input to V_{CM}, outlining the robustness of the dc current removal block. Here, the TIA negative input voltage should be set at V_{CM}, but there is a small inaccuracy on its value that is due to the small loop gain of the dc current removal feedback loop (i.e., 6.5 V/V), as was previously mentioned in Section II-A. Note that this inaccuracy translates into a variation in the command voltage of the nanopore. For instance, this command voltage change for a relatively large 4 nA input dc current, is below 10 mV, as shown in Fig. 5(b). Considering a 0.5 GΩ resistance for the nanopore, this input current corresponds to a 2 V command voltage. Thus, this variation results in only 0.5% error on the command voltage and does not limit the DNA sequencing resolution. For the same input current, higher nanopore resistance results in a higher command voltage and, hence, a smaller error. Moreover, command voltages are typically of the order of 100 mV to a few hundred millivolts [2], [3], which is much larger than this variation. Furthermore, this variation is almost constant for a specific nanopore dc current. Hence, it does not limit the DNA sequencing resolution. The TIA negative input measurement is carried out over a few hours to confirm that no small dc current remains to cause slow saturation of the integrator. This confirms that the dc current cancellation is complete even though the dc-current removal loop gain is small, resulting in an imprecise dc voltage at the negative input of Amp1 in Fig. 2, as measured in Fig. 5(b). This is because the residual current I_{RES} flowing into the negative input of Amp1 is integrated by the opamp and represents the error signal of the feedback loop setting the dc voltage at the negative input. Due to this integration, the dc gain of the current to voltage transfer function V_I/I_{RES} is infinite, and, because of the feedback, the residual current is zero at dc.

Fig. 5(c) outlines the test setup that was used to generate the varying dc current. Since V_{in} is a highly sensitive voltage, it cannot be measured directly. Accordingly, it is measured using the output voltage and current of a source meter and an accurate resistor ($R = 100$ MΩ).

As dc currents in nanopore-based DNA analysis flow out of the nanopore, this TIA was designed to cancel only dc currents that are flowing into its input, eliminating any noise contribution stemming from reverse dc current cancellation circuitry. Reverse dc current flow cancellation circuitry could be added in a similar fashion in order to tailor the circuit to applications requiring bidirectional dc current cancellation. Moreover, although the dc information of the input current signal is removed, it can still be directly measured by estimating the dc current of the M_C transistor. This can be done by adding a resistor at the drain of M_C, and measuring the associate voltage drop. This is not implemented in this design.

1) Small-Signal Behavior of the DC Removal Block: As was previously mentioned, the dc current removal block, including the first stage of Amp1, has a single ended gain A_{loop} of 6.5 V/V (16.3 dB). In Fig. 5(a), tail transistor M13 is biased in subthreshold, and transistors M9-M12 are sized such

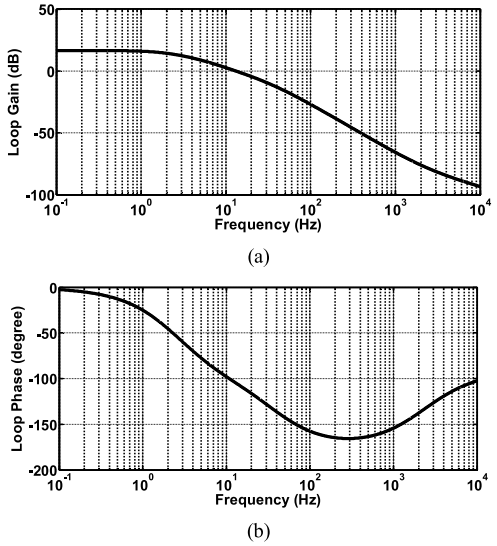

Fig. 6. DC current removal block (a) loop gain and (b) loop phase at a 300 pA input dc current.

that the transistors transcondunctance ratio in each branch is unity.

This loop has two low frequency poles. In Fig. 5(a), the *RC* LPF in the dc removal block produces the first pole P_1 at approximately 2 Hz, according to simulations.

The second pole of this loop is at the inverting input of Amp1, and is given as

$$P_2 = \frac{1}{(1/g_{mc}||R_{\text{pore}})(C_{\text{pore}} + A_{\text{Amp1}}C_F)}. \tag{1}$$

Here, g_{mc} is the transconductance of transistor M_C and A_{Amp1} is the midband gain of Amp1. Based on simulations, g_{mc} is around 10 nS at a 300 pA dc current, which results in a pole at 30 Hz. Here, $A_{\text{Amp1}}C_F$ is the miller capacitance stemming from C_F at the inverting input of Amp1.

Considering that the unity gain frequency of the loop f_u is equal to $A_{\text{loop}}P_1$, f_u is calculated to be of 12 Hz. Since this frequency is well below the second pole P_2, it guarantees a good PM for the dc current removal block loop.

Fig. 6 shows the loop gain amplitude and phase responses of the dc current removal block, illustrating a good PM at a 300 pA dc current.

As M_C is in weak inversion, its transconductance is given as

$$g_{mc} = \frac{I_{\text{DC}}}{nV_T} \tag{2}$$

where $n = 1.2$–1.5, I_{dc} is the dc current of M_C, and V_T is the thermal voltage of 25 mV at room temperature. Thus, from (1) and (2), a decreasing input dc current I_{dc} pushes the second pole to a lower frequency and reduces the PM. In the worst case for stability, when I_{dc} becomes zero, g_{mc} becomes very low. Thus, the pore resistance will dominate the second pole. Based on simulations, in such a situation, this pole is placed at around the same location as the first pole (i.e., $\approx$2 Hz). In this case, to calculate the PM, the unity-gain frequency of the loop needs to be calculated as

$$\frac{A_{\text{loop}}}{1 + \left(f_u/P_1\right)^2} = 1 \tag{3}$$

where

$$f_u = P_1(\sqrt{A_{\text{loop}} - 1}). \tag{4}$$

Since A_{loop} is 6.5 V/V, f_u then becomes 3 Hz. Here, the PM is given as

$$PM = 180 - 2\tan^{-1}\left(f_u/P_1\right). \tag{5}$$

Given $f_u = 3$ Hz and $P_1 = 2$ Hz, the PM becomes 46°, yielding that even in the worst stability case, the loop will still yield good stability. Interestingly, considering a worst case of 30° PM, and solving (4) and (5) results in an A_{loop} of 8.25 V/V. Considering this gain as the maximum gain to achieve good stability, the selected gain of 6.5 V/V is 27% below this margin to assure stability in all corners.

Note that the values of the first and the second poles can vary due to the nonlinear behavior and variations of the pseudo-resistor, the input dc current, the pore resistance, and capacitance. However, as shown, even in the worst stability case that both poles fall at the same location, the loop still had sufficient PM. Thus, a variation of the first and second poles will not render it unstable. The guaranteed stability of the dc current removal feedback loop is an important consequence of its *low loop gain*.

2) Effect of DC Current Removal Block on Noise Performance: The noise generated by the dc current removal block is filtered by the RC LPF shown in Fig. 5(a) as its bandwidth is of the order of 2 Hz, much lower than the targeted cutoff frequency (i.e., >100 Hz). Particularly, most of the pseudo-resistor kT/C noise falls below the required low cutoff frequency of the targeted application (i.e., 100 Hz). Accordingly, only the current noise generated by M_C is directly added to the input current. As M_C operates in deep subthreshold due to its very small dc current $I_{\text{in-dc}}$, its total noise is almost equal to the shot noise generated due to the flow of I_{dc} [3], which has a power spectral density given as [21]

$$i_{\text{in}}^2(f) = 2qI_{\text{in-DC}}. \tag{6}$$

Note that M_C could be implemented using an NMOS device using the opposite differential pair outputs of the dc current removal block shown in Fig. 5(a), in order to ensure negative feedback of the dc current removal loop. However, this would increase the loop gain, and could result in instability. Moreover, the shot noise is similar for both PMOS and NMOS devices. Thus, there is no noise penalty of using a PMOS transistor for M_C instead of an NMOS transistor. Moreover, at high $I_{\text{in-dc}}$ values, the flicker noise of M_C can couple to the TIA input since the transconductance of M_C increases at high $I_{\text{in-dc}}$. Here, the use of a PMOS device minimizes this flicker noise due to the lower transconductance achieved.

Note that M11 could be removed and the drain of M9 could be shorted to the supply. However, by adding M11, which does not add any significant complexity, the amplifier becomes fully symmetric, and, potentially, can have better common-mode noise behavior.

3) Effect of DC Current Removal Block on Gain Performance: As mentioned previously, an approach that can be used to set the dc value of the TIA input is to use an extremely

TABLE I
MAIN TIA INTEGRATED NOISE CONTRIBUTORS*

Transistors	100 kHz BW	1 MHz BW
M1 and M2 (Flicker)	59%	20%
M1 and M2 (Thermal)	13%	56%
kxres Resistors	1.8%	8%
M4 and M5 (Flicker)	6%	3%
M4 and M5 (Thermal)	1.5%	6%

*As reported by the Spectre circuit simulator.

large resistor in the feedback of the TIA (i.e., gigaohm range). This extremely large resistor is usually implemented using a pseudo-resistor. This pseudo-resistor sinks the input dc current and steers it to the output. However, the pseudo-resistor value reduces as the input dc current is increased, and as a result, the TIA gain and bandwidth are altered because of the feedback change, causing a detrimental performance variation for different input dc current levels. Alternatively, in the proposed dc removal block, transistor M_C does not affect the TIA gain as long as its output impedance is higher than the input impedance of the TIA. This ensures that the input ac current will go into the TIA and be amplified, instead of going through M_C to ground. The output resistance of transistor M_C, r_{oc}, is related to its transconductance such that $r_{oc} \sim 1/g_{mc}$. As M_C is operating in subthreshold, its transconductance is given by (2) with $I_{\rm DC} = I_{\text{in-dc}}$. Therefore, the output resistance of transistor M_C is lowered by the input dc current $I_{\text{in-dc}}$ and care must be taken to ensure that it remains sufficiently high with respect to the input impedance of the TIA. The TIA input impedance can be derived from the miller effect of its feedback impedance implemented by C_F, and is given as

$$Z_{\rm in}(f) \cong \frac{1}{2\pi f C_F A_{\rm Amp1}} \tag{7}$$

where $A_{\rm Amp1}$ is the midband gain of Amp1 and f is the frequency. At frequencies where the TIA is expected to operate (i.e., $>$ 100 Hz), this input impedance must be minimized (e.g., by increasing $A_{\rm Amp1}$). This facilitates design such that r_{oc} remains larger than $Z_{\rm in}$. Considering $A_{\rm Amp1} =$ 560 V/V in the proposed design, the lower bandwidth of 100 Hz is guaranteed up to $I_{\text{in-dc}} = 1.5$ nA. For higher dc current values, a digital gain correction at very low frequencies is used to compensate for the reduced gain due to the impedance of M_C that is sufficiently low to load $Z_{\rm in}(f)$. This design can be further improved by increasing $A_{\rm Amp1}$ such that no gain correction at low frequencies is needed at higher dc input currents.

III. NOISE ANALYSIS

Typically, the noise performance of a biomedical current sensing application such as nanopore-based DNA analysis is limited by the noise performance of the current sensing circuit (i.e., the TIA), as the sensor (i.e., nanopore) thermal noise and flicker noise are typically considered to be negligible [2]. In the proposed TIA, the main source of noise is the first stage of Amp1, as the noise of its second stage and the differentiator are effectively divided by the gain of this first stage. In [18] and [22], the value of the input-referred current noise spectrum of a TIA is calculated. Considering the thermal noise of the first stage of Amp1, the input-referred current noise power spectral density is given as [18], [22]

$$i_{\rm in}^2(f) = \frac{16KT}{3g_m}(1+F)(C_1+C_g)^2(2\pi f)^2 \tag{8}$$

where $C_1 = C_P + C_F$, C_F is the feedback capacitance, C_P is the modeled nanopore capacitance, g_m, and$C_g$are the transconductance and the effective gate capacitance of the input transistors of Amp1, M_1, and M_2. Here, K, T, and F are the Boltzmann's constant, absolute temperature, and a factor to include the extra noise generated by other opamp components, respectively. In (8), the noise of the second stage and any subsequent stages of the opamp are neglected, since their noise impact is reduced by the gain of the first stage of the opamp when referred to the input. Note that (8) does not include the noise from M_C, expressed in (6), which can simply be added if noise performance with an input dc current is wanted. For this resistively loaded first stage, F can be derived by normalizing the input-referred thermal noise of the kxres resistors to the input-referred thermal noise of the input transistors. Referring the thermal noise of the kxres resistors (i.e., $4KTR_{\rm kxres}$) to the inputs using the power gain of the first stage (i.e., $g_m^2 R_{\rm kxres}^2$), and referring the thermal noise current of the input transistors (i.e., $8KTg_m/3$) to their gates yields

$$F = \frac{3}{2g_m R_{\rm kxres}}. \tag{9}$$

The input transistors have the minimum length available in order to maximize their transconductance g_m and minimize their input-referred thermal noise. Table I shows the main integrated input-referred noise contributors in the TIA, as reported from Spectre noise simulation, where the transistors in the input pair of Amp1 are shown to be the most significant contributors. The thermal noise of the input transistors becomes dominant at a high integration bandwidth (i.e., 1 MHz), while at a low integration bandwidth (i.e., 100 kHz), their flicker noise becomes the dominant source. Moreover, based on Table I, the ratio of the thermal noise contribution of the kxres resistors and the thermal noise of input transistors M1 and M2 [i.e., factor F in (9)] is 0.14. This is in line with what is predicted by (9), considering that the gain of the first stage of Amp1 $g_m R_{\rm kxres}$ is of 13 V/V, as discussed in Section II-B.

IV. MEASUREMENT RESULTS

This TIA was implemented in IBM standard 0.13 μm CMOS technology and operated at a 3.3 V supply with a power consumption of 30 mW, which is suitable in high performance applications such as nanopore DNA analysis [3]. The die micrograph is shown in Fig. 7, with the TIA subblocks outlined. The circuitry occupies an active area of 250 μm $\times$ 800 μm. Both the integrator and differentiator are operating from the same supply voltage. High-voltage 3.3 V transistors were used due to their better simulated noise performance. Since the designed gain of this TIA is

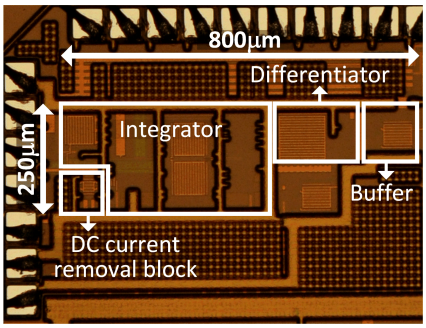

Fig. 7. Die micrograph of the fabricated TIA with outlined subblocks.

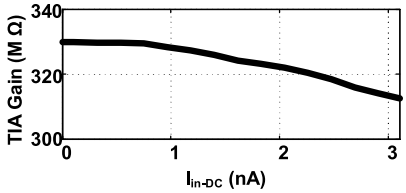

Fig. 8. TIA gain measured at 1 kHz versus the injected input dc current, $I_{\text{in-dc}}$, showing the negligible effect of the dc current removal block on the gain.

very high (see Fig. 2), it is prone to instability or saturation caused by insufficient output to input isolation or external input noise. Thus, both of the inputs of Amp1 were bonded to the package such that their bond wires were adjacent, even if the positive input is not used on the PCB, and the output was bonded at the other side of the package. This allows for the external noise present on the input to be rejected as common-mode noise and it precludes from instability due to output to input feedthrough. Moreover, in order to report consistent measurement results, the TIA was shielded and environmental effects were suppressed by performing all of the tests in a Faraday cage.

As previously mentioned, the nanopore was modeled with a capacitor and resistor, $C_P = 6$ pF and $R_P = 10$ GΩ, both implemented on the test PCB.

The TIA gain was measured to be of 330 MΩ or 170 dBΩ. Fig. 8 shows the TIA gain versus the injected input dc current, $I_{\text{in-dc}}$. At low dc current values, the output impedance of the dc current removal block is very high, such that the gain is not affected by this block. However, as explained in Section II-B, when the dc current increases, some gain reduction is expected. As shown in Fig. 8, this reduction in gain is relatively small even in the presence of a relatively large input dc current (i.e., a 5% gain reduction in the presence of a 3 nA dc current), confirming the negligible effect of the dc current removal block on the TIA gain. Moreover, this validates the dc current removal block operation such that the saturation of the integrator stage is prevented.

In order to measure the input-referred current noise spectrum, the differentiator bandwidth is reduced according to the TIA bandwidth of interest through its opamp bias current, thus lowering the noise-related output swing of the differentiator and output buffer. This leads to improved noise performance as the reduced signal swing improves the linearity of these stages and, hence, prevents out-of-band noise from folding back to lower frequencies inside the band of interest. The output of the TIA is sampled using an oscilloscope

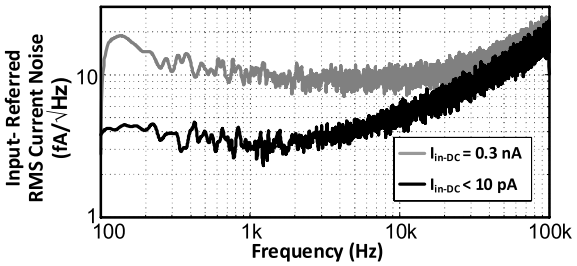

Fig. 9. Measured TIA input-referred RMS current noise spectrum, when connected to a 6 pF capacitor and 10 GΩ resistor external input load used to model a nanopore for two input dc current conditions: $I_{\text{in-dc}} < 10$ pA and $I_{\text{in-dc}} = 0.3$ nA. Here, the differentiator bandwidth is set to 300 kHz.

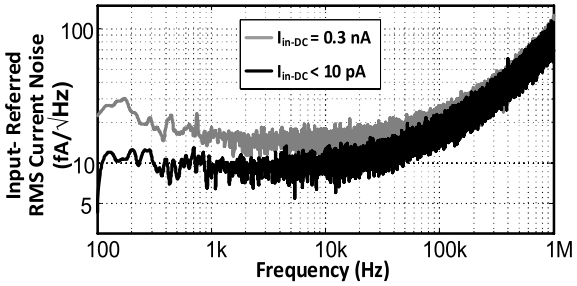

Fig. 10. Measured TIA input-referred RMS current noise spectrum, when connected to a 6 pF capacitor and 10 GΩ resistor external input load used to model a nanopore for two input dc current conditions: $I_{\text{in-dc}} < 10$ pA and $I_{\text{in-dc}} = 0.3$ nA. Here, the differentiator bandwidth is set to 2 MHz.

with a sampling frequency of 20 MS/s. The spectrum of the output is then divided by the transimpedance-gain frequency response to measure the input-referred current noise spectrum. Figs. 9 and 10 show the measured input-referred RMS current noise spectrum of the TIA with the nanopore modeled with a capacitor and resistor, $C_P = 6$ pF and $R_P = 10$ GΩ, both implemented on the test PCB. Note that the large resistance for this model is used to measure the baseline noise that is generated by the TIA. If a smaller resistor is used, the input-referred current noise of the resistor should be added to the reported noise values. The input-referred RMS current noise is plotted for two different dc input currents, $I_{\text{in-dc}}$: <10 pA and 0.3 nA. In Fig. 9, a band of interest of 100 kHz is considered while in Fig. 10, a band of interest of 1 MHz is considered. The differentiator bandwidth is set to 300 kHz for the 100 kHz band of interest measurement, and to 2 MHz for the 1 MHz band of interest measurement. The input-referred RMS current noise spectrum in Figs. 9 and 10 shows that flicker noise dominates at low frequencies while thermal noise dominates at higher frequencies, and is increasing linearly with frequency as is expected in such circuits [18] and as apparent from (8). Fig. 11 shows the measured transimpedance-gain frequency response of the TIA for the two different bandwidth settings of 300 kHz and 2 MHz, illustrating the uniformity of the achieved 170 dBΩ gain in-band.

The input-referred RMS current noise within 10 and 100 kHz integration bandwidths is calculated by integrating the current noise in Fig. 9. At a dc input current of <10 pA, the resulting measured integrated input-referred RMS current noise is of 0.4 pA_{RMS} and of 3.8 pA_{RMS} within 10 and 100 kHz integration bandwidths, respectively. At a dc input current of 0.3 nA, this current noise increases to 1.0 pA_{RMS}

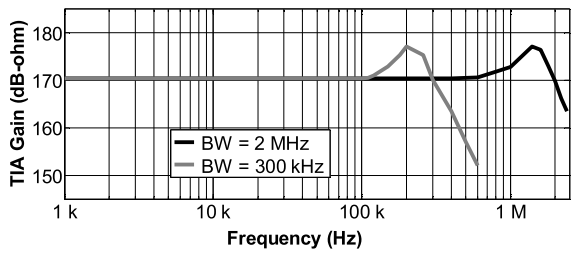

Fig. 11. Measured transimpedance-gain frequency response of the TIA for two different bandwidth settings. The bandwidth limits of 300 kHz and 2 MHz are used when the TIA output is digitally filtered to 100 kHz and 1 MHz, respectively. After the digital filtering, the TIA gain becomes flat within the entire 100 kHz or 1 MHz bandwidth.

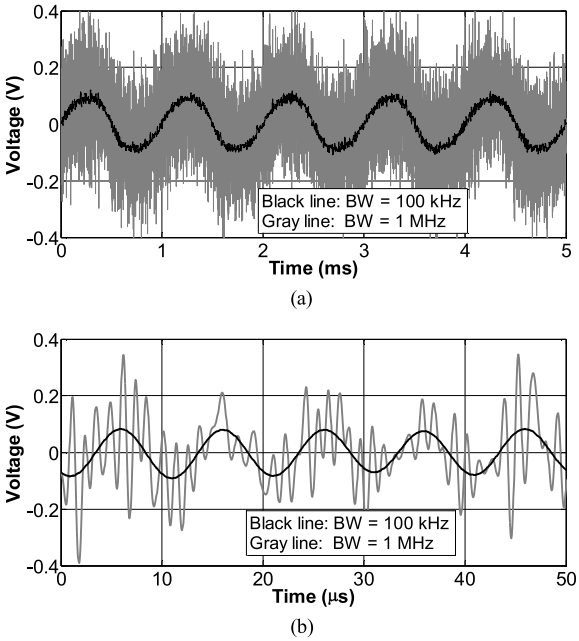

Fig. 12. Transient output of the TIA for a 100 $pA_{Pk\text{-}Pk}$ sinewave current input of (a) 1 kHz and (b) 100 kHz. The output is measured after the 5 V/V buffer stage and a digital bandpass filter is configured with 100 Hz-100 kHz and 100 Hz-1 MHz bandwidths. The output of Fig. 12(a) has a total harmonic distortion (THD) of < -30 dB.

and 4.7 pA_{RMS} within 10 and 100 kHz integration bandwidths, respectively. This increase is due to the greater injected shot noise, resulting from the input dc current passing through the dc removal block, as discussed in Section II-B. Note that this shot noise is a fundamental limit in a wide range of TIAs used for nanopore sequencing [8]. By integrating the current noise in Fig. 10 within a 1 MHz bandwidth, an integrated input-referred RMS current noise of 52 pA_{RMS} and 54 pA_{RMS} results for input dc currents of $<$10 pA and 0.3 nA, respectively. In the 1 MHz bandwidth, as a significant portion of the integrated noise stems from higher frequencies where noise is not dominated by the dc current removal block (i.e., the input dc current), the integrated noise performance for different input dc currents is relatively constant within the 1 MHz integration bandwidth. Fig. 11 shows the transient output of the TIA after the buffer stage shown in Fig. 2, and a digital bandpass filter implemented in MATLAB. Fig. 12(a) shows the output for a 1 kHz 100 pA_{Pk-Pk} input current, while Fig. 12(b) shows the output for a 100 kHz 100 pA_{Pk-Pk} input current. Two bandpass filter bandwidths are used to plot

TABLE II

COMPARISON OF THIS WORK WITH OTHER HIGH-PERFORMANCE STATE-OF-THE-ART TIAS INTENDED FOR NANOPORE-BASED DNA ANALYSIS

	Integrated Input-referred RMS Current Noise (pA_{RMS})			External Input Cap. (pF)	TIA Gain (MΩ)	Power Cons. (mW)	CMOS Tech. (μm)
	10kHz int. BW	100kHz int. BW	1MHz int. BW				
[3]	7.2	12.9	155	6†	100	45	0.13
[2]	5.87	N/A	N/A	N/A††	263	0.502	0.35
[22]	0.75	N/A	N/A	47	N/A	3.3	0.5
[23]	4.25	N/A	N/A	N/A†	257	0.437	0.35
[24]	5	N/A	N/A	10	25	0.3	0.5
This work	**0.4**	**3.8**	**52**	**6**	**330**	**30**	**0.13**

Note: As the TIA input load impacts noise performance significantly, this comparison considers TIAs that were connected to a nanopore or to a 6 pF or larger input load capacitance modeling the nanopore.
†Connected to a solid-state nanopore. ††Connected to an α-HL protein nanopore.

the outputs in Fig. 12: 100 Hz–100 kHz and 100 Hz–1 MHz. This input is generated using a voltage source and a series resistor connected to the input of the TIA. Note that the capacitive coupling across this series resistor can also affect the measurement, however, since the output signal is constant at frequencies around the 1 kHz input frequency, this capacitive coupling is negligible. Since the on-chip buffer stage has a gain of 5 V/V, the total gain from the TIA input current to buffer output voltage is observed to be of 330 MΩ × 5 V/V. Moreover, the amplitude of the 100 Hz–100 kHz filtered output for both input frequencies is comparable, as expected from the frequency response shown in Fig. 11.

Table II compares the performance of the proposed circuit to other published state-of-the-art TIA circuits for use in nanopore-based DNA analysis. In order to be representative, this comparison considers TIAs with measurements reported when the TIA is connected to a nanopore or to a nanopore model with a capacitance of at least ∼6 pF. This is done because of the strong effect of the nanopore capacitive loading on the noise performance of TIAs [18]. Compared to the state of the art, this TIA exhibits the most competitive noise performance within the 10 kHz, 100 kHz, and 1 MHz integration bandwidths. This performance within all these three integration bandwidths stems from the circuit's low and high frequency noise performance. While the power consumption of this design is higher than some of the designs in Table II, it remains lower than that of [3], while providing lower noise and higher gain. Notably, power consumption is typically not the limiting design metric in nanopore sequencing applications [8]. It should be noted that in this design, the bondwire, the PCB trace, the on-chip routing, and the gate capacitance of M1 can amount to 2.5 pF of extra capacitance on the input of the TIA. This capacitance is added to the nanopore capacitance and can have an impact on the TIA noise. This could be mitigated using more advanced packaging and integration techniques that reduce parasitics.

Fig. 13 compares the input-referred RMS current noise spectrum of this paper with that reported in [8] at frequencies

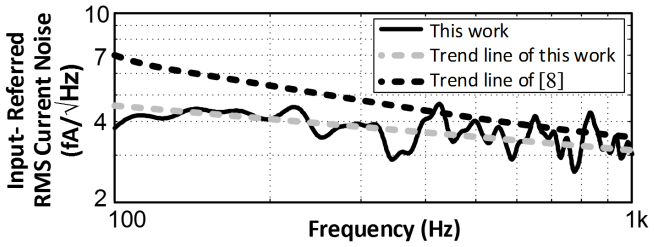

Fig. 13. Comparison of this paper with that reported in [8] at low frequencies.

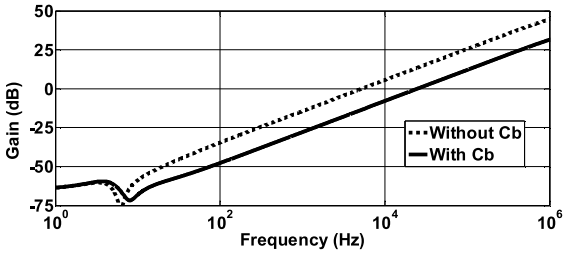

Fig. 14. Voltage gain from the supply to the TIA output, with and without the inclusion of capacitor C_b.

below 1 kHz. Notably, at lower frequencies, this work achieves lower noise, particularly lower flicker noise. At 1 kHz, similar performance is observed. It should be noted that the pore capacitance here is considered to be of 6 pF, while it is estimated as 0.6 pF in [8]. Thus, at higher frequencies, the noise in this paper will be much higher, as given by (8), and cannot be directly compared with that in [8].

V. Conclusion

This paper presented a fully integrated ultralow-noise TIA for biomedical current sensing applications, specifically demonstrating the architecture for the stringent requirements of nanopore-based DNA analysis. The TIA is composed of an integrator stage cascaded with a differentiator stage. The input impedance is optimized to attain low noise and high gain operation, and this is done while taking into account a typical nanopore model capacitance. This is an important consideration, as this capacitance significantly affects the performance of such circuits. Furthermore, an input dc current removal block and associated cancellation loop are included in the design and were shown to enable robust operation of the TIA for a wide range of input dc currents. When connected to a 6 pF and 10 GΩ nanopore model, the TIA integrated input-referred noise current is of 0.4 pA_{RMS}, 3.8 pA_{RMS}, and 52 pA_{RMS} within 10 kHz, 100 kHz, and 1 MHz integration bandwidths, respectively. The TIA was fabricated in IBM standard CMOS 0.13 μm CMOS technology to facilitate monolithic integration of the interface circuitry with a solid-state nanopore. This is desirable, as it can enhance circuit performance in DNA analysis applications.

Appendix

This appendix considers the noise contribution at the source (or gate) of the tail transistor, with and without including capacitor C_b.

Note that R_B is a very large resistor that does not affect the behavior of the circuit in the band of interest (i.e., >100 Hz). As such, its variability does not have a significant impact.

A. Equations not Including the Impact of Capacitor C_b

When not considering the impact of C_b, the following equations can be derived:

$$\frac{V_n}{V_s} = \frac{g_{m-\text{tail}}}{g_{m-\text{input}}} \tag{10}$$

$$V_{gsn1} \approx \frac{-C_P}{C_P + C_{gs}} V_s \tag{11}$$

and

$$V_{gsn2} = \frac{-1}{1 + R_b C_{gs} s} V_s \tag{12}$$

where V_n is the total noise at the source (or gate) of the tail transistor, V_s is this noise referred at the source of the input pair, V_{gsn1} is the gate–source voltage of inverting input (M1), and V_{gsn2} is the gate–source voltage of noninverting input (M2). Moreover, C_{gs}, $g_{m-\text{tail}}$, and $g_{m-\text{input}}$ are the gate–source capacitance of the input transistor, and the transconductances of the tail and input transistors, respectively. In deriving (11), it is assumed that the pore impedance is mostly dominated by the pore capacitance C_P.

From (12), V_{gsn2} tends to zero since R_b is of the order of gigaohms, and C_{gs} is of the order of picofarads. This causes a noise signal imbalance within the differential pair. Hence, the noise at the gate of the tail transistor is not removed differentially, causing it to deteriorate the output noise.

B. Equations Including the Impact of Capacitor C_b

When not considering the impact of C_b, the following equations can be derived:

$$\frac{V_n}{V_s} = \frac{g_{m-\text{tail}}}{2g_{m-\text{input}}} \tag{13}$$

$$V_{gsn1} \approx \frac{-C_P}{C_P + C_{gs}} V_s \tag{14}$$

and

$$V_{gsn2} \approx \frac{-C_b}{C_b + C_{gs}} V_s. \tag{15}$$

In deriving (15), it is assumed that the impedance of C_b is lower than its parallel pseudo-resistor, R_B. Thus from (14) and (15), when C_b is made equal to C_P, the noise at the gate of the tail transistor is rejected differentially, improving the output noise.

Fig. 14 shows the ac gain from the supply to the TIA output with and without the inclusion of C_b, showing a minimum 12 dB reduction in the gain level and, hence, a minimum 12 dB enhancement in the PSRR. The minimum improvement is at 100 Hz, which is the low cutoff frequency of this system.

It should be noted that if C_b is not exactly equal to C_P, the improvement in PSRR is less than 12 dB. For example, based on our simulations, if C_b is 60% of C_P, the simulated improvement is more than 6 dB. In addition, the rejection improvement remains above 3 dB even if C_b is only 20% of C_P.

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REFERENCES

[1] E. Kamrani, F. Lesage, and M. Sawan, "Low-noise, high-gain transimpedance amplifier integrated with SiAPD for low-intensity near-infrared light detection," *IEEE Sensors J.*, vol. 14, no. 1, pp. 258–269, Jan. 2014.

[2] J. Kim, R. Maitra, K. D. Pedrotti, and W. B. Dunbar, "A patch-clamp ASIC for nanopore-based DNA analysis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 285–295, Jun. 2013.

[3] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nature Methods*, vol. 9, no. 5, pp. 487–492, Mar. 2012.

[4] A. Balan *et al.*, "Improving signal-to-noise performance for DNA translocation in solid-state nanopores at MHz bandwidths," *Nano Lett.*, vol. 14, pp. 7215–7220, Nov. 2014.

[5] G. Ferrari, M. Farina, F. Guagliardo, M. Carminati, and M. Sampietro, "Ultra-low-noise CMOS current preamplifier from DC to 1 MHz," *Electron. Lett.*, vol. 45, no. 25, pp. 1278–1280, Dec. 2009.

[6] Y. Dong and K. W. Martin, "A high-speed fully-integrated POF receiver with large-area photo detectors in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2080–2092, Sep. 2012.

[7] H. M. Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1149–1157, May 2013.

[8] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance amplifier for high sensitivity current measurements on nanodevices," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, May 2009.

[9] M. Crescentini *et al.*, "A distributed amplifier system for bilayer lipid membrane (BLM) arrays with noise and individual offset cancellation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 3, pp. 334–344, Jun. 2015.

[10] C.-L. Hsu, A. G. Venkatesh, H. Jiang, and D. A. Hall, "A hybrid semi-digital transimpedance amplifier for nanopore-based DNA sequencing," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Oct. 2014, pp. 1–4.

[11] E. E. Schadt, S. Turner, and A. Kasarskis, "A window into third-generation sequencing," *Human Molecular Genet.*, vol. 19, no. R2, pp. R227–R240, 2010.

[12] J. Clarke, H.-C. Wu, L. Jayasinghe, A. Patel, S. Reid, and H. Bayley, "Continuous base identification for single-molecule nanopore DNA sequencing," *Nature Nanotechnol.*, vol. 4, no. 4, pp. 265–270, Apr. 2009.

[13] R. D. Maitra, J. Kim, and W. B. Dunbar, "Recent advances in nanopore sequencing," *Electrophoresis*, vol. 33, no. 23, pp. 3418–3428, Dec. 2012.

[14] Y. Zhang, "Combined nanochannel-nanopore device for single-molecule DNA analysis and manipulation," M.S. thesis, Dept. Phys., McGill Univ., Montreal, QC, Canada, May 2012.

[15] D. Branton, "The potential and challenges of nanopore sequencing," *Nature Biotechnol.*, vol. 26, no. 10, pp. 1146–1153, 2008.

[16] B. M. Venkatesan and R. Bashir, "Nanopore sensors for nucleic acid analysis," *Nature Nanotechnol.*, vol. 6, pp. 615–624, Sep. 2011.

[17] E. A. Manrao, I. M. Derrington, M. Pavlenok, M. Niederweis, and J. H. Gundlach, "Nucleotide discrimination with DNA immobilized in the MSPA nanopore," *PLoS ONE*, vol. 6, no. 10, p. e25723, 2011.

[18] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise limits of CMOS current interfaces for biosensors: A review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 278–292, Apr. 2014.

[19] D. R. Garalde, C. R. O'Donnell, R. D. Maitra, D. M. Wiberg, G. Wang, and W. B. Dunbar, "Modeling the biological nanopore instrument for biomolecular state estimation," *IEEE Trans. Control Syst. Technol.*, vol. 21, no. 6, pp. 2038–2051, Nov. 2013.

[20] R. M. M. Smeets, U. F. Keyser, N. H. Dekker, and C. Dekker, "Noise in solid-state nanopores," *Proc. Nat. Acad. Sci. USA*, vol. 105, no. 2, pp. 417–421, Jan. 2008.

[21] R. Sarpeshkar, T. Delbruck, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits Devices Mag.*, vol. 9, no. 6, pp. 23–29, Nov. 1993.

[22] D. Kim, B. Goldstein, W. Tang, F. J. Sigworth, and E. Culurciello, "Noise analysis and performance comparison of low current measurement systems for biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 1, pp. 52–62, Feb. 2013.

[23] J. Kim, K. D. Pedrotti, and W. B. Dunbar, "On-chip patch-clamp sensor for solid-state nanopore applications," *Electron. Lett.*, vol. 47, no. 15, pp. 844–846, Jul. 2011.

[24] P. Weerakoon, E. Culurciello, K. G. Klemic, and F. J. Sigworth, "An integrated patch-clamp potentiostat with electrode compensation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 2, pp. 117–125, Apr. 2009.

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