



A Novel CMOS Realization of the Differential Input Balanced Output Current Operational Amplifier and its Applications

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Abstract. In this paper a new realization of the differential input balanced output current opamp is proposed, operating with ± 1.5 V supplies. Its architecture is based on the use of current inverters to sense the input currents while providing a very low input resistance, $23\ \Omega$. The opamp provides a maximum output swing of $700\ \mu\text{A}$, with an input offset current of $3.5\ \text{nA}$. The differential gain achieved is $65.5\ \text{dB}$, and the differential structure adopted in the design provided a high CMRR, $89.5\ \text{dB}$, the proposed circuit is compared to other realizations with single and differential inputs. The applications of the current opamp are exploited some new applications are presented such as: MOSFET-C integrators, full non-linearity cancellation for MOS transistors, and finally a digitally tuned current-mode variable gain amplifier, which has a gain tuning range of $25\ \text{dB}$ with a $0.05\ \text{dB}$ step.

Key Words: current operational amplifier, current-mode, current inverter, transconductor, variable gain amplifier, current division network

1. Introduction

The voltage operational amplifier (VOA) is unquestionably one of the most flexible and widely used analog building blocks. This stems from its generality, since it can be used in implementing many different applications. Such applications are: Addition/subtraction circuits, amplifiers, multipliers/dividers, interface circuitry, digital-to-analog conversion, analog-to-digital conversion, variable gain amplifiers, filters, oscillators... etc. Most of the systems based on VOAs represent the signal of interest in the voltage domain. During the past decade scaling down the technology feature size limited the maximum supply voltage that can be used to provide a constant electric field scaling. This scaling in the supply voltage limited the signal's dynamic range. This motivated designing new circuits in which the signal representation would not be directly affected by the supply scaling, the other alternative was using current representation for the desired signal. So in the past years current-mode circuits began to receive a great attention as a new alternative to voltage-mode circuits. Current-mode building blocks such as, current-feedback operational

amplifiers and current-conveyers have already been well documented. The current operational amplifier (COA) is still an emerging current-mode building block.

An ideal VOA is modeled as a three terminal (or four for a fully differential VOA) device with a high gain voltage-controlled voltage source having infinite input resistance and zero output resistance. On the other hand, in the current domain the analogous building block is the COA. A single input balanced output COA is shown in Fig. 1(a), it can be obtained by applying the theorem of adjoint networks [1] to a single ended VOA. An ideal COA is mainly an infinite gain current-controlled current source, but in practical cases the gain A becomes a function in frequency exhibiting a single pole response, this will guarantee the stability of the closed loop systems. It should exhibit a very low input resistance (ideally zero), and a very high output resistance (ideally infinity).

Several behavioral models have been proposed for the COA [2–8]. It is well known that fully differential voltage-mode circuits provide better performance than single ended circuits, mainly due to higher power supply rejection ratio ($PSRR$). Thus fully differential

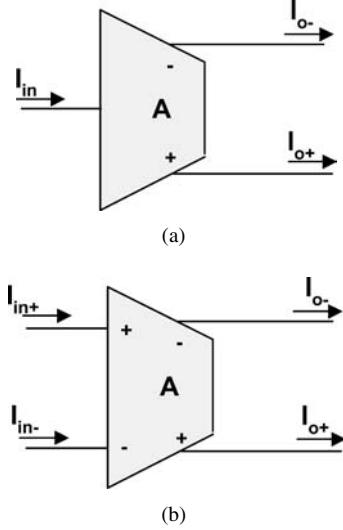


Fig. 1. (a) Circuit symbol of the COA. (b) Circuit symbol of the differential input COA.

VOAs are required to build such systems. By applying the theorem of adjoint networks the resulting building block is the differential input balanced output COA shown in Fig. 1(b). This shows the necessity to design differential input balanced output COAs for building fully balanced current-mode circuits. Recently, various CMOS implementations for the single input balanced output COA were reported [2, 3, 6–12]. While a few implementations for the differential input balanced output COA were presented in [2, 3, 13, 14].

The realization introduced in [2, 3] is based on the second-generation current conveyors (CCII). It consists of two input CCII:s: a CCII+ and a CCII-. The two input currents are applied to the X terminals of the input CCII:s as shown in Fig. 2(a). The Z terminal currents of both CCII:s are added at the Y terminal of the third CCII \pm , which is a high impedance node. This corresponds to subtracting the two input currents and multiplying them by the output impedance of the two input CCII:s connected in parallel. The voltage generated at the Y terminal is copied to the X terminal of the output CCII \pm , where it is converted to a current using the resistor R. This current is then conveyed to the two balanced output terminals. It can be shown that at low frequencies the relation between the input and output currents can be given by

$$I_{o+} = -I_{o-} = \frac{R_{out}}{R}(I_{in+} - I_{in-}) \quad (1)$$

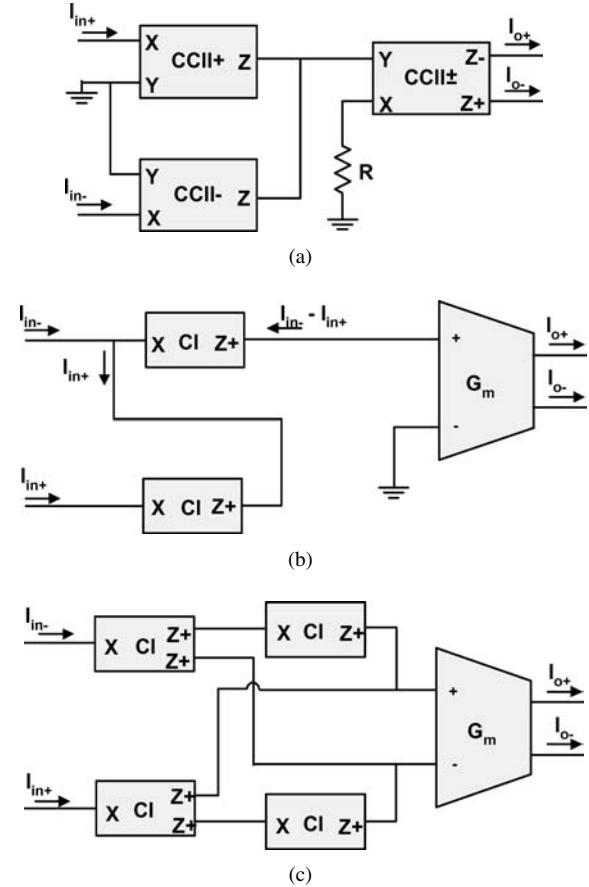


Fig. 2. (a) Block diagram of CCII based COA's. (b) First proposed block diagram for the COA. (c) Second proposed block diagram for the COA.

where \$R_{out}\$ is the output resistance of the input CCII:s connected in parallel. The main disadvantages of this architecture are: Firstly, to maximize the gain R should be shorted to ground or chosen a very small value, but the voltage following property between the X and Y terminals of the CCII is not insured in this case. Secondly, the output resistance of the input CCII:s is reduced due to their parallel connection. This reduces the overall gain by 6 dB. Finally, matching the two CCII blocks is not an easy design task due to their different polarities.

The realizations reported in [13, 14] are based on cascading a transresistance and transconductance amplifiers. The first stage is a high gain transresistance amplifier to convert the two input currents into two differential voltages, followed by a high gain transconductance amplifier to convert the two voltages into two

balanced currents. The transresistance amplifier is responsible for providing the low input impedance of the COA, while the transconductance amplifier is responsible for providing the high output impedance of the COA. The relation governing the input-output is

$$I_{o+} = -I_{o-} = R_m G_m (I_{in+} - I_{in-}) \quad (2)$$

In this work a new realization of the differential input balanced output COA is presented. It employs a different architecture for the COA based on current inverters and the floating current source (FCS) [15]. This implementation allows the COA to provide low input impedance and very small input offset current, while providing a high common mode rejection ratio (*CMRR*). The performance of the circuit will be compared with the reported single input and differential input COAs, and different applications based on the COA will be introduced.

2. New Realization of the COA

The proposed block diagram of the COA is shown in Fig. 2(b) where the two input currents are sensed using two current inverters to provide very low input resistance, and low offset voltage. The two currents are subtracted at one of the input nodes and the corresponding current inverter conveys the current difference to the Z terminal. The current difference is multiplied by the high output resistance of the current inverter to generate a voltage. This voltage is applied to a transconductor with two balanced output currents. The new architecture has overcome the disadvantages of the previous architecture in [2, 3]. Firstly, both currents are subtracted at the input of the first current inverter and not at the high impedance node, thus the gain is enhanced by approximately 6 dB. Secondly, the output CCII is removed and replaced by a balanced output transconductor. Finally, it is easier to match between the two current inverters as they have the same polarity. The output currents of the COA can be expressed as

$$I_{o+} = -I_{o-} = R_{out} G_m (I_{in+} - I_{in-}) \quad (3)$$

where R_{out} is the output resistance of the current inverter. From the above equation, it is evident that the proposed block diagram leads to the same gain when cascading a transresistance and transconductance amplifiers, but in this case simple current inverters replace the transresistance amplifier.

This architecture can be modified as shown in Fig. 2(c) to drive the output transconductor with two differential signals. This will increase the differential current gain by approximately 6 dB, but the differential gain is also reduced by approximately 6 dB due to the parallel connection of the current inverters. So the overall differential gain is not changed from the previous architecture. The modified architecture gives the COA a differential structure and thus increases its *CMRR*. To prove this we assume that the current conveying ratio is A_c instead of unity and express the voltage appearing at the input of the transconductor in Fig. 2(b) as

$$V_1 = -A_c R_{out} (A_c I_{in+} - I_{in-}) \quad (4)$$

This leads to a differential and common mode signal deriving the transconductor given by

$$\begin{aligned} V_{diff} &= -A_c R_{out} (A_c + 1) I_{in+} \\ V_{cm} &= -A_c R_{out} (A_c - 1) I_{in+} \end{aligned} \quad (5)$$

while for the circuit in Fig. 2(c) the voltage appearing at the input of the transconductor is expressed as

$$V_1 = -V_2 = -\frac{A_c R_{out}}{2} (I_{in+} - A_c I_{in-}) \quad (6)$$

Hence the differential and common mode voltages deriving the transconductor can be expressed as

$$\begin{aligned} V_{diff} &= -A_c R_{out} (1 + A_c) I_{in+} \\ V_{cm} &= 0 \end{aligned} \quad (7)$$

This shows that both architectures have the same differential gain but the second one provides a much higher *CMRR*. But any variations in the current conveying ratios or the output resistances of the current inverters will generate a common-mode signal. So the overall *CMRR* of the COA will still depend on the *CMRR* of the transconductance amplifier used.

3. Circuit Description of the COA

The architecture of the COA shown in Fig. 2(c) requires only two building blocks: current inverters and a balanced output transconductor.

The current inverter has an input terminal (X terminal) and one or more output terminals (Z terminals). An ideal current inverter is characterized by: Firstly, the current drawn into the Z terminal I_Z should perfectly

follow the current drawn into the X terminal I_X . Secondly, the voltage level at X terminal should be constant and independent of the value of the current drawn into it. This implies that the input resistance seen at the X terminal should ideally be zero. Arbitrarily, the value of the X terminal voltage is kept at zero potential. Thirdly, the output resistance seen at the Z terminal should be very high. The input terminals of the current inverters are responsible for realizing the two low impedance inputs of the COA. The class AB current inverter circuit used in realizing the COA is shown in Fig. 3 it was first proposed in [16]. The two current mirrors formed by transistors M₃ and M₄ force equal currents through both transistors M₁ and M₂. Neglecting the channel length modulation effect then both transistors M₁ and M₂ will have the same overdrive voltage, and since both gates are connected together they will both have the same source voltage. If the source of M₂ is kept at a constant voltage V_B , then the input terminal X will have approximately the same voltage. Grounding V_B will result in a zero potential at the X terminal independent of the input current. The negative feedback applied by transistors M₆–M₉ is responsible for further reduction in the input resistance of the current inverter and consequently the input resistance of the COA, which can be expressed as

$$R_{in} = \frac{R_2(1 + g_{m7}R_1)}{(1 + g_{m7}R_1) + R_2(1 + g_{m1}r_{ds1})(g_{m9}(1 + g_{m7}R_1) + R_1g_{m7}g_{m8})} \quad (8)$$

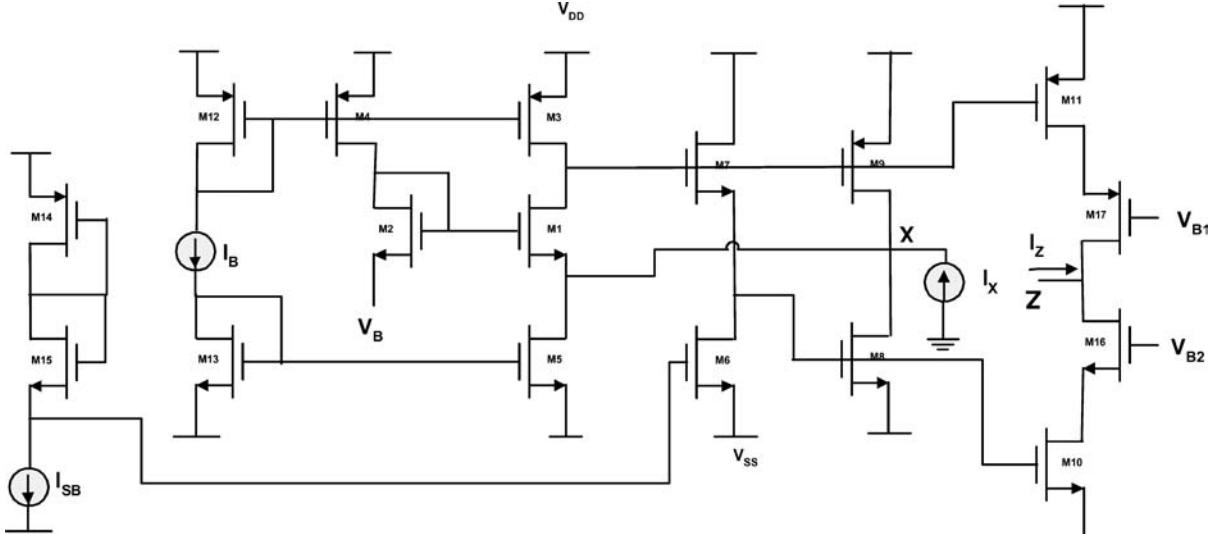


Fig. 3. Circuit diagram of the current inverter [16].

where

$$\begin{aligned} R_1 &= r_{ds6} \parallel r_{ds7} \\ R_2 &= r_{ds8} \parallel r_{ds9} \end{aligned} \quad (9)$$

Equation (8) can be approximated as

$$R_{in} \approx \frac{1}{g_{m1}r_{ds1}(g_{m8} + g_{m9})} \quad (10)$$

The current inversion action can be explained as follows: The current flowing in M₅ is I_B , which forces the input current I_X through both transistors M₈ and M₉. This current is then conveyed to output terminal through transistors M₁₀ and M₁₁. The output stage is cascaded to boost the output resistance of the circuit since the gain of the COA is directly related to its value. To obtain another version of the output current an additional output stage can be added. The class AB feedback loop reduces the power dissipated in the circuit, since when the current inverter is supplying current transistor M₁₁ supplies the majority of the current while transistor M₁₀ carries a negligible current. On the other hand, when the circuit is sinking current then both transistors interchange roles. When no input current is applied the current flowing through the output stage is equal to the stand by current, which can be chosen small to reduce the stand by power dissipation of the COA.

After creating a differential voltage representing the difference between the input currents multiplied by the

output resistance of the current inverter a balanced output transconductance amplifier is used to convert it into two balanced output currents. The FCS shown in Fig. 4 [15] is used to generate the balanced output currents. It can be viewed as two differential pairs: a matched NMOS pair and a matched PMOS pair connected in parallel. Assuming that all the transistors are operating in the saturation region, and neglecting the channel length modulation, then the differential transconductance can be given by

$$\begin{aligned} G_{\text{DM}} &= g_{\text{mn}} + g_{\text{mp}} = \sqrt{2I_T}(\sqrt{K_n} + \sqrt{K_p}) \\ &= \sqrt{2I_T C_{\text{ox}}}(\sqrt{\mu_n W_n / L_n} + \sqrt{\mu_p W_p / L_p}) \end{aligned} \quad (11)$$

where G_{DM} is the differential transconductance. To obtain the high differential gain required by the COA a high differential transconductance value must be achieved. Equation (11) points out that this can be achieved by increasing I_T , but the value of the current source I_T determines: the value of G_{DM} , the maximum output current swing, and the power dissipated by the transconductance amplifier. As a result, to maximize G_{DM} the aspect ratios of the transistors should be chosen large enough to achieve the desired gain. Also a trade-off exists between the power consumption of the transconductance amplifier and the output current swing of the COA. The $CMRR$ of the COA depends on the $CMRR$ of the transconductance amplifier as previously discussed. The output resistances of the tail current sources are the main source of the common-mode current gain. It can be shown that the differential and common-mode transconductances G_{DM} and G_{CM} are given by

$$G_{\text{DM}} = \frac{(g_{\text{mn}} + g_{\text{mp}})}{1 + R_L g_{\text{dn}} + R_L g_{\text{dp}}}$$

$$G_{\text{CM}} = \frac{2(g_{\text{mn}} + g_{\text{mp}}) \frac{R_{\text{TN}}}{R_{\text{TP}}} \left(\frac{2g_{\text{mn}} + 2g_{\text{dn}} + 1/R_{\text{TN}}}{2g_{\text{mp}} + 2g_{\text{dp}} + 1/R_{\text{TP}}} \right)}{R_L g_{\text{dn}} + R_{\text{TN}}(2g_{\text{mn}} + 2g_{\text{dn}} + 1/R_{\text{TN}}) + g_{\text{dp}} R_L \frac{R_{\text{TN}}}{R_{\text{TP}}} \left(\frac{2g_{\text{mn}} + 2g_{\text{dn}} + 1/R_{\text{TN}}}{2g_{\text{mp}} + 2g_{\text{dp}} + 1/R_{\text{TP}}} \right)} \quad (13)$$

where R_L is the load resistance, R_{TN} and R_{TP} are the output resistances of the NMOS and PMOS current sources, respectively. g_{dn} and g_{dp} are the output conductances of the NMOS and PMOS pairs, respectively. If the output conductances of the NMOS and PMOS pairs can be neglected then

$$G_{\text{DM}} = g_{\text{mn}} + g_{\text{mp}} \quad (14)$$

$$G_{\text{CM}} = 2 \left(\frac{g_{\text{mn}}}{1 + 2g_{\text{mn}}R_{\text{TN}}} + \frac{g_{\text{mp}}}{1 + 2g_{\text{mp}}R_{\text{TP}}} \right) \quad (15)$$

The $CMRR$ of the transconductance amplifier can be expressed as

$$\begin{aligned} CMRR &= \frac{G_{\text{DM}}}{G_{\text{CM}}} \\ &= \frac{(g_{\text{mn}} + g_{\text{mp}})(1 + 2g_{\text{mn}}R_{\text{TN}})(1 + 2g_{\text{mp}}R_{\text{TP}})}{2g_{\text{mn}}(1 + 2g_{\text{mp}}R_{\text{TP}}) + 2g_{\text{mp}}(1 + 2g_{\text{mn}}R_{\text{TN}})} \end{aligned} \quad (16)$$

$$CMRR \approx (g_{\text{mn}} + g_{\text{mp}})(R_{\text{TN}} \parallel R_{\text{TP}}) \quad (17)$$

Equation (17) shows that the $CMRR$ of the transconductance amplifier and consequently the COA is a direct function in the output resistances of the current sources R_{TN} and R_{TP} . The output resistance of the transconductance amplifier determines the output resistance of the COA, which can be expressed as

$$\begin{aligned} R_{\text{out}} &= \frac{(1 + 2(g_{\text{mn}} + g_{\text{dn}})R_{\text{TN}})(1 + 2(g_{\text{mp}} + g_{\text{dp}})R_{\text{TP}})}{g_{\text{dn}}(1 + 2(g_{\text{mp}} + g_{\text{dp}})R_{\text{TP}}) + g_{\text{dp}}(1 + 2(g_{\text{mn}} + g_{\text{dn}})R_{\text{TN}})} \end{aligned} \quad (18)$$

This can be approximated to

$$R_{\text{out}} = \frac{2g_{\text{mn}}g_{\text{mp}}R_{\text{TN}}R_{\text{TP}}}{g_{\text{dn}}g_{\text{mp}}R_{\text{TP}} + g_{\text{dp}}g_{\text{mn}}R_{\text{TN}}} \quad (19)$$

For stable operation frequency compensation is necessary. This is can be done by connecting a Miller compensation capacitance and series resistance between the input of the transconductor and the output of the first stage current inverters. The value of the compensation

$$(12)$$

capacitor used was 0.13 pF and the series compensation resistance used was 2 KΩ.

4. Simulation Results of the Proposed COA

In this section the simulation results of the proposed differential input balanced output COA are reported. Simulations were carried-out using level 8 Spice parameters for a 0.5 μm standard CMOS process. All

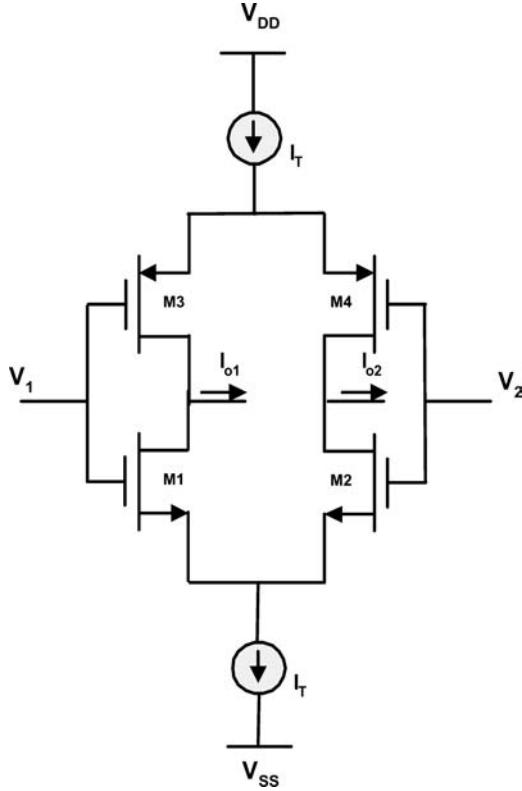


Fig. 4. Circuit diagram of the FCS [15].

circuits were operated using a ± 1.5 V supply voltage. The biasing current for the transconductance amplifier I_T was chosen $350 \mu\text{A}$ to provide an output current swing of $700 \mu\text{A}$ while maintaining an appropriate level of power dissipation. The current inverters were biased using a $100 \mu\text{A}$ current source and the stand-by current source was chosen $50 \mu\text{A}$, this value won't lead to a power efficient solution but was used to achieve a high bandwidth for the current inverters and consequently the COA. The DC characteristics of the COA are shown in Fig. 5, they were obtained by sweeping one of the input currents from -350 to $350 \mu\text{A}$ while the other was set to zero. This shows that the maximum output current that the COA can drive is $350 \mu\text{A}$. The input offset current is shown in Fig. 6 and a value as low as 3.5nA was obtained. The frequency response of the COA is shown in Figs. 7 and 8 showing a differential current gain of 65.3 dB and a unity gain bandwidth of 266 MHz with a phase margin of 55.4° . Figure 7 also shows a common mode current gain of -24.4 dB , leading to a $CMRR$ of 89.7 dB . The differential input

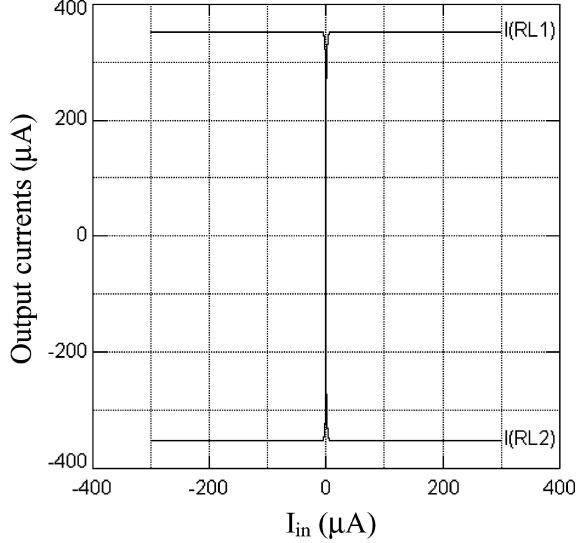


Fig. 5. DC characteristics of the COA.

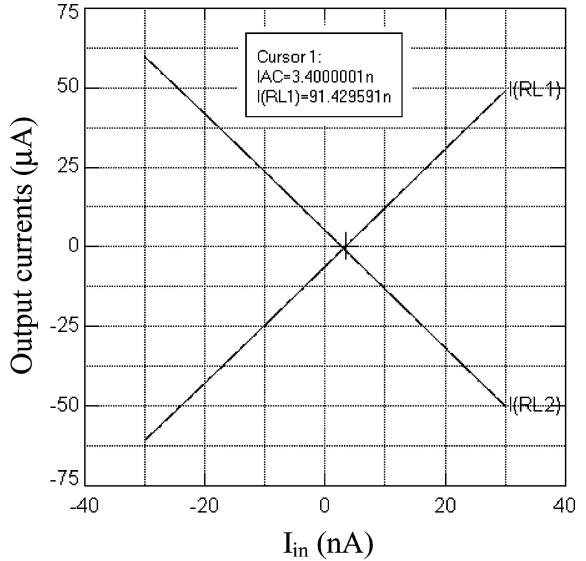


Fig. 6. DC characteristics, showing input offset current.

resistance of the COA was 23.16Ω , while it offered an output resistance of $15 \text{ M}\Omega$. The current inverters fixed the voltage of the input terminals to ground with an offset of 23 mV . The proposed differential input balanced output COA dissipates 4 mW . To compare the performance of the proposed differential input balanced output COA the simulation results were tabulated and compared with other realizations in Table 1. The

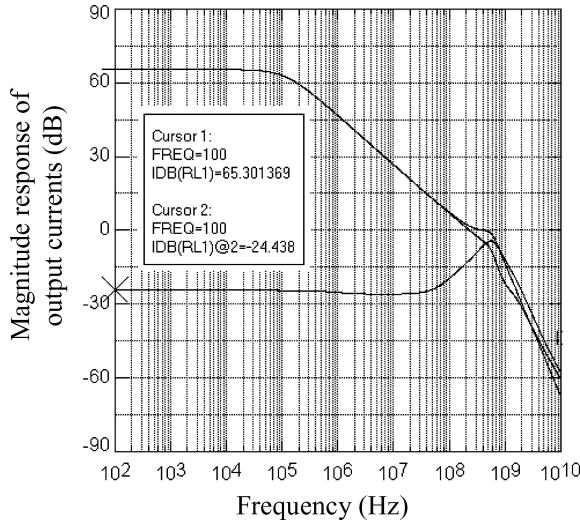


Fig. 7. Frequency response of the COA: Magnitude of output currents for both differential and common modes.

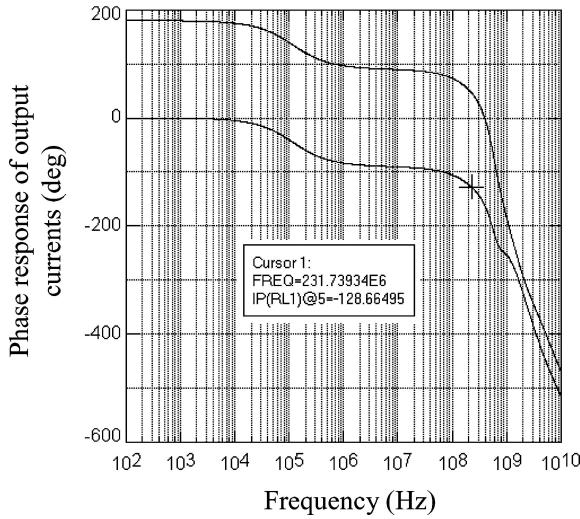


Fig. 8. Frequency response of the COA: Phase of output currents.

realization in [2, 3] offers a slightly higher differential gain and higher output current swing but on the expense of the bandwidth and the power consumption, and the input offset current is two orders of magnitude higher. While the realization in [14] offers a tunable gain that is much higher than the gain of the proposed circuit and dissipates a less amount of power, but it provides a very small output swing. Finally, the realization in [13] provides a slightly higher bandwidth and a higher output swing, but on the expense of the power dissipation and

it suffers from a small *CMRR*. Some specifications were unavailable in [2, 3] and [13, 14] for the comparison between the differential input COAs. To demonstrate the low input offset current, and input resistance Table 2 presents a comparison between the simulated results obtained from the proposed circuit and the reported specifications for single input COAs. It is evident that the proposed COA offers a high *CMRR* due to its differential structure and very low input resistance provided by the current inverters. It also offers a very small input offset current and a high unity gain bandwidth while dissipating a moderate amount of power.

5. Applications Based on Differential Input Balanced Output COAs

Analog circuit designers could make use of the theorem of adjoint networks [1] when designing current-mode circuits, since any voltage-mode circuit may be transformed into its current-mode version using this theorem. Applying it to traditional designs based on VOAs such as: amplifiers, integrators, and filters will result in current-mode circuits performing the same function but based on the COA. Besides, the COA is a powerful current-mode building block and can be utilized to build many different applications as will be discussed later.

Applying the theorem of adjoint networks to the VOA-based differential amplifier a current-mode amplifier is obtained, this is shown in Fig. 9. To analyze this circuit it should be noted that the two input terminals of the COA have a zero potential independent of the feedback, which is a major difference between it and the VOA. In addition to that the negative feedback applied to the COA forces the differential input current to zero, hence equating the two input currents results in

$$V_{o1} - V_{o2} = R_2(I_{in1} - I_{in2}) \quad (20)$$

Since the two output currents of the COA are balanced then

$$V_{o1} = -V_{o2} \quad (21)$$

Solving Eqs. (20) and (21), and relating the output voltages to the two balanced output currents the following

Table 1. Comparison between differential input balanced output realizations of COAs.

Comparison of C/Cs of differential inputs COA	[3]	[13]	[14]	Proposed	Units
Differential gain	72	57.71	70–96	65.5	dB
CMRR	NA	41.25	NA	89.5	dB
Gain bandwidth product	3	314	145	266	MHz
Phase margin	60°	50°	NA	55°	Degree
Maximum output swing (pp)	1400	2000	280	700	μA
Settling time	NA	14	NA	20	ns
Slew rate	NA	160/6.4	NA	120/1.9	μA/ns
Input resistance	NA	NA	NA	23.16	Ω
Output resistance	NA	NA	NA	15.38	MΩ
Input offset current	800	NA	NA	3.5	nA
Input offset voltage	NA	NA	NA	23.16	mV
Power dissipation	NA	6.5	<0.5	4.07	mW
Supply voltage	NA	±1.5	±1.5	±1.5	V
Technology	CMOS 2.4	CMOS 0.5	BiCMOS 0.8	CMOS 0.5	μm

Table 2. Comparison between different realizations of single input balanced output COAs.

C/Cs of single input COAs	[3]	[6]-a	[6]-b	[9]	[10]-a	[10]-b	[10]-c	[11]	[12]	Proposed	Units
DC gain	72	65	54	65	66.2	63	66	94.2	67	65.5	dB
CMRR	NA	NA	NA	NA	NA	NA	NA	58.8	150	89.5	dB
GBP	3	8	90	200	21.5	57.5	105	67	100	266	MHz
PM	60°	60°	60°	60°	57°	90°	81°	NA	61°	55°	Degree
Max. output current swing (peak-to-peak)	NA	NA	NA	NA	100	NA	200	NA	NA	700	μA
Settling time	NA	150	15	5.1	NA	NA	NA	NA	NA	20	ns
Slew rate	NA	NA	NA	NA	NA	NA	NA	NA	NA	120/1.93	μA/ns
Input resistance	NA	3.65	5	0.14	0.032	0.032	0.032	5.7	0.3	0.02316	KΩ
Output resistance	NA	0.89	0.18	2.8	4.7	4.7	4.7	7.6	0.3	15.38	MΩ
Input offset current	NA	NA	NA	NA	1000	1000	80	NA	200	3.5	nA
Input offset voltage	NA	NA	NA	NA	4.47	4.47	51	NA	NA	23.16	mV
Power dissipation	NA	3.1	4.6	4.5	0.66	NA	NA	0.03	4.5	4.07	mW
Supply voltage	NA	NA	NA	±3	±3.3	±3.3	±3.3	1.5	3	±1.5	V
Technology (CMOS)	2.4	2	2	1.2	1.2	1.2	1.2	2	1.2	0.5	μm

is obtained

$$I_{o1} = -I_{o2} = -\frac{R_2}{R_1} \frac{(I_{in1} - I_{in2})}{2} \quad (22)$$

It is noted that the negative feedback around the COA produced an accurate closed loop current gain, which is insensitive to variations in process, supply voltage, and temperature.

Similarly a current-mode integrator can be obtained from the voltage-mode integrator, this is shown in Fig. 10. Following the same procedure described for the amplifier it can be shown that the input-output relation is given by

$$I_{o1} = -I_{o2} = -\frac{1}{sCR} \frac{(I_{in1} - I_{in2})}{2} \quad (23)$$

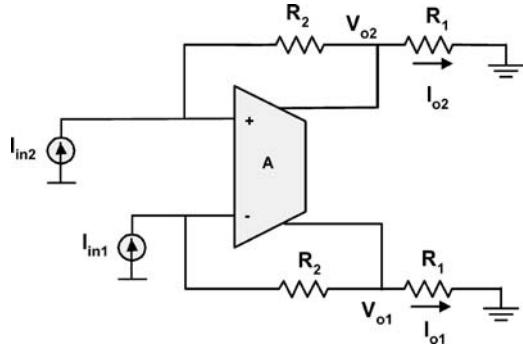


Fig. 9. Differential input balanced output current-mode amplifier.

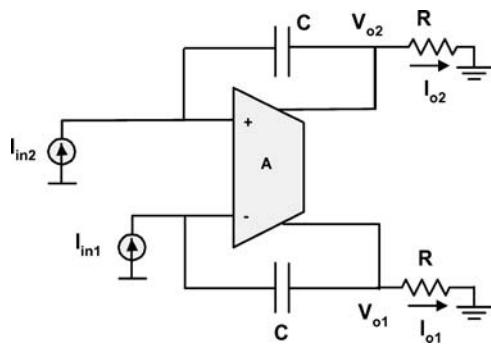


Fig. 10. Differential input balanced output current-mode integrator.

5.1. A Differential Input Balanced Output Current-Mode MOSFET-C Integrator

Designing fully integrated filters is one of the most important targets in modern filter design. This factor made digital filters and switched capacitor filters dominate over active RC filters. Other alternatives appeared such as G_M -C filters, filters based on current conveyors, and MOSFET-C filters. The latter uses only MOSFETs, capacitors, and active elements eliminating the need for integrating resistors on chip [17], which is associated with inaccuracy of the filter time constant.

To design resistor free current-mode filters it is desired to eliminate the use of resistors in the integrator based on the COA. A new circuit is proposed to achieve a differential input balanced output current-mode integrator suitable for integration. The block diagram of the proposed circuit is shown in Fig. 11. The difference between the two input currents is integrated and converted to a differential voltage. It can be shown that the two voltages V_{o1} and V_{o2} are balanced and are given

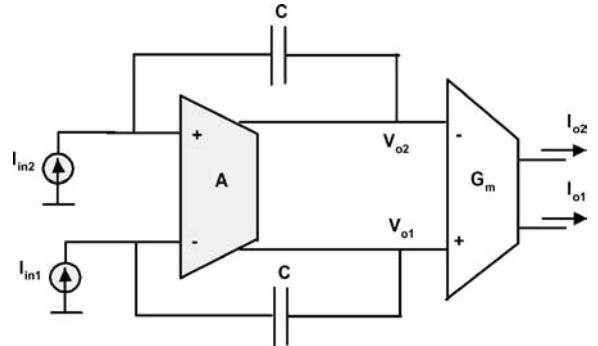


Fig. 11. Block diagram of the proposed differential input balanced output MOSFET-C current integrator.

by

$$V_{o1} = -V_{o2} = \frac{1}{2sC}(I_{in2} - I_{in1}) \quad (24)$$

To achieve the function required by the integrator the above differential voltage should be transformed into two balanced currents, this can be done using any transconductance amplifier. Here the FCS [15] is used since its linearity and range of operation can be easily extended as both voltages are balanced. The detailed circuit is shown in Fig. 12. Assuming the transistors are operating in the saturation region, (M_1, M_2) are matched, and (M_3, M_4) are matched then the output currents can be expressed as

$$I_{o1} = -I_{o2} = G_m \frac{(I_{in2} - I_{in1})}{sC} \quad (25)$$

where G_m is given by

$$G_m = \sqrt{2I_T}(\sqrt{K_n} + \sqrt{K_p}) \quad (26)$$

where I_T is the tail current, K_n and K_p are the transconductance parameters of the NMOS and PMOS pairs, respectively.

Simulation results of the integrator are shown in Figs. 13 and 14. Figure 13 shows the magnitude response of the output currents versus frequency indicating a slope of -20 dB/dec. A square-wave with $100\ \mu\text{A}$ peak-to-peak amplitude and $2\ \mu\text{sec}$ period is applied to the integrator and the two balanced integrated output currents are plotted in Fig. 14. The proposed integrator can be used to build fully balanced MOSFET-C current-mode filters.

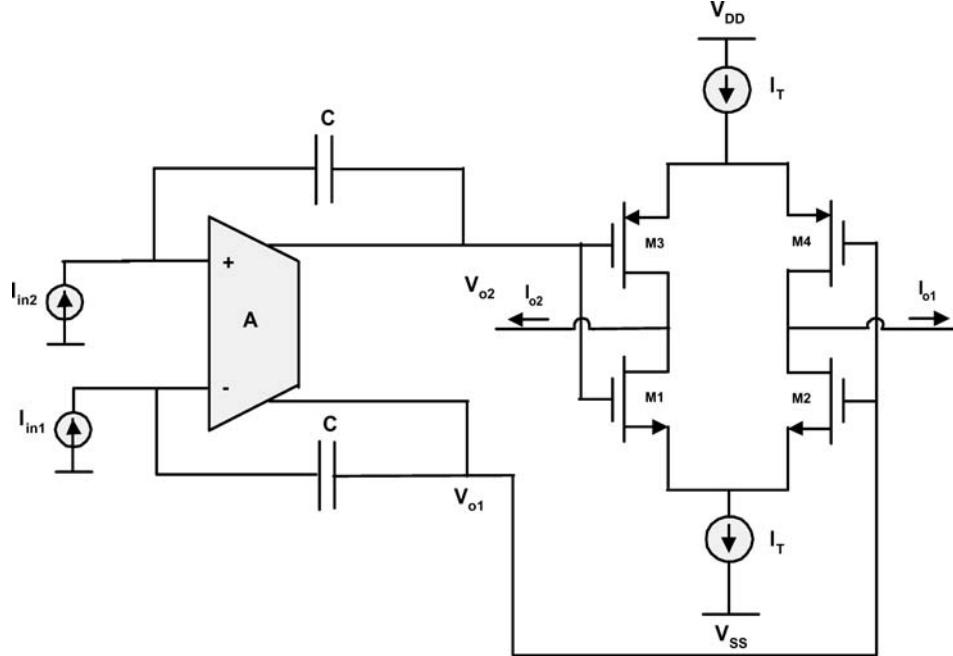


Fig. 12. The proposed MOSFET-C current integrator.

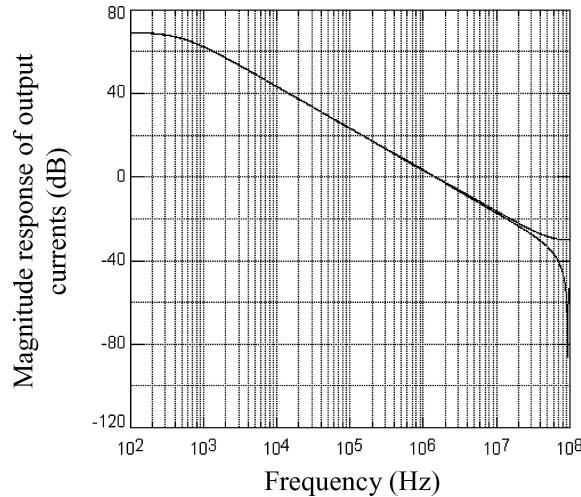


Fig. 13. Frequency response: Magnitude of output currents.

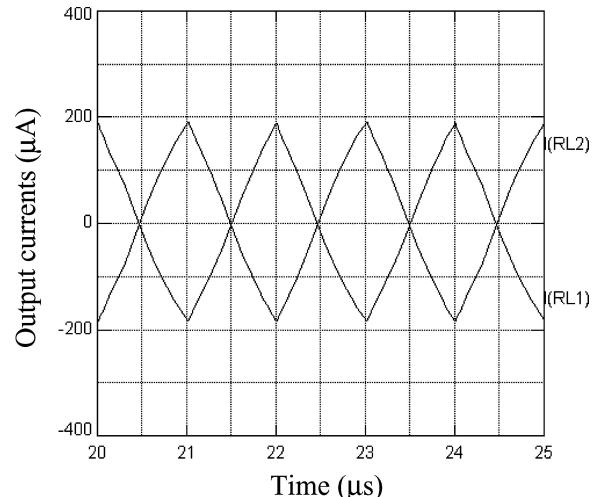


Fig. 14. Balanced output current waveforms.

5.2. A Second Order Current-Mode LP/BP Filter Based on the COA

The basic building blocks in filter design are integrators, since it was possible to design differential input balanced output integrators based on the COA. One can

now extend it to the design of current-mode continuous time filters. One of the simplest second order filters is the biquad filter; in a biquad filter the first integrator is a lossy integrator, while the second is an ideal integrator. To design a current-mode biquad, current integrators will replace the voltage integrators. Figure 15 shows

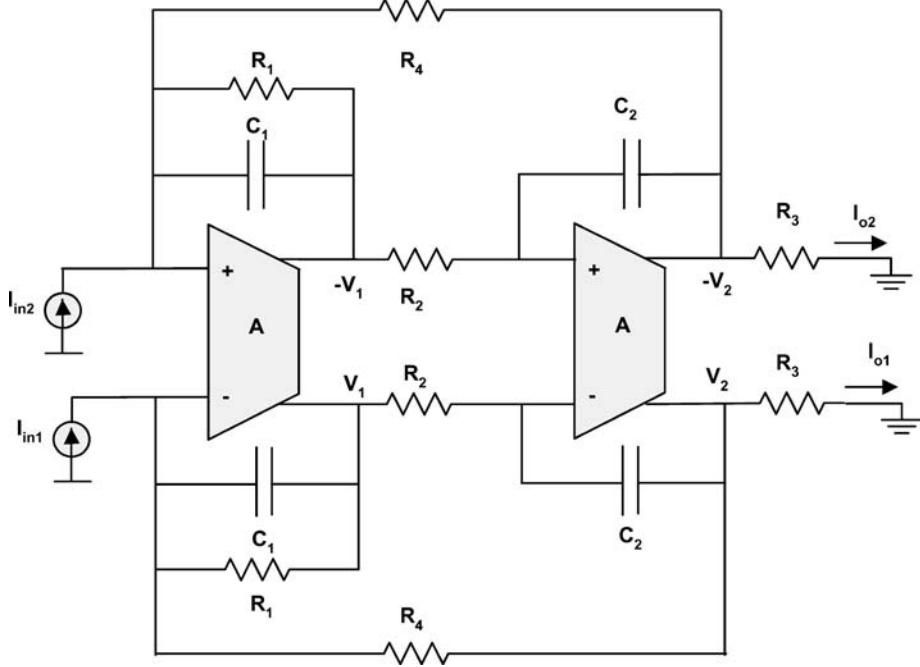


Fig. 15. Current-mode LPF.

the circuit diagram of the LPF, it can be shown that the voltages at the output terminals of each COA are differential. Writing the basic equations of each COA yields

$$I_{in2} - I_{in1} = 2 \left(V_1 \left(\frac{1}{R_1} + sC_1 \right) + \frac{V_2}{R_4} \right) \quad (27)$$

$$V_1 = sC_2R_2V_2 \quad (28)$$

Solving the above two equations together and given that

$$I_{o1} = -I_{o2} = \frac{V_2}{R_3} \quad (29)$$

then the output currents can be expressed as

$$I_{o1} = -I_{o2} = \frac{(I_{in2} - I_{in1})}{2} \frac{\frac{1}{C_1C_2R_2R_3}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2R_2R_4}} \quad (30)$$

The filter parameters: ω_o , Q , and the DC gain can be obtained from Eq. (30).

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_2R_4}} \quad (31)$$

$$\text{DC gain} = \frac{R_4}{R_3} \quad (32)$$

For an equal R equal C design $C_1 = C_2 = C$, $R_2 = R_4 = R$ then

$$\begin{aligned} \omega_o &= \frac{1}{CR} \\ Q &= \frac{R_1}{R} \end{aligned} \quad (33)$$

A bandpass output can be obtained from the same filter by adding two grounded resistors connected to the output terminals of the first COA, this is shown in Fig. 16. Adding the two resistors will not affect the lowpass transfer function it can be shown that

$$I_{BP1} = -I_{BP2} = \frac{(I_{in2} - I_{in1})}{2} \frac{\frac{s}{C_1R_5}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2R_2R_4}} \quad (34)$$

In this case the center frequency gain of the bandpass filter is

$$\text{Center frequency gain} = \frac{R_1}{R_5} \quad (35)$$

The LP filter is designed to obtain a Butterworth response ($Q = 0.717$) with a normalized DC gain of

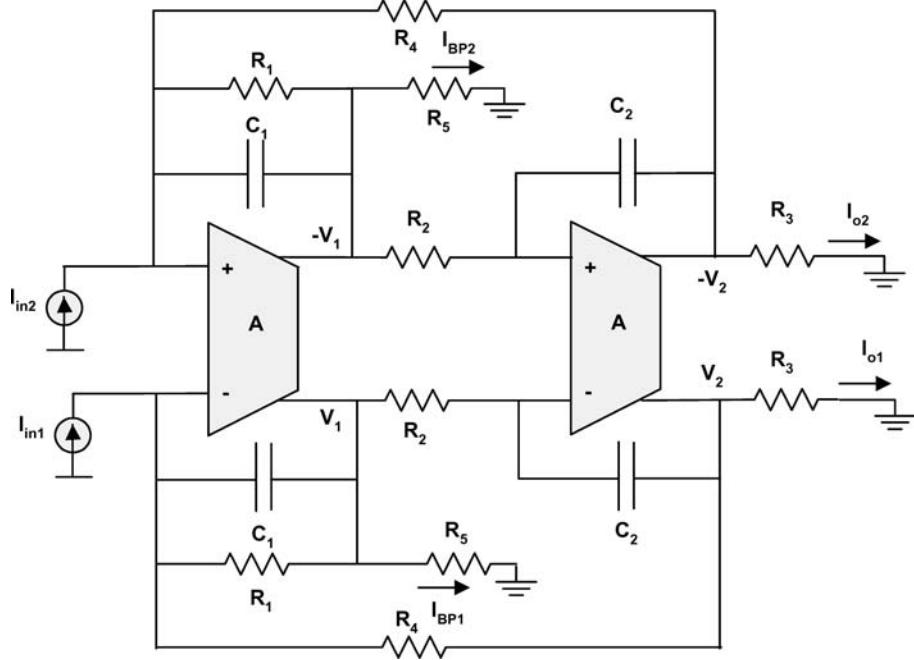


Fig. 16. Current-mode LPF/BPF.

0 dB, while for the BP output the center frequency gain is set to 0 dB. The resistor values were chosen: $R_2 = R_3 = R_4 = 2 \text{ k}\Omega$, $R_1 = R_5 = 1.414 \text{ k}\Omega$, and the capacitors were chosen 10 pF. Using these values the center frequency can be calculated using Eq. (33). From calculations the center frequency is expected to be 7.96 MHz. AC analysis was carried out to characterize the filter magnitude response and the simulation results are shown in Fig. 17. The cutoff frequency of the LPF and the center frequency of the BPF are the same as the expected frequencies obtained from the calculations.

5.3. Full Non-Linearity Cancellation Based on the COA

VOA have been used to cancel the non-linearity of the MOS transistor [17], similarly the COA can also be used for full non-linearity cancellation in MOS transistors operating in the linear region. The proposed circuit is shown in Fig. 18, assuming that: the transistors are operating in the linear region, (M_1, M_2) are matched, and (M_3, M_4) are matched

then

$$\begin{aligned} I_1 &= K_1 \left((V_G - V_T) V_{o1} - \frac{V_{o1}^2}{2} \right) \\ I_2 &= K_1 \left((V_G - V_T) V_{o2} - \frac{V_{o2}^2}{2} \right) \\ I_{o1} &= K_2 \left((V_G - V_T) V_{o1} - \frac{V_{o1}^2}{2} \right) \\ I_{o2} &= K_2 \left((V_G - V_T) V_{o2} - \frac{V_{o2}^2}{2} \right) \end{aligned} \quad (36)$$

where K_1 and K_2 are the transconductance parameters of $M_{1,2}$ and $M_{3,4}$ respectively. Since the outputs of the COA are balanced then

$$I_1 + I_{o1} = -(I_2 + I_{o2}) \quad (37)$$

The negative feedback through the feedback transistors will force the differential input currents to zero

$$I_1 + I_{in1} = I_2 + I_{in2} \quad (38)$$

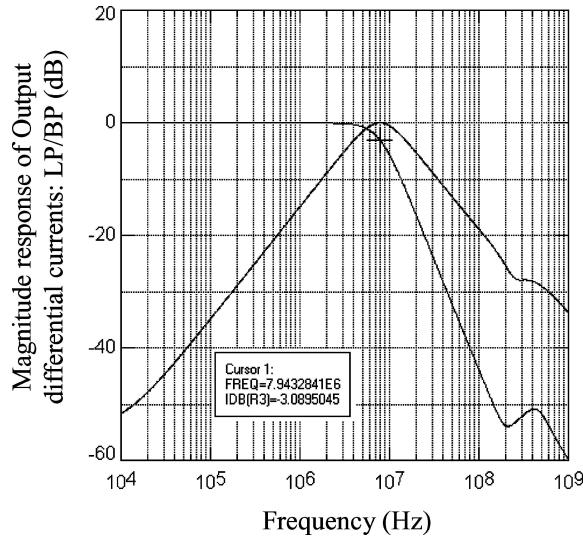


Fig. 17. Frequency response of the current-mode differential input balanced output LPF/BPF.

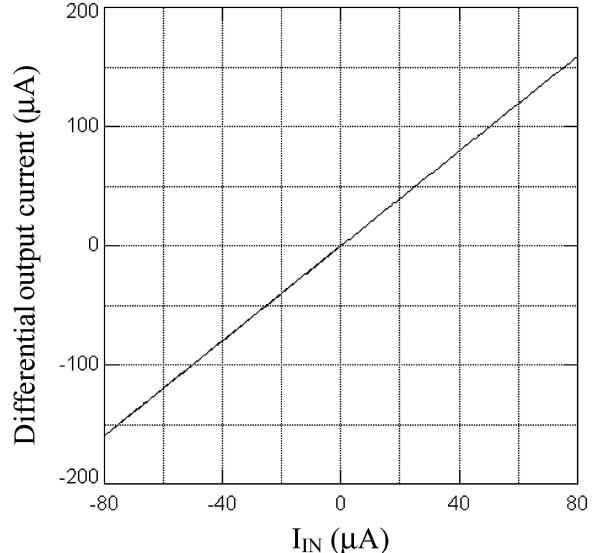


Fig. 19. DC characteristics of the current amplifier.

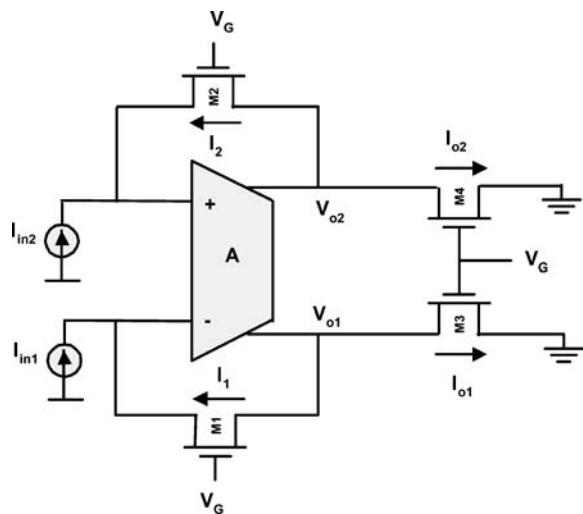


Fig. 18. Non-linearity cancellation using the COA.

Solving Eqs. (36)–(38) yields the following

$$\begin{aligned} I_{o1} &= -I_{o2} \\ I_{o1} - I_{o2} &= -\frac{K_2}{K_1}(I_{in1} - I_{in2}) \\ \frac{I_{OD}}{I_{IN}} &= -\frac{W_2/L_2}{W_1/L_1} \end{aligned} \quad (39)$$

This circuit represents a current-mode differential input balanced output amplifier. It is important to notice

that the output is independent of V_G so it is chosen to ensure that the transistors operate in the linear region. The main advantage of this current-mode amplifier is that its gain is set by the aspect ratios of the transistors, which can be much more accurate than the ratio of the resistors. This provides a gain that is independent of process variation and etching accuracy. The transistor ratios were chosen the same to provide a unity gain amplifier. The differential input current was swept from -160 to $160 \mu\text{A}$, and the differential output current is plotted in Fig. 19 demonstrating a highly linear amplifier.

5.4. A Differential Input Balanced Output Current-Mode VGA

Variable gain amplifiers (VGAs) are employed in many applications to adapt the gain of the overall system. Thus enabling the system to deal with very small signals and very large signals at the same time. This increases the dynamic range of the system. Many of these applications are mixed analog and digital systems; mainly the input is in an analog form and some processing may take place in the analog domain. Eventually this signal is converted into the digital domain to allow more complex signal processing. Usually the VGA is controlled by the digital part to perform the automatic gain control (AGC) action. A VGA controlled

by an analog signal will need an extra digital-to-analog converter (DAC) in the AGC loop increasing the complexity and delay. Using a digitally controlled VGA would increase the system performance.

The gain of the VGA should be an exponential function in the control signal. This is required to maintain the AGC loop settling time independent of the input signal level. In this work the exponential function will be approximated by

$$e^x \approx \frac{1+x/2}{1-x/2} = \frac{A_1}{A_2} \quad (40)$$

where x is an n -bit control signal. The exponential function can also be approximated by dividing a linearly increasing function A_1 by a linearly decreasing function A_2 [18], where A_1 and A_2 are digital words and can be expressed as

$$\begin{aligned} A_1 &= A_o D = A_o(a_o + 2^{-1}a_1 + \dots + 2^{-(n-1)}a_{n-1}) \\ A_2 &= A_o \bar{D} = A_o(\bar{a}_o + 2^{-1}\bar{a}_1 + \dots + 2^{-(n-1)}\bar{a}_{n-1}) \end{aligned} \quad (41)$$

The resolution, n , of the digital control word D , determines the number of gain steps of the VGA circuit, and A_o is any constant depending on the circuit realization.

The proposed current-mode VGA circuit employs the current division network (CDN) to realize precise digital control [19]. The circuit diagram of a 3-bit CDN is shown in Fig. 20, all transistors have equal dimensions. According to the current division principle, the input current I_{in} is divided equally into two parts; the first part flows through transistor M_2 and the remaining part flows through transistor M_3 . The current carried by transistor M_2 is again divided into two equal currents. So one fourth of the input current I_{in} flows through

the transistor M_4 and the remaining one fourth continues to the last stage of the CDN to be further divided. Transistors $M_5, M_6, M_7, M_8, M_{13}, M_{14}$ act as switches where the digital word D and its complement are applied to their gates to produce the following two output currents

$$\begin{aligned} I_{o1} &= \frac{I_{in}}{2} \sum_{i=0}^{n-1} a_i 2^{-i} \\ I_{o2} &= \frac{I_{in}}{2} \sum_{i=0}^{n-1} \bar{a}_i 2^{-i} \end{aligned} \quad (42)$$

For the current division principle to hold the two output terminals A and B of the CDN must be kept at zero potential. In the CDN the transistors responsible for the switching are at the same time used in the current division to provide two identical paths for the current to divide equally. Therefore the CDN provides precise digital trimming without any spread in the transistor aspect ratio. The symbol of the CDN is shown in Fig. 21.

Using the CDN with the COA is much more straightforward than with the VOA [18], this stems from the grounds at the two input terminals of the COA regardless of the feedback action. On the other hand if VOAs are used, then the input nodes must be forced to ground by the effect of the negative feedback. The proposed current-mode digitally controlled VGA is shown in Fig. 22. Since negative feedback is applied to the COA then the differential input current should be forced to zero, and

$$\begin{aligned} I_{in1} + \bar{D} I_o &= I_{in2} - \bar{D} I_o \\ I_o &= \frac{(I_{in2} - I_{in1})}{2\bar{D}} \end{aligned} \quad (43)$$

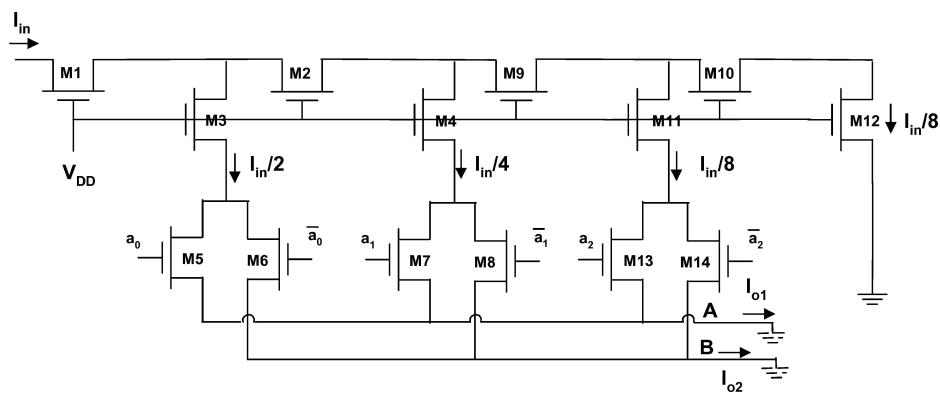


Fig. 20. Circuit diagram of a 3-bit CDN.

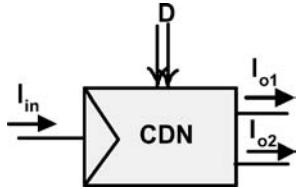


Fig. 21. Symbol used for the CDN.

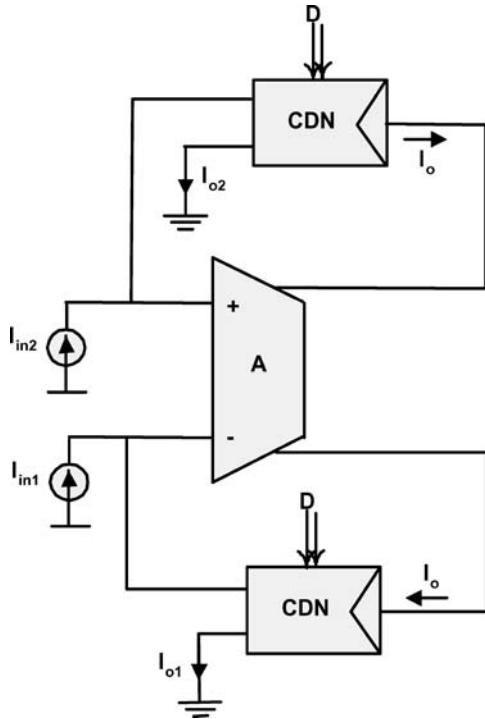


Fig. 22. Block diagram of the proposed differential input balanced output digitally controlled VGA.

The two output currents I_{o1} and I_{o2} can be expressed as

$$I_{o1} = -I_{o2} = \frac{D}{\bar{D}} \frac{(I_{in2} - I_{in1})}{2} \quad (44)$$

Equation (44) indicates that the gain of the VGA is the ratio of two functions in the input control word. The numerator is an increasing function, while the denominator is a decreasing function thus approximating the exponential characteristics. The maximum and minimum gains achieved and the gain step are a direct function of the number of bits, n , used for the CDN. Increasing the number of bits will: increase the maximum gain, increase the maximum attenuation, and decrease

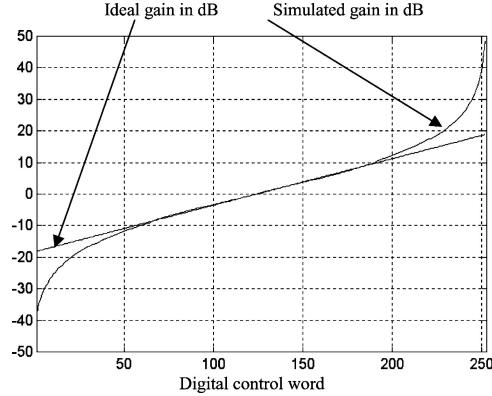


Fig. 23. The gain of the proposed digitally controlled VGA and the ideal gain in dB, versus the digital control word.

the step size. This will consequently increase the system dynamic range. The VGA was simulated using a 10-bit CDN, the two least significant bits were fixed to obtain only 256 different combination. The gain was measured for each of these combinations and plotted in Fig. 23 as a function of the decimal value of the digital control word. The ideal and the simulated characteristics show perfect matching in about four fifth of the full scale of the digital control word. The gain varies over approximately a 25 dB range with gain error less than 0.5 dB. The gain step achieved is approximately 0.05 dB, which is a very fine step. The gain error is plotted in Fig. 24. A fully balanced voltage-mode digitally controlled VGA based on the CDN would utilize two VOAs, thus the new COA would be more suitable for this application, since only one COA is used to perform the same function.

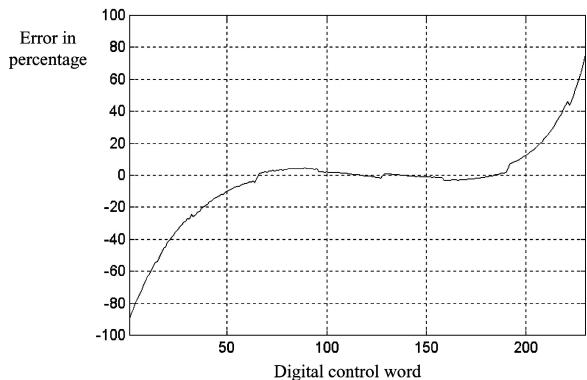


Fig. 24. The error between the ideal and simulated gains, in percentage, versus the digital control word.

6. Conclusion

In this paper a new CMOS realization of a differential input balanced output COA was proposed operating with a ± 1.5 V supply voltage. The architecture of the COA was based on utilizing current inverters to provide a very low input resistance. The output resistance of the current inverter was used to achieve the very high differential gain required and to convert the input currents into two differential voltages at the same time. The proposed circuit was compared to previous realizations and showed better performance mainly in the value of the input resistance, input offset current, bandwidth, and dissipating moderate power. The differential input balanced output COA was employed in some of the applications traditionally designed using fully differential VOAs. Some of these applications were presented such as: current amplifiers, integrators. Furthermore, a new integrator was proposed suitable for MOSFET-C filters designed without using resistors. After that a current-mode differential input balanced output continuous time LPF/BPF was presented based on a two-integrator loop. It was also proved that Full non-linearity cancellation in MOS transistors is possible using the COA. This was utilized to design an accurate current-mode amplifier in which the gain was set by the ratio of the transistor dimensions. The COA was then used to design a fully balanced current-mode digitally controlled VGA using the CDN for precise digital trimming.

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