ULTRA-LOW-NOISE TRANSIMPEDANCE AMPLIFIER FOR HIGH-PERFORMANCE MEMS RESONANT GYROSCOPES

J.-K. Woo, C. Boyd, J. Cho, and K. Najafi
Center for Wireless Integrated MicroSensing and Systems (WIMS^2)
University of Michigan, Ann Arbor, Michigan, USA

ABSTRACT

This paper describes a generic, ultra-low-noise transimpedance amplifier (TIA) for capacitive MEMS sensors. The TIA obtains both very low input referred current noise (5.12 fA/√Hz) and wide dynamic range (123 dB) by employing a digitally-controlled floating resistor, a voltage-and-temperature tolerant current generator, and low-noise operational amplifier (op-amp). The floating resistor allows the amplifier to obtain excellent output linearity and obtain a wide dynamic range. An integrated digital controller of the current generator lowers the TIA noise by reducing the amount of fluctuation in the resistance of the floating resistor by eliminating the transmission of control voltages for the floating resistor through a bonding pad. A beta-multiplier current reference circuitry with a resistor with low temperature coefficient of resistance (TCR) generates bias current with very low sensitivity to variations in supply voltage and temperature. A two-stage Miller-compensated op-amp with optimized transistor dimensions is designed. The prototype chip was fabricated using a 0.18 μm standard CMOS process with 1.8 V supply voltage. The circuitry is evaluated with a high performance vibratory MEMS gyroscope and excellent bias stability (0.04 deg/h) is measured.

KEYWORDS

Low noise, capacitive sensing, transimpedance amplifier, floating resistor, vibratory gyroscope, MEMS gyroscope

INTRODUCTION

The performance of MEMS gyroscopes is rapidly approaching the level that can be adopted in a wide range of military and high-end industrial applications. One of the most highly desired applications for a high-performance gyroscope is GPS-free inertial navigation for autonomous cars, drones, and indoor pedestrians. A gyroscope for these applications is required to have very high bias stability (< 0.1 deg/h).

A front-end capacitive readout circuitry to satisfy this noise performance is required to have extremely low noise, wide dynamic range (> 100 dB), and high tolerance to variations in supply voltage and temperature. It is also highly desirable for the circuitry to have a wide feedback gain control range to be compatible with a wide range of detection capacitances and frequencies.

Existing capacitive detection schemes have limitations in meeting all these requirements. Charge integration using a switched capacitor front-end [1] suffers from folding noise and the parasitic electrical coupling of switching noise. A continuous-time (CT) charge integrator front-end [2] does not suffer from *kT/C* but requires a large feedback resistance to bias the input node. Various techniques, such as the use of controlled impedance FETs and series of subthreshold MOSFETs, have been proposed to implement a large feedback resistance. However, they suffer from large parasitic capacitance due to the large size of the feedback resistor.

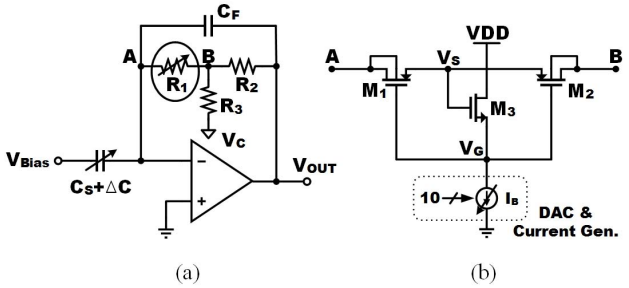

Figure 1: (a) Variable T-network TIA and (b) its variable floating resistor with 10-b current-steering DAC.

A TIA is attractive because the mass of a capacitive sensor can be biased at a DC voltage to eliminate the parasitic electrical coupling of switching noise. A TIA using a resistor T-network with MOSFET [3] has been demonstrated; however, this approach suffers from small output voltage swing and external noise injection due to MOSFET's control voltage through a bonding pad.

In this paper, we introduce a new TIA that employs an on-chip digitally-controlled floating resistor as the variable resistor for a resistor T-network. Our approach has several key advantages over existing approaches such as [3]: 1) a floating resistor obtains much higher linearity than MOSFET [4] and 2) on-chip digital control of the floating resistor with a digital-to-analog converter (DAC) lowers the TIA noise by eliminating injected noise through a bonding pad and can obtain a wide range of precise TIA gains. We also discuss a voltage-and-temperature bias current generator for the DAC and the op-amp and the design of a low-noise op-amp. The prototype IC is tested with a high-performance vibratory MEMS gyroscope [5].

CIRCUIT IMPLEMENTATION

TIA with Floating Resistor T-Network

Figures 1a and 1b illustrate the T-network TIA front-end with a floating resistor and the architecture of the floating resistor [4], respectively. The primary advantage of T-network is that a high feedback resistance (up to several GΩ) can be obtained only using the level of electrical resistance for on-chip resistors (<10s MΩ). Also, the DC offset voltage of the amplifier can be nulled by applying an appropriate correction voltage V_C to R_3.

R_1 can be implemented as a single MOSFET operating in the triode or deep-triode region [3]. A key limitation for this approach is a small output voltage swing range when the load resistance is in the range of several MΩ because of

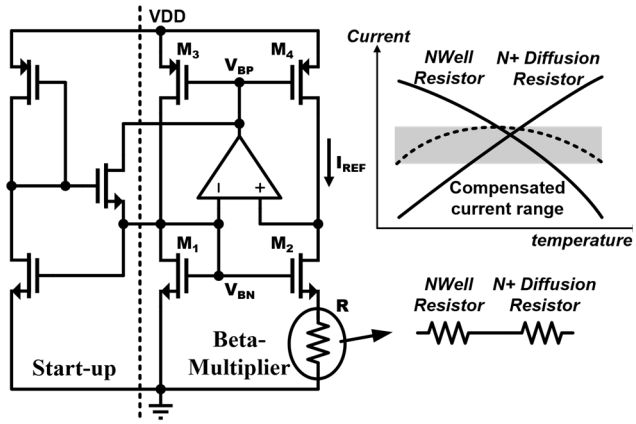

Figure 2: V-T Tolerant Current Generator.

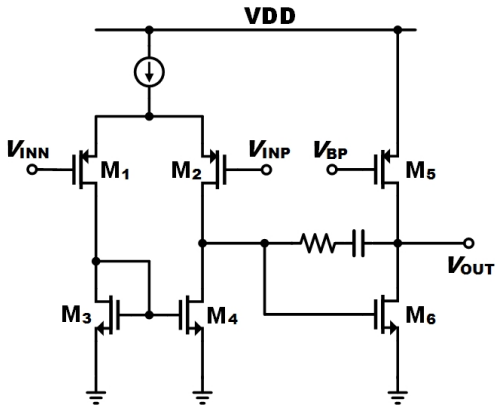

Figure 3: Low-noise Amplifier.

a poor linearity between the current and voltage across the drain and source nodes of a MOSFET. This issue could be addressed with a MOSFET with a long channel length; however, the drawbacks of this approach are a large device size and a large parasitic capacitance.

A floating resistor (Figure 1b) [4] is highly advantageous over a single MOSFET for R_1 due to a wider voltage swing range. A floating resistor consists of 1) two identically-sized PMOS transistors (M_1 and M_2) that are connected symmetrically (*i.e.* their source nodes are shared); and 2) an integrated resistance control block for M_1 and M_2 comprising an NMOS transistor (M_3) and a variable current source. M_1 and M_2 are connected symmetrically so that the sum of their drain-to-source resistances becomes constant regardless of the polarity of the voltage across their drain nodes (*i.e.* terminals A and B) over a wide voltage range. The drain-to-source resistance of M_1 and M_2 is controlled with V_G. V_G is generated from M_3 and a current generator rather than an external voltage because current biasing scheme is less susceptible to process variations. The current source is steered by a 10-bit DAC.

Our circuitry has several attractive features. First, the TIA gain can be controlled precisely to cover a wide range of readout capacitance and frequency ranges. Second, the TIA gain can be actively controlled to compensate for process and temperature variations. Third, the integrated resistance control block reduces the TIA noise by reducing the fluctuation in the feedback resistance by eliminating the transmission of the control signals for the floating resistor through a bonding pad.

From SPICE simulation, we verified that for identical fabrication technology (0.18 μm) and voltage (1.8 V) and for similar TIA feedback gain, the floating resistor approach achieves nearly 10 times larger output voltage swing. We also experimentally confirmed a very large output swing range (~955 $mV_{p\text{-}p}$) can be obtained.

Voltage and Temperature Tolerant Current Generator

A current source is required to have low sensitivity to variations in the supply voltage and temperature. Short-channel transistors made with a deep submicron technology suffers significantly from channel length modulation. We designed a beta-multiplier current reference circuitry with a resistor with a very low temperature coefficient of resistance (TCR) (Figure 2). The beta multiplier consists of two NMOS transistors (M_1 and M_2) with different channel width to length ratios ($W_1/L_1 = 1/K \times W_2/L_2$. $K > 1$); two PMOS transistors (M_3 and M_4) with same W/L; a reference resistor (R) connected between the source node of M_2 and ground; and a differential amplifier whose positive input node is connected to the drain node of M_2 and the negative input node is connected to the gates of M_1 and M_2 and the drain of M_1 [6].

The operating principle of the circuit is described as follows: M_3 and M_4 together with the differential amplifier form a current mirror. The differential amplifier also regulates the drain voltage of M_2 to the drain voltage of M_1 using negative feedback. The current through M_1 and M_2 become identical (= I_{REF}). I_{REF} is related to the dimensions of M_1, M_2, and R to be:

$$I_{REF} \approx \frac{2}{R^2 \beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (1)$$

where $\beta_1 = \mu_n C_{ox}(W_1/L_1)$, μ_n is electron mobility of the MOSFET and C_{ox} is gate oxide capacitance per unit area. This relationship indicates that I_{REF} is nearly independent from supply voltage (VDD) can be generated.

R is designed by connecting an N-well resistor and N+ diffusion resistor in series (Figure 2). The TCR of the N-well resistor and N+ diffusion resistor are around -800 ppm/ºC and +1260 ppm/ºC, respectively. From SPICE simulation, our circuitry achieves a very low current drift of less than ±1% over a temperature range of -20 °C – 80 °C.

Low-Noise Operational Amplifier

A two-stage Miller compensated op-amp (Figure 3) is designed due to its abilities to obtain high gain, large output voltage swing, and low noise. PMOS transistors are used as an input pair. The width of these transistors is designed to be large to reduce size mismatch and offset, substrate coupling noise, and $1/f$ noise. Thermal noise of a PMOS transistor, however, is higher than an NMOS transistor for the same current and device size due to lower transconductance (g_m). The input-referred thermal noise ($\overline{V_{n,thermal}^2}$) and $1/f$ noise ($\overline{V_{n,flicker}^2}$) densities of the op-amp are calculated as follows:

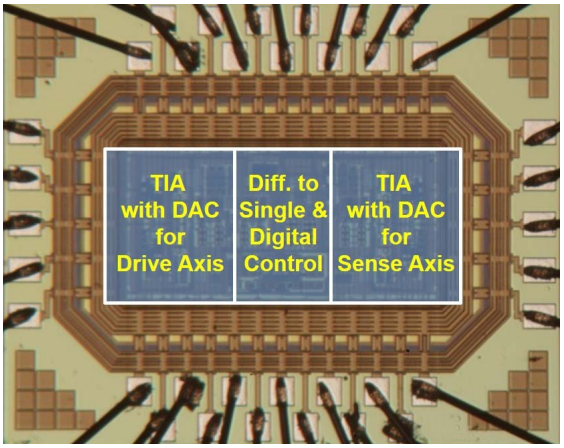

Figure 4: Chip microphotograph (1.7mm×1.3mm).

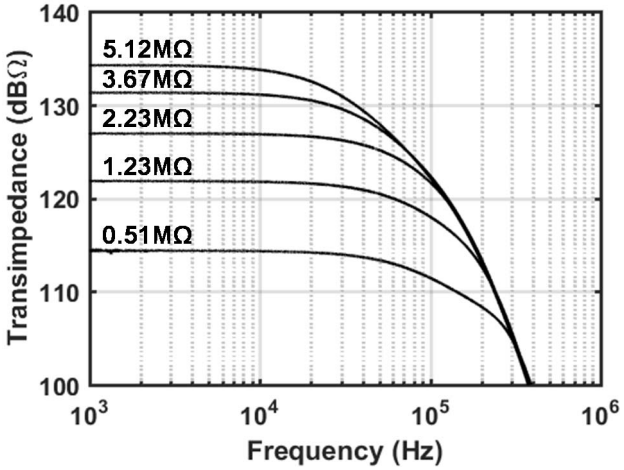

Figure 5: Measured T-network TIA gain.

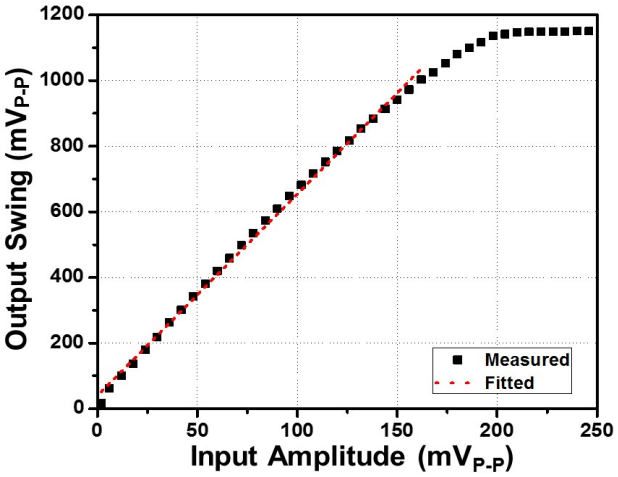

Figure 6: Measured Output Linearity of TIA.

$$\overline{V_{n,thermal}^2} \approx \frac{16kT}{3}\frac{1}{g_{m1}^2}(g_{m1}+g_{m3}) \qquad (2)$$

$$\overline{V_{n,flicker}^2} \approx \frac{2}{C_{oxf}}\left(\frac{K_P}{W_1L_1}+\frac{\mu_nK_nL_1}{\mu_pW_1L_3^2}\right) \qquad (3)$$

where f: frequency, p: PMOS, n: NMOS, $K = \mu C_{ox}$, k: Boltzmann constant, and T: temperature. From Equation (2), thermal noise can be reduced by increasing g_{m1}. g_{m1} can be increased by increasing the current from the current source or by increasing W_1. From Equation (3), $1/f$ noise is inversely proportional to L_1 and L_3^2. Therefore, M_1 is designed with a large channel width and M_3 is designed with a long channel length. Since a large L_3 limits the output signal swing of the first stage of the amplifier, W_3 needs to be also increased. Increasing W_3 does not affect $1/f$ noise.

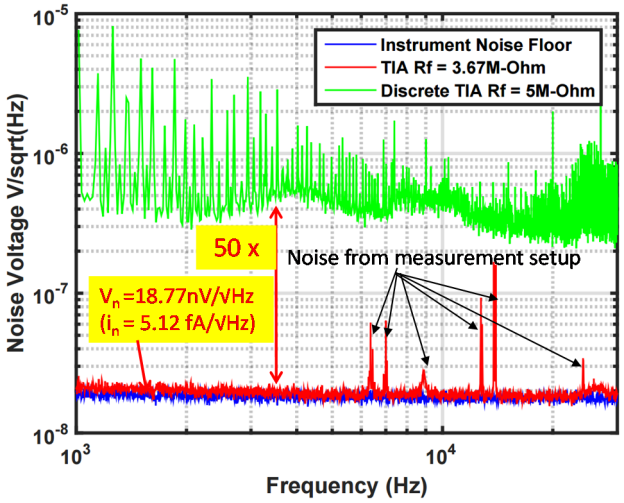

Figure 7: Comparison between output noise spectral densities of TIA ASIC and discrete low-noise TIA (LF353).

MEASUREMENT RESULTS

Circuit Evaluation

The prototype chip was fabricated in a 0.18 µm standard CMOS process with 1.8 V supply voltage (Figure 4). Figure 5 shows the relationship between the frequency and the feedback resistance of the TIA. The TIA has a wide feedback resistance range (510 kΩ – 5.12 MΩ). The wide resistance range is highly useful for compensating gap mismatches of a capacitive sensor or controlling oscillator's amplitude over a wide range when the TIA is used for a front-end capacitive readout circuitry. Figure 6 shows the relationship between the input and output voltage amplitudes of the TIA. A large output swing of ~955 mV_{P-P} was measured for 1.8 V supply, which is approximately 60% larger than the data reported in [3] even with a lower supply voltage.

Figure 7 shows a comparison between the output noise spectral densities of our TIA and a discrete low-noise TIA (LF353). Our circuitry has ~50 times lower noise floor. The input current noise of our circuitry is measured to be 5.12 fA/√Hz at 10 kHz. The dynamic range is calculated by dividing the maximum output voltage by the product of output voltage noise floor and the square root of bandwidth to be 123 dB. Table I summarizes the measured performances of the TIA.

Device and Gyroscope Evaluation

Our TIA is evaluated by interfacing with a MEMS birdbath resonator gyroscope (BRG) [7]. The device is operated in the standard force-rebalance mode [5]. The TIA chip and BRG are directly wire-bonded to a PCB. The PCB is placed inside an Ideal Aerosmith® Aero900 rotation

Table 1: Front-end ASIC Performance Summary

Technology	0.18 µm 1P6M CMOS
Feedback Gain Range	510 kΩ – 5.12 MΩ
Output linearity	~ 955 mV_{P-P}
Input current noise	5.12 fA/√Hz
Minimum Detectable Capacitance	0.45 zF/√Hz
Dynamic Range	123 dB

table at <1 mTorr at room temperature. The frequencies of the $n = 2$ wineglass modes of the BRG are electronically matched to less than 73 mHz ($f_{n=2}$ = 9030.925 Hz and 9030.998 Hz). Further electrical tuning is done using a quadrature cancellation loop. The ring down time of the two modes ($\tau_{n=2}$) are measured to be 14.77 seconds ($Q_{n=2}$ = 419.047k) and 14.14 seconds ($Q_{n=2}$ = 401.176k). A large scale factor of 100 mV/deg/s and excellent angle random walk (ARW < 0.0087 deg/√hr) and bias stability (= 0.0391 deg/hr) are measured. Table II compares the results of this work with other low-noise MEMS gyroscope systems.

Table 2: Comparison of ASIC and Gyroscope Performance

References	[2]	[3][8]	[9]	This Work
Category	Front-end ASIC Performances			
Front-end Architecture	CSA*	TIA	CSA*	TIA
Input current noise (fA/√Hz)	-	88	-	5.12
ΔC_{MIN} (zF/√Hz)	12 (zF)	20**	220	0.45***
Technology (µm)	3	0.6	0.35	0.18
Category	Gyroscope Performances			
Bias instability (°/h)	50	0.16	25	0.0391
Mode matching	No	Yes	No	Yes

*: Charge sense amplifier **: V_{Bias}=40V, f=15kHz
***: V_{Bias}=200V, f=9.03kHz

SUMMARY

This paper describes a novel architecture of a CMOS TIA with one of the lowest reported noise performance and very wide dynamic range. The floating resistor of the TIA provides excellent output linearity. The prototype chip was fabricated in a 0.18 µm standard CMOS process with 1.8 V supply voltage. An input current noise density of 5.12 fA/√Hz and a dynamic range of 123 dB are measured. The circuitry is interfaced with a prototype MEMS gyroscope, which measures excellent noise performance.

ACKNOWLEDGEMENTS

This work is supported by DARPA MRIG award #W31P4Q-11-1-0002. The authors thank Mr. Robert Gordenker for testing support.

REFERENCES

[1] V. Petkov and B. Boser, "A Fourth-order ΣΔ Interface for Micromachined Inertial Sensors," in *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1602–1609, Dec. 2005.

[2] J. A. Geen, S. J. Sherman, J. F. Chang, and S. R. Lewis, "Single-Chip Surface Micromachined Integrated Gyroscope With 50°/h Allan Deviation," in *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1860–1866, Dec. 2002.

[3] A. Sharma, M. F. Zaman, and F. Ayazi, "A 104-dB Dynamic Range Transimpedance Based CMOS ASIC for Tuning Fork Microgyroscopes," in *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1790-1802, Aug. 2007.

[4] A. Tajalli, Y. Leblebici and E.J. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors," in *Electronics Letters,* vol. 44, no. 5, pp. 349-350, Feb. 2008.

[5] C. Boyd, J.-K. Woo, J. Y. Cho, T. Nagourney, A. Darvishian, B. Shiari, and K. Najafi, "Effect of Drive-Axis Displacement on MEMS Birdbath Resonator Gyroscope Performance," in *Inertial Sensors & Systems (Inertial '17),* Kauai, HI, USA, Mar. 2017.

[6] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design Layout and Simulation*, NJ, Piscataway:IEEE Press, 1998.

[7] J. Cho, J.-K. Woo, J. Yan, R. L. Peterson, and K. Najafi, "Fused-Silica Micro Birdbath Resonator Gyroscope (µ-BRG)," in *IEEE Journal of Microelectromechanical Systems*, vol. 23, no. 1, pp. 66-77, Feb. 2014.

[8] A. Sharma, M. F. Zaman, and F. Ayazi, "A Sub-0.2°/hr Bias Drift Micromechanical Silicon Gyroscope With Automatic CMOS Mode-Matching," in *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1593–1608, May 2009.

[9] L. Aaltonen, A. Kalanti, M. Pulkkinen, M. Paavola, M. Kamarainen, and K. A. I. Halonen, "A 2.2 mA 4.3 mm^2 ASIC for a 1000°/s 2-Axis Capacitive Micro-Gyroscope," in *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1682–1692, July 2011.

CONTACT

*K. Najafi, tel: +1-734-763-6650; najafi@umich.edu