A Low-Power, Compact, Adaptive Logarithmic Transimpedance Amplifier Operating Over Seven Decades of Current

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***Abstract*—This paper presents a detailed insight into the design space of wide-range transimpedance amplifiers enabling the design of micro-power, adaptive circuits for integrated current sensing applications. The analysis proves that the power dissipation of the nonadaptive structures varies linearly with dynamic range and quadratically with bandwidth. We present two adaptation techniques, modifying the bias current or output resistance, both of which alleviate this strong dependence on dynamic range. It is shown that adapting the bias current is most suitable for our application which requires a modest bandwidth but very wide dynamic range. Measurements demonstrate operation with currents ranging seven orders of magnitude from 200 fA to 2 μA with an average error of 0.8% and maximum error of 3.4%. The power consumption averaged over this entire range of currents is 3.45 μW. Either signal-to-noise ratio (SNR) or bandwidth can be made to tradeoff with the input current magnitude depending on the application. If the bandwidth is limited to 5 kHz, it achieves an average SNR of 65 dB.**

***Index Terms*—Adaptive circuits, logarithmic compression, low power, nonlinear system, transimpedance amplifier (TIA).**

I. Transimpedance Amplifiers (TIAs)

TRANSIMPEDANCE amplifiers (TIAs) are used in a wide variety of applications ranging from microsystem sensors [1] to optical preamplifiers [2]–[7]. Challenging work on TIAs involving applications where high speed is required with very low currents has been done in [8], [9]. Optical stimulus localization and centroid computation systems [10], [11] also require sensing low currents spanning several decades. Highly integrated systems demanding low power consumption pose especially difficult challenges. Further complicating the problem is the need for wide dynamic ranges, particularly in sensing systems and reprogrammable systems. Sensing systems interface the physical world which is inherently highly dynamic and reprogrammable systems must cater to a wide variety of applications and specifications. We have fabricated such integrated systems, which serve as the basis for this work.

The first system is an on-chip floating-gate programming system requiring a current measurement circuit which indirectly quantifies the amount of charge on the floating gate.

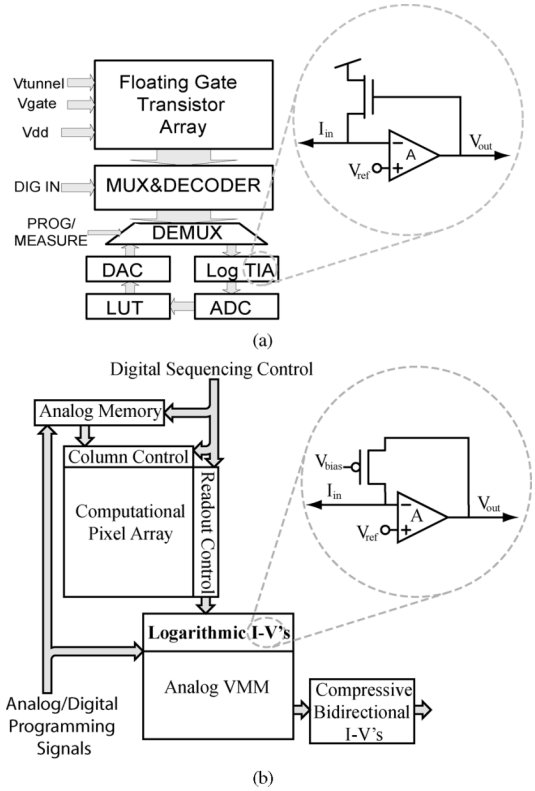

Fig. 1. Applications of wide dynamic range TIA. (a) Block diagram of an on-chip programming system. The decoder and the multiplexors allow selection of a particular gate. The log TIA and the analog–digital converter produce a digital representation of the drain current. This is used to feedback the next drain voltage to be used in programming. (b) Block diagram of a computational imager. The small but widely varying photodiode currents are cascoded and converted to voltage logarithmically by the log TIA. The logarithmic representation allows efficient multiplications in the following vector matrix multiplier.

Traditionally, this has been accomplished by measuring the channel current in a transistor using a pico-ammeter. But, this makes the programming process slow since the current measurement time dominates the programming cycle [12]. A fully on-chip programming methodology as depicted in Fig. 1(a) would drastically hasten the programming time of large arrays of floating gates that are commonly used in many neuromorphic applications. The major bottleneck in such a system is the TIA capable of faithfully converting currents ranging from picoamperes to microamperes with resolution > 8 bits and moderate (few kilohertz) bandwidth. Power dissipation and chip area pose additional constraints on the design.

Manuscript received August 15, 2006; revised May 5, 2007. This paper was recommended by Associate Editor G. Cauwenberghs.

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Digital Object Identifier 10.1109/TCSI.2007.905657

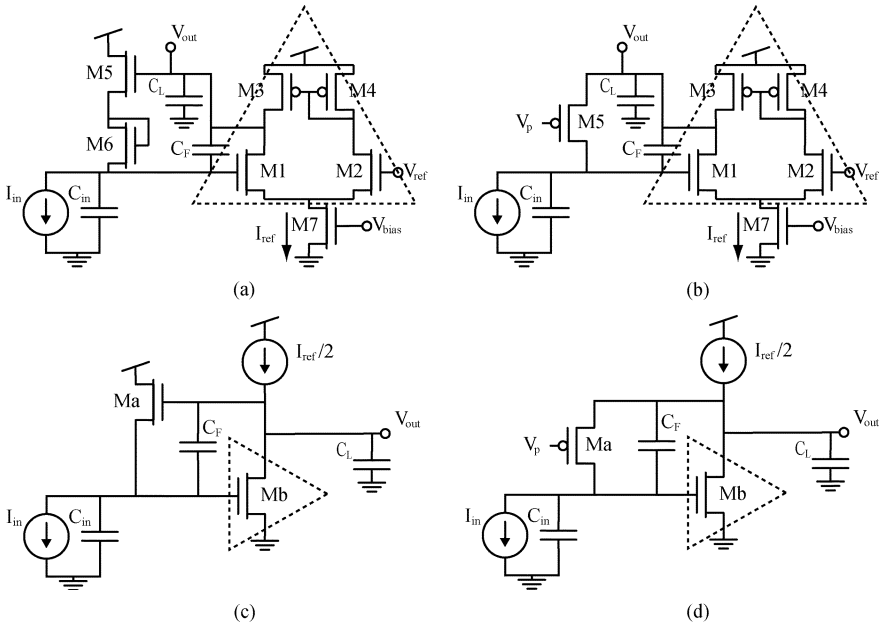

Fig. 2. Topologies of logarithmic TIA. (a) Common-drain logarithmic TIA. (b) Common-gate logarithmic TIA. (c) Simplified version of (a) for small-signal analysis. (d) Simplified version of (b) for small-signal analysis.

A second system where a wide range TIA plays a crucial role is a focal-plane imaging system as depicted in Fig. 1(b). The widely varying pixel currents are converted to a voltage by this block and are further processed by other blocks which utilize translinear computation. For real-time imaging, amplifiers in this system have an additional design constraint of high bandwidth. For this reason, applications requiring very wide dynamic range and low noise need some form of gain adaptation.

Logarithmic compression of the current using a MOSFET in subthreshold has been explored to solve the issue of obtaining a wide dynamic range [8], [9]. For proper phase margin, all of these approaches assume that the poles of the amplifier are far away from the dominant pole set by the feedback element. However, satisfying this assumption entails dissipating considerable power in the amplifier to push the pole away from the maximum input pole set by the highest input current. This simple approach is particularly wasteful if it is known that most of the time the input current will be much lower than the maximum value. A solution where the bias current of the amplifier is adjusted has been proposed in [13]. However, the adaptation loop requires a large off-chip capacitor for stability and also degrades the signal-to-noise ratio (SNR) of the system.

The adaptive logarithmic circuit described in this paper is part of a chip designed for programming floating gates. We analyze in detail the tradeoffs involved in a power efficient design of such a system and propose two adaptive strategies to accomplish the same. The two adaptation methods described are very general and can be used in a wide variety of applications depending on specified bandwidth and dynamic range. We show that adapting bias currents is the most power optimal solution for this application. The problem of temperature compensation in these logarithmic amplifiers has been discussed extensively [14], [15] and are not discussed here.

In Section II, the design parameters are introduced and the tradeoffs underlined. In Section III, possible topologies of the logarithmic amplifier are introduced along with a small-signal analysis and discussions on power dissipation constraints of each structure. Section IV introduces two methods of adaptation to stabilize the circuit for wide range of input currents while maintaining low-power operation. The power requirements of each adaptation method are analyzed and cases where each method would be advantageous are detailed. Section V discusses the noise performance of the circuit showing tradeoffs between bandwidth and SNR. Finally, we compare our approach with others and draw conclusions in the last section.

II. Overview of Logarithmic Amplifier Design: Problem Statement

The fundamental function of a logarithmic TIA is the generation of an output voltage proportional to the log of an input current. The traditional implementation of this logarithmic I–V conversion is done by a passing the current into a diode, a bipolar junction transistor (BJT), or a MOSFET operating in its subthreshold, exponential region of operation. In the BJT and subthreshold MOSFET, the current may be passed into a terminal with large exponential conductance (emitter or source), or a node performing a diode connected configuration. The problem with these elements is that the small-signal bandwidth at low currents is limited, since the G_m of these elements is set by the input current $G_m = I_{\text{in}}/U_T$, where U_T is the thermal voltage equal to kT/q. The approach then becomes one of using an amplifier in a feedback loop, as in Fig. 2, to alter the effective conductance to be AG_m, thus increasing the bandwidth by the amplifier gain A from G_m/C to AG_m/C. The primary design parameters and corresponding notations that are used in the remaining paper are listed in Table I for convenience.

The final parameter $I_{\text{in,max}}$ or DR, is relevant because the design is a multiple pole, feedback system, which implies another design specification of stability. The functions to be optimized can be power consumption, noise, and area. In this work

TABLE I
LIST OF SYMBOLS

BW	Desired bandwidth.
A	Amplifier gain.
$I_{\rm ref}$	Bias current in the amplifier.
$C_{\rm IN}$	Capacitance at the input node of the amplifier.
$C_{\rm F}$	Capacitance in feedback across the amplifier.
$C_{\rm L}$	Capacitance at the output of the amplifier.
$I_{\rm in,min}$	Minimum Input Current.
$I_{\rm in,max}$	Maximum Input Current.
DR	Dynamic range $= \frac{I_{\rm in,max}}{I_{\rm in,min}}$.

we optimize the power consumption. The analysis will show the basic design of such a structure assuming subthreshold operation yields an amplifier current consumption given by

$$I_{\rm ref} > U_T^2 \frac{C_{\rm IN} C_L ({\rm BW}^2)({\rm DR})}{I_{\rm in,min}}. \tag{1}$$

So, the challenges include coping with a power requirement that increases linearly with the required dynamic range and quadratically with bandwidth. It will be shown how adaptive approaches can effectively reduce the power consumption's relation to dynamic range. This is critical in the systems where the desired dynamic range is several orders in magnitude and the reduction is significant.

III. LOGARITHMIC TIA: TOPOLOGIES

In this section, we introduce two topologies which operate as wide dynamic range TIAs by log compressing the input current using the exponential characteristics of MOS transistors in the subthreshold regime. The small-signal transfer function is derived first, followed by a discussion on minimum power dissipation to meet bandwidth and dynamic range specifications. In the remaining sections of the paper, it is assumed the desired specifications of the TIA conform with the floating-gate programming application.

A. Common-Drain Topology

Fig. 2(a) depicts the structure of a common-drain logarithmic TIA. It should be noted that in our convention, we name the TIA by the type of feedback stage employed and not the type of amplifier used. Hence, a common-drain logarithmic amplifier has a common drain or a source–follower feedback stage as in Fig. 2(a). Transistors M_1–M_4, form a basic differential amplifier with M_7 as the current source. M_5 and M_6 form the feedback element. The operation of the circuit is as follows: the amplifier tries to hold the input node fixed at $V_{\rm ref}$, thus forcing $I_{\rm in}$ to flow through M_5 and M_6 and not the capacitor. M_5 and M_6 form an equivalent transistor with an effective $\kappa, \kappa_{\rm eff}$ lower than that of a single transistor, where κ is the inverse of the subthreshold slope factor [16]. The logarithmic conversion of current to voltage is obtained naturally by the exponential I–V relation of a MOS transistor in subthreshold. The dc output voltage can be expressed as

$$\begin{aligned} V_{\rm out} &= \frac{V_{\rm ref} + (\kappa+1) U_T \ln\left(\frac{I_{\rm in}}{I_n}\right)}{\kappa^2} \\ &= \frac{V_{\rm ref}}{\kappa^2} + \frac{U_T}{\kappa_{\rm eff}} ln\left(\frac{I_{\rm in}}{I_n}\right) \end{aligned} \tag{2}$$

where U_T is the thermal voltage and I_n is the pre-exponential factor in the I–V relation of a subthreshold nMOS.

A version of this circuit was created in 0.5-μm CMOS. Fig. 3 shows the measured and simulated current voltage relation with both curves showing good correlation. The slope of the curve changes at high currents because the transistor transitions from below threshold operation to above threshold operation and thus the voltage at the gate increases in proportion to the square root of current instead of the logarithm. A second-order curve fit to this plot for currents ranging from 200 fA to 2 μA gives a linear slope of 0.55, which translates to $\kappa_{\rm eff} = 0.47$. The ratio of the second-order term to the first-order term is -45 dB.

1) Small-Signal Analysis: To generate a small-signal transfer function for the structure, Fig. 2(c) can be used. It is to be noted that M_b in Fig. 2(c) represents the amplifier while M_a in Fig. 2(c) represents M_5 and M_6 in Fig. 2(a) and has an effective degenerate G_{ma} given by $\kappa G_{m5}/(\kappa+1)$, which actually encodes the effect of $\kappa_{\rm eff}$. This simplification ignores the effect of the current-mirror pole at the gates of M_3-M_4 as it occurs at much higher frequencies compared with the dominant pole of the amplifier at its output. Also a zero at exactly twice the frequency of the pole is created due to the two paths to the output reducing its effect even more. However, it should be noted that this simplified model is used only for analysis, while simulations are performed on the actual circuit. Analyzing Fig. 2(c), we get

$$\begin{aligned} \frac{V_{\rm out}(s)}{I_{\rm in}(s)} &\approx \frac{A}{G_{ma}(1+A)} \frac{1 - \frac{sC_F}{G_{mb}}}{1 + as + bs^2} \\ a &= \frac{C_L G_{ma} + C_F G_{mb} + C_{\rm IN} G_{\rm ob}}{G_{ma} G_{mb}} \\ b &= \frac{C_F (C_{\rm IN} + C_L) + C_{\rm IN} C_L}{G_{ma} G_{mb}} \end{aligned} \tag{3}$$

where C_F is the sum of $C_{\rm gdb}$, $C_{\rm gsa}$ and any explicit compensation capacitor placed across M_b, $G_{\rm ob}$ is the output conductance of the amplifier and A is the gain of the amplifier equalling $G_{mb}/G_{\rm ob}$. It should be noted that $C_{\rm gsa}$ in the above equation is the equivalent capacitance due to the series combination of $C_{\rm gs5}$ and $C_{\rm gs6}$ in Fig. 2(a) and is thus equal to half the value of any of them (assuming M_5 and M_6 are similarly sized). The poles of the circuit are calculated considering two particular cases of interest.

Case I: $C_{\rm IN} \gg C_F$

This is the most frequently encountered scenario when the input capacitance dominates the frequency response. Using the

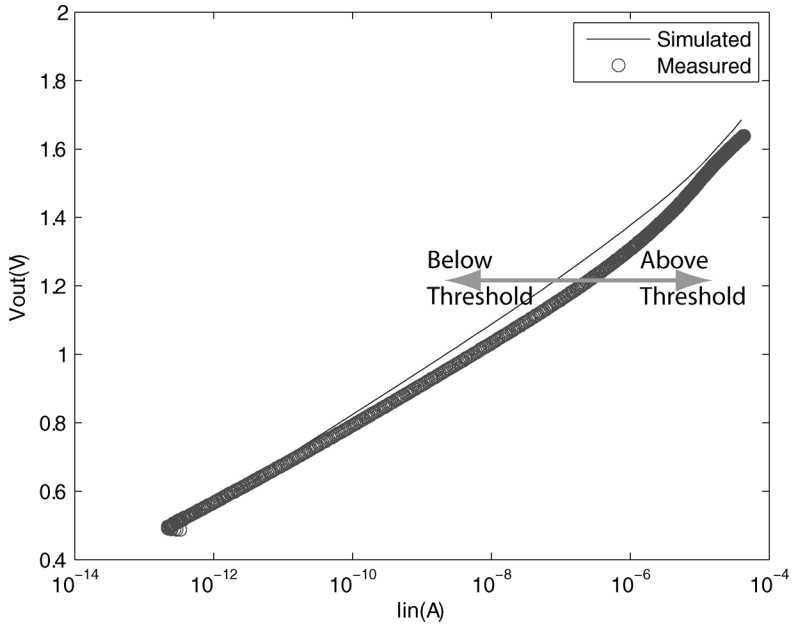

Fig. 3. Current–voltage characteristics. Measured and simulated current to voltage curves at dc. At higher currents, the slope becomes steeper because of the MOSFET entering above threshold region from subthreshold.

dominant pole approximation and noting that $G_{mb} \gg G_{ma}$, the poles are given by

$$p_1 \approx -\frac{AG_{ma}}{C_{\rm IN}}; \quad p_2 \approx -\frac{G_{\rm ob}}{C_F + C_L}. \tag{4}$$

Case II: $C_F \gg C_{\rm IN}$

In this case, the input capacitance is so small that generally an explicit C_F is needed to robustly design the input pole. In this case

$$p_1 \approx -\frac{G_{ma}}{C_F}; \quad p_2 \approx -\frac{G_{mb}}{C_{\rm IN} + C_L}. \tag{5}$$

The value of p_1 can be intuitively computed by noting that the total capacitor at input $C_{\rm tot}$ and the input impedance $Z_{\rm in}$ are given by

$$C_{\rm tot} = C_{\rm IN} + AC_F = A \times C_{\rm eff}; \quad Z_{\rm in} \approx \frac{1}{AG_{ma}} \tag{6}$$

where A is the gain of the amplifier. Thus, the amplifier effectively reduces any input capacitance by the magnitude of its gain. Also, it is important to realize that adding the degeneration transistor does not hamper the bandwidth much since the increase of $Z_{\rm in}$ is almost compensated by the decrease in C_F.

From the above analysis, we see that p_1 depends on the input current and thus moves to higher frequencies as the input current increases.

2) Power Dissipation Limits: In this text, minimizing power dissipation is used synonymously with minimizing $I_{\rm ref}$, the bias current of the amplifier. It is assumed that $I_{\rm ref}$ flows through M_b in Fig. 2(c) and (d). κ is assumed 1 for simplicity. It is also assumed that typically $C_{\rm IN} \gg C_F$ unless otherwise mentioned.

The conditions constraining $I_{\rm ref}$ are $\text{bandwidth} > \text{BW}$ and $\text{phase margin} > 45^\circ$ for all currents. Since the minimum bandwidth occurs when the input current is minimum, it is sufficient to ensure that the bandwidth at minimum input current is larger than BW. Thus, we need

$$\frac{AI_{\rm in,min}}{C_{\rm IN}U_T} > \text{BW} \tag{7}$$

where it is assumed that $C_F < C_{\rm IN}/A$. Equation (7) defines the minimum gain needed to meet the bandwidth specification and enables the designer to choose the number of stages. Here, we assume that a one-stage structure is sufficient. The second equation comes from the phase margin specification

$$p_{2,\rm OPENLOOP} > \text{BW}_{\max} = \frac{AI_{\rm in,max}}{C_{\rm IN}U_T}. \tag{8}$$

This second pole of the system is actually the first pole of the amplifier. Thus, the power dissipation of the amplifier can be found by considering it to be proportional to the gain–bandwidth product

$$I_{\rm ref} > \frac{U_T^2 C_L C_{\rm IN} (\text{BW})^2 \text{DR}}{I_{\rm in,min}}. \tag{9}$$

Equation (9) is a very important equation since it shows the dependence of the power dissipation on the design parameters. The power can be seen to be proportional to dynamic range, input, and output capacitances and the square of the bandwidth. The term $I_{\rm in,min}$ in the denominator shows that the power is actually a function of the desired speedup or $\text{BW}U_T C_{\rm IN}/I_{\rm in,min}$. It should be noted that the term $I_{\rm in,min}/U_T C_{\rm IN}$ represents the natural bandwidth of the system.

Fig. 4 demonstrates the dependence of the power dissipation on bandwidth and dynamic range. This strong dependence can be nullified to a great extent by using adaptation as will be shown later.

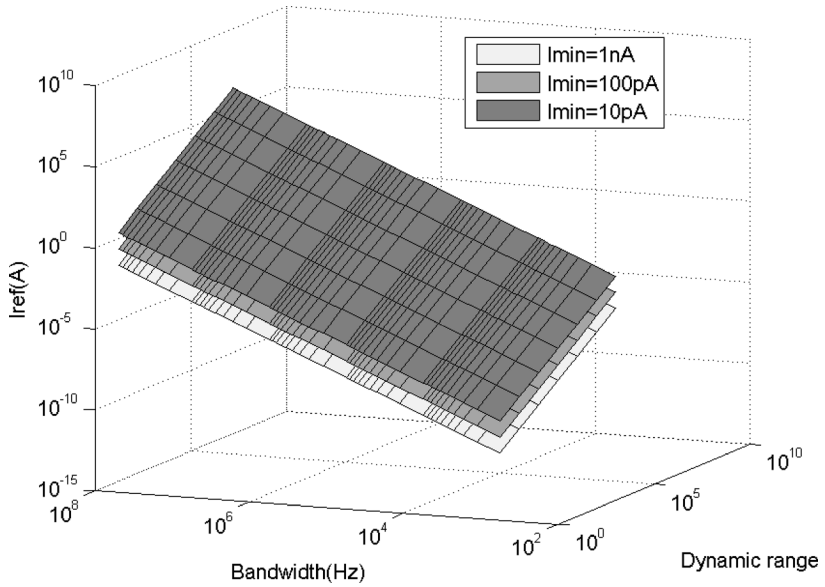

Fig. 4. Power requirement of nonadaptive log TIA. Plot showing dependence of power dissipation on dynamic range is linear and on bandwidth is quadratic. Also the required power increases for lower values of $I_{\mathrm{in,min}}$ showing dependence of power on speedup.

B. Common-Gate Topology

Fig. 2(b) depicts the structure of a common-gate logarithmic TIA. Again, a common-gate TIA refers to an amplifier with a common-gate stage in feedback. The amplifier structure is kept similar to the previous case. Only one transistor M_5 is shown as the feedback element, though source degeneration like the earlier case may be used here as well. The operating principle is similar to what has been previously discussed. The logarithmic conversion is obtained from the subthreshold exponential current relationship between current through M_5 and the source voltage of M_5. Thus, the logarithmic relationship is limited to the subthreshold region of operation for M_5

$$\begin{aligned} I &= I_p e^{(\kappa(V_{\mathrm{dd}}-V_g)-(V_{\mathrm{dd}}-V_{\mathrm{out}}))/U_T} \\ V_{\mathrm{out}} &= ln\left(\frac{I}{I_p}\right) U_T + \kappa V_g + (1-\kappa)V_{\mathrm{dd}} \end{aligned} \tag{10}$$

where U_T is the thermal voltage, I_p is the pre-exponential factor in the I–V relation of a subthreshold pMOS, and V_g is the bias gate voltage.

1) Small-Signal Analysis: Fig. 2(d) can be used to generate a small-signal transfer function for the common-gate structure. Here again, M_b represents the amplifier while M_a represents the feedback element. Analyzing Fig. 2(d), we get

$$\begin{aligned} \frac{V_{\mathrm{out}}(s)}{I_{\mathrm{in}}(s)} &\approx \frac{1}{G_{\mathrm{sa}}} \frac{1-\frac{sC_F}{G_{mb}}}{1+as+bs^2} \\ a &= \frac{C_{\mathrm{IN}}}{G_{mb}} + \frac{C_F}{G_{\mathrm{sa}}} + \frac{(C_{\mathrm{IN}}+C_F)}{AG_{\mathrm{sa}}} \\ b &= \frac{C_{\mathrm{IN}}C_F + C_L C_{\mathrm{IN}} + C_L C_F}{G_{\mathrm{sa}} G_{mb}} \end{aligned} \tag{11}$$

where G_{sa} is the source conductance of M_a and other symbols are as described previously. Here, C_F is the sum of the C_{gd} of M_b and any explicit compensation capacitor, with no contribution from M_a as in the common-drain topology. Most amplifiers beyond a single transistor amplifier would make the C_F term insignificant. Here, we consider only the case $C_{\mathrm{IN}} \gg C_F$ as that is representative of the scenario is which this structure is used. Using the dominant pole approximation and noting that $G_{mb} \gg G_{ma}$, the poles are given by

$$p_1 \approx -\frac{AG_{\mathrm{sa}}}{C_{\mathrm{IN}}}; \quad p_2 \approx -\frac{G_{\mathrm{ob}}}{(C_L+C_F)}. \tag{12}$$

So, the dominant pole is set by the input node which includes the conductance of the feedback transistor. Again, it is clear that as the input current increases, p_1 increases proportionally.

2) Power Dissipation Limits: The power dissipation constraints on the common-gate structure based on small-signal parameters exactly follows that of its common-drain counterpart. The small-signal analysis sets a minimum requirement on I_b, the current flowing through the amplifier transistor M_b. However, since the input current is sourced from the same current supply as the amplifier, I_{ref} must be larger than the maximum possible input current $I_{\mathrm{in,max}}$, i.e.,

$$I_{\mathrm{ref}} = I_{\mathrm{in,max}} + I_{b,\mathrm{max}}. \tag{13}$$

Hence, the common drain is always more power efficient than the common gate, though this may not be significant if the requirements of the system dictate that $I_{b,\mathrm{max}}$ need be much larger than $I_{\mathrm{in,max}}$. However, the common- gate topology avoids a fundamental limit of the common-drain configuration. In the common-drain configuration, the C_{GS} of M_a is the minimum value of C_F, which gets Miller multiplied by the gain of the amplifier. This inherently sets a limit on the maximum bandwidth attainable (f_t) at a particular input current. So if the desired bandwidth is larger than this, the only option is the common-gate topology. With these points in mind we shall focus on the common-drain topology in the remainder of the paper.

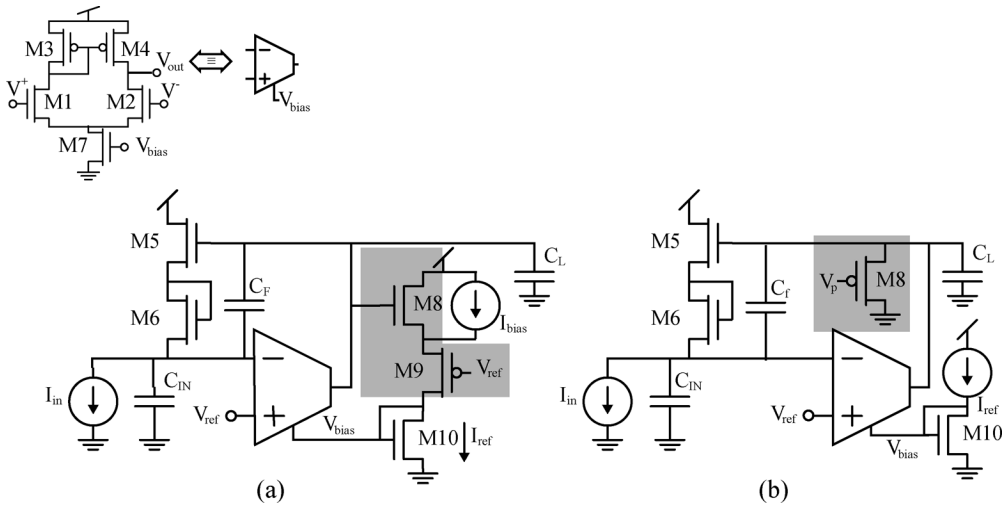

Fig. 5. Topologies of adaptation. (a) Circuit for adaptation of amplifier bias current based on input current. The output voltage is taken as a representation of the input current and used to produce $I_{\rm adapt}$. (b) Second scheme using a pMOS in the adaptive network to reduce the output resistance and hence gain of the amplifier when the input current is large. Thus, loop stability is maintained over the current range.

IV. Adaptation in the Logarithmic Amplifier

In the last section, it was shown that the small-signal poles of the circuit move depending on input current. Two possible ways of designing this circuit to be stable over a wide range of input currents are as follows.

1) For maximum bandwidth at lowest input currents, bias the amplifier by a large current to move p_2 sufficiently higher than the largest possible value of p_1. But this solution obviously entails large power dissipation.
2) For minimum power dissipation, fix a particular bias current and then suitably choose C_F such that largest p_1 is sufficiently smaller than p_2. This clearly sacrifices bandwidth.

In this section, we explore two solutions which elegantly tradeoff bandwidth and power to meet the specifications. The properties of each adaptation method are discussed first followed by a derivation of its power requirements.

A. Configuration I: Adaptation of Amplifier Bias Current

The first method senses the input current magnitude and uses it to set the amplifier's bias current. This method is particularly useful for wide dynamic range systems as will be shown.

1) Operation: Fig. 5(a) depicts the schematic of the bias current adaptation method. Transistors M_8 and M_9 replicate $I_{\rm in}$ to produce the adaptive current $I_{\rm adapt}$. M_9 acts as a follower to hold the source of M_8 constant. In a small-signal sense, the source of M_8 sees an impedance of $1/G_{m9}$. Since the difference between $V_{\rm out}$ and $V_{\rm ref}$ encodes the value of $I_{\rm in}$, $V_{\rm ref}$ is applied to the gate of M_9 to make $I_{\rm adapt}$ directly dependant on $I_{\rm in}$. $V_{\rm ref}$ sets the voltage across the current source being measured and hence varies with application. The current through M_{10} is mirrored with a typical gain of $K \approx 10$. To find an expression for $I_{\rm adapt}$, we equate the currents through M_8 and M_9 to obtain

$$I_8 = I_n e^{(\kappa V_{\rm out} - V_{\rm S})/U_T}; I_9 = I_p e^{(\kappa V_{\rm S} - V{\rm ref})/U_T}$$
$$I_{\rm adapt} = K I_{\rm in} e^{((1-\kappa)V_{\rm ref} - \alpha)/((1+\kappa)U_T)} \quad (14)$$

where $V_{\rm S}$ is the voltage at the source of M_8 α is given by $U_T \ln(I_n/I_p)$ and other symbols are as previously described. The adaptation circuitry moves p_2 by increasing the tail current of the differential amplifier but does not modify $V_{\rm out}$ due to the high common-mode rejection ratio (CMRR) of the amplifier. A current source is added parallel to M_8 to ensure that a minimum bias current always flows through the differential pair ensuring a minimum amplifier speed. This helps particularly in step-responses for low currents. The loop gain of this adaptation loop is very low due to the high CMRR of the amplifier and thus there is no possibility of instability. Another attractive property of this adaptation is that any noise contributed by the transistors M_8–M_{11} is rejected by the CMRR. The bandwidth of the adaptation loop is set by the sum of $I_{\rm in}$ and the fixed bias current. In this implementation, p_1 is always the dominant pole. Consequently, bandwidth always scales linearly with G_{m5}. G_{m5} varies linearly with $I_{\rm in}$ when M_5 is in subthreshold and as the square root of $I_{\rm in}$ when M_5 is above threshold.

The bandwidth of the circuit can be improved slightly by including cascode transistors in the differential amplifier as it would remove the contribution of $C_{\rm gd1}$ to C_F. This scheme of adapting the bias current can be applied to other amplifier structures like a folded cascode amplifier or a standard nine transistor OTA. The simulated plots of the Open Loop gain of the TIA biased at a baseline value of $I_{\rm ref} = 128$ nA are shown in Fig. 6. The top plot shows that without adaptation loop bandwidth stops increasing with input current when the input current crosses the value of ≈ 70 nA indicating that the dominant pole switched from input to output. The bottom plot for the adaptive amplifier shows the loop bandwidth increasing uniformly with input current indicating that the input pole is always dominant. Fig. 8 shows the measured bandwidth of this configuration with increasing input currents. The slope becomes smaller at higher currents because the feedback transistor moves into above threshold region. From this plot, the value of $C_{\rm eff}$ is extracted to be 22 fF. Fig. 7 demonstrates measured adaptation of the bias current of the amplifier. The total current drawn from

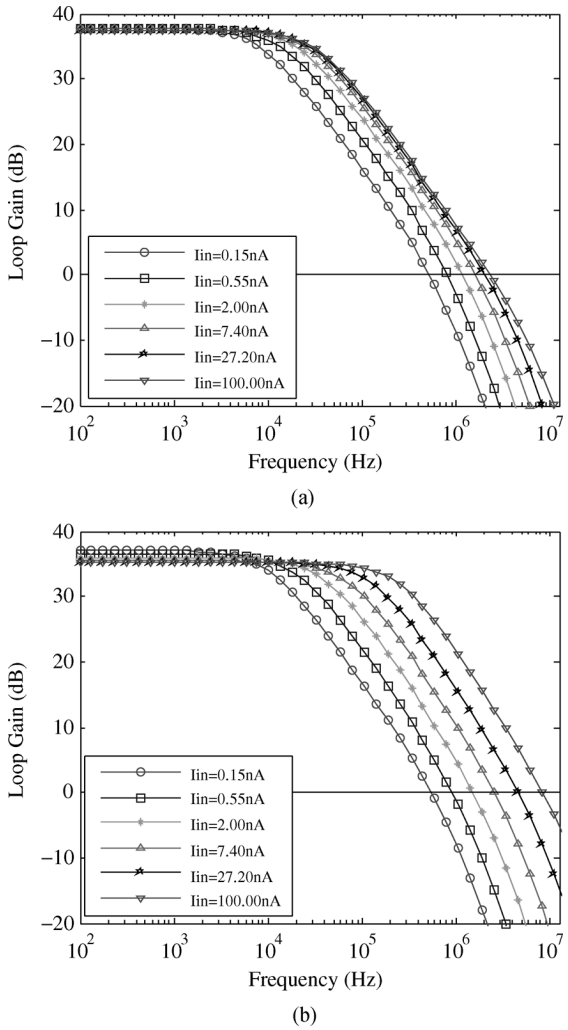

Fig. 6. Loop gain of bias adaptation technique. (a) Without adaptation the bandwidth does not increase uniformly with current indicating that the output pole becomes dominant for large input currents. (b) With adaptation the loop bandwidth increases with input current indicating that the output pole moves to higher frequencies with increasing input current.

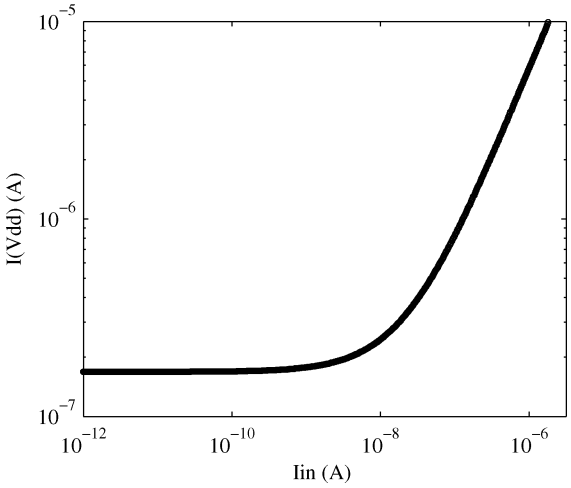

Fig. 7. Bias current adaptation. Measured current drawn from the power supply demonstrating adaptation of the amplifier bias. The curve is flat initially when the adaptation current is smaller than the baseline value of $I_{\rm ref}$ set at 128 nA.

the power supply is initially dominated by the baseline value of $I_{\rm ref} = 128$ nA when the adaptation current is much smaller than that, but after a certain value of $I_{\rm in}$ the adaptation current dominates the total current. From this curve, the average (geometric mean) power consumed from the 3.3-V power supply is 3.45 μW. In the next subsection, we discuss the power dissipation limit for this type of adaptation.

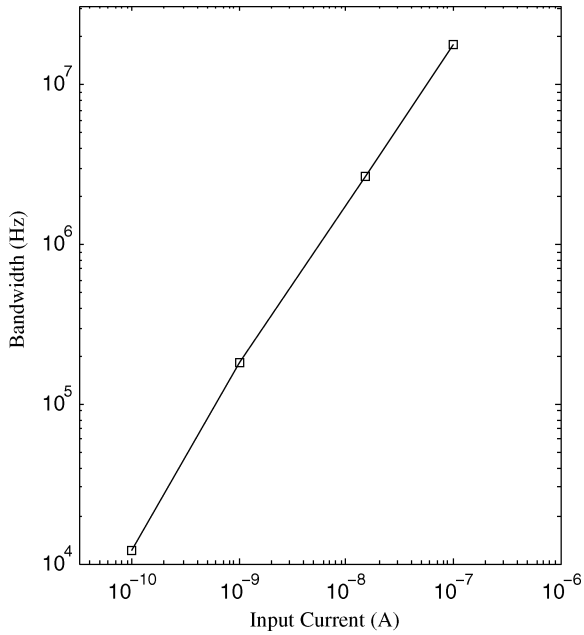

Fig. 8. Variation of bandwidth. Measured small-signal bandwidth based on step responses of configuration I. From this plot, we extract the value of $C_{\rm eff}$ to be 22 fF.

2) Power Dissipation: The first constraint based on bandwidth requirement is the same as (7). For the second constraint, we know that $I_{\rm ref}$ in this case is variable (as it is adapting) and relate it to the value of $I_{\rm in}$

$$p_{2,\rm OPENLOOP} \geq \frac{AI_{\rm in}}{C_{\rm IN}U_T} \tag{15}$$

where the symbols used were introduced in the last section on power dissipation. Similar to previous sections, the power is found by considering it to be proportional to gain bandwidth

$$I_{\rm ref} > \frac{U_T^2 C_L C_{\rm IN} ({\rm BW})^2 I_{\rm in}}{I_{\rm in,min}^2}. \tag{16}$$

In order to find the average power dissipation it should be noted that due to the nature of the data (varying over decades), the geometric mean is the proper measure of average. Therefore

$$I_{\rm ref}({\rm avg}) = \frac{U_T^2 C_L C_{\rm IN} ({\rm BW})^2 \sqrt{\rm DR}}{I_{\rm in,min}}. \tag{17}$$

Thus, comparing (9) and (17), we see that adaptation improves the power dissipation by a factor of the square root of the dynamic range which can be as large as one thousand for a system operating over six decades of current.

B. Configuration II: Adapting Output Resistance of the Amplifier

The second method reduces the gain of the amplifier at higher input currents when the speedup requirement is typically much lower. It achieves this gain reduction by lowering the impedance at the amplifier's high gain node, which pushes the amplifier's dominant pole to higher frequencies.

1) Operation: The second adaptation method is depicted in Fig. 5(c). The current in transistor M_8 approximately replicates the variations in $I_{\rm in}$. As $I_{\rm in}$ increases so does $V_{\rm out}$. Being the source voltage of M_8, an increase in $V_{\rm out}$ increases the current through M_8. As its conductance comes in parallel to the amplifier's output conductance, it starts resistively loading the output of the amplifier at high enough $I_{\rm in}$ values. This gain reduction at higher current values allows the feedback loop to be stable even when p_1 approaches p_2. Since the loading depends on the value of V_p with respect to $V_{\rm out}$, V_p is chosen from simulations based on the other parameter values. In practice, it is advisable to allow for trimming V_p to account for variation in the estimated capacitances which might affect the phase margin at some currents. This method of adaptation assumes that the desired bandwidth does not scale with input current as the lowering of the loop gain means $C_{\rm eff}$ increases at higher currents. The design has to be such that the increase in $I_{\rm in}$ and $C_{\rm eff}$ allow the system to maintain a minimum bandwidth over the entire range of currents. However this method requires that the amplifier supply the input current directly thus necessitating the amplifier bias current to be larger than the maximum input current. In this sense, it is quite similar to the common-gate topology of logarithmic amplifiers and hence dissipates more power for wide dynamic range inputs. The significance of this limitation depends on whether the amplifier already required currents larger than $I_{\rm in,max}$ to satisfy the BW requirements at $I_{\rm in,min}$. Fig. 9 demonstrates the effect of gain reduction with increasing input current to maintain stability.

2) Power Dissipation: Following the earlier derivations, we use the constraint that the minimum desired bandwidth is BW to satisfy

$$\begin{aligned}\mathrm{BW} &\le \frac{G_{ma}}{C_F+\frac{C_{\rm IN}}{A}} \approx \frac{I_{\rm in}}{U_T\frac{C_{\rm IN}}{A}} \\ &\Rightarrow I_{\rm ref} \ge \frac{AI_{\rm in}(I_{\rm in}+U_TC_{\rm IN}\mathrm{BW})}{AI_{\rm in}-U_TC_{\rm IN}\mathrm{BW}} = f(I_{\rm in}) \quad (18)\end{aligned}$$

where $G_{\rm ad}$ is the source conductance of the adaptation MOS added to the output of the amplifier. So, $I_{\rm ref}$ has to be always larger than $f(I_{\rm in})$ when $I_{\rm in}$ varies over a specified range. We can make some approximations to get a rough idea about the range of $I_{\rm ref}$ based on this equation. If $\mathrm{DR} > 10A$, $I_{\rm ref} > I_{\rm in,max}$ is a sufficient condition. If $\mathrm{DR} < A/10$, $I_{\rm ref} > AI_{\rm in,min}$ is the pertinent equation. For the general case, a solution can be graphically obtained by plotting $f(I_{\rm in})$. The second constraint using the phase margin condition can be obtained as

$$\begin{aligned}\frac{G_{\rm ad}+G_{\rm o2}}{C_L} &\ge \frac{AI_bI_{\rm in}}{U_TC_{\rm IN}(AI_{\rm in}+I_b)} \\ &\Rightarrow I_{\rm ref}^2 + I_{\rm ref}I_{\rm in}\left(2A-\frac{A^2C_L}{C_{\rm IN}}\right) \\ &\quad + A^2I_{\rm in}^2\left(1+\frac{C_L}{C_{\rm IN}}\right) \ge 0. \quad (19)\end{aligned}$$

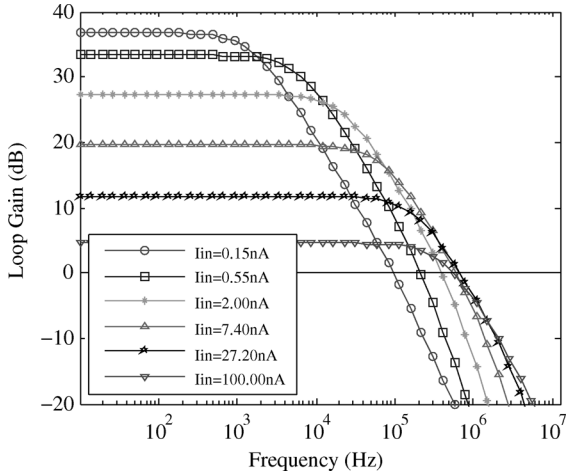

Fig. 9. Loop gain of gain adaptation technique: The loop gain for configuration II drops as current increases. This assures stability while ensuring a minimum bandwidth is still obtained.

From (19), we can infer the range of $I_{\rm ref}$ under some simplifying assumptions.

Case I: $AC_L/C_{\rm IN} \gg 1$

Equation (19) reduces to

$$I_{\rm ref} \ge A^2I_{\rm in,max}\frac{C_L}{C_{\rm IN}} = \frac{U_T^2C_LC_{\rm IN}(\mathrm{BW})^2(\mathrm{DR})}{I_{\rm in,min}}. \quad (20)$$

Comparing this with (17), it is clear that this method consumes more power than adapting $I_{\rm ref}$.

Case II: $AC_L/C_{\rm IN} < 2$

In this case, (19) does not put any constraint on $I_{\rm ref}$. The only constraint is from (18). Firstly, assuming $\mathrm{DR} > 10A$, we get

$$I_{\rm ref} \ge I_{\rm in,max} = \frac{\mathrm{DR}}{A}\frac{U_T^2C_LC_{\rm IN}(\mathrm{BW})^2}{I_{\rm in,min}}. \quad (21)$$

Comparing with (17), again we see that this solution consumes more power if $\mathrm{DR} > A^2$. This case corresponds to a situation where the desired dynamic range is much more than required speedup.

In the second case, assuming $\mathrm{DR} < A/10$, we get

$$I_{\rm ref} \ge AI_{\rm in,min} = \frac{U_T^2C_LC_{\rm IN}(\mathrm{BW})^2}{I_{\rm in,min}}. \quad (22)$$

Thus, in this case, comparing with (17), output impedance adaptation consumes lesser power than $I_{\rm ref}$ adaptation by a factor of $\approx \sqrt{\mathrm{DR}}$. From (21) and (20), for a floating-gate programming system that requires measurements spanning a very wide range of currents ($\mathrm{DR} \approx 10^6$) and a modest speedup ($\mathrm{A} \approx 100$), adapting the amplifier's bias current is the better solution compared to adapting the output impedance.

V. Noise Performance of the Adaptive Logarithmic TIA

In this section, the noise performance of the circuit in Fig. 5(a) referred to as configuration I is discussed in detail. Configuration II can be analyzed following the analysis presented.

For the noise analysis, we consider channel noise current sources for each transistor separately and compute their contribution to voltage noise power, $\hat{V}_{\rm out}^2$ at the output. The total noise

power is found by adding the noise power due to these uncorrelated sources. The calculation can be simplified by noting that noise currents due to transistors M_7–M_{11} appear as a common-mode signal to the differential amplifier and are thus attenuated by the CMRR. Also, M_5 and M_6 are in saturation with equal values of G_m denoted by G_{m5} in the following analysis. Then, we have

$$\hat{V}_{\rm out}^2 \approx \frac{(\tilde{i}_5^2+\tilde{i}_6^2)}{G_{\rm m5}^2} + \frac{(\tilde{i}_1^2+\tilde{i}_2^2+\tilde{i}_3^2+\tilde{i}_4^2)}{G_{\rm m1}^2} \tag{23}$$

where $\tilde{i}_k^2$ denotes the channel current noise power of transistor M_k. The output noise can also be referred back to the input as a current noise whose value is given by

$$\hat{i}_{\rm in}^2 \approx \left(\frac{\kappa}{\kappa+1}\right)^2 (\tilde{i}_5^2+\tilde{i}_6^2) + \left(\frac{\kappa}{\kappa+1}\frac{G_{\rm m5}}{G_{\rm m1}}\right)^2 \left(\sum_{k=1}^{4}\tilde{i}_k^2\right). \tag{24}$$

From (24), it is evident that as the adaptation makes $G_{\rm m1} \gg G_{\rm m5}$ the noise due to the amplifier becomes negligible. The noise at the output is going to have a thermal noise component and a component due to $1/f$ noise. This expression needs to be integrated over the bandwidth of the TIA to get the total integrated output noise. For the analytic derivation, we only consider the thermal noise component of a transistor modeled following [17] as

$$\frac{\tilde{i}^2}{\Delta f} = 2qI \tag{25}$$

where q is the electronic charge and I is the current flowing through the transistor. Using the transfer function from $I_{\rm in}$ to $V_{\rm out}$ calculated earlier, we get the total noise to be

$$\hat{V}_{\rm out,total}^2 = \frac{4qI}{G_{\rm m5}^2}\int \frac{df}{1+\frac{\omega^2}{p_1^2}} = \frac{kT}{(\kappa+1)C_{\rm eff}}. \tag{26}$$

Thus, the total integrated noise is independent of I, a result that is expected because the bandwidth increases with I while the voltage noise density at the output decreases with I. An intuitive explanation of this phenomenon based on equipartition of energy is found in [8].

The output voltage noise spectrum till 100 kHz was measured for configuration I using a spectrum analyzer (Stanford research System's SR 780) for different input currents. The result is plotted in Fig. 10. The bandwidth obtained from the noise plots corroborate the value of $C_{\rm eff} \approx 20$ fF which is close to the value calculated based on process parameter values in the AMI 0.5-μm process and also from measured step responses. From the figure, integrating the noise spectrum gives a total noise of 700 μV rms. The theoretical equation for thermal noise predicts a value of 396 μV rms with the difference probably being due to $1/f$ noise and measurement noise. The theoretically calculated thermal noise density for $I_{\rm in} = 65$ pA is 3.7 $\mu {\rm V}_{\rm rms}$ which matches closely with the measured noise density of 4.7 μV rms as shown in Fig. 10. Also, the fact that the adaptation circuitry does not indeed add more noise was verified by comparing the noise spectra of a circuit in Configuration I with a similar circuit but with no adaptation circuit. Both the circuits were biased at an input current $\approx$ 1 nA. The results are plotted in Fig. 11.

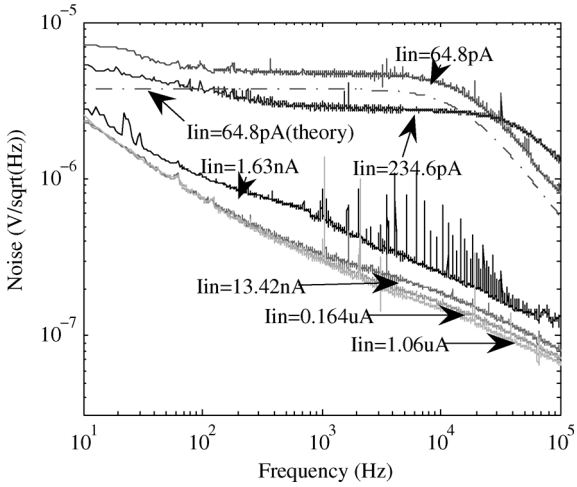

Fig. 10. Noise performance. Measured output voltage noise spectrum for Configuration I. The thermal noise floor reduces and the corner frequency increases with increasing input current. At higher currents the $1/f$ noise dominates in a 5-kHz band.

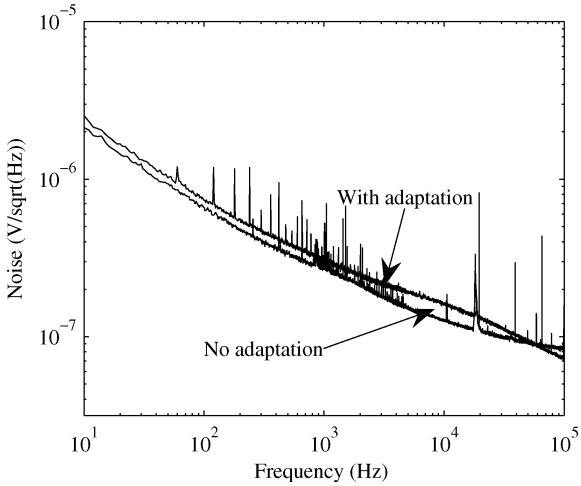

Fig. 11. Adaptation noise. Comparison of measured noise performance of a circuit with and without adaptation. The adaptation introduces minimal noise.

The SNR can now be computed using the transfer function as follows:

$$\mathrm{SNR}_{\rm power} = \frac{(\kappa+1)^3}{\kappa^4}\frac{C_{\rm eff}U_T}{q}. \tag{27}$$

Using the earlier obtained value of $C_{\rm eff}$ and choosing $\kappa = 1$, we get an approximate value of SNR as 45 dB. But it should be noted that in applications like floating-gate programming or imaging, the scaling of bandwidth with input current is not required. Rather, this system demands a constant bandwidth of a few kilohertz depending on a fixed sample rate of the system clock. Thus, using a filter after the TIA to limit the bandwidth to say 5 kHz, we get the SNR to scale with $I_{\rm in}$. The SNR in the case where the bandwidth is limited to "$f_{\rm BW}$" is given by

$$\mathrm{SNR}_{\rm power} \approx \left(\frac{\kappa+1}{\kappa}\right)^2 \frac{I_{\rm in}}{qf_{\rm BW}}. \tag{28}$$

This equation ignores the noise introduced by the filter itself.

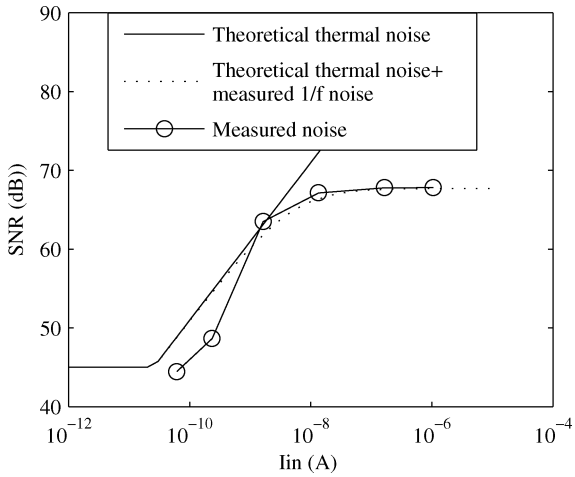

Fig. 12. SNR: Scaling of SNR with input current for a fixed bandwidth of 5 kHz. The plot based on theoretical thermal noise and measured $1/f$ noise is close to the measured curve.

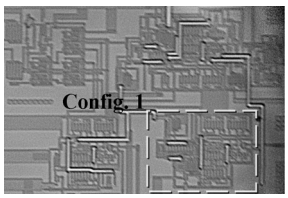

Fig. 13. Die micrograph. Die photo of the fabricated chip in 0.5-μm AMI CMOS process. Configuration I occupies 91×75 μm^2 of area.

Fig. 12 depicts the theoretically predicted and the measured variation of SNR. Thus, over the plotted range of input currents the average SNR is approximately 65 dB. The theoretical curve flattens out at low currents when the bandwidth of the TIA is lower than 5 kHz. It should be noted that the increase in SNR with increasing current saturates for the measured case because the contribution of $1/f$ noise starts dominating in the 5-kHz band. A curve plotted with theoretical thermal noise and measured $1/f$ noise corresponds very closely to actual data proving the claim. Fig. 13 shows the micrograph of the fabricated chip.

VI. Conclusion

Traditionally, different architectures for TIAs including common source, common gate, and common drain have been explored. In all these systems, there is an inherent tradeoff between input-current noise and bandwidth due to the fixed feedback impedance [18]. For this reason, applications requiring very wide dynamic range and low noise need some form of gain adaptation. Techniques that extend the dynamic range right at the preamplifier include varying the preamplifier gain [3], [6], [19], placing a variable signal attenuator before the preamplifier [4], [20] or using two feedback paths with different gains [5]. The first two techniques use neither continuous nor automatic adaptation, but instead have a gain control input which is set by the user. The third technique has the disadvantage of having two outputs which need to be combined using additional circuitry. Table II compares this work with some of the references.

In this paper, we analyze in detail the power dissipation for the two main logarithmic TIA topologies and show their functional dependence on speedup ($\mathrm{BW}U_T C_{\mathrm{IN}}/I_{\mathrm{in,min}}$), dynamic range ($I_{\mathrm{in,max}}/I_{\mathrm{in,min}}$) and input, output capacitances. We present two adaptation methods to overcome this problem. The first technique adapts the amplifier's bias current depending on input current to maintain bandwidth and stability. The second method reduces the gain of the amplifier at higher currents when the required speedup is less. It is shown that configuration I is ideal for wide dynamic ranges. For this configuration, bandwidth or SNR can be made to scale with input currents. It is also shown that adaptation does not adversely affect bandwidth or noise performance. Measured results show operation over 7 decades of current with an average power consumption of 3.45 μW. The average SNR for operation at 5 kHz is 65 dB. The adaptation schemes introduced are very general and can be applied to a wide class of circuits.

TABLE II
Comparison of Performance

Reference	[13]	[6]	[5]	This Work
Process	1.6μm	1.5μm	Discrete	0.5μm
Area	-	$2.9\times3.7mm^2$	-	$91 \times 75\mu m^2$
Supply	-	$\pm$6V	-	3.3 V
DR	100dB	114dB	80dB	140dB
Bandwidth	>10Hz	1kHz	25kHz	>3.5kHz
Power	10pA-1μA[1]	30mW	-	.1μW - 33μW

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