3.3.2. Designing Flyback Transformer by the Help of AN4137 Application Note

After I learned required electronical components for designing flyback transformer, I was asked to design an offline continuous mode flyback converter. The supervisor engineer gave me AN4137 Application Note which is a guide for designing a flyback transformer. However, AN4137 explains how to design a flyback converter by using Fairchild Power Switch, not UC3845. Therefore, I used another application note which is AN1327/D. Even though AN1327/D Application Note uses UC3845 IC, it guides for discontinuous mode flyback transformer which is not the case I was asked. So, I synthesized both application notes and did some extra internet research.

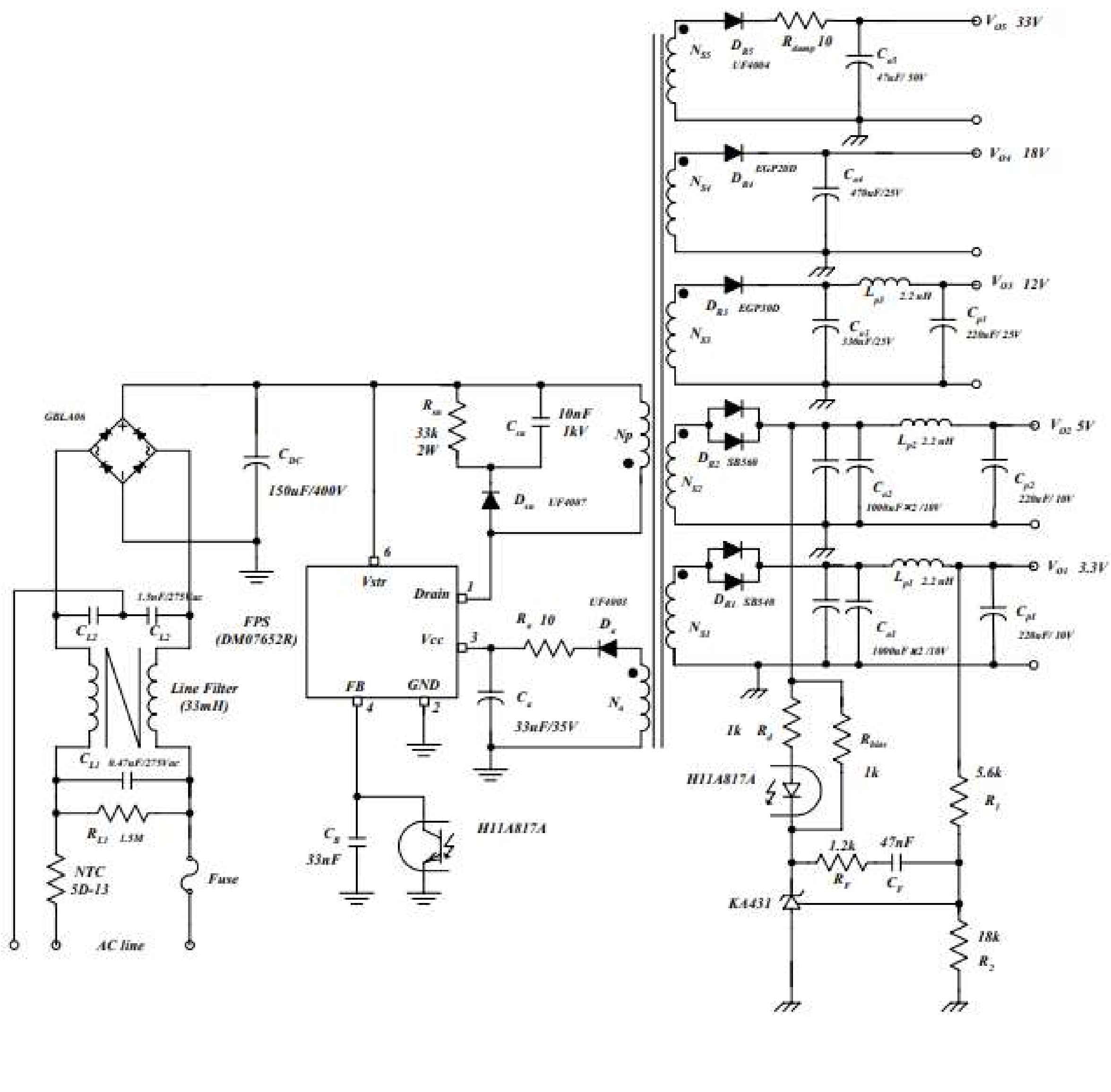

Figure 37: Schematic of Flyback Transformer Designed in AN4137 Application Note

3.3.2.1 Specifications

First step of designing a flyback converter is determining the specifications. The specifications for my flyback transformer design are below.

- Line voltage range is between 85-265V AC (V_{line}^{min} = 85V AC V_{line}^{max} = 265V AC)
- Line Frequency f_L is 50Hz
- 4 Outputs 24V 0.5A, 18V 0.5A, 15V 1A and 12V 1A respectively
- Load Occupancy Factor for Output 1 $K_{L(1)}$ = 0.25, Output 2 $K_{L(2)}$ = 0.1875, Output 3 $K_{L(3)}$ = 0.3125 and Output 4 $K_{L(4)}$ = 0.25
- Max Output Power is 48W
- Estimated Efficiency is 0.7 (Input power P_{in} is 68W)
- Switching frequency of MOSFET, f_s = 67 kHz

3.3.2.2 Calculating DC Link Voltage Range and Choosing the DC Link Capacitor

After determining the specifications, DC link capacitance should be determined. DC link Capacitor should be chosen 2-3 µF per watt for Universal Input Range (85-265V AC). 150 µF capacitor is chosen.

The next step is calculating the DC link voltage range. According to AN4137 application note following formulas should be used. D_{ch} is line capacitor charging duty ratio which is usually 0.2. Therefore, D_{ch} is taken as 0.2.

$$V_{DC}^{min} = \sqrt{2 \cdot (V_{line}^{min})^2 - \frac{P_{in} \cdot (1 - D_{ch})}{C_{DC} \cdot f_L}}$$

(Formula 4)

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max}$$

(Formula 5)

According to Formula 4 and 5, V_{DC}^{min} = 85V and V_{DC}^{max} = 375V are calculated. DC link capacitor should be resisted V_{DC}^{max} = 375V, therefore final decision for DC link capacitor is 150 µF 450V.

3.3.2.3 Determining the Maximum Duty Ratio and Calculating Reflected Voltage and Maximum Nominal MOSFET Voltage

In order to design continuous mode flyback converter, maximum duty cycle must be less than 0.5. Moreover, recommended maximum duty ratio is between 0.45 and 0.5 for universal input range. Therefore 0.48 is chosen as maximum duty ratio D_{max}.

After determining the D_{max}, reflected voltage from transformer V_{RO} and maximum nominal MOSFET voltage V_{ds}^{nom} are calculated according to following formulas given in AN4137 Application Note.

$$V_{RO} = \frac{D_{max}}{1 - D_{max}} \cdot V_{DC}^{min}$$

(Formula 6)

$$V_{ds}^{nom} = V_{DC}^{max} + V_{RO}$$

(Formula 7)

By using Formula 6 and 7, V_{RO} = 80V and V_{ds}^{nom} = 485V are calculated. According to AN4137 application note, V_{ds}^{nom} should be less than 70% of drain source voltage of chosen MOSFET. Therefore, the chosen MOSFET's DS voltage should be larger than 650V.

3.3.2.4 Calculating the Transformer Inductances and Choosing Proper Core

According to the AN4137 application note, transformer primary side inductance can be calculated by following formula

$L_m = (V_{DC}^{min} \times D_{max})^2 / (2 \times P_{in} \times f_s \times K_{RF})$ **(Formula 8)**

K_{RF} at above formula is ripple factor of in full load minimum input condition. For continuous mode flyback operation ripple factor should be less than 1. Moreover, for universal input range 85-265V AC, optimum ripple factor should be between 0.25 and 0.5. Smaller value of ripple factor reduces the conduction loss of transformer. On the other hand, larger value of ripple factor reduces the size of transformer. In order to balance both situations, I choose ripple factor as 0.35. After doing calculations L_m is calculated as 500 µH.

The information given in application note says that choosing the transformer core should be done according to following table.

Output Power	EI core	EE core	EPC core	EER core
0-10W	EI12.5 EI16 EI19	EE8 EE10 EE13 EE16	EPC10 EPC13 EPC17	
10-20W	EI22	EE19	EPC19	
20-30W	EI25	EE22	EPC25	EER25.5
30-50W	EI28 EI30	EE25	EPC30	EER28
50-70W	EI35	EE30		EER28L
70-100W	EI40	EE35		EER35
100-150W	EI50	EE40		EER40 EER42
150-200W	EI60	EE50 EE60		EER49

Table 1: Core Quick Selection Table (For Universal Input Range, fs=67kHz and Single Output)

However, the laboratory where I done my works doesn't have transformer cores. Therefore, I took a present transformer from junk cards and broke it into pieces so that I get the core. Because of I take an arbitrary core I don't have datasheet of it. In order to determine it's A_L value, I done some experiments. I wind the core 5 laps with copper wire and measured the inductance by LCR meter. After, I done same thing with 10 laps and 15 laps. Results were 8 µH, 30 µH and 74 µH respectively.

By using the formula below

$A_L = L / N^2$ **(Formula 9)**

A_L is calculated nearly 320 nH per turn square. Since Primary winding of transformer must be 500 µH, primary winding must be 40 turns.

After deciding the primary turn number of the transformer, secondary and auxiliary windings of the transformer should be determined. In order determine these numbers following formulas are used.

$$n = \frac{N_P}{N_{s1}} = \frac{V_{R0}}{V_{o1} + V_{F1}}$$

(Formula 10)

V_{RO} = 80V calculated before. V_{O1} is reference output which is 24V and V_{F1} is output diode voltage of 24V output. The $V_{F()}$ value of the suitable diodes for the output in the laboratory is 1.7V. As a result, the ratio n and N_{S1} are calculated as 3.1 and 13 respectively.

$$N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1}$$

(Formula 11)

Rest of the outputs turn numbers are calculated according to above formula. Ns2 (18V Output), Ns3 (15V Output), and Ns4 (12V Output) are calculated as 11, 9 and 7 respectively. The auxiliary winding V_{cc} must be larger than 9V. Therefore, N_a is 6 turns.

After deciding the turn numbers, I winded the transformer by hand. In order to make the winding simple I use common ground for 4 secondary windings.

3.3.2.5 Choosing the Output Diodes and Output Capacitor

There are 3 things to pay attention while choosing output diodes. First, reverse recovery time should be smaller than period of the system. Second, Maximum repetitive peak reverse voltage must be large enough. Third, average forward current must be large enough. Period of our system is inverse of the switching frequency.

T= 1/f **(Formula 12)**

According to Formula 12, our system's period is 15 µs. Therefore, chosen diode's t_{rr} value must be smaller than 15 µs.

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max} \cdot (V_{o(n)} + V_{F(n)})}{V_{RO}}$$

(Formula 13)

$$I_{D(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{RO} K_{L(n)}}{(V_{o(n)} + V_{F(n)})}$$

(Formula 14)

According to Formula 13 and 14, following results are obtained.

	$V_{D(n)}$	$I_{D(n)}$
24V Output	145V	1.2A
18V Output	110V	1.1A
15V Output	95V	2.2A
12V Output	75V	2.1A
V_{cc}	65V	-

Table 2: Maximum Reverse Voltage and RMS Current Values of Output Diodes

$$V_{RRM} > 1.3 \cdot V_{D(n)}$$

(Formula 15)

$$I_F > 1.5 \cdot I_{D(n)}^{rms}$$

(Formula 16)

Therefore, final choice for output capacitor must be

	V_{RRM}	I_F	t_{rr}
24V Output V_{O1}	>188V	>1.8A	<15µs
18V Output V_{O2}	>143V	>1.65A	<15µs
15V Output V_{O3}	>123V	>3.3A	<15µs
12V Output V_{O4}	>97V	>3.15A	<15µs
V_{cc}	>85V	-	<15µs

Table 3: Limits of V_{RRM}, I_F and t_{rr} Values of Output Diodes

Output Capacitor capacitance should be large enough to minimize the output ripple and resist to output voltage. Therefore, I choose, C_{O1} and C_{O2} as 470 µF 35V; C_{O3} and C_{O4} as 1000 µF 25V. In order to decide the capacitance values, I used following formulas.

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2}$$

(Formula 17)

$$\Delta V_{o(n)} = \frac{I_{o(n)} D_{max}}{C_{o(n)} f_s} + \frac{I_{ds}^{peak} V_{RO} R_{C(n)} K_{L(n)}}{(V_{o(n)} + V_{F(n)})}$$

(Formula 18)

After deciding output capacitors, in order to minimize output ripple, I added extra LC filter to my design. While deciding LC filter inductance and capacitor values I set the corner frequency between 1/10 and 1/5 of the switching frequency in order to avoid making system unstable.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

(Formula 19)

Setting L as 10 µH and C as 22 µF satisfies the condition. f = 10000 is between 67000/10 and 67000/5.

3.3.2.6 Designing the RCD Snubber Circuit

I used predesigned RCD Snubber Circuit.

3.3.2.7 Designing the UC3845 Connections and Feedback Loop

In order to satisfy switching frequency condition according to Formula 3, RT and CT is chosen as 5.6 kΩ and 2.2 nF respectively. One pin of 470 nF ceramic capacitor is connected to reference pin (pin number 8) and other pin of the capacitor is connected to ground.

Start resistors are determined according to following formula given in AN1327 datasheet. $I_{START(MIN)}$ = 0.3 mA $V_{in(MIN)}$ = 85V. As a result, R_{ST} = 300 kΩ.

$$R_{st} = \frac{V_{in(min)}}{I_{start(min)}}$$

(Formula 20)

Resistor power also need to be considered. $V_{in(MAX)}$ was calculated before as 375V. So start up resistor must resist 0.5W.

$$P_D = \frac{(V_{in(max)})^2}{R_{st}}$$

(Formula 21)

Other pins of UC3845 are connected as specified in the datasheet.

24V output is chosen as reference output for feedback loop. Since TL 431 tries to keep the voltage 2.5V at reference pin, I done voltage division with 5 kΩ and 43 kΩ resistors. PC817 compensation connections are done according to datasheet.

3.3.3. Setting Up the Designed Flyback Circuit on Prototype Card

After I designed the flyback transformer, I was asked to set it up on a prototype card. Before starting to set up, firstly I draw the schematic of my design.

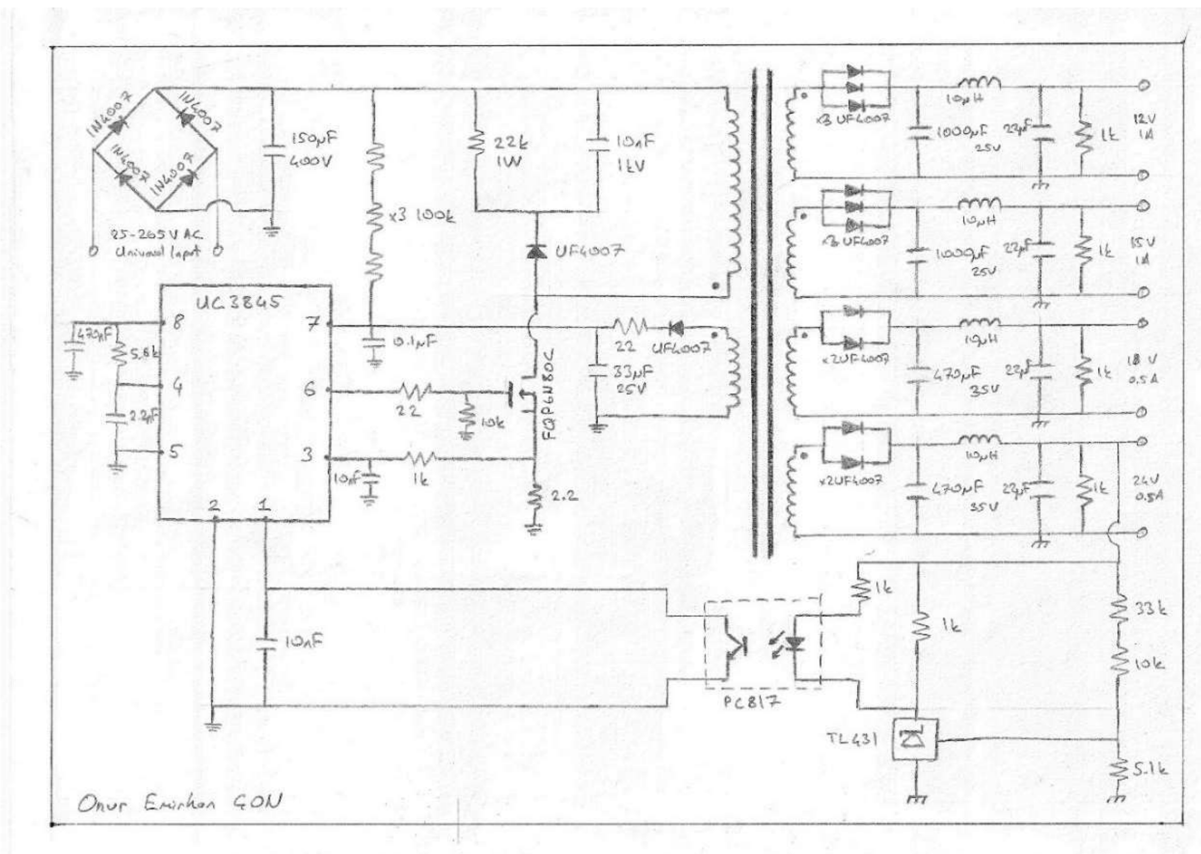

Figure 38: Schematic of Flyback Converter Design

Secondly, I winded the transformer. I explained how to decide the number of turns at PART 3.3.2.4. While winding the transformer I set three layers. First, I winded 40 turns for primary winding and I taped. Second, I winded 13 turns for secondary windings, I got outputs from 7^{th}, 9^{th}, 11^{th} and 13^{th} turns and taped. By winding like that I used common ground for outputs. Third, I winded 6 turns for auxiliary winding and tape it again. I did not set up the LC filter part because my supervisor told me it is not necessary for prototype.

After these preparations, I started to solder the components to the prototype card. After soldering process, I tested the circuit, but it failed. Because of this failure I asked my supervisor what the problem is. He said that I should set the circuit part by part and test it between every part in order to detect the problem. Therefore, I ripped of the circuit, and set it part by part.

While setting the circuit part by part, first I set the MOSFET and tested it whether I can drive it. Second, I set the secondary part of the flyback without feedback section, and I drive the MOSFET with signal generator in order to test the circuit whether I can get any output. Third, I set the UC3845 but didn't connect it to the MOSFET yet. I gave external voltage to UC3845, and I measure the output of the UC3845 to understand whether UC3845 works correctly. Fourth, I connect the UC3845 to the circuit and checked the output again. Fifth, I connected the feedback section and checked whether I get expected outputs. Sixth, I connected the RCD Snubber and start up resistors and checked again. Finally, I connected the full bridge rectifier and did the final test.

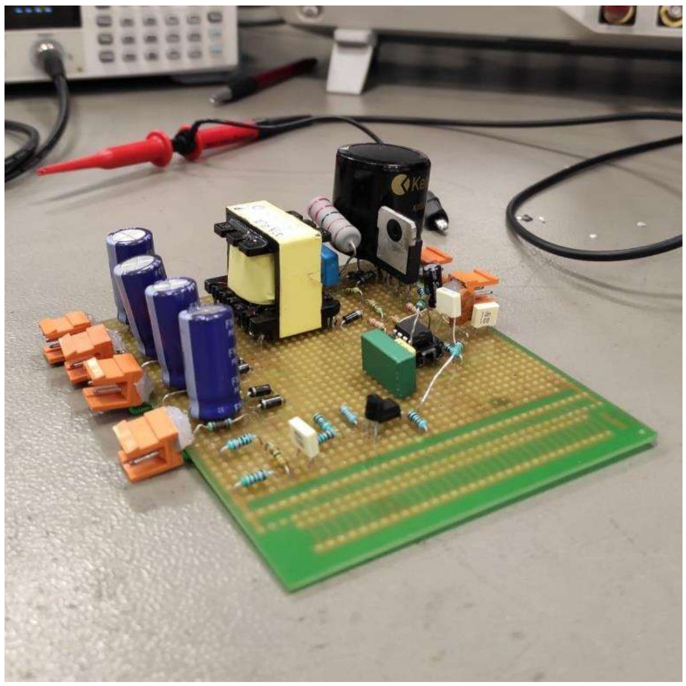

Figure 39: Final View of My Flyback Converter

3.3.4. Test Results

Because of the safety issues, I was not allowed to work with AC voltage. Moreover, I was not allowed to test my circuit with higher than 100V DC. Therefore, I connected the DC Voltage source right after the full bridge rectifier and tested my circuit.

Test results under 100V DC input are given below.

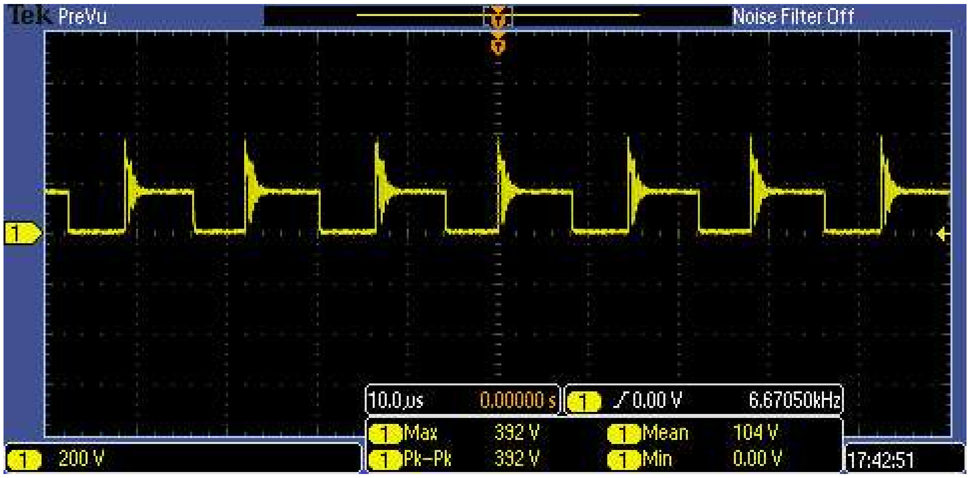

Figure 40: Drain Source Voltage of MOSFET

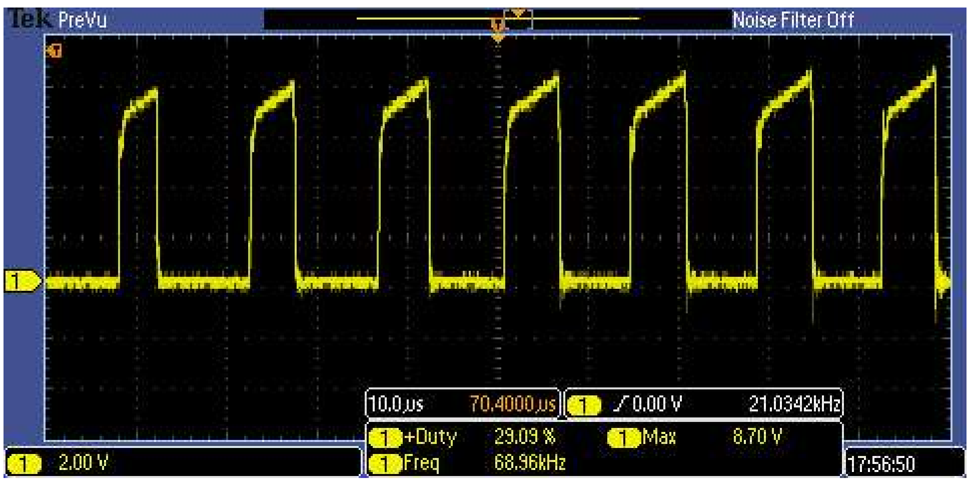

Figure 41: Gate Voltage of MOSFET

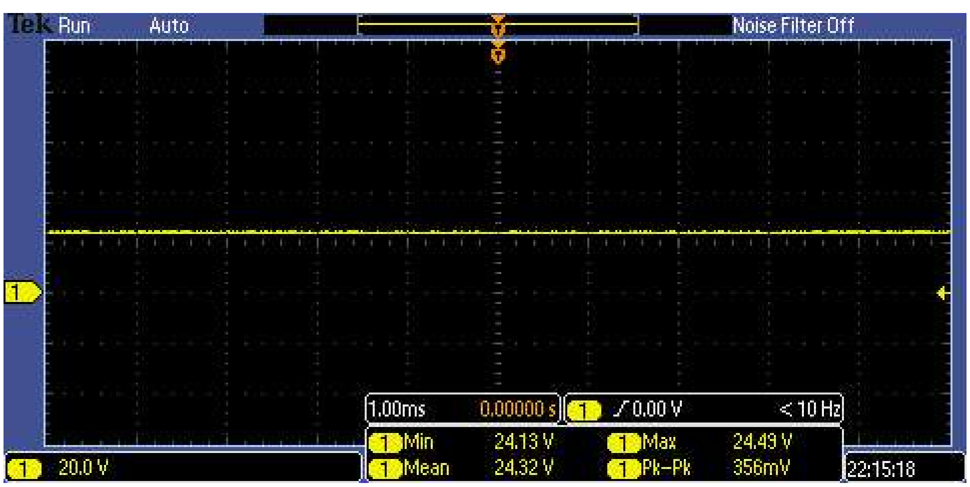

Figure 42: Measured Output Voltage of Output 1

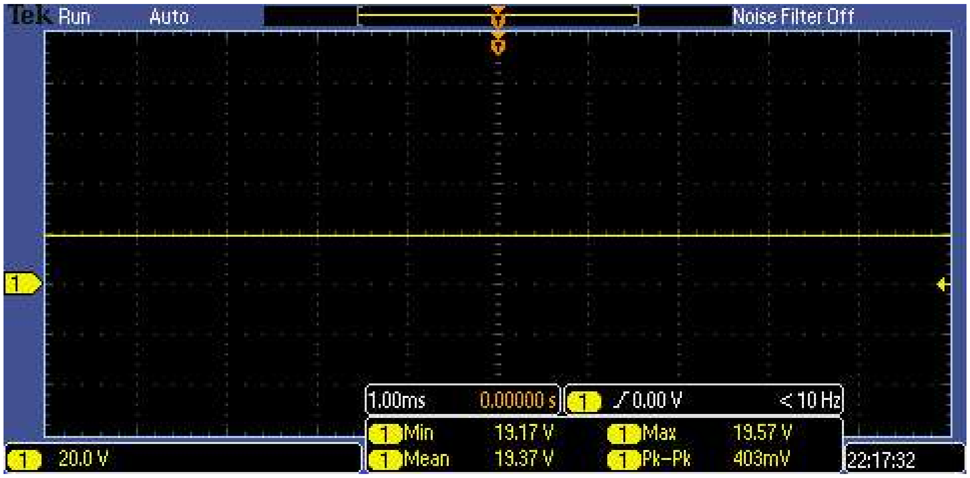

Figure 43: Measured Output Voltage of Output 2

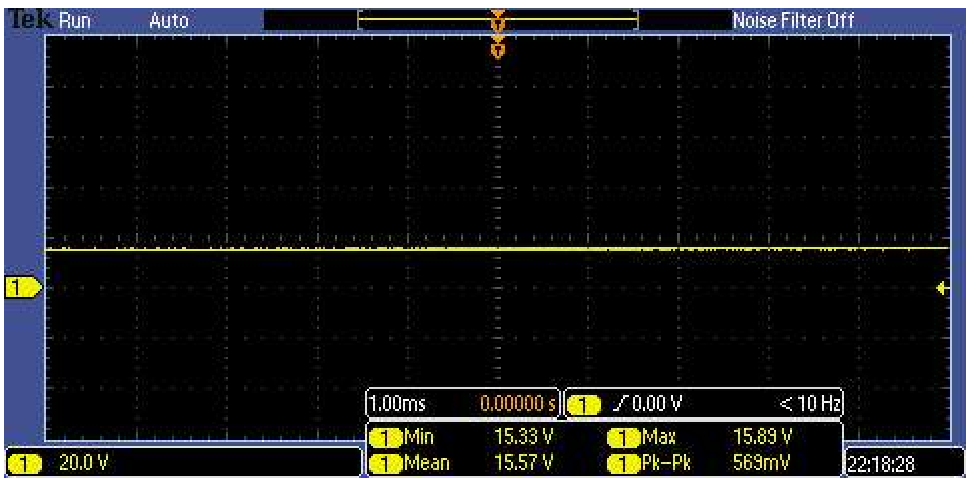

Figure 44: Measured Output Voltage of Output 3

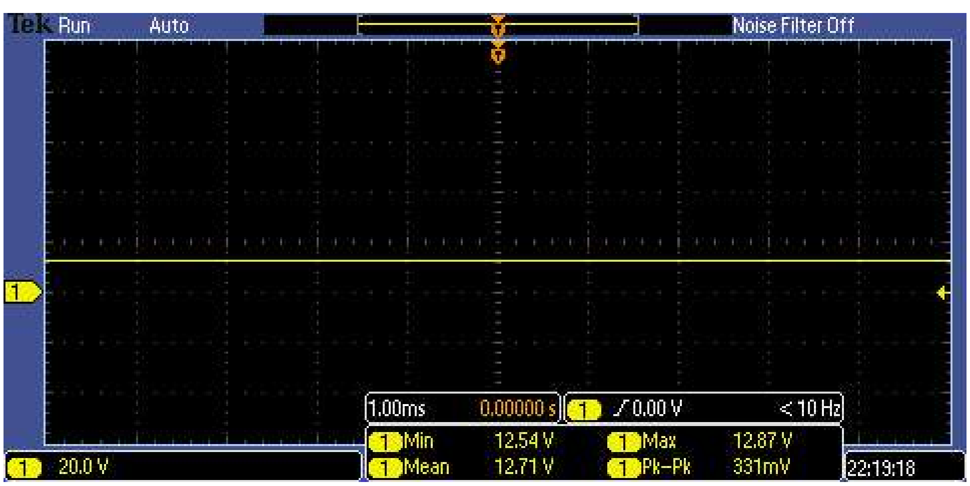

Figure 45: Measured Output Voltage of Output 4

3.3.5. Comments

In Figure 40, drain source voltage of the MOSFET is shown. As can be seen from the Figure 40, there are spikes which have maximum value 392V. My calculations says that 70 percent of the MOSFET's maximum drain to source voltage must be larger than 450V. Therefore, these spikes are not very dangerous for MOSFET. Nevertheless, better RCD Snubber Circuit design could reduce these spikes.

In Figure 41, gate voltage of the MOSFER is shown. Duty cycle is as it's supposed to be. However, shape of the waveform is not perfect rectangular. With better calculation of current limiting resistor, this waveform could look like more similar to a rectangular.

In Figure 42, 43, 44 and 45, outputs of the flyback converter are shown. The outputs are close to what I wanted but not the same. There are possible reasons for this situation. First one is uncalculated resistances of solders. Second is winding of the transformers is not perfect and turn numbers are rounded. Third one is output diodes voltage drops are not the same as the calculated ones. Moreover, there are ripples at the outputs. These ripples can be reduced by better feedback loops, better calculations of output capacitors and adding LC filter (Even though LC Filter was taken place at schematic, I did not set it up.).

I tried to measure the efficiency of the system with $(Vout^2 / R_{out})/ (V_{in}I_{in})$. V_{Out} is shown in Figure 42, 43, 44 and 45. I tested the circuit with R_{Out} = 1 kΩ and V_{in} = 100V DC. Only missing point is I_{in}. In order to measure the I_{in}, I used a pens amperemeter. However, the pens amperemeter I used was not sensitive enough to measure the input current. Therefore, I couldn't calculate the efficiency of the system.

3.4. Extras

- While doing the tasks I explained above, I also discover the research and development department. I observed the production line, organizational structure etc.
- I was given a PCB design tutorial by using Altium Software.
- I was given a MATLAB SIMULINK tutorial.
- I learnt how to use PSPICE and PROTEUS software programs in order to simulate my works.
- I learnt basic of embedded programming by using C Programming Language and STM32 Discovery Board.

4. Comment and Conclusion

I completed my internship at 20th of August 2021. I liked working at İnform Elektronik I asked to extend my internship. However, human resources told me they hire only 1 intern at the same period at the same department because of Covid 19 and if I extend my internship I overlap with the next intern. Therefore, my extension request denied.