Middle East Technical University
Department of Electrical and Electronics Engineering
EE463: Static Power Conversion I
Homework 4 Report

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Introduction

In Homework 4, we designed and analyzed the Buck Converter and the Boost Converter. We focus on theoretical understanding, simulation, and practical considerations. Key parameters of the Buck Converter, such as minimum switching frequency and output ripple, are examined. Simulation results illustrate crucial waveforms, providing insights into the converter's behavior. The Boost Converter, designed for step-up voltage regulation, is analyzed for minimum inductance and output capacitance needed for low voltage ripple. Real-world considerations, like equivalent series resistance (ESR) in the output capacitor, are introduced. Practical aspects involve selecting commercial semiconductor products and analyzing losses and thermal considerations. This study aims to bridge theoretical knowledge with practical considerations for efficient and reliable power electronics design.

Q1)

a)

$$I_{L-Average} = I_{out}$$

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{24}{5} = 4.8A$$

At the DCM – CCM Boundary

$$I_{L-Average} = \frac{I_{L-Peak}}{2}$$

$$I_{L-Peak} = \frac{1}{L}\int V_L dt = t_{on} \times \frac{V_{Diode} - V_{out}}{L} = \frac{D \times (1-D) \times V_{Diode}}{f_s \times L}$$

$$I_{L-Average} = \frac{D \times (1-D) \times V_{Diode}}{2 \times f_s \times L}$$

$$f_s = \frac{D \times (1-D) \times V_{Diode}}{2 \times I_{L-Average} \times L}$$

$$D = \frac{V_{out}}{V_{in}} = \frac{5}{20} = 0.25$$

$$f_s = \frac{0.25 \times 0.75 \times 20}{2 \times 4.8 \times 12 \times 10^{-6}} = 32552\ Hz$$

b)

Current Ripple formula

$$\Delta i_L = \frac{V_0 \times (1 - D)}{L \times f_s}$$

Voltage Ripple formula

$$\Delta V_0 = \frac{\Delta i_L \times T_s}{8C}$$

For 20V

$$\Delta \mathrm{i_L} = \frac{5 \text{ x } (1 - 0.25)}{12 \times 10^{-6} \times 300 \times 10^3} = 1.042\ A$$

$$\Delta \mathrm{V_o} = \frac{1.042 \text{ x } 3.33 \text{ x } 10^{-6}}{8 \times 20 \text{ x } 10^{-6}} = 0.022\mathrm{V}$$

For 8V

$$\Delta \mathrm{i_L} = \frac{5 \text{ x } (1 - 0.625)}{12 \times 10^{-6} \times 300 \times 10^3} = 0.521\ A$$

$$\Delta \mathrm{V_o} = \frac{0.52 \text{ x } 3.33 \text{ x } 10^{-6}}{8 \times 20 \text{ x } 10^{-6}} = 0.011\mathrm{V}$$

c)

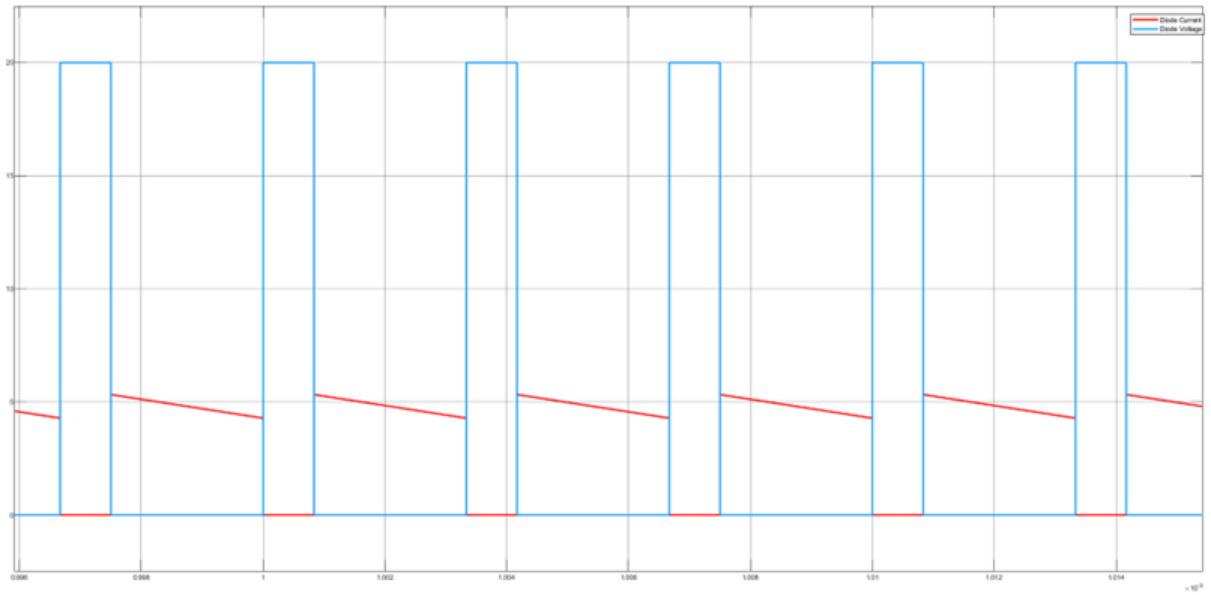

Figure 1. Diode Voltage and Current (Vin = 20V, Pout = 24W)

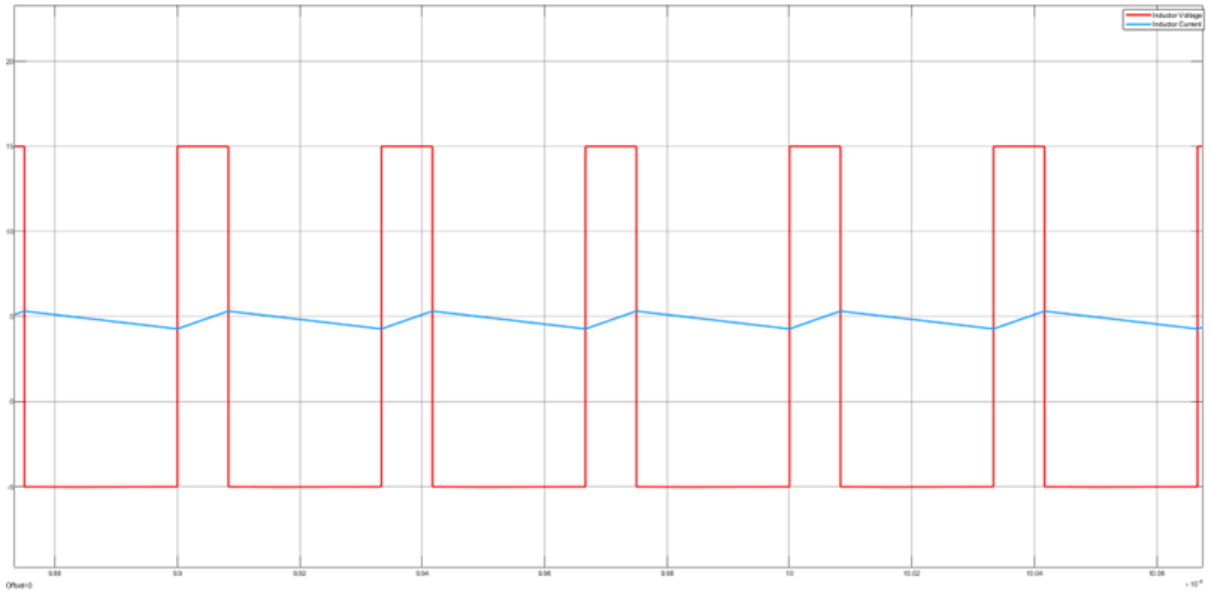

Figure 2. Inductor Voltage and Current (Vin = 20V, Pout = 24W)

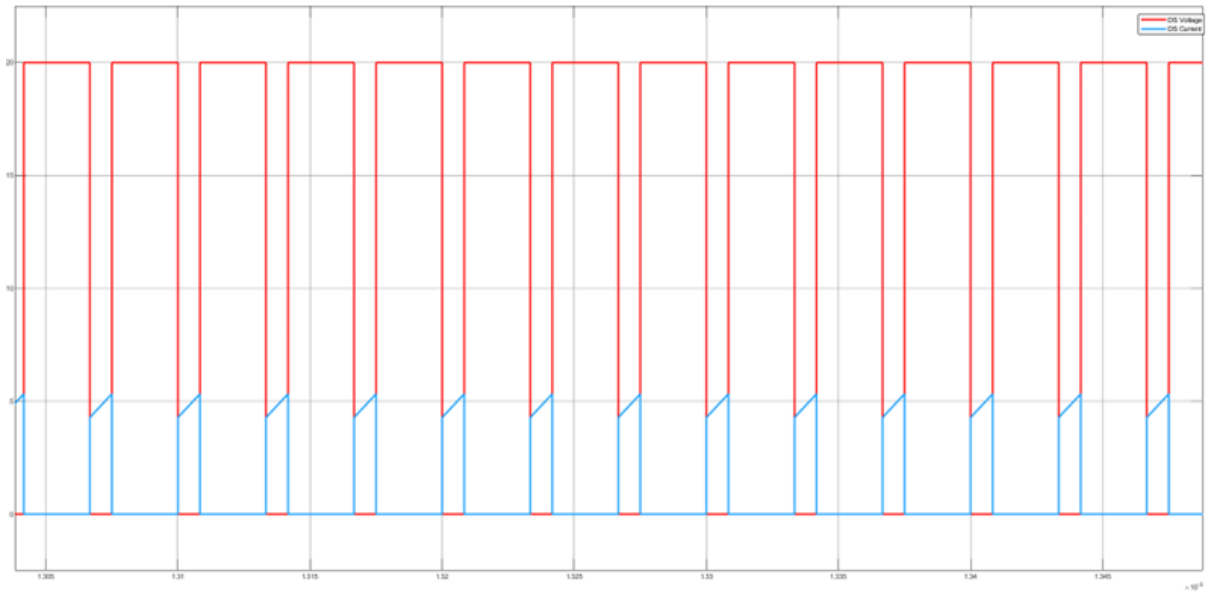

Figure 3. Switch Voltage and Current (Vin = 20V, Pout = 24W)

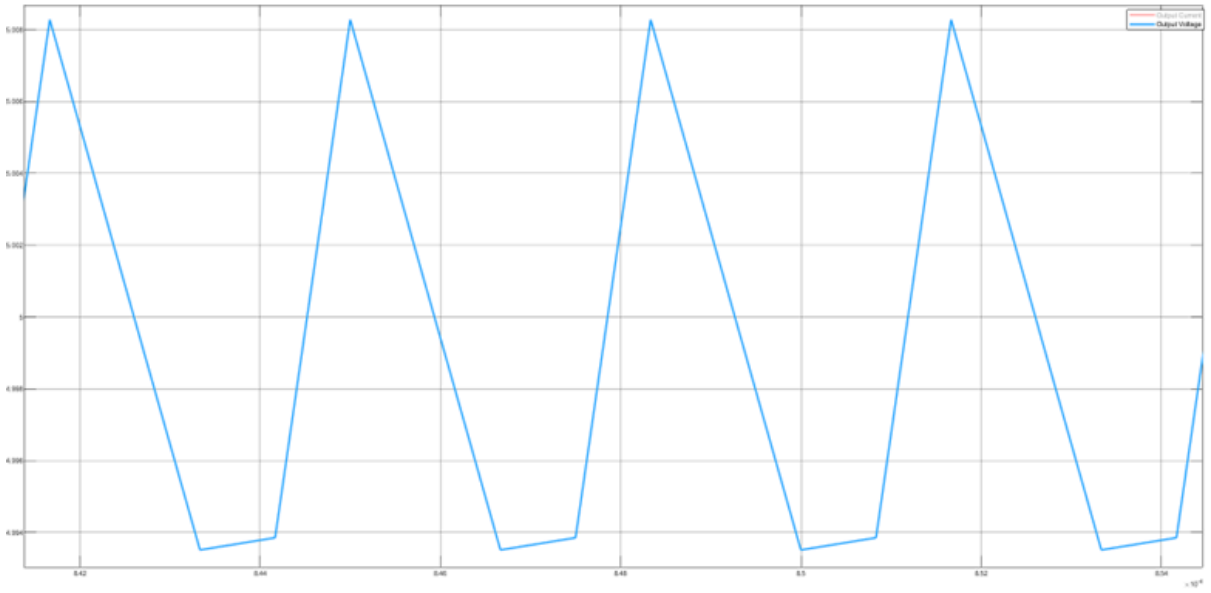

Figure 4. Output Voltage (Vin = 20V, Pout = 24W)

As can be seen from the Figure 2, inductor current never reaches the zero which means that the buck converter is operating at CCM mode. While the switch is conducting, inductor current is increasing with constant slope from 4.3A to 5.3A and inductor voltage is constant at 15V. On the other hand, while the switch is not conducting, inductor current decreases with constant slope from 5.3A to 4.3A and inductor voltage is constant at -5V. Ratio of -5/15 V is consistent with the duty cycle 0.25 as expected.

While the diode is conducting, the diode voltage is 0 and while the diode is not conducting the diode voltage is 20V which is Vin voltage which can be seen from Figure 1. Moreover, diode current is equal to inductor current when the switch is open, and it decreases from 5.3A to 4.3A as expected which means that the inductor is discharging.

In Figure 3, we can see that when the switch is open its voltage is equal to Vin voltage and it is not conducting; on the other hand, when the switch is off its voltage is 0 and its current is equal to inductor current, and it is increasing from 4.3A to 5A as expected which means that the inductor is charging.

In Figure 4, the output voltage waveform can be observed. Its max value is 5.00825V and its min value is 4.99353V.

d)

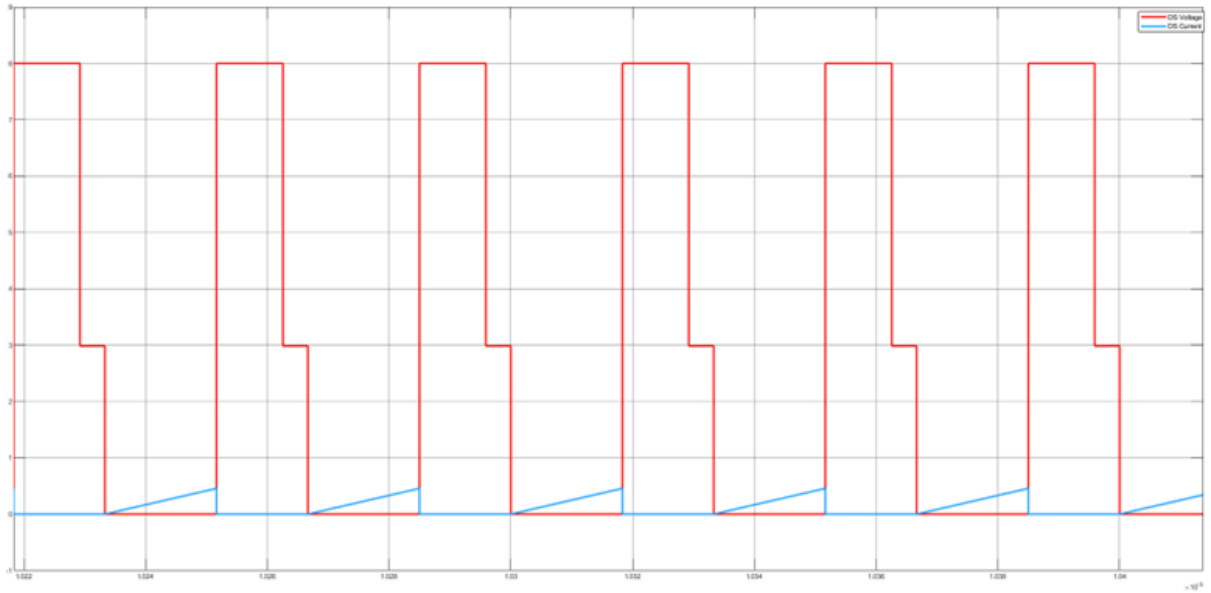

Figure 5. Switch Voltage and Current (Vin = 8V, Pout = 1W)

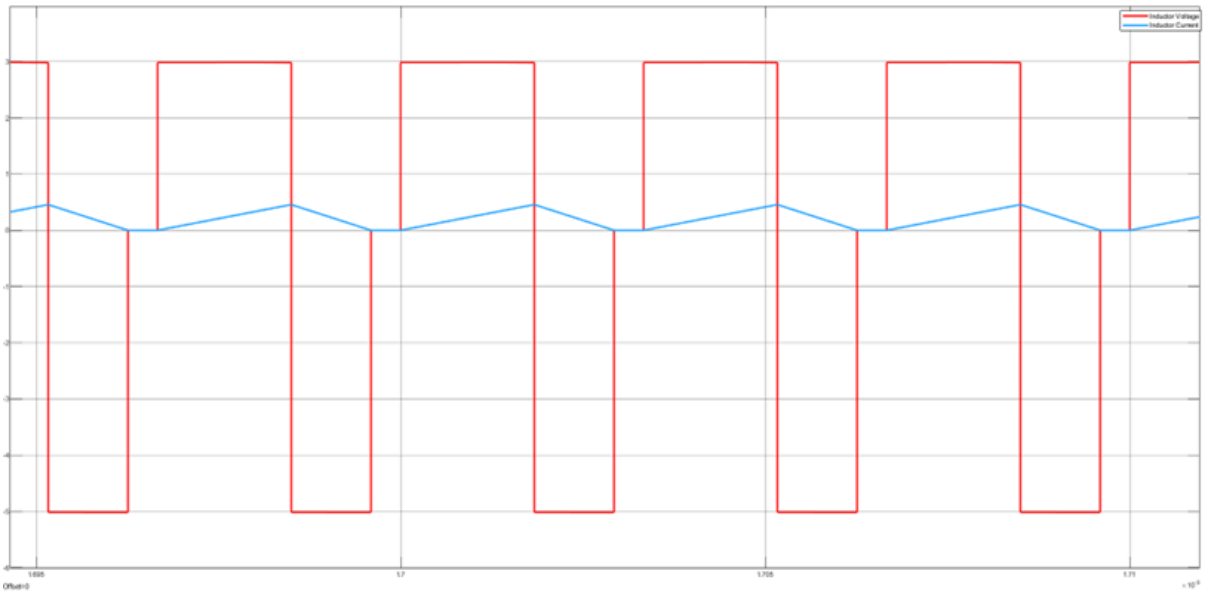

Figure 6. Inductor Voltage and Current (Vin = 8V, Pout = 1W)

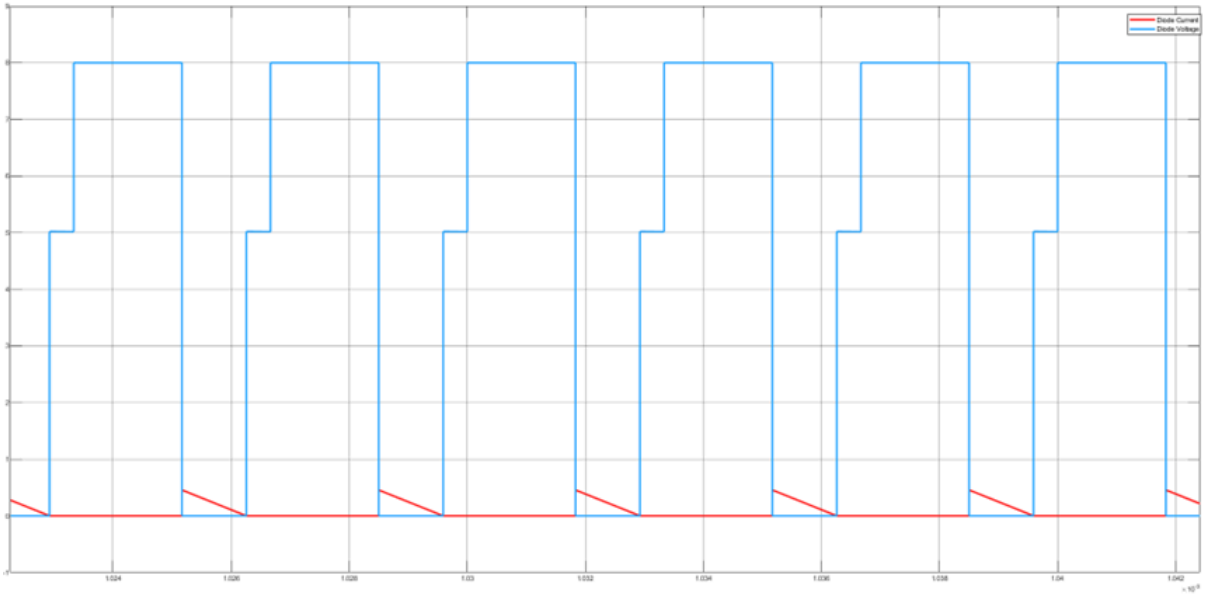

Figure 7. Diode Voltage and Current (Vin = 8V, Pout = 1W)

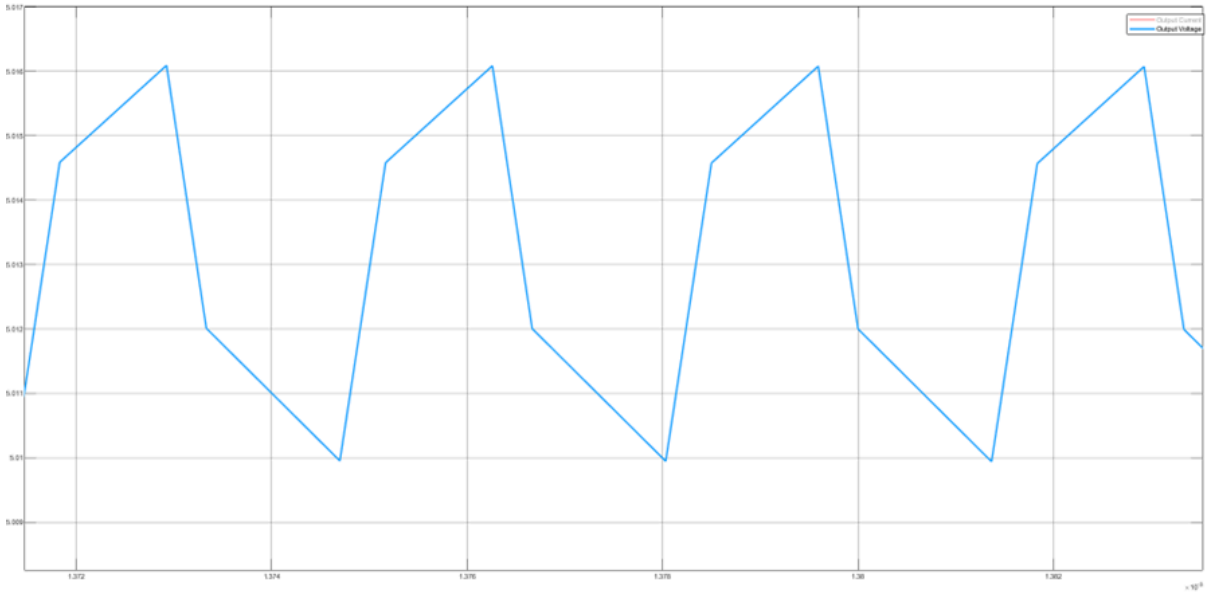

Figure 8. Output Voltage (Vin = 8V, Pout = 1W)

As can be seen from Figure 6, inductor current reaches 0 and remains constant for a while at 0A which means that the buck converter is operating at DCM mode. Since operation mode is DCM, duty cycle is not directly proportional with output voltage and duty cycle is lower than CCM calculations. While the inductor current is zero, switch and diode voltages make a step. Previous diode and switch current comments are valid for this part as well.

e)

In-Rush Current is the current drawn by capacitors until they reach steady state. When the buck converter is powered on, there is a rush current into the capacitors as they start to charge. This surge in current is known as inrush current. Inrush current can lead to voltage spikes and potential damage to components. Therefore, it needs to be reduced.

In order to reduce inrush current soft starting techniques can be used or simply enlarging the inductor of the buck converter will reduce the inrush current. In simulation, we increased the inductance of the inductor from 12 uH to 120 uH.

Initial inrush current and reduced inrush current can be seen from Figure 9 and Figure 10 respectively. As can be seen from the figures inrush current decreased from 6A to 1.8A. However, increasing the L value affects the time for it to reach the steady state negatively which can be seen from Figure 11 and Figure 12.

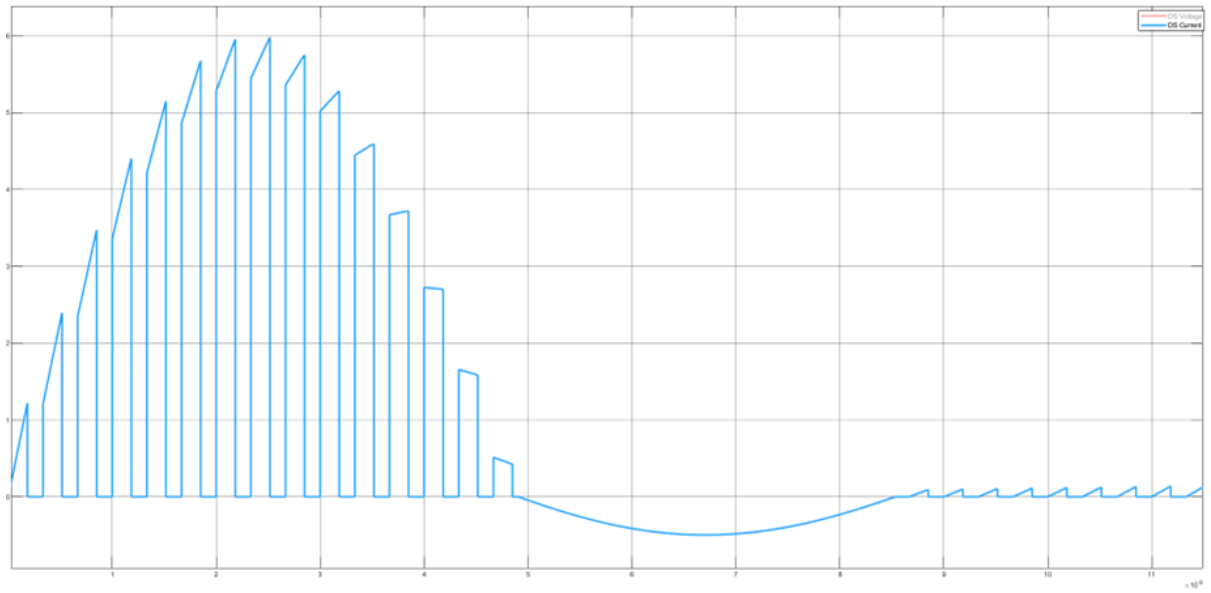

Figure 9. Inrush Current for L = 12 uH

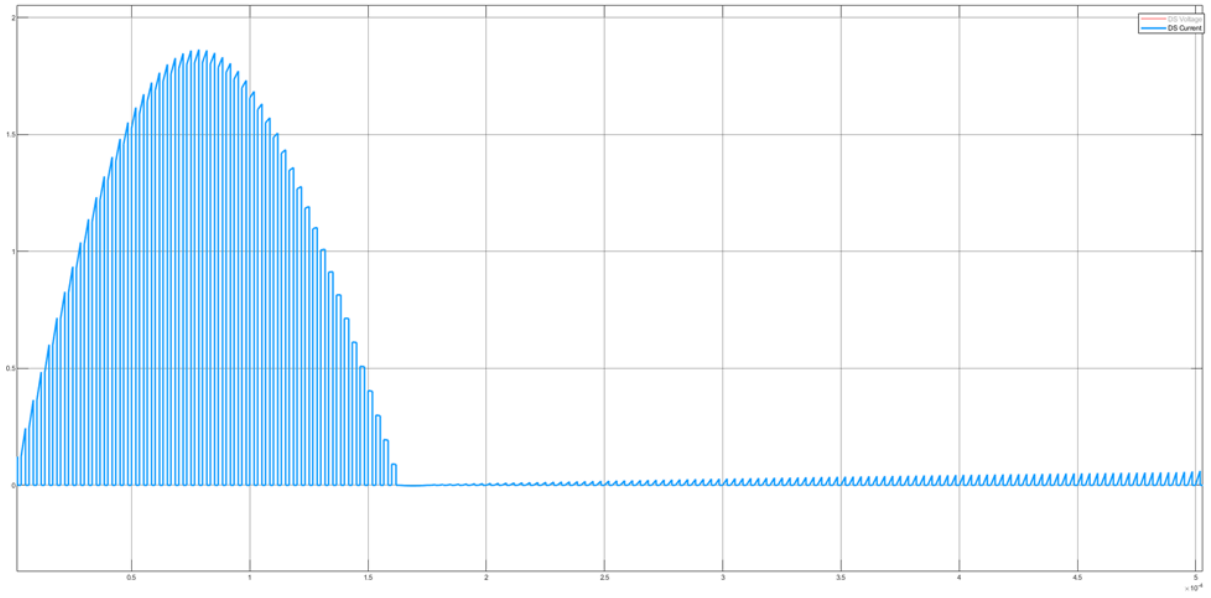

Figure 10. Inrush Current for L = 120 uH

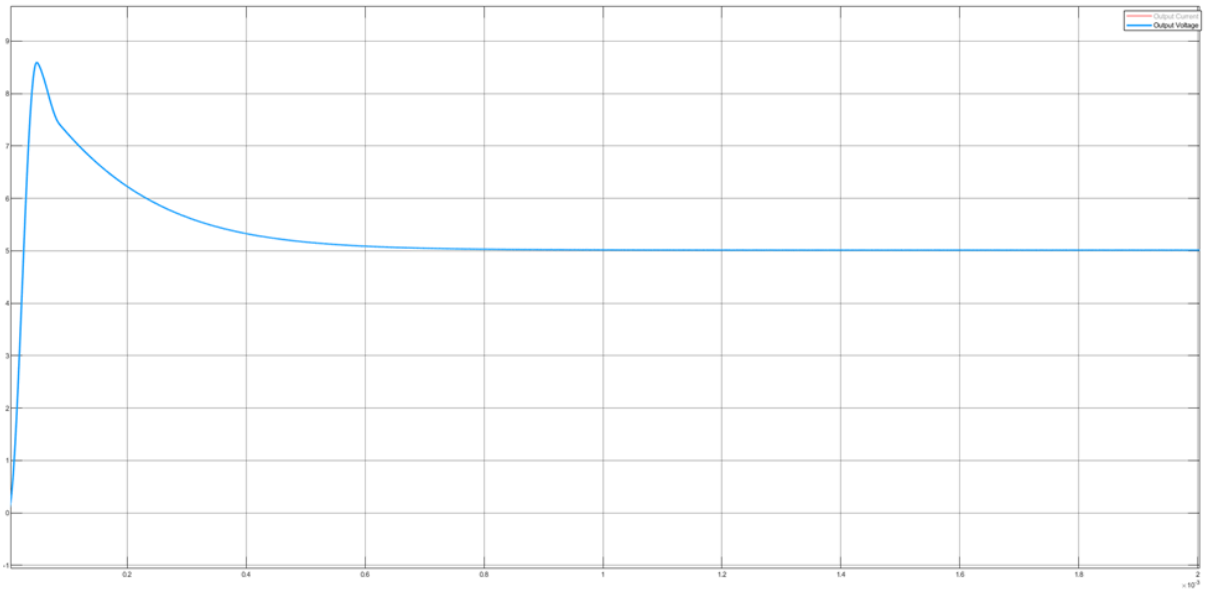

Figure 11. Output Voltage for L = 12 uH

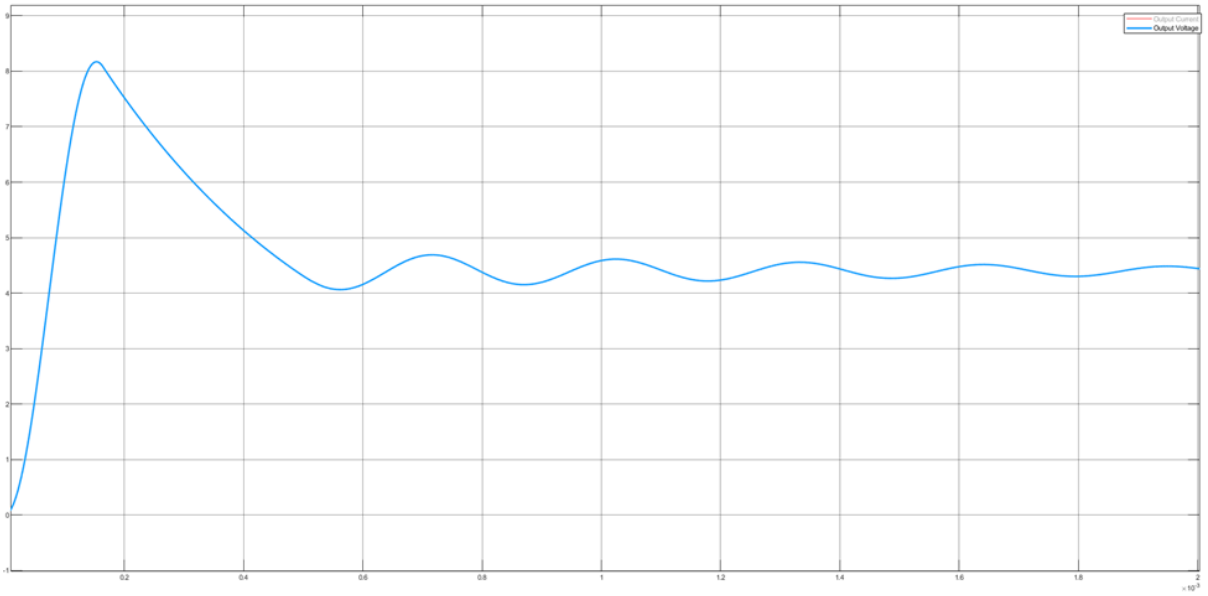

Figure 12. Output Voltage for L = 120 uH

f)

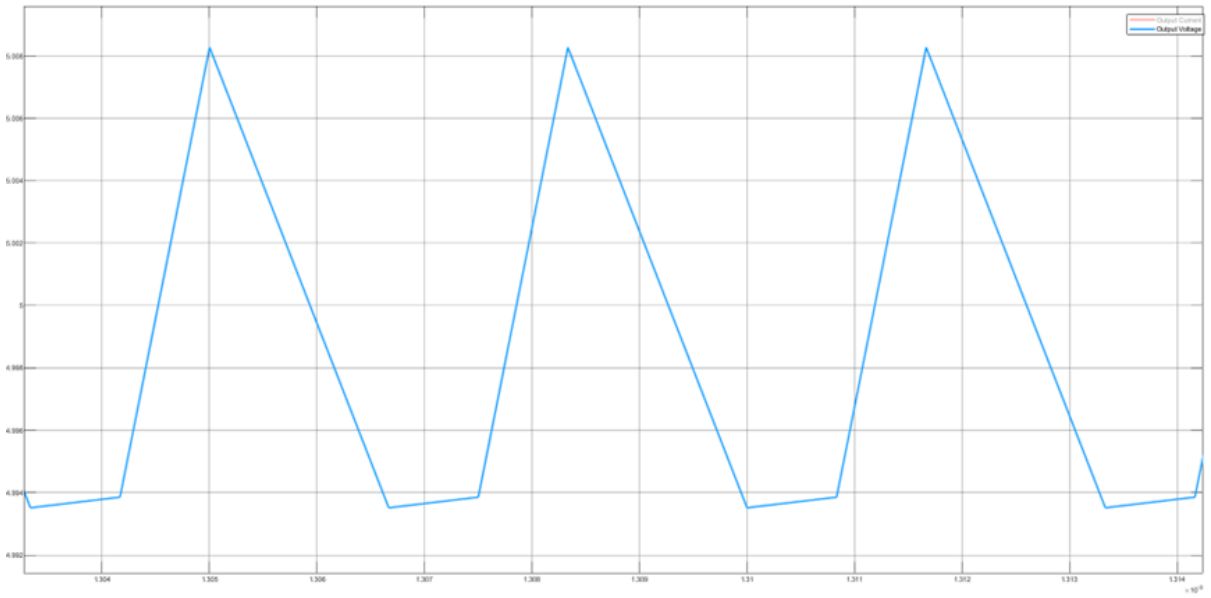

Figure 13. Output Voltage without ESR

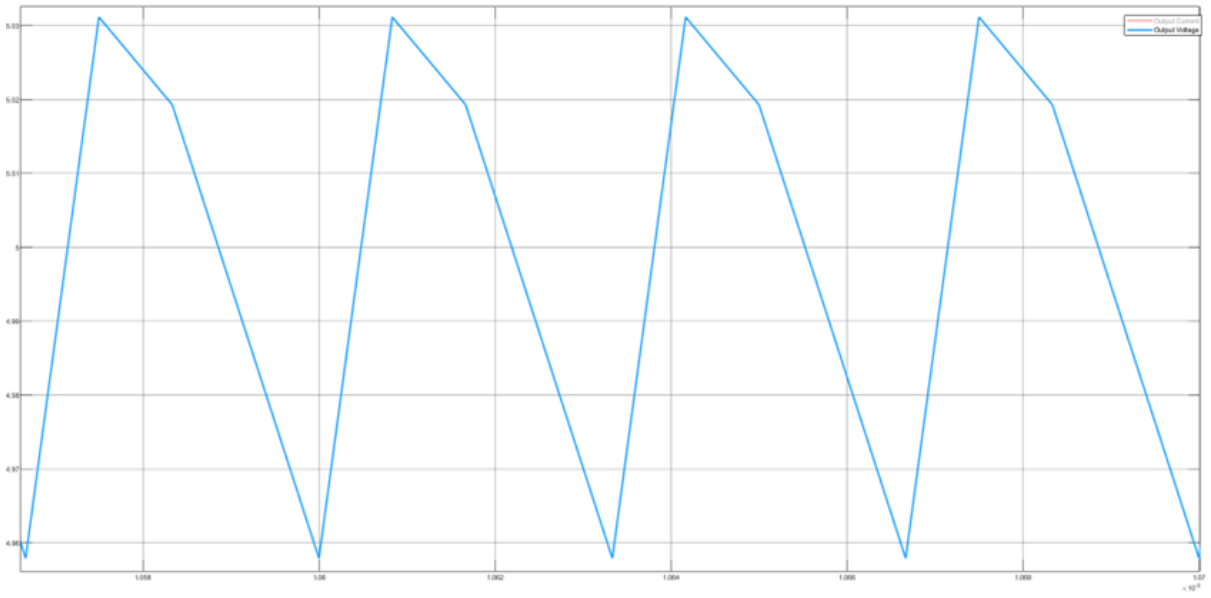

Figure 14. Output Voltage with ESR

As can be seen from Figure 13, maximum and minimum of the output voltage with no ESR are 5.008 and 4.994. On the other hand, maximum and minimum of the output voltage with ESR are 5.03 and 4.96 in Figure 14. With these data, we can say that adding ESR increases the output voltage ripple. Moreover, adding ESR means introducing a new resistance to the circuit which decreases the efficiency of the converter.

In order to decrease the effect of the ESR, instead of using one capacitor, a parallel capacitor bank can be used. In this way, ESRs are connected in parallel and total ESR is decreased. Moreover, if possible low ESR capacitors should be chosen.

2) Boost Converter

In step-up DC/DC converter, let input voltage range be 12-24 V and output voltage be 48 V with switching frequency of 400 kHz. Assume that rated output power is 96 W.

a) Consider all components as ideal. Calculate minimum inductance that will keep the converter operating in the CCM operation for rated output power.

$$V_{out,mean} = 48V$$

$$P_{out,mean} = 96W$$

$$I_{out,mean} = 2A$$

$$R_{out} = 24\Omega$$

$$T = 2.5 \cdot 10^{-6}s$$

Those values are given by the problem. We know that at the boundary of the CCM to DCM, output current $\hat{I}_{out,mean}$ is equal to

$$\hat{I}_{out,mean} = \frac{V_{out,mean}(1-D)^2 DT}{2L}$$

Where D, T and L represents duty, period and inductance respectively.

$$L = \frac{V_{out,mean}(1-D)^2 DT}{2 \cdot I_{out,mean}}$$

Note that all terms expect duty is constant. Also note that $(1-D)^2 D$ term is not easy to anticipate. The worst case scenario duty (i.e. expression must be maximum to have higher L) should be choosen. For CCM;

$$D = 1 - \frac{V_{in,mean}}{V_{out,mean}}$$

In this case, the input voltage is between 12 to 24 volts. Then for 12 and 24 Volts, maximum and minimum duties are found as 0.75 and 0.50 respectively. For this interval, $(1-D)^2 D$ takes maximum value of 0.125 with the duty of 0.5. Then L can be found as;

$$L = \frac{V_{out,mean}(1-D)^2 DT}{2 \cdot I_{out,mean}} = \frac{48 \cdot (0.125) \cdot (2.5 \cdot 10^{-6})}{2 \cdot 2}$$

$$L = 3.75\mu H$$

b) Calculate the output capacitance for peak-to-peak voltage ripple less than 3% under rated output power.

Under CCM, output voltage ripple is approximated as;

$$\frac{\Delta V_{out}}{V_{out,mean}} = \frac{DT}{RC}$$

It is evident that as the duty is increased, the ripple gets worse. Also it is discussed that the duty is between 0.5 to 0.75. Thus $D = 0.75$ *is used.*

$$C = \frac{DT}{R(\frac{\Delta V_{out}}{V_{out,mean}})}$$

$$C = \frac{(0.75)(2.5 \cdot 10^{-6})}{24(0.03)}$$

$$C = 2.6\mu F$$

c) Simulate the steady-state behaviour of the converter and show the important waveforms for boundary conduction mode of part-a. Plot following waveforms and comment on the results.

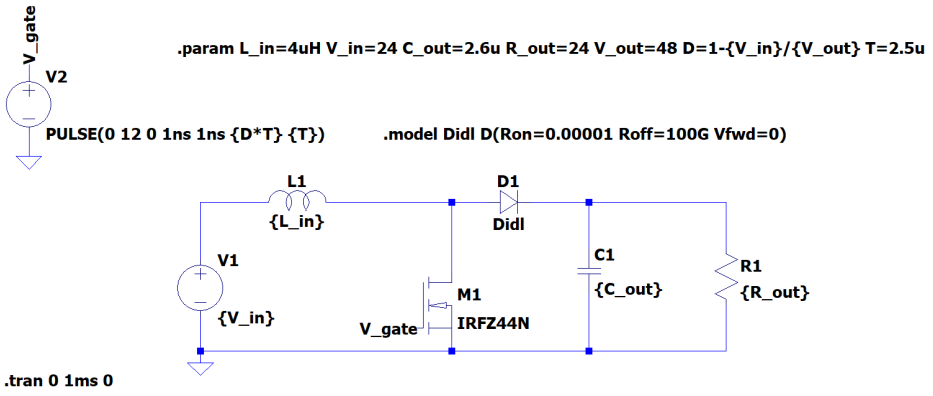

Figure 15: Simulated circuit where parameters are changed for each part

Inductor voltage and current

For $L = 4\mu H$ & $C = 2.6\mu F$, the inductor current and voltages are as shown in figures 16,17 and 18. It is obvious that as the input voltage gets closer to the output voltage (increases), the circuit gets closer to DCM of operation. The reason for that is the input current decreases due to conservation of power. As it decreases below a point, the circuit operates as DCM.

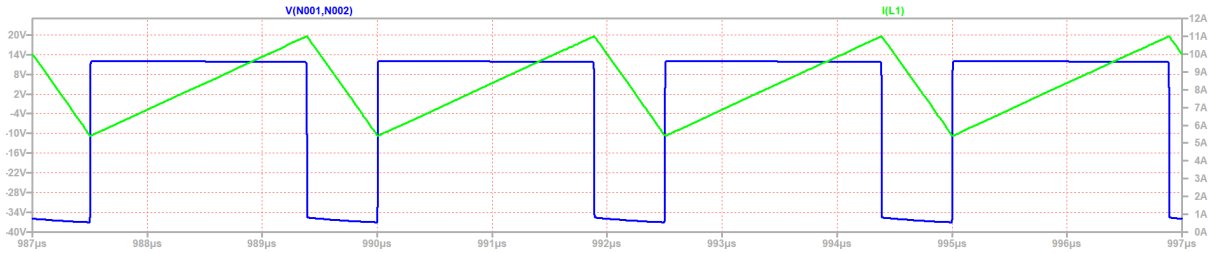

Figure 16: Plots of the inductor current and voltage when the circuit operates at the CCM with an input voltage of 12V

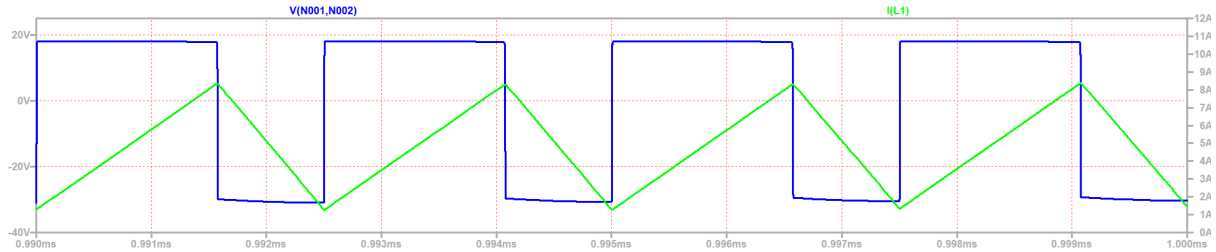

Figure 17: Plots of the inductor current and voltage when the circuit operates at the CCM with an input voltage of 18V

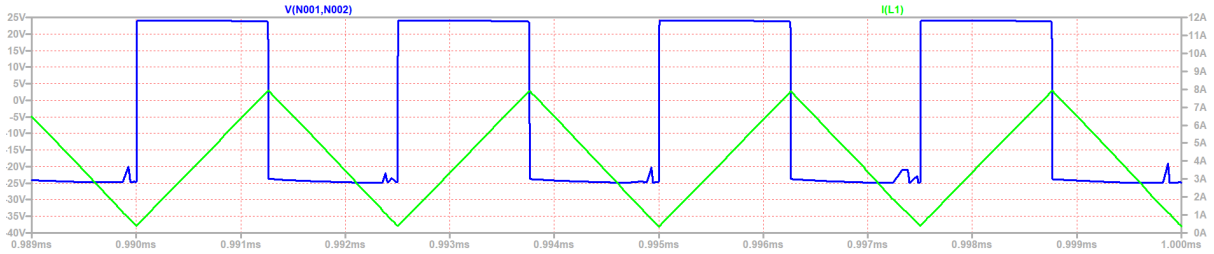

Figure 18: Plots of the inductor current and voltage when the circuit is at the edge of DCM with an input voltage of 24V

Output voltage

In this part, showing the transition from CCM to DCM for a open loop approach was important. For $L = 2.75\mu H$ & $C = 10\mu F$, the input voltage is swept from 6 volts to 30 volts with an increment of 3V. the output voltage is shown in fig. 19. One should note that as the input voltage reaches a certain value (i.e. inductor current drops to zero), if we continue to set duty using the formula derived for the CCM, the output voltage increases. If the components were ideal (i.e. no power loss expect the load) and the load power was constant, the output voltage would go to infinity gradually. Thanks to nonidealities, as the voltage is increased, the losses are also increased which balances the voltage at a certain value.

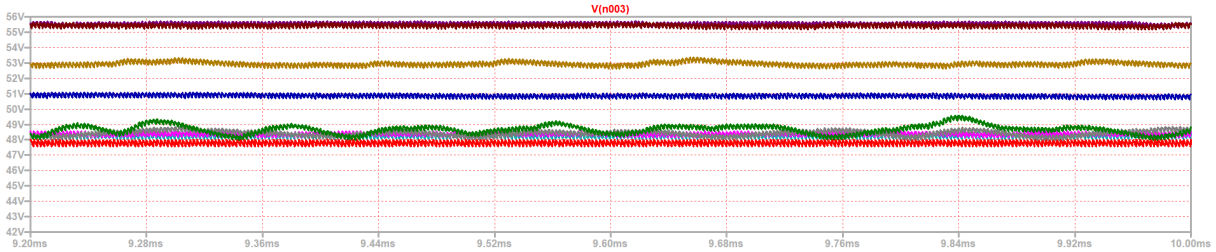

Figure 19: Plots of the output voltages for different input voltage values starting from 6 up to 30 incremented by 3 Volts.

Diode voltage and current

For $L = 10\,\mu H,\ C = 50\mu F\ and\ V_{in} = 18V$, the CCM approximations are sufficiently valid. The simulation results can be found in Fig. 20.

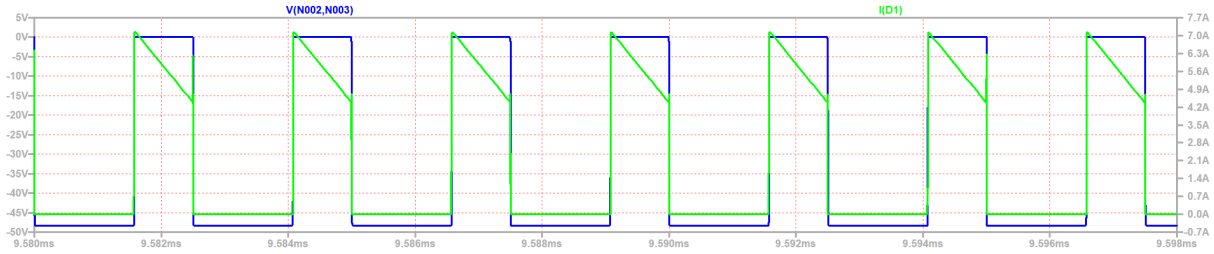

Figure 20: Plot of the diode current and voltage

Switch voltage and current

For $L = 10\,\mu H,\ C = 50\mu F\ and\ V_{in} = 18V$, the CCM approximations are sufficiently valid. The simulation results can be found in Fig. 21.

Figure 21: Switch voltage and current

d) Assuming the switches and capacitors are ideal, but the inductor has a non-zero ESR, derive the voltage gain as a function of duty cycle (d), inductor ESR (r) and load resistance (RLoad). Show your steps clearly. On the MATLAB, plot the voltage gain with and without ESR on the same graph as a function of duty cycle assuming that ESR is 100 mΩ and rated load is connected. Comment on the results.

$\bar{f}$ notation denotes the average value of $f(x)$

Note that the magnitude of the peak of the inductor current is 10Amps. For 100 mΩ ESR and applied voltage of 24V, The steady state current of the RL circuit would be 240Amps. Thus, we can assume that the inductor current increases and decreases linearly without much loss of accuracy. Other assumption is that the capacitor is large (i.e. voltage ripple is sufficiently less than the average voltage drop on the ESR.).

Step 1) *Utilizing steady state inductor mean voltage*

$$\overline{V_{L,on}} = \overline{V_{in}} - \overline{I_L} R_L$$
$$\overline{V_{L,off}} = \overline{V_{in}} - \overline{V_{out}} - \overline{I_L} R_L$$

Due to steady state assumption ;

$$(DT)\,\overline{V_{L,on}} + (1 - D)T\overline{V_{L,off}} = 0$$

Which yields

$$\overline{V_{out}} = \left(\frac{\overline{V_{in}}}{1-D}\right) - \left(\frac{\overline{I_L}R_L}{1-D}\right) \textbf{ (eq. 1)}$$

Note that for $R_L = 0$, this equation matches with the the ideal version (i.e. $Gain = \frac{1}{1-D}$).

Step 2) *Utilizing steady state capacitor mean current*

$$\overline{I_{Load}} = \frac{\overline{V_{out}}}{R_{Load}} \; ; \; \overline{I_C} = 0 \; ; \; \overline{I_D} = \left(\frac{1}{T}\right)\left[(1 - D)T\overline{I_L}\right]$$

$$\overline{I_D} = \overline{I_{Load}} + \overline{I_C}$$

Which yields

$$\overline{I_L} = \frac{\overline{V_{out}}}{R_{Load}(1-D)} \textbf{ (eq. 2)}$$

Step 3) *Find the gain by combining equation 1 and 2.*

$$G = \frac{\overline{V_{out}}}{\overline{V_{in}}} = \frac{1}{(1-D)+\frac{R_L}{(1-D)R_{Load}}} \textbf{ (eq. 3)}$$

Step 4) *Comments on the new gain.*

The effect of the ESR (Equivalent Series Resistance) on the gain depends on different parameters. When the ESR is zero, there is no loss in voltage, so the gain remains as high as the ideal case. However, if the ESR is extremely high, the output voltage drops to zero. The load resistance, which is the resistance in the circuit, also impacts this. With high load resistance, the circuit draws less current, leading to a smaller voltage drop across the ESR. Conversely, with low load resistance, more current is drawn, increasing the voltage drop and making the ESR more significant. This concepts is well observed in the eq. 3. The gain plot can be seen in fig. 22. The main takeaway is as the voltage conversion is greater, the nonidealities become more noticeable. This model is close to the real life scenarios. Thus, we can assume that it is suitable to increase about five times to its original value. As the conversion gets greater than that, the boost converter fails.

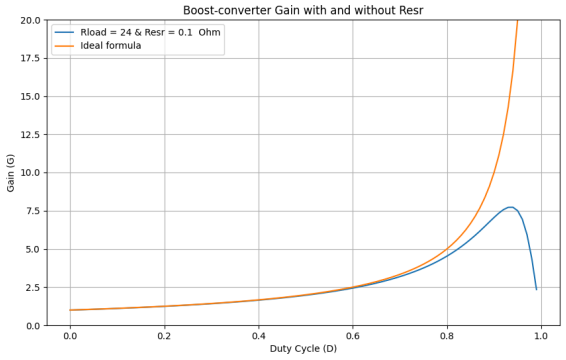

Figure 22: Boost converter gains for ESR ignored and not ignored cases

e) Repeat the same steps in part-d for the converter efficiency.

The only part in the converter that power is lost is the ESR.

$$P_{loss} = I_L(t)^2 \cdot R_{ESR}$$

At step two of part d, mean inductor current is found as;

$$\overline{I_L} = \frac{\overline{V_{out}}}{R_{Load}(1-D)}$$

And at step one of part d, mean inductor voltage when the switch is on is found as;

$$\overline{V_{L,on}} = \overline{V_{in}} - \overline{I_L} R_L$$

Then;

$$\overline{V_{L,on}} = \overline{V_{in}} - \frac{R_L \overline{V_{out}}}{R_{Load}(1-D)}$$

The current ripple of the inductor is;

$$\Delta I_L = (DT)\frac{\overline{V_{L,on}}}{L} = \left(\frac{DT}{L}\right)\left(\overline{V_{in}} - \frac{R_L \overline{V_{out}}}{R_{Load}(1-D)}\right)$$

Since we assumed that the inductor current is linearly increasing and decreasing,

$$I_{L,on}(t) = \overline{I_L} + \Delta I_L\left(\frac{t}{DT} - 0.5\right)$$

$$I_{L,on}(t) = \frac{\overline{V_{out}}}{R_{Load}(1-D)} + \left(\frac{DT}{L}\right)\left(\overline{V_{in}} - \frac{R_L \overline{V_{out}}}{R_{Load}(1-D)}\right)\left(\frac{t}{DT} - 0.5\right)$$

Then the analytical power loss is;

$$\overline{P_{loss}} = \frac{1}{DT}\int_0^{DT} I_{L,on}(t)^2 R_{ESR}\, dt$$

The efficiency is

$$\eta = \frac{\overline{P_{out}}}{\overline{P_{out}} + \overline{P_{loss}}}$$

Since the integral expression is a polynomial, it is very easy to integrate. However, for the seek of simplicity, it is calculated numerically by a python script. Then using the efficiency relation, the efficiency vs duty graph is plotted as shown in Fig. 23.

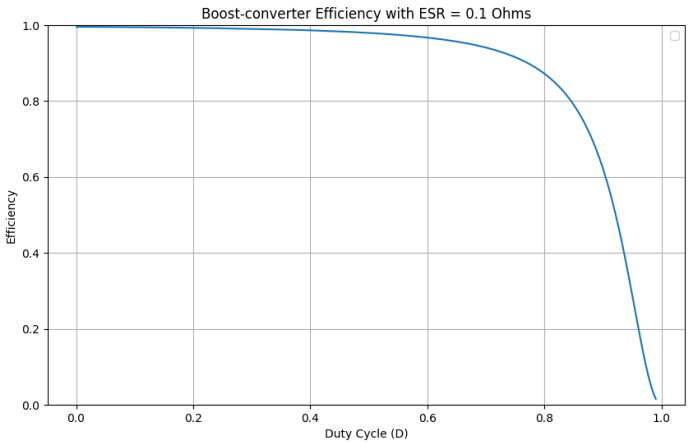

Figure 23: Boost converter efficiency for different duties when ESR is not ignored.

f) Choose commercial semiconductor products using Digikey that is appropriate for your design. Calculate the losses on these devices for rated power operation with 12 V input voltage. How would losses on the diode and switch change if the input voltage is increased? Explain in detail.

An n-type mosfet (i.e. IRFZ44N) is chosen. It's important parameters are shown in Fig. 24.

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	49	A
P_{tot}	Total power dissipation	110	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	22	mΩ

Figure 24: Important parameters of IRFZ44N

When the input voltage is 12V, the duty should be 0.75 according to Fig. 22 given in part d.

Step 1) *conduction losses*

$$\overline{I_L} = \frac{\overline{V_{out}}}{R_{Load}(1-D)} = \frac{48}{24(0.25)} = 8\,A$$

$$P_{conduction}(t) = I_L(t)^2 \cdot R_{DS(on)} \approx \overline{I_L}^2 \cdot R_{DS(on)}$$

$$\overline{P_{conduction}} \approx \overline{I_L}^2 \cdot R_{DS(on)} = 8^2(0.022) = 1.44W$$

It is always good to have a safety margin (i.e. 0.75), Thus assume;

$$\overline{P_{conduction}} = 2W$$

Step 2) *Switching losses*

$$P_{switching}(t) = V_{DS}(t) \cdot I_{L,on}(t)$$

$$\overline{P_{switching}} \approx \frac{V_{DS,peak} \cdot I_{L,peak}}{2} \cdot f_s \cdot (t_r + t_f)$$

$$\overline{P_{switching}} \approx \frac{V_{out} \cdot \overline{I_L}}{2} \cdot f_s \cdot (t_r + t_f)$$

Assume rise and fall time of 150ns;

$$\overline{P_{switching}} \approx \frac{V_{out} \cdot \overline{I_L}}{2} \cdot (t_r + t_f) \cdot f_s = \frac{48 \cdot 8}{2} \cdot (400 \cdot 10^3) \cdot (300 \cdot 10^{-9})$$

$$\overline{P_{switching}} \approx 23W$$

It is always good to have a safety margin (i.e. 0.75) , Thus assume;

$$\overline{P_{switching}} = 30W$$

Step 2) *Total loss*

$$\overline{P_{mosfet}} = \overline{P_{conduction}} + \overline{P_{switching}}$$

$$\overline{P_{mosfet}} = 32W$$

How would losses on the diode and switch change when input voltage is changed ?

If the output load is kept constant, the mean current of the diode is equal to the mean load current due to capacitor steady state balance. In such a case, assuming the forward voltage

drop is slightly changing w.r.t increase in the diode current, the loss on the diode is about the same for any input voltage.

$$P_{diode}(t) = V_f(I_D(t)) \cdot I_D(t) \approx V_f(\overline{I_D}) \cdot \overline{I_D} = Constant\ power\ loss$$

In terms of mosfet, as the duty cycle is increased, $\overline{I_L}$ increases. The relation is shown in Fig. 25.

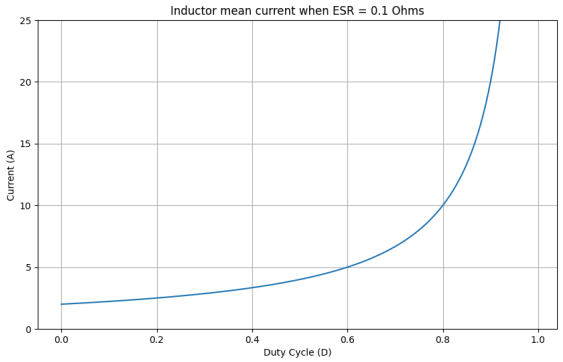

Figure 25: Inductor mean current versus duty cycle when ESR is not ignored

As discussed, the duty above 0.75 is not realistic due to ESR. Thus we can consider up to D=0.75. One should note that conduction loss is proportional to I^2 whereas switching loss is proportional to I. Thus, as input voltage is decreased (duty is increased) , the effect of conduction loss becomes more noticeable compared to switching losses. In both cases, the switching losses are dominant and conduction losses may be ignored.

g) Using the calculated loss values, construct a thermal lumped element model and estimate the junction temperature without a heatsink. If necessary, choose a thermal interface material and heatsink and find out the junction temperature with these materials. Clearly state any assumption that you made.

The thermal model is given in Fig. 26. The calculations are not completed for this part.

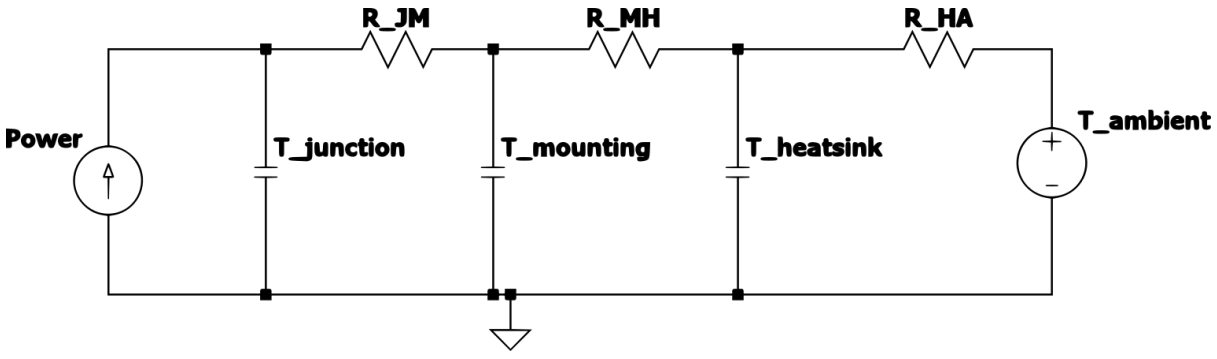

Figure 26: time dependent thermal model of the circuit

Conclusion

In conclusion, the exploration of buck and boost converters in this homework has provided a comprehensive understanding of their operational principles and limitations, particularly under ideal and non-ideal conditions. Initially, we derived the fundamental relations for both buck and boost converters, assuming ideal scenarios where all components operate perfectly without losses. This theoretical framework is crucial for understanding the basic functionality and potential of these converters in efficiently converting input to output DC voltages. However, the introduction of nonidealities, especially series resistances, significantly impacts these ideal derivations. Our analysis revealed that series resistances play a pivotal role in the performance of these converters, particularly under certain conditions. This impact is profound as it limits the practical efficiency and effectiveness of these converters, diverging from the ideal cases. We observed that while theoretically, buck and boost converters can achieve a wide range of conversion rates, practically, maintaining conversion ratios of 2 to 5 is more feasible due to the influence of nonideal components. Furthermore, our comprehensive power loss calculations illuminated how these nonidealities, especially resistive losses, diminish the efficiency of the converters. By examining the voltage and current characteristics under various conditions, we gained deeper insights into the operational limitations and practical constraints of buck and boost converters. These observations underscore the importance of considering real-world component imperfections when designing and implementing these converters. In essence, this homework underscores the complexity and challenges in achieving high efficiency in power conversion systems. It highlights the necessity of balancing theoretical principles with practical considerations, such as component nonidealities, to optimize the performance of buck and boost converters in real-world applications.