MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EE464 Term Project

Final Report

Group: The Isolated Ones

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ABSTRACT

To introduce the initial design of the Term Project for the EE464 Static Power Conversion II course, our group, The Isolated Ones, has compiled this final report. The primary objective of the term project is to create an isolated DC-DC battery charger. This report includes specified requirements, topology selection, simulation results, component selection, magnetic design, test results of the final design, .

INTRODUCTION & SPECIFICATIONS

In this project, we are going to create isolated battery charger system from a DC source. This entails designing an DC-to-DC power converter circuit with the necessary control mechanisms. Since DC sources are not constant, we need to design a system that gives the same output voltage while the input voltage is changing. Design specifications are given below:

- Input Voltage: 20-40 V DC
- Output Voltage: 12 V
- Output Power: 60 W
- Output Voltage Peak-to-Peak Ripple: %3
- Line Regulation: %3
- Load Regulation: %3

TOPOLOGY SELECTION

In this section, we are going to compare three topologies, which are flyback converter, forward converter, and push-pull converter to choose which topology we are going to use.

Comparison of the three converter topologies according to five different criteria is shown in Table 1. According to this table, even though the efficiency and voltage ripple of the flyback converter are worse compared to the other topologies, we chose the flyback converter topology because we won't be working with high power applications, and its lower cost and complexity are more important to us.

	Efficiency	**Output Ripple**	**Power Range**	**Complexity**	**Cost**
Flyback Converter	Moderate efficiency	Higher output ripple	Low to medium power	Least Complex	Cheapest
Forward Converter	Better efficiency	Lowest output ripple	Medium to high power	Medium Complexity	Medium
Push-Pull Converter	Can also have good efficiency	Moderate output ripple	Medium power	Most Complex	Most Expensive

Table 1: Topology Comparison

ANALYTICAL CALCULATIONS

Magnetic Design

From the previous experiences, we agreed that the most difficult part of this project to choose suitable control unit and control the switching actions. Due to that, we fist choose a controller UC3845. We also find another controller LT3757, but it is much more expensive, so we decided to do calculations according to UC3845.

UC3845 can supply a duty cycle of 0.5 maximum, which gives us an upper boundary to choose our duty cycle. Hence, we have chosen a duty cycle range of 0.2 to 0.4. To ensure that the controller gives a duty cycle in this range, our turns ratio should be 1:1. This can be calculated as follows:

Due to the diode between the secondary side and the load, assume secondary voltage as 12.75V ($V_{secondary}$= 12.75V) so that our output voltage is around 12V. Moreover, it is known that the voltage equation of a flyback converter is as follows:

$$\frac{V_1}{V_2} = \frac{D}{1-D} * \frac{N_2}{N_1}$$

Where V_2 = 12.75 V, V_1 = 20-40 V. When V_1 = 20 and $N2/N1$ ratio is taken as 1, D_{max} is found as around 0.39. Furthermore, when V_1 = 40 and $N2/N1$ ratio is taken as 1, D_{min} is found as around 0.24.

For the transformer of the flyback converter, we have selected an E-core with a gap of 1mm. The datasheet of the core can be found in the appendix section. An E-core is selected since the leakage flux in E cores is smaller than toroid cores due to their shape. Moreover, due to the existence of coil formers for each and every E-core, it is much easier to wind the coils to the core. Also, since we are to design a flyback converter, the energy should be stored in the core first to transfer the energy to the secondary side. Hence, an E-core with a gap is required for us to implement a better solution to store the energy in the core when the switch is ON. Another reason for us to select this core is that it has a high permeability, even with the air gap, and it does not have a high volume, with a volume of 11.5 cm3, so that the core will not take up so much space in our final design. In order to find the required number of turns for both the primary and the secondary, which are the same for our design, we need to determine the magnetizing inductance value first. By using the magnetizing inductance formula in the Application Note, AN4137, Design Guidelines for Off-line Flyback Converters Using FPS [1], the magnetizing inductance L_m can be calculated as follows:

$$L_m = \frac{\left(V_{s,min} * D_{max}\right)^2}{2 * P_{in} * f_s * K_{RF}}$$

where P_{in} is the input power, which is selected as 72W to ensure an efficiency more that 80%, K_{RF} is the ripple factor, which is defined as in the Figure 1 and selected as 0.35. f_s is the switching frequency, which was selected as 80 kHz. The core selection was done according to this frequency level. However, in order to decrease core losses, we decreased it to 80 kHz.

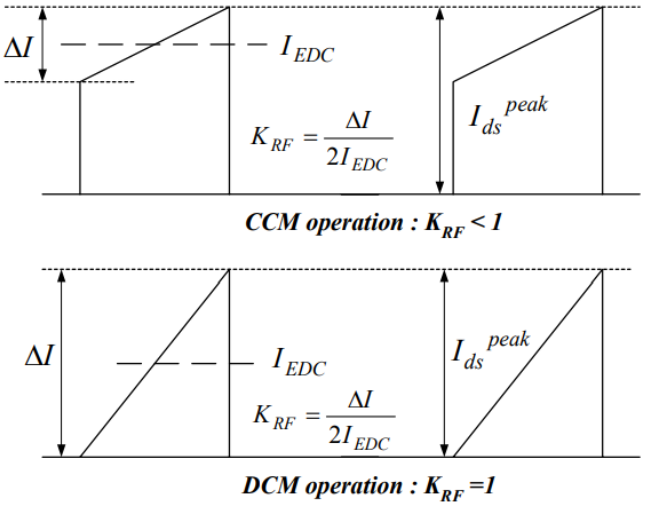


Figure 1. MOSFET Drain Current and Ripple Factor

After putting the values into the equation, L_m is found to be 20.58 µH. Then, to find the required number of turns of the primary, the A_L value of the core is used, and the required number of turns is found by using the following formula:

$$N^2 = \frac{L_m}{A_L}$$

We have selected the core "B66363G0500X187" which is an N87 type ETD39 ferrite core from TDK Electronics, where A_L value of the core we have selected having a 1mm of air gap is 196 nH/T^2. Hence, after making the calculation, the required number of turns are found as 11, approximately. Moreover, by limiting the Bmax value, the minimum required number of turns can also be calculated to check whether the previously calculated number of turns is valid or not by using the formula present in [2] as follows:

$$N_{min} > \frac{V_{s,max} * D_{max}}{B_{sat} * A_{effective,core} * f_s}$$

where B_{max} is selected as 0.2T, and effective area of the core we have selected is 125 mm^2. When putting all the numbers to the equation above, it is found that minimum required number of turns should be larger than 7.77 turns (N_{min} > 7.77 turns). This concludes that 11 turns in the primary and the secondary meet the requirement of minimum turns and can be used further in this design.

When the required number of turns is taken as 11, the inductance value of the primary winding can be calculated as 23.71 µH. Also, by knowing the relative permeability (μ_r = 115) and the effective length of the core (l_e = 92.2 mm), the actual magnetic flux density can be calculated by using the Ampere's Circuital Law:

$$N * I_{max} = \int H_{max} * dl = 11 * 12.5 = H_{max} * 92.2 * 10^{-3}$$

$$H_{max} = 1489.4\frac{A}{m}$$

Where I_{max} is calculated as follows:

$$I_{EDC} = \frac{P_{in}}{V_{in,min} * D_{max}} = \frac{72}{20 * 0.39} = 9.25\ A$$

$$\Delta I = 2 * I_{EDC} * K_{RF} = 2 * 9.25 * 0.35 = 6.47\ A$$

$$I_{max} = I_{EDC} + \frac{\Delta I}{2} = 12.48\ A$$

Then, B_{max}, can be found as follows:

$$B_{max} = \mu_r * \mu_0 * H_{max} = 115 * 4\pi * 10^{-7} * 1489.4 = 0.215\ T$$

The value found is well below the saturation value of the used core, which is found to be 0.4T. Despite slightly increasing the core loss of the transformer, it has no effect on the design.

In order to determine the cable size in AWG system, the switching frequency and the current capability of the cable should be considered. Since our switching frequency is 80kHz and the RMS value of the current in the primary is around 9.5 A, a wire that can carry a current having these features should be selected. Also, when the skin depth is calculated using the equation $\delta = \frac{75}{\sqrt{f_s}}$, where the unit of the skin depth is mm, and skin depth is found as 0.265 mm. Thus, the selected cable should also have a radius smaller than 0.265mm and have a power transmission capability up to 107kHz, minimum. Hence, we selected a cable with a size of AWG 26. In order to carry the current in the primary and the secondary side of the transformer, more than 26 AWG26 size cables should be paralleled. Since one AWG26 cable can carry up to 0.361 A, the number of required cables is calculated as follows [3]:

$$I_{RMS} = I_{EDC} * \sqrt{1 + \frac{1}{12}\left(\frac{\Delta I}{I_{EDC}}\right)^2} = 9.25 * \sqrt{1 + \frac{1}{12}\left(\frac{6.47}{9.25}\right)^2} = 9.43\ A$$

$$n = \frac{I_{RMS}}{0.361} = \frac{9.43}{0.361} = 26.13 \rightarrow n = 27\ will\ be\ used$$

One AWG26 cable has a cross section area of 0.128 mm^2, but this value is taken as 0.14 mm^2 by considering the insulation of the cables to have a more realistic calculation. Moreover, the window area of the used core is given as 178 mm^2 in its datasheet. Hence, the fill factor can be calculated as follows:

$$fill\ factor = \frac{2 * 0.140 * 27 * 11}{178} = 0.46$$

Which is an acceptable value.

In order to calculate the copper losses of the transformer, the ohms per km value of the AWG26 cable, which is 133.8568 Ω/km is used to calculate the DC resistance of the cable. Also, the mean path length of the core is given in its datasheet as 69mm. Then, the DC resistance of the cable can be calculated as follows:

$$R_{DC} = \frac{133.8568 * 69 * 11}{27 * 1000000} = 0.0038\Omega$$

The AC resistance of the cable in 80kHz is calculated using the following formula:

$$\delta = \sqrt{\frac{\rho}{\pi * f_s * \mu}}$$

$$A_{eff} = \delta * \pi * d$$

$$R_{AC} = \frac{\rho * l}{A_{eff} * 27} = \frac{0.09213}{27} = 3.75 * 10^{-3}$$

where d is the diameter of the conductor. As can be seen from the resistance calculations, the DC resistance and the AC resistance are very close to each other. Hence, a higher value can be used to have a more robust calculation. Then, the copper losses in the conductor becomes:

$$P_{cu} = I_{RMS}^2 * R_{AC} = 2 * 9.43^2 * 3.8 * 10^{-3} = 0.67W$$

The above equation is multiplied with 2 since RMS values in the primary and in the secondary are the same since the turns ratio of the transformer is 1.

As declared previously, the selected core is "B66363G0500X187" which is an N87 type ETD39 ferrite core. In its datasheet, the core loss graphs are given for different frequencies and for different magnetic flux densities for different temperatures. The core loss value for 80kHz is given as 300kW/m^3, and also, the volume of the core is given as 11.5 mm^2. Hence, the core loss of the transformer can be calculated as follows:

$$P_{core} = 0.300 * 11.5 = 3.45W$$

Then, the total losses on the transformer can be calculated as:

$$P_{transformer} = P_{core} + P_{cu} = 3.45 + 0.67 = 4.12W$$

RCD Clamp Design

The RCD clamp is to suppress voltage spikes generated during switching transitions, ensuring protection for sensitive components. By providing a path for energy recovery from the leakage inductance of the transformer it reduces voltage stress on the power switch. For calculating the R_{clamp} and C_{clamp} we are going to use the formulas below. [4]

$$V_{clamp} = V_{max} - V_{in}$$

$$R_{clamp} = \frac{2 * V_{clamp} * (V_{clamp} - NV_{out})}{f_s * L_{leakage} * {I_{peak}}^2}$$

$$C_{clamp} = \frac{5}{R_{clamp}} * f_s$$

From the above equations, by putting V_{max}=90V, V_{in} = 40V, f_s = 80kHz, N = 1, $L_{leakage}$ = 250nH, and I_{max} = 25A during the transient, which is found from the simulation results, R and C parameters found as; $R_{clamp} = 300\ \Omega$, $C_{clamp} = 0.2\ \mu F$.

MAGNETIC DESIGN RESULTS

At first, we planned to create our own litz wire by paralleling AWG26 cables, but when we realized that we couldn't wind it as tightly as we calculated during cable winding, we chose to use ready-made litz wire. We wound the transformer with 11 turns on the primary and 11 turns on the secondary. To minimize leakage inductance, we wound the primary and secondary wires in parallel. Primary winding inductance, and leakage inductance measurements are provided in Figure 2, Figure 3 respectively.

Figure 2.Magnetizing Inductance

Figure 3.Leakage Inductance

SIMULATION RESULTS

To ensure the functionality of our design and choose components based on current and voltage readings, we conduct simulations using LTspice environment, incorporating non-idealities. Simulation schematic is given in Figure 4.

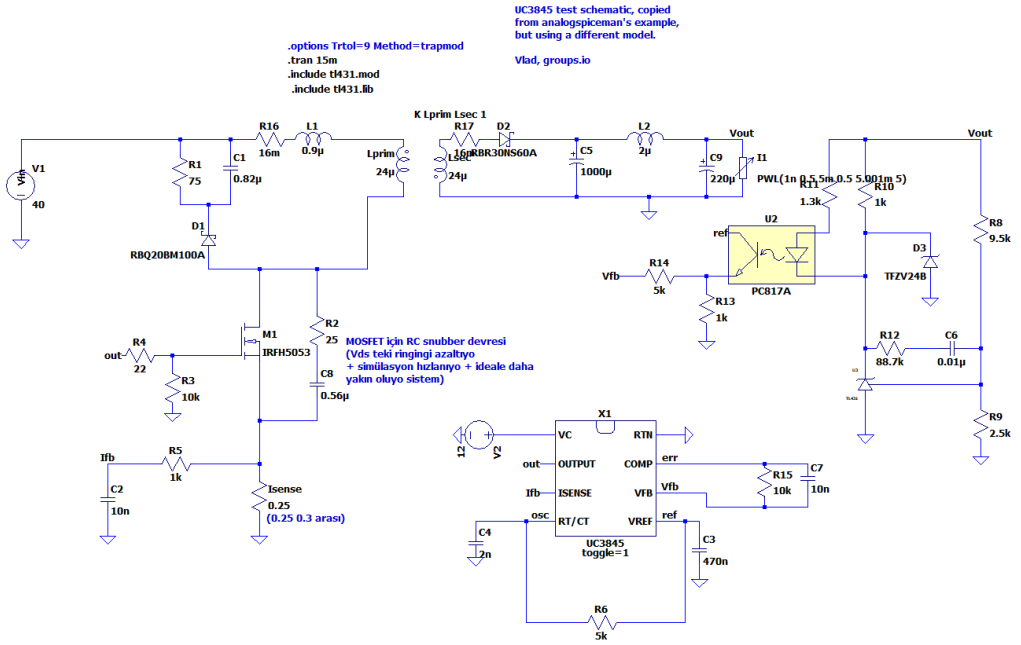


Figure 4. Simulation Schematic of Flyback Design

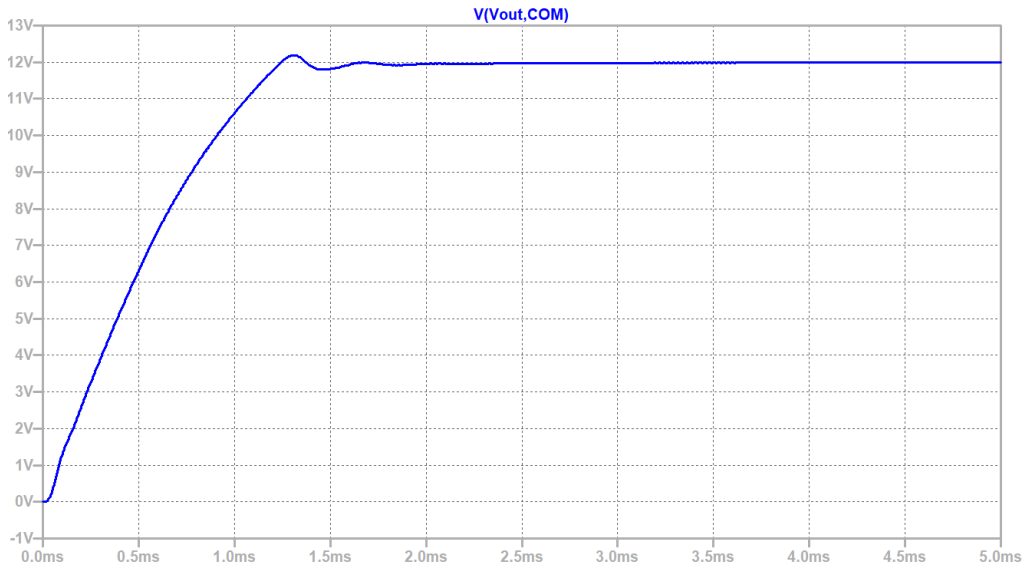


Figure 5. Output Voltage Waveform

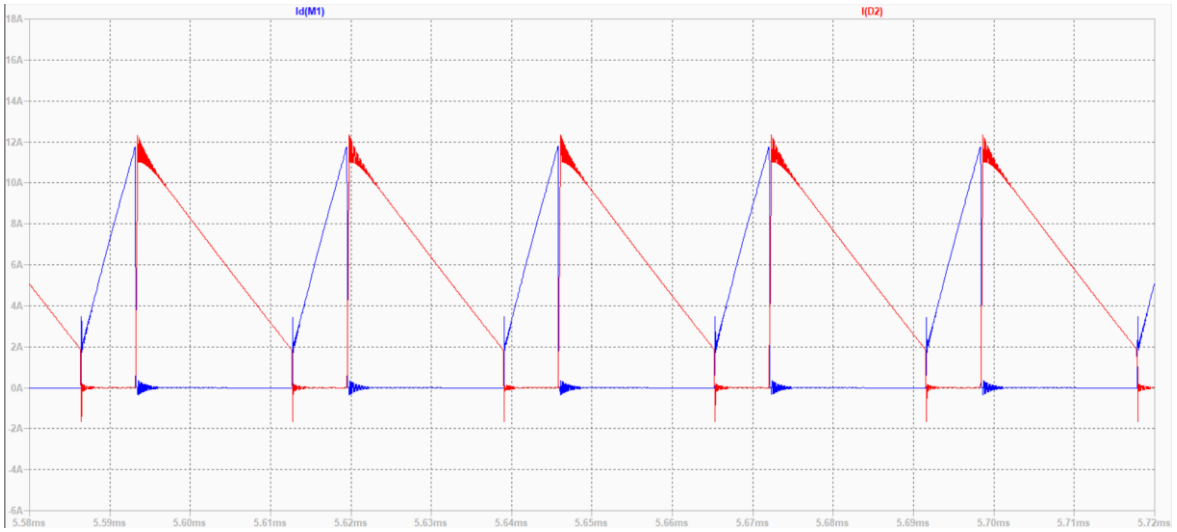


Figure 6. Current passes through MOSFET (Blue) and D2 (Red) 40V input

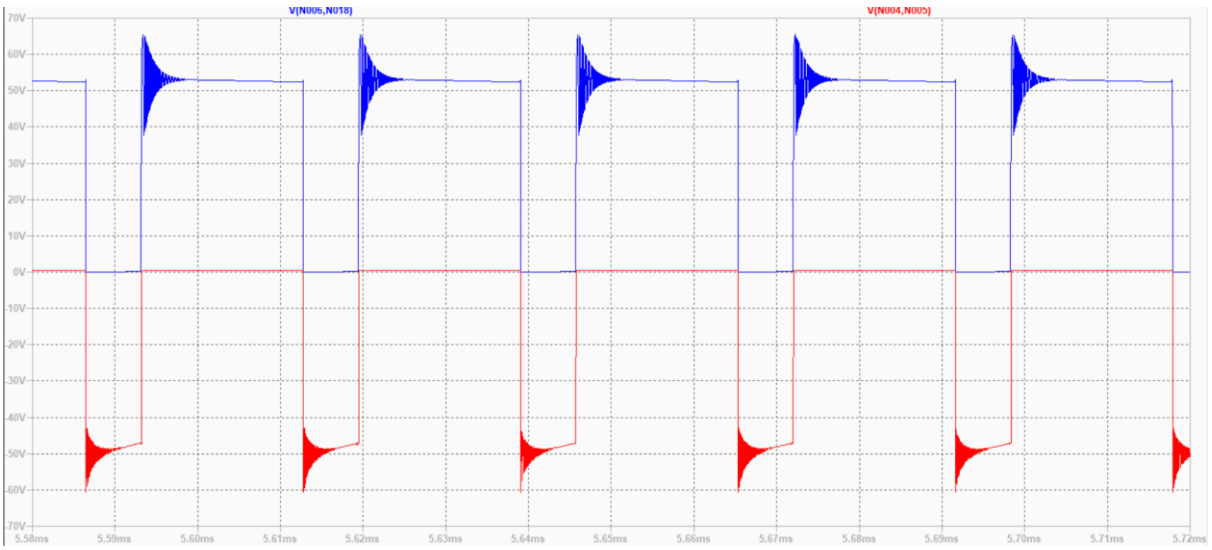


Figure 7.Voltage Stress on MOSFET (Blue) and D2 (Red)

Figure 5 shows the output voltage characteristic. Output inductance (L2) and capacitances (C5, C9) output voltage is much smaller than %3 of output voltage. Current passes through MOSFET (Blue) and D2 (Red) can be seen from Figure 6. As we can see from these graphs, our circuit works in CCM. Furthermore, maximum current on MOSFET is 12A and on diode is 9A. From the Figure 7, we can get maximum voltage stress on both MOSFET and the diode. The MOSFET and the diode that we will select must have voltage range greater than 70 V and 60 V respectively.

Figure 8 shows the output voltage response to changing input. In the specifications of the project, line regulation must be below to %3 which means 0.36V. When we zoom in, we can see from Figure 9 that voltage does not go below 11.64V.

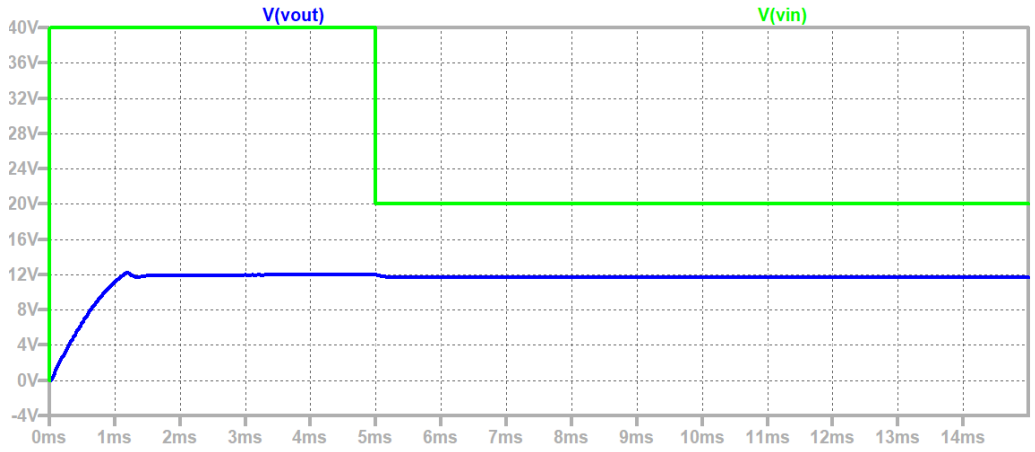


Figure 8. Output Voltage (Blue) Response to Changing Input Voltage (Green)

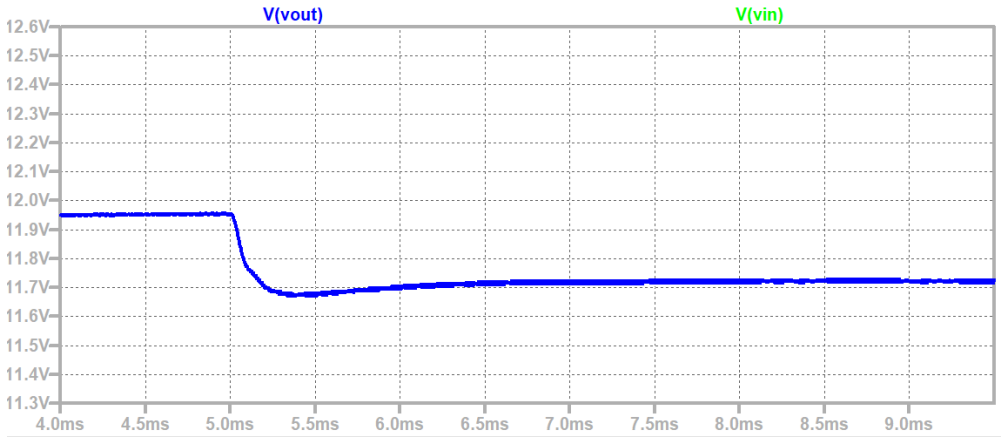


Figure 9. Output Response (Blue) when the Input Voltage (Green) Change

Figure 10 shows the output voltage response to changing load current. In the specifications of the project, load regulation must be below to %3 which means 0.36V. When we zoom into steady state value, we can see from Figure 11, voltage does not go below 11.64V.

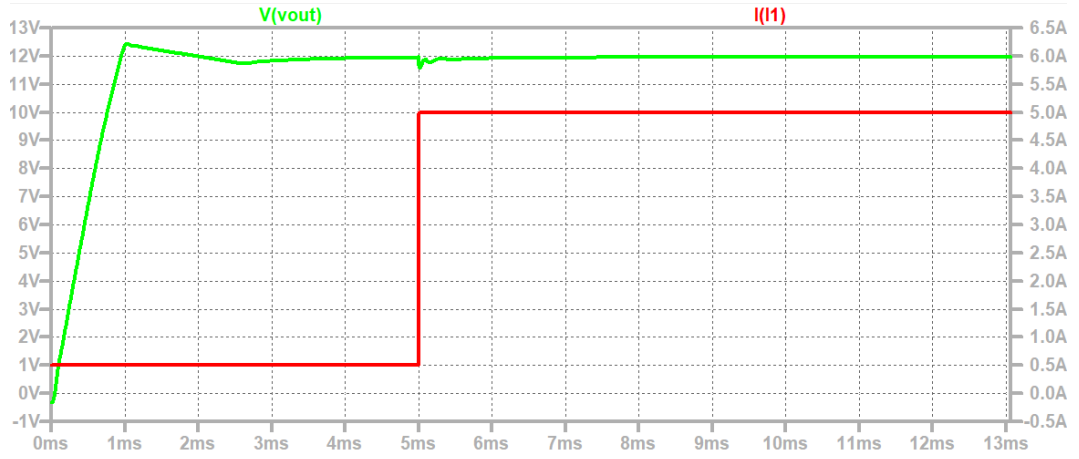


Figure 10. Output Voltage (Green) Response to Changing Load (Red) Current

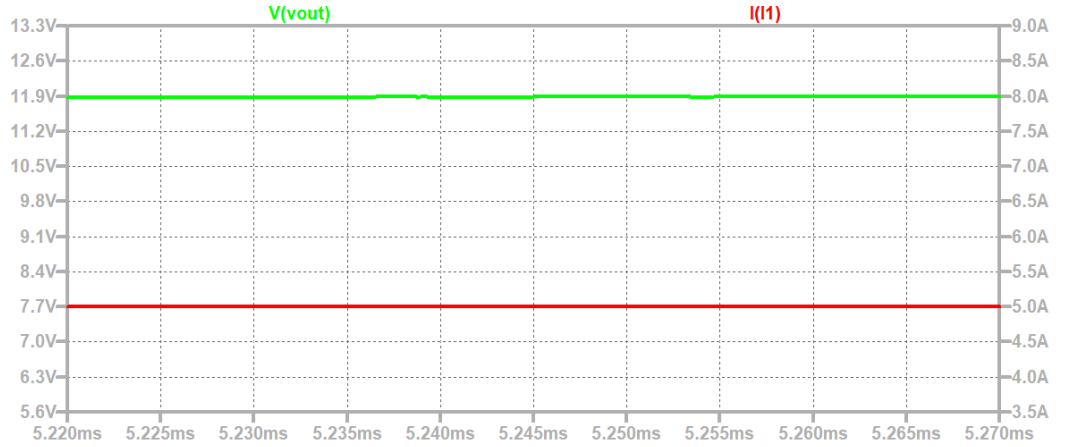


Figure 11.Output Response (Green) when the Load Current (Red) Change

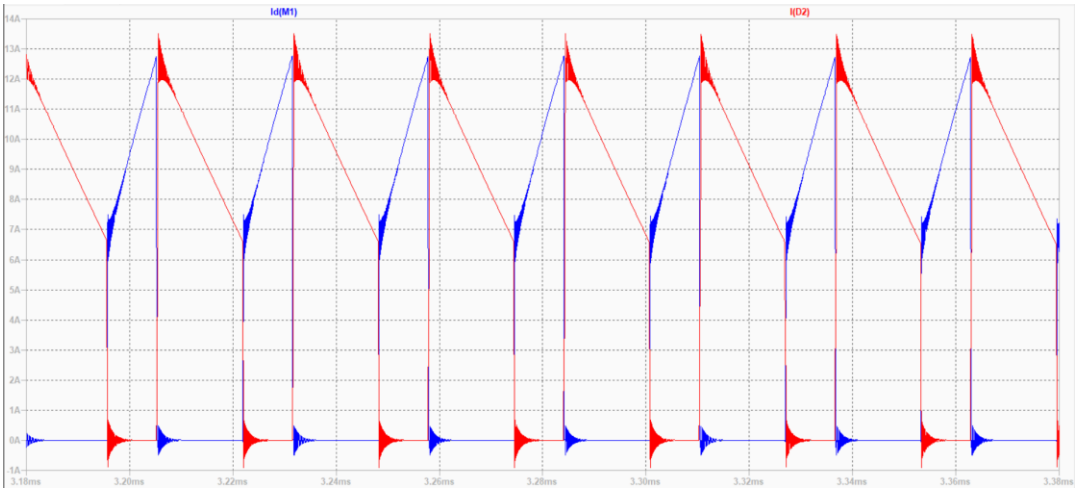


Figure 12. Current passes through MOSFET (Blue) and D2 (Red) for 20V input

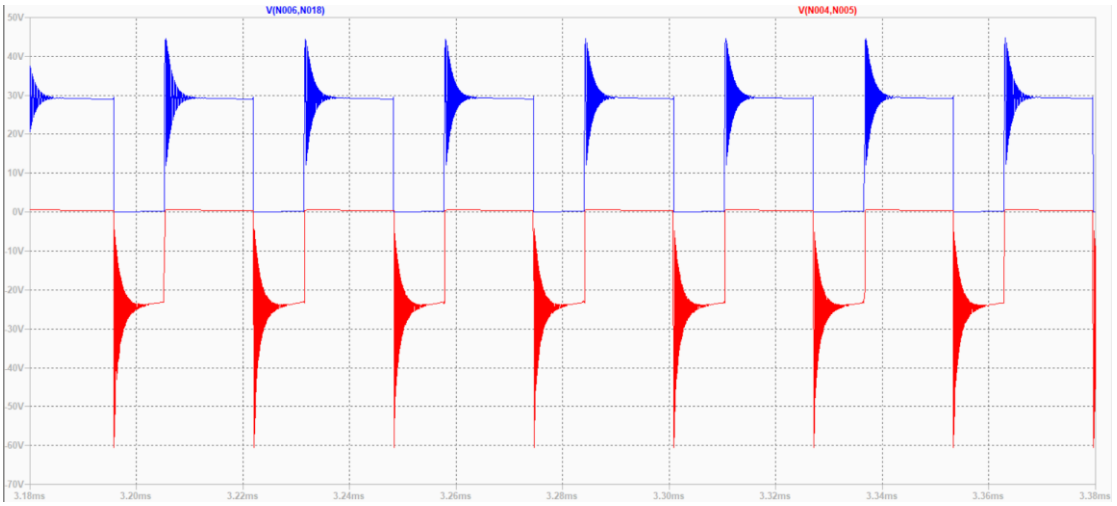


Figure 12. Voltage Stress on MOSFET (Blue) and D2 (Red)

According to the simulation results, when the input voltage is 40V, the output power is calculated as 59.57W, whereas the input power is 71W, which results in an efficiency of 84%. Moreover, when the input voltage is 20V, the output power is calculated as 59.5W, whereas the input power is 72.2W, which results in an efficiency of 82.4%.

COMPONENT SELECTION

After the simulation results, we have an idea about what the voltage and current limitations of the components would be. We decided to use the following components after an extensive search.

For minimum input maximum load case transient current of the secondary diode reaches 24A and transient current of the RCD clamp diode reaches the 22A. For the maximum input voltage maximum load case, transient reverse voltage of the secondary diode reaches 60V and the transient reverse voltage of the RCD snubber diode reaches 78V. Therefore, **DSA30I100PA** diode is chosen for both of them which has 30A current rating and 100V voltage rating.

For 40V input 85V and 26A is observed on the MOSFET during transient. For 20V input 65V 24A is observed on the MOSFET during transient. Therefore, **IRFZ540N** power MOSFET is chosen as the switching device which has 33A current rating and 100V voltage rating.

Since we decided to control our converter with **UC3845**, **TL431** shunt regulator and **PC817** optocoupler are chosen for the control operation which are commonly used with UC3845.

There is an excessive power loss on the current sense resistor. Since UC3845 reads the voltage drop on this resistor we decided to use **ACS712-30** Current Sensor instead of a resistor to eliminate the losses on the sense resistor and to increase the efficiency.

DESIGN MODIFICATIONS

During the design and implementation process, we have faced some difficulties and observed some points that can be improved. Therefore, we needed to modify some of the parts of our circuit to obtain the desired operation.

- After constructing the circuit on the stripboard and testing it before the demonstration, we observed that our Type-2 compensator designed using TL431 voltage reference IC at the feedback side does not work as desired. Our circuit was not able to feed the output voltage back to the controller and hence, our controller was not able to adjust the duty cycle accordingly. Thus, we disregarded the Type-2 compensator at the feedback side constructed with TL431 voltage reference IC. We used a 10V Zener diode and a 1kΩ resistor before the optocoupler. Moreover, in order to fine tune the output voltage, we added a potentiometer in front of the optocopuler resistor. In this way, we achieved to feed the output voltage back to the controller as desired and we observed that our controller, UC3845, is able to adjust the duty cycle to regulate the output voltage.

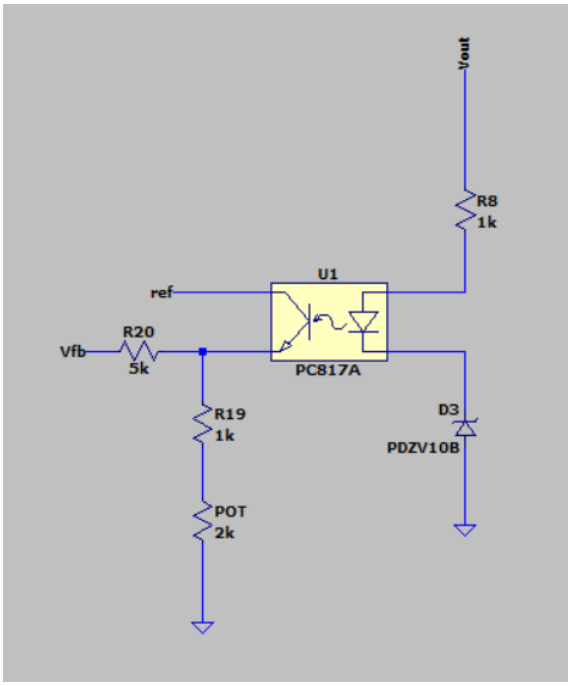


Figure 13. Modified voltage feedback circuit

- One of the changes we added is a fan to prevent the overheating of the MOSFET. By doing that we increase the performance period and increase the efficiency. Even though adding an external component usually decrease the efficiency, since the fan helps MOSFET to cool down, efficiency increased.

- Another modification is, we added 10kΩ resistor to assist in the discharge of the output capacitor. By doing that we protected the device in situations where it suddenly went to no load.
- At the beginning, in order to eliminate the losses on the sense resistor, we had planned to use a current sensor, as discussed in the component selection section. In order to place the current sensor, we had constructed a circuit with OPAMPs to map the voltage generated by the ACS712-30 current sensor as if it was a shunt resistor. However, when we measured the signal coming to the "ISENSE" pin of UC3845, we observed that the it does not match with the MOSFET current waveform, which was due to the bandwidth of both the current sensor and the OPAMPs we used. Moreover, we detected that there exists a phase shift between the current on the MOSFET and the voltage coming t to the "ISENSE" pin of UC3845, which was also due to the bandwidth of the OPAMPs we used. Consequently, we used a shunt resistor to sense the MOSFET current and connected it to the "ISENSE" pin of UC3845.
- In the initial design, we did not put any capacitors to the input side since both the input and the output is DC. However, we observed that our input current contained some ripples. Moreover, during the start-up, our circuit drew excessive currents from the source. In order to solve these problems, we have connected one electrolytic, one film, and one ceramic capacitor in parallel to the input side.
- After running the first simulation, in order to get rid of the output voltage and current ripples after we observed them, we have designed an LC filter and obtained a ripple free output voltage and current. However, during the demonstration, the inductor of the LC filter is removed since it is recognized that its current affected the operation of the controller badly. Hence, we have short circuited the inductor of the LC filter. After that, we obtained a significant increase in the efficiency.

EXPERIMENTAL and PERFORMANCE RESULTS

In this part, we are going to represent the experimental results obtained after the final demonstration. Figure 14 represents the test setup. Figure 15, Figure 16 and Figure 17 represent the full load, half load and quarter load conditions at 20 V input, respectively.

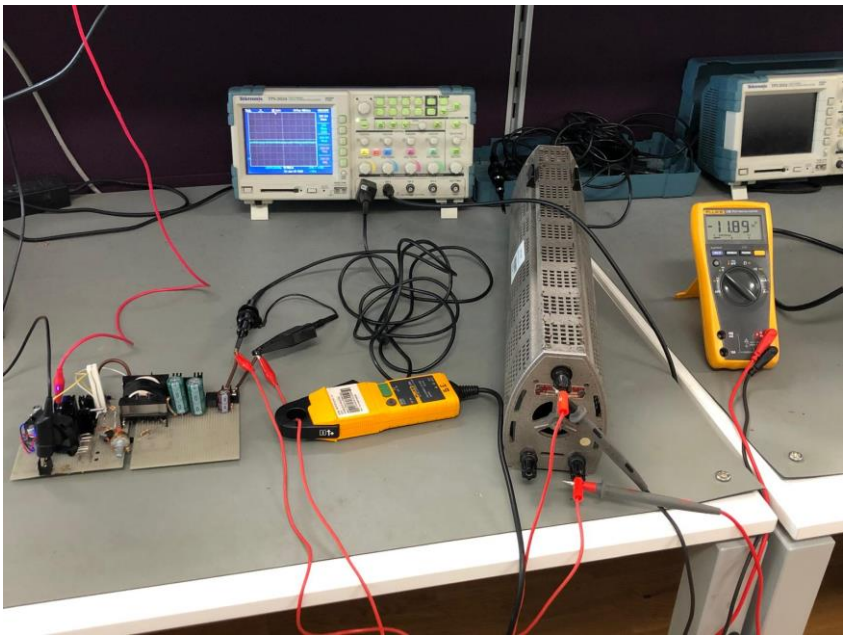


Figure 14. The test setup when the experimental results are collected

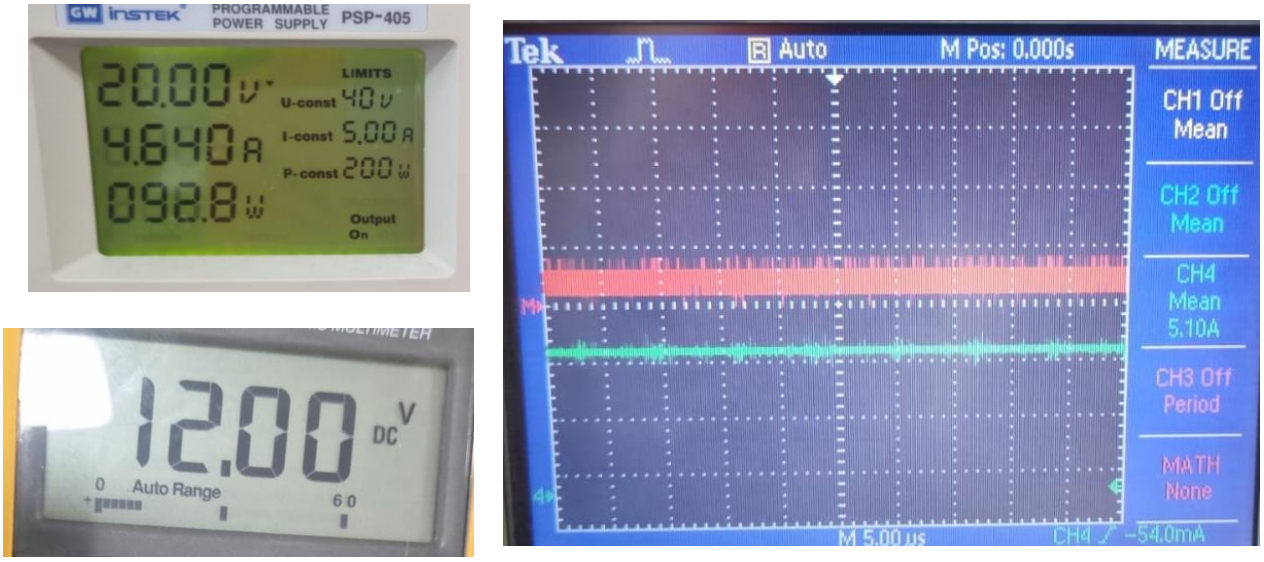


Figure 15. Full load condition with 20 V input

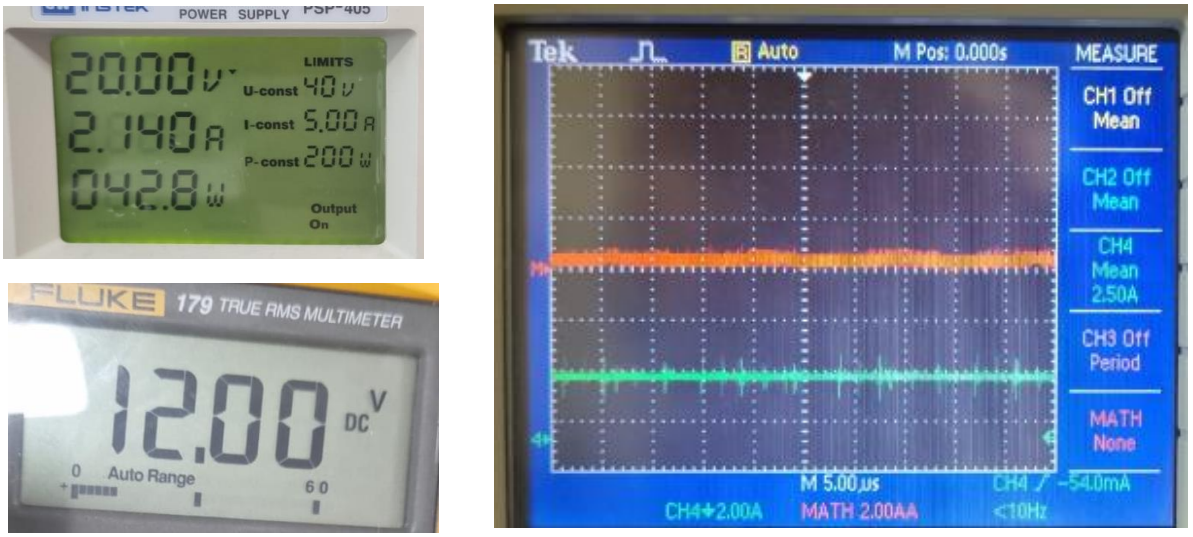


Figure 16. Half load condition with 20 V input

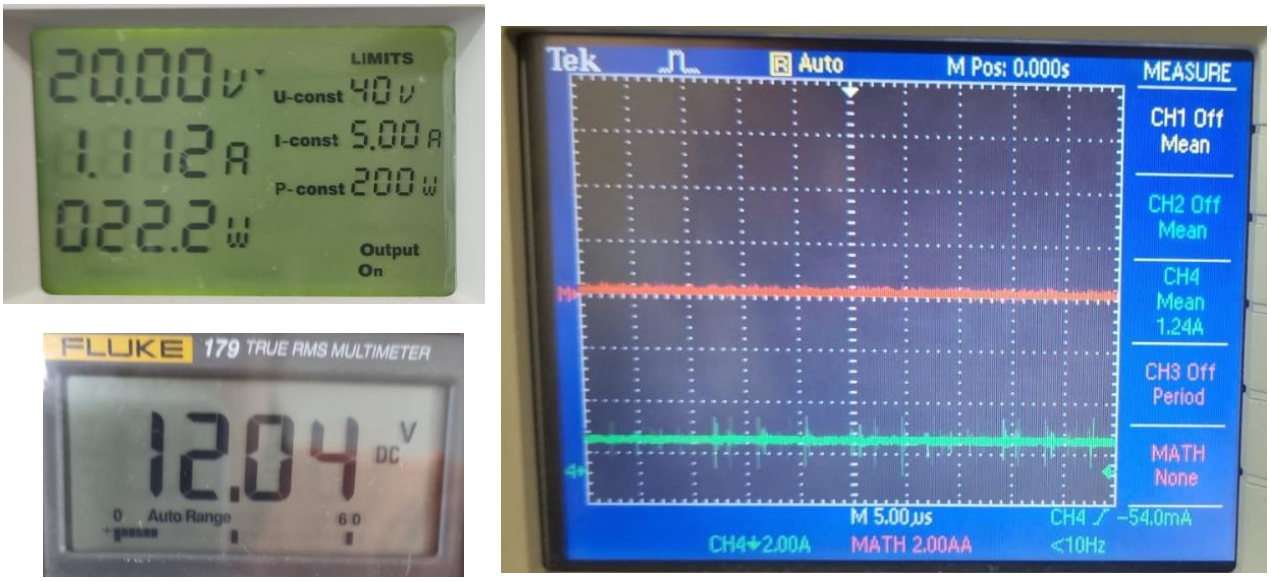
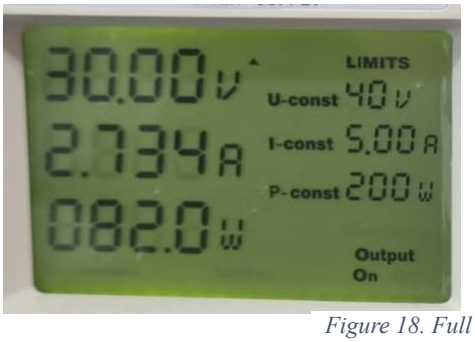


Figure 17. Quarter load condition with 20 V input

When we calculate the efficiency from the full load condition, efficiency will be 65%. However, during the final demo, efficiency calculated by Ogün Altun is 72% for the 20V full load case. From that we assume that while taking measurement, current sensing probe put -450mA offset.

The measurements taken for full load, half load and quarter load with 30V input are given in Figures 18, 19, 20 respectively. Furthermore, thermal data for the MOSFET after the 2-minute operation at 30 V full load condition is given in Figure 21.



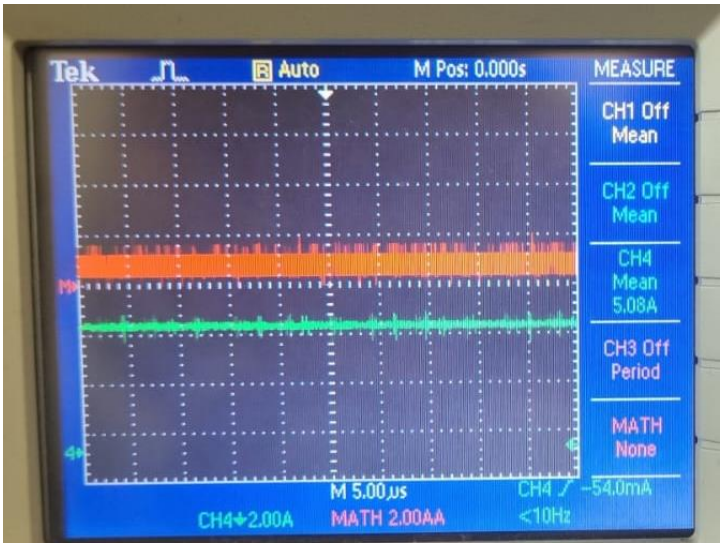


Figure 18. Full load condition with 30 V input

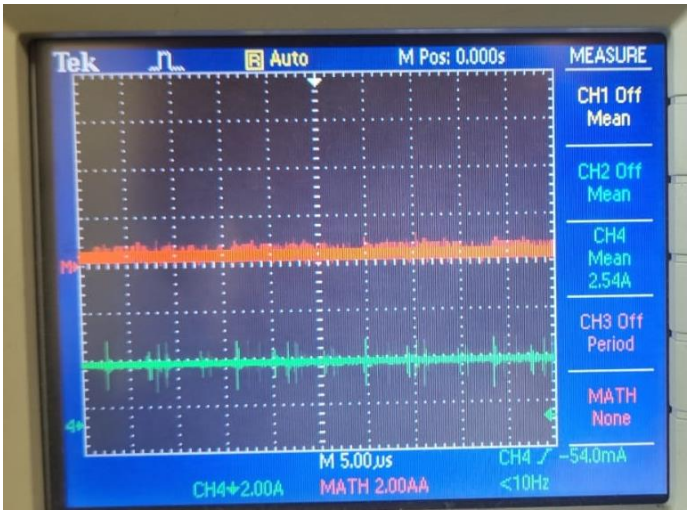


Figure 19. Half load condition with 30 V input

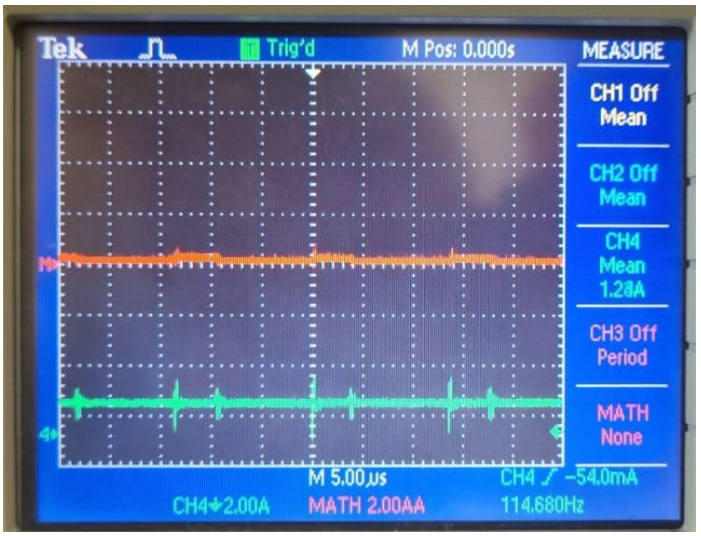


Figure 20. Quarter load condition with 30 V input

Figure 21. MOSFET temperature after 2 minutes of operation on full load with 30V input

As can be seen from the Figure 21, MOSFET temperature reach 61.4 °C. Since the selected MOSFET can resist up to 175 °C, this temperature increase will not damage the MOSFET.

The measurements taken for full load, half load and quarter load for 40V input are given in Figure 22, 23, 24 respectively. Furthermore, thermal data for the MOSFET after the 2-minute operation of full load condition at 40V input is given in Figure 25.

Figure 22. Full load condition with 40 V input

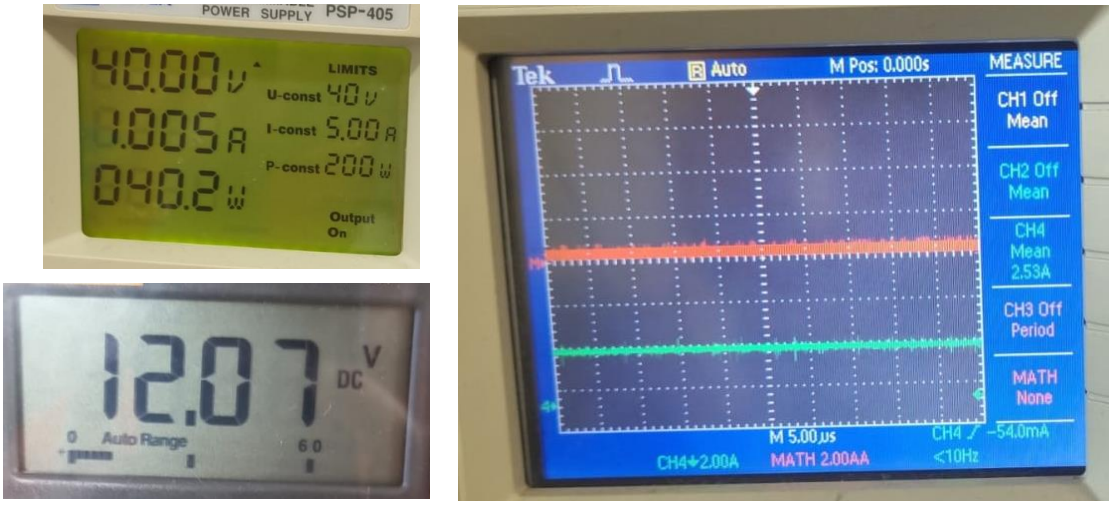


Figure 23. Half load condition with 40 V input

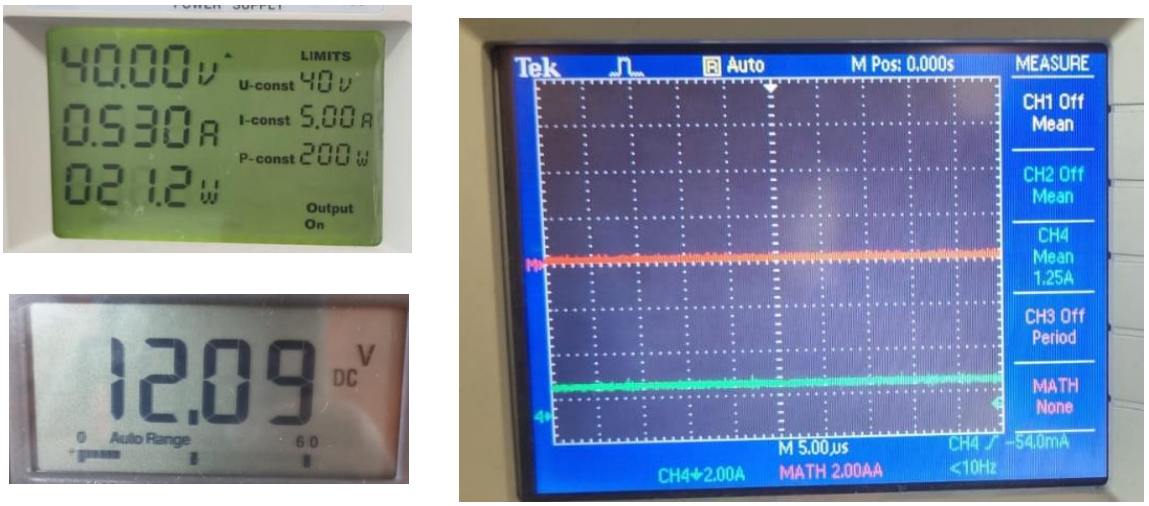


Figure 24. Quarter load condition with 40 V input

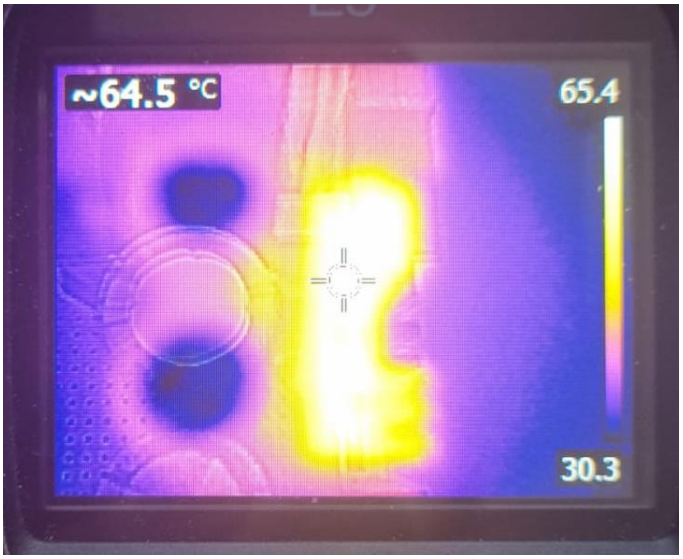


Figure 135. MOSFET temperature after 2-minute operation under full load with 40V input

The MOSFET temperature after 2-minute operation is higher than that of 30V input case. The reason for that the MOSFET initial temperature is higher in the 40 V case since the test are completed one after another.

The observed efficiency during the final demo for the 40V input case is 78%. However, the calculated efficiency according to taken data is 76%. From that calculation, we can assume that during taking the data, the current probe put nearly -450mA offset to the current measurements.

In Figure 26, the step response of the system to the sudden load change is shown. During this test, the load is disconnected at an instant and the output voltage response is observed.

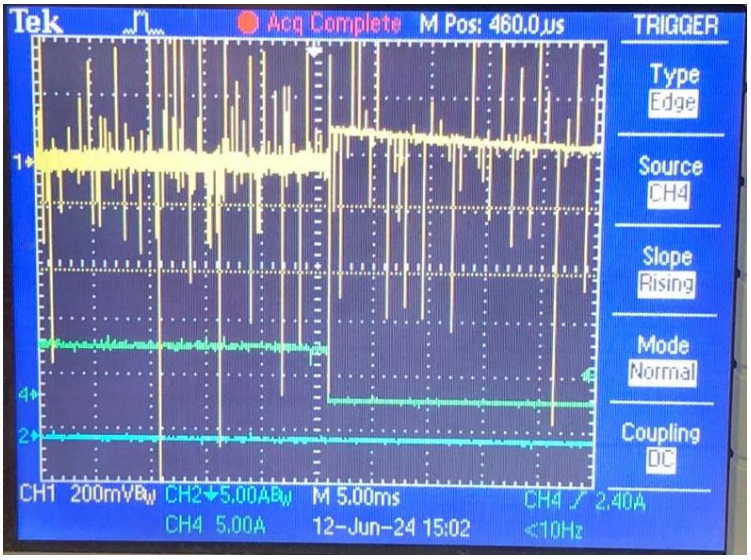


Figure 26. Step response of the system when the load is disconnected

As can be seen from Figure 26, when the load is disconnected, the output current drops to zero as expected. Moreover, the output voltage makes a peak at first, and settles down in about 20ms.

In Figure 27, the step response of the system to the sudden load change is shown. During this test, the disconnected load is connected at an instant and the output voltage response is observed.

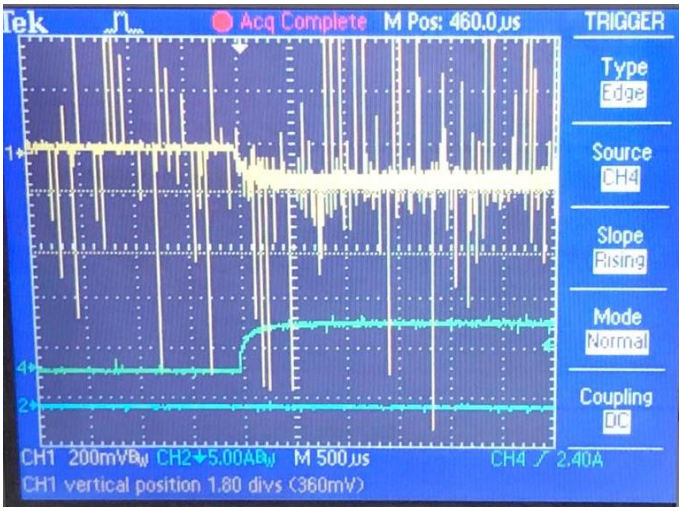


Figure 27. Step response of the system when the load is connected

Before the load is connected, the system was operating at no load condition. When the load is connected, the output current starts increasing and the output voltage starts decreasing. Both the voltage and the current settle in about 250 μs, which can be concluded from Figure 27.

CONCLUSION

In this report, as The Isolated Ones team, we share our design and approach to addressing the requirement for a device with a 20V-40V input and a 12V 60W output isolated battery charger. All process from beginning to end is explained in details in this report.

Our experimental results supported most of the theoretical calculations and simulations, confirming the viability of the chosen topology and design. Of course, there was several discrepancies between the simulation results and the test results. First of all, the efficiency calculation results are different between the simulation and the experimental results. This is mainly due to the fact that the power lost on the transformer cannot be modelled in the simulation environment. Even though the power lost on the transformer would have been taken into account while calculating the efficiency, the theoretical result will not match with the experimental results. This is mostly due to the nonidealities that were not modelled in the simulation and due to the resistances because of soldering. Moreover, we have not observed any oscillations at the output voltage and current in the simulations, we observed a little oscillation in the output voltage and ripple during the experiments. This is also due to the nonidealities in the circuit.

While the design proved successful, there is still room for improvement, particularly in PCB design and further optimization of the magnetic components. Overall, this project provided valuable insights into the complexities and practical considerations of designing isolated DC-DC converters.

REFERENCES

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[3] Alferink, F. (n.d.). Average and effective values. Average and effective values: Electronic

Measurements. https://meettechniek.info/compendium/average-effective.html

[4]: RCD Clamp Circuit Design

RCD Clamp (youtube.com)

APPENDIX

Link to core datasheet:

Ferrites and accessories - ETD 39/20/13 - Core and accessories (tdk.com)

Link to core material datasheet:

Ferrites and accessories - SIFERRIT material N87 (tdk.com)