STREET FIGHTER SVS SYSTEM NEW PRODUCT PLAN

PRODUCT DESCRIPTION

Street Fighter (SF) is a register configurable, cost optimized CapSense express solution for high volume, low end market. The SF SVS (System Validation Suite) project involves 1) Development of hardware, firmware and software required for validation of SF 2) Mode Transition (MT) Validation, 3) Systems Validation and 4) IP validation of SF. The validation is performed at both Pre silicon and Post Silicon stages. Validation of SF uses PSVP and SVS.

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OWNERSHIP

FINANCIALS + OVERALL NPP	BUM	DIRK
	TL	DEPK
	QA: PLRB Chair	BMT
MARKETING PLAN	PL MKT MGR	KRSH
	QA: MLRB Chair	RSUB
DEVELOPMENT PLAN	PM	VJYA
		RRAM
	TL	DEPK
	QA: PLRB Chair	BMT

MANUFACTURING PLAN	MFG MGR	RQB
	MGR TE	RQB
	QA: MFRB Chair	RQB
WHOLE PRODUCT PLAN	PL MKT MGR	KRSH
	QA: VP APPS	PDK
EXECUTION TO SPEC ON SCHEDULE	DCM	RRAM
	QA: VP PM	BMT

EXCEPTIONS

EXCEPTIONS	YES / NO	APPROVALS		COMMENTS
BUILT AT NEW CONTRACT MANUFACTURER?	NO	PM		No. Existing approved supplier used.
FUNDAMENTALLY NEW/DIFFERENT TECHNOLOGY?	NO	PM		None
	NO	PM		
	NO	PM		
	NO	PM		
	NO	PM		

RESPONSIBILITIES

TL	DEPK	We will follow the CY Design Policy faithfully. The Design Policy is our primary design specification for people (culture, training, quality, compensation), principles (block-based design or BBD), and processes (IP Vault, scheduling methods, goals and memos).
DCM	RRAM	We will ensure that all team members read, understand, and follow the CY Design Policy.
PM	VJYA	We will ensure the chip will be taped out with IP blocks exclusively from the IP Vault. Chip = Vault IP + wires. ("No FUTs or FURTL.").
		We will ensure that the chip meets its specifications with zero defects. Change the specification or change the chip.
PM	VJYA	We will ensure that all engineers on the team are well trained.
DCM	RRAM	We will ensure that all engineers on the team use goals to record tasks and memos to record accomplishments.
BUM TL	DEPK	We own the integrity of the EROS/IROS. We will not get caught designing a product properly to a poorly drawn spec.
PM TL	DEPK	We own the integrity of the Risk Mitigation Plan. We will warn about and react to risks early, during the project, not use them as after-the-fact excuses.
DCM	RRAM	I own design quality. Peer Reviews, Expert Reviews, Circuit Audits will be done with energy and thoughtfulness, not just to meet requirements. I will ensure that my design site is staffed to execute competently on their COE charters.
DCM	RRAM	I will use CY state-of-the-art tools/methods. We will not have a problem that was preventable by a CY tool we did not use.
PM	VJYA	I own the integrity of the schedule and resource plans. There will be no obvious mistakes in them. The schedule will be continuously valid.

PRESIDENT'S APPROVAL: _____N/A (cost < $250K)_____

STREET FIGHTER SVS: DOCUMENT HISTORY

STREET FIGHTER SVS SCHEDULE HISTORY										
REV	WHEN	NPP	PR3	TO	ES10	ES100	PR4	FQ	PR5	NPP MWs
**	1312	1312	1342	1340	1342	1350	1405	1405	1405	93

NPP SUMMARY ($M)		
UNDISC REV	DISC GM	DISC INV
0.0	0.0	0.1

REV	ECN NUMBER	WHO	CHANGE	DESCRIPTION OF CHANGE
**	3860126	DEPK	PROBLEM	Initial Release
			SCHEDULE	Initial Release
			FINANCIALS	Initial Release
			RCCA	Initial Release

PRODUCT DESCRIPTION

SF SVS project includes development of validation platform, Pre silicon validation, post silicon validation and system validation. This project will update and reuse the following from PSoC4A validation platform with SF specific modifications: MT validation platform, PSoC Component Validation Platform (PCVP) based IP validation suite. Additional target application boards to validate SF target applications shall be developed. The target application scenarios such as proximity sensing, touch intimation and water proofing will be validated.

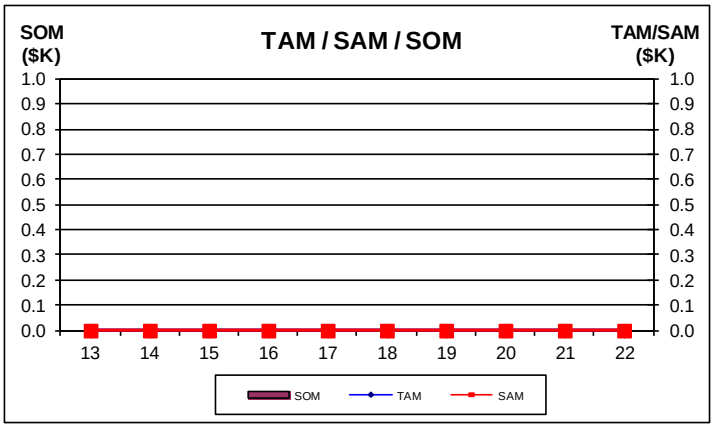
FINANCIALS	13	14	15	16	17	18	19	20	21	22
REV ($K)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
VOL(K)	0	0	0	0	0	0	0	0	0	0
ASP($)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
UCOST($)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DM (%)	-	-	-	-	-	-	-	-	-	-
GM($K)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
GM (%)	-	-	-	-	-	-	-	-	-	-
INV ($K)	99.24	9.66	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PROFIT($K)	#####	-9.91	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

MARKETING SUMMARY

Division:	PSD	**Business Unit:**	Capsense
10yr NPV ($K):	-133.95	**100% Automotive Bin:**	No
10yr ROI:	-1.00	**10yr Incremental ROI:**	-1.00
5yr ROI (Desired >2):	-1.00	**5yr Incremental ROI:**	-1.00
Discounted Inv ($K):	133.95		

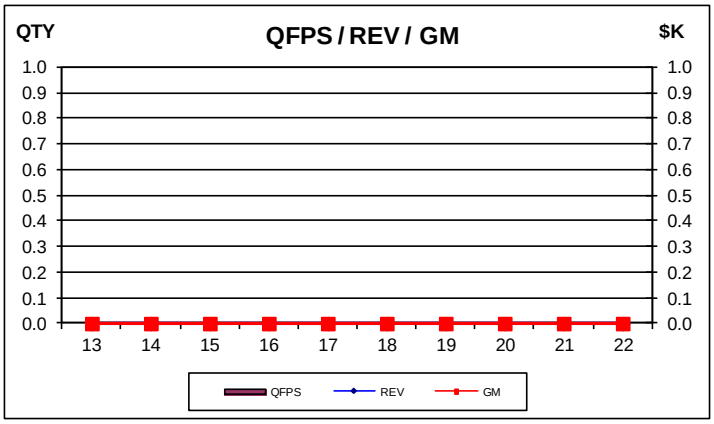
Product	Target Platforms	Lead Customers	PR4
SF Validation	Internal platform	N/A	WW4

The SF validation platform will not be sold separately as a product



DEVELOPMENT SUMMARY

Product Type:	NA	**Product Complexity:**	NA
Product Category:	A	**Process Complexity:**	NA
Technology:	Pick One	**Technical Leader:**	DEPK
Project Manager:	VJYA		

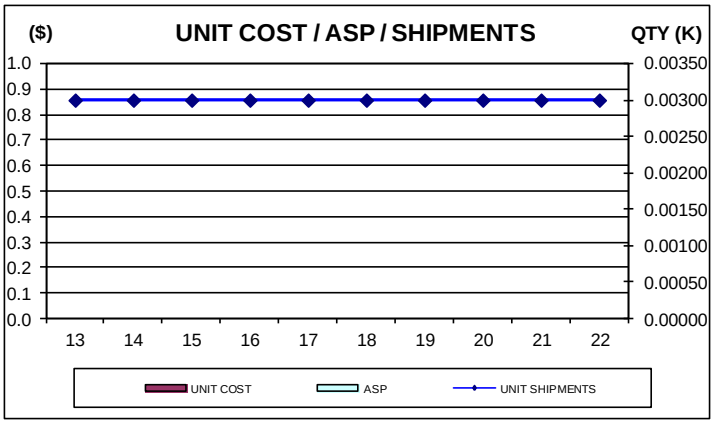


WHO	NPP-RCCA MILESTONE	OS	CS

The SF SVS project uses multiple hardware boards, PCVP based scripts, PSoC Creator firmware and documentation. The following hardware boards shall be developed: 1) MT validation board, 2) Processor module to interface with PCVP DUT board 3) Target application validation board and 4) CapSense Validation board. PCVP based scripts used for PSoC4A validation shall be reused for IP block validation after SF specific modifications. For new IPs, SRSS lite, CPUSS lite and Flash lite, additional PCVP based scripts shall be developed. PSoC creator firmware from PSoC4A shall be reused for existing IPs after SF specific modifications and new firmware shall be developed for new IPs.

LEAD PROJECT SCHEDULE		
MS	**OS**	**CS**
NPP	1312	1312
TO	1340	1340
ES100	1350	1350
PR4	1405	1405

* OS, CS DEFINED IN THE DEV PLAN



MANUFACTURING SUMMARY

Target application boards will be manufactured using contract manufacturer (CM). These are internal boards and volume manufacturing is not involved.

STREET FIGHTER SVS: FINANCIAL SUMMARY

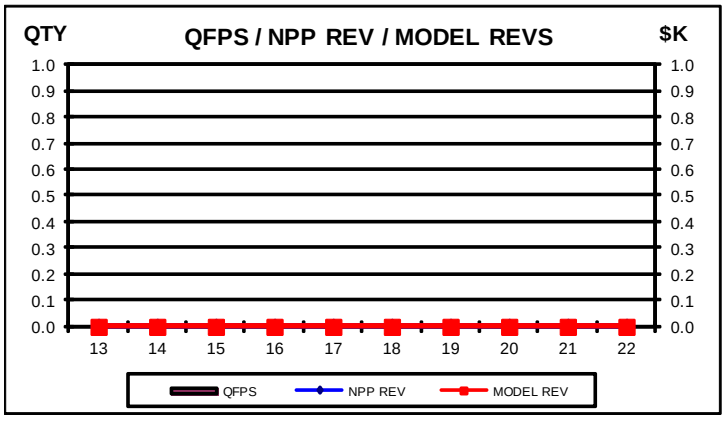
OWNER: KRSH
APPROVER: ?

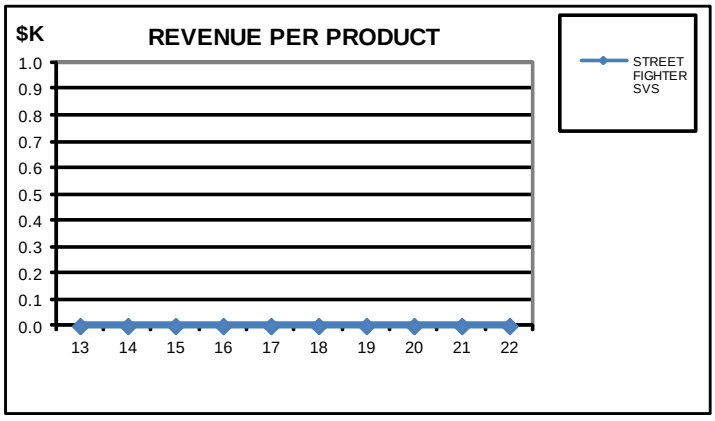
PROJECT PARAMETERS			
NPP NUMBER	001-85596	PM	VJYA
REVISION	**	PMM	KRSH
COST OF SLIP	**REV**	**MP COST**	**TOTAL**
1 QTR ($K)	0.00	44.36	44.36
1 MONTH ($K)	0.00	14.79	14.79
1 WEEK ($K)	0.00	3.41	3.41

FINANCIALS	
REVENUE ($K)	0.00
DISC REV ($K)	0.00
DISC GM ($K)	0.00
DISC INV ($K)	133.95
NPV ($K)	-133.95
10YR ROI	-1.00

KEY ASSUMPTIONS	
10 YRS STARTING IN	2013
CYPRESS DISC RATE	15.0%
Capsense TOT S&M OVH RATE	
Capsense TOT G&A OVH RATE	
INC. S&M OVH RATE	
INC. G&A OVH RATE	

P&L	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
STREET FIGHTER SVS										
SHIPMENTS (KUNITS)	0	0	0	0	0	0	0	0	0	0
ASP ($)	-	-	-	-	-	-	-	-	-	-
REVENUE										
PRODUCT REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
NON PRODUCT REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
TOTAL REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
AVG UNIT COST ($)	-	-	-	-	-	-	-	-	-	-
TOTAL DIRECT COST ($K)	-	-	-	-	-	-	-	-	-	-
DIRECT MARGIN ($K)	-	-	-	-	-	-	-	-	-	-
LEAKAGE ($K)	-	-	-	-	-	-	-	-	-	-
GROSS MARGIN ($K)	-	-	-	-	-	-	-	-	-	-
OPEX										
R&D										
MANPOWER COST ($K)	84.24	9.66	-	-	-	-	-	-	-	-
MASKS & HARDWARE ($K)	6.00	0.25	-	-	-	-	-	-	-	-
OTHER R&D EXPENSES ($K)	7.50	-	-	-	-	-	-	-	-	-
TOTAL R&D ($K)	97.74	9.91	-	-	-	-	-	-	-	-
S&M ($K)	-	-	-	-	-	-	-	-	-	-
G&A ($K)	-	-	-	-	-	-	-	-	-	-
TOTAL OPEX ($K)	97.74	9.91	-	-	-	-	-	-	-	-
OPERATING PROFIT (LOSS) ($K)	(97.74)	(9.91)	-	-	-	-	-	-	-	-
DIRECT MARGIN (%)	-	-	-	-	-	-	-	-	-	-
GROSS MARGIN (%)	-	-	-	-	-	-	-	-	-	-





SF SVS developed under this NPP will not be sold, and therefore, no revenue is planned. Costs consist of R&D expenses and the cost to build new hardware boards.

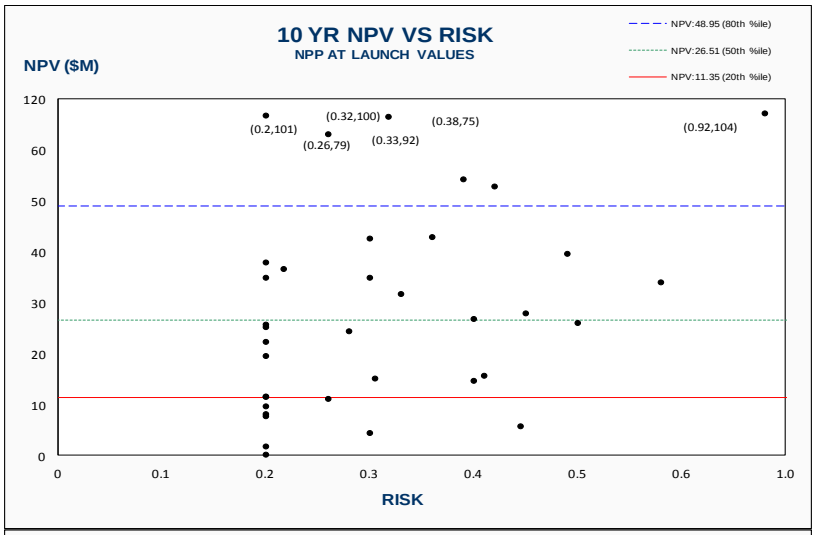
PRODUCT COMPARISON

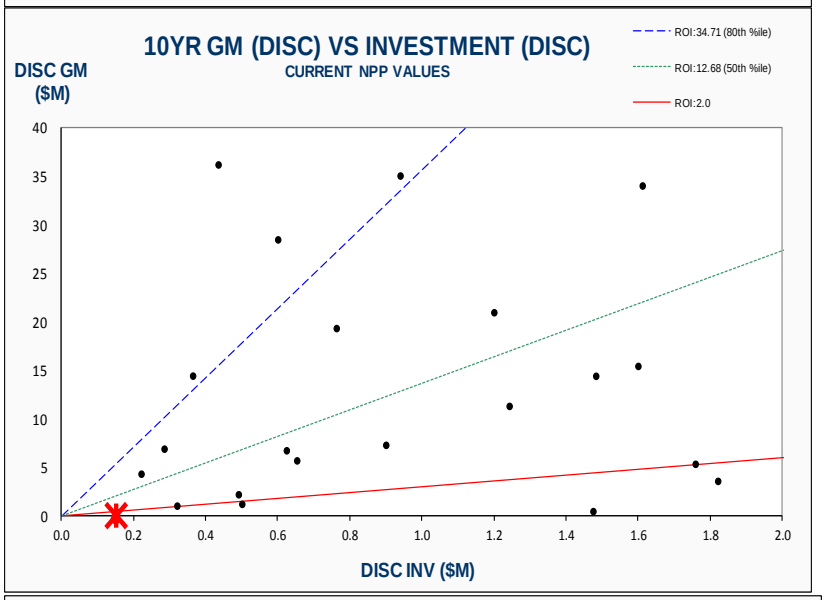
This is not applicable.

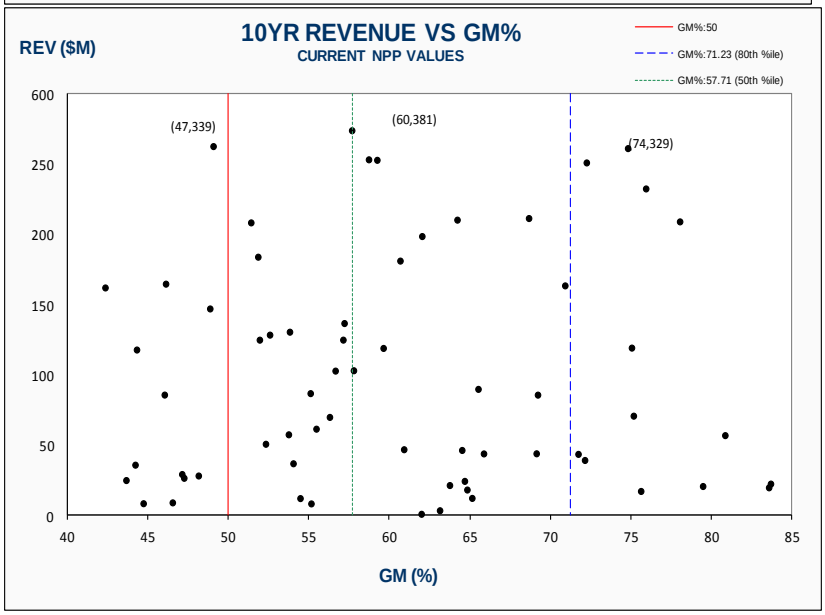
	PROJECT COMPARISON
✖	STREET FIGHTER SVS

The first chart compares this NPP to the Risk and NPV figures in the ** revision of the comparison NPPs. If the comparison products were not in the 10 year NPP format at launch they do not show up on the chart. Risk value is a function of Market, Internal Technical, and User Risks, with weights based on the product category. Risk values will range between 0.2 to 1.0. NPPs with risk values >0.6 will be considered high risk NPPs.
The second chart compares this NPP to the Disc Investment and Disc GM $ in the current revision of the comparison NPPs. This chart is fixed to one of three investment ranges: 0 to 2M, 2M to 10M or 10M to 60M. If the comparison products do not fall in the same range as this NPP they do not show up on the chart.
The third chart compares this NPP to the GM % and Revenue in the current revision of the comparison NPPs.

Each chart includes 50th percentile and 80th percentile lines as reference points. Additionally each chart has a lower threshold reference point which is 20th percentile (for NPV), 2.0 (for ROI) and 50% (for GM%)







SF SVS project consists of the following: 1) Development of validation platform (Hardware, firmware and software), 2) Mode Transition (MT) validation, 3) IP block validation and 4) Target application validation.

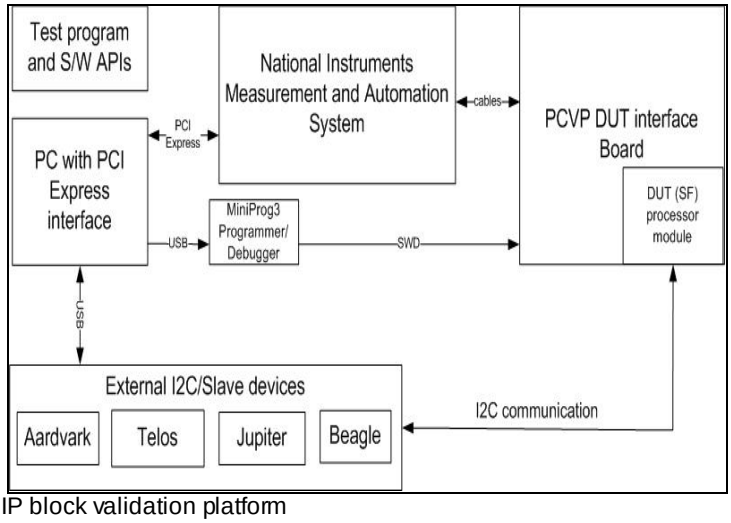
The validation shall be carried out in two stages: Pre-Si validation (before SF silicon is available) and Post-Si validation. The Pre-Si validation shall be performed on the PSVP (Pre Silicon validation platform). The PSVP platform is developed by the PSVP team (HFO) There are two types of PSVPs available, they are P4A based PSVP and FPGA based PSVP. The P4A based PSVP shall be used for the following: 1) To develop and debug MT validation test cases 2) To configure the CapSense firmware for target application validation. The FPGA based PSVP shall be used for the following: 1) To develop and debug IP block validation tests and 2) To validate the digital portion of all the IP blocks 3) Validate all the modes in MT validation and the transition between the modes that are available on the PSVP. Post the Si availability MT validation, IP validation and Target application validation shall be carried out on the actual silicon.

For IP block validation the PSoC Component Validation Platform (PCVP) shall be used for validation. The PCVP shall interface to the PSVP during pre-si validation stage and after the Si availability the actual silicon will be mounted on the PCVP DUT interface board for performing IP block validation.

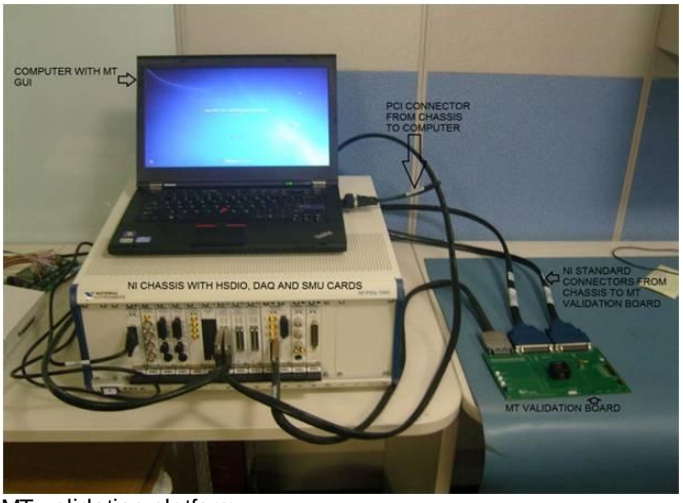
The following hardware boards shall be developed for SF validation:

1) Target application validation board
2) CapSense validation board
3) MT validation board
4) Street Fighter processor module

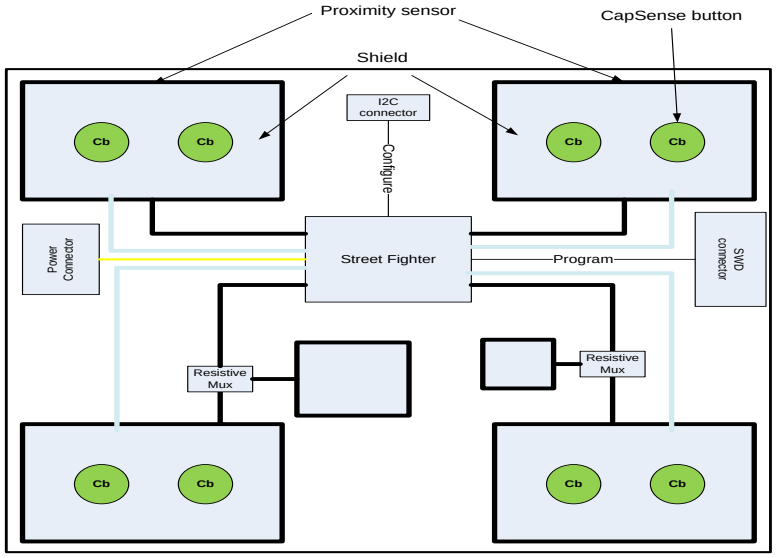
The setup for MT validation, IP validation and target application validation is shown below:



IP block validation platform



MT validation platform



Target application validation platform

No Marketing data as this is an internal project

TAM, SAM, AND SOM

No TAM, SAM and SOM as this is an internal platform

This is an internal project and there is no competitive summary.

System validation suite developed as part of this project will be used by the SF validation team for Pre-Si and Post-Si validation. It will be used for IP block validation, MT validation and Testing of Target Application scenarios.

SF validation project is an internal project, it is used by Si validation team and there are no target customers.

SF validation is an internal project and marketing plan is not applicable.

STREET FIGHTER SVS: FINANCIAL PLAN (fin_1)

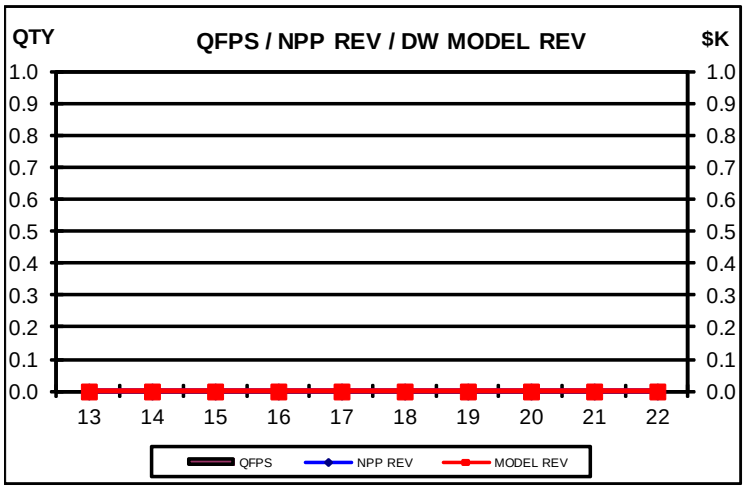
OWNER: KRSH
APPROVER: ?

PROJECT PARAMETERS			
NPP NUMBER	001-85596	DIV	PSD
REVISION	**	BU	Capsense
TOOLKIT REV	8.00	EVP	EHK
LEAD PROJ	1	PM	VJYA
STATUS	Active	PMM	KRSH
This device is a NF / CR?		NEW FUNCTION	

FINANCIALS	
REVENUE ($K)	0.00
DISC REV ($K)	0.00
DISC GM ($K)	0.00
DISC INV ($K)	138.71
NPV ($K)	-138.71
10YR ROI	-1.00

KEY INFORMATION	
DISCOUNT TO QTR	Q113
CYPRESS DISC RATE	15%
MANPOWER COST ($K)	139.32
MANPOWER OVERHEAD ($K)	3.51
MANPOWER OVERHEAD (%)	3%

P&L	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
STREET FIGHTER SVS										
SHIPMENTS (KUNITS)	0	0	0	0	0	0	0	0	0	0
ASP ($)	-	-	-	-	-	-	-	-	-	-
REVENUE										
PRODUCT REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
NON PRODUCT REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
TOTAL REVENUE ($K)	-	-	-	-	-	-	-	-	-	-
AVG UNIT COST ($)	-	-	-	-	-	-	-	-	-	-
TOTAL DIRECT COST ($K)	-	-	-	-	-	-	-	-	-	-
DIRECT MARGIN ($K)	-	-	-	-	-	-	-	-	-	-
LEAKAGE ($K)	-	-	-	-	-	-	-	-	-	-
GROSS MARGIN ($K)	-	-	-	-	-	-	-	-	-	-
OPEX										
R&D										
MANPOWER COSTS ($K)	129.66	9.66	-	-	-	-	-	-	-	-
MASKS & HARDWARE ($K)	7.25	0.25	-	-	-	-	-	-	-	-
OTHER R&D EXPENSES ($K)	7.50	-	-	-	-	-	-	-	-	-
TOTAL R&D ($K)	144.41	9.91	-	-	-	-	-	-	-	-
S&M ($K)	-	-	-	-	-	-	-	-	-	-
G&A ($K)	-	-	-	-	-	-	-	-	-	-
TOTAL OPEX ($K)	144.41	9.91	-	-	-	-	-	-	-	-
OPERATING PROFIT (LOSS) ($K)	(144.41)	(9.91)	-	-	-	-	-	-	-	-
DIRECT MARGIN (%)	-	-	-	-	-	-	-	-	-	-
GROSS MARGIN (%)	-	-	-	-	-	-	-	-	-	-



QFPS REVENUE MODEL PARAMETERS				
NPP OR PM MODEL	NPP MODEL1			
NPP	NPP MODEL2			
PARAMETERS	M1 CATA	M1 CATB	M2 CATA	M2 CATB
ACTIVE-QFPS LATENCY	0	0	0	0
ACTIVE-QFPS YIELD	0%	0%	0%	0%
QFPS-NDW LATENCY	0	0	0	0
QFPS-NDW YIELD	0%	0%	0%	0%
UNITS / WIN	0.0	0.0	0.0	0.0
QUARTERS / WIN	0	0	0	0
UNITS / QTR	0	0	0	0
% OTHER	0%	0%	0%	0%
1ST QACT-PR4 LATENCY	0	0	0	0
CATA/CATB UNITS RATIO	0.00		0.00	
CATA/CATB ASP RATIO	0.00		0.00	
/ ASP RATIO	0.00			

DEVELOPMENT STRATEGY OVERVIEW

The Programmable Systems Division's (PSD's) Validation group will manage this project and ensure that the validation project meets CY standards as per the System New Product Development process (001-55229), SVS requirements spec (001-83369) and PSVP requirements spec (001-83368).

IP PLAN

Not applicable

TEAM CONSTRUCTION

The SF project team comprises of the following members:

Role	Initials	Job Title	Location
Project manager	VJYA	Systems Engineer Principal	INDIA
Technical Lead	DEPK	Software Engineer Sr	INDIA
Systems Engineer	ANTV	Systems Engineer	INDIA
Hardware Engineer	SRVS	Systems Engineer Sr	INDIA
Systems Engineer	ANKU	Systems Engineer	INDIA
Systems Engineer	THLK	Systems Engineer	INDIA

DEVELOPMENT RISK

The following are the risks identified:

a) I2C testing may be in critical path for ES100
b) Capsense validation board SNR Quality
c) Availability of PSoC creator components – CSD, SmartSense and I2C
d) TO6 Si arrival co-incides with SF ES10 or ES100 - may result in shortage of equipments.

To address risk (a), I2C testing shall be automated. To address risk (b), Capsense layout best practices spec will be followed while designing the CapSense validation board. To address risk (c) Component team has committed the schedule (BJBU#118). To address risk (d), the test equipment will be shared between TO6 project and SF project and this may prevent pull in of dates on each of the individual silicon.

DESIGN / CUSTOMER INTERACTIONS

The SF validation team is not involved in customer interactions. Feedback on requirements is obtained from CapSense applications, design and marketing teams. The feedback from design team is received from the chip lead and the feedback from applications team is received from applications manager. The EROS for SF validation project has been reviewed by design, marketing and applications teams.

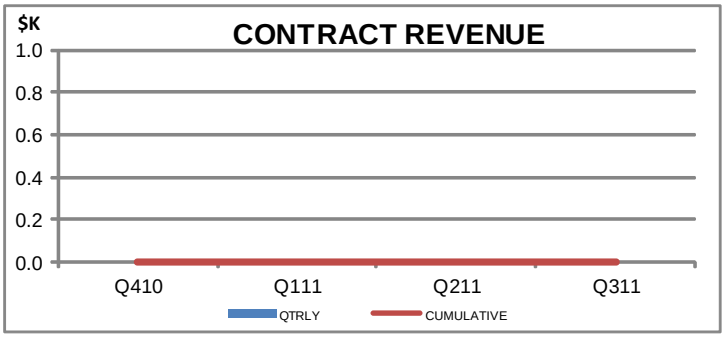
ALIGNMENT WITH LONG TERM STRATEGY

The System Validation Suite (SVS) will be reused across all the devices in the CapSense controller and PSoC4 product families. The hardware platform consisting of PCVP, validation boards and third party test equipments such as Telos will be reused for validation across all the devices in the product family after device specific modifications to the validation boards. The validation scripts and the validation firmware will be reused after device specific modifications. The test execution will be automated for the entire test suite to reduce the test execution time.

SCHEDULE AND MANPOWER																
MS	OS	CS			PM	SYS	HW	APPS	MKT OTHER	FW SW TEST	HC	COST ($K)	ITEM	MW	$K	%
	WW	WW	QTR	CT	MW											
PPP	1312	1312	Q113										PM/TL	41	62	40
NPP1	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	FW/SW Design	-	-	-
NPP2	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	HW Design	-	-	-
NPP	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	Systems Design	51	77	50
TC	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	Test	-	-	-
FPGA	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	Marketing	-	-	-
PR1	1321	1321	Q213	9	21	0.3	2.1	-	-	-	-	2.3	32	Apps	-	-	-
PR2	1336	1336	Q313	15	35	0.3	2.1	-	-	-	-	2.3	53	Other	-	-	-
CFR	1336	1336	Q313	-	-	-	-	-	-	-	-	-	-	Hardware (WPP)	N/A	-	-
PR3	1342	1342	Q413	2	5	0.3	2.1	-	-	-	-	2.3	7	Hardware	N/A	8	5
TO	1340	1340	Q413	4	9	0.3	2.1	-	-	-	-	2.3	14	Masks	N/A	-	-
1ST SI	1340	1340	Q413	-	-	-	-	-	-	-	-	-	-	Other	N/A	8	5
ES10	1342	1342	Q413	-	-	-	-	-	-	-	-	-	-	TOTAL	93	154	100
CR	1342	1342	Q413	-	-	-	-	-	-	-	-	-	-				
CQ	1342	1342	Q413	-	-	-	-	-	-	-	-	-	-	MASK CONTRACT			
TO2	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	Cost Center		PSD-DC	
TO3	1312	1312	Q113	-	-	-	-	-	-	-	-	-	-	Technology		Pick One	
ES100	1350	1350	Q413	8	16	0.3	1.8	-	-	-	-	2.0	24	Mask Set Cost ($K)			
PR4	1405	1405	Q114	7	6	0.3	0.6	-	-	-	-	0.9	10	Planned Mask Ratio			
FGI1K	1405	1405	Q114											* For Total Mask Revenue: Refer to the Design Financials Contract			
FQ	1405	1405	Q114	-	-	-	-	-	-	-	-	-	-				
PR5	1405	1405	Q114	-	-	-	-	-	-	-	-	-	-				
PROD10K	1405	1405	Q114														
M0	1405	1405	Q114														
M1	1405	1405	Q114														

DEVELOPMENT CONTRACT (CREATED AND LOCKED WHEN PROJECT IS LAUNCHED USING NPP TOOLKIT v6.26 OR GREATER)																
GROUP	MWs	WKLY RATE	NPP MS PAYMENTS ($K)								IP MS PAYMENTS ($K)				TOT ($K)
			PR1	PR2	PR3	TO	MASK	ES100	PR4	PR5	IPS1	IPS2	IPS3	IPS4	
Remaining Cost Centers															
TOTALS	0	0.00	0.0	0.0	0.0	0.0	*	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

IP DEVELOPMENT COMPLEXITY WEIGHT				
IP TYPE	COMP	# NEW	# RE-USED	IP WEIGHT
ANALOG	LOW			
	HIGH			
LOGIC	LOW			
	HIGH			
MEMORY	LOW			
	HIGH			
TOOLKIT	LOW			
	HIGH			
IO	LOW			
	HIGH			
	TOTALS			



UNIT COST BREAKDOWN			2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
FRONT END		K-UNITS/WK	0	0	0	0	0	0	0	0	0	0
		WAFERS/WK	-	-	-	-	-	-	-	-	-	-
		%INT	100	100	100	100	100	100	100	100	100	100
		INT FAB COST ($/wfr)	-	-	-	-	-	-	-	-	-	-
		EXT FAB COST ($/wfr)	-	-	-	-	-	-	-	-	-	-
		BL FAB COST($/wfr)	-	-	-	-	-	-	-	-	-	-
		LASER TIME (min/wfr)	-	-	-	-	-	-	-	-	-	-
		WLBI TIME (min/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 1 TIME (min/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 1 COST ($/min)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 1 COST ($/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 2 TIME (min/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 2 COST ($/min)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 2 COST ($/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 3 TIME (min/wfr)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 3 COST ($/min)	-	-	-	-	-	-	-	-	-	-
		PLATFORM 3 COST ($/wfr)	-	-	-	-	-	-	-	-	-	-
		TOT FE COST($/wfr)	-	-	-	-	-	-	-	-	-	-
		DEF DEN (def/sq in)	-	-	-	-	-	-	-	-	-	-
		SYS YIELD (%)	-	-	-	-	-	-	-	-	-	-
		SORT YIELD (%)	-	-	-	-	-	-	-	-	-	-
		NDPW	-	-	-	-	-	-	-	-	-	-
BACK END	PKG MIX		25	25	25	25	25	25	25	25	25	25
			25	25	25	25	25	25	25	25	25	25
			25	25	25	25	25	25	25	25	25	25
			25	25	25	25	25	25	25	25	25	25
		MIXED ASSY YIELD (%)	-	-	-	-	-	-	-	-	-	-
		MIXED TEST YIELD (%)	-	-	-	-	-	-	-	-	-	-
		MIXED FINISH YIELD (%)	-	-	-	-	-	-	-	-	-	-
		MIXED ASSY COST ($)	-	-	-	-	-	-	-	-	-	-
		MIXED TEST COST ($)	-	-	-	-	-	-	-	-	-	-
		MIXED FINISH COST ($)	-	-	-	-	-	-	-	-	-	-
YIELDED UNIT COST ($)		DIE	-	-	-	-	-	-	-	-	-	-
		ASSY	-	-	-	-	-	-	-	-	-	-
		TEST	-	-	-	-	-	-	-	-	-	-
		BI	-	-	-	-	-	-	-	-	-	-
		FINISH	-	-	-	-	-	-	-	-	-	-
		SHIP	-	-	-	-	-	-	-	-	-	-
		TOTAL	-	-	-	-	-	-	-	-	-	-
MFG LKG (% OF REV)		MFG VARIABLE	10	10	10	10	10	10	10	10	10	10
		MFG FIXED	-	-	-	-	-	-	-	-	-	-
		ROYALTY (NEW)	-	-	-	-	-	-	-	-	-	-
		ASP ($)	-	-	-	-	-	-	-	-	-	-
		DIRECT MARGIN (%)	-	-	-	-	-	-	-	-	-	-
		DM TO GM LKG (%)	1	1	1	1	1	1	1	1	1	1
		GROSS MARGIN (%)	-	-	-	-	-	-	-	-	-	-

FE DATA SOURCE
CORPORATE
001-42139 *S

BE DATA SOURCE
MANUAL

BE YIELDS AND COSTS PER PKG (PRE PR5 | POST PR5)								
ASSY YIELD (%)								
TEST YIELD (%)								
FINISH YIELD (%)								
ASSY COST ($)								
TEST INSERTS								
TEST TIME (s)								
TEST COST ($/s)								
FINISH COST ($)								
QA TEST TEMPS								
CLASS TEST TEMPS								

TAPEOUT DATE	1340
WORST CASE PKG	
NEW YIELD MODEL?	

MTL LYRS	-
MSK LYRS	-
NEW TECH	

GDPW	-
DS (mm^2)	-

NPDIS PROJECT	STREET FIGHTER SVS	FAB YLD ENG		CHIP LEAD	DEPK
MFG PART #	STREET FIGHTER SVS	PM	VJYA	PE LEAD	
PRODUCT LINE	PSD				

		NPP (PLAN)		PR3 (REVISED PLAN)		ACTUAL		MIN/MAX REQUIREMENTS		
	FAB MANUFACTURING	**PR4**	**PR5**	**PR4**	**PR5**	**PR4**	**PR5**	**PASS**	**PR4**	**PR5**
GENERAL INFO	TECHNOLOGY									
	FAB LOCATION(S)									
	SORT PLATFORM(S)									
	SORT LOCATION(S)									
	GROSS DIE PER WAFER (GDPW)									
	PROBE CARD TECHNOLOGY AND PARALLELISM									
FAB REQUIREMENTS	FOCUS AND EXPOSURE MATRIX PROCESS WINDOW MET (YES/NO)									
	PROCESS CORNERS REQUIREMENTS MET (YES/NO)									
	FIX TO ATTEMPT RATIO (%)									
	BIN SPLIT (% PRIME BIN)									
	NUMBER OF SORTS (NOT INCLUDING WLBI)									
	PRODUCTION CTAS PROGRAM ONLINE (YES / NO)									
	WIP LIMITS (WAFERS)									
	LINE YIELD (%) | NUMBER OF WAFERS									
	SORT YIELD (%) | NUMBER OF WAFERS								1LOT w/ 6 WAFERS	3 LOTS w/ 12 WFRS EACH
	TOTAL SORT TIME (MINS PER WAFER)								<250 MIN	
	SORT TEMP(S)									
	POST SORT 1 YIELD LOSS (%)								≤5%	≤2.5%
	AUTO RETEST OVERTURN (% OF TOTAL YIELD)								2%	1%
	MAX. POST LASER LOSS (% OF TOTAL YIELD)								6%	4%
	WAFER LEVEL BURNIN (MINUTES PER WAFER)								180 MIN	120 MIN
	STATISTICAL BIN LIMITS FOR ALL PASS/FAIL BINS (SBL)								N/A	IN PLACE
	CUSTOM SPC TARGETS (THROUGH E-TEST)								N/A	0
	B/E MANUFACTURING									
GENERAL INFO	LEAD COUNT AND PACKAGE(S)									
	BACKGRIND LOCATION / THICKNESS									
	ASSEMBLY LOCATION									
	TEST LOCATION									
	LOW COST TEST PLATFORM									
	OTHER TEST PLATFORM									
ATF EQUIP INFO	AUTOLINE									
	LINE NUMBER | PACKAGE									
	MAX UPH TT + CP (SECS) | TEMP									
	AUTOLINE MAX UPH (UNITS)									
	CONVENTIONAL HANDLER									
	HANDLER TYPE | PARALLELISM									
	MAX UPH TT + CP (SECS) | TEMP									
	HANDLER MAX UPH (UNITS)									
YIELDS	ASSEMBLY YIELD (%)									99.00%
	CLASS TEST YIELD (%)									
	FINISH YIELD (%)									98.50%
	ASSEMBLY, TEST, FINISH YIELD (%)									
	FQA (%)									0 REJECTS
	MRB RATE (%)								<10%	<5%
BE DETAILS	NUMBER OF INSERTS								3	
	PRODUCTION CTAC PROGRAM ONLINE (YES/NO)									
	BIN SPLIT (% PRIME BIN)								≥50%	≥50%
	BURNIN DURATION (HOURS)									

Manufacturing is done by contract manufacturer.