Simple CPU Design (Vivado HLS example)

Instruction set / Instruction encoding

FINISH

Finish the program. Use at the end of your assembly program.

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0 0 0

WR_IMM

Write immediate

Register[DST]= VALUE

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	VALUE				DST	0 0 1

Example: WR_IMM 0x3, 0x012F

Set Register3 to 0x012F

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	0000 0001 0010 1111				0011	0 0 1

LOAD

Load from data memory

Register[DST] = MEMORY[Register[SRC0]]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	SRC0	DST	0 1 0

Example: LOAD 0x3, 0x5

R3 = MEMORY[R5]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0101	0011	0 1 0

STORE

Store data to memory

MEMORY[REGISTER[SRC0]] = REGISTER[SRC1]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	SRC1	SRC0	0 1 1

Example: STORE 0x3, 0x5

MEMORY[R3] = R5

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0101	0011	0 1 1

BEQ

Branch equal

Go to the instruction at NEW_PC if Register[SRC0] == Register[SRC1]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{2'b0, NEW_PC}			SRC1	SRC0	1 0 0

Example: BEQ 0x3, 0x5, 0x3AB

Go to the instruction at 0x3AB if Register3 == Register5

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0101	0011	1 0 0

BNE

Branch not equal

Go to the instruction at NEW_PC if Register[SRC0] != Register[SRC1]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{2'b0, NEW_PC}			SRC1	SRC0	1 0 1

Example: BEQ 0x3, 0x5, 0x3AB

Go to the instruction at 0x3AB if Register3 != Register5

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0101	0011	1 0 1

ADD

Add registers

REGISTER[DST] = REGISTER[SRC0] + REGISTER[SRC1]

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	SRC1	SRC0	DST	1 1 0

Example: ADD 0x2, 0x3, 0x5

R2 = R3 + R5

9 bits	4 bits	4 bits	4 bits	4 bits	4 bits	3 bits
{9 {1'b0}}	{4 {1'b0}}	{4 {1'b0}}	0101	0011	0010	1 1 0