

Lab 4 - Combinational Circuits and Code Converters

Exp.1: Design, construct, and test two combinational logic circuits. The circuits are to be constructed with NAND gates.

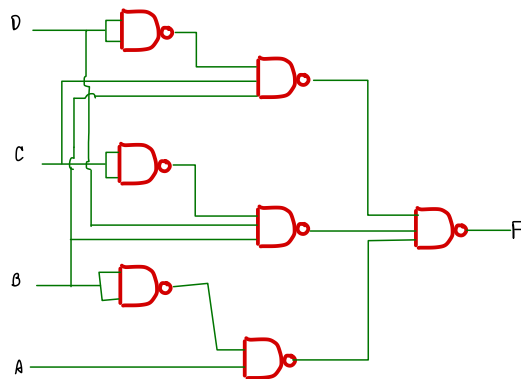
1.1 Design a combinational circuit with four inputs— A, B, C, and D —and one output, F. F is to be equal to 1 when A = 1, provided that B = 0, or when B = 1, provided that either C or D (not both) is also equal to 1. Otherwise, the output is to be equal to 0.

- Fill in the truth table.
- Simplify the output function.
- Draw the logic diagram of the circuit, using NAND gates.
- Construct the circuit and test it in Proteus program for proper operation by verifying the given conditions. Show the simulation result circuit to the TA.

AB\CD	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	0	1	0	1
10	1	1	1	1

$$= A\bar{B} + B\bar{C}D + B\bar{C}\bar{D}$$

$$= \overline{(\overline{A\bar{B}})(\overline{B\bar{C}D})(\overline{B\bar{C}\bar{D}})}$$



A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

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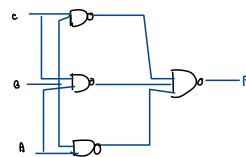
1.2 A majority logic is a digital circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. Design and test a three-input majority circuit using NAND gates. Construct the circuit and test it in Proteus program for proper operation by verifying the given conditions. Show the simulation result to the TA.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$AC + BC + AB$$

$$= \overline{(AC) (BC) (AB)}$$



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Exp.2: Design and construct seven-segment display

2.1 Consider the BCD to 7-segment converter truth table. Determine the Boolean functions for each segment. Simplify the functions using *Karnaugh* maps. Construct the simplified circuit and simulate it. Show the result to the TA.

Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

DC\BA	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11				
10	1	1		

F_a

$$B + AC + \bar{A}\bar{C} + D$$

DC\BA	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11				
10	1	1		

F_b

$$\bar{C} + \bar{B}\bar{A} + BA$$

DC\BA	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11				
10	1	1		

F_c

$$\bar{B} + A + C$$

DC\BA	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11				
10	1	1		

F_d

$$\bar{A}\bar{C} + C\bar{B}A + \bar{B}\bar{C} + \bar{B}\bar{A} + D$$

DC\BA	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11				
10	1	0		

F_e

$$\bar{A}\bar{C} + \bar{B}\bar{A}$$

DC\BA	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11				
10	1	1		

F_f

$$\bar{B}\bar{A} + \bar{B}\bar{C} + D + \bar{A}\bar{B}\bar{C}$$

DC\BA	$\bar{b}\bar{a}$ 00	$\bar{b}a$ 01	$b\bar{a}$ 11	ba 10
$\bar{b}\bar{a}$ 00	0	0	1	1
$\bar{b}a$ 01	1	1	0	1
$b\bar{a}$ 11				
ba 10	1	1		

$$F_g = \bar{b}\bar{c} + b\bar{c} + b\bar{a} + D$$

2.2 Figure 1 shows the connections necessary between the decoder and the display. The 7447 IC is a BCD-to-seven-segment decoder/driver that has four inputs for the BCD digit. Input D is the most significant and input A the least significant. The four-bit BCD digit is converted to a seven-segment code with outputs a through g. The outputs of the 7447 are applied to the inputs of the 7-segment common anode display.

Construct the circuit shown in Fig. 1. Apply the four-bit BCD digits through four switches, and observe the decimal display from 0 to 9. Inputs 1010 through 1111 have no meaning in BCD. These values may cause a meaningless pattern to be displayed. Observe and record the output patterns of the six unused input combinations.

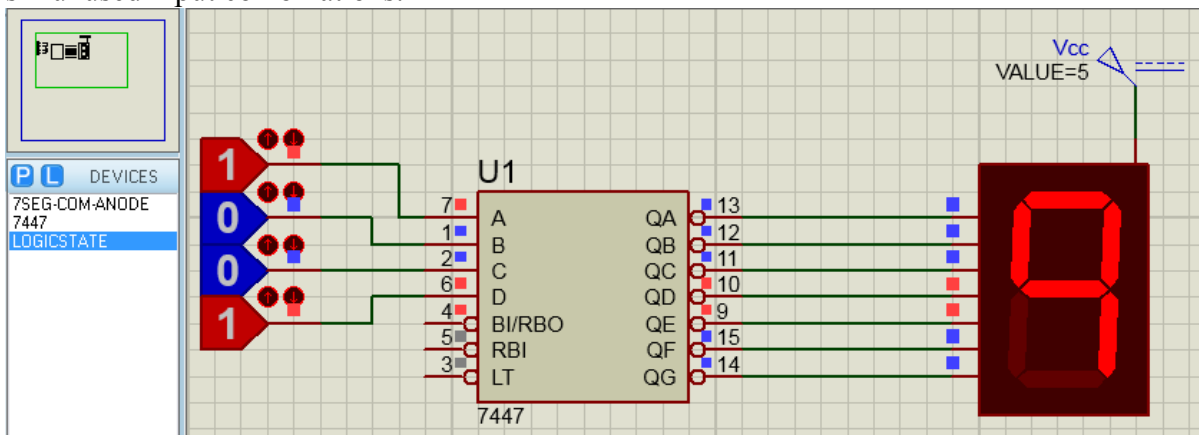
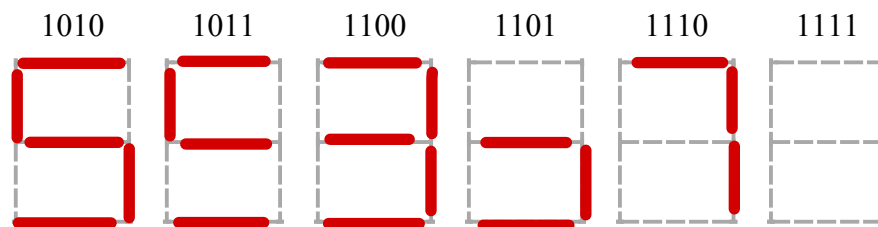


Figure 1



The diagram illustrates an 8x3 Priority Encoder. On the left, eight input lines are labeled D_7 through D_0 , with D_7 at the top marked "Highest Priority" and D_0 at the bottom marked "Lowest Priority". These inputs feed into a light blue rectangular block labeled "8 x 3 Priority Encoder". Three output lines, labeled Q_2 , Q_1 , and Q_0 , emerge from the right side of the block under the heading "Output".

To the right of the diagram is the truth table for the 8x3 Priority Encoder, which shows the relationship between the 8 inputs (D_7 to D_0) and the 3 outputs (Q_2 , Q_1 , Q_0). The table is organized with inputs as columns and outputs as rows. 'X' denotes a "Don't care" condition.

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = Don't care

(Hint: Notice that Q_2 is “0” when D_7 - D_4 are all “0s”, otherwise Q_2 is “1”. For Q_0 and Q_1 , look for significant inputs D_7 - D_0 .)

