| V$_{x1}$(volt) | V$_{x2}$(volt) | V$_y$(volt) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 5 | 5 |
| 5 | 0 | 5 |
| 5 | 5 | 5 |

Figure 10

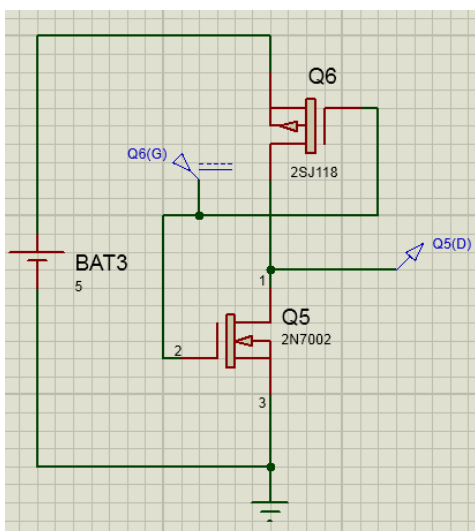2. Specify the logic gate for circuit 6-10

6 ) NOT gate

7 ) NOR gate

8 ) NAND gate

9 ) AND gate

10) OR gate

## CMOS Logic gates

1. Implement PMOS logic gate circuits in Figure 11-13, change the values of V$_{x1}$ and V$_{x2\ according}$ to the table and observe the output V$_f$.



| V$_{x1}$ (volt) | V$_f$(volt) |
|---|---|
| 0 | 5 |
| 5 | 0 |

Figure 11