6207050106 6 ลิลัคณี อิ่มใจ
6207050106 4 อรวิภา คูเจริญไพศาล

Lab 1 - The basic elements of digital logic circuits

Logic circuits are built with transistors. The most popular type of transistor for implementing a simple switch is the metal oxide semiconductor field-effect transistor (MOSFET). There are two different types of MOSFETs, known as n-channel (NMOS) and p-channel (PMOS).

NMOS Logic gates

1. Implement NMOS logic gate circuits in Figure 1-5, change the values of V_{x1} and $V_{x2\ according}$ to the table and observe the output V_f.

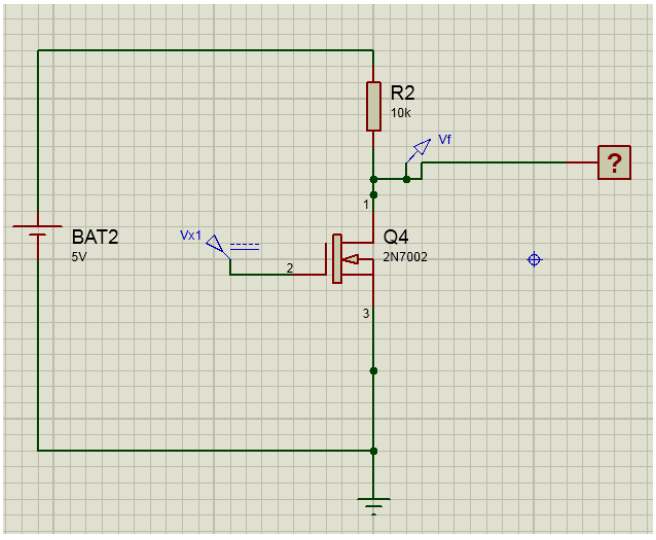

Figure 1

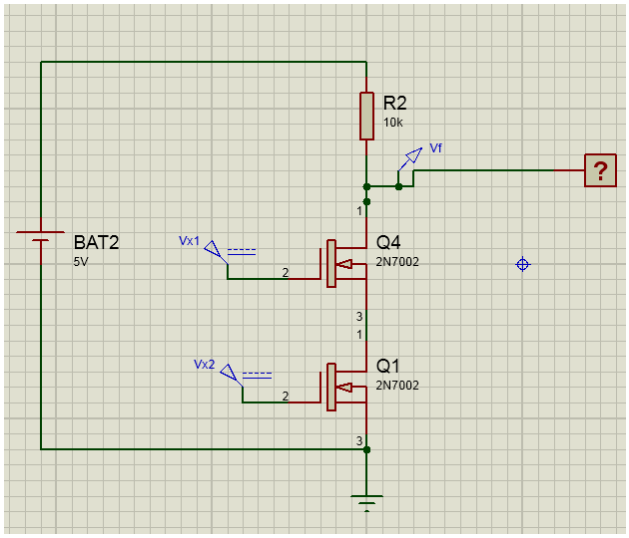

Figure 2

V_{x1} (volt)	V_f(volt)
0	5
5	0

V_{x1} (volt)	V_{x2}(volt)	V_f(volt)
0	0	5
0	5	5
5	0	5
5	5	0

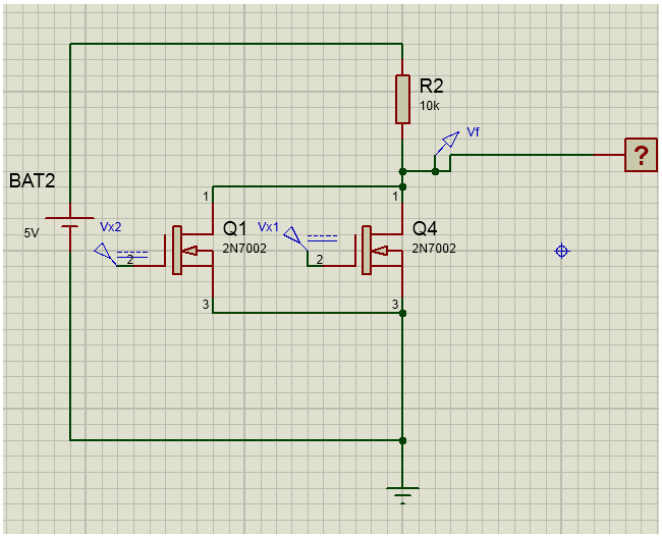

Figure 3

V_{x1} (volt)	V_{x2}(volt)	V_f(volt)
0	0	5
0	5	0
5	0	0
5	5	0

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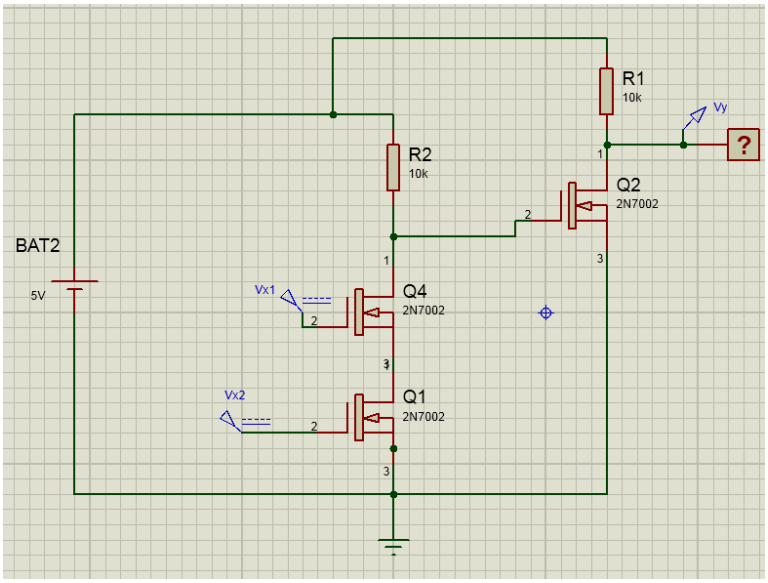

Figure 4

V_{x1}(volt)	V_{x2}(volt)	V_y(volt)
0	0	0
0	5	0
5	0	0
5	5	5

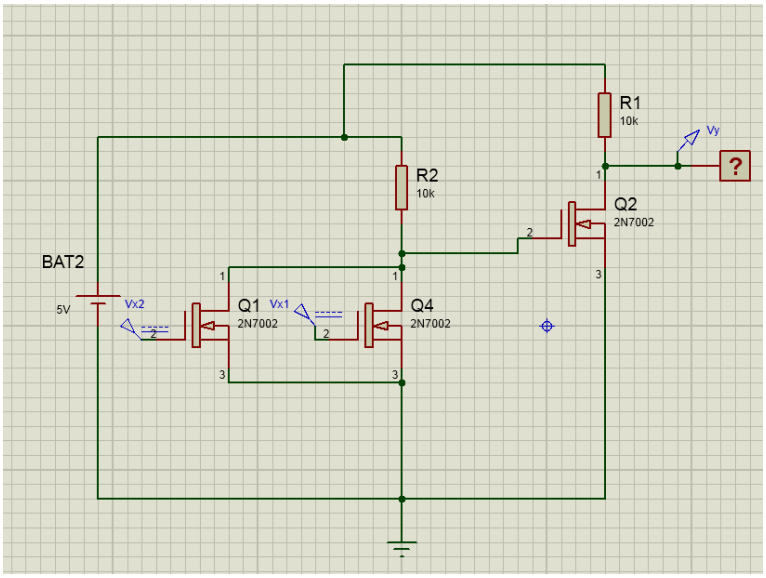

Figure 5

V_{x1} (volt)	V_{x2}(volt)	V_y(volt)
0	0	0
0	5	5
5	0	5
5	5	5

2. Specify the logic gate for circuit 1-5

1) NOT gate

2) NAND gate

3) NOR gate

4) AND gate

5) OR gate

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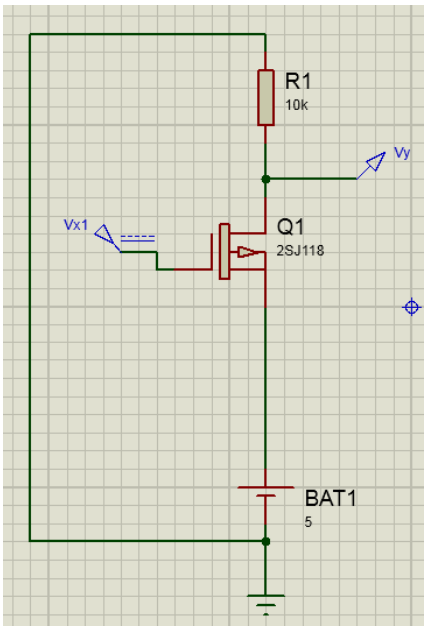
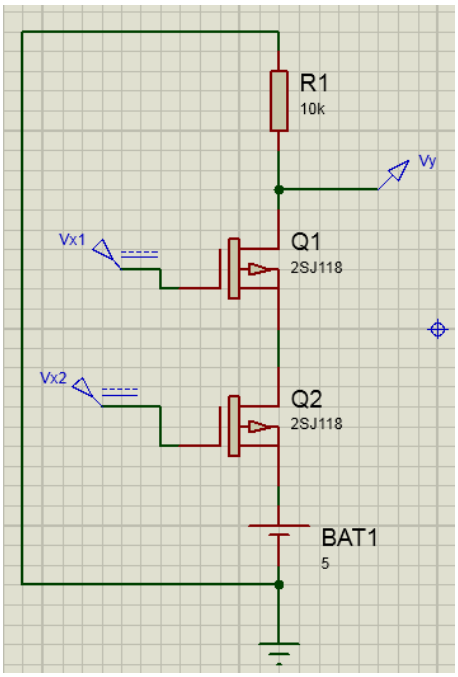
PMOS Logic gates

1. Implement PMOS logic gate circuits in Figure 6-10, change the values of V_{x1} and V_{x2} according to the table and observe the output V_f.



V_{x1}(volt)	V_y(volt)
0	5
5	0

Figure. 6



V_{x1}(volt)	V_{x2}(volt)	V_y(volt)
0	0	5
0	5	0
5	0	0
5	5	0

Figure 7

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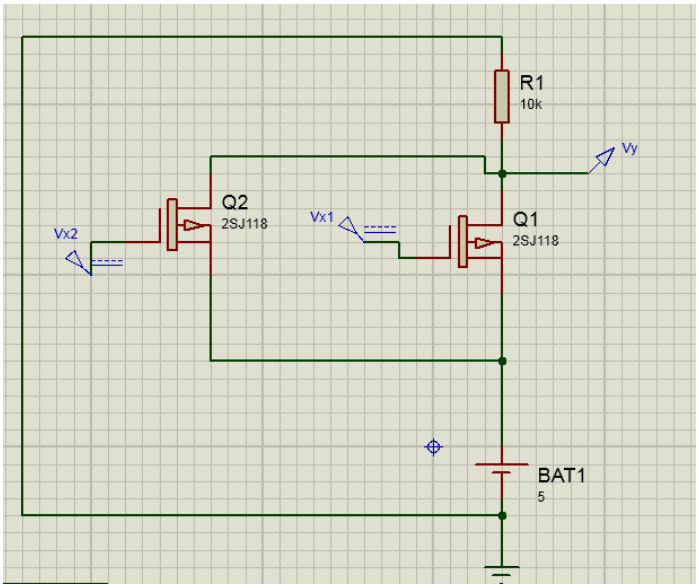
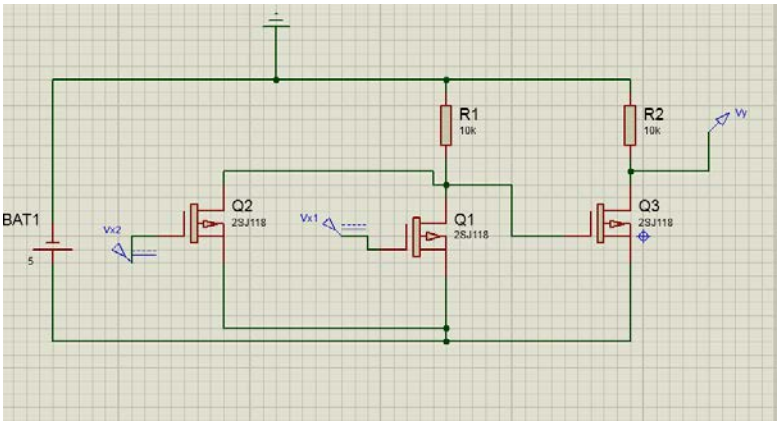


V_{x1} (volt)	V_{x2}(volt)	V_y(volt)
0	0	5
0	5	5
5	0	5
5	5	0

Figure 8



V_{x1} (volt)	V_{x2}(volt)	V_y(volt)
0	0	0
0	5	0
5	0	0
5	5	5

Figure 9

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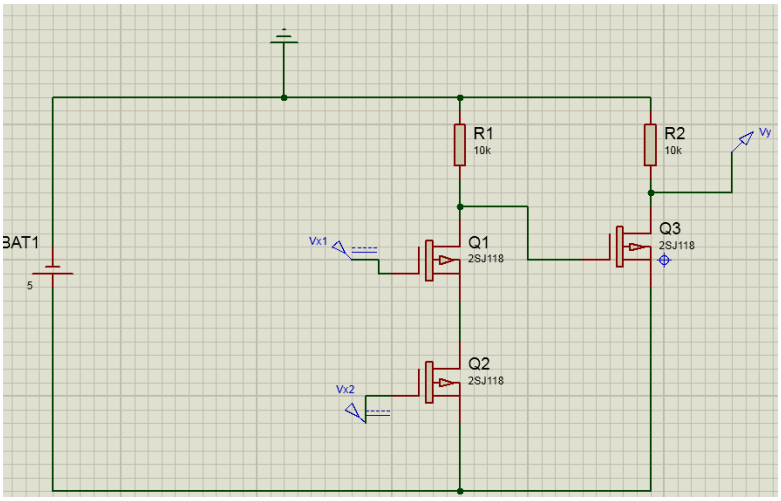


V_{x1}(volt)	V_{x2}(volt)	V_y(volt)
0	0	0
0	5	5
5	0	5
5	5	5

Figure 10

2. Specify the logic gate for circuit 6-10

6) NOT gate

7) NOR gate

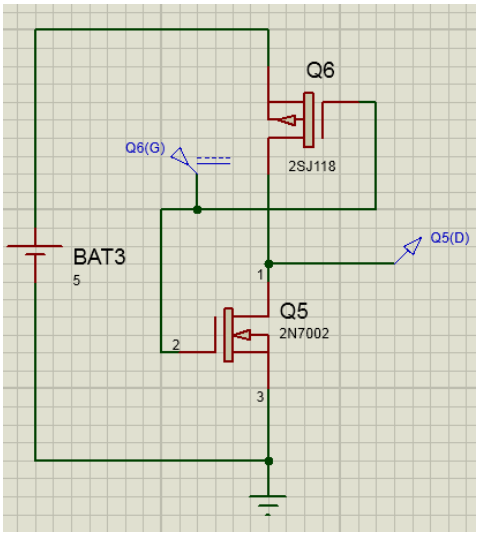
8) NAND gate

9) AND gate

10) OR gate

CMOS Logic gates

1. Implement PMOS logic gate circuits in Figure 11-13, change the values of V_{x1} and V_{x2} according to the table and observe the output V_f.



V_{x1} (volt)	V_f(volt)
0	0
5	5

Figure 11

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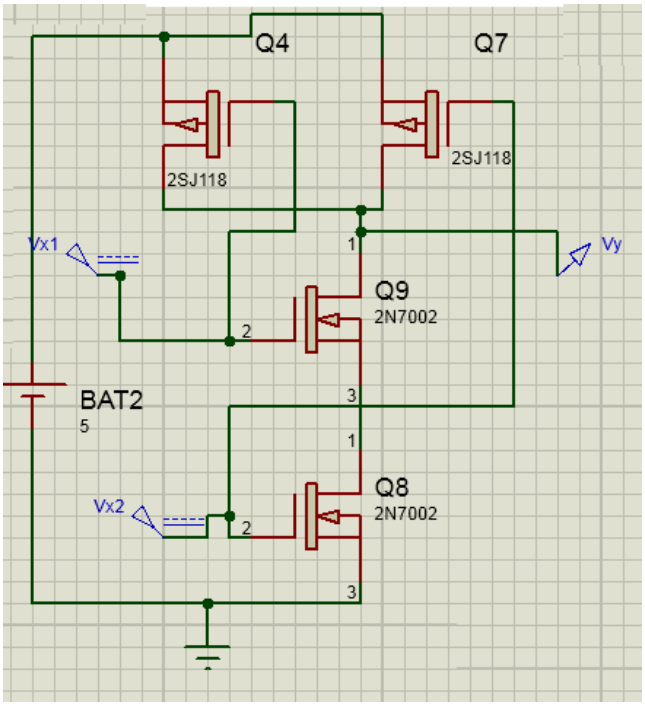
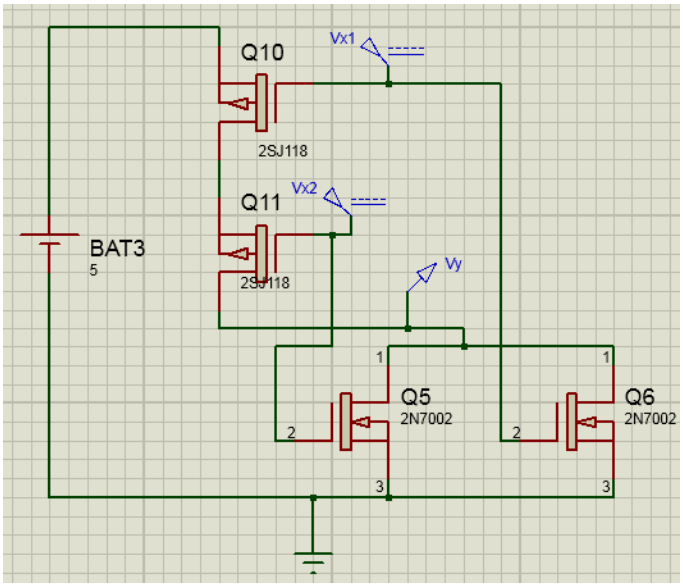


V_{x1}(volt)	V_{x2}(volt)	V_y(volt)
0	0	5
0	5	5
5	0	5
5	5	0

Figure 12



V_{x1} (volt)	V_{x2}(volt)	V_y(volt)
0	0	5
0	5	0
5	0	0
5	5	0

Figure 13

2. Specify the logic gate for circuit 11-13

11) NOT gate

12) NAND gate

13) NOR gate