Lab 3 - Binary and BCD numbers, digital logic gates, and simplification of Boolean functions

AX-1 digital logic trainer

A digital logic trainer contains 8 LED lamps, a 7-segment BCD, 8 toggle switches, 2 pulsers (P0, P1), a variable clock, a power supply, and IC socket strips.

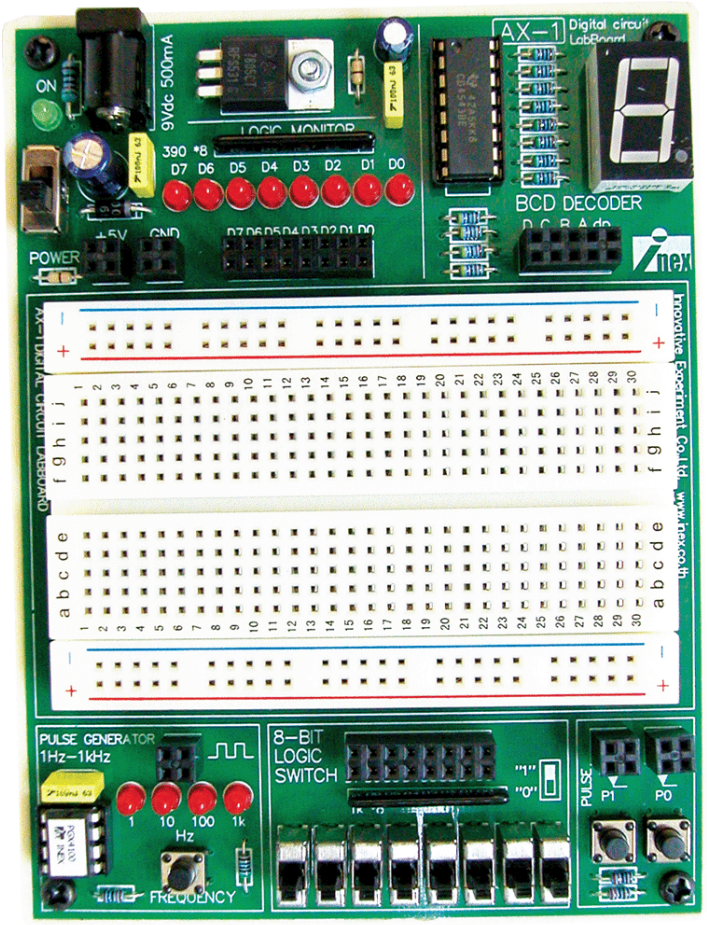
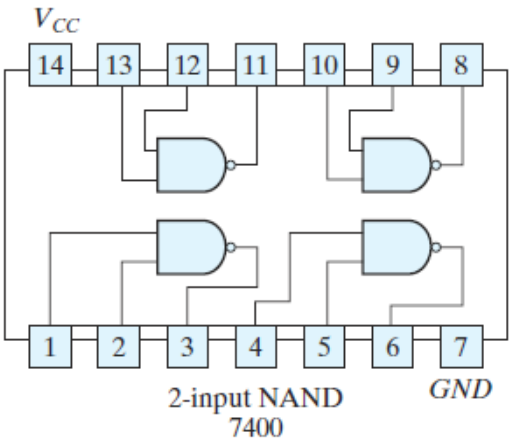
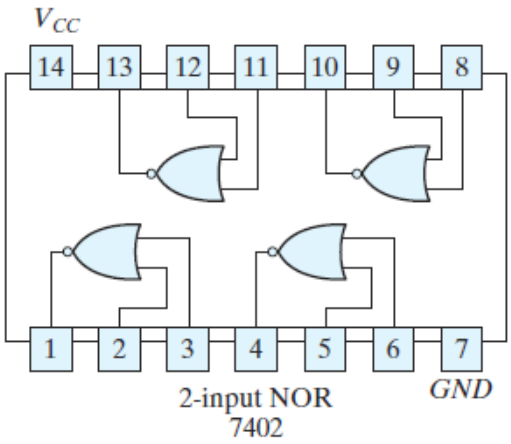


Fig. 1 AX-1 digital logic trainer.

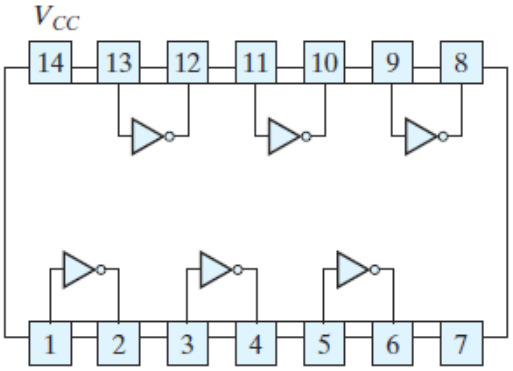
The integrated circuits to be used in the experiments can be classified as small-scale integration (SSI) or medium-scale integration (MSI) circuits. SSI circuits contain individual gates or flip-flops, and MSI circuits perform specific digital functions. The eight SSI gate ICs needed for the experiments—two-input NAND, NOR, AND, OR, and XOR gates, inverters, and three-input and four-input NAND gates—are shown in Fig. 2. The pin assignments for the gates are indicated in the diagram. The pins are numbered from 1 to 14. Pin number 14 is marked *Vcc*, and pin number 7 is marked *GND* (ground). These are the supply terminals, which must be connected to a power supply of 5 V for proper operation of the circuit. Each IC is recognized by its identification number; for example, the two-input NAND gates are found inside the IC whose number is 7400.



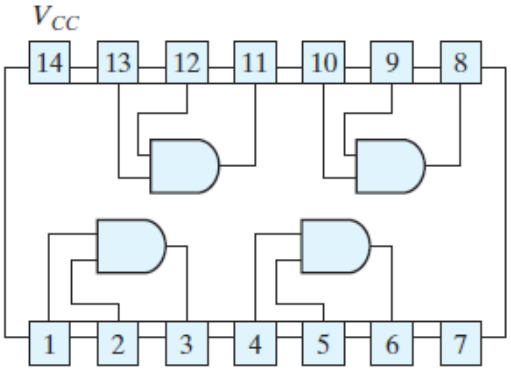
2-input NAND
7400



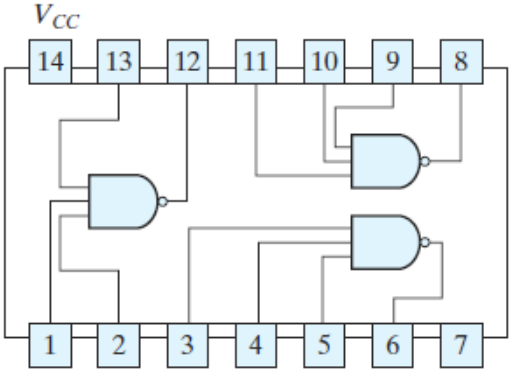
2-input NOR
7402



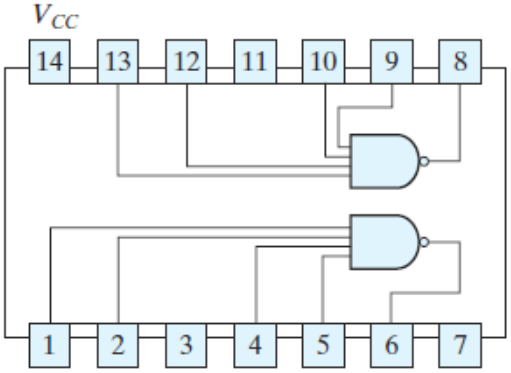
Inverters
7404



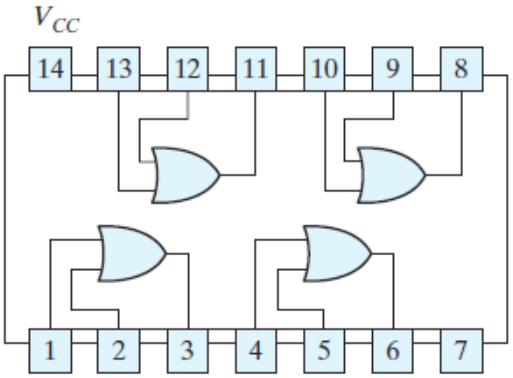
2-input AND
7408



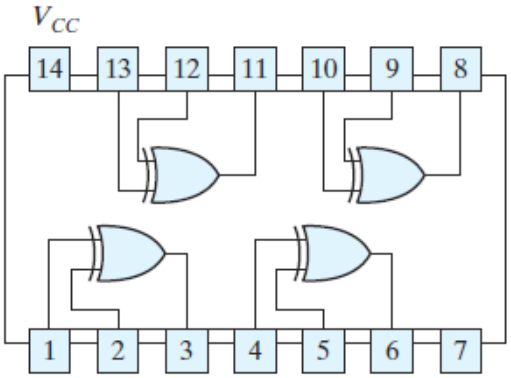
3-input NAND
7410



4-input NAND
7420



2-input OR
7432



2-input XOR
7486

Fig. 2 Digital gates in IC packages with identification numbers and pin assignments

The ripple counter IC, type 7493, is used in Experiment 1 and in subsequent experiments to generate a sequence of binary numbers for verifying the operation of combinational circuits. The information about the 7493 IC that is found in a data book is shown in Figs. 3(a) and (b). Part (a) shows the physical layout of the IC, together with its 14-pin assignment to signal names. Some of the pins are not used by the circuit and are marked as *NC* (no connection). The IC is inserted into a socket, and wires are connected to the various pins through the socket terminals. Part(b) shows schematic diagrams. The IC number (here, 7493) is written inside the block. All input terminals are placed on the left of the block and all output terminals on the right. The letter symbols of the signals, such as *A, R1*, and *QA*, are written inside the block, and the corresponding pin numbers, such as 14, 2, and 12, are written along the external lines. *VCC*, and *GND* are the power terminals connected to pins 5 and 10.

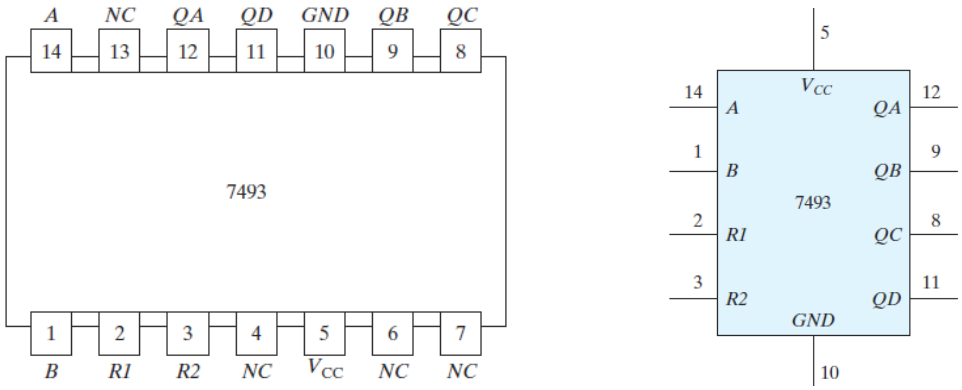


Fig. 3 (a) Physical layout (NC: no connection); (b) Schematic diagram.

The 7493 IC can operate as a three-bit counter using input *B* and flip-flops *QB, QC*, and *QD*. It can operate as a four-bit counter using input *A* if output *QA* is connected to input *B*. Therefore, to operate the circuit as a four-bit counter, it is necessary to have an external connection between pin 12 and pin 1. The reset inputs, *R1* and *R2*, at pins 2 and 3, respectively, must be grounded. Pins 5 and 10 must be connected to a 5-V power supply. The input pulses must be applied to input *A* at pin 14, and the four flip-flop outputs of the counter are taken from *QA, QB, QC*, and *QD* at pins 12, 9, 8, and 11, respectively, with *QA* being the least significant bit.

Experiment 1

Objective: This experiment demonstrates the count sequence of binary numbers and the binary coded decimal (BCD) representation. It serves as an introduction to the breadboard used in the laboratory.
2.1 Build a binary counter (Figure 4) and a BCD counter (Figure 5) in Proteus. Simulate them and explain the behavior of the circuits.

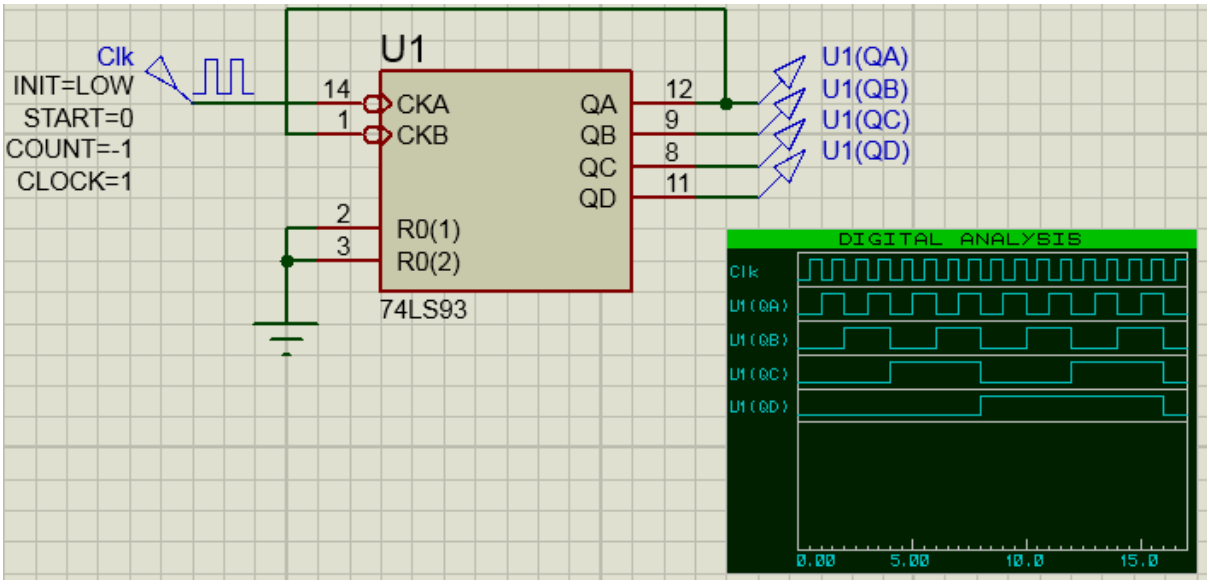
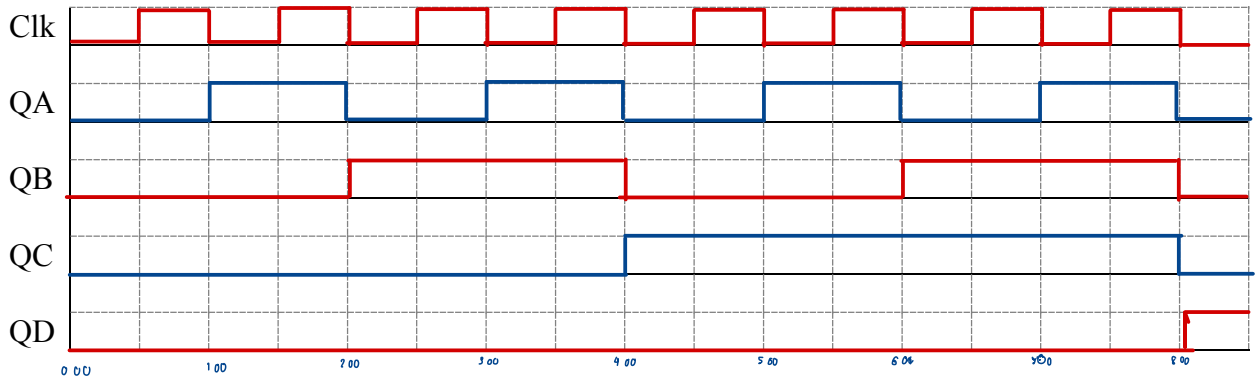


Figure 4

Sketch the output patterns: -

a. Binary Counter Circuit using 74LS93



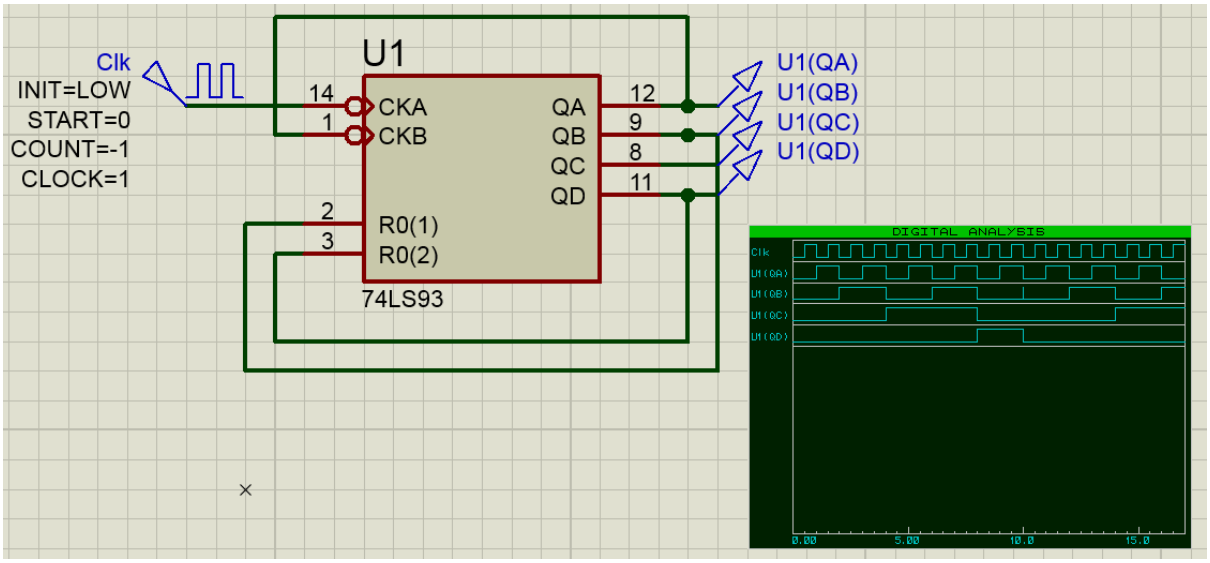
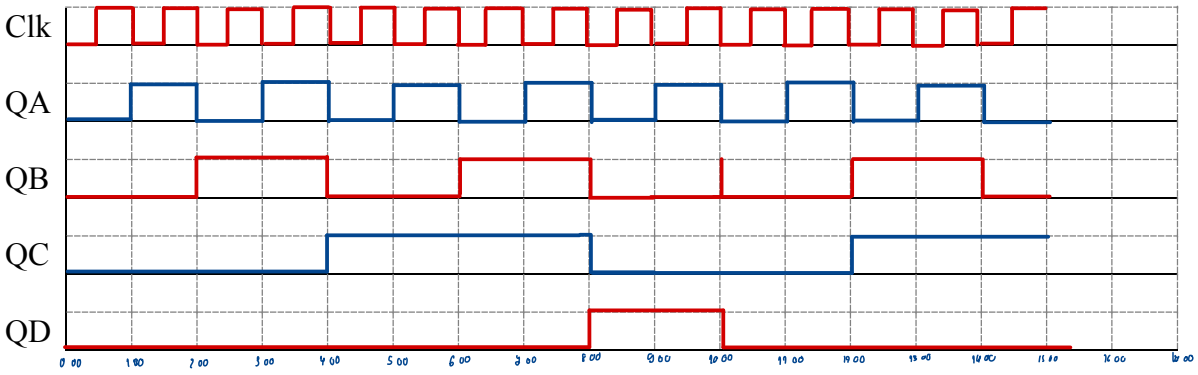


Figure 5

b. BCD Counter Circuit using 7493



2.2 Build the circuit shown in Figure 6 in Proteus to generate gate pattern and waveforms of the NAND gate. Sketch the waveforms of the NAND gate and obtain its truth table. Repeat the process for NOR, NOT, AND, OR, and XOR gates.

a. NAND

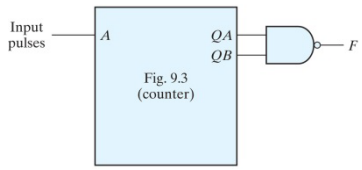
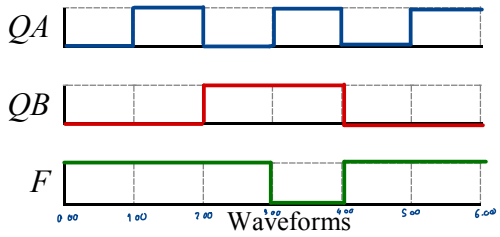


Figure 6

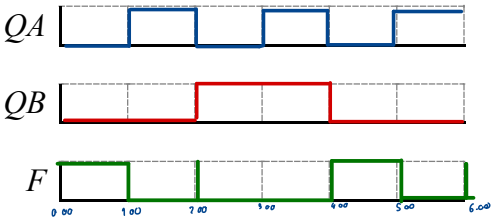
QB	QA	F
0	0	1
0	1	1
1	0	1
1	1	0



Waveforms

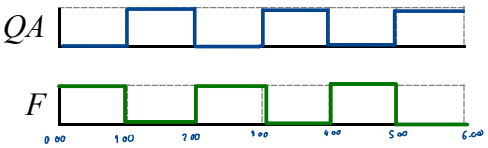
b. NOR

QB	QA	F
0	0	1
0	1	0
1	0	0
1	1	0



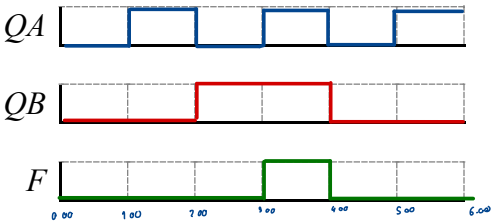
c. NOT

-	QA	F
	0	1
	1	0
	0	1
	1	0



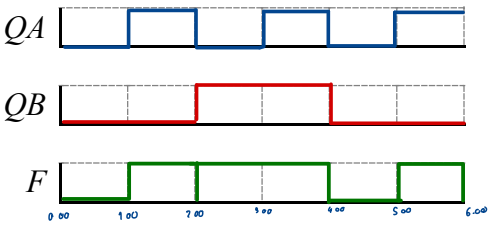
d. AND

QB	QA	F
0	0	0
0	1	0
1	0	0
1	1	1



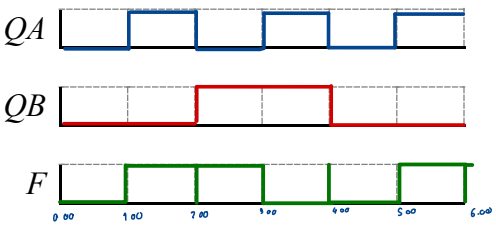
e. OR

QB	QA	F
0	0	0
0	1	1
1	0	1
1	1	1



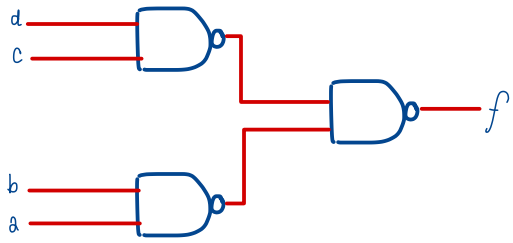
f. XOR

QB	QA	F
0	0	0
0	1	1
1	0	1
1	1	0



Experiment 2 Using NAND gates to implement the Boolean function $F = AB + CD$

a. Draw the circuit diagram.

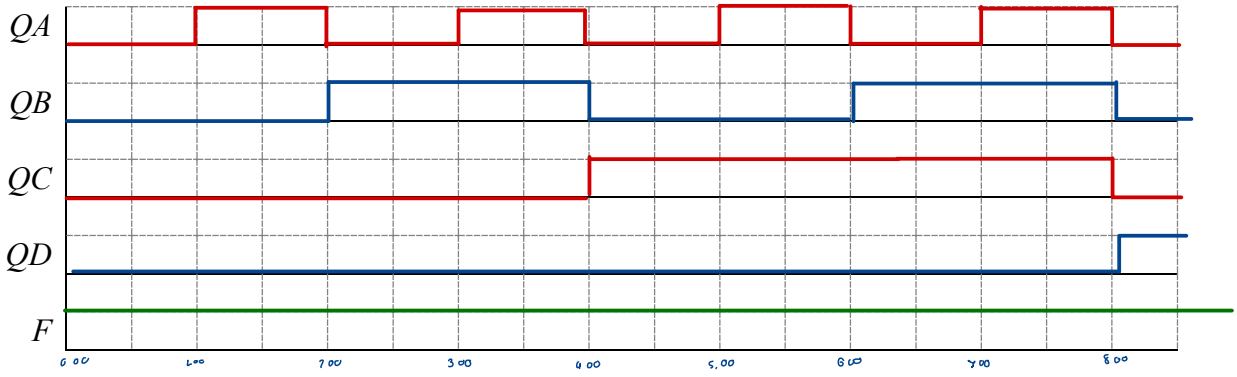


b. Obtain the truth table for F.

D	C	B	A	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1

D	C	B	A	F
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

c. Connect the four outputs of the binary counter shown in Figure 4 to the four inputs of the NAND circuit. Simulate and sketch the waveforms.



Experiment 3 Obtain the Boolean function of the circuit shown in Fig. 7 and simplify it, using postulates and theorems of Boolean algebra (or the map method). Use Proteus program to test both circuits; the original and the simplified ones. Show the test results to the Lab assistant.

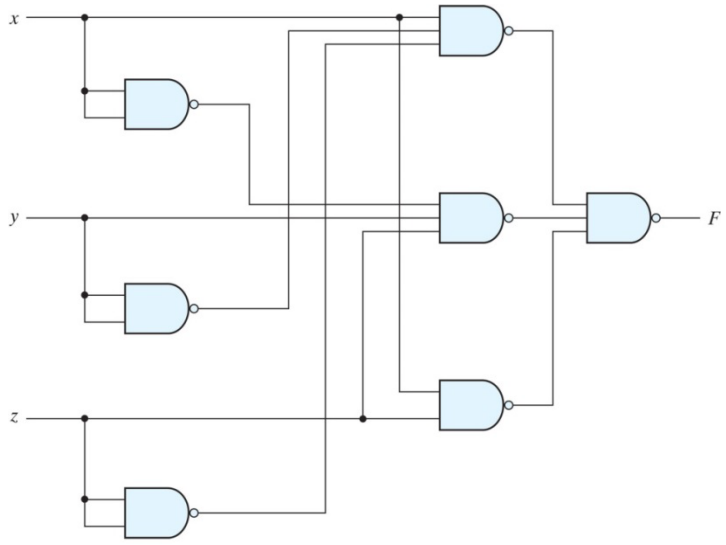


Fig. 7

Boolean function.

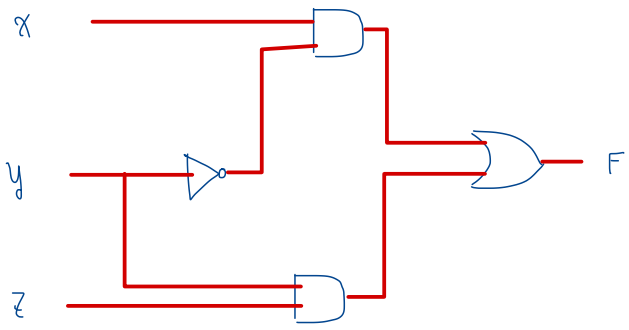
x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$\Sigma\,(3,4,5,7)$

x \ yz	00	01	11	10
0			1	
1		1	1	

$= x\bar{y} + yz$

Sketch the simplified circuit.



Circuit Testing

Build the simplified circuit (TEST CCT) using 74LS00 (NAND gates) and 74LS93 as a test pattern generator (Fig. 8). Show the result to the Lab assistant.

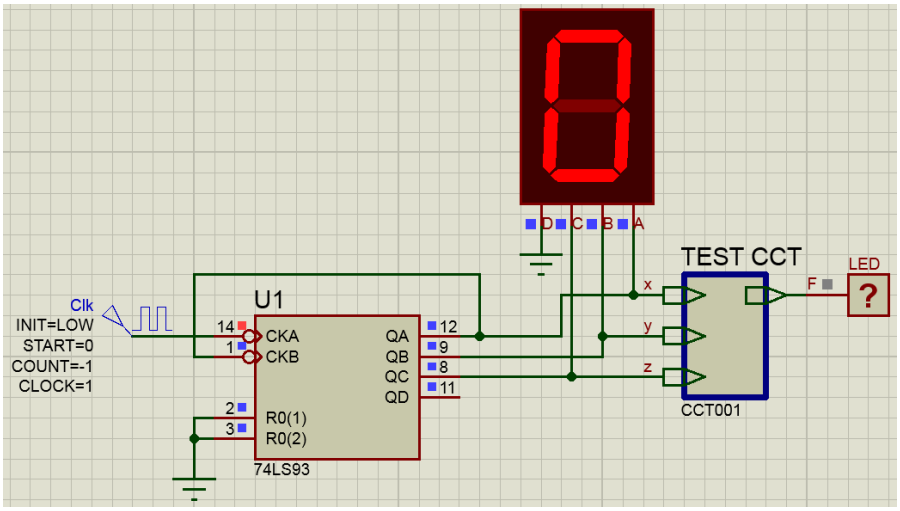


Fig. 8

z	y	x	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1