LA_LAT_MISO -> BPIO_MISO

Some kind of FLASH (Winbond?) to store the FPGA bitstreams
connect to MCU hardware SPI so we can use DMA

SRAM UB/LB signal not needed

GBIN/BUF = CLOCK: 0,2,4,6=RESET; 1,3,5,7=CLOCK ENABLE
MCU clock out to GBIN
FSMC (OE/WE/CE) to GBIN?
MCU PWM to GBIN?

SS pulled low for slave config mode

FGPA to MCU hardware SPI
Also to pin header for development programming

DIR IO OD BP
H H H H
H L H L
L IN H Z (input)
L IN L L (open drain LOW)
H X L :((contention)

BUILT-IN LOGIC ANALYZER
10 SRAM + IO_OE need to connect to FPGA and MCU

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BUS PIRATE V5
Ian Lesnet 2014
http://dangerousprototypes.com

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