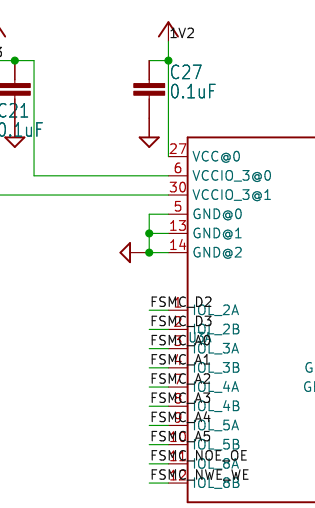
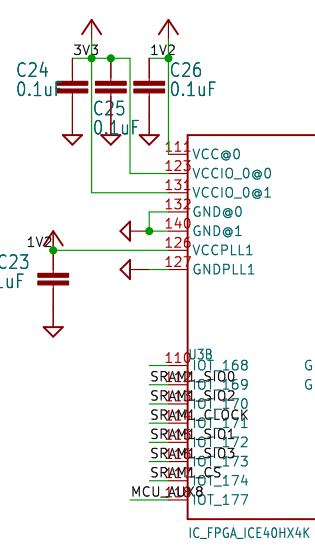
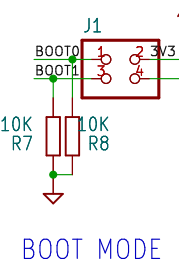
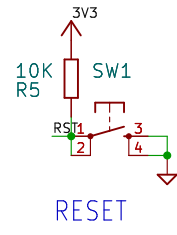
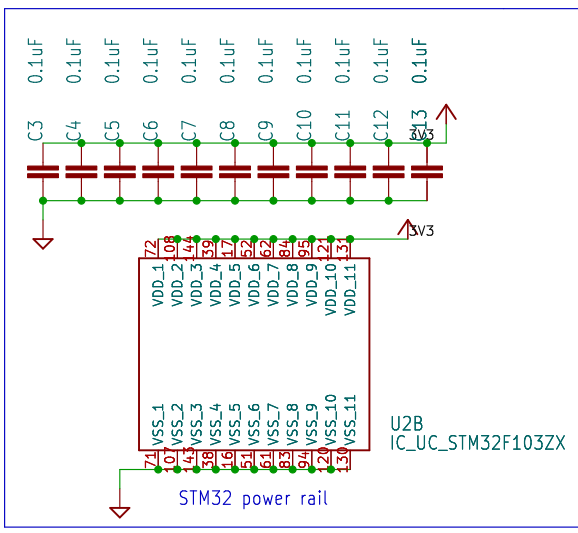
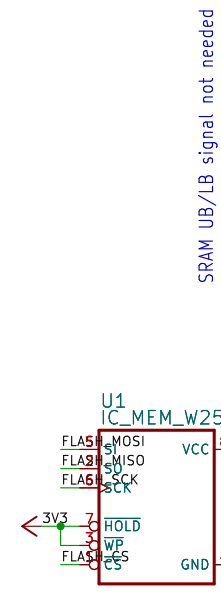
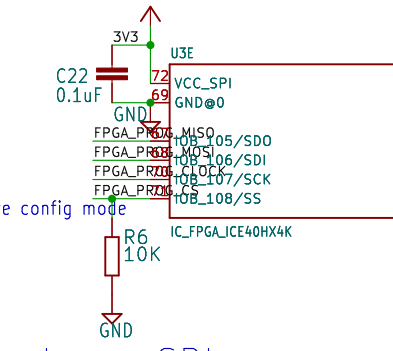


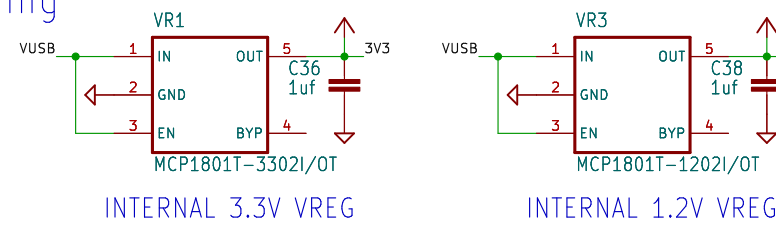
Some kind of FLASH (Winbond?) to store the FPGA bitstreams
connect to MCU hardware SPI so we can use DMA



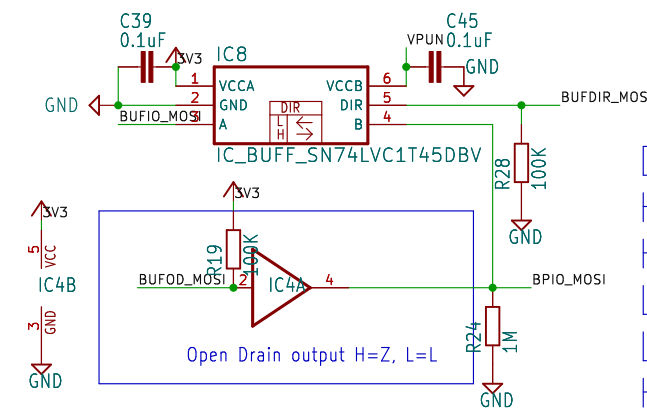
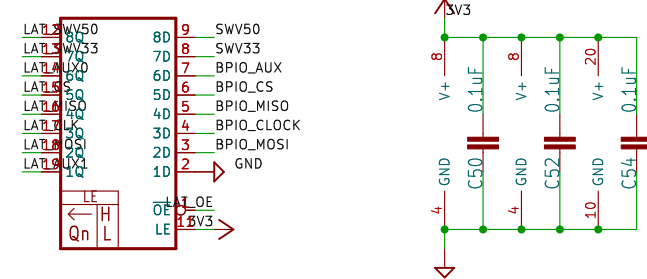
GBIN/BUF = CLOCK; 0,2,4,6=RESET; 1,3,5,7=CLOCK ENABLE
MCU clock out to GBIN?
FSMC OE/WE/CE to GBIN?
MCU PWM to GBIN?



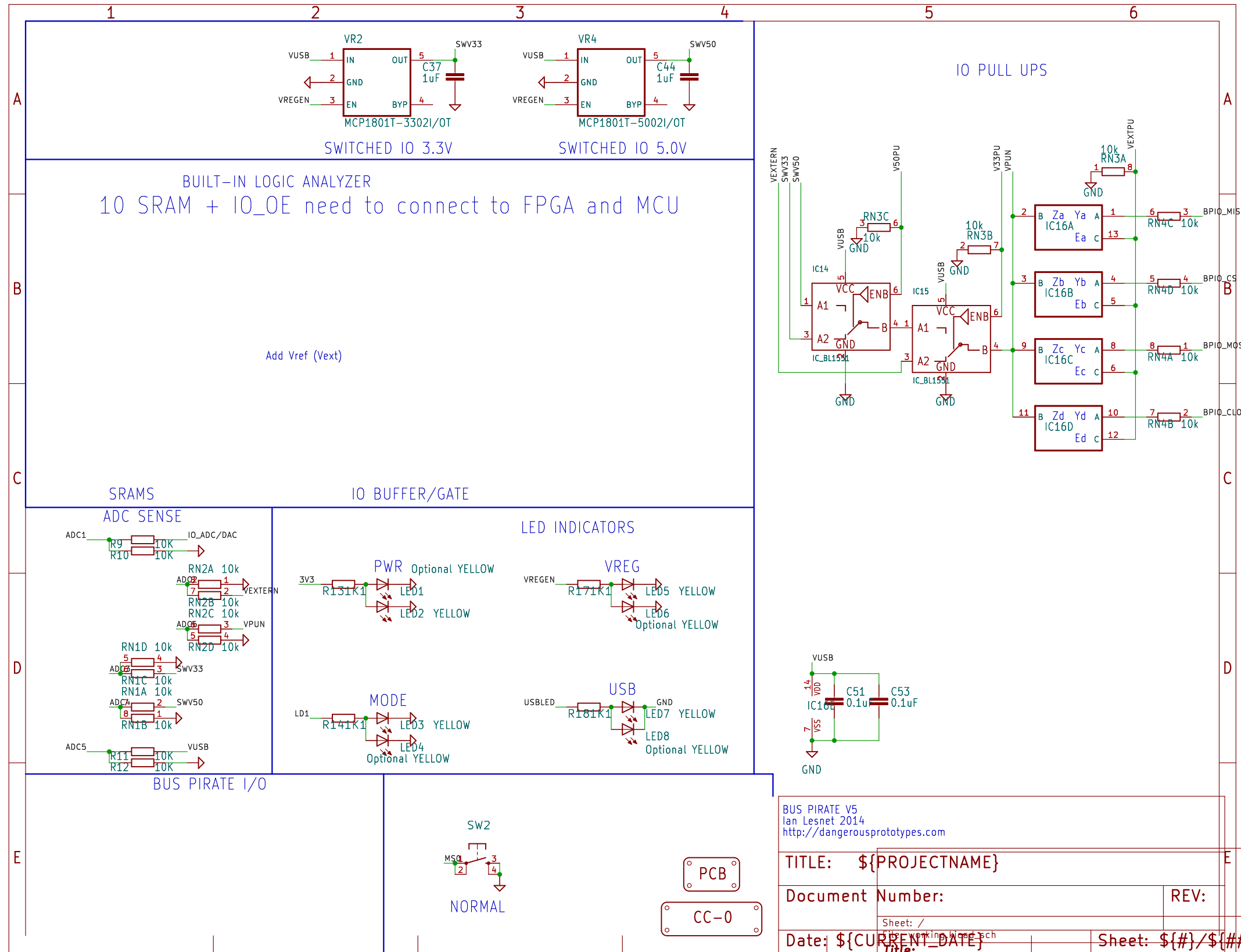
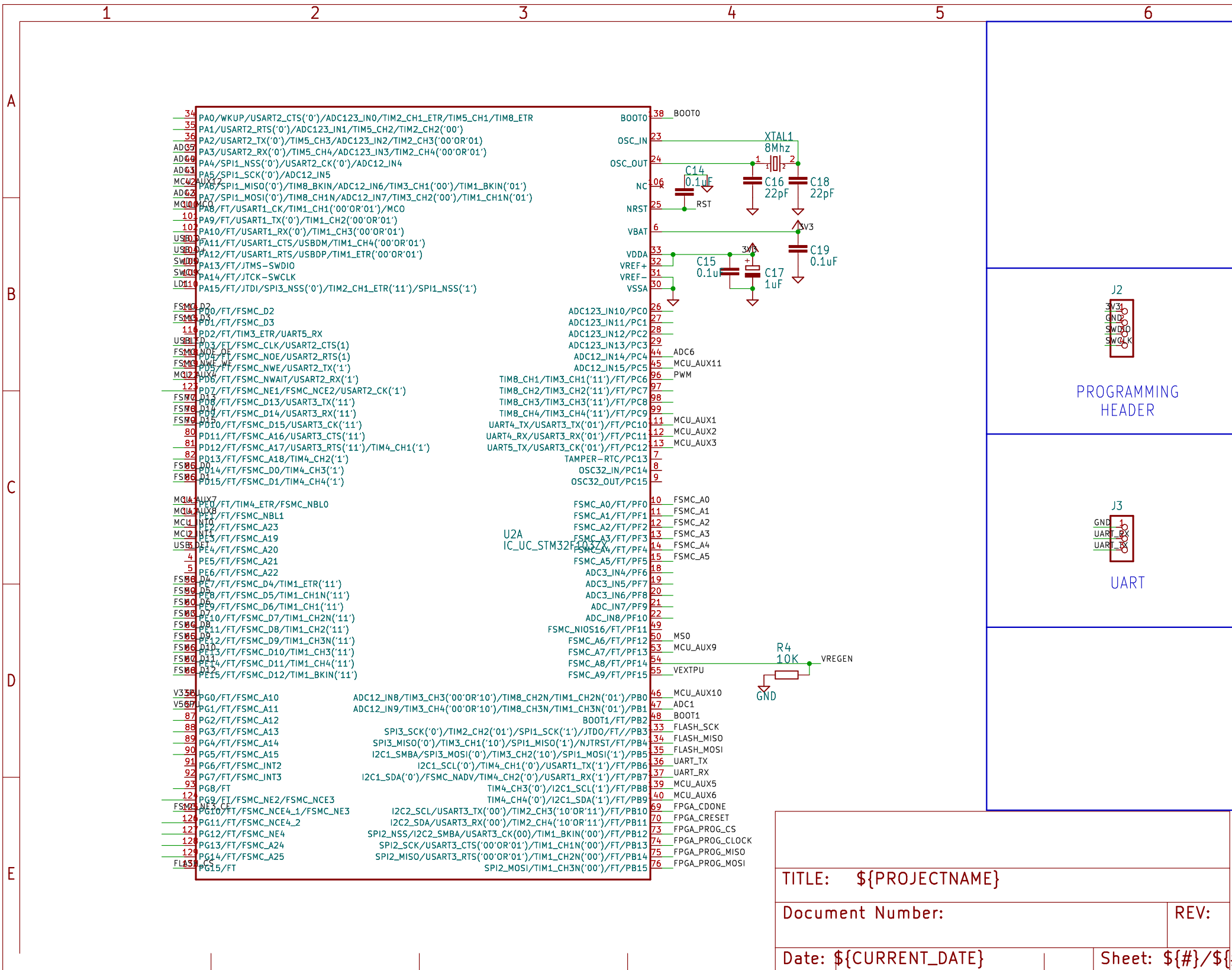
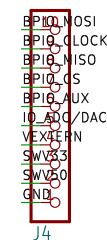
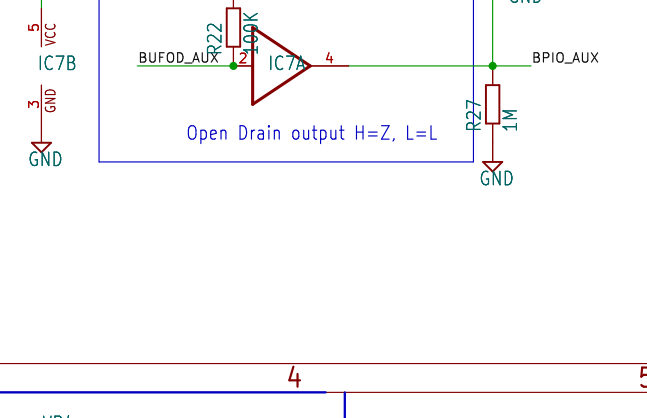
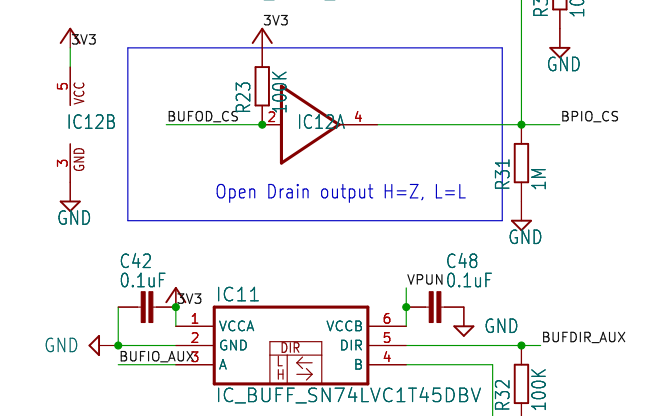
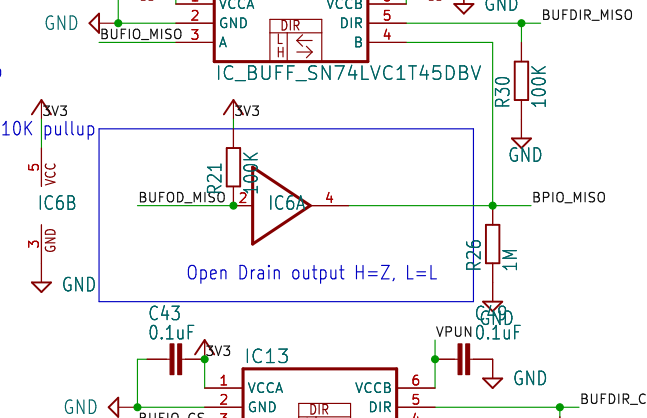
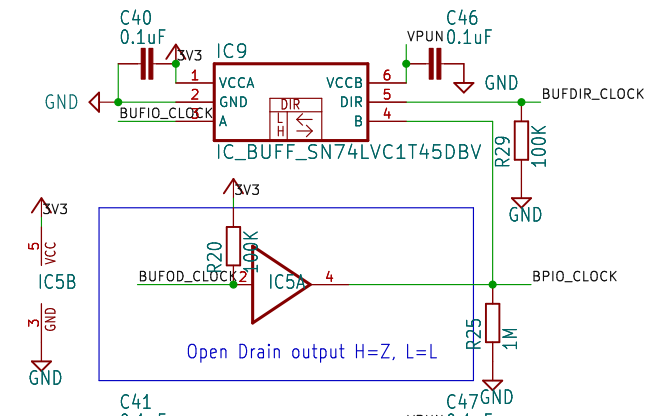
FPGA to MCU hardware SPI
Also to pin header for development programming



LAT_LAT_MISO -> BPIO_MISO



DIR IO OD BP
H H H L
H L H L
H IN H Z (input)
H IN L L (open drain LOW)
H X L : (contention)



TITLE: \${PROJECTNAME}

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