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HDL LAB-10ECL48. VIVA – VOCE QUESTIONS Expand VHDL.What is the difference between VHDL and Verilog? What is the difference between (i) signal and variable (ii) generic & Parameter (iii) function & procedure (iv) task & function (v) always & initial (vi) register & variable (vii) signal & wire

HDL LAB VIVA VOCE Questions

This top 10 VHDL,Verilog,FPGA interview questions and answers will help interviewee pass the job interview for FPGA programmer job position with ease. These questions are very useful as FPGA viva questions also. Question -1: Write a simple VHDL program for D Flipflop and D latch.

10 VHDL,Verilog,FPGA interview questions and answers

Sushanth KJ, Asst. Pr of. Dept. of ECE, BIT, Mangalur u Page 8 VLSI Lab Viva questions and answ er s Hold Time: The after the active clock edge of the flip-flop, the input should be stable. If the signal changes during this interval, the output of that flip-flop cannot be predictable (called metastable).

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