

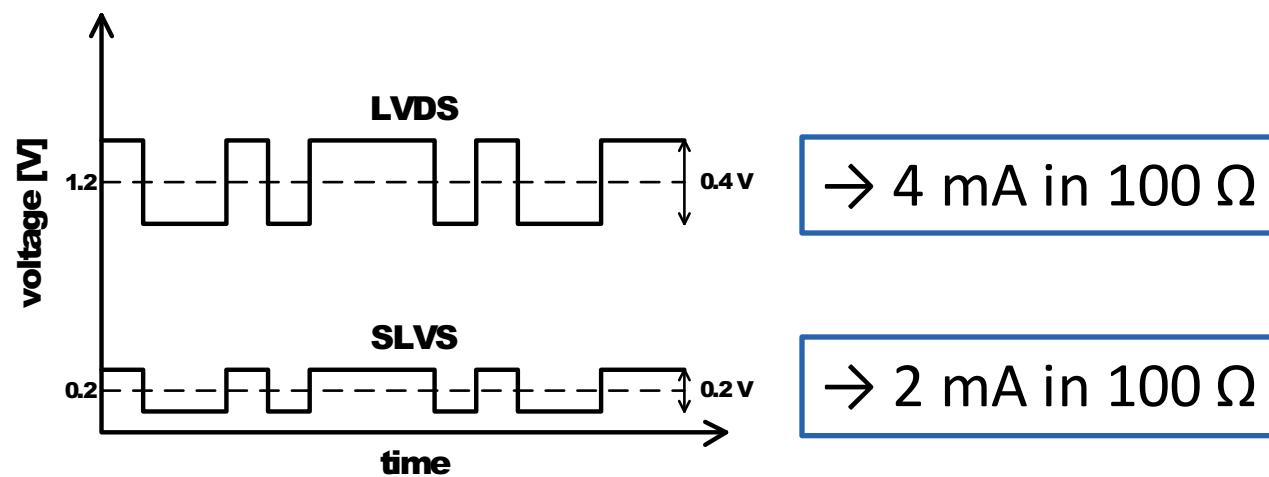


# SLVS interface circuits

**Filip Tavernier  
Paulo Moreira**

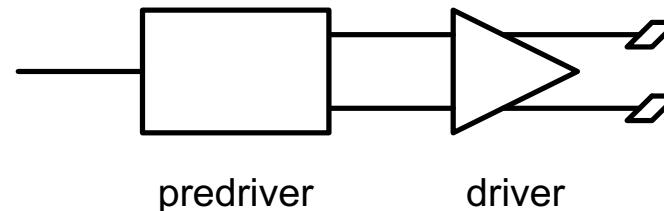
# General specifications

- **TX:** transmit SLVS signals up to 320 Mbit/s or clocks up to 320 MHz
- **RX:** receive SLVS and LVDS signals up to 320 Mbit/s or clocks up to 320 MHz
- **Rx:** integrated programmable (ON/OFF) termination resistor
- **Tx/Rx:** working at a supply voltage between 1.2 V and 1.5 V (1.5 V is required if LVDS signals need to be received)
- **Tx/Rx:** can be disabled (Tx has a high-impedance output)



# Architecture of the SLVS Tx

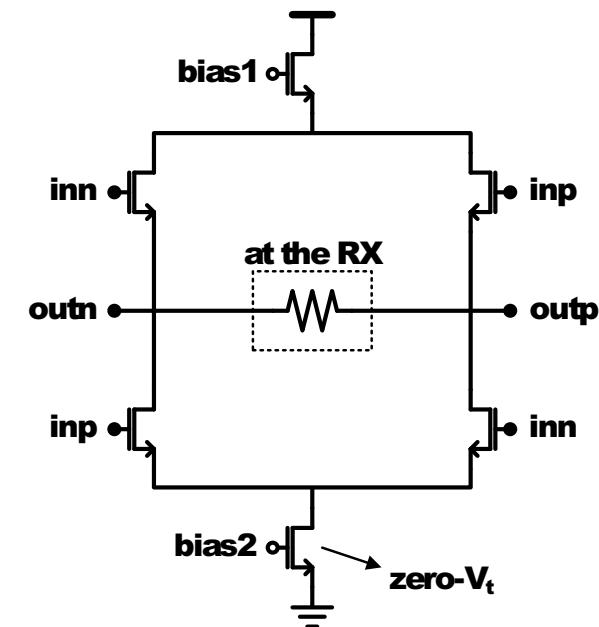
- signals:
  - input: digital single-ended voltage
  - output: analog differential current
- building blocks:
  - predriver: converts the input signal into a differential digital voltage
  - driver: converts the differential voltage into a differential current (programmable with  $cset<3:0>$ )





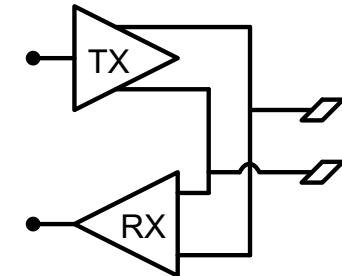
# The TX driver

- off = **LOW**
  - inp = **HIGH** & inn = **LOW**  
→ current flows ‘from right to left’ in the termination resistor
  - inp = **LOW** & inn = **HIGH**  
→ current flows ‘from left to right’ in the termination resistor
  - The current in the driver stage is set by the ‘cset’ bits in the biasing circuit (not shown here)
- off = **HIGH**
  - bias1 = bias2 = 0 V (set by the biasing circuit)
  - Although the zero-V<sub>t</sub> current source is never completely off, both inp and inn are **LOW** (see previous slide) so that the outputs are high impedance → can be used on a bus



# Simulation of the SLVS Tx

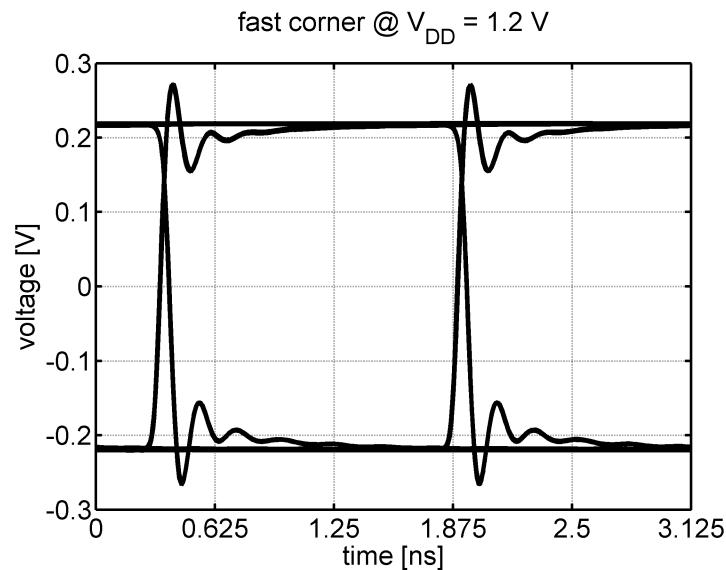
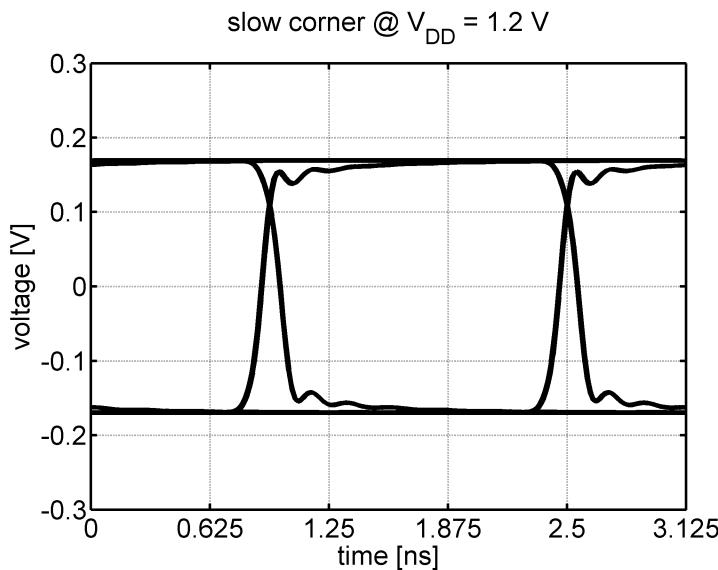
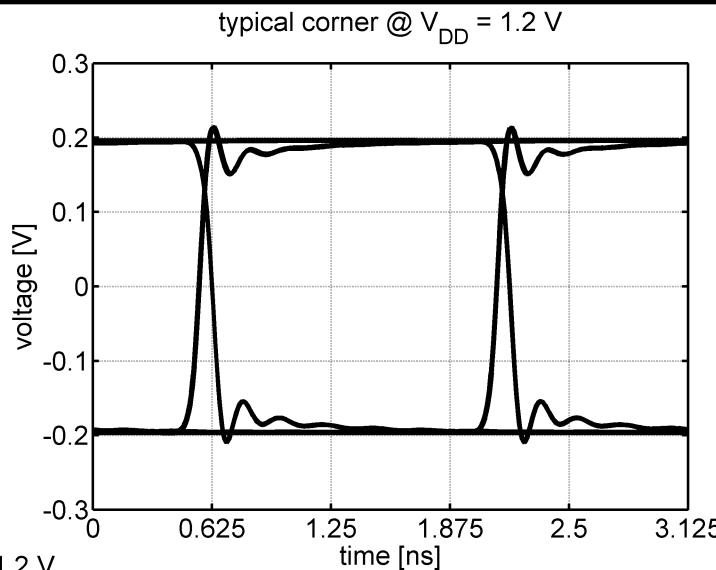
- simulation of the Tx in the bi-directional cell
- simulation of RC-extracted netlists
- simulation in 3 corners:
  - typical:**  $V_{DD} = 1.2 \text{ V}$  (1.5 V) /  $T = 27^\circ \text{ C}$  / TT models
  - slow:**  $V_{DD} = 1.1 \text{ V}$  (1.4 V) /  $T = 100^\circ \text{ C}$  / SS models
  - fast:**  $V_{DD} = 1.35 \text{ V}$  (1.65 V) /  $T = -30^\circ \text{ C}$  / FF models
- simulation with the ‘nominal’ current setting (2 mA)
- input signal:  $2^7\text{-}1$  PRBS @ 640 Mbit/s
- off-chip termination resistor of  $100 \Omega$
- package modeled by 1 nH bondwire inductors and 1 pF off-chip parasitic capacitance



# Simulation of the SLVS Tx @ $V_{DD} = 1.2 \text{ V}$

current [mA] / power [mW]:

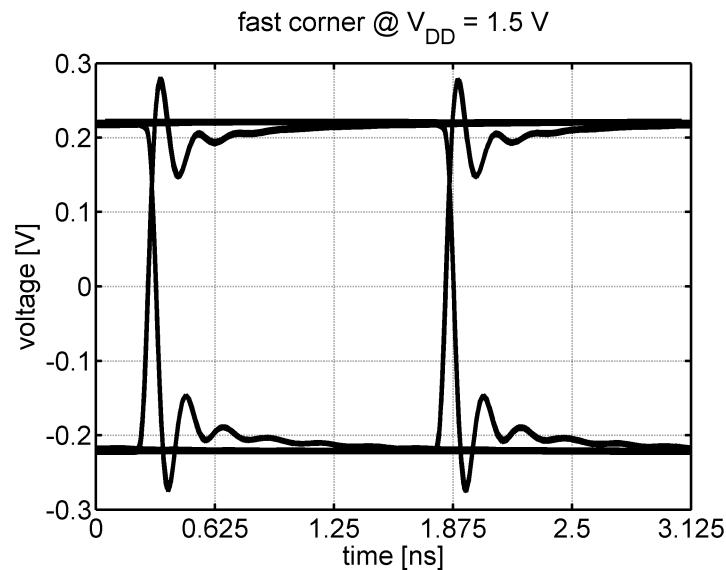
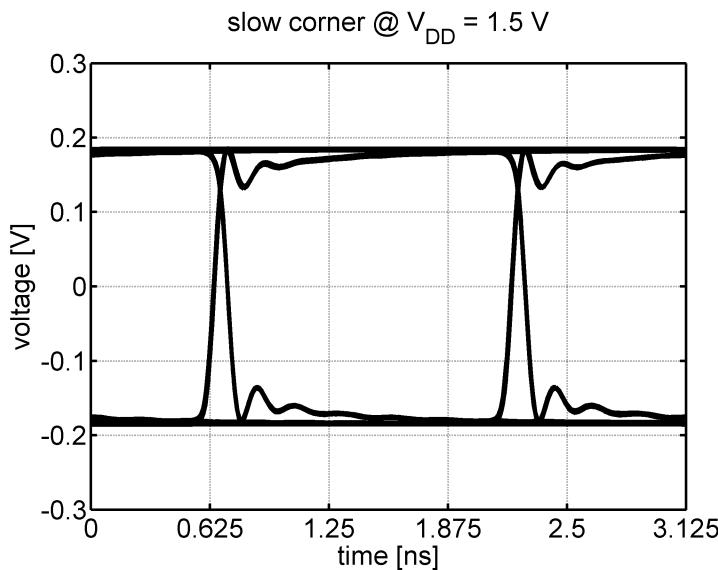
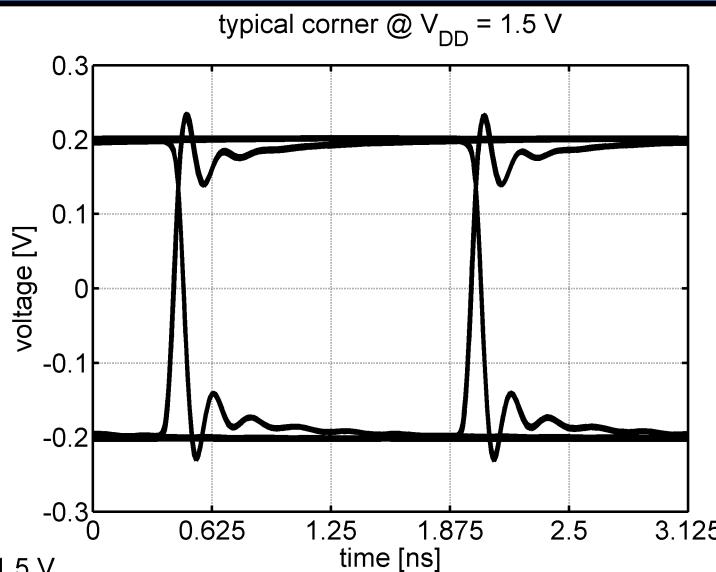
- typical: 3.31 / 3.97
- slow: 2.73 / 3.00
- fast: 4.13 / 5.58



# Simulation of the SLVS Tx @ $V_{DD} = 1.5$ V

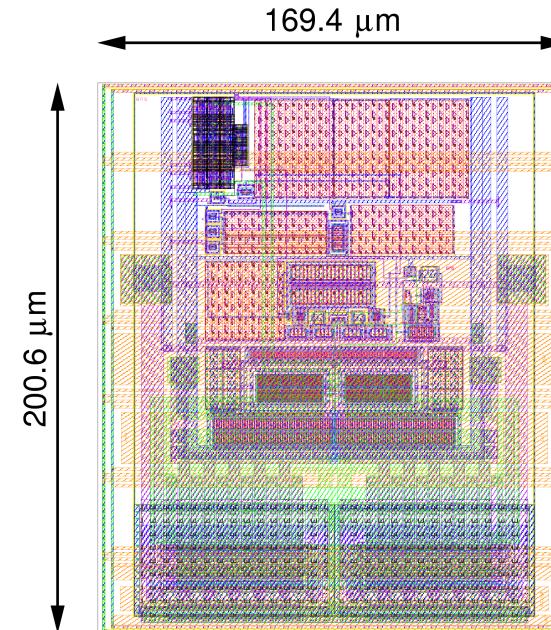
current [mA] / power [mW]:

- typical: 4.01 / 6.02
- slow: 3.41 / 4.77
- fast: 4.93 / 8.13



# SLVS Tx versions

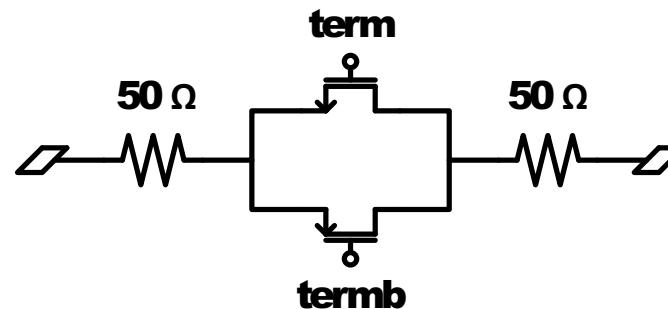
	C4	wirebond
technology	IBM 130 nm LM	IBM 130 nm DM
metals used	M1-M4	M1-MA
size	169.4 $\mu\text{m}$ x 200.6 $\mu\text{m}$	146.28 $\mu\text{m}$ x 215.28 $\mu\text{m}$
pitch	168.4 $\mu\text{m}$ vertical 199.6 $\mu\text{m}$ horizontal	146 $\mu\text{m}$ vertical 215 $\mu\text{m}$ horizontal



# Programmable Rx termination resistor

Rx needs to terminate SLVS ( $V_{CM} = 0.2$  V) and LVDS ( $V_{CM} = 1.2$  V) signal levels with a  $100\ \Omega$  resistance

- nMOS switch is needed to enable a low switch resistance while receiving SLVS signals
- pMOS switch is needed to enable a low switch resistance while receiving LVDS signals
- large switches are needed to minimize the dependency of the termination resistance on supply voltage variations  
(design point: switch resistance <  $10\ \Omega$  in all cases)



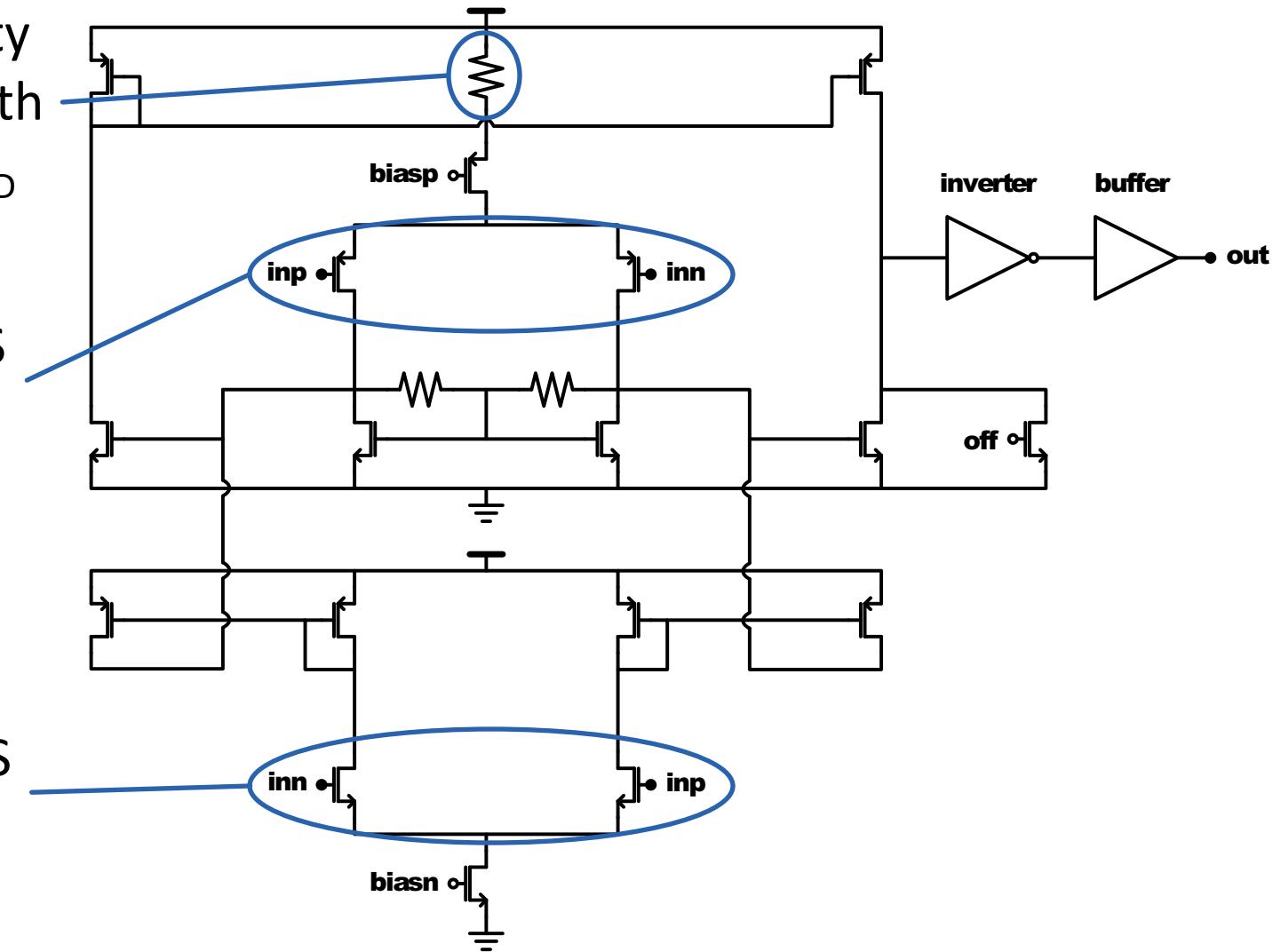


# Amplifier of the SLVS/LVDS Rx

reduce sensitivity  
of the current with  
variations of  $V_{DD}$

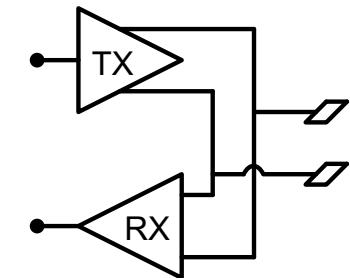
input pair for SLVS  
(off for LVDS)

input pair for LVDS  
(off for SLVS)



# Simulation of the new SLVS/LVDS Rx

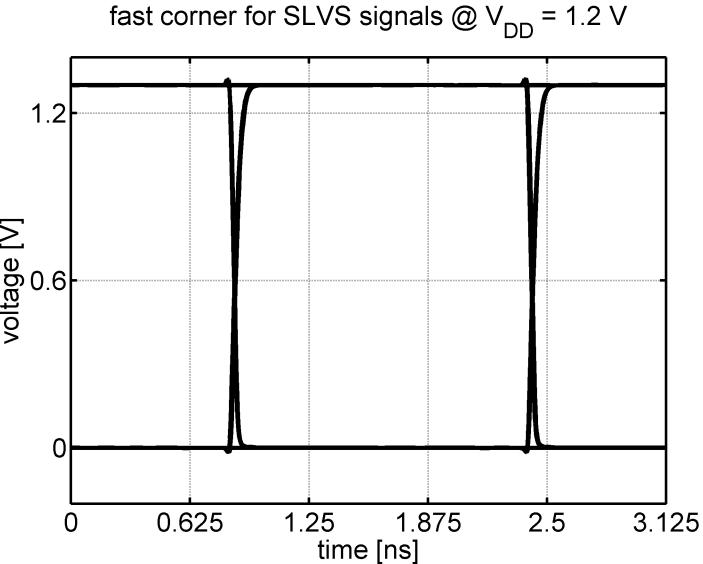
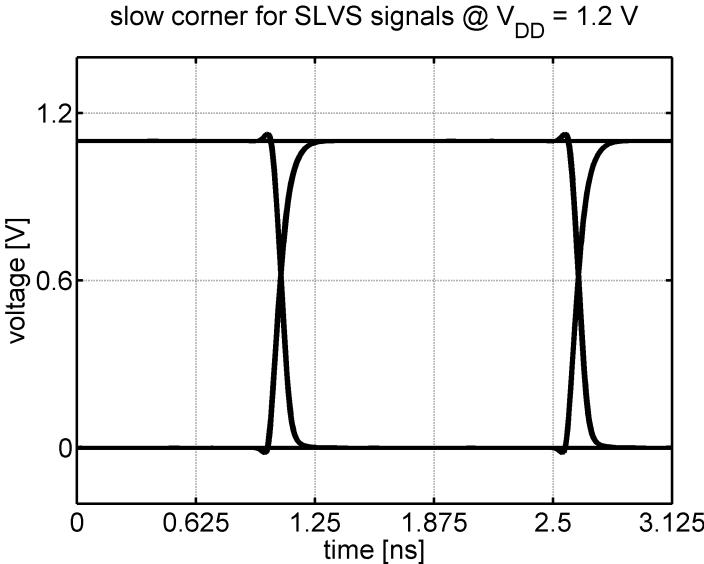
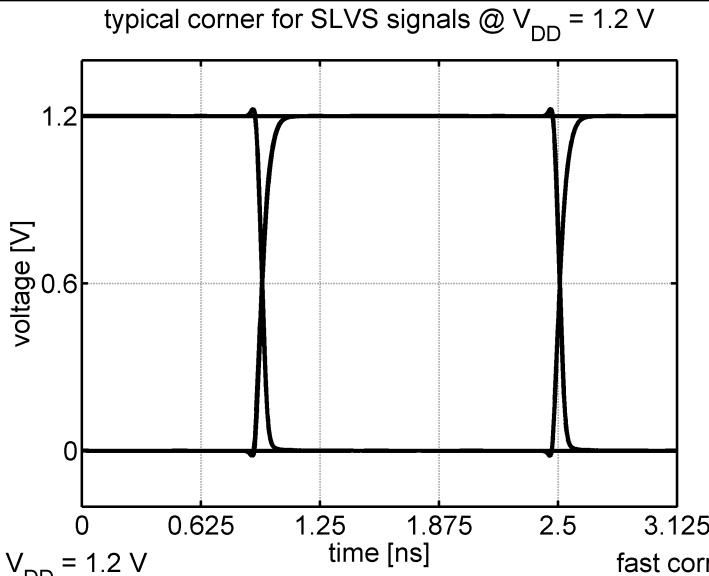
- simulation of the Rx in the bi-directional cell
- simulation of RC-extracted netlists
- simulation in 3 corners:
  - typical:**  $V_{DD} = 1.2 \text{ V}$  ( $1.5 \text{ V}$ ) /  $T = 27^\circ \text{ C}$  / TT models
  - slow:**  $V_{DD} = 1.1 \text{ V}$  ( $1.4 \text{ V}$ ) /  $T = 100^\circ \text{ C}$  / SS models
  - fast:**  $V_{DD} = 1.35 \text{ V}$  ( $1.65 \text{ V}$ ) /  $T = -30^\circ \text{ C}$  / FF models
- simulation with the on-chip termination network activated
- input signal:  $2^7\text{-}1$  PRBS @ 640 Mbit/s
- package modeled by 1 nH bondwire inductors and 1 pF off-chip parasitic capacitance



# Simulation of the Rx @ $V_{DD} = 1.2$ V with SLVS input signals

current [ $\mu$ A] / power [ $\mu$ W]:

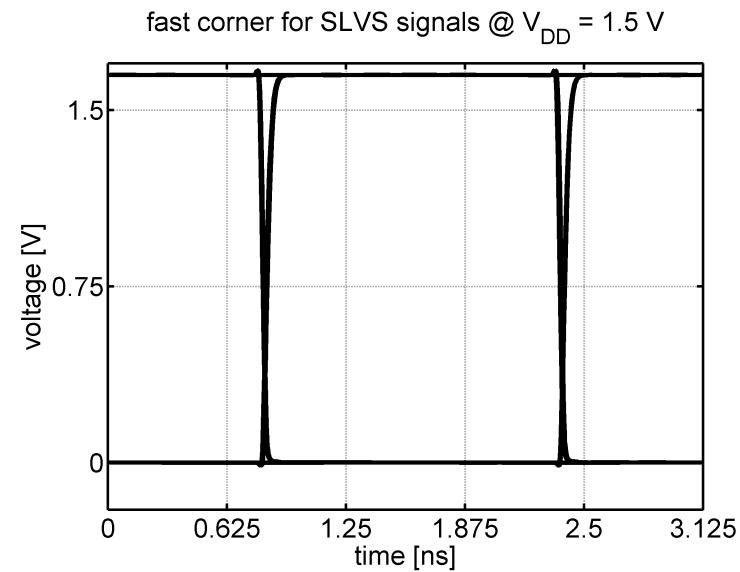
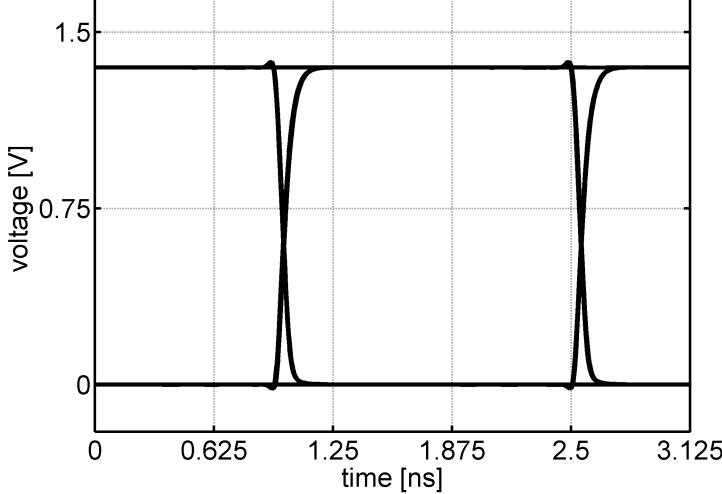
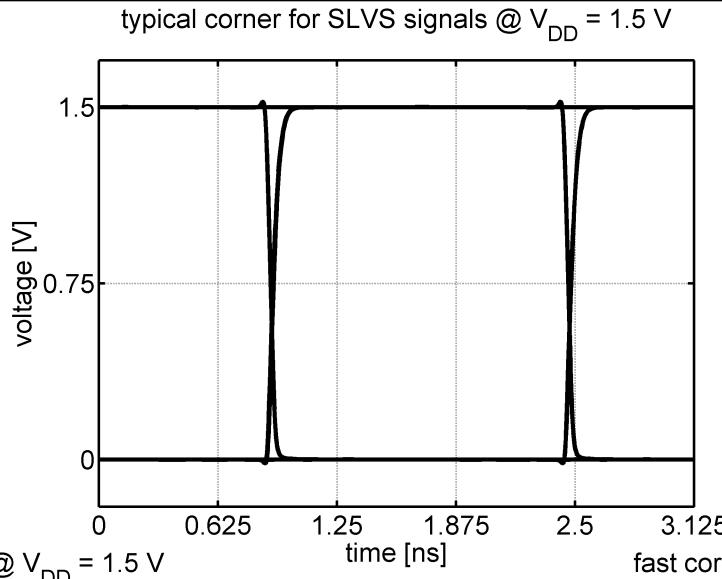
- typical: 320 / 384
- slow: 310 / 341
- fast: 298 / 402



# Simulation of the Rx @ $V_{DD} = 1.5$ V with SLVS input signals

current [ $\mu$ A] / power [ $\mu$ W]:

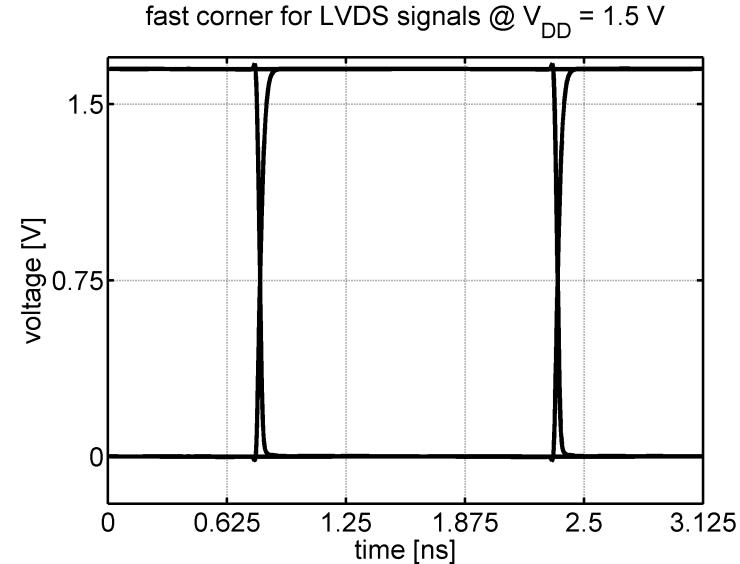
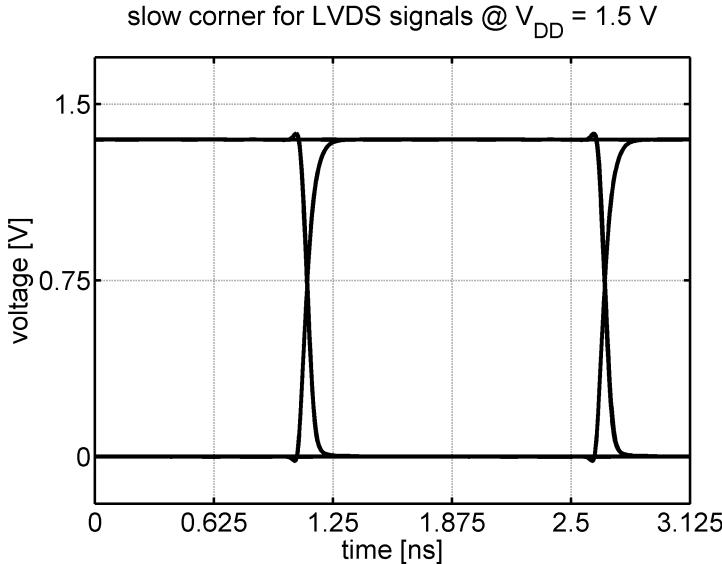
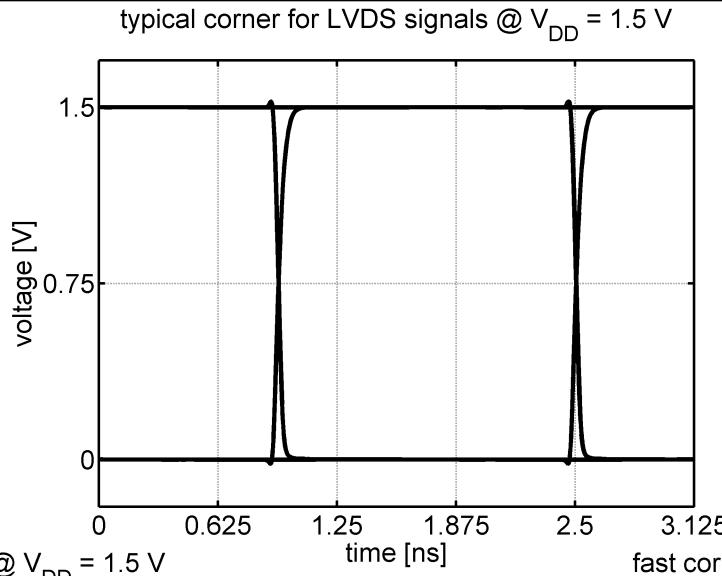
- typical: 391 / 587
- slow: 439 / 615
- fast: 390 / 644



# Simulation of the Rx @ $V_{DD} = 1.5$ V with LVDS input signals

current [ $\mu$ A] / power [ $\mu$ W]:

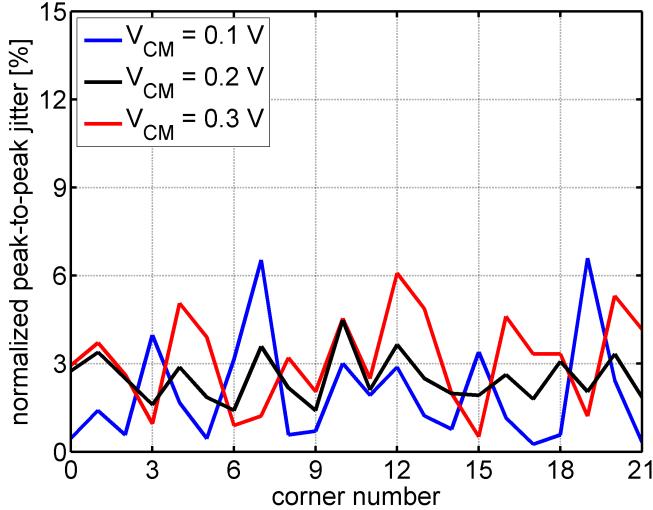
- typical: 453 / 680
- slow: 474 / 664
- fast: 481 / 794



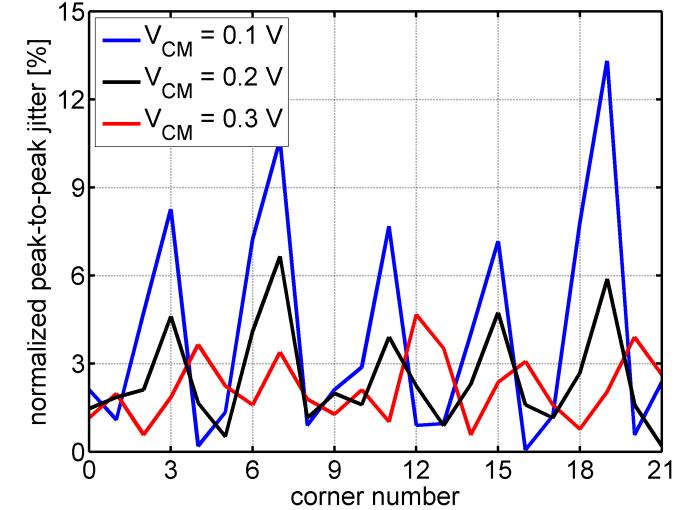


# Cross-corner DDJ for smaller-than-nominal input signals (1)

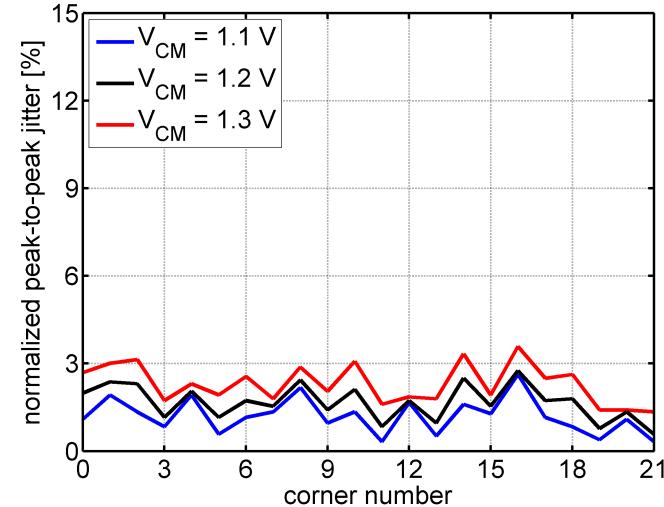
SLVS CM level @  $V_{DD} = 1.2$  V &  $I_{mod} = 0.75$  mA & 640 Mbit/s



SLVS CM level @  $V_{DD} = 1.5$  V &  $I_{mod} = 0.75$  mA & 640 Mbit/s



LVDS CM level @  $V_{DD} = 1.5$  V &  $I_{mod} = 0.75$  mA & 640 Mbit/s





# SLVS/LVDS Rx versions

	C4	wirebond
technology	IBM 130 nm LM	IBM 130 nm DM
metals used	M1-M4	M1-MA
size	169.4 $\mu\text{m}$ x 200.6 $\mu\text{m}$	146.28 $\mu\text{m}$ x 215.28 $\mu\text{m}$
pitch	168.4 $\mu\text{m}$ vertical 199.6 $\mu\text{m}$ horizontal	146 $\mu\text{m}$ vertical 215 $\mu\text{m}$ horizontal

