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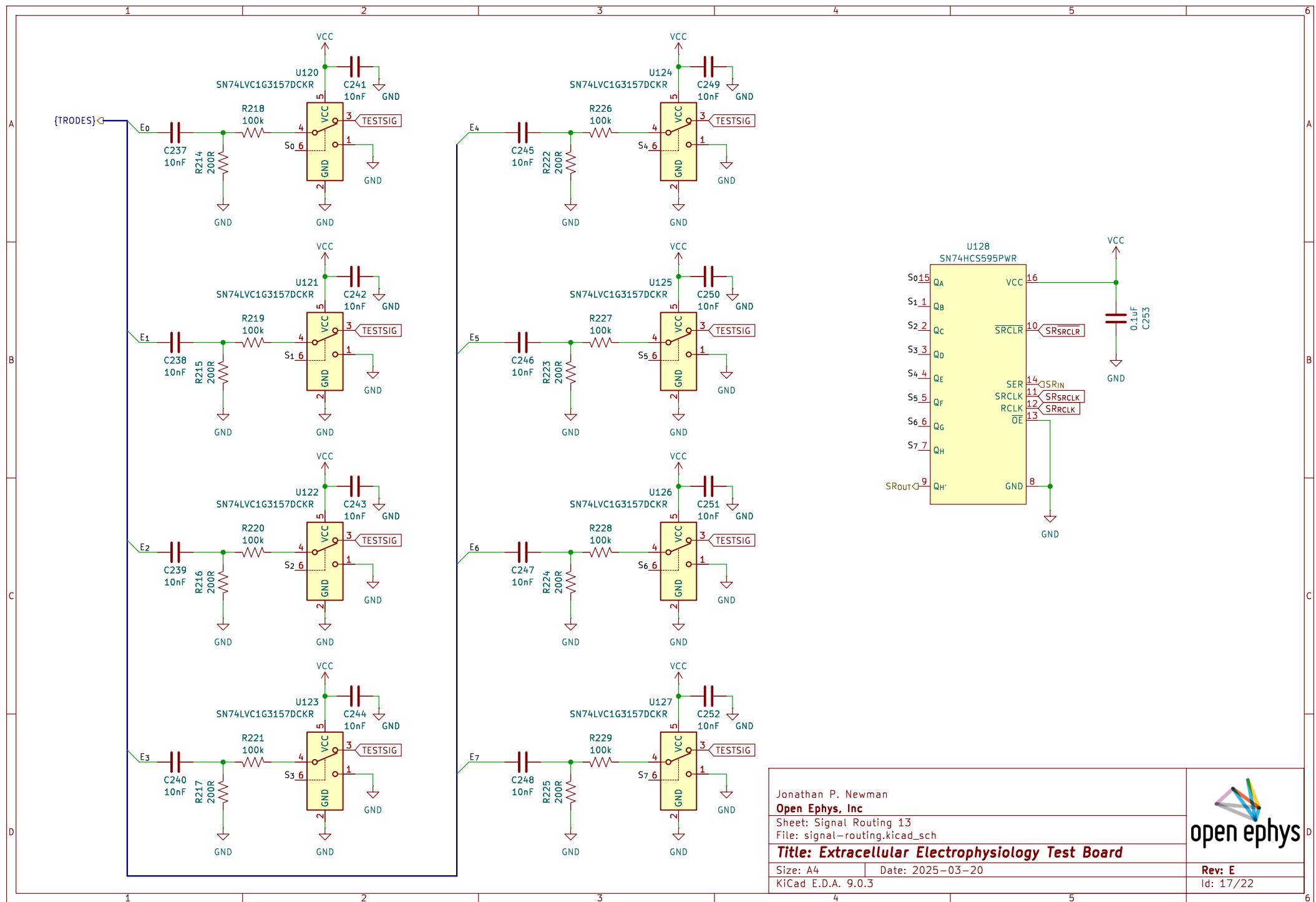
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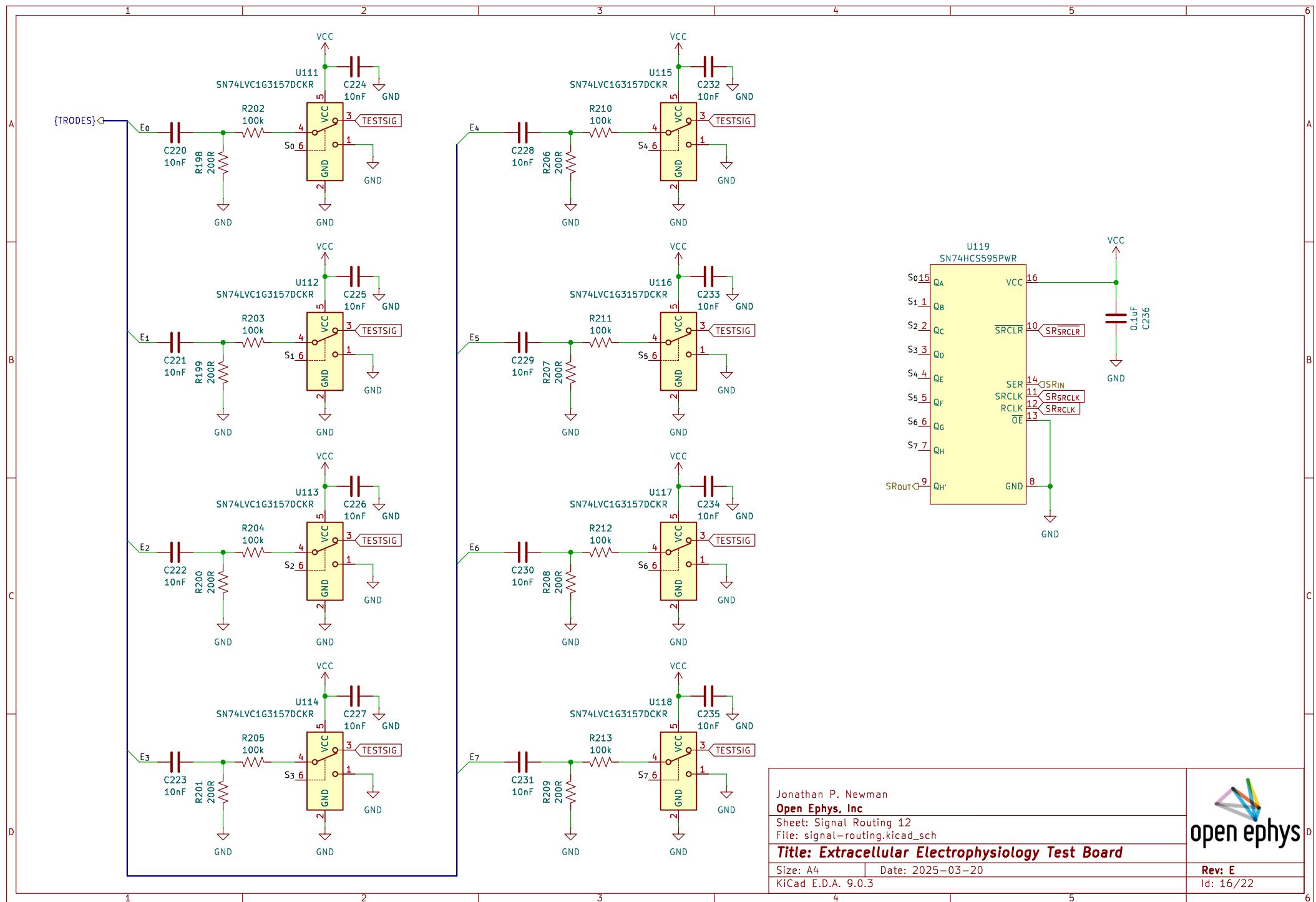
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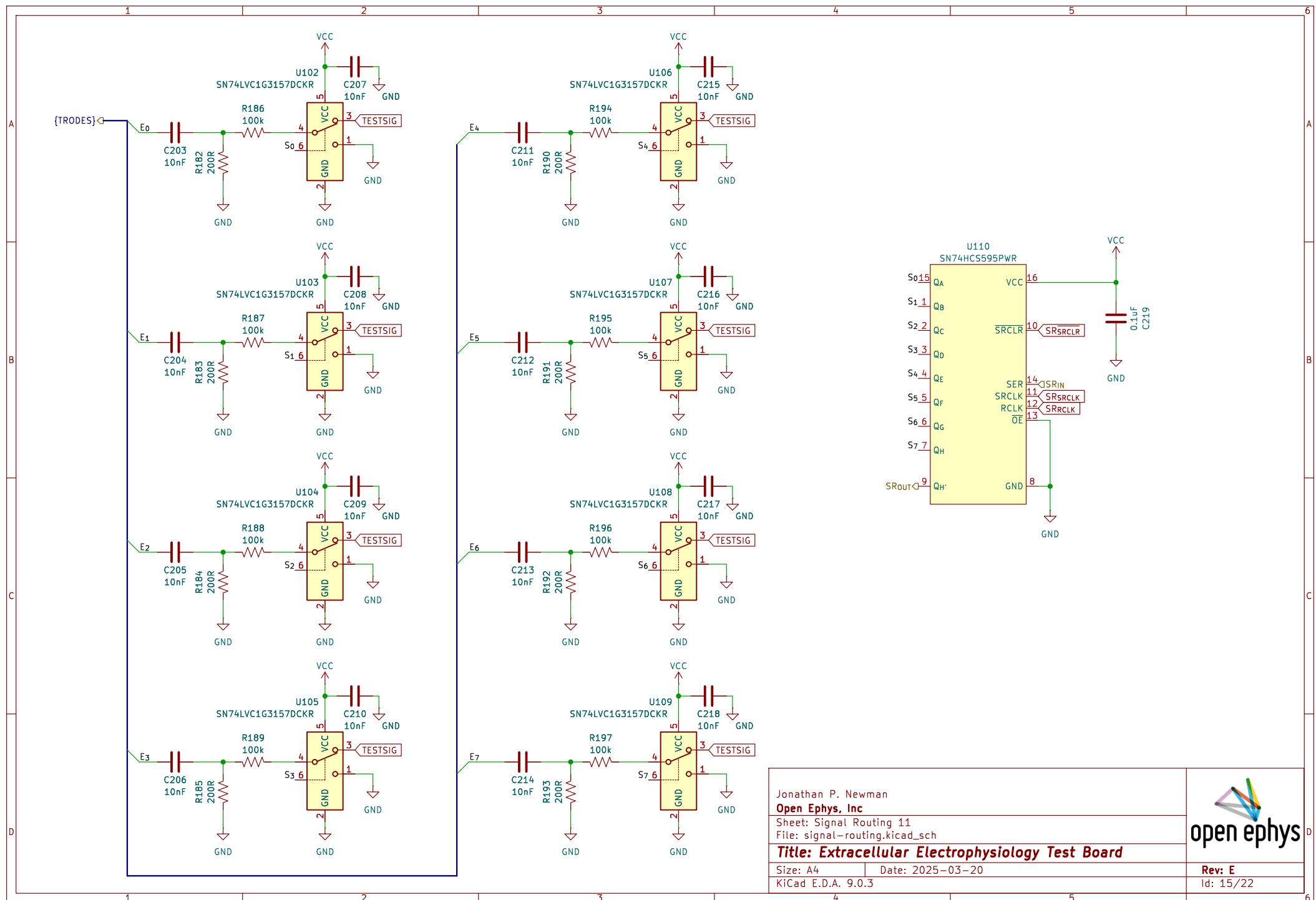
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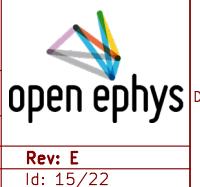


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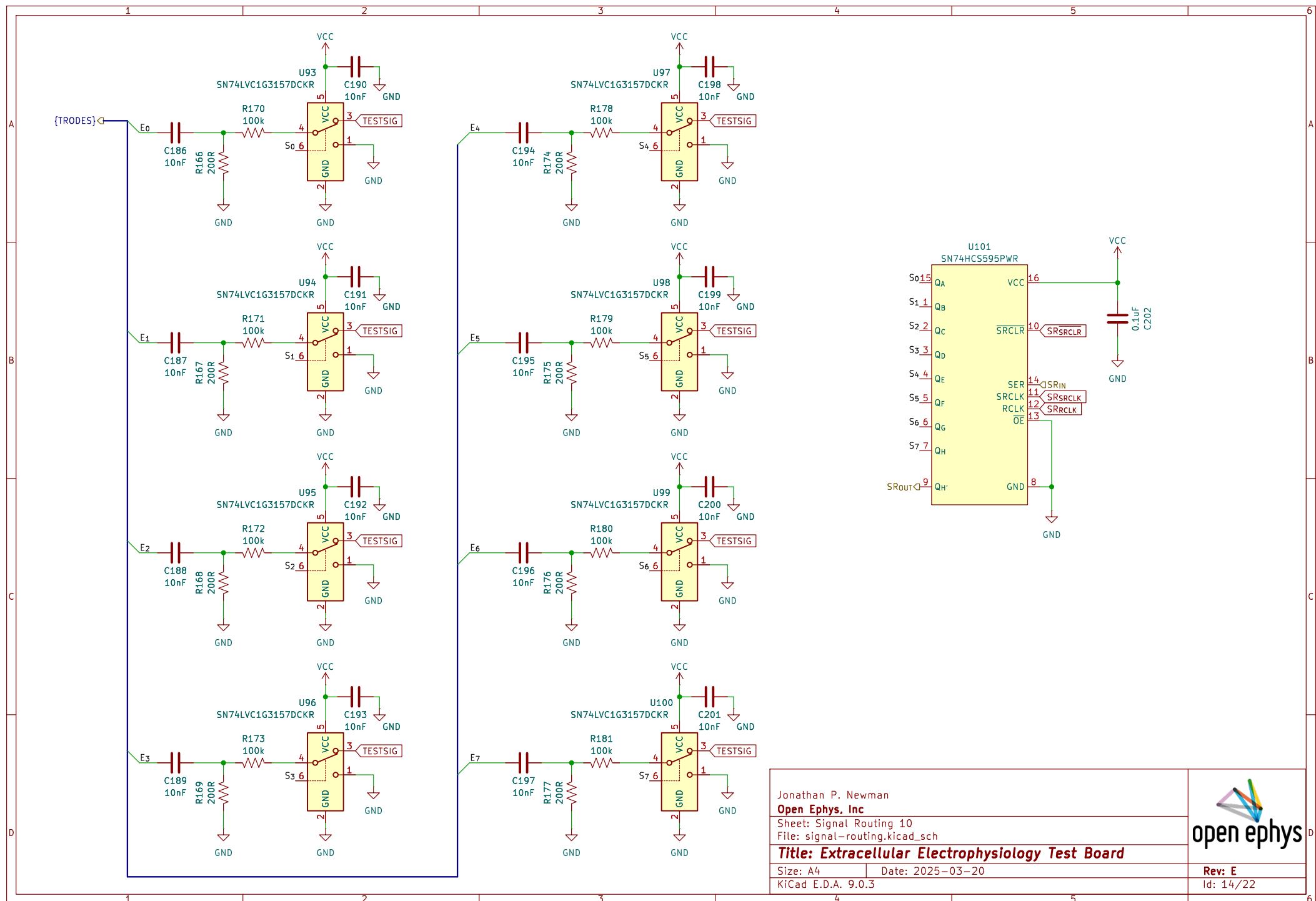
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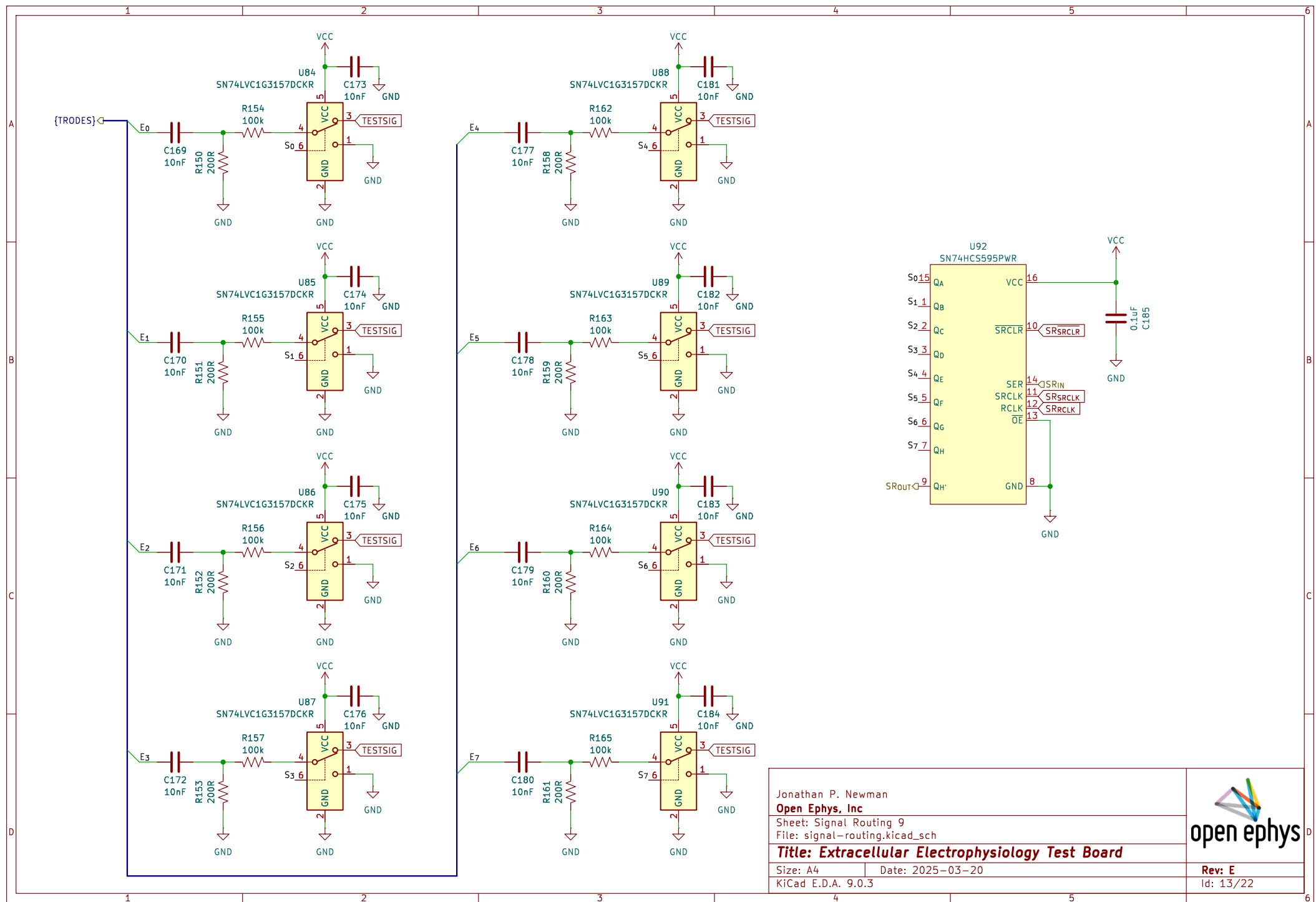
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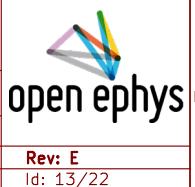


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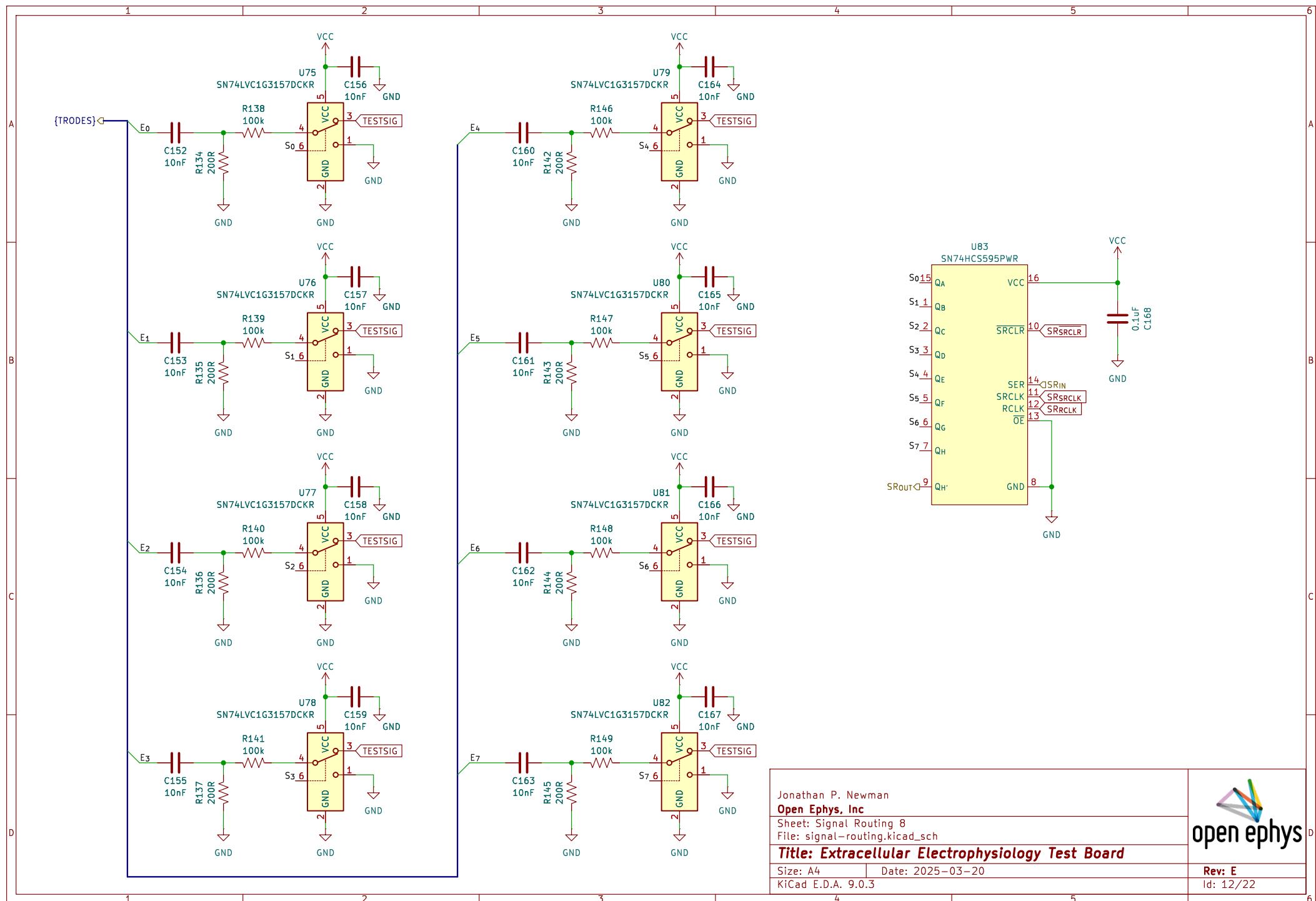
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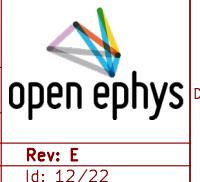


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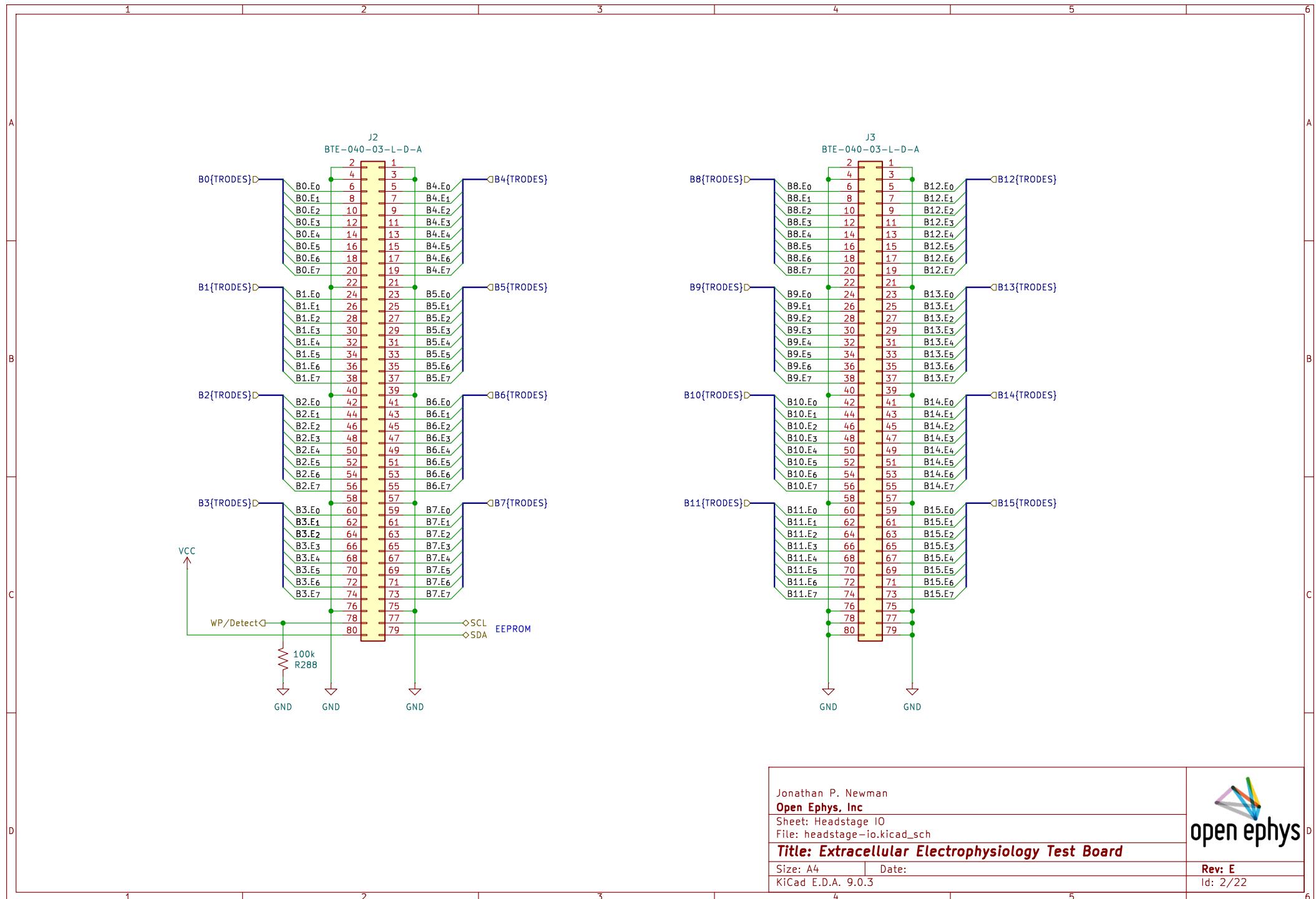
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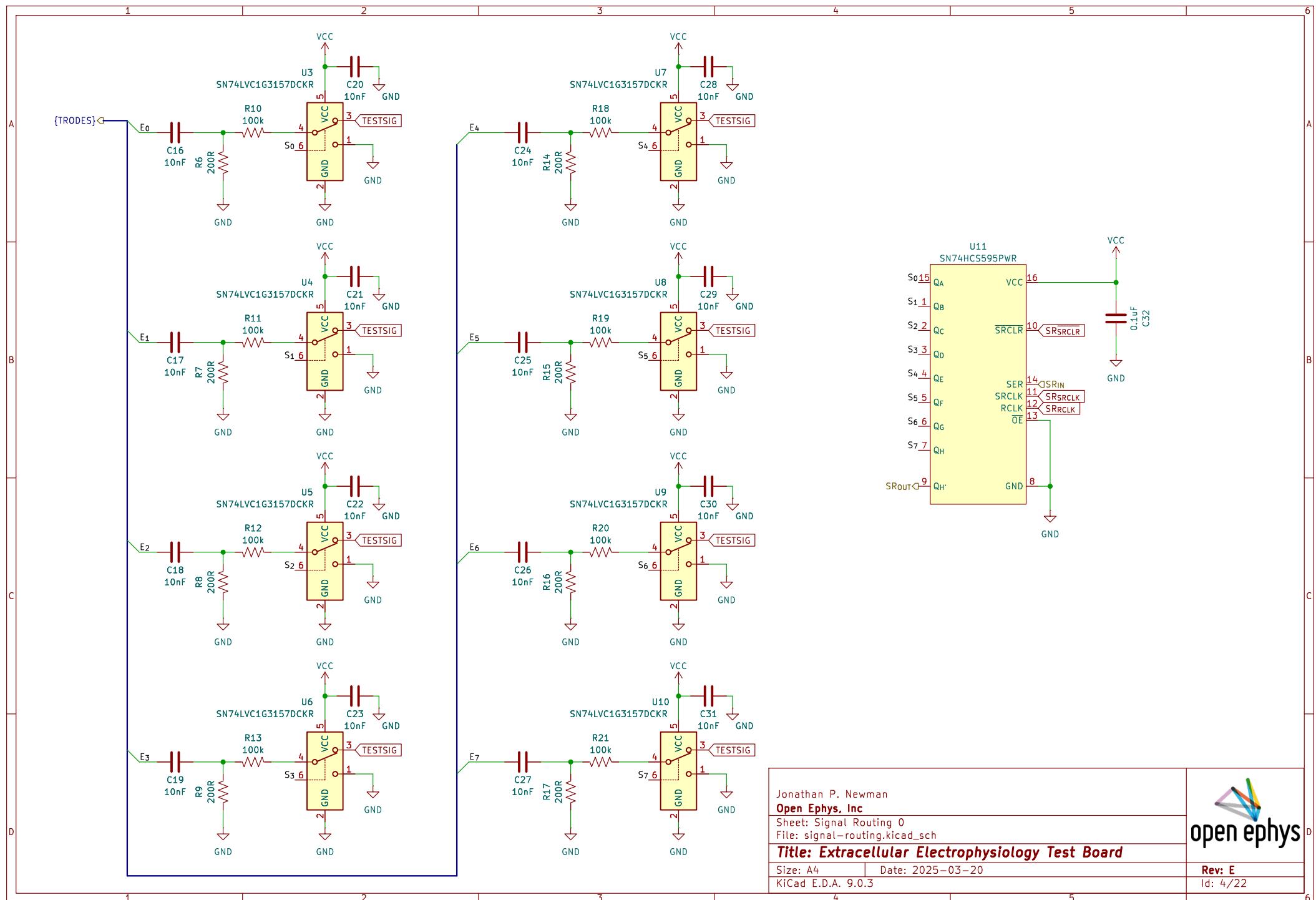
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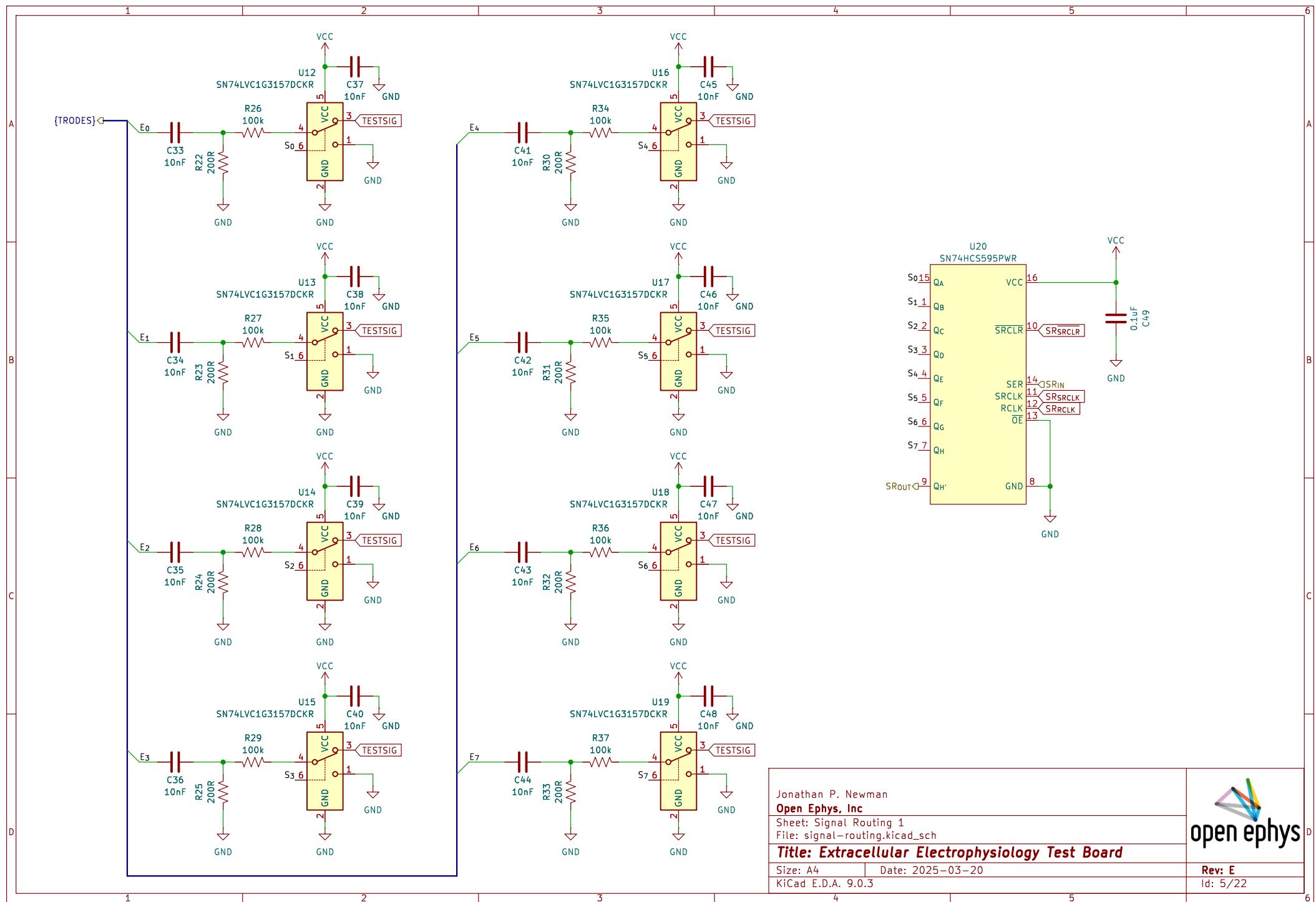
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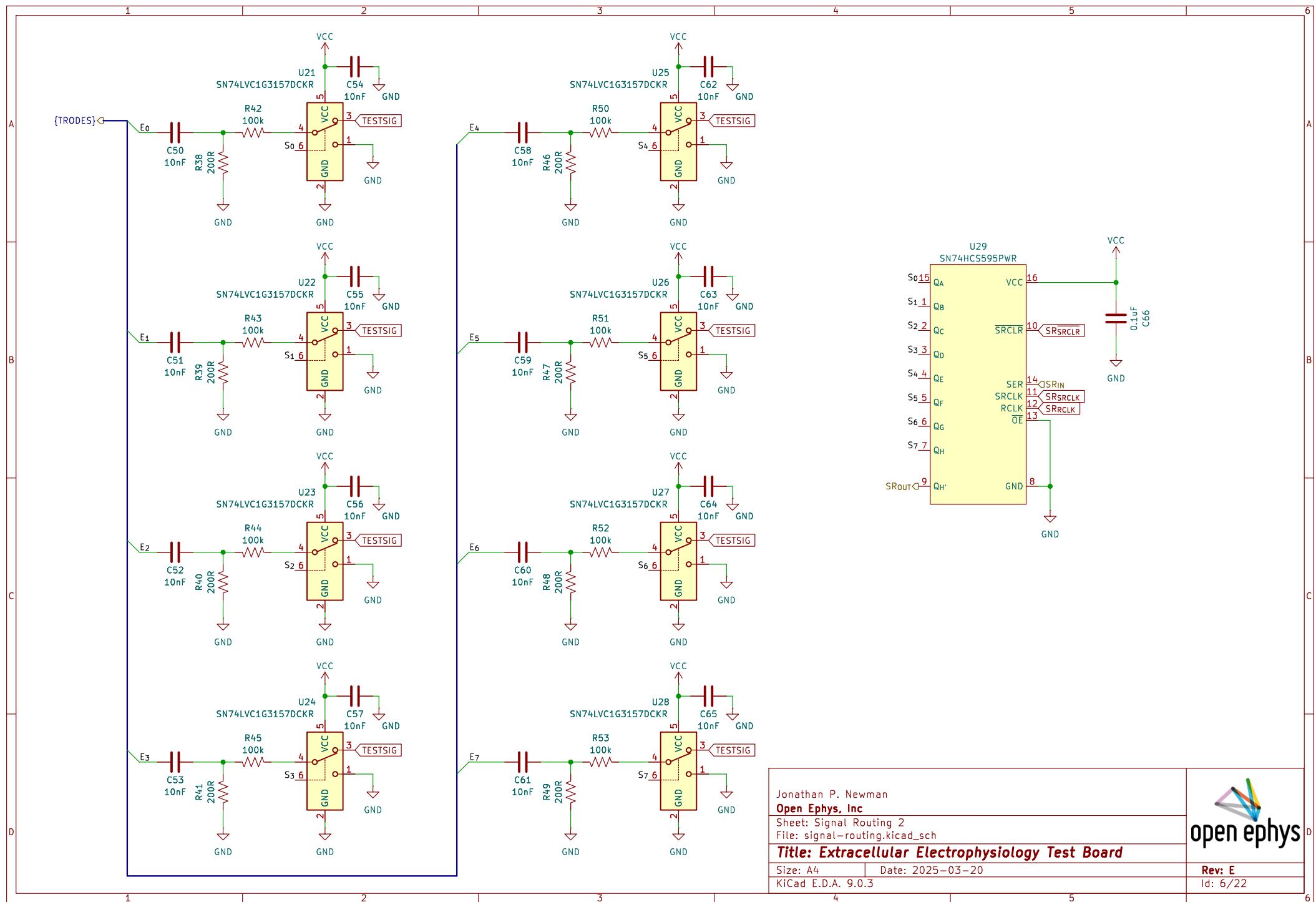
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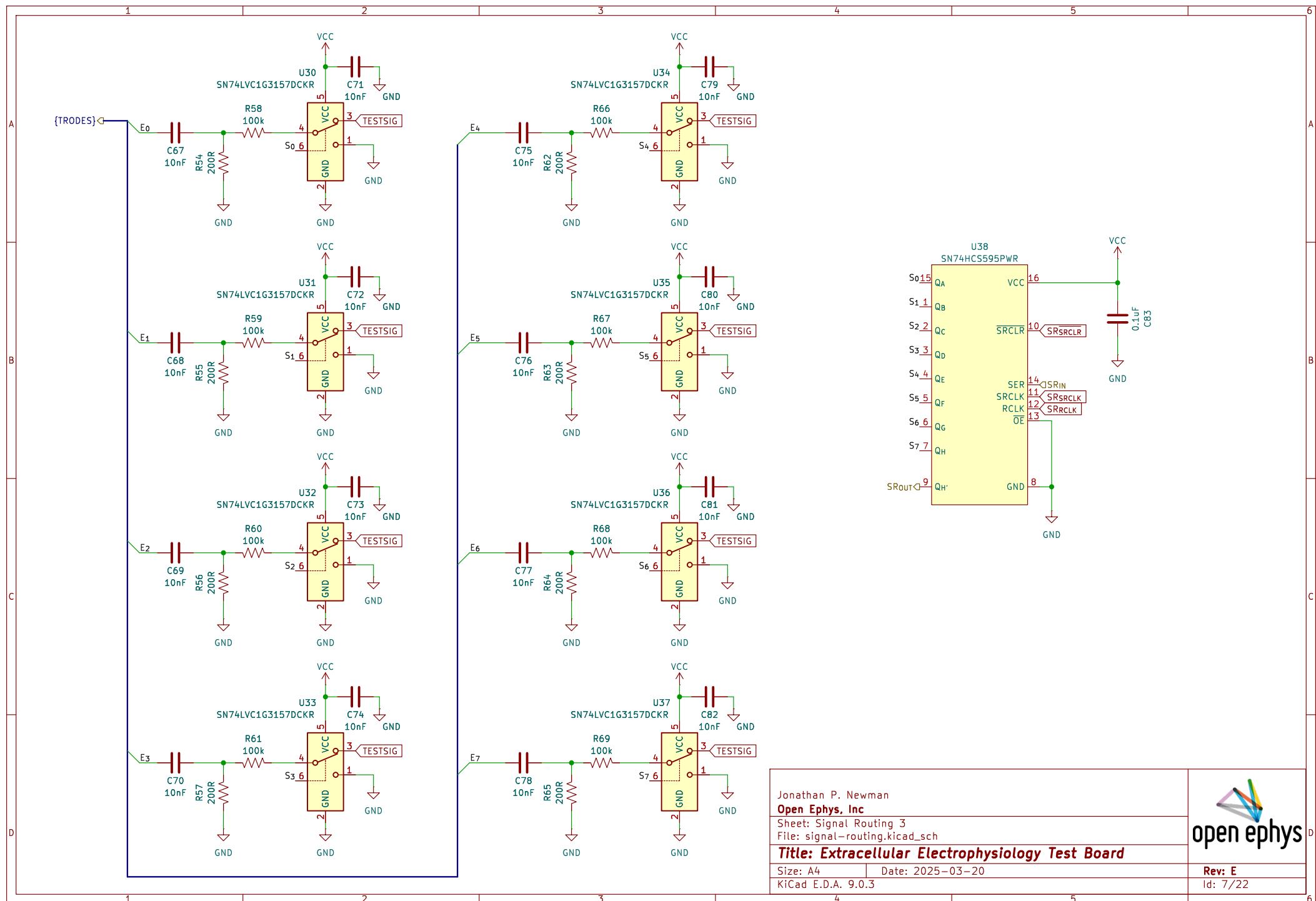
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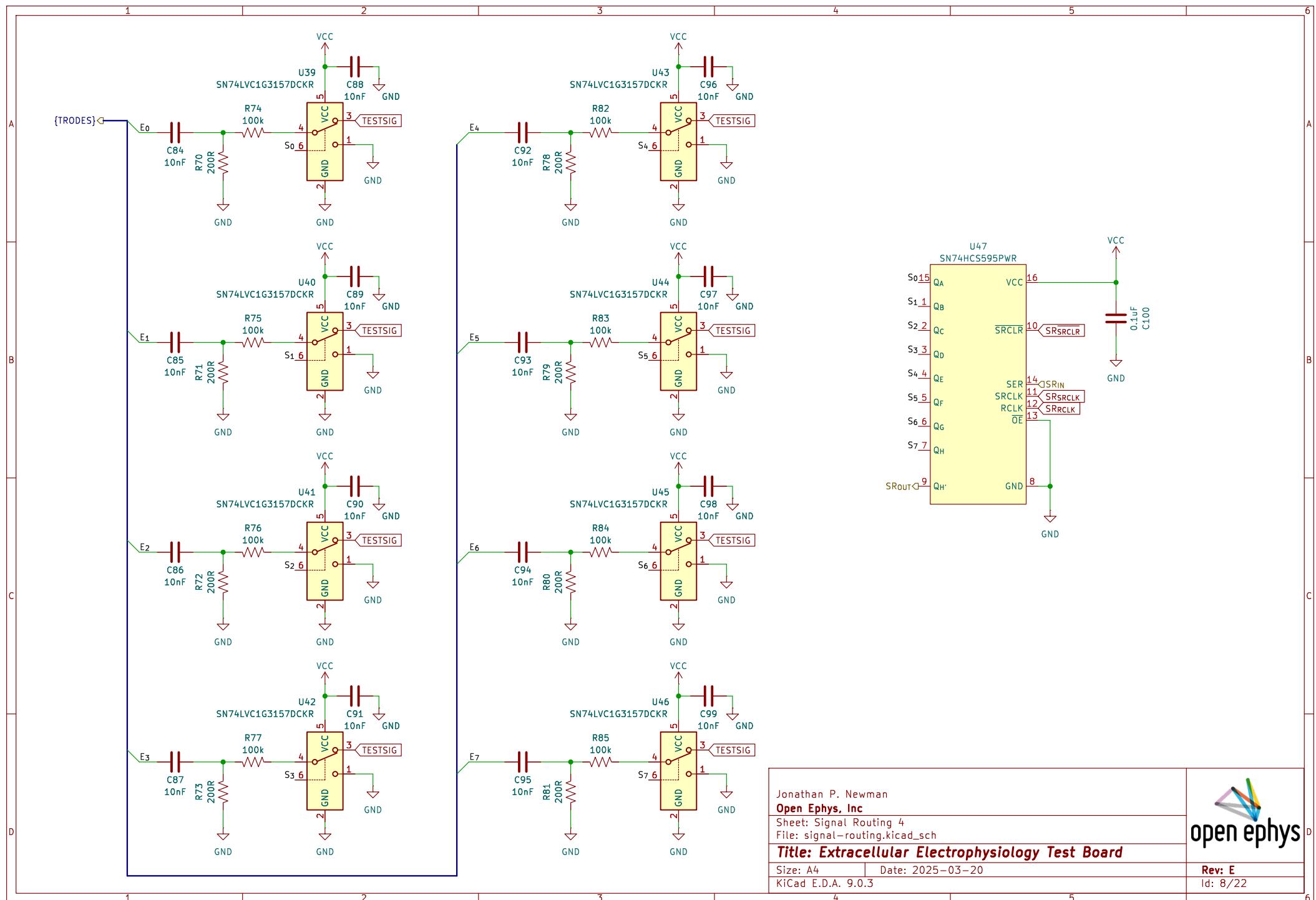
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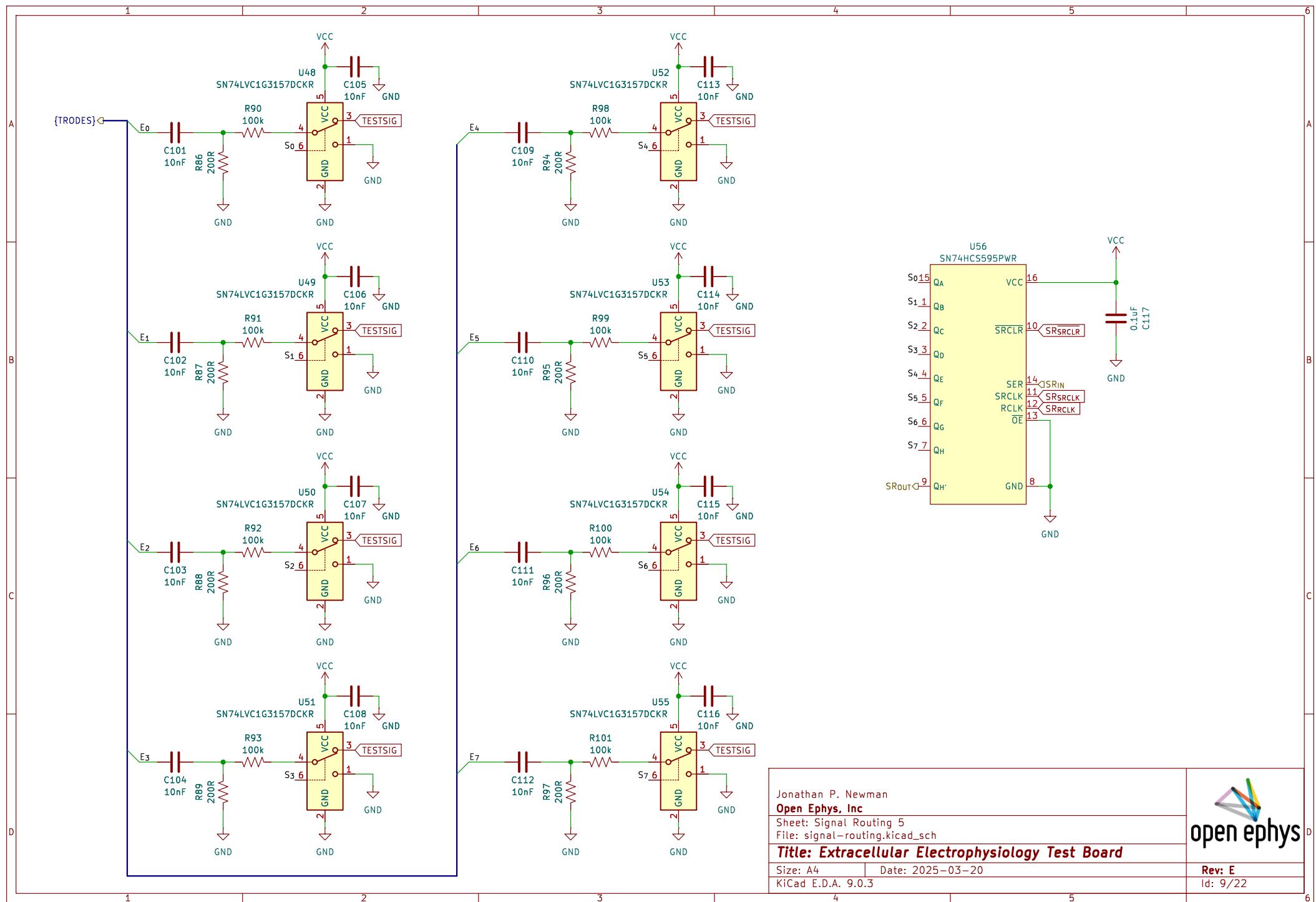
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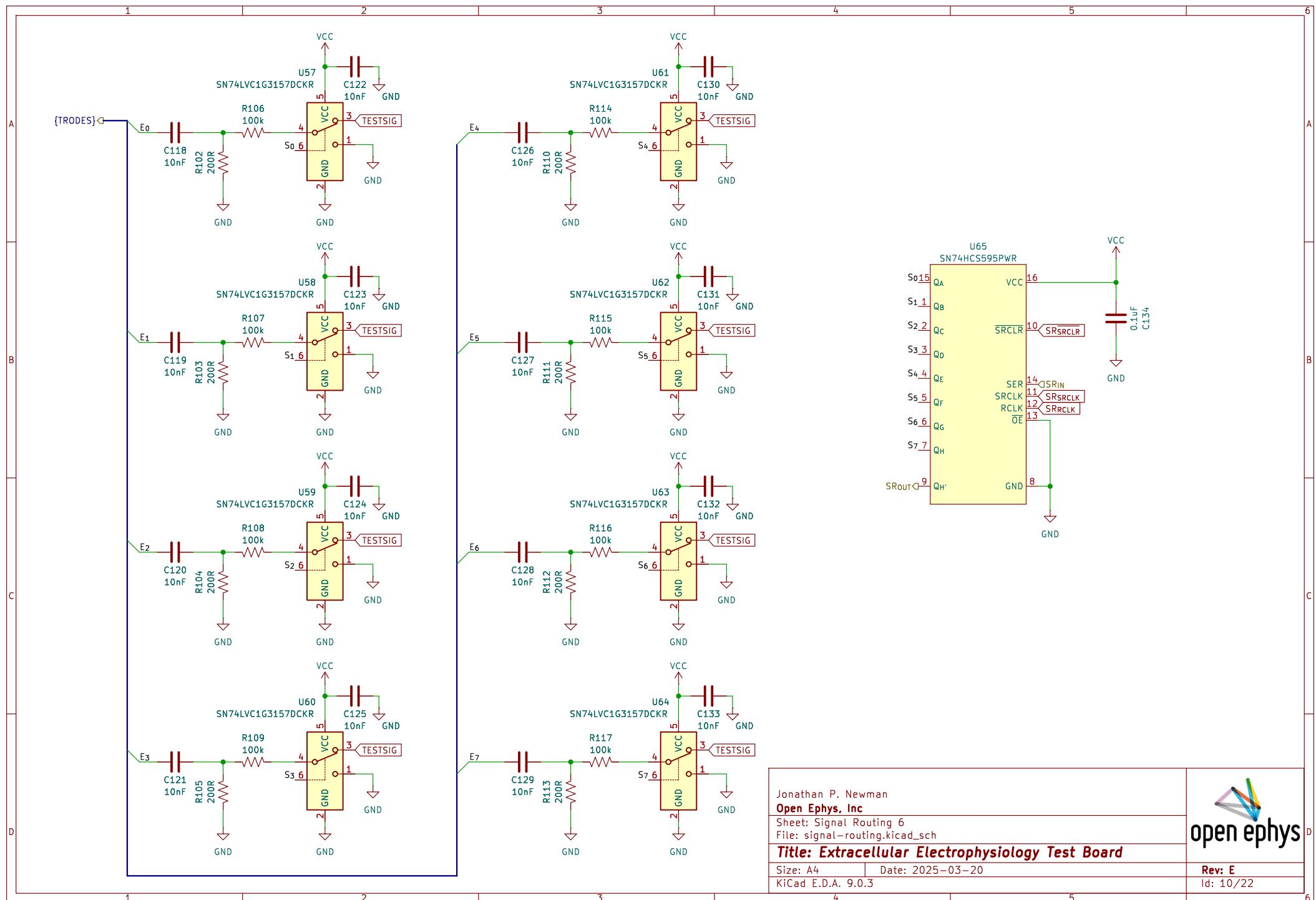
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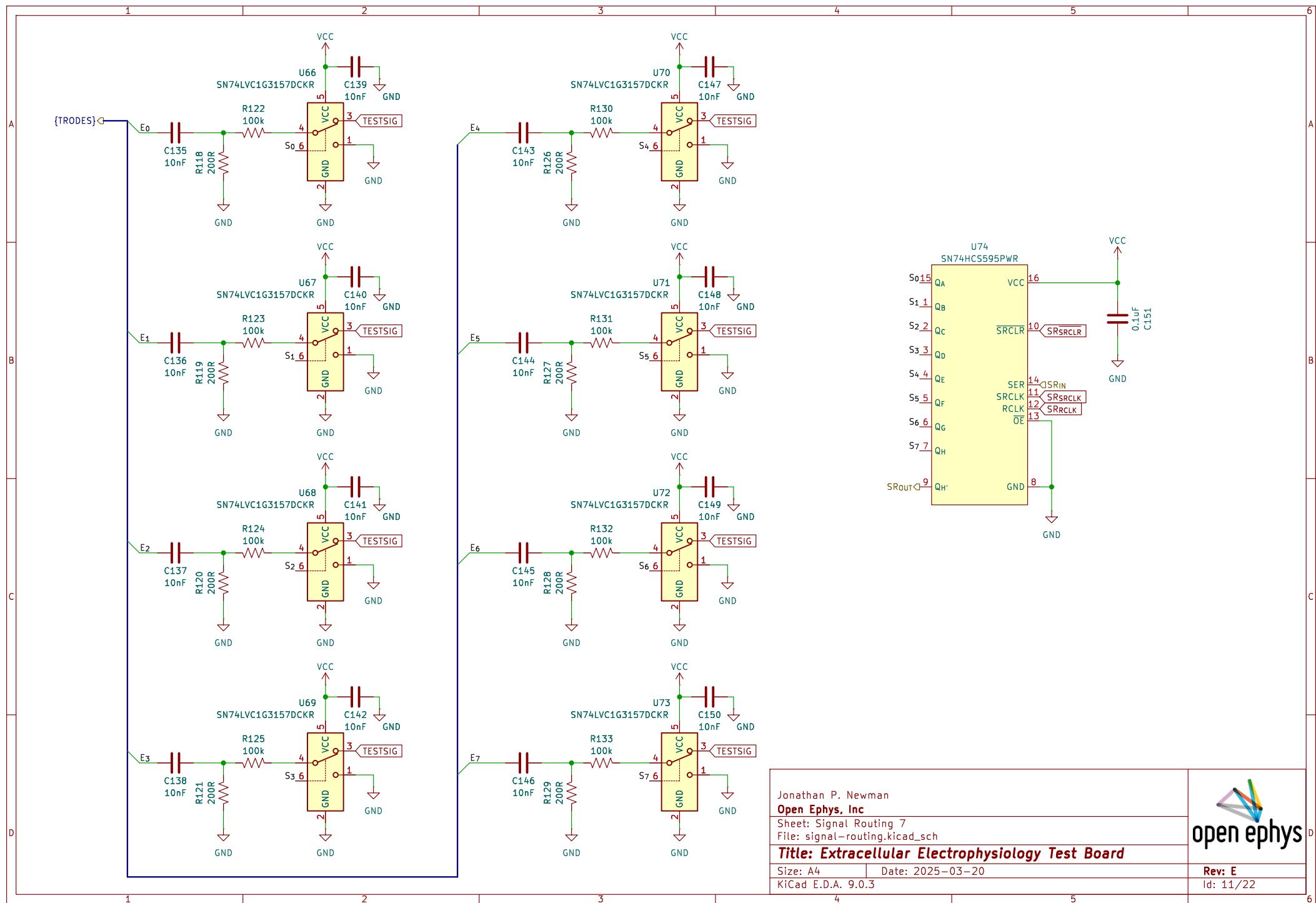
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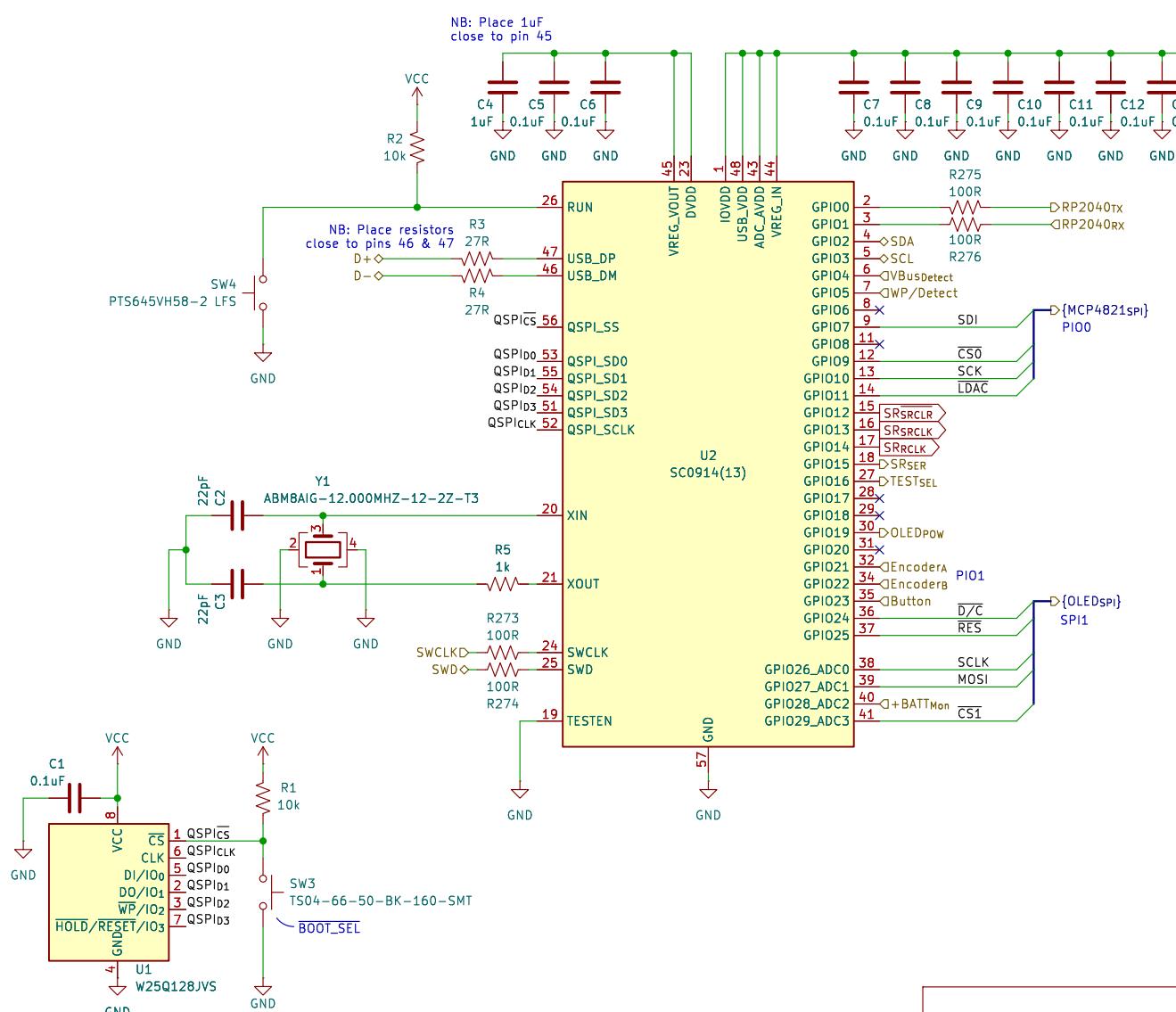
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1.4.3. GPIO Functions

Each individual GPIO pin can be connected to an internal peripheral via the GPIO functions defined below. Some internal peripheral connections appear in multiple places to allow some system level flexibility. SIO, PIO0 and PIO1 can connect to all GPIO pins and are controlled by software (or software controlled state machines) so can be used to implement many functions.

	Function								
GPIO	F1	F2	F3	F4	F5	F6	F7	F8	F9
0	SPI0_RX	UART0_RX	I2C0_SDA	PWM0_A	SIO	P100	P101		USB_OVCUR_DET
1	SPI0_CSH	UART0_RX	I2C0_SCL	PWM0_B	SIO	P100	P101		USB_VBUS_DET
2	SPI0_SCK	UART0_CTS	I2C1_SDA	PWM1_A	SIO	P100	P101		USB_VBUS_EN
3	SPI0_RX	UART0_RTS	I2C1_SCL	PWM1_B	SIO	P100	P101		USB_OVCUR_DET
4	SPI0_RX	UART1_RX	I2C0_SDA	PWM2_A	SIO	P100	P101		USB_VBUS_DET
5	SPI0_CSH	UART1_RX	I2C0_SCL	PWM2_B	SIO	P100	P101		USB_VBUS_DET
6	SPI0_SCK	UART1_CTS	I2C1_SDA	PWM3_A	SIO	P100	P101		USB_OVCUR_DET
7	SPI0_RX	UART1_RTS	I2C1_SCL	PWM3_B	SIO	P100	P101		USB_VBUS_DET
8	SPI1_RX	UART1_RX	I2C0_SDA	PWM4_A	SIO	P100	P101		USB_VBUS_EN
9	SPI1_CSH	UART1_RX	I2C0_SCL	PWM4_B	SIO	P100	P101		USB_OVCUR_DET
10	SPI1_SCK	UART1_CTS	I2C1_SDA	PWM5_A	SIO	P100	P101		USB_VBUS_DET
11	SPI1_RX	UART1_RTS	I2C1_SCL	PWM5_B	SIO	P100	P101		USB_VBUS_EN
12	SPI1_RX	UART0_RX	I2C0_SDA	PWM6_A	SIO	P100	P101		USB_OVCUR_DET
13	SPI1_CSH	UART0_RX	I2C0_SCL	PWM6_B	SIO	P100	P101		USB_VBUS_DET
14	SPI1_SCK	UART0_CTS	I2C1_SDA	PWM7_A	SIO	P100	P101		USB_VBUS_EN
15	SPI1_RX	UART0_RTS	I2C1_SCL	PWM7_B	SIO	P100	P101		USB_OVCUR_DET
16	SPI0_RX	UART0_RX	I2C0_SDA	PWM8_A	SIO	P100	P101		USB_VBUS_DET
17	SPI0_CSH	UART0_RX	I2C0_SCL	PWM8_B	SIO	P100	P101		USB_VBUS_DET
18	SPI0_SCK	UART0_CTS	I2C1_SDA	PWM1_A	SIO	P100	P101		USB_OVCUR_DET
19	SPI0_RX	UART0_RTS	I2C1_SCL	PWM1_B	SIO	P100	P101		USB_VBUS_DET
20	SPI0_RX	UART1_RX	I2C0_SDA	PWM2_A	SIO	P100	P101	CLOCK_GPIO0	USB_VBUS_EN
21	SPI0_CSH	UART1_RX	I2C0_SCL	PWM2_B	SIO	P100	P101	CLOCK_GPIO0	USB_OVCUR_DET
22	SPI0_SCK	UART1_CTS	I2C1_SDA	PWM3_A	SIO	P100	P101	CLOCK_GPIO1	USB_VBUS_DET
23	SPI0_RX	UART1_RTS	I2C1_SCL	PWM3_B	SIO	P100	P101	CLOCK_GPIO1	USB_VBUS_DET
24	SPI1_RX	UART1_RX	I2C0_SDA	PWM4_A	SIO	P100	P101	CLOCK_GPIO2	USB_OVCUR_DET
25	SPI1_CSH	UART1_RX	I2C0_SCL	PWM4_B	SIO	P100	P101	CLOCK_GPIO3	USB_VBUS_DET
26	SPI1_SCK	UART1_CTS	I2C1_SDA	PWM5_A	SIO	P100	P101		USB_VBUS_EN
27	SPI1_RX	UART1_RTS	I2C1_SCL	PWM5_B	SIO	P100	P101		USB_OVCUR_DET
28	SPI1_RX	UART0_RX	I2C0_SDA	PWM6_A	SIO	P100	P101		USB_VBUS_DET
29	SPI1_CSH	UART0_RX	I2C0_SCL	PWM6_B	SIO	P100	P101		USB_VBUS_DET

Table 2 from Section 1.4.3, GPIO Functions, page 13

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The logo for open ephys, featuring a stylized 'N' shape composed of three colored sticks (purple, yellow, and blue) above the word "open ephys" in a lowercase sans-serif font.

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ANSWER

RP2040 hardware design guide:
<https://datasheets.raspberrypi.com/rp2040/hardware-design-with-rp2040.pdf>

1 2 3 4 5 6

A

A

B

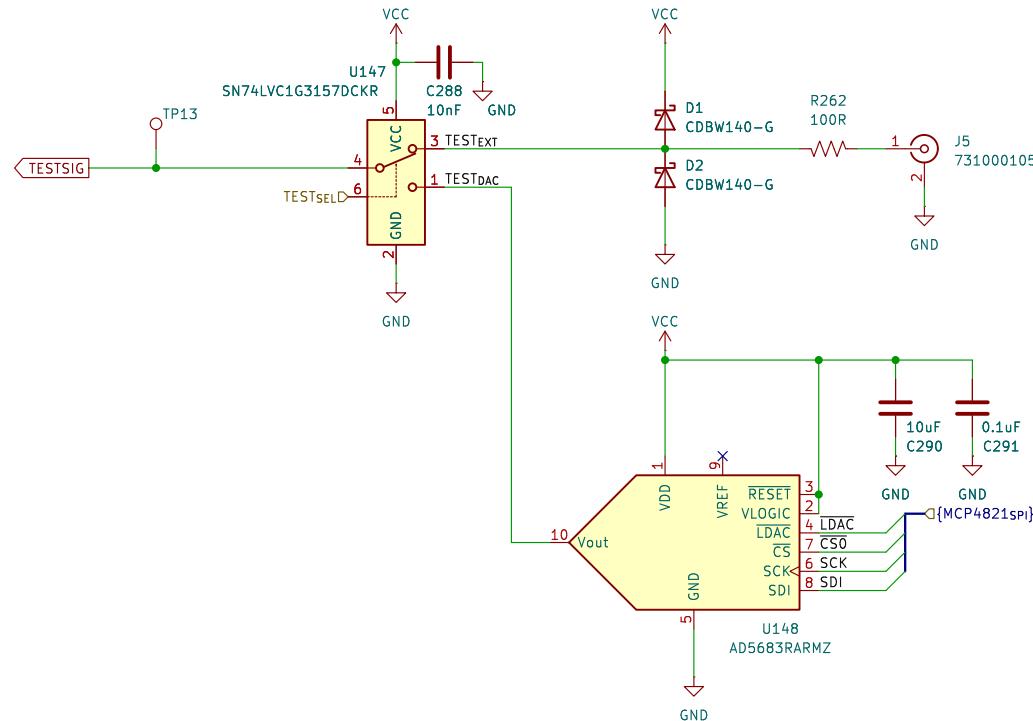
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C

C

D

D



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Size: A4 Date:
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1 2 3 4 5 6

