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November 2013

FCD600N60Z

N-Channel SuperFET[®] II MOSFET 600 V, 7.4 A, 600 m Ω

Features

- 650 V @ T_{.1} = 150°C
- Typ. $R_{DS(on)}$ = 510 m Ω
- Ultra Low Gate Charge (Typ. Q_q = 20 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 74 pF)
- · 100% Avalanche Tested
- · ESD Improved Capacity
- RoHS Compliant

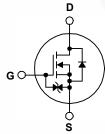
Applications

- · LCD / LED / PDP TV and Monitor Lighting
- · Solar Inverter
- · AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCD600N60Z	Unit
V _{DSS}	Drain to Source Voltage			600	V
	Cata to Course Voltage	- DC		±20	V
V _{GSS} Gate to Source Voltage	- AC	(f > 1 Hz)	±30	V	
	Drain Current	- Continuous (T _C = 25°C)		7.4	А
Lirain Current		- Continuous (T _C = 100°C)		4.7	A
DM	Drain Current	- Pulsed	(Note 1)	22.2	Α
AS	Single Pulsed Avalanche Energy (Note 2)			135	mJ
AR	Avalanche Current (Note 1)		1.5	Α	
= AR	Repetitive Avalanche Energy (Note 1)		0.89	mJ	
dv/dt	MOSFET dv/dt			100	V/ns
av/at	Peak Diode Recovery dv/dt		(Note 3)	20	V/IIS
.	Dower Dissipation	(T _C = 25°C)		89	W
P_{D}	Power Dissipation - Derate Above 25°C			0.71	W/°C
Γ _J , T _{STG}	Operating and Storage Temp	erature Range		-55 to +150	°C
T _I	Maximum Lead Temperature	for Soldering, 1/8" from Case for 5	Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FCD600N60Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 100		*C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD600N60Z	FCD600N60Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
D\/	Drain to Course Prockdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
BV _{DSS} Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V	
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
BV _{DS}	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 7.4 \text{ A}$	-	700	-	٧
1	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	5	
IDSS	Zero Gate Voltage Drain Guirent	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	20	μΑ
I _{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	uA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.7 \text{ A}$	-	0.51	0.6	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 3.7 A	_	6.7	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 25 V V - 0 V	- \	840	1120	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	- \	630	840	pF
C _{rss}	Reverse Transfer Capacitance	1 = 1 Wil 12	-	30	45	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	16.5	-	pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0 V \text{ to } 480 V, V_{GS} = 0 V$	-	74	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 3.7 A,	-	20	26	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	3.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	7.5	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	- /	2.89	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	13	36	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_{D} = 3.7 \text{ A},$	-	7	24	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	39	88	ns
t _f	Turn-Off Fall Time	(Note 4)	-	9	28	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diod	Maximum Continuous Drain to Source Diode Forward Current		-	7.4	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	22.2	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 3.7 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 3.7 A,	-	200	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	2.3	\\ -	μС

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. I_{AS} = 1.5 A, V_{DD} = 50 V, R_{G} = 25 Ω_{r} starting T_{J} = 25°C.
- 3. I $_{SD}$ \leq 3.7 A, di/dt \leq 200 A/ μ s, V $_{DD}$ \leq BV $_{DSS}$, starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

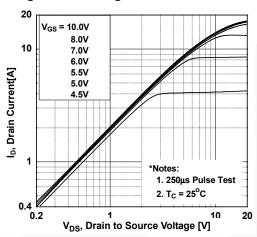


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

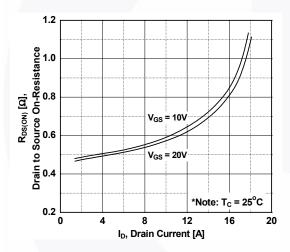


Figure 5. Capacitance Characteristics

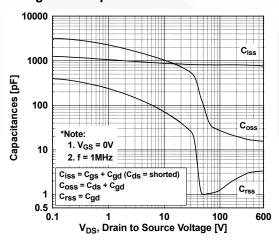


Figure 2. Transfer Characteristics

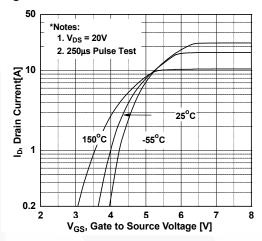


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

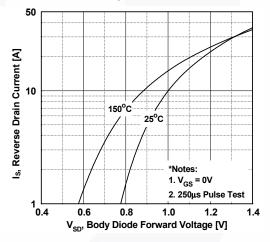
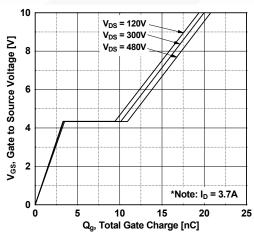


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

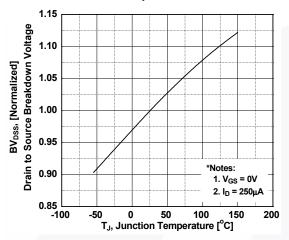


Figure 9. Maximum Safe Operating Area

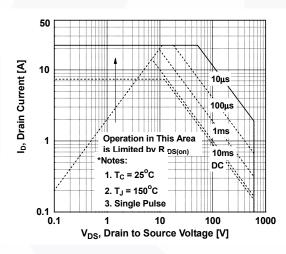


Figure 11. Eoss vs. Drain to Source Voltage

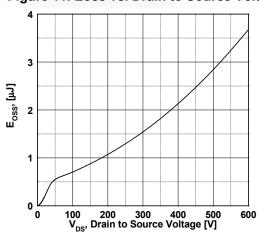


Figure 8. On-Resistance Variation vs. Temperature

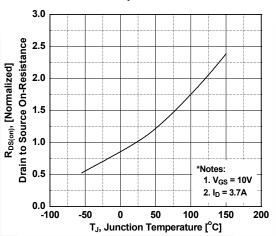
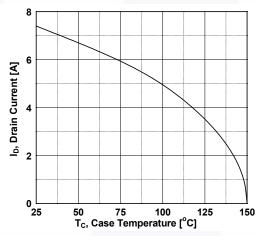
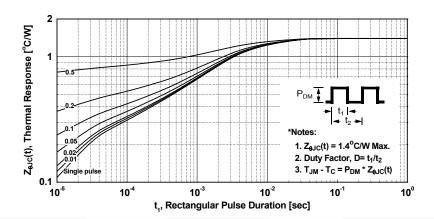


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



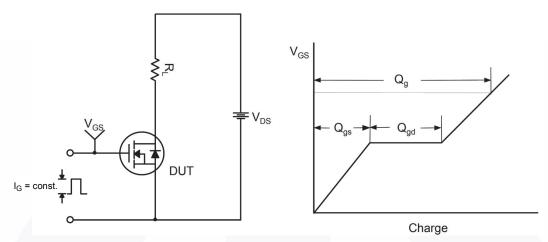


Figure 13. Gate Charge Test Circuit & Waveform

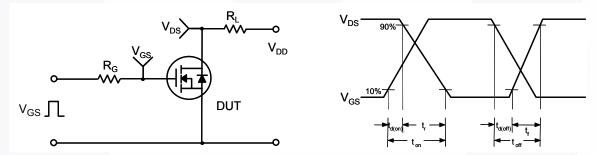


Figure 14. Resistive Switching Test Circuit & Waveforms

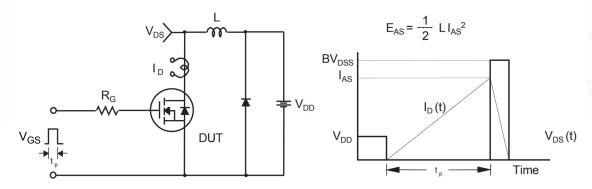


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

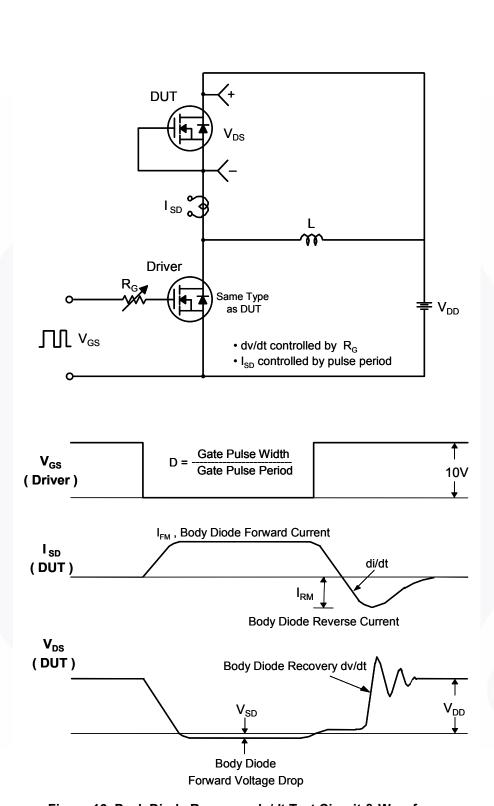


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

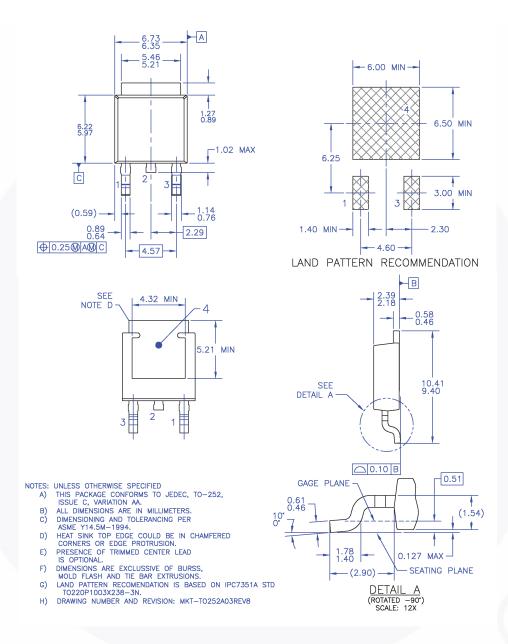


Figure 17. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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No Identification Needed Full Production		Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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