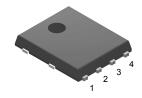


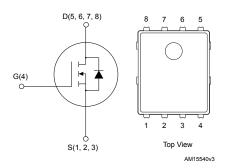


Automotive N-channel 100 V, 4.6 m Ω max., 125 A STripFET F8 Power MOSFET in a PowerFLAT 5x6 package

Features



PowerFLAT 5x6



Order code	V _{DS}	R _{DS(on)} max.	l _D
STL125N10F8AG	100 V	4.6 mΩ	125 A



- AEC-Q101 qualified
- MSL1 grade
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Low gate charge Q_q
- · Wettable flank package

Applications

- Automotive motor control
- Electro mobility

Description

The STL125N10F8AG is a 100 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure.

It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.





Product status link

STL125N10F8AG

Product summary			
Order code	STL125N10F8AG		
Marking ⁽¹⁾	125N10F8		
Package	PowerFLAT 5x6		
Packing	Tape and reel		

 For engineering samples marking, see Section 3.3: PowerFLAT 5x6 marking information.



1 Electrical ratings

Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
	Drain current (continuous) at T _C = 25 °C ⁽³⁾	125	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C ⁽³⁾	88	Α
	Drain current (continuous) at T _C = 25 °C ⁽²⁾	120	-
I _{DM} ⁽¹⁾⁽³⁾⁽⁴⁾	Drain current (pulsed), t _P = 10 μs	500	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	150	W
I _{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	60	Α
E _{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = 60 A, R_G = 25 Ω)	140	mJ
TJ	Operating junction temperature range	-55 to 175	°C
T _{stg}	Storage temperature range	-33 (0 175	°C

- 1. Specified by design, not tested in production.
- 2. This current value is limited by package.
- 3. This is the theoretical current value only related to the silicon.
- 4. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	16.2	°C/W
R _{thJC}	Thermal resistance, junction-to-case	1.0	°C/W

1. Defined according to JEDEC standards (JESD51-5, -7).

DS14553 - Rev 4 page 2/15



2 Electrical characteristics

 T_J = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	100			V
I	Zana mata waltana dunin awanat	V _{DS} = 100 V, V _{GS} = 0 V			1	
I _{DSS}	Zero gate voltage drain current	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 60 A		3.6	4.6	mΩ

^{1.} Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} ⁽¹⁾	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V		3600	-	pF
C _{oss} ⁽¹⁾	Output capacitance			840	-	pF
C _{rss} ⁽¹⁾	Reverse transfer capacitance		-	25	-	pF
Q _g ⁽¹⁾	Total gate charge		-	56	-	nC
Q _{gs} ⁽¹⁾	Gate-source charge	V_{DD} = 50 V, I_{D} = 120 A, V_{GS} = 0 to 10 V	-	17	-	nC
Q _{gd} ⁽¹⁾	Gate-drain charge		-	15	-	nC

^{1.} Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} ⁽¹⁾	Turn-on delay time		-	17	-	ns
t _r ⁽¹⁾	Rise time	$V_{DD} = 50 \text{ V}, I_D = 60 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	16	-	ns
t _{d(off)} ⁽¹⁾	Turn-off delay time		-	41	-	ns
t _f ⁽¹⁾	Fall time		-	17	-	ns

^{1.} Specified by design and evaluated by characterization, not tested in production.

DS14553 - Rev 4 page 3/15



Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾⁽²⁾	Forward on current (continuous)	T _C = 25 °C	-		100	Α
V _{SD}	Forward on voltage	I _{SD} = 60 A, V _{GS} = 0 V	-		1.2	V
t _{rr} ⁽¹⁾	Reverse recovery time		-	67		ns
Q _{rr} ⁽¹⁾	Reverse recovery charge	$I_D = 60 \text{ A}, \text{ di/dt} = 100 \text{ A/µs}, V_{DD} = 80 \text{ V}$	-	127		nC
I _{RRM} ⁽¹⁾	Reverse recovery current		-	3.7		Α

^{1.} Specified by design and evaluated by characterization, not tested in production.

DS14553 - Rev 4 page 4/15

^{2.} This is the theoretical current value only related to the silicon.



2.1 Electrical characteristics (curves)

Figure 1. Total power dissipation

PTOT GADG021120221356TPD
[W]
140
120
100
80
60
40
20
0 25 50 75 100 125 150 175 Tc [°C]

Figure 2. Drain current vs case temperature

GADG021120221400DTC

[A]

120

100

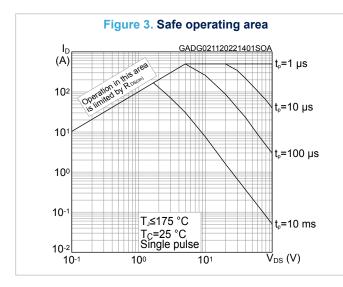
80

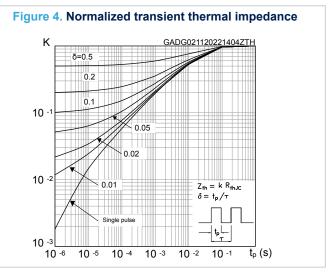
60

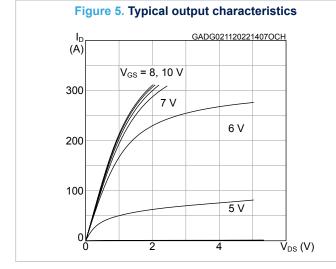
40

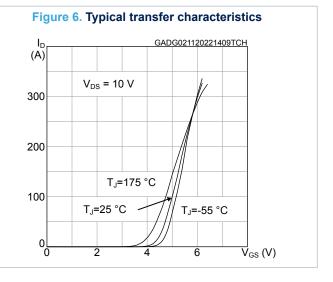
20

0 25 50 75 100 125 150 175 Tc [°C]









DS14553 - Rev 4 page 5/15



Figure 7. Typical on-resistance vs gate-source voltage

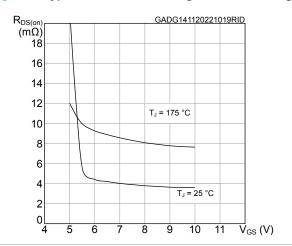


Figure 8. Typical gate charge characteristics

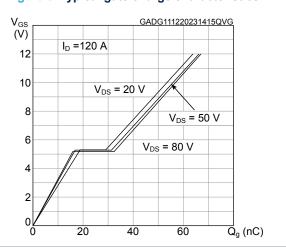


Figure 9. Typical capacitance characteristics

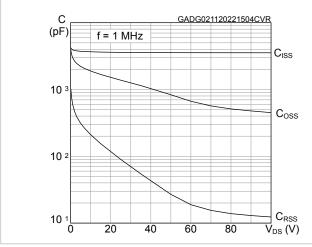


Figure 10. Avalanche characteristics

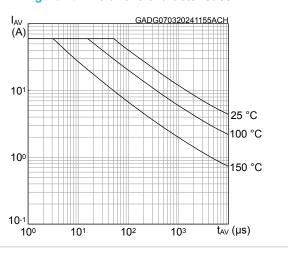


Figure 11. Avalanche energy

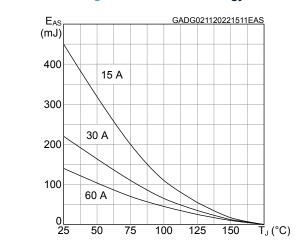
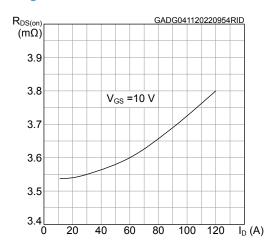


Figure 12. Static drain-source on-resistance



DS14553 - Rev 4 page 6/15



Figure 13. Normalized on-resistance vs temperature

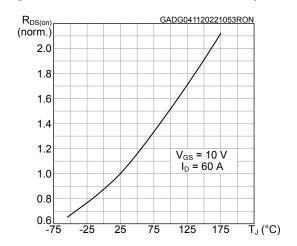


Figure 14. Normalized gate threshold voltage vs temperature

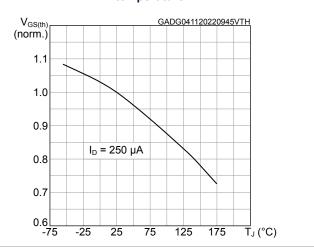


Figure 15. Typical reverse diode forward characteristics

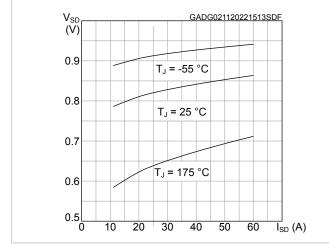
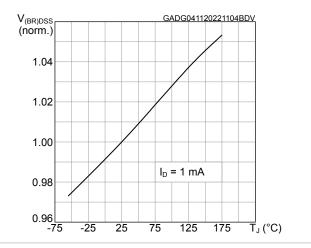


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature



DS14553 - Rev 4 page 7/15

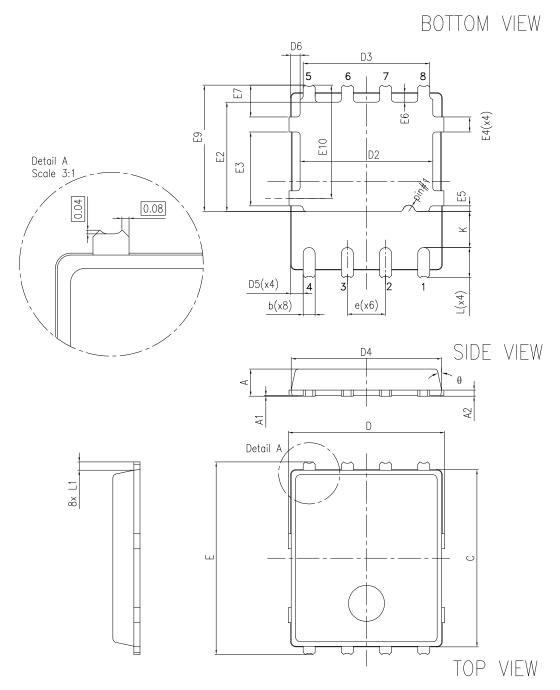


3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerFLAT 5x6 WF type C package information

Figure 17. PowerFLAT 5x6 WF type C package outline



8231817_WF_typeC_r23

DS14553 - Rev 4 page 8/15



Table 7. PowerFLAT 5x6 WF type C mechanical data

Dim.		mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.00		0.05
A2		0.25	
b	0.30		0.50
С	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
е		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

DS14553 - Rev 4 page 9/15



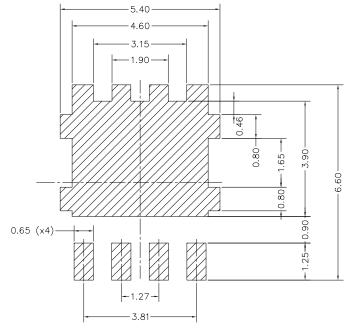
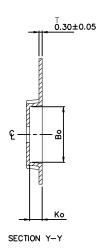


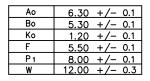
Figure 18. PowerFLAT 5x6 recommended footprint (dimensions are in mm)

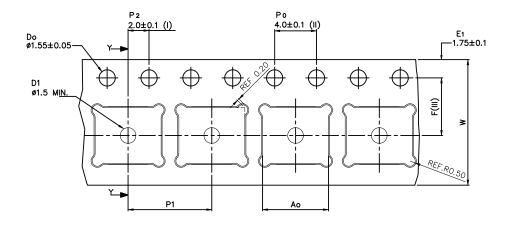
8231817_FOOTPRINT_rev23

3.2 PowerFLAT 5x6 packing information

Figure 19. PowerFLAT 5x6 tape (dimensions are in mm)







(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs All dimensions are in millimeters

8234350_Tape_rev_C

DS14553 - Rev 4 page 10/15



Figure 20. PowerFLAT 5x6 package orientation in carrier tape

Pin 1 identification

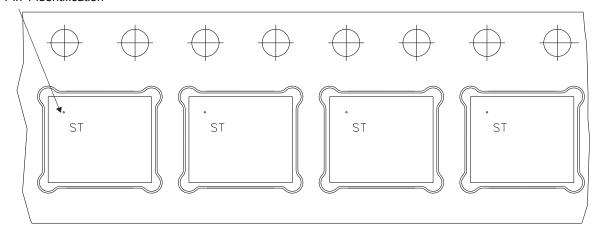
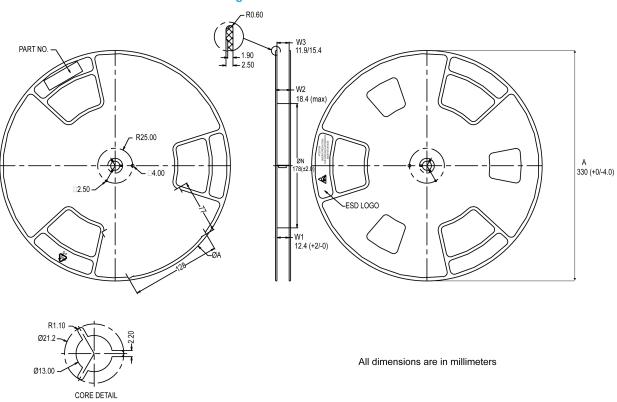


Figure 21. PowerFLAT 5x6 reel



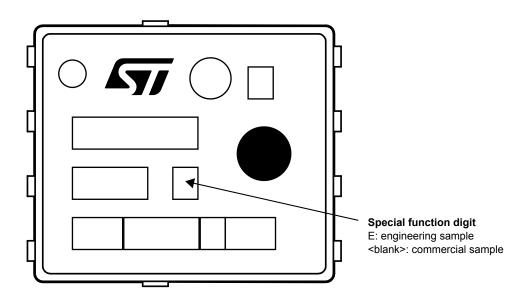
8234350_Reel_rev_C

DS14553 - Rev 4 page 11/15



3.3 PowerFLAT 5x6 marking information

Figure 22. PowerFLAT 5x6 marking information



Note:

Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

DS14553 - Rev 4 page 12/15



Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Dec-2023	1	First release.
11-Mar-2024	2	Updated Figure 10. Avalanche characteristics.
06-May-2024	3	Updated Section PowerFLAT 5x6 single island WF cover image.
10-May-2024	4	Updated Section Internal schematic.

DS14553 - Rev 4 page 13/15



page 14/15



Contents

1	Elec	trical ratingstrical ratings	2
2		etrical characteristics	
	2.1	Electrical characteristics (curves)	5
3	Pacl	kage information	8
	3.1	PowerFLAT 5x6 WF type C package information	8
	3.2	PowerFLAT 5x6 packing information	10
	3.3	PowerFLAT 5x6 marking information	12
Rev	ision	history	13

DS14553 - Rev 4



IMPORTANT NOTICE - READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved

DS14553 - Rev 4 page 15/15