MOSFET – Power, Single, N-Channel

100 V, 27 mΩ, 29 A

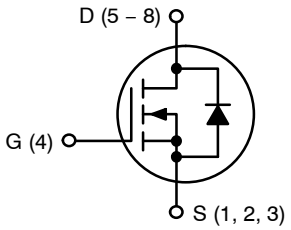
NVTYS027N10MCL

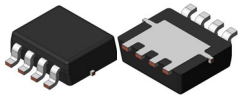
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	27 mΩ @ 10 V	29 A
	32.8 mΩ @ 4.5 V	

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

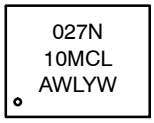
N−Channel





LFPAK8
3.3x3.3
CASE 760AD

MARKING DIAGRAM



027N10MCL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	29	A
		T_C = 100°C		21	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	T_C = 25°C	P_D	51	W
		T_C = 100°C		26	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	7	A
		T_A = 100°C		5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.2	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs		I_{DM}	128	A
Source Current (Body Diode)			I_S	39.5	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 1.5 A)			E_{AS}	174	mJ
Lead Temperature for Soldering Purposes (1/8″ from Case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	3	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			–	73.2	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C	–	–	1.0	μA
			T_J = 125°C	–	–	250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V		–	–	100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 45 μA		1.0	1.7	3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			–	−6.23	–	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 8 A	–	19.1	27	mΩ
		V_{GS} = 4.5 V	I_D = 6 A	–	26.9	32.8	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 7 A		–	18.3	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V		–	856	–	pF
Output Capacitance	C_{OSS}			–	309	–	
Reverse Transfer Capacitance	C_{RSS}			–	4.4	–	
Gate Resistance	R_G	f = 1 MHz		–	0.52	–	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 80 V; I_D = 8 A		–	5.6	–	nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 80 V; I_D = 8 A		–	11.8	–	
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 80 V; I_D = 8 A		–	1.3	–	nC
Gate−to−Source Charge	Q_{GS}			–	2.2	–	
Gate−to−Drain Charge	Q_{GD}			–	1.4	–	
Plateau Voltage	V_{GP}			–	2.8	–	V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 80 V, I_D = 6 A, R_G = 6 Ω		–	11.5	–	ns
Rise Time	t_r			–	6.7	–	
Turn−Off Delay Time	$t_{d(OFF)}$			–	14.2	–	
Fall Time	t_f			–	6.5	–	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 8 A	T_J = 25°C	–	0.85	1.25	V
			T_J = 125°C	–	0.72	–	
Reverse Recovery Time	t_{RR}	I_F = 8 A, di/dt = 100 A/μs		–	29.5	–	ns
Charge Time	t_a			–	14.6	–	ns
Discharge Time	t_b			–	15.2	–	ns
Reverse Recovery Charge	Q_{RR}			–	18.9	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

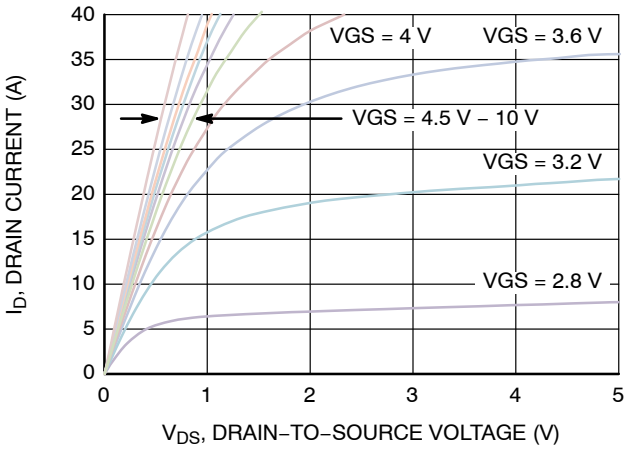


Figure 1. On–Region Characteristics

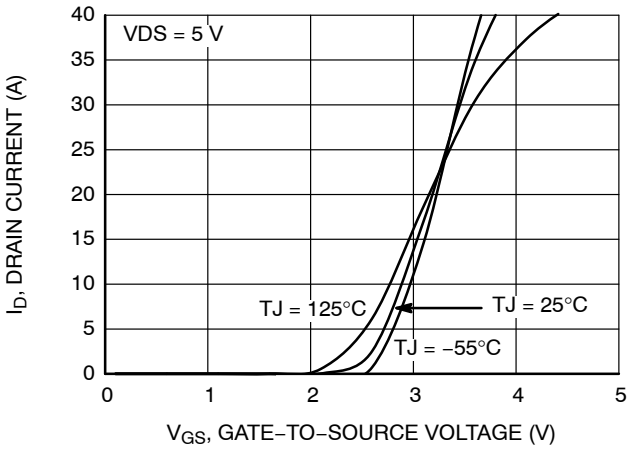


Figure 2. Transfer Characteristics

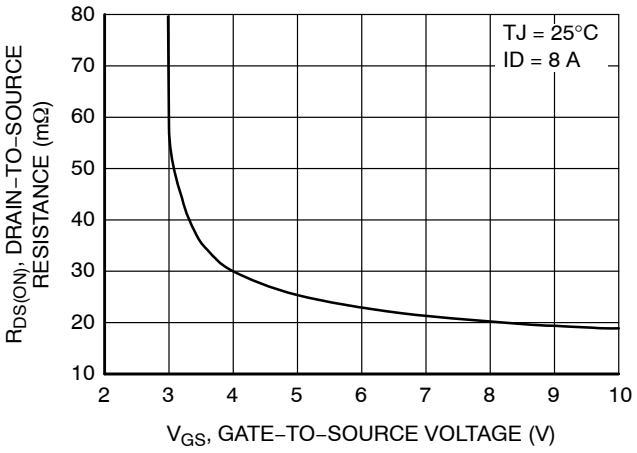


Figure 3. On–Resistance vs. Gate–to–Source Voltage

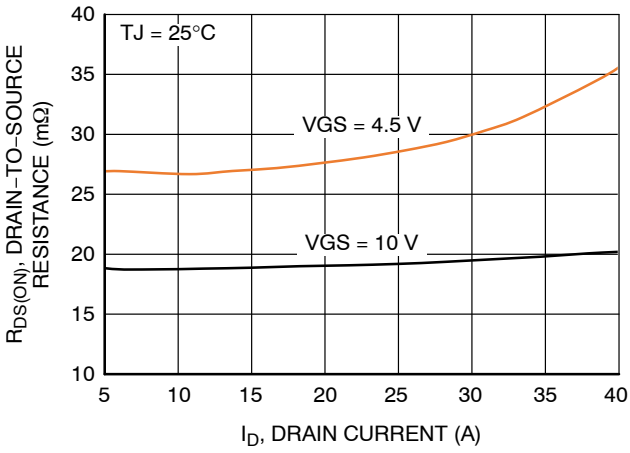


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

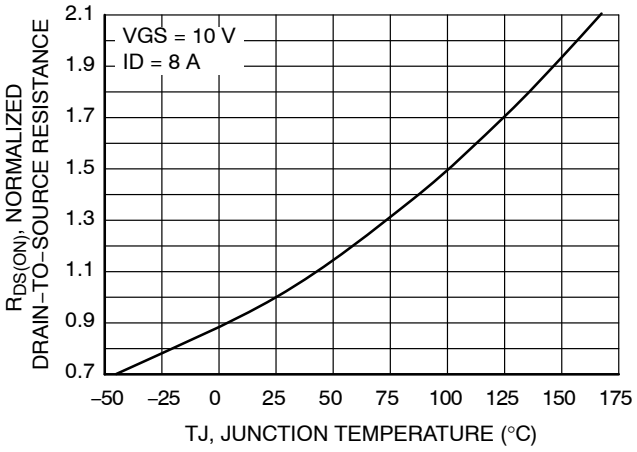


Figure 5. On–Resistance Variation with Temperature

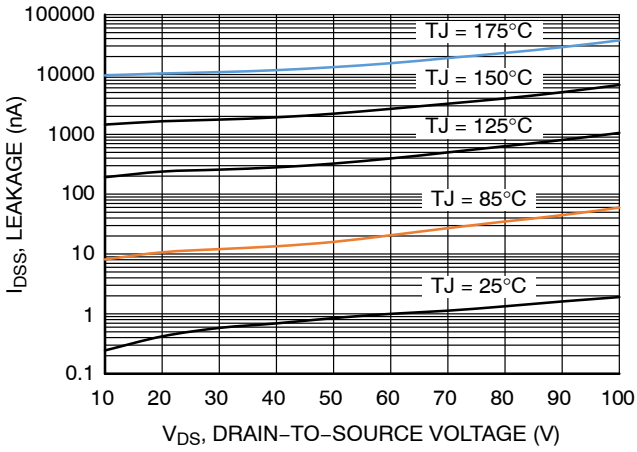


Figure 6. Drain–to–Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

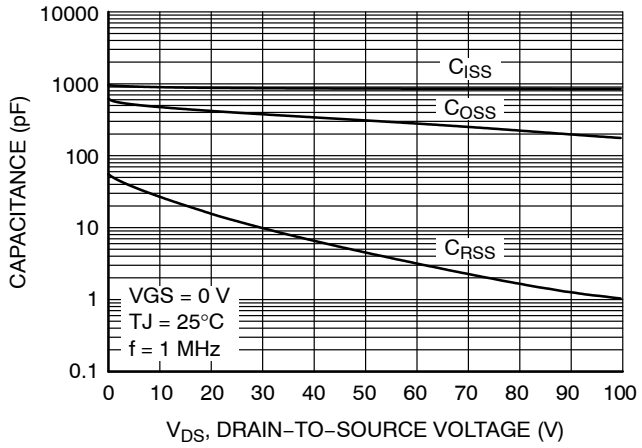


Figure 7. Capacitance Variation

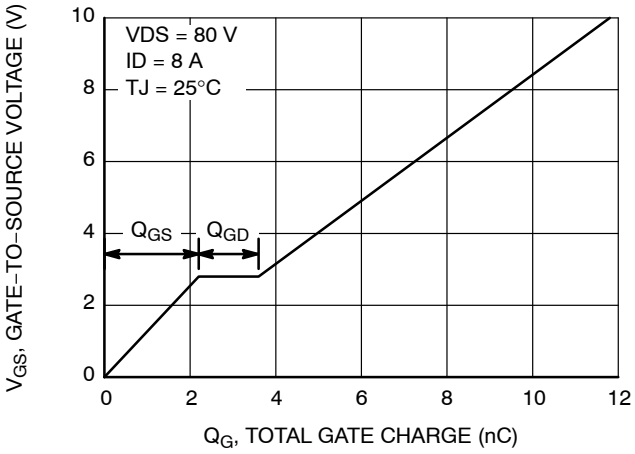


Figure 8. Gate−to−Source vs. Total Charge

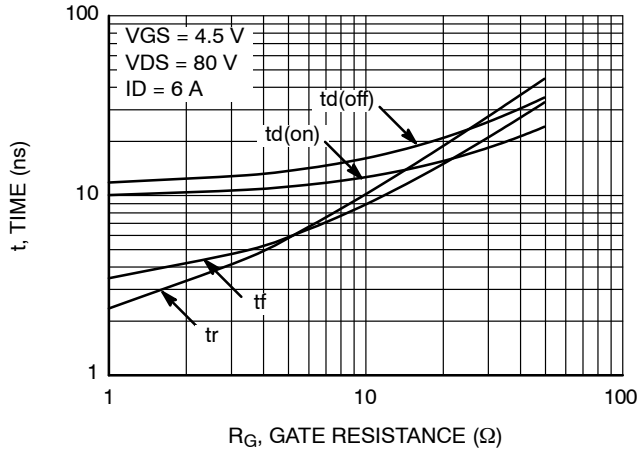


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

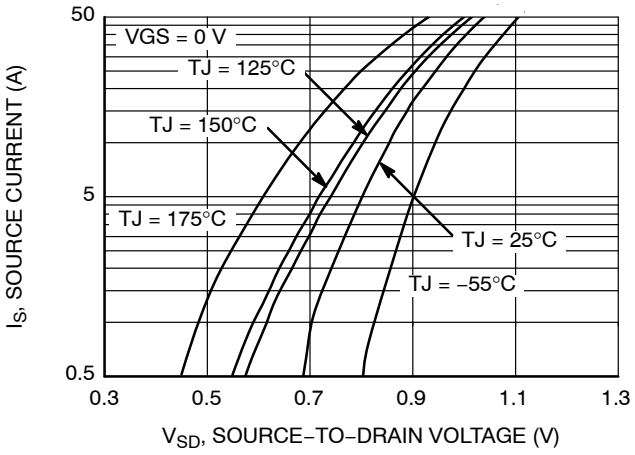


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

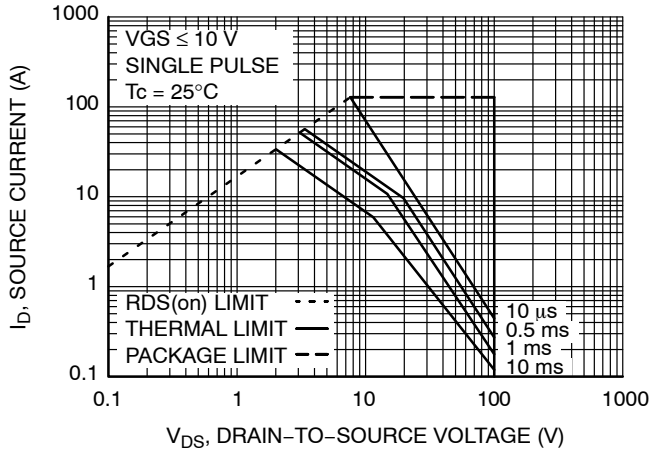


Figure 11. Maximum Rated Forward Biased Safe Operating Area

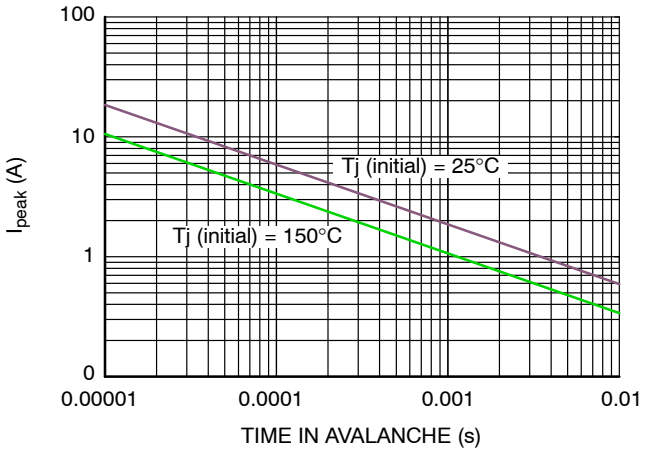


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

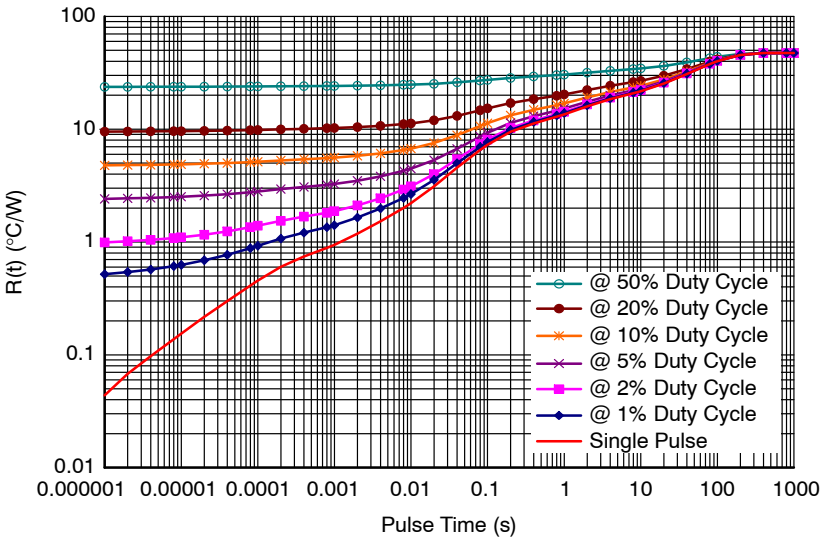
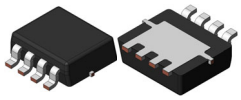


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

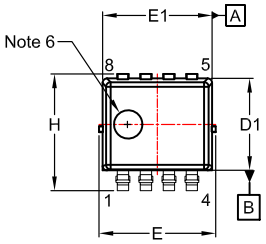
Device	Marking	Package	Shipping†
NVTYS027N10MCLTWG	027N 10MCL	LFPAK8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

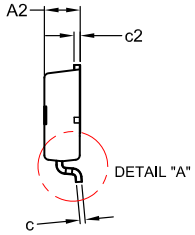


LFPAK8 3.3x3.3, 0.65P
CASE 760AD
ISSUE E

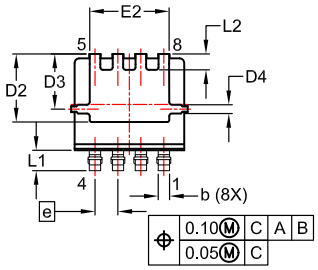
DATE 16 NOV 2020



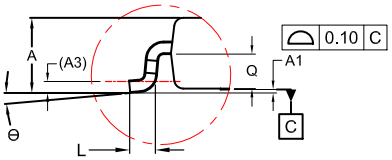
TOP VIEW



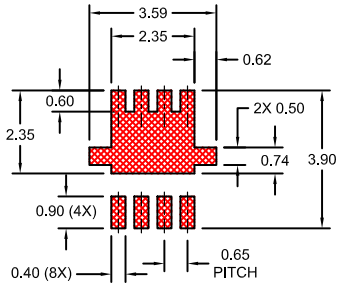
SIDE VIEW



BOTTOM VIEW



DETAIL 'A'
SCALE: 2:1



LAND PATTERN
RECOMMENDATION

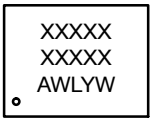
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3		0.15 REF	
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e		0.65 BSC	
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
θ	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**LFPAK8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales