[MOSFET](#) - Power, Single N-Channel, TOLL
60 V, 0.9 mΩ, 422 A

NVBLS001N06C

ON Semiconductor®

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	0.9 mΩ @ 10 V	422 A

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	422	A
		T_C = 100°C		298	
Power Dissipation $R_{\theta JC}$ (Note 2)		T_C = 25°C	P_D	284	W
		T_C = 100°C		142	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	51	A
		T_A = 100°C		36	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	4.2	W
		T_A = 100°C		2.1	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	236	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 39 A)			E_{AS}	1640	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

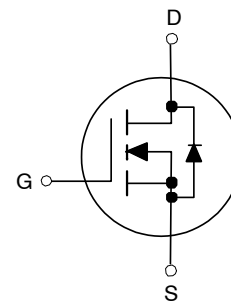| Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.53	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	36	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

H−PSOF8L
CASE 100CU

ORDERING INFORMATION

Device	Package	Shipping[†]
NVBLS001N06C	H−PSOF8L (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVBLS001N06C

Table 1. ELECTRICAL CHARACTERISTICS $(T_J = 25°C$ unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 562\ \mu A$, ref to 25°C			26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ V$, $V_{GS} = 0\ V$	$T_J = 25°C$			10	μA
			$T_J = 125°C$			100	μA
Gate−to−Source Leakage Current	I_{GSS}	$V_{DS} = 0\ V$, $V_{GS} = 20\ V$				100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 562\ \mu A$		2.0	2.8	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$	$I_D = 562\ \mu A$, ref to 25°C			9.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\ V$, $I_D = 80\ A$			0.75	0.9	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 5\ V$, $I_D = 80\ A$			290		S
CHARGES & CAPACTIANCES							
Input Capacitance	C_{iss}	$V_{GS} = 0\ V$, $V_{DS} = 30\ V$, f = 10 kHz			11575		pF
Output Capacitance	C_{oss}				5973		pF
Reverse Transfer Capacitance	C_{rss}				76		pF
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10\ V$, $V_{DS} = 30\ V$, $I_D = 80\ A$			143		nC
Threshold Gate Charge	$Q_{G(th)}$				31		nC
Gate−to−Source Charge	Q_{gs}				54		nC
Gate−to−Drain Charge	Q_{gd}				13		nC
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	$V_{GS} = 10\ V$, $V_{DS} = 30\ V$, $I_D = 80\ A$, $R_G = 6\ \Omega$			34		ns
Rise Time	t_r				53		ns
Turn−Off Delay Time	$t_{d(off)}$				119		ns
Fall Time	t_f				91		ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	$I_S = 80\ A$, $V_{GS} = 0\ V$	$T_J = 25°C$		0.79	1.2	V
		$I_S = 80\ A$, $V_{GS} = 0\ V$	$T_J = 125°C$		0.66		V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\ V$, $dI_S/d_t = 100\ A/\mu s$, $I_S = 56\ A$			120		ns
Charge Time	t_a				60		ns
Discharge Time	t_b				60		ns
Reverse Recovery Charge	Q_{rr}				322		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Switching characteristics are independent of operating junction temperatures

NVBLS001N06C

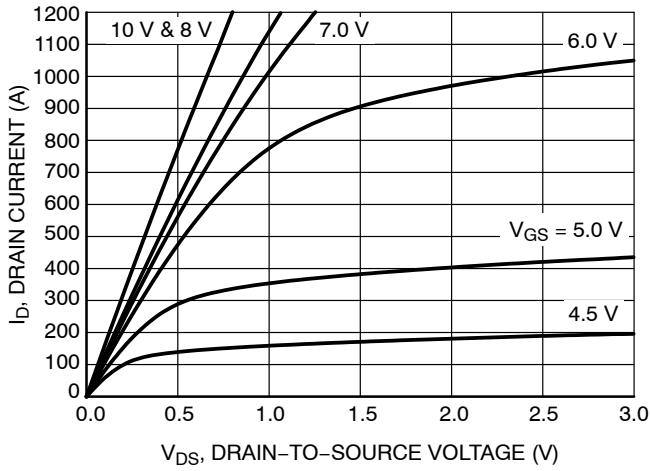## TYPICAL CHARACTERISTICS

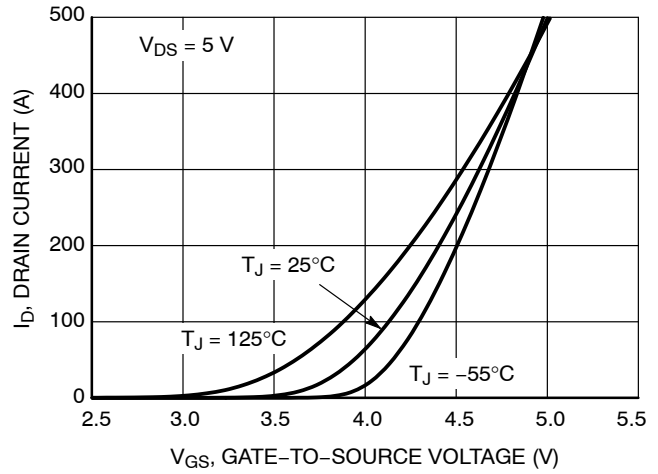Figure 1. On−Region Characteristics
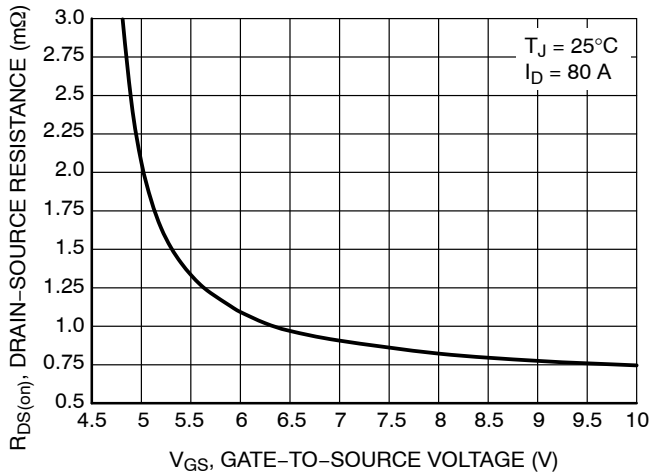

Figure 2. Transfer Characteristics

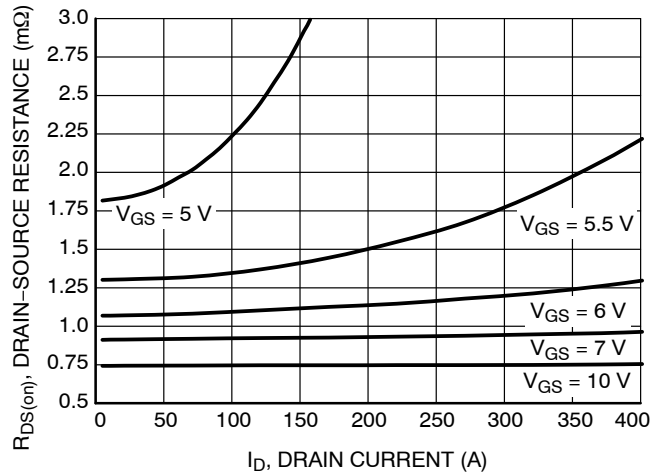Figure 3. On−Resistance vs. V_{GS}

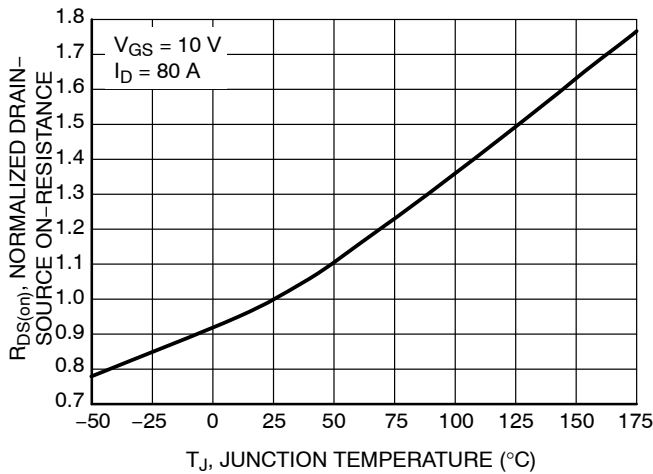
Figure 4. On−Resistance vs. Drain Current and Gate Voltage
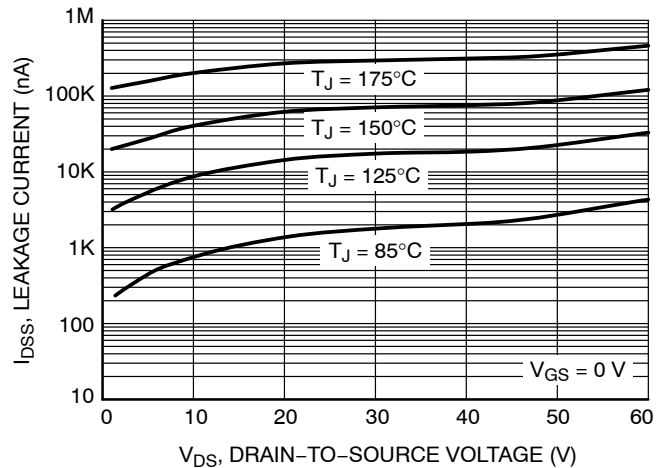

Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage

NVBLS001N06C

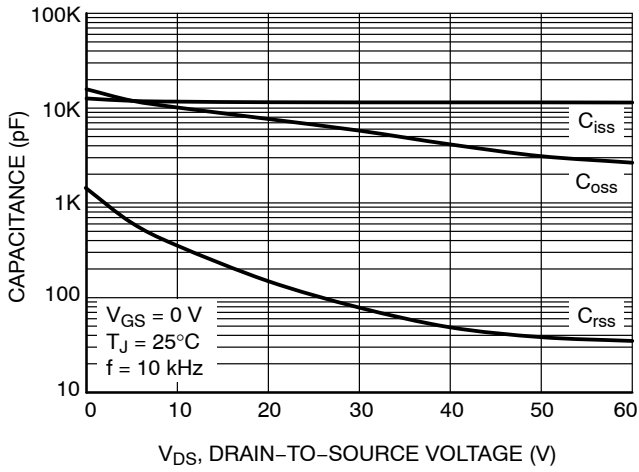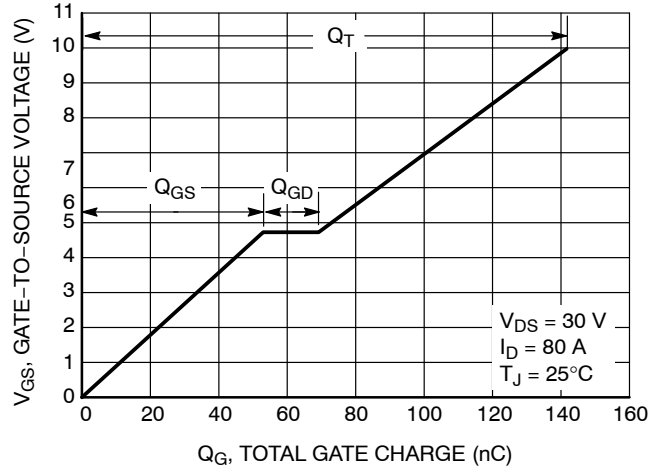**Figure 7. Capacitance Variation**

Figure 8. Gate−to−Source Voltage vs. Total Gate Charge
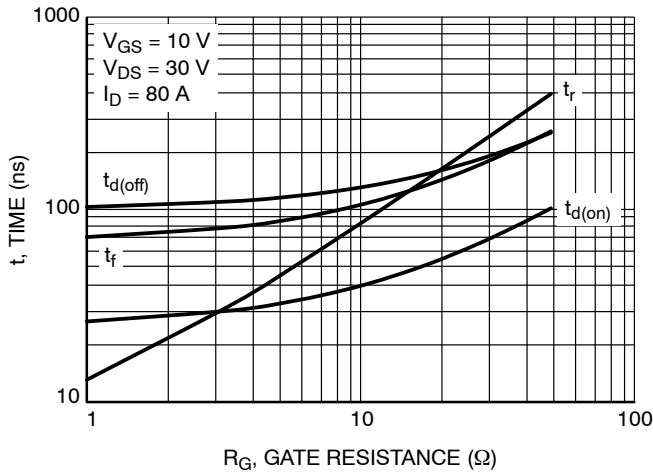
Figure 9. Resistive Switching Time Variation vs. Gate Resistance
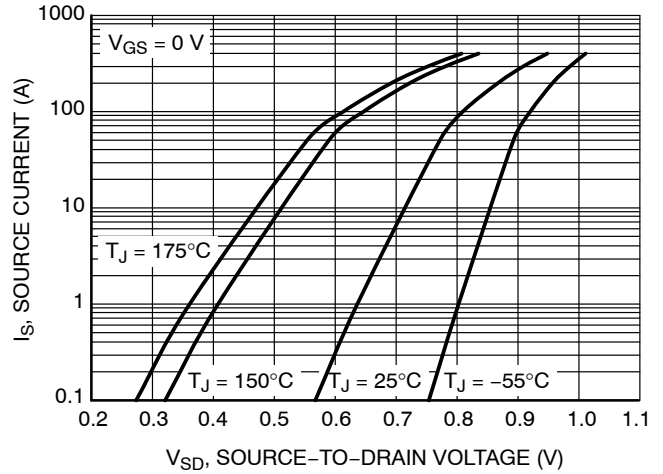
Figure 10. Diode Forward Voltage vs. Current
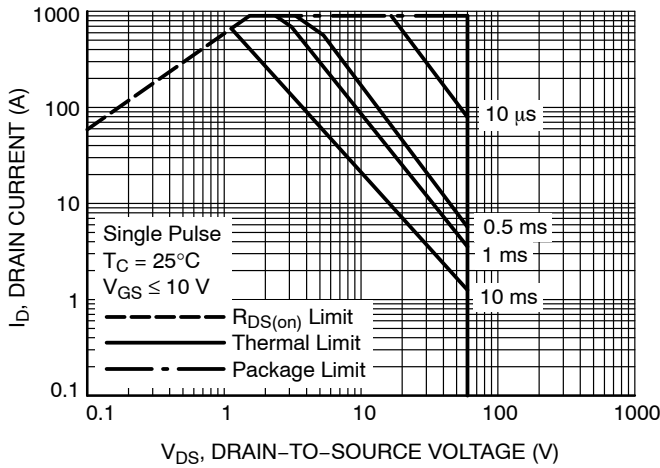
Figure 11. Maximum Rated Forward Biased Safe Operating Area
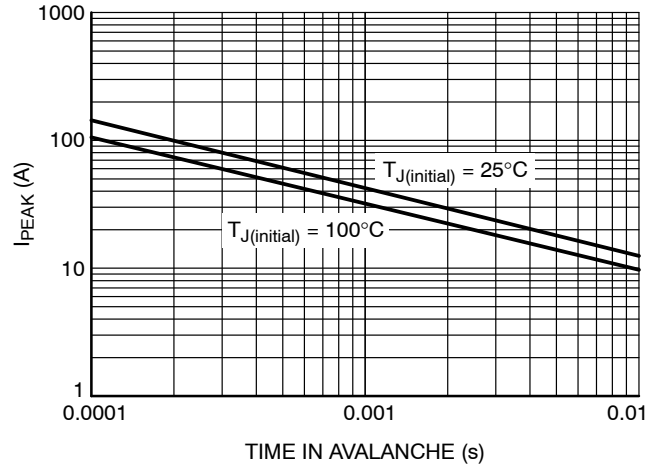
Figure 12. Avalanche Characteristics

TYPICAL CHARACTERISTICS
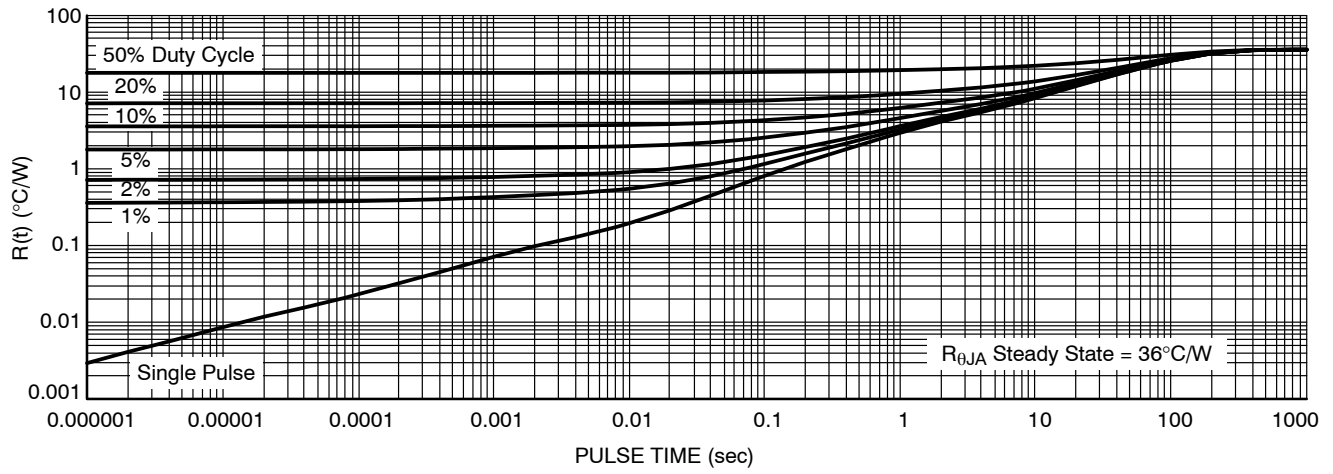
Figure 13. Thermal Characteristics (Junction−to−Ambient)
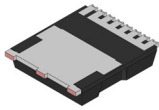
onsemi™

H−PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

DATE 30 JUL 2024

(2x) ⌒ ccc | D | B

TERMINAL 1 CORNER INDEX AREA △5

TOP VIEW

SECTION "A-A"
SCALE: 2X

DETAIL "B"

SIDE VIEW

DETAIL "B"
SCALE: 2X

BOTTOM VIEW

HEAT SLUG TERMINAL
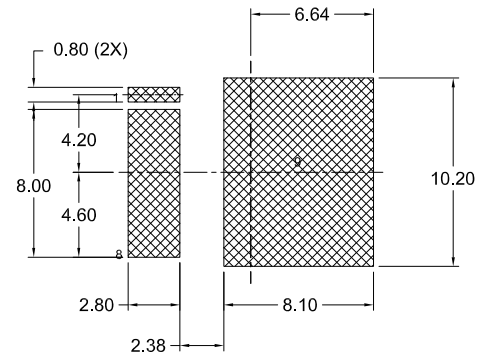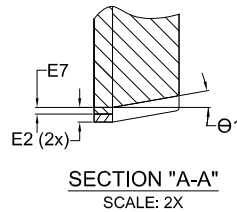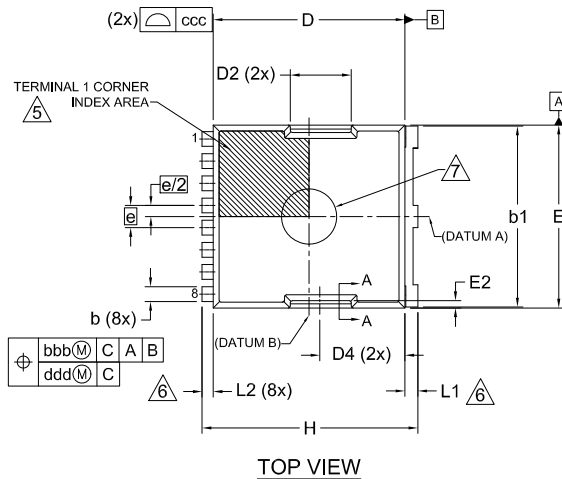
LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.
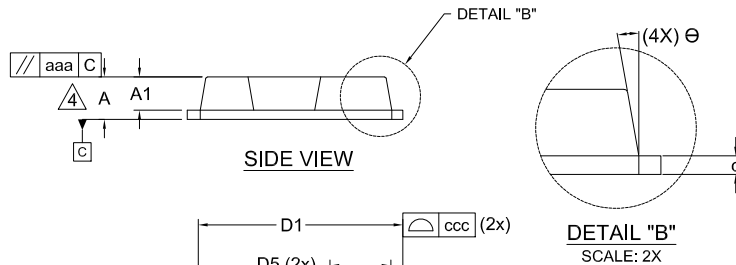
NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*

AYWWZZ

XXXXXXXX
XXXXXXXX

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code
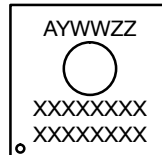
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13813G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	H−PSOF8L 11.68x9.80x2.30, 1.20P		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊