

MOSFET
StrongIRFET™ 2 Power-Transistor, 100 V

TOLL

Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified for applications according to the test conditions in the relevant tests of JEDEC JESD22 and J-STD-020.

Table 1 Key performance parameters

Table with 3 columns: Parameter, Value, Unit. Rows include V_DS (100 V), R_DS(on),max (1.5 mΩ), I_D (315 A), Q_oss (204 nC), and Q_G (161 nC).

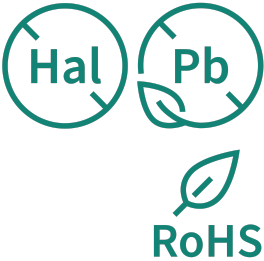
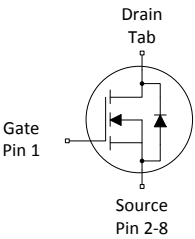
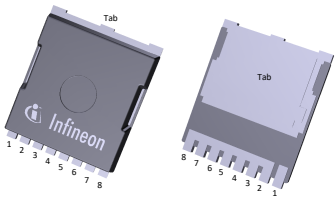


Table with 4 columns: Part number, Package, Marking, Related links. Row 1: IPT015N10NF2S, PG-HSOF-8, 015N10NS, -



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	315	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				223		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				198		$V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$
				35		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1260	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	406	mJ	$I_D=150\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300	W	$T_C=25\text{ °C}$
				3.8		$T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}			40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}			62		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=267\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.5	m Ω	$V_{GS}=10\text{ V}$, $I_D=150\text{ A}$
			1.6	2.0		$V_{GS}=6\text{ V}$, $I_D=75\text{ A}$
Gate resistance	R_G	-	1.4	-	Ω	-
Transconductance ⁶⁾	g_{fs}	135	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	11000	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		1700			
Reverse transfer capacitance	C_{rss}		76			
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		65			
Turn-off delay time	$t_{d(off)}$		60			
Fall time	t_f		33			

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	51	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		34	-	nC	
Gate to drain charge	Q_{gd}		32	-	nC	
Switching charge	Q_{sw}		49	-	nC	
Gate charge total ⁸⁾	Q_g		161	242	nC	
Gate plateau voltage	$V_{plateau}$		4.4	-	V	
Output charge	Q_{oss}	-	204	-	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	214	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1260		
Diode forward voltage	V_{SD}	-	0.85	1.2	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	49	-	ns	$V_R=50\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		437		nC	

4 Electrical characteristics diagrams

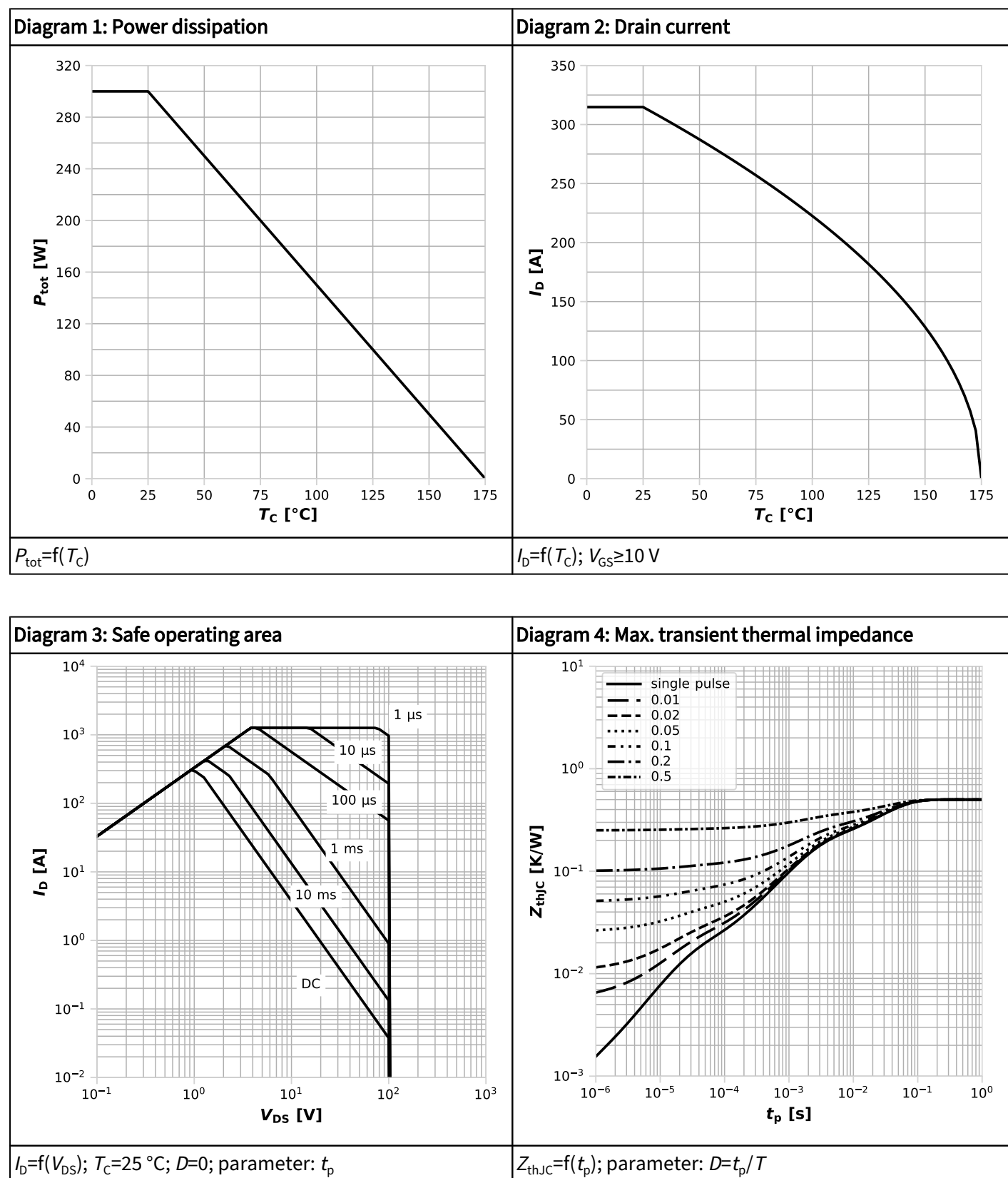
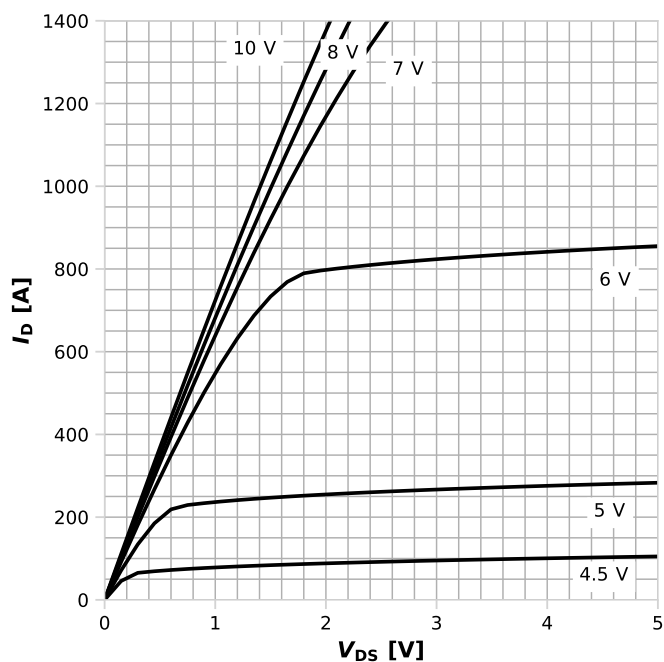
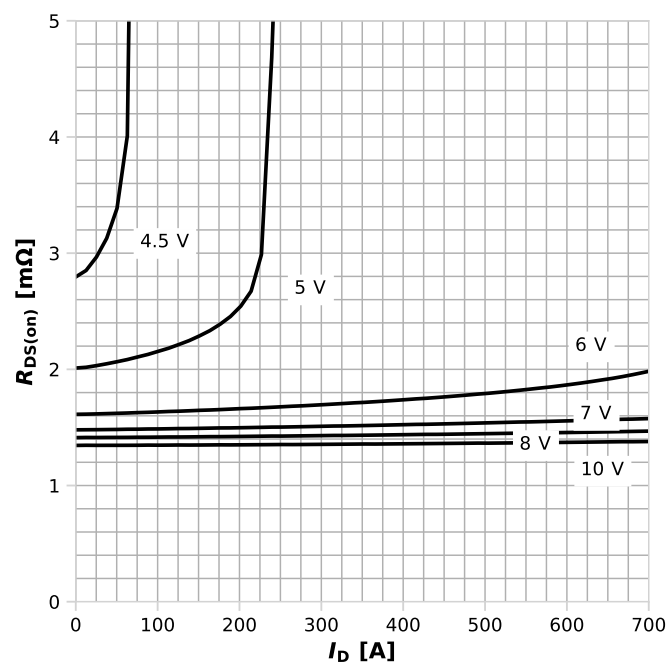


Diagram 5: Typ. output characteristics



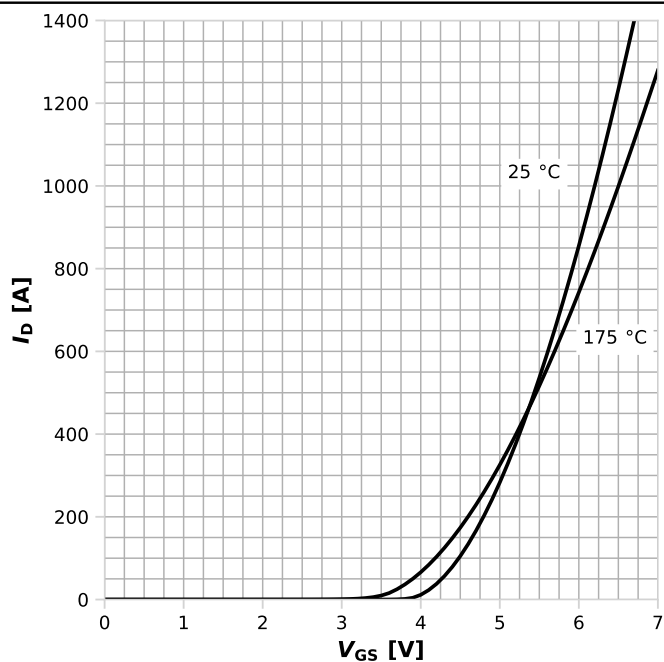
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



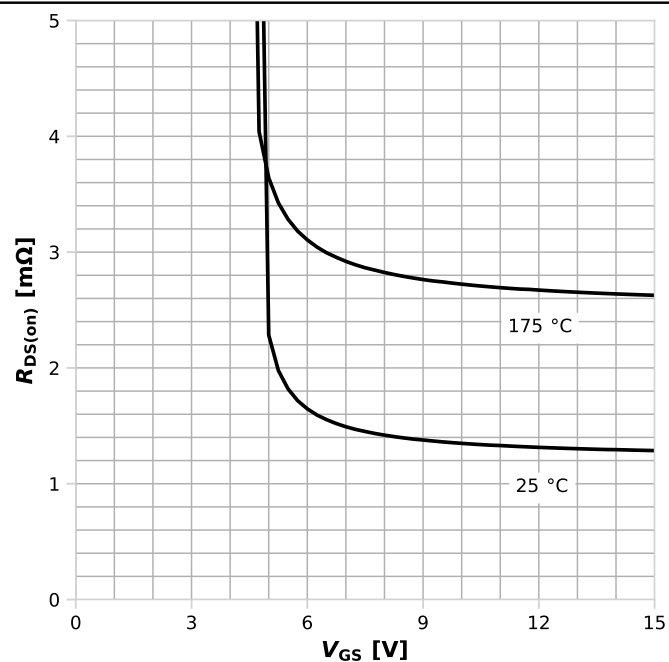
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



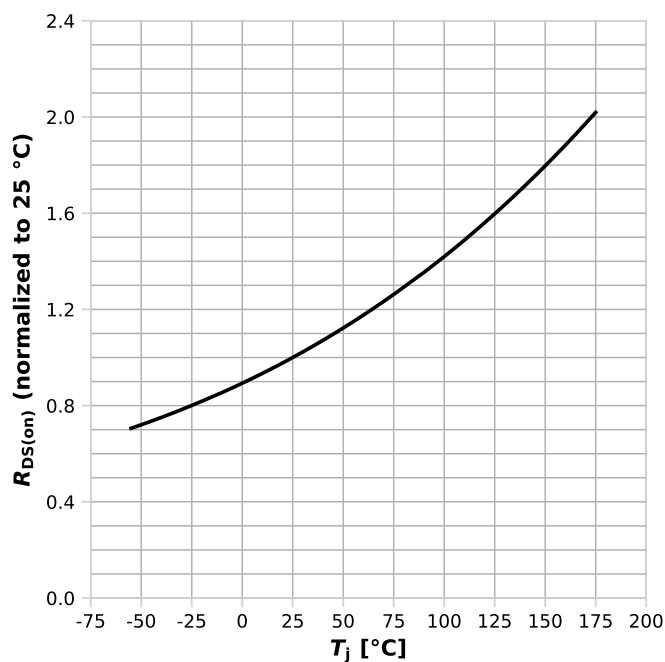
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



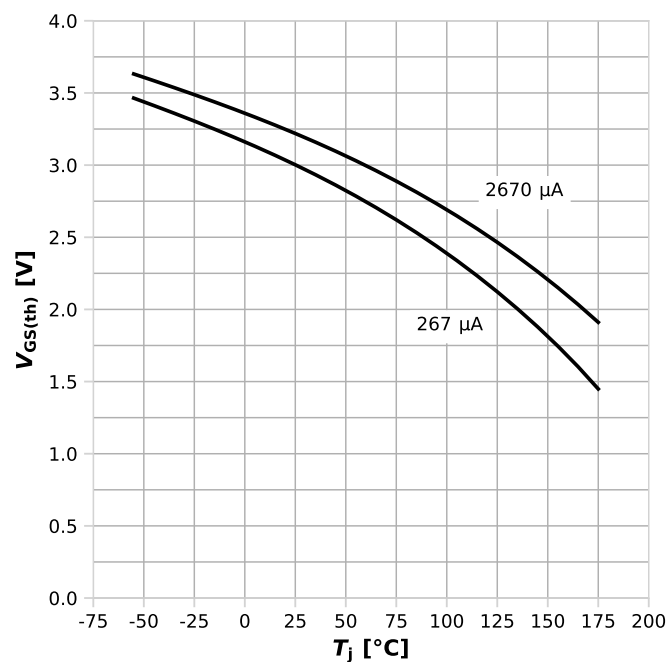
$R_{DS(on)} = f(V_{GS})$, $I_D = 150\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



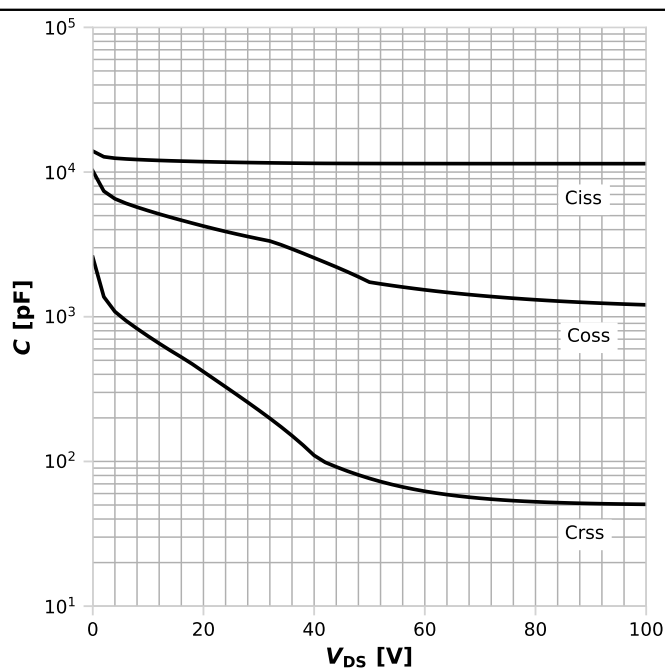
$$R_{DS(on)} = f(T_j), I_D = 150 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



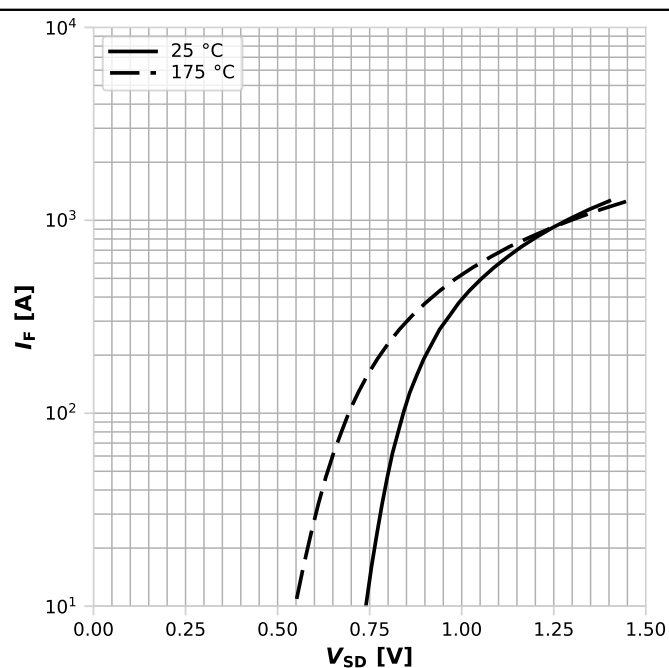
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{parameter: } I_D$$

Diagram 11: Typ. capacitances



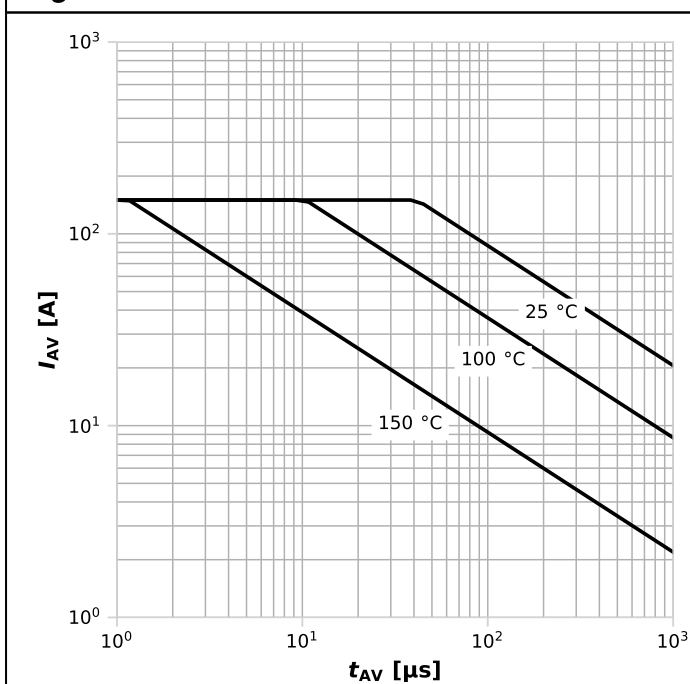
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Typ. forward characteristics of reverse diode



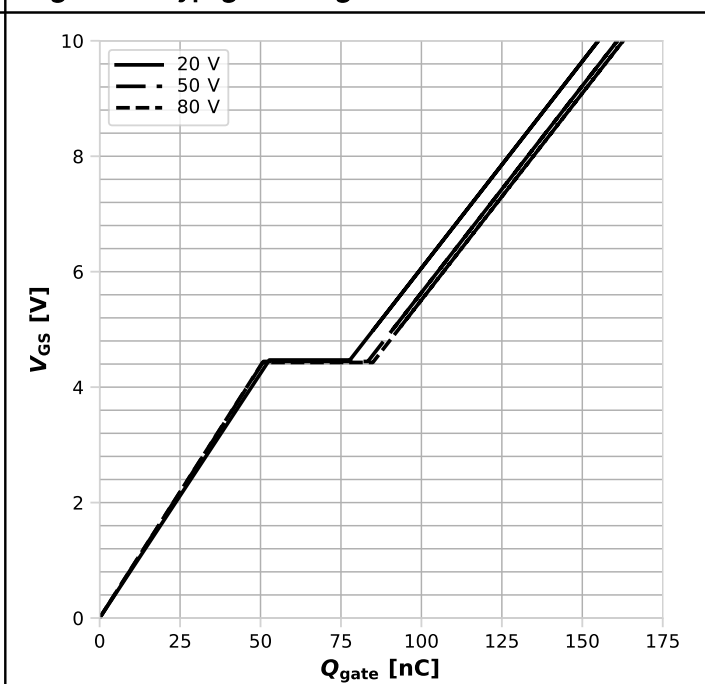
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Diagram 13: Avalanche characteristics



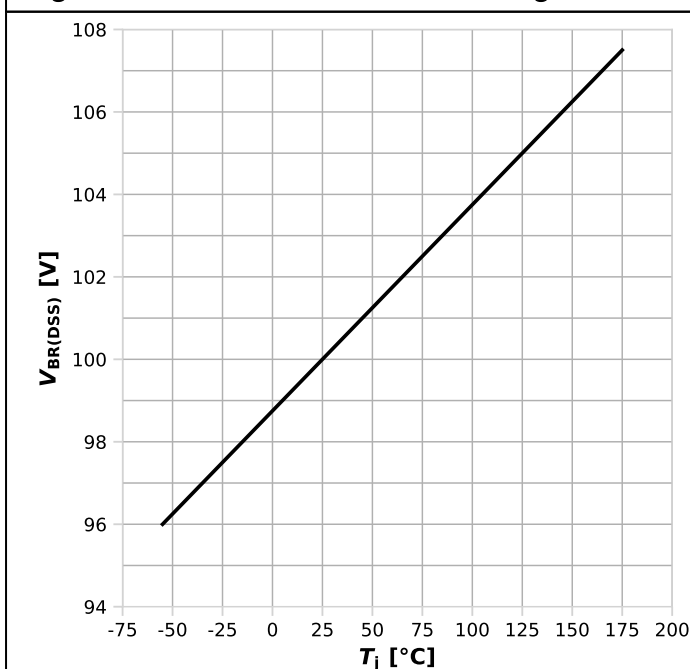
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



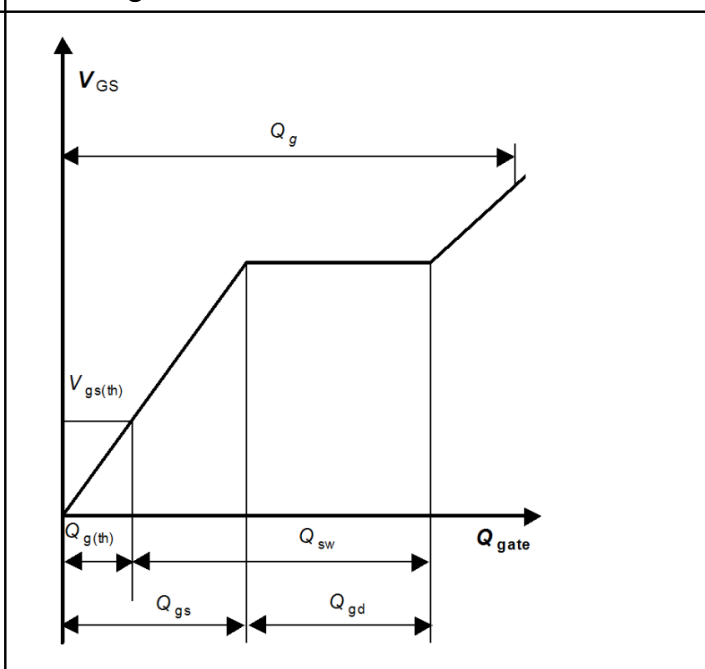
$V_{GS}=f(Q_{gate})$, $I_D=100\text{ A pulsed}$, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



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5 Package outlines

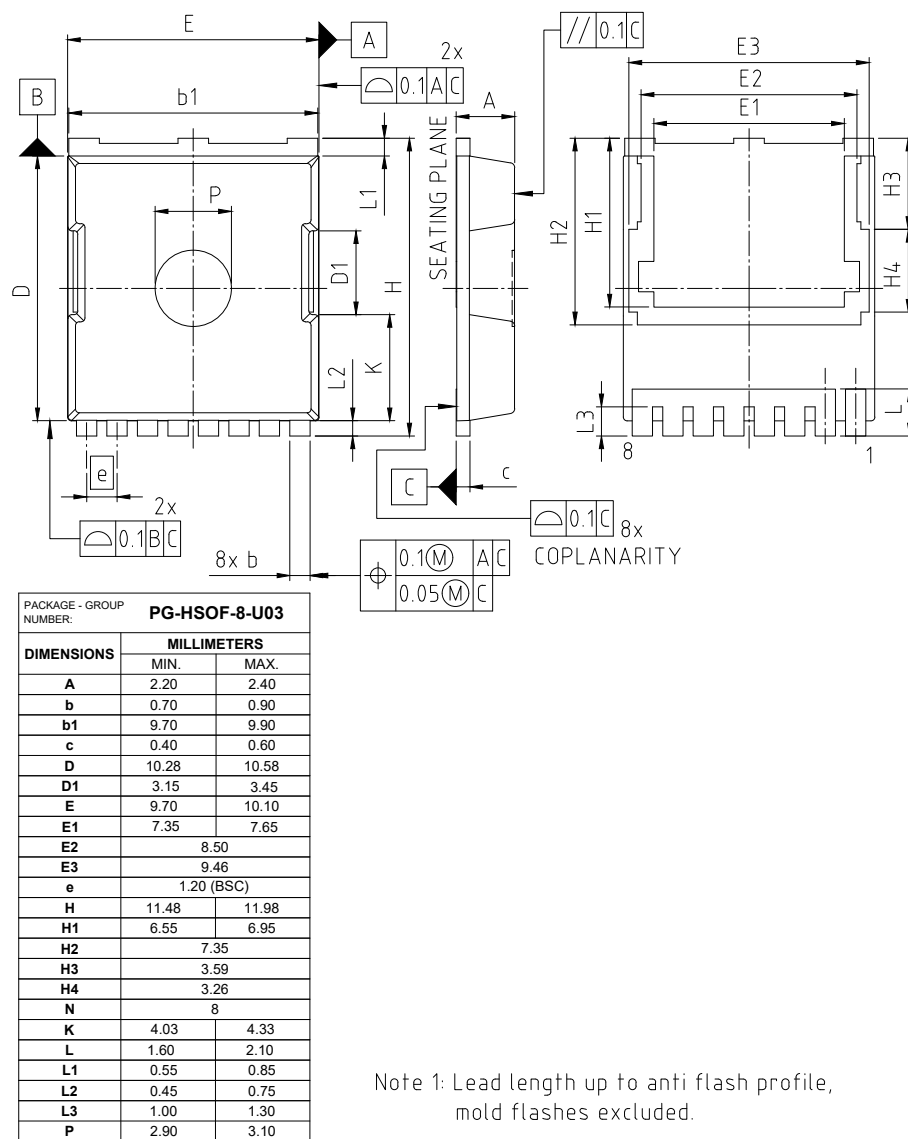


Figure 1 Outline PG-HSOF-8, dimensions in mm

Revision history

IPT015N10NF2S

Revision 2025-04-29, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2022-08-04	Release of final version
2.1	2025-04-29	Update SOA Diagram

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