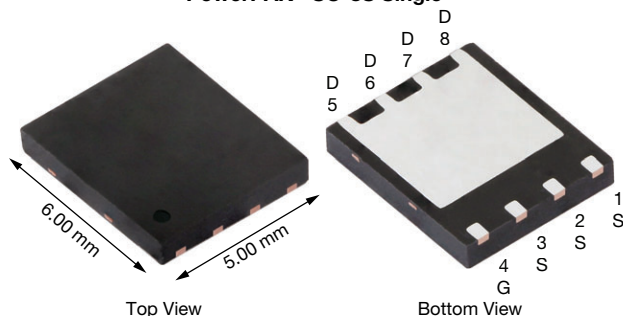


# N-Channel 100 V (D-S) MOSFET

**PowerPAK® SO-8S Single**


## FEATURES

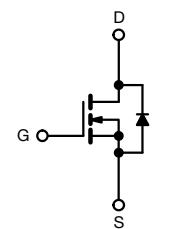
- TrenchFET® Gen IV power MOSFET
- Very low  $R_{DS(on)}$  x  $Q_g$  figure-of-merit (FOM)
- Leadership  $R_{DS(on)}$  minimizes power loss from conduction
- 100 %  $R_g$  and UIS tested
- Enhance power dissipation and lower  $R_{thJC}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0035
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0043
$Q_g$ typ. (nC)	86
$I_D$ (A) <sup>a</sup>	171
Configuration	Single

## ORDERING INFORMATION

Package	PowerPAK SO-8S
Lead (Pb)-free and halogen-free	SiRS700DP-T1-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	100	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	127
		$T_C = 70$ °C	102
		$T_A = 25$ °C	30 <sup>b, c</sup>
		$T_A = 70$ °C	24 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	350	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	120
		$T_A = 25$ °C	6.7 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	50	
Single pulse avalanche energy	$E_{AS}$	125	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	132
		$T_C = 70$ °C	84
		$T_A = 25$ °C	7.4 <sup>b, c</sup>
		$T_A = 70$ °C	4.7 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	13	17	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	0.73	0.95	

### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 45 °C/W

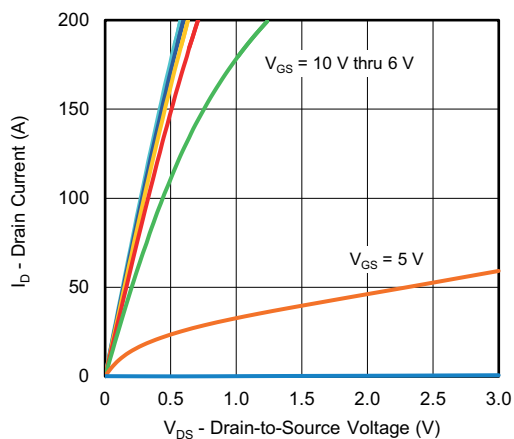
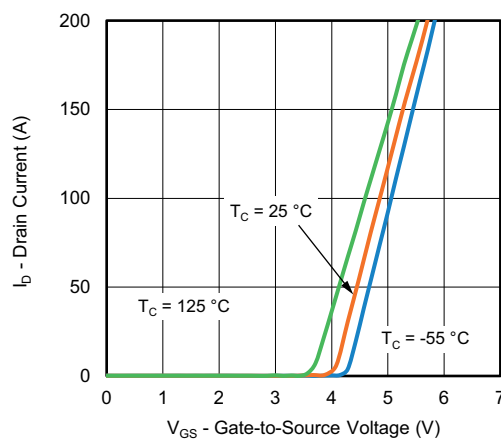
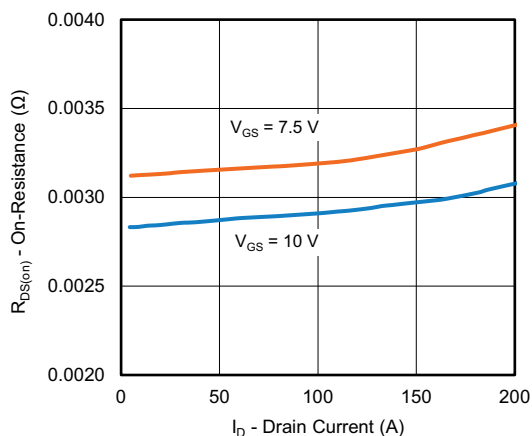
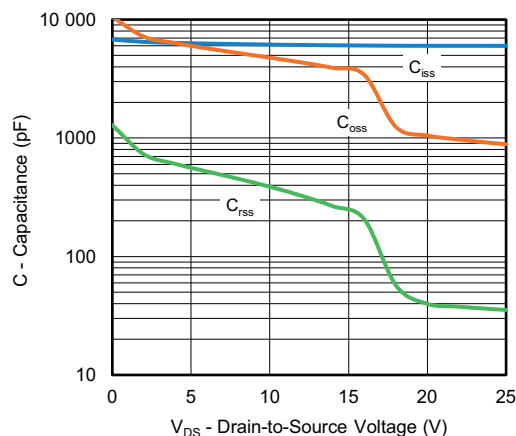
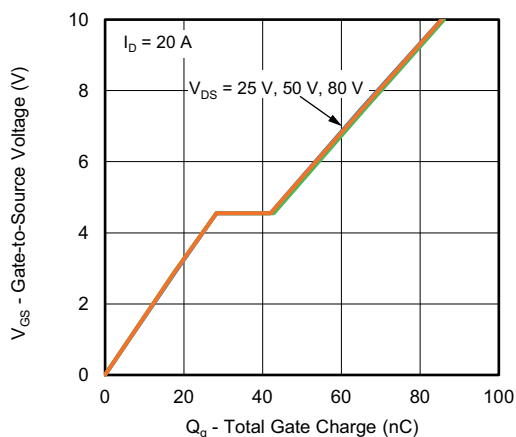
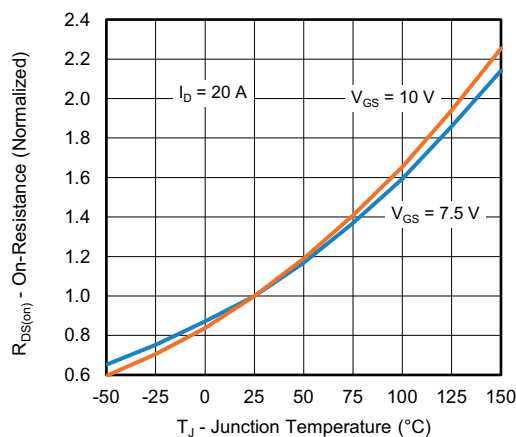


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	81	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	9.7	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.0028	0.0035	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.0032	0.0043	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	125	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	5950	-	pF
Output capacitance	C <sub>oss</sub>		-	580	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	27	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	86	130	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	66	100	
Gate-source charge	Q <sub>gs</sub>		-	29	-	
Gate-drain charge	Q <sub>gd</sub>		-	14	-	
Output charge	Q <sub>oss</sub>	-	120	-		
Gate resistance	R <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V	-	120	-	Ω
		f = 1 MHz	0.2	1.1	2.2	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	20	40	ns
Rise time	t <sub>r</sub>		-	8	20	
Turn-off delay time	t <sub>d(off)</sub>		-	40	80	
Fall time	t <sub>f</sub>		-	12	25	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 60 V, R <sub>L</sub> = 5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 7.5 V, R <sub>g</sub> = 1 Ω	-	25	50	
Rise time	t <sub>r</sub>		-	20	40	
Turn-off delay time	t <sub>d(off)</sub>		-	35	70	
Fall time	t <sub>f</sub>		-	13	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	120	A
Pulse diode forward current	I <sub>SM</sub>		-	-	350	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.71	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	65	130	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	110	220	nC
Reverse recovery fall time	t <sub>a</sub>		-	43	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	22	-	

**Notes**

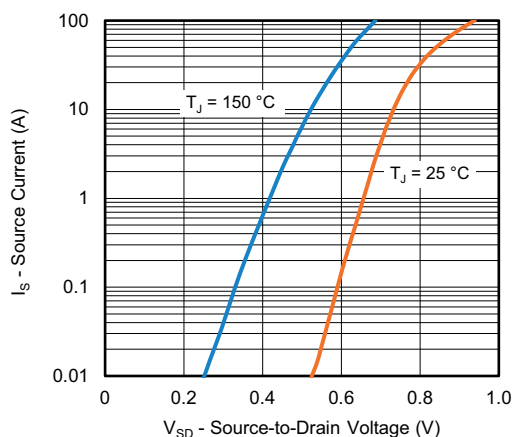
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

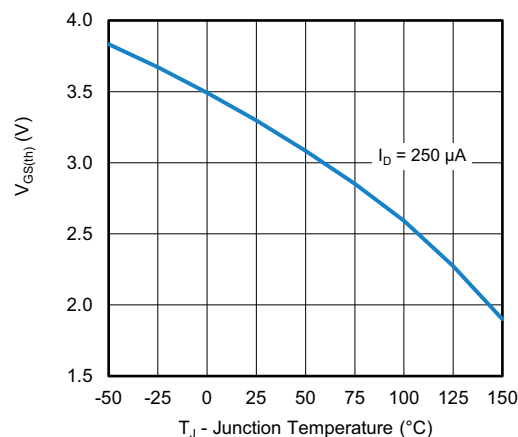
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**



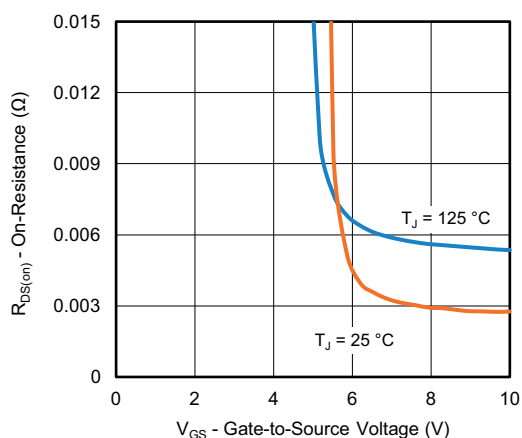
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



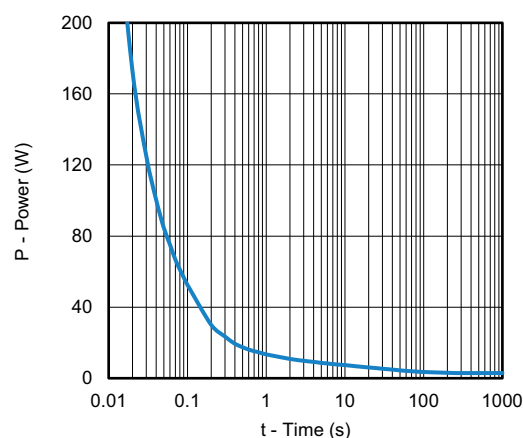
**Source-Drain Diode Forward Voltage**



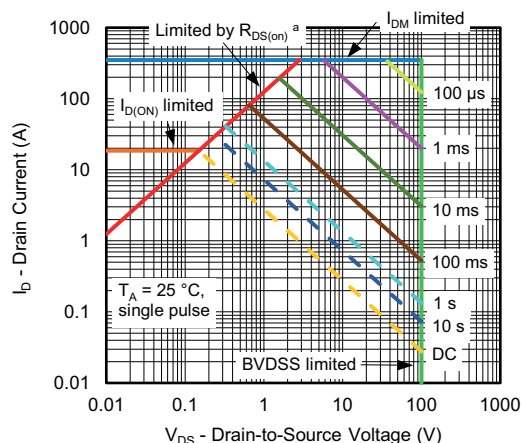
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



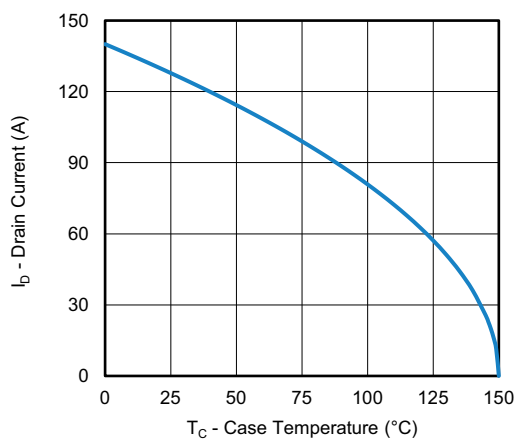
**Safe Operating Area, Junction-to-Ambient**

**Note**

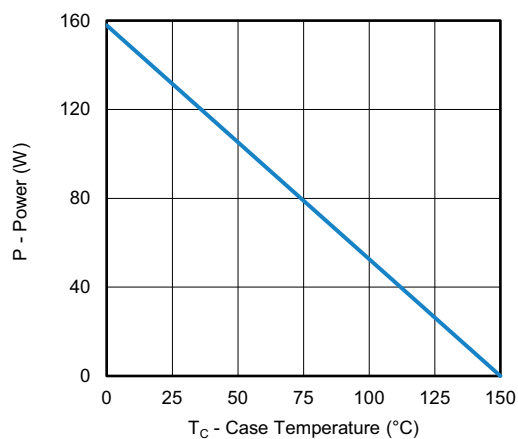
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



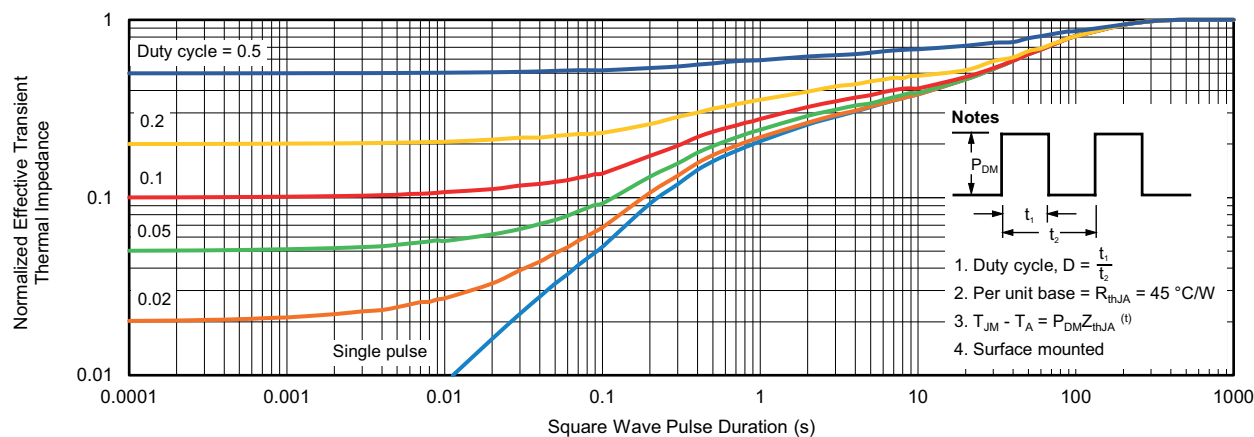
**Power, Junction-to-Case**

**Note**

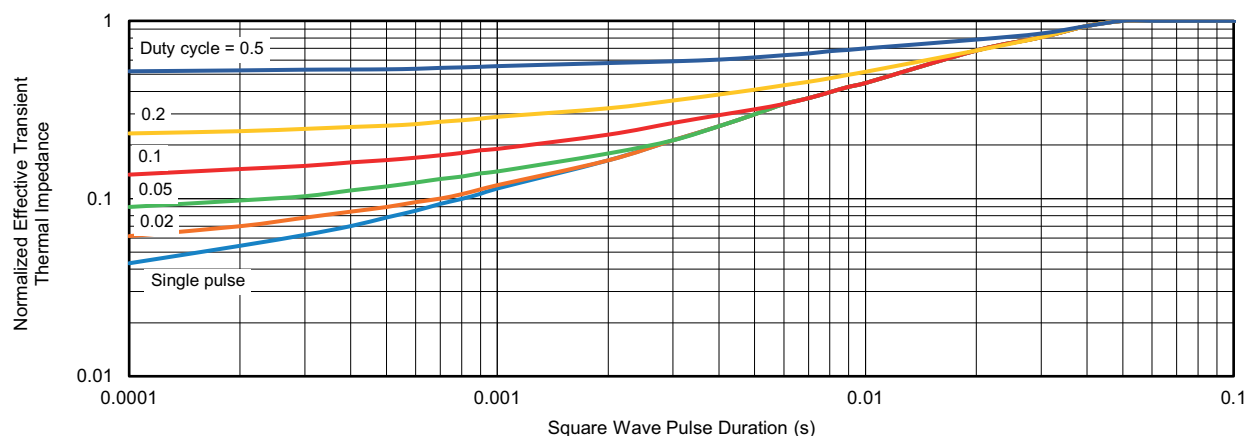
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

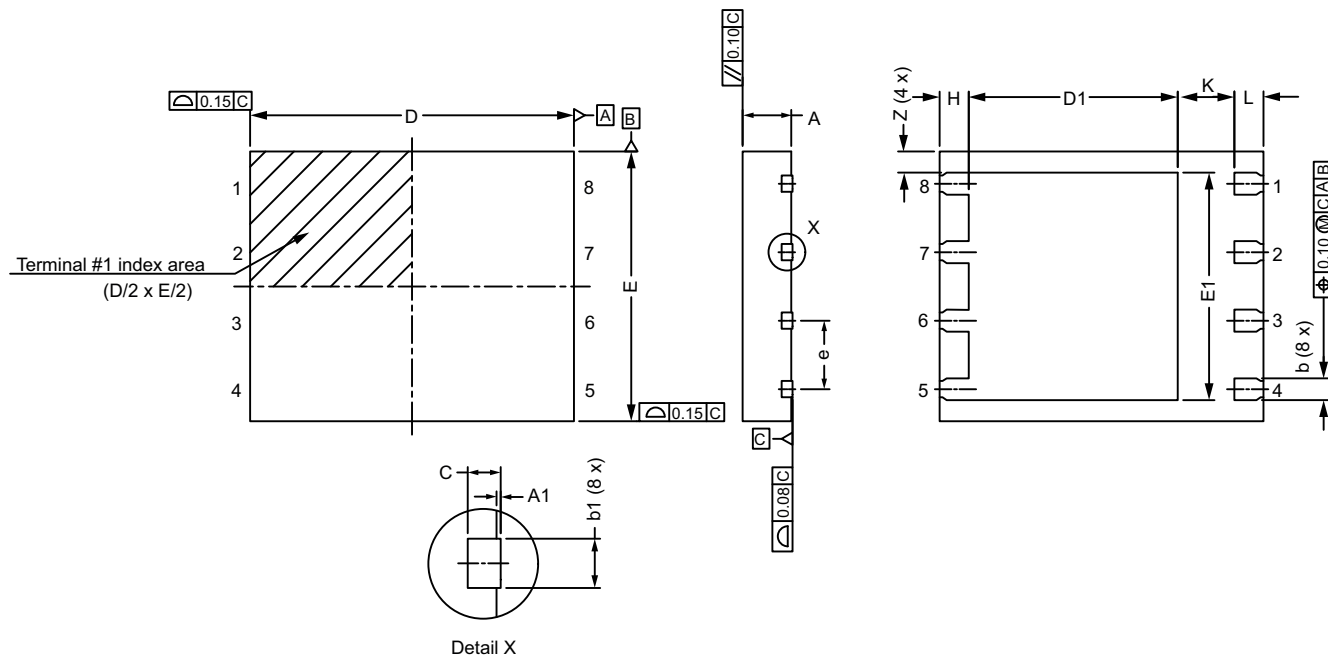


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63060](http://www.vishay.com/ppg?63060).

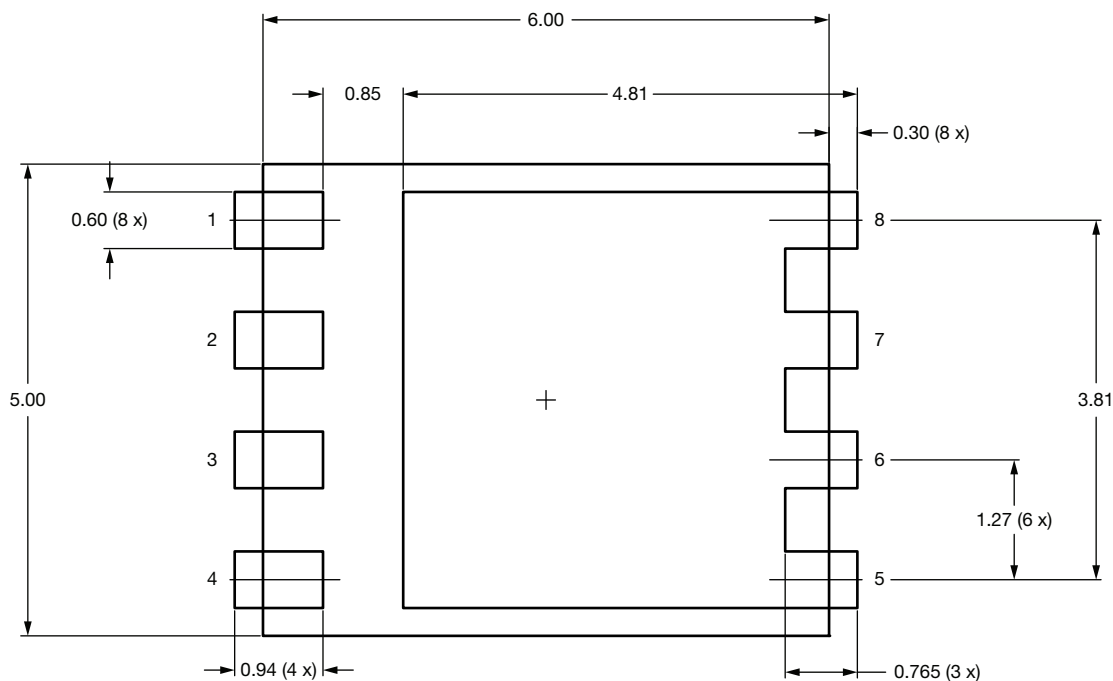
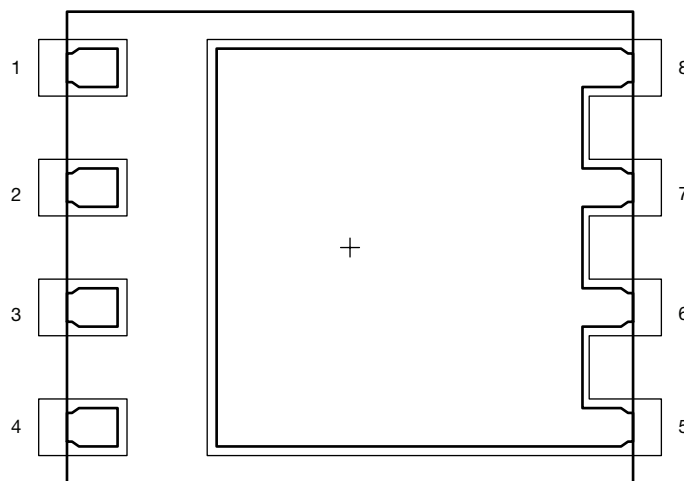


## PowerPAK® SO-8S BWL



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	-	-	0.05	-	-	0.002
b	0.31	0.41	0.51	0.012	0.016	0.020
b1	0.20	0.30	0.40	0.008	0.012	0.016
c	0.20 ref.			0.008 ref.		
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	3.78	3.88	3.98	0.149	0.153	0.157
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.12	4.22	4.32	0.162	0.166	0.170
e	1.27 BSC			0.050 BSC		
H	0.44	0.54	0.64	0.017	0.021	0.025
K	1.05 ref.			0.041 ref.		
L	0.44	0.54	0.64	0.017	0.021	0.025
Z	0.39 ref.			0.015 ref.		
ECN: C20-0936-Rev. A, 03-Aug-2020						
DWG: 6082						

# Recommended Land Pattern PowerPAK® SO-8S BWL







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