

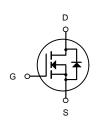
### **General Description**

The SIR106ADP-T1-RE3 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness.



DFN5X6-8L (Power(5x6))



N-Channel MOSFET

### **General Features**

 $V_{DS} = 100V I_{D} = 75A$ 

 $R_{DS(ON)} < 7.5 m\Omega V_{GS} = 10 V$ 

## **Applications**

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
SIR106ADP-T1-RE3	DFN5X6-8L(Power(5x6))	HXY MOSFET	5000

## Absolute Maximum Ratings at T<sub>i</sub>=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	100	V
Gate source voltage	VGS	±20	V
Continuous drain current <sup>1)</sup>	ID	75	А
Pulsed drain current <sup>2)</sup>	ID, pulse	300	А
Power dissipation <sup>3)</sup>	P <sub>D</sub>	97	W
Single pulsed avalanche energy <sup>5)</sup>	EAS	90	mJ
Operation and storage temperature	Tstg,Tj	-55 to 150	°C
Thermal resistance, junction-case	RθJC	1.3	°C/W



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

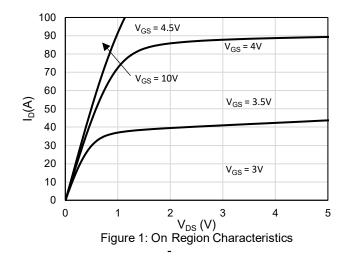
Symbol	Parameter	Parameter Test Condition		Тур.	Max.	Units
Off Charac	cteristic					
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, - V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V -		-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current			-	±100	nA
On Charac	cteristics			•		
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.6	2.5	V
В	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A -		6.4	7.5	mΩ
$R_{DS(on)}$	note3	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		9.2	11.4	mΩ
Dynamic (	Characteristics			•		
C <sub>iss</sub>	Input Capacitance		-	2944	-	pF
Coss	Output Capacitance	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V,	-	736	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	2.04	-	pF
Qg	Total Gate Charge	501/1 004	_	39.4	-	nc
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS}$ =50V, $I_{D}$ =30A, $V_{GS}$ =10V	-	5.6	-	nc
$Q_{\text{gd}}$	Gate-Drain("Miller") Charge	VGS-10V	-	7.6	-	nc
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-on Delay Time		_	13	-	nc
t <sub>r</sub>	Turn-on Rise Time	V <sub>DD</sub> =50V, I <sub>D</sub> =25A,	_	27.5	-	nc
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =6Ω, V <sub>GS</sub> =10V	_	45.5	-	nc
t <sub>f</sub>	Turn-off Fall Time		_	41.5	-	nc
Drain-Sou	rce Diode Characteristics and Maxim	um Ratings				
Is	Maximum Continuous Drain to Source Diode Forward		_	_	75	Α
		Current				
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	300	Α
$V_{\text{SD}}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	-	1	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T -25°0	-	177	-	ns
Qrr	Body Diode Reverse Recovery Charge	T <sub>J</sub> =25°C, I <sub>F</sub> =12A,dI/dt=100A/μs	-	1291	-	nc

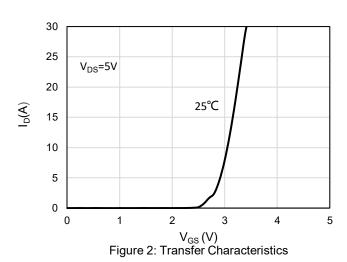
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

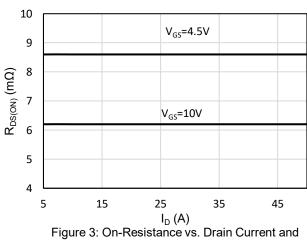
- 2. EAS condition:  $T_J$ =25°C,  $V_{DD}$ =50V,  $V_G$ =10V,  $R_G$ =25 $\Omega$ , L=0.5mH,  $I_{AS}$ =19A
- 3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%

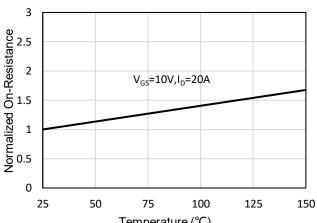


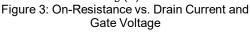
## **Typical Performance Characteristics**

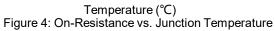


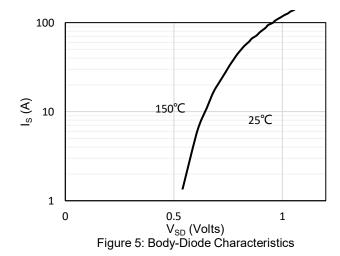


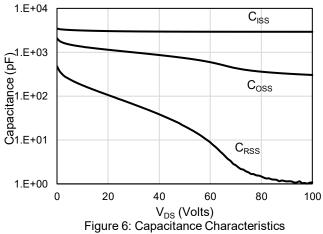




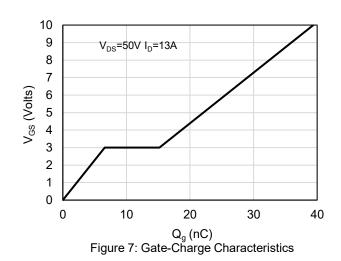


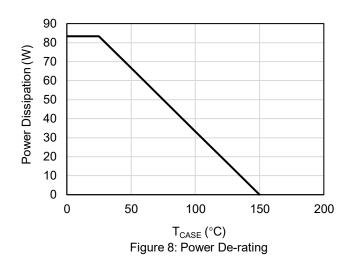


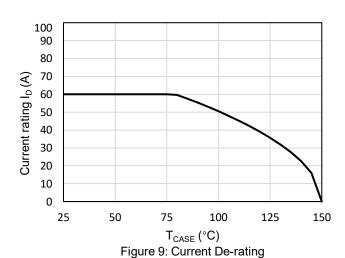




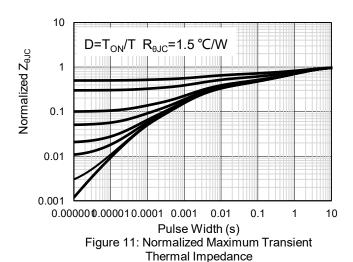












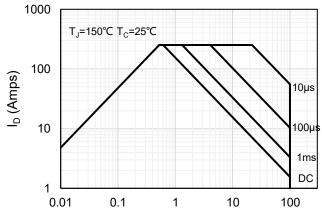
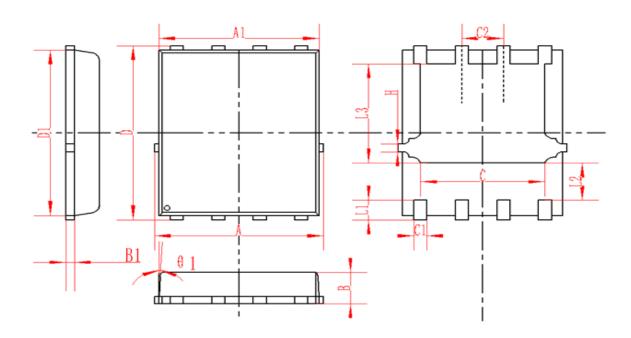


Figure 12: Maximum Forward Biased Safe Operating Area



# DFN5X6-8L(Power(5x6)) Package Information



SYMBOL	MM		INCH			
STIVIDOL	MIN	NOM	MAX	MIN	NOM	MAX
Α	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
В	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF		0.010REF			
С	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2		1.27TYP			0.5TYP	
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
Η	0.24	0.25	0.26	0.009	0.010	0.010



#### N-SGT Enhancement Mode MOSFET

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