

#### **Description**

The SI4822DY uses advanced trench technology to provide excellent R<sub>DS(ON)</sub>, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

# S S G SOP-8

(SO-8)

#### **General Features**

 $V_{DS} = 30V I_{D} = 15 A$ 

 $R_{DS(ON)} < 9m\Omega$  @  $V_{GS}=10V$ 

 $R_{DS(ON)}$  < 14m $\Omega$  @  $V_{GS}$ =4.5V

# PIN1 G PIN3 S

# **Application**

Battery protection

Load switch

Uninterruptible power supply

#### N-Channel MOSFET

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
SI4822DY	SOP-8(SO-8)	HXY MOSFET	3000

#### Absolute Maximum Ratings (Tc=25℃unless otherwise noted)

Symbol	Parameter	Limit	Unit
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>G</sub> s	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous	15.0	Α
I <sub>D</sub> (70 °C)	Drain Current-Continuous(Tc=70℃)	8.2	А
Ірм	Pulsed Drain Current	42	А
P <sub>D</sub>	Maximum Power Dissipation	1.5	W
Eas	Single pulse avalanche energy (Note 5)	62	mJ
Тл,Тѕтс	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}\!$
Rejc	Thermal Resistance,Junction-to-Case <sup>(Note 2)</sup>	36	°C/W



## Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.027		V/°C
В	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =10A		7.5	9	mΩ
R <sub>DS(ON)</sub>	Static Dialii-Source Off-Resistance	V <sub>GS</sub> =4.5V , I <sub>D</sub> =8A		11	14	
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.5	2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	VGS-VDS , ID -230UA		-5.8		mV/°C
less	Dunin Course Lookens Course	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C				
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	uA
Igss	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =10A		5.8		S
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.2	3.8	Ω
Qg	Total Gate Charge (4.5V)			12.6	17.6	
$Q_{gs}$	Gate-Source Charge	V <sub>DS</sub> =15V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =10A		4.2	5.9	nC
$Q_{gd}$	Gate-Drain Charge			5.1	7.1	
T <sub>d(on)</sub>	Turn-On Delay Time			6.2	12.4	ns
T <sub>r</sub>	Rise Time	$V_{DD}$ =15V , $V_{GS}$ =10V , $R_{G}$ =3.3 $\Omega$		59	106	
$T_{d(off)}$	Turn-Off Delay Time	I <sub>D</sub> =10A		27.6	55	
Tf	Fall Time			8.4	16.8	
Ciss	Input Capacitance			1317	1845	
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		163	228.2	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			131	183.4	
Is	Continuous Source Current <sup>1,5</sup>	V -V -0V Faras Ourset			15	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			42	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V
t <sub>rr</sub>	Reverse Recovery Time			12.5		nS
Qrr	Reverse Recovery Charge	lF=10A , dl/dt=100A/μs , Tյ=25°C		5		nC

#### Note:

<sup>1.</sup>The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

<sup>2.</sup>The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%

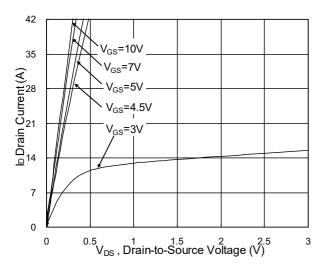
<sup>3.</sup> The EAS data shows Max. rating . The test condition is  $V_{DD}$ =25V,  $V_{GS}$ =10V, L=0.1mH,  $I_{AS}$ =35A

<sup>4.</sup> The power dissipation is limited by 150°C junction temperature

<sup>5.</sup> The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

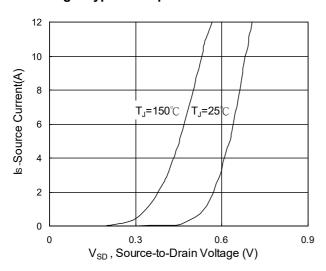


Fig.3 Forward Characteristics of reverse

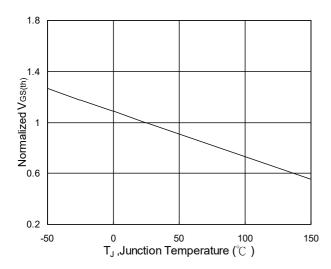


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$ 

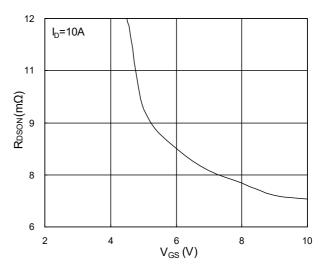


Fig.2 On-Resistance vs. Gate-Source

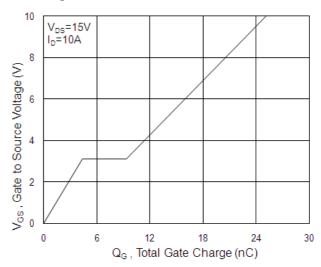


Fig.4 Gate-Charge Characteristics

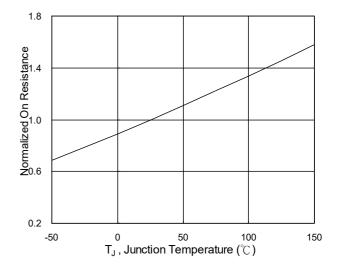
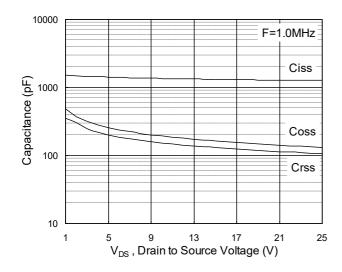


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>



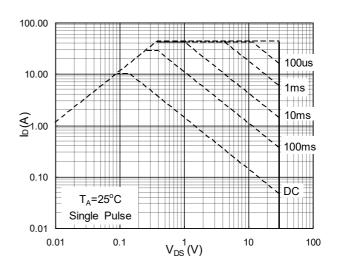


Fig.7 Capacitance

Fig.8 Safe Operating Area

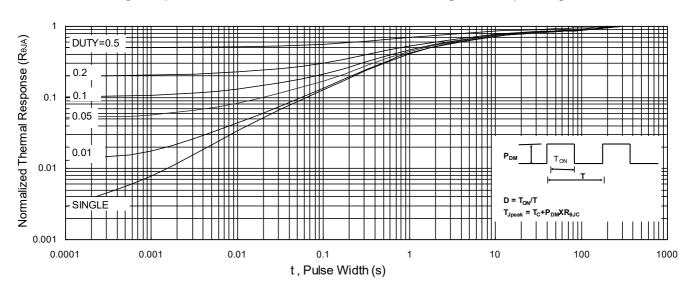


Fig.9 Normalized Maximum Transient Thermal Impedance

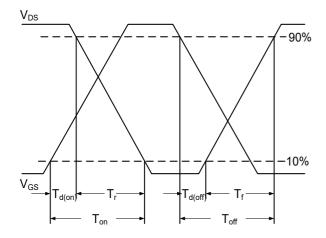


Fig.10 Switching Time Waveform

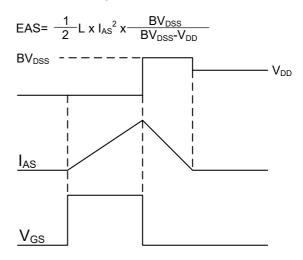
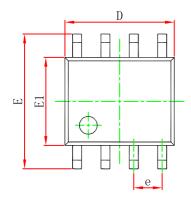
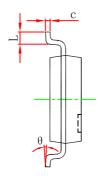


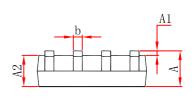
Fig.11 Unclamped Inductive Switching Waveform



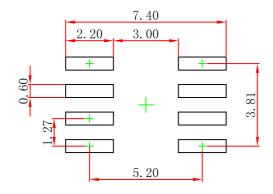
# **SOP-8(SO-8) Package Outline Dimensions**







Symbol	Dimensions In Millimeters		Dimensions In Inches		
3y111001	Min	Max	Min	Max	
A	1.350	1.750	0.053	0.069	
A1	0.100	0. 250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
c	0.170	0.250	0.007	0.010	
D	4.800	5.000	0.189	0. 197	
e	1.270 (BSC)		0.050 (BSC)		
E	5.800	6. 200	0. 228	0.244	
E1	3.800	4.000	0.150	0.157	
L	0.400	1.270	0.016	0.050	
θ	0°	8°	0°	8°	



- Note: 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.



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