

MOSFET

StrongIRFET™ 2 Power-Transistor, 30 V

Features

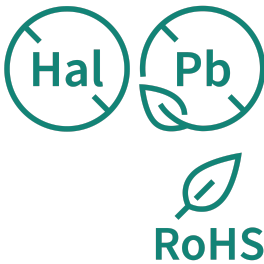
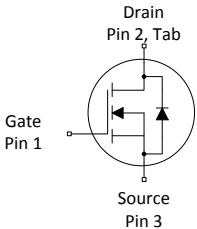
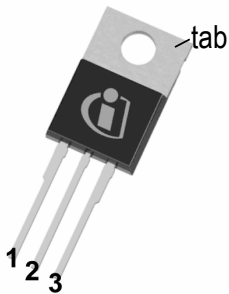
- Optimized for a wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS}$	30	V
$R_{DS(on),max}$	4.95	mΩ
$I_D$	53	A
$Q_{oss}$	17	nC
$Q_g (0V..4.5V)$	10	nC



Type/Ordering Code	Package	Marking	Related Links
IPP050N03LF2S	PG-TO220-3	050N03F2	-



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## 1 Maximum ratings

unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	53 41 21	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{THJA}=40\text{ °C/W}^{2)}$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	212	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	72 143	mJ	$I_D=30\text{ A}$ , $R_{GS}=25\text{ }\Omega$ $I_D=15\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	65 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{THJA}=40\text{ °C/W}^{2)}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.3	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=2\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.35	1.85	2.35	V	$V_{DS}=V_{GS}$ , $I_D=30\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance <sup>6)</sup>	$R_{DS(on)}$	-	4.2 5.2	4.95 7.5	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=15\text{ A}$
Gate resistance	$R_G$	-	1.9	-	$\Omega$	-
Transconductance <sup>7)</sup>	$g_{fs}$	40	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$ , $I_D=30\text{ A}$

<sup>6)</sup>  $R_{DS(on)}$  is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1400	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	290	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	80	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	16	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	12	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	6.4	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics <sup>8)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	4.8	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.5	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	$Q_{gd}$	-	3.2	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	$Q_{sw}$	-	5.5	-	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>9)</sup>	$Q_g$	-	10	15	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.4	-	V	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>9)</sup>	$Q_g$	-	21	32	nC	$V_{DD}=15\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET <sup>9)</sup>	$Q_{g(sync)}$	-	8.9	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge <sup>9)</sup>	$Q_{oss}$	-	17	-	nC	$V_{DS}=15\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

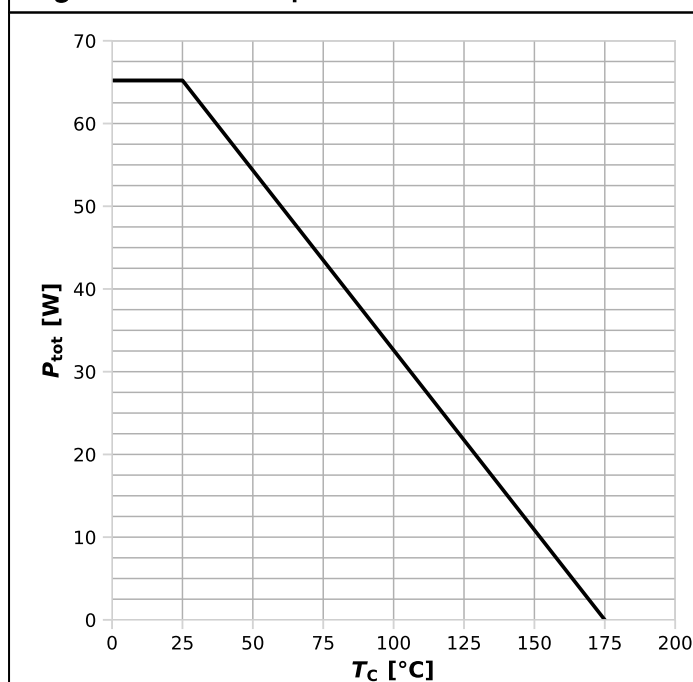
<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	42	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	212	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.85	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=30\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	15	-	ns	$V_R=15\text{ V}$ , $I_F=30\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	33	-	nC	$V_R=15\text{ V}$ , $I_F=30\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$

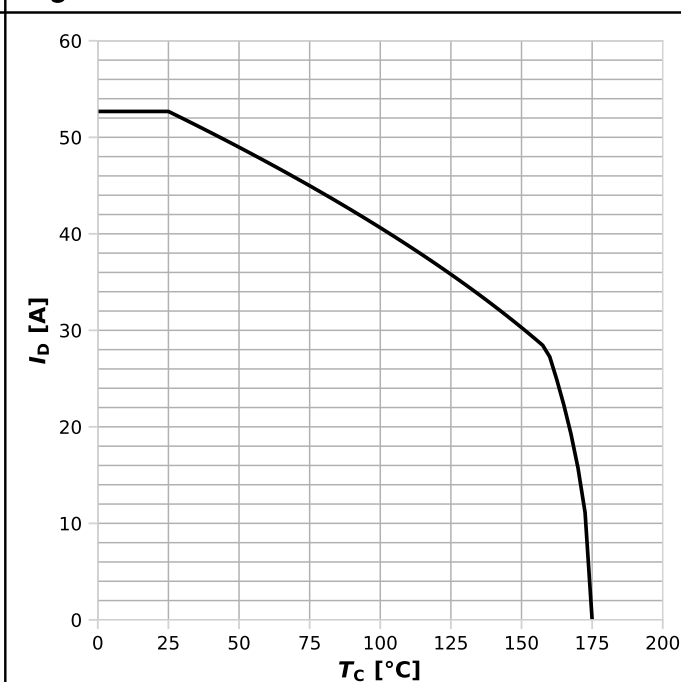
## 4 Electrical characteristics diagrams

Diagram 1: Power dissipation



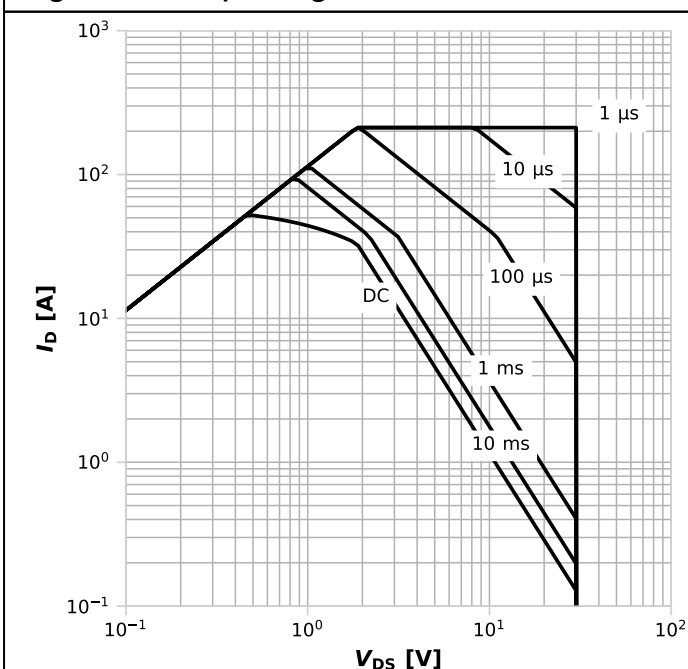
$$P_{tot}=f(T_c)$$

Diagram 2: Drain current



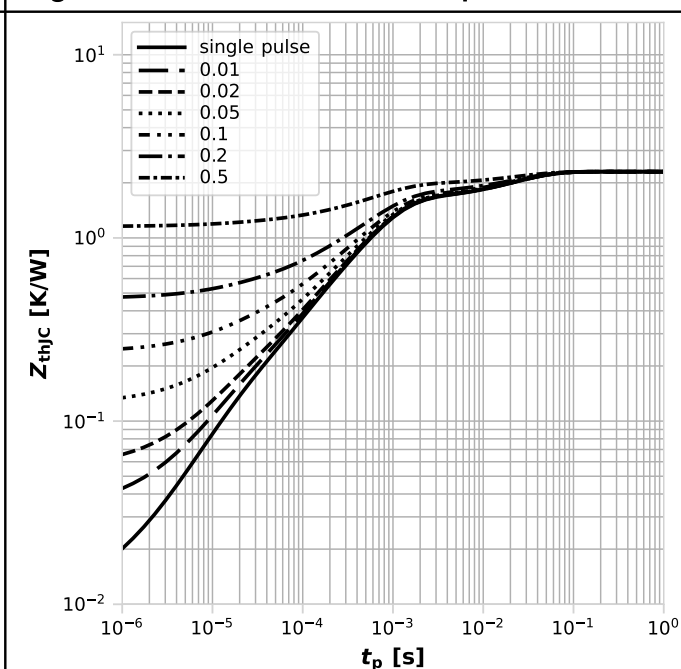
$$I_D=f(T_c); V_{GS}\geq 10\text{ V}$$

Diagram 3: Safe operating area



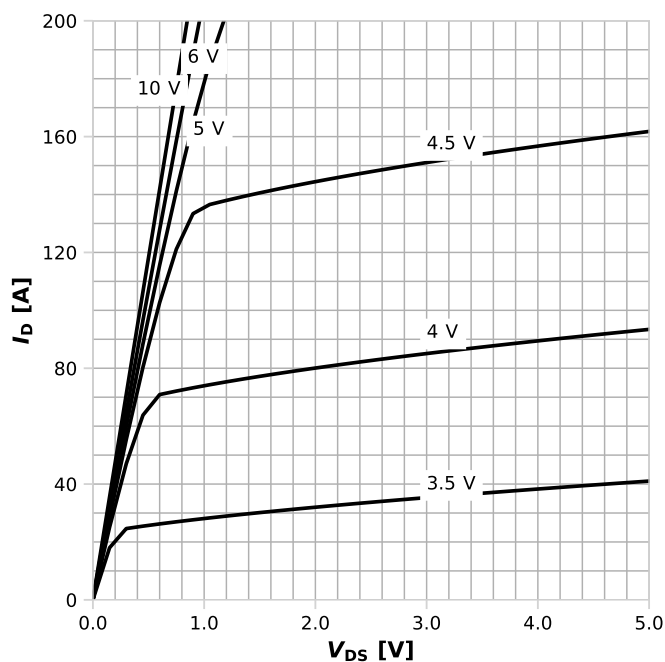
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



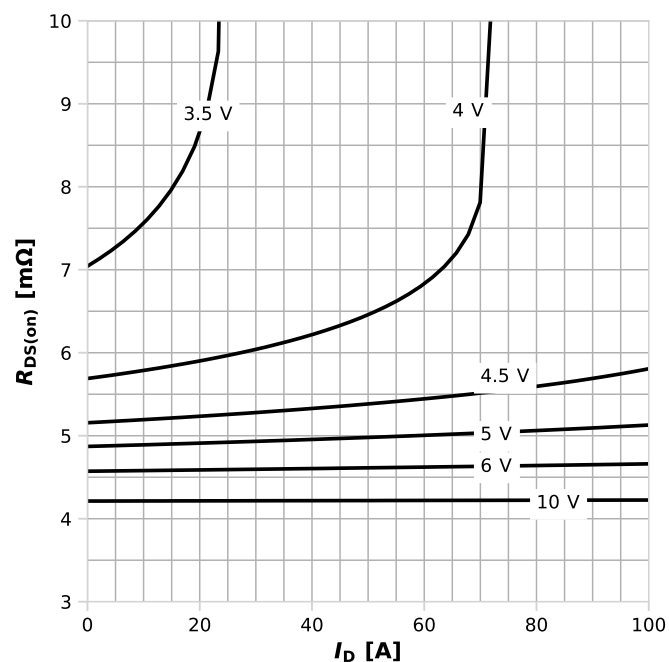
$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

**Diagram 5: Typ. output characteristics**



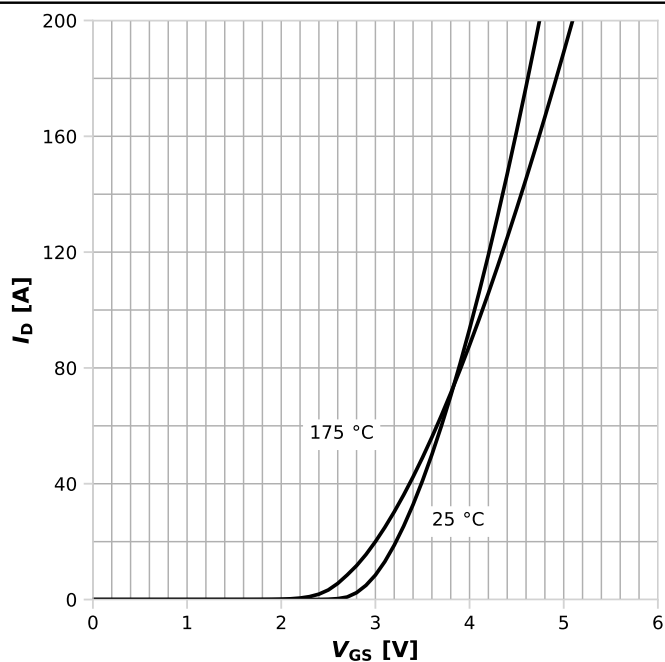
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



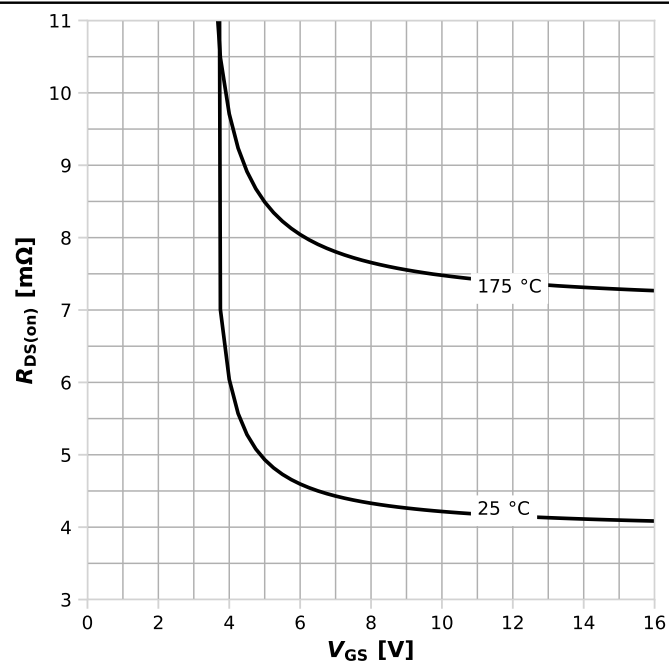
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



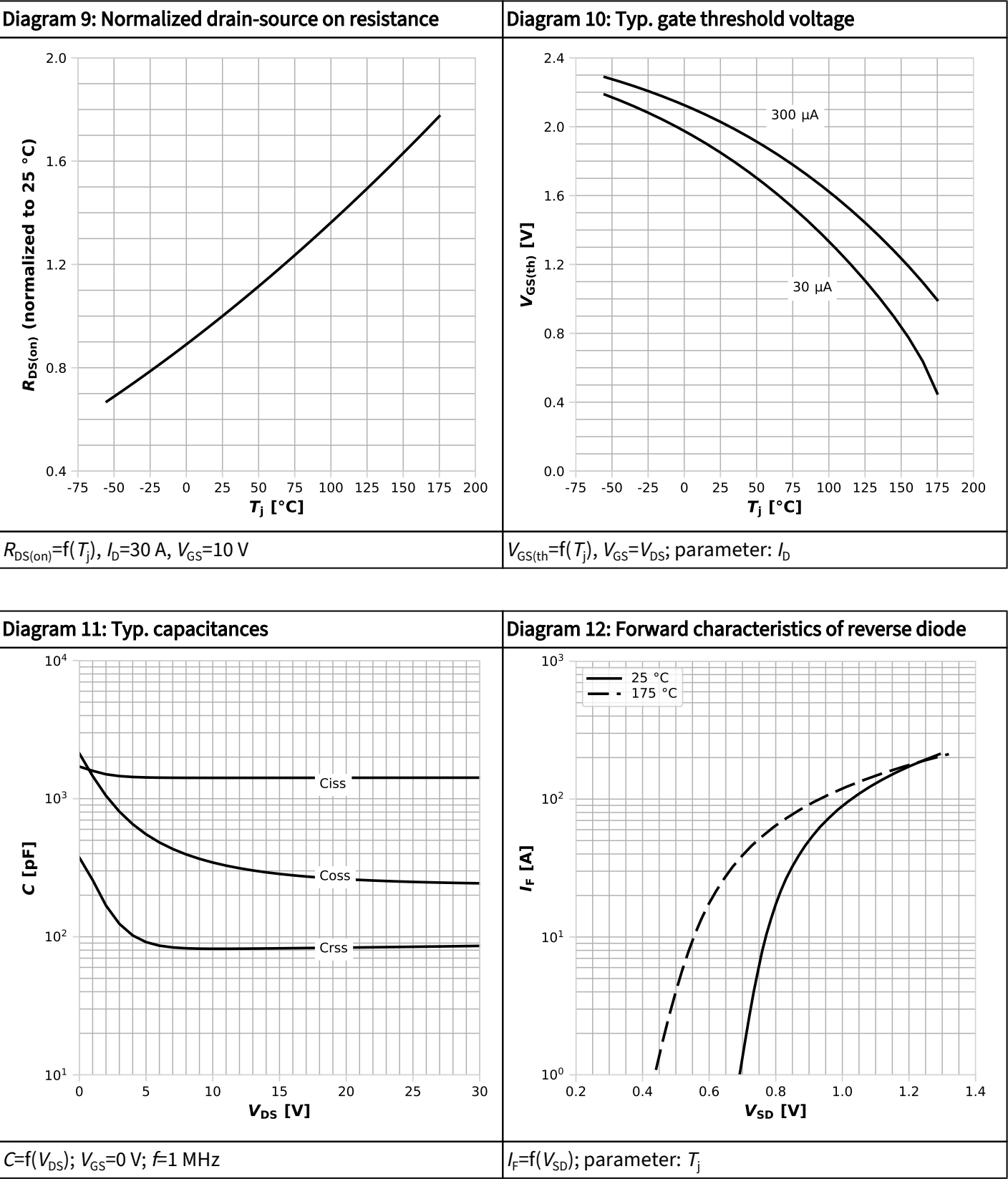
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)\max}$ ; parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**

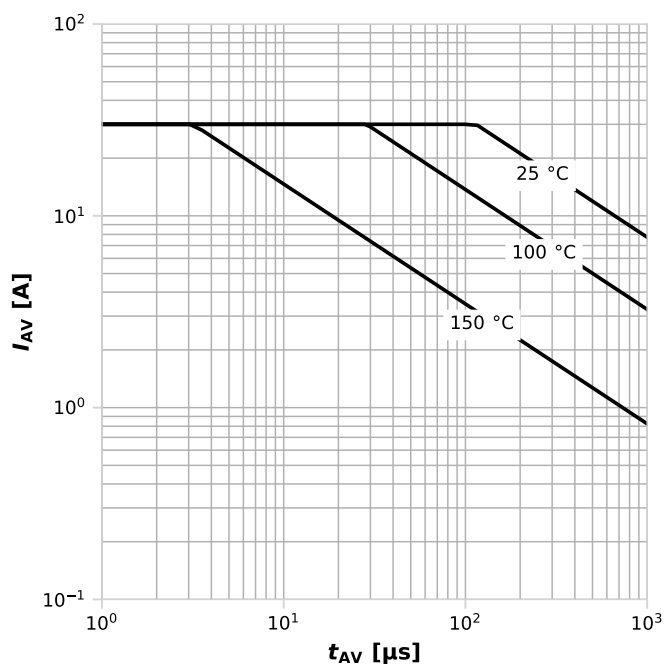


$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 30$  A; parameter:  $T_j$



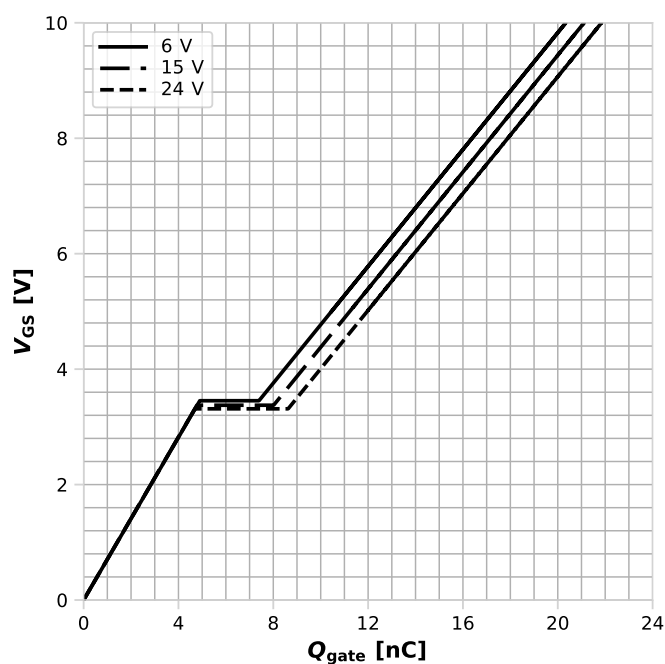


**Diagram 13: Avalanche characteristics**



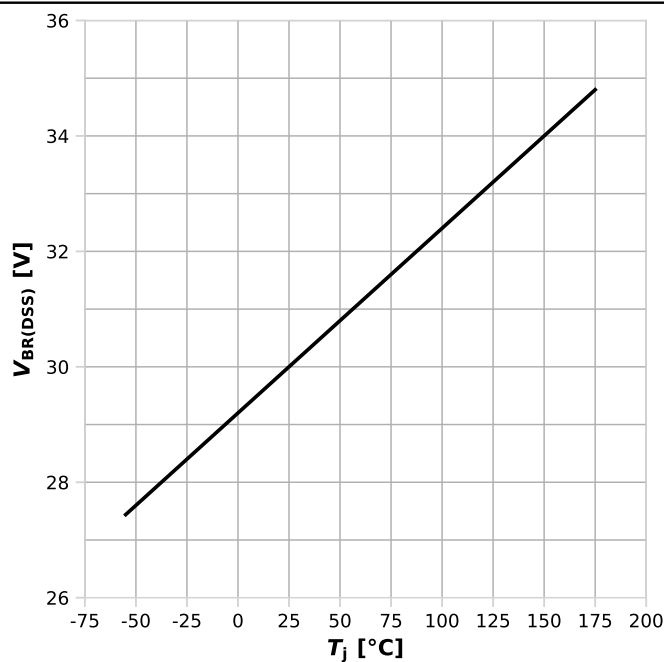
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



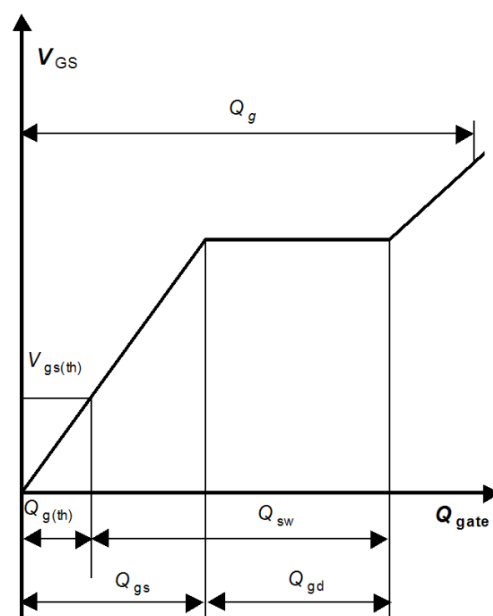
$V_{GS}=f(Q_{gate})$ ,  $I_D=30\text{ A}$  pulsed,  $T_j=25\text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=2\text{ mA}$

**Gate charge waveforms**



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5 Package Outlines

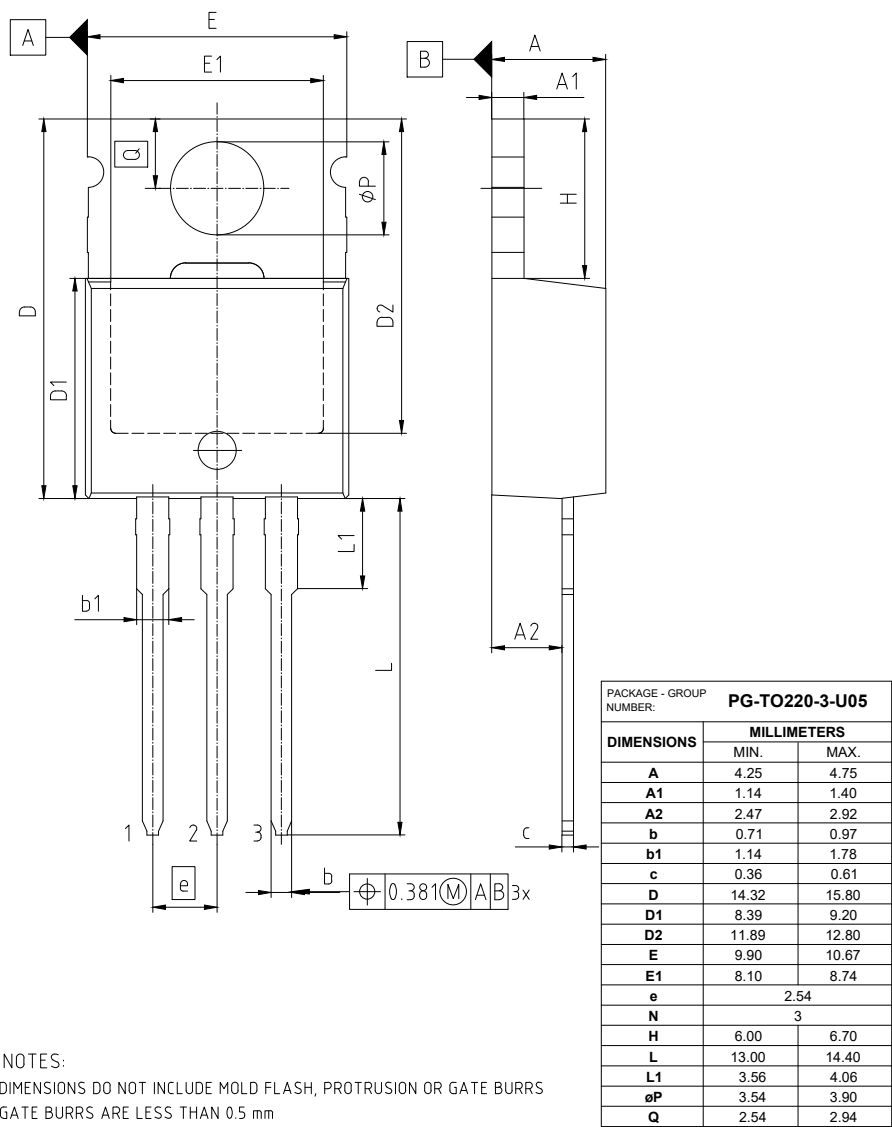


Figure 1 Outline PG-TO220-3, dimensions in mm

Revision History

IPP050N03LF2S

Revision 2024-05-23, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-05-23	Release of final

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