# PerFET™ Power Transistor

## FEATURES

- Excellent FOM
- Reliability meets AEC-Q101 requirements
- Wettable flank leads for enhanced AOI
- 100% UIS and Rg tested
- 175°C operating junction temperature
- RoHS Compliant
- Halogen-free

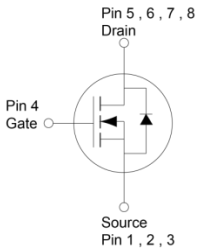
| KEY PERFORMANCE PARAMETERS | | | |
|---|---|---|---|
| **PARAMETER** | | **VALUE** | **UNIT** |
| $V_{DS}$ | | 100 | V |
| $R_{DS(on)}$ (max) | $V_{GS}$ = 10V | 10 | mΩ |
| | $V_{GS}$ = 4.5V | 14 | |
| $Q_g$ | $V_{GS}$ = 4.5V | 13 | nC |

## APPLICATIONS

- Solenoid and motor drivers
- DC-DC converters
- Load Switch
- SMPS

Pb-Free RoHS COMPLIANT HALOGEN FREE

**PDFN56U**




Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted) | | | | |
|---|---|---|---|---|
| **PARAMETER** | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $T_C$ = 25°C | $I_D$ | 72 | A |
| | $T_C$ = 100°C | | 51 | |
| | $T_A$ = 25°C | | 12 | |
| Pulsed Drain Current (Note 1) | | $I_{DM}$ | 288 | A |
| Single Pulse Avalanche Current (Note 2) | | $I_{AS}$ | 14.9 | A |
| Single Pulse Avalanche Energy (Note 2) | | $E_{AS}$ | 33.3 | mJ |
| Total Power Dissipation | $T_C$ = 25°C | $P_D$ | 115 | W |
| | $T_C$ = 125°C | | 38 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | - 55 to +175 | °C |

| THERMAL PERFORMANCE | | | |
|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **LIMIT** | **UNIT** |
| Junction to Case Thermal Resistance | $R_{\Theta JC}$ | 1.3 | °C/W |
| Junction to Ambient Thermal Resistance (Note 3) | $R_{\Theta JA}$ | 50 | °C/W |

**Notes:**

1. Pulse Width ≤ 100μs.
2. L = 0.3mH, $V_{GS}$ = 10V, $R_G$ = 25Ω, Starting $T_J$ = 25°C.
3. Device on a PCB FR4 with 1 $in^2$ (single layer, 2 oz thickness) copper area for drain connection.

| **ELECTRICAL SPECIFICATIONS** ($T_A$ = 25°C unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **CONDITIONS** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 1mA | $BV_{DSS}$ | 100 | -- | -- | V |
| Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | $V_{GS(TH)}$ | 1.4 | 1.6 | 2.2 | V |
| Gate Body Leakage | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | $I_{GSS}$ | -- | -- | ±100 | nA |
| Drain-Source Leakage Current | $V_{GS}$ = 0V, $V_{DS}$ = 100V | $I_{DSS}$ | -- | -- | 1 | μA |
| | $V_{GS}$ = 0V, $V_{DS}$ = 100V<br>$T_J$ = 125°C | | -- | -- | 100 | |
| Drain-Source On-State Resistance (Note 4) | $V_{GS}$ = 10V, $I_D$ = 36A | $R_{DS(on)}$ | -- | 7.4 | 10 | mΩ |
| | $V_{GS}$ = 4.5V, $I_D$ = 36A | | -- | 9.1 | 14 | |
| Forward Transconductance (Note 4) | $V_{DS}$ = 10V, $I_D$ = 9A | $g_{fs}$ | -- | 53 | -- | S |
| **Dynamic** (Note 5) | | | | | | |
| Total Gate Charge | $V_{DS}$ = 50V, $I_D$ = 12A,<br>$V_{GS}$ = 4.5V | $Q_g$ | -- | 13 | -- | nC |
| Total Gate Charge | $V_{DS}$ = 50V, $I_D$ = 12A,<br>$V_{GS}$ = 10V | $Q_g$ | -- | 25 | -- | nC |
| Gate-Source Charge | | $Q_{gs}$ | -- | 5.3 | -- | |
| Gate-Drain Charge | | $Q_{gd}$ | -- | 3.8 | -- | |
| Input Capacitance | $V_{DS}$ = 60V, $V_{GS}$ = 0V,<br>f = 1.0MHz | $C_{iss}$ | -- | 1363 | -- | pF |
| Output Capacitance | | $C_{oss}$ | -- | 228 | -- | |
| Reverse Transfer Capacitance | | $C_{rss}$ | -- | 26 | -- | |
| Gate Resistance | f = 1.0MHz | Rg | -- | 0.5 | -- | Ω |
| **Switching** (Note 6) | | | | | | |
| Turn-On Delay Time | $V_{DD}$ = 50V, $R_G$ = 6Ω,<br>$I_D$ = 12A, $V_{GS}$ = 10V | $t_{d(on)}$ | -- | 8.6 | -- | ns |
| Turn-On Rise Time | | $t_r$ | -- | 24 | -- | |
| Turn-Off Delay Time | | $t_{d(off)}$ | -- | 26 | -- | |
| Turn-Off Fall Time | | $t_f$ | -- | 52 | -- | |
| **Source-Drain Diode** | | | | | | |
| Forward Voltage (Note 4) | $I_S$ = 36A, $V_{GS}$ = 0V | $V_{SD}$ | -- | -- | 1.1 | V |
| Reverse Recovery Time | $I_S$ = 12A,<br>di/dt = 100A/μs | $t_{rr}$ | -- | 62 | -- | ns |
| Reverse Recovery Charge | | $Q_{rr}$ | -- | 95 | -- | nC |

**Notes:**

4. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
5. Defined by design. Not subject to production test.
6. Switching time is essentially independent of operating temperature.

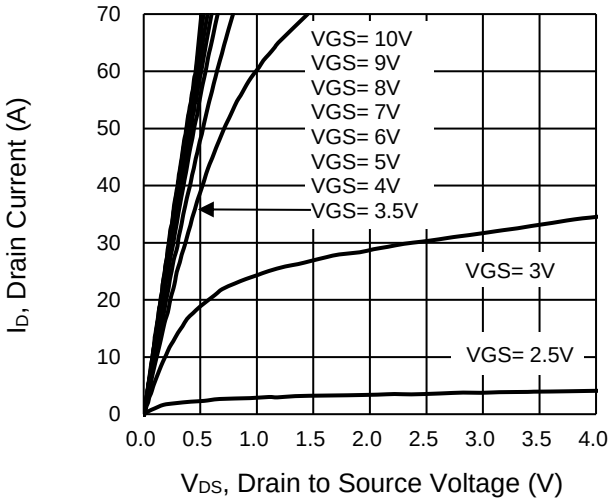
## ORDERING INFORMATION

| ORDERING CODE | PACKAGE | PACKING |
|---|---|---|
| TSM100NH10LCR RLG | PDFN56U | 2,500pcs / 13” Reel |

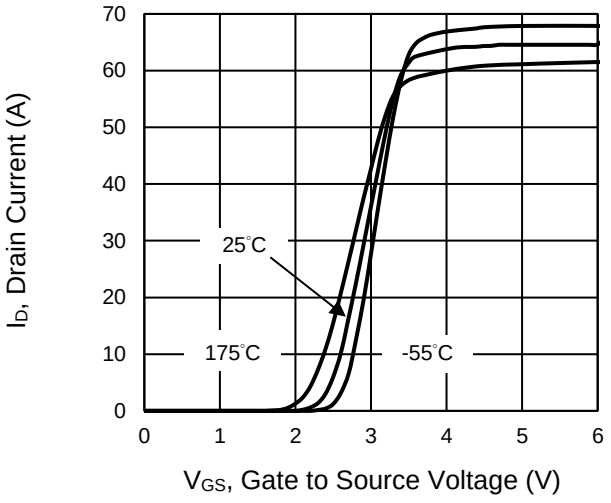
## CHARACTERISTICS CURVES

($T_A$ = 25°C unless otherwise noted)

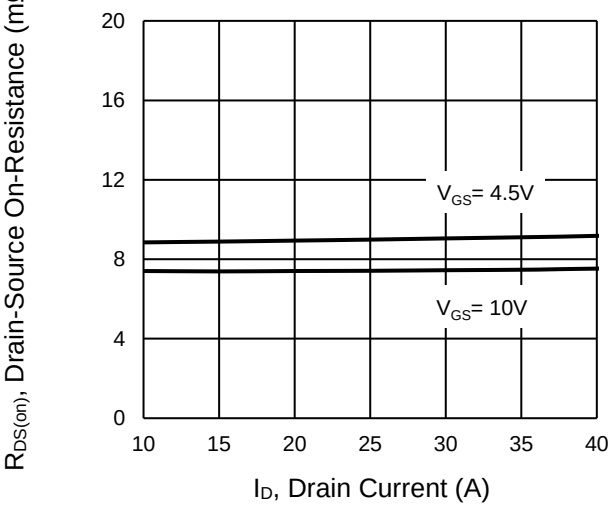
**Output Characteristics**



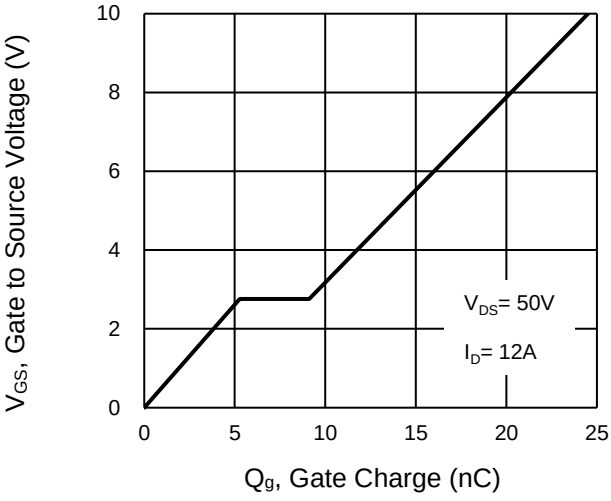

**Transfer Characteristics**



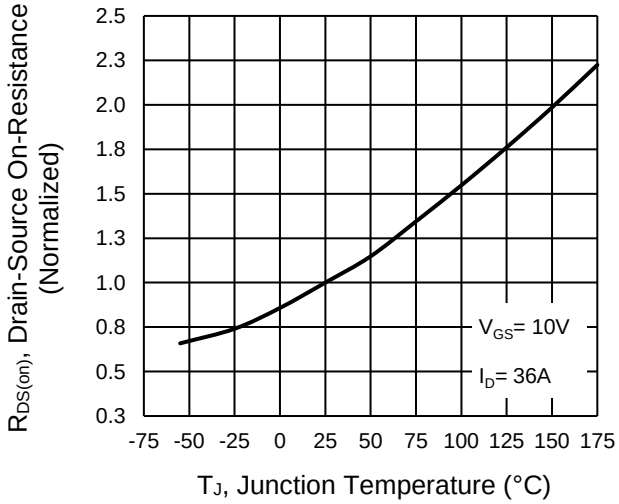

**On-Resistance vs. Drain Current**



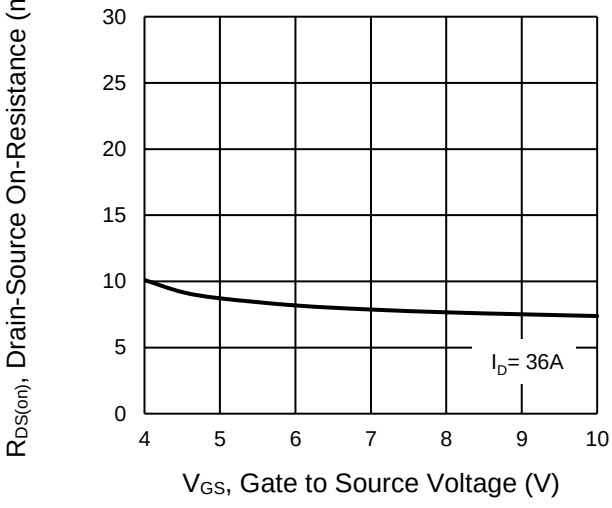

**Gate-Source Voltage vs. Gate Charge**




**On-Resistance vs. Junction Temperature**



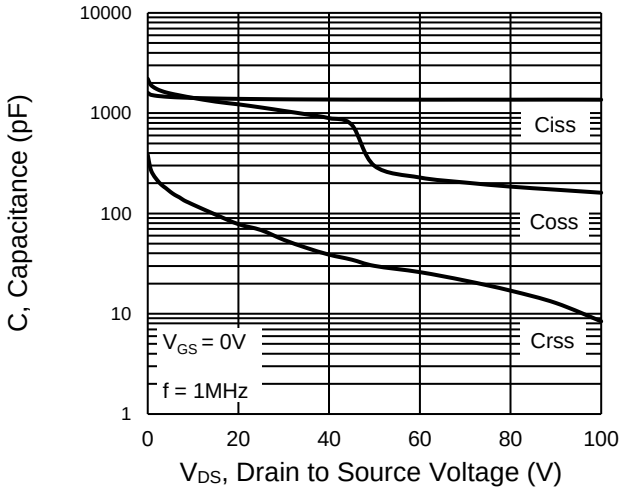

**On-Resistance vs. Gate-Source Voltage**



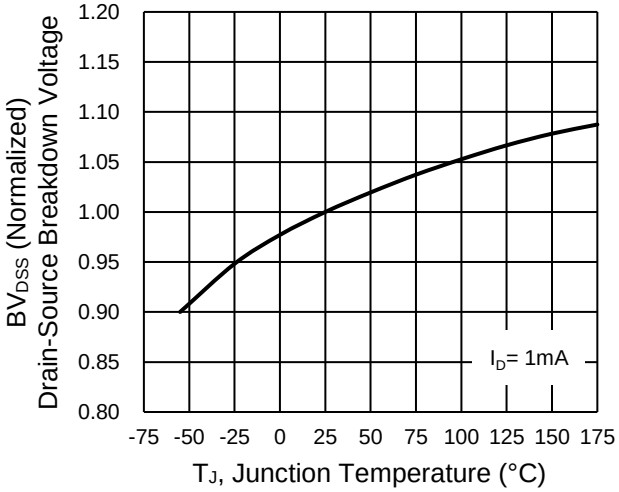
## CHARACTERISTICS CURVES

($T_A$ = 25°C unless otherwise noted)

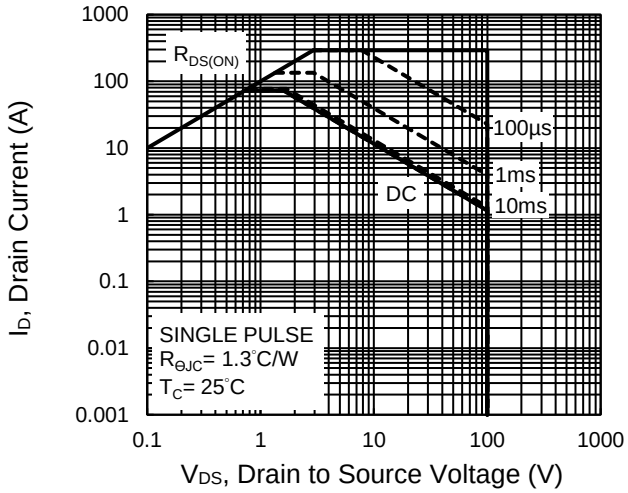
**Capacitance vs. Drain-Source Voltage**



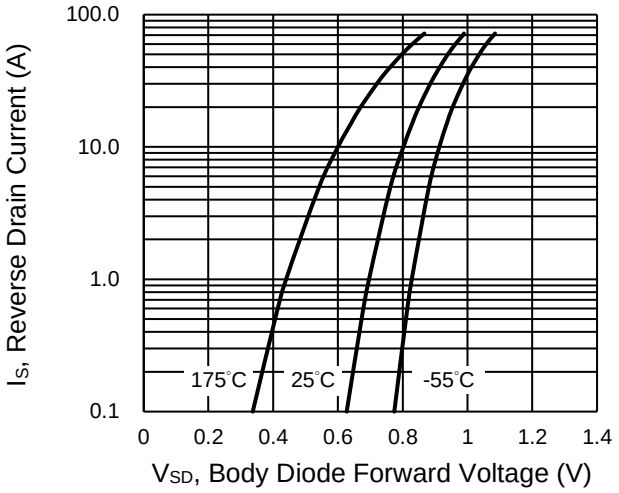

**$BV_{DSS}$ vs. Junction Temperature**



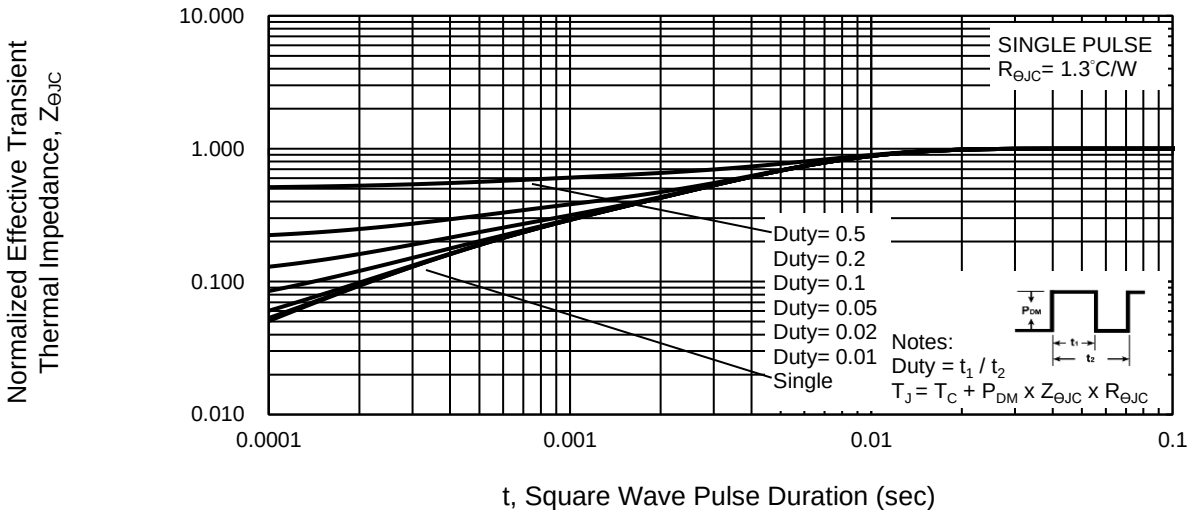

**Maximum Safe Operating Area, Junction-to-Case**




**Source-Drain Diode Forward Current vs. Voltage**



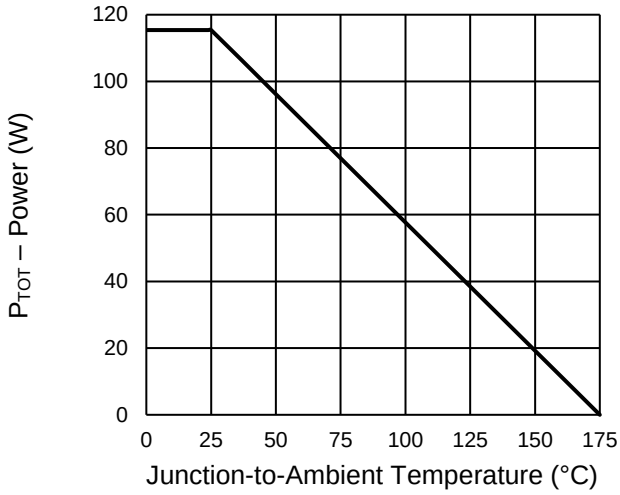

**Normalized Thermal Transient Impedance, Junction-to-Case**



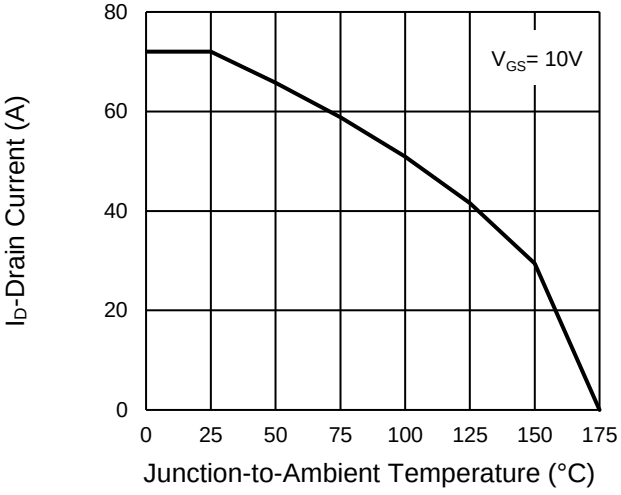
## CHARACTERISTICS CURVES

($T_A$ = 25°C unless otherwise noted)

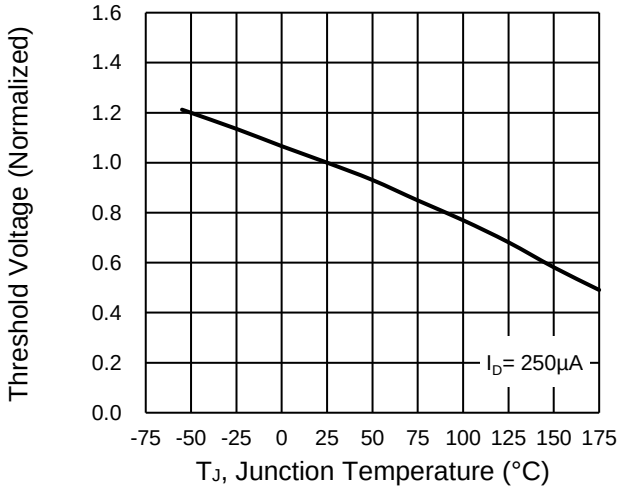
**Power Dissipation**




**Drain Current**

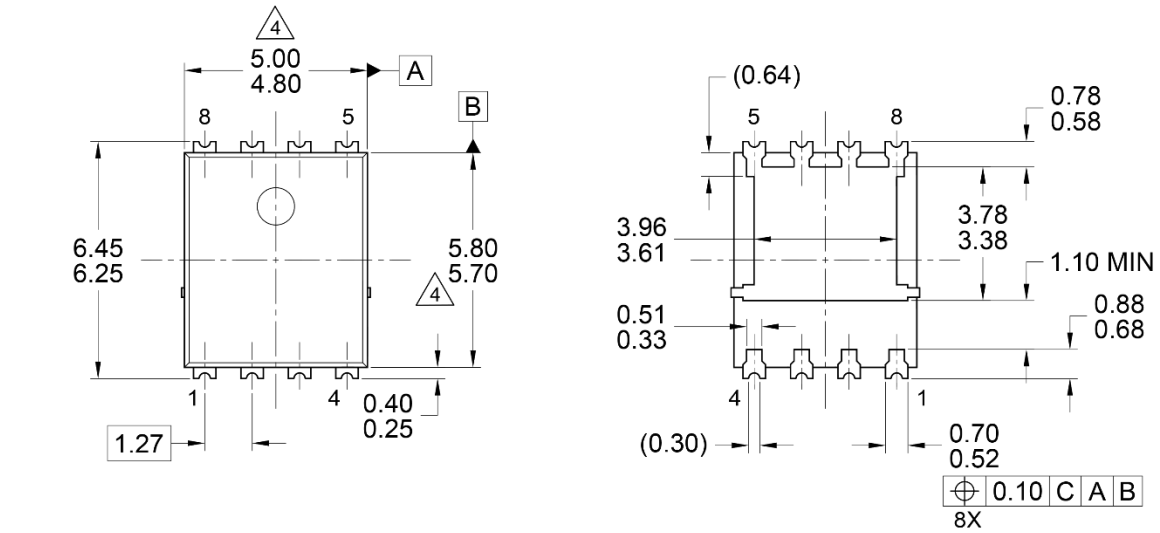


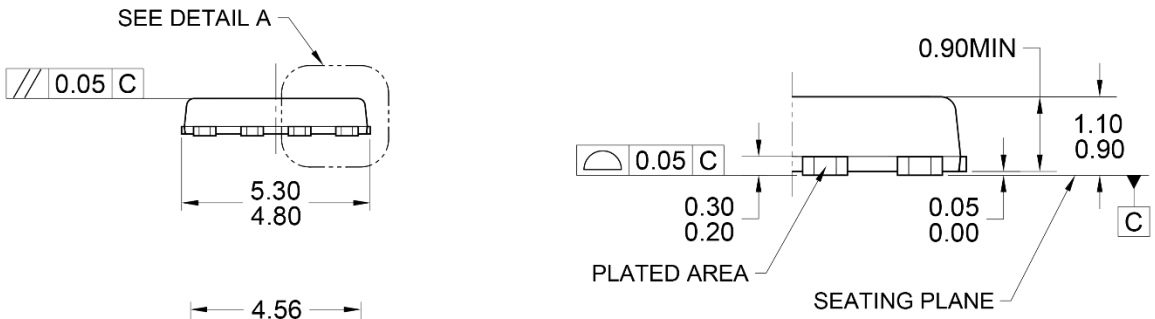

**Normalized gate threshold voltage vs Temperature**



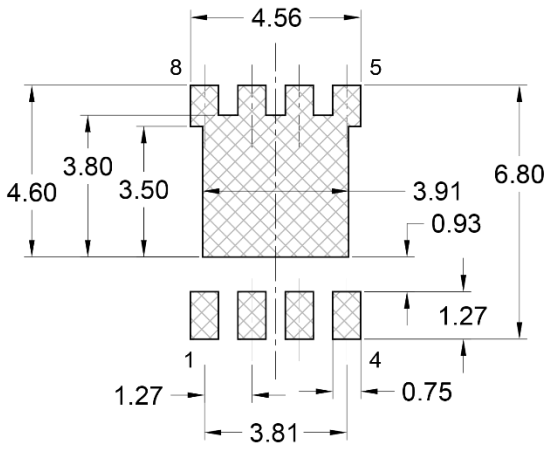
## PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

**PDFN56U**

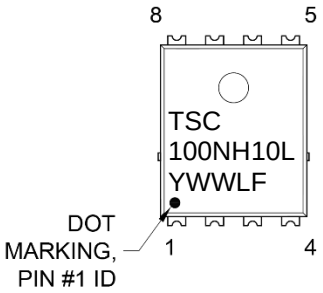



DETAIL A
(SCALE 2:1)




SUGGESTED PAD LAYOUT
(REFERENCE ONLY)




MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

| | |
|---|---|
| 100NH10L | = Device marking |
| Y | = Year code |
| WW | = Week code (01~52) |
| L | = Lot code (1~9,A~Z) |
| F | = Factory code |

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