UNIT



Taiwan Semiconductor

# **N-Channel Power MOSFET**

# **FEATURES**

- Latest super-junction technology
- Low gate charge capacitance

Low gate charge capacitance	V <sub>DS</sub> @ T <sub>i,max</sub>	650	V	
<ul><li>High gate noise immunity</li><li>RoHS compliant</li></ul>	R <sub>DS(on)</sub> (max)	84	mΩ	
Halogen-free	$Q_{g,typ}$	68	nC	

### **APPLICATIONS**

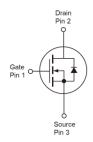
- Switching applications
- HV motor driver
- Industrial



**KEY PERFORMANCE PARAMETERS** 

**VALUE** 





**PARAMETER** 

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	600	V	
Gate-Source Voltage		V <sub>G</sub> s	±30	V	
Continuous Drain Current	$T_C = 25^{\circ}C$	ID	42	Α	
Pulsed Drain Current (Note 1)		I <sub>DM</sub>	168	Α	
Total Power Dissipation @ T <sub>C</sub> = 25°C		P <sub>D</sub>	357	W	
Single Pulse Avalanche Energy (Note 2	)	Eas	612	mJ	
Single Pulse Avalanche Current (Note 2)		I <sub>AS</sub>	5	А	
Operating Junction and Storage Tem	perature Range	T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	Rejc	0.35	°C/W	
Junction to Ambient Thermal Resistance (Note 3)	Reja	50	°C/W	

#### Notes:

- 1. Pulse Width ≤ 100µs.
- 2. L = 50mH,  $R_G$  = 25 $\Omega$ , Starting  $T_J$  = 25 $^{\circ}$ C.
- 3. Reja is the sum of the junction-to-case and case-to-ambient thermal resistances. Reja is guaranteed by design while Reja is determined by the user's board design.

1



<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V$ , $I_D = 1mA$	BV <sub>DSS</sub>	600			V
Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 2.9 \text{mA}$	V <sub>GS(TH)</sub>	4	4.7	6	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>			100	μA
	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A	_		71	84	mΩ
Drain-Source On-State Resistance	V <sub>GS</sub> = 12V, I <sub>D</sub> = 14A	R <sub>DS(on)</sub>		68	80	
Dynamic (Note 5)	•					
Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 42A, V <sub>GS</sub> = 10V	Qg		68		nC
Gate-Source Charge		Qgs		23		
Gate-Drain Charge		Q <sub>gd</sub>		37		
Input Capacitance		C <sub>iss</sub>		2939		
Output Capacitance	$V_{DS} = 300V, V_{GS} = 0V,$	Coss		81		pF
Reverse Transfer Capacitance	f = 100kHz	Crss		6		
Gate Resistance	f = 1.0Hz	Rg		0.9		Ω
Switching (Note 6)						
Turn-On Delay Time		t <sub>d(on)</sub>		44		
Turn-On Rise Time	$V_{DD} = 300V, R_G = 3.3\Omega,$ $I_D = 42A, V_{GS} = 10V$	t <sub>r</sub>		68		
Turn-Off Delay Time		t <sub>d(off)</sub>		66		ns
Turn-Off Fall Time		t <sub>f</sub>		41		
Source-Drain Diode				•		•
Forward Voltage (Note 4)	I <sub>S</sub> = 14A, V <sub>GS</sub> = 0V	V <sub>SD</sub>		0.9	1.5	V
Reverse Recovery Time	I <sub>S</sub> = 21A	t <sub>rr</sub>		438		ns
Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs	Qrr		9		μC
		•	•		•	

### Notes:

- 4. Pulse test: Pulse Width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

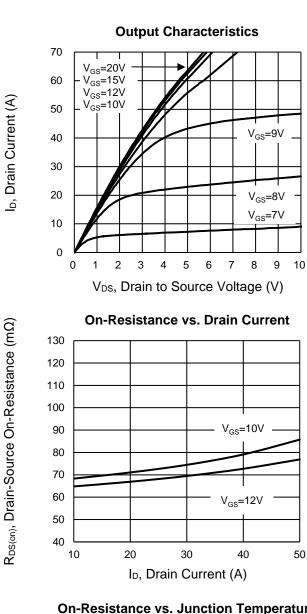
# **ORDERING INFORMATION**

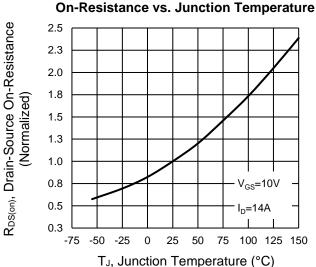
ORDERING CODE	PACKAGE	PACKING
TSM60NE084PW C0G	TO-247	30pcs / Tube

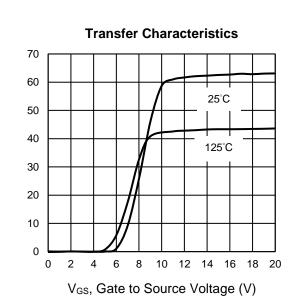


# **CHARACTERISTICS CURVES**

(T<sub>C</sub> = 25°C unless otherwise noted)





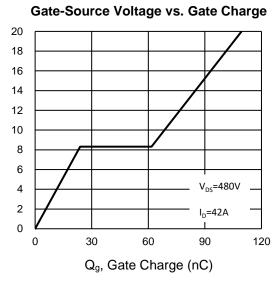


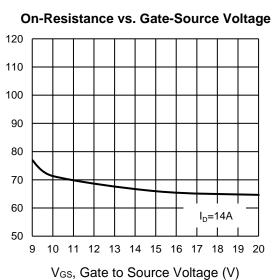
Ip, Drain Current (A)

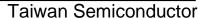
V<sub>GS</sub>, Gate to Source Voltage (V)

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})},$  Drain-Source On-Resistance (m $\Omega$ )

3









### **CHARACTERISTICS CURVES**

(T<sub>C</sub> = 25°C unless otherwise noted)

=0V

100kHz

100

200

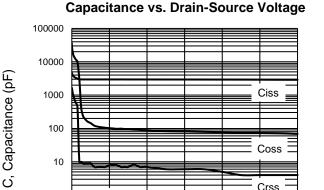
1

0.1

Normalized Effective Transient

Thermal Impedance, Zeuc

0



BV<sub>DSS</sub> vs. Junction Temperature 1.20 Drain-Source Breakdown Voltage 1.15 BV<sub>DSS</sub> (Normalized) 1.10 1.05 1.00 0.95 0.90 0.85  $I_D = 1 \text{mA}$ 0.80 -50 25 50 100 125 150 T<sub>J</sub>, Junction Temperature (°C)

Maximum Safe Operating Area, Junction-to-Case

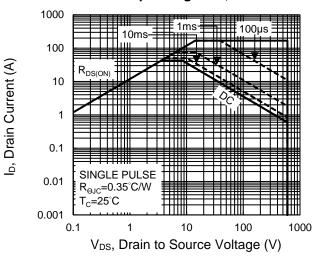
300

V<sub>DS</sub>, Drain to Source Voltage (V)

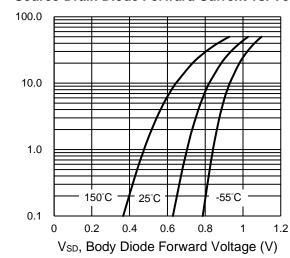
400

500

600

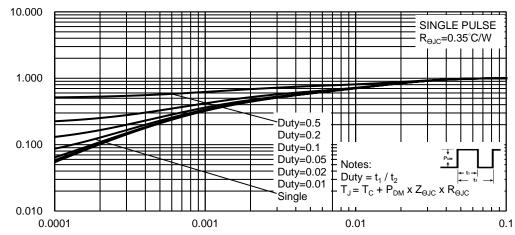


Source-Drain Diode Forward Current vs. Voltage



Normalized Thermal Transient Impedance, Junction-to-Case

Reverse Drain Current (A)



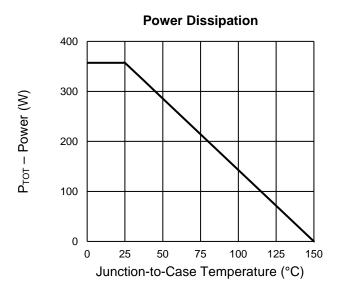
t, Square Wave Pulse Duration (sec)

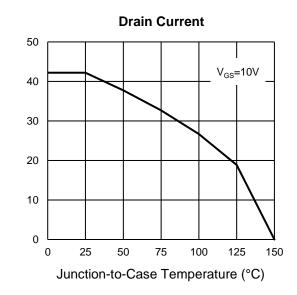




# **CHARACTERISTICS CURVES**

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

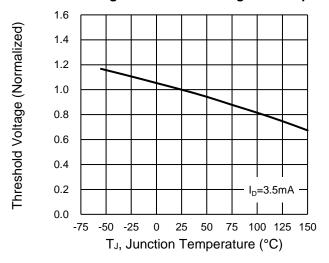




Ip-Drain Current (A)

5

# Normalized gate threshold voltage vs Temperature

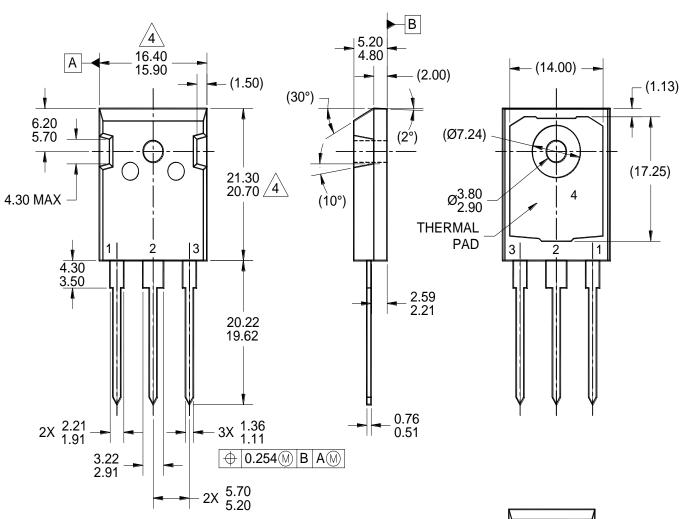




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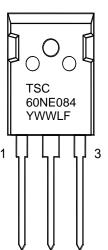
# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

### TO-247



### NOTES: UNLESS OTHERWISE SPECIFIED

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PACKAGE OUTLINE REFERENCE: JEDEC TO-247, VARIATION AD, ISSUE E.
- MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
- 5. DWG NO. REF: HQ2SD07-TO247AD-071 REV C.



MARKING DIAGRAM

Y = YEAR CODE

WW = WEEK CODE (01~52)

L = LOT CODE (1~9, A~Z)

F = FACTORY CODE



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