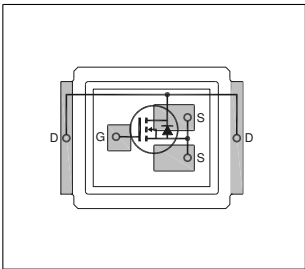
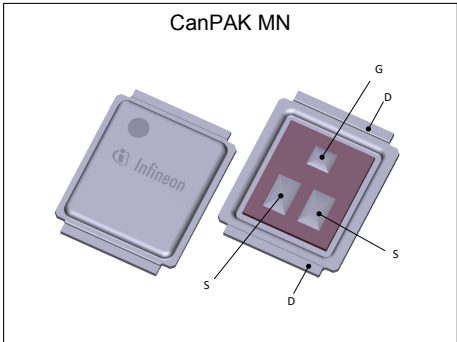


MOSFET

OptiMOS™ 3 Power-MOSFET, 100 V

Features

- Pb-free plating; RoHS compliant
- Dual sided cooling
- Low profile (<0.7 mm)
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Optimized for high switching frequency DC/DC converter
- Low parasitic inductance
- Halogen-free according to IEC61249-2-21



RoHS

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	5.6	mΩ
I_D	83	A
Q_{OSS}	73	A
Q_g (typ)	56	A

Type / Ordering Code	Package	Marking	Related Links
BSB056N10NN3 G	MG-WDSO5-5	0110	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	83 52 9	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=45\text{ K/W}^{1)}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	332	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	450	mJ	$I_D=30\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	78 2.8	-	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=45\text{ K/W}^{1)}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	-	1.6	K/W	-
Thermal resistance, junction - case, bottom	R_{thJC}	-	1	-	K/W	-
Device on PCB, 6 cm ² cooling area ¹⁾	R_{thJA}	-	-	45	K/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See figure 3 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5	V	$V_{DS}=V_{GS}$, $I_D=100\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	10 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5 6.2	5.6 8.1	m Ω	$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=15\text{ A}$
Gate resistance	R_G	-	0.5	-	Ω	-
Transconductance	g_{fs}	34	69	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4100	5500	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	750	1000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	27	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Fall time	t_f	-	8	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	17	-	nC	$V_{DD}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	9.7	-	nC	$V_{DD}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	20	-	nC	$V_{DD}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	56	74	nC	$V_{DD}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.2	-	V	$V_{DD}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	73	97	-	$V_{DD}=50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	65	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	316	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=I_S$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	64	-	ns	$V_R=50\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	174	-	nC	$V_R=50\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

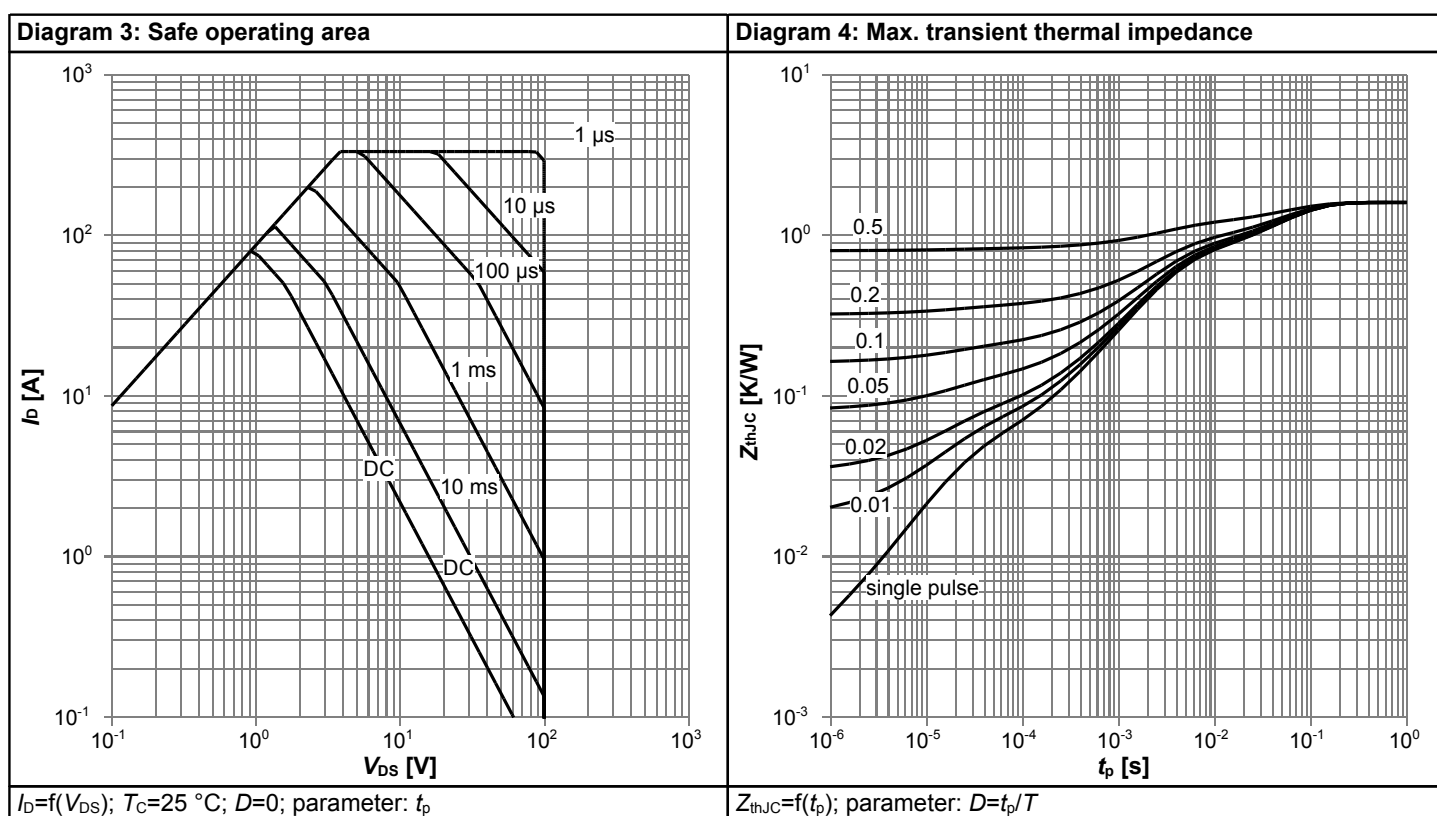
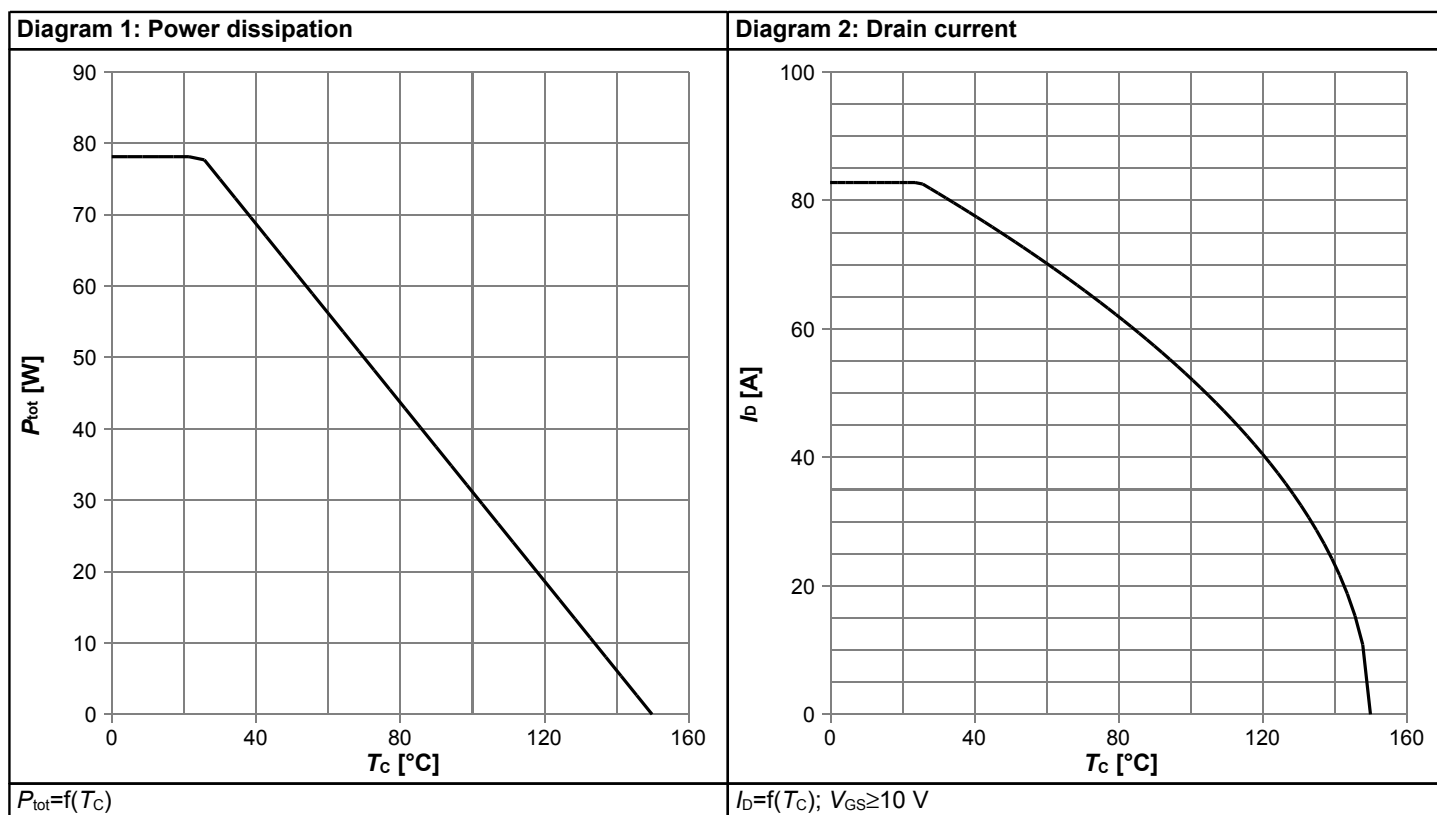
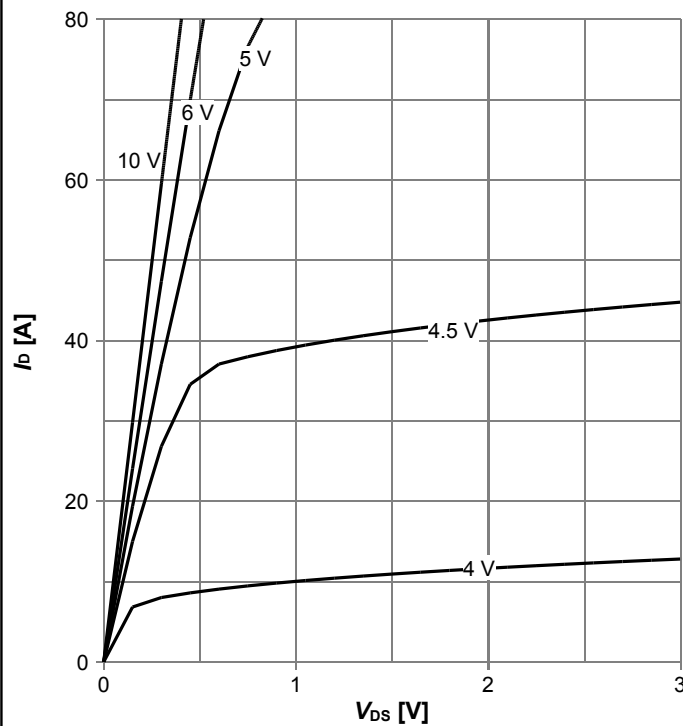
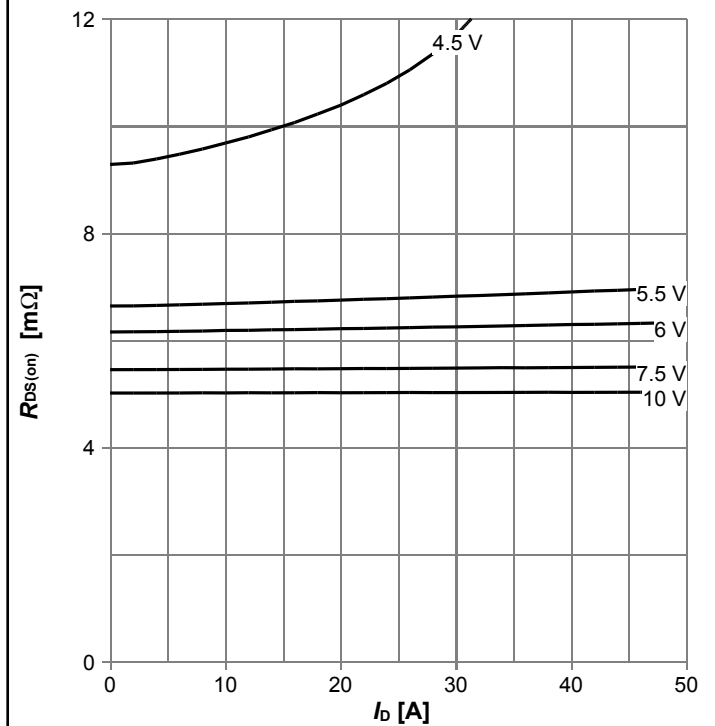


Diagram 5: Typ. output characteristics



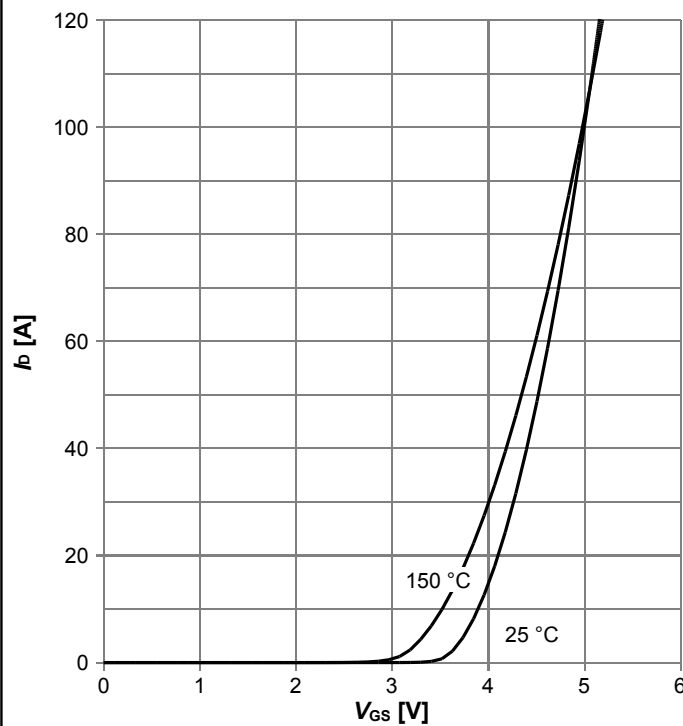
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



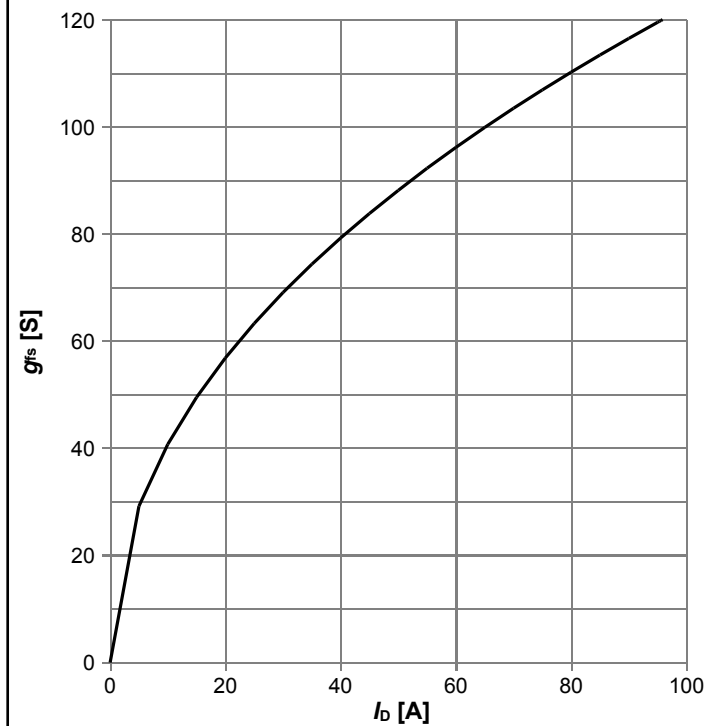
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



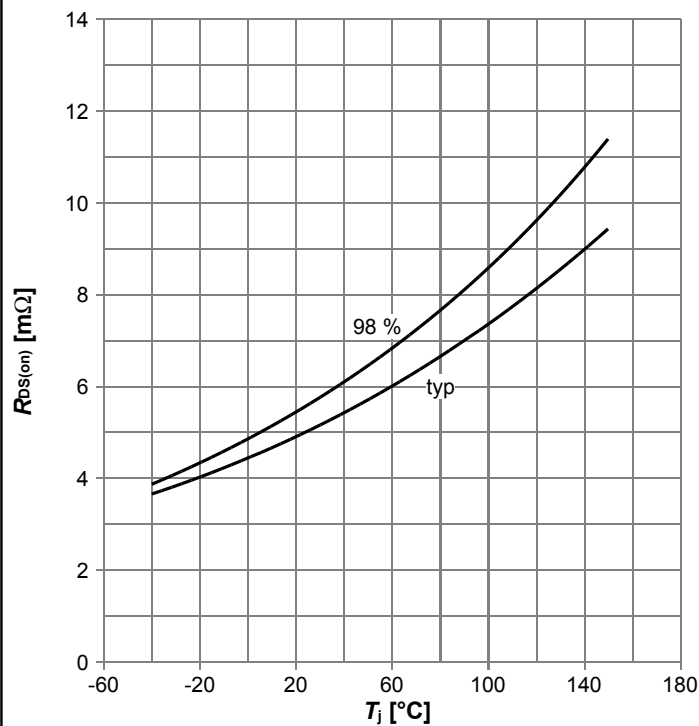
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



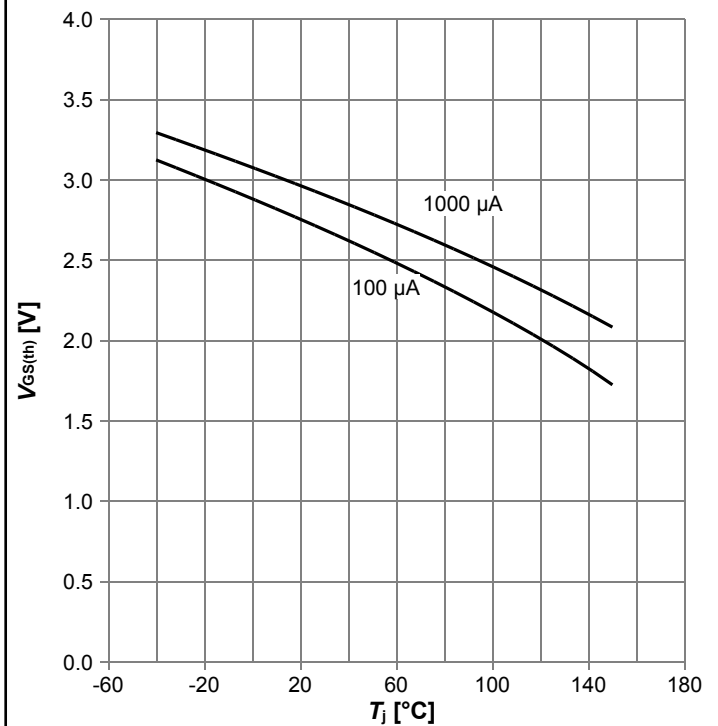
$g_{fs} = f(I_D)$; $T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



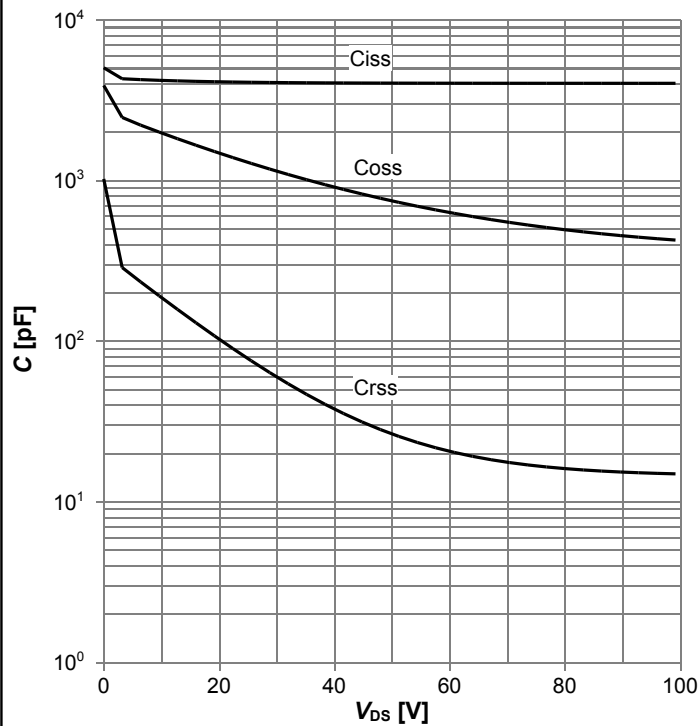
$R_{DS(on)} = f(T_j)$; $I_D = 30$ A; $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



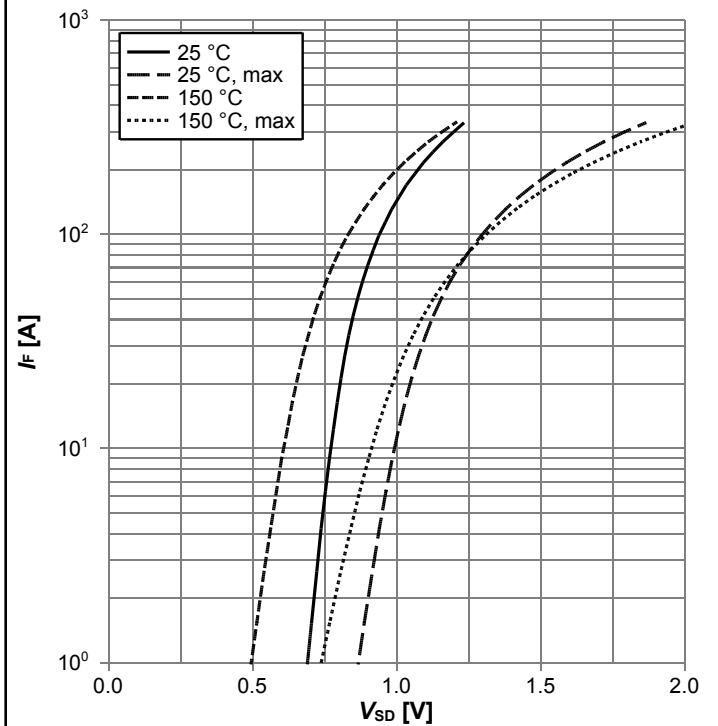
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

Diagram 11: Typ. capacitances



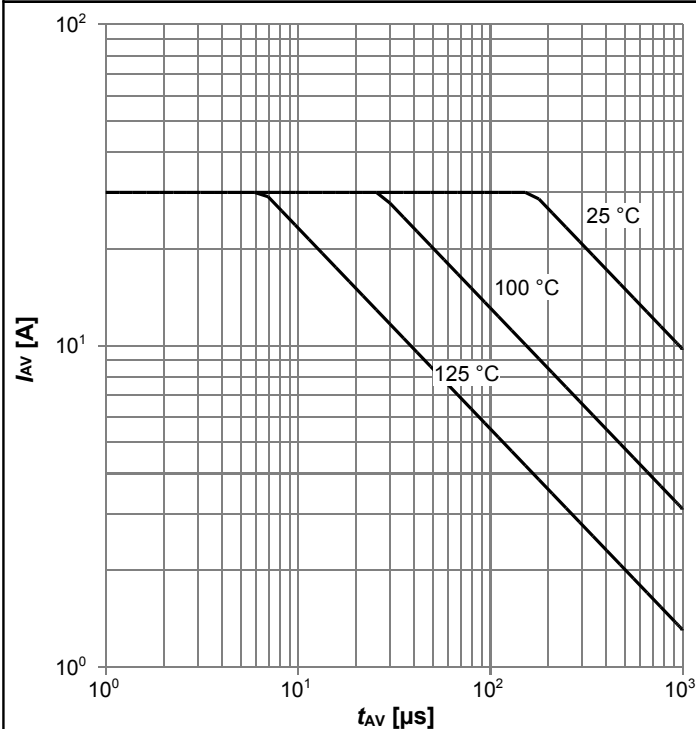
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



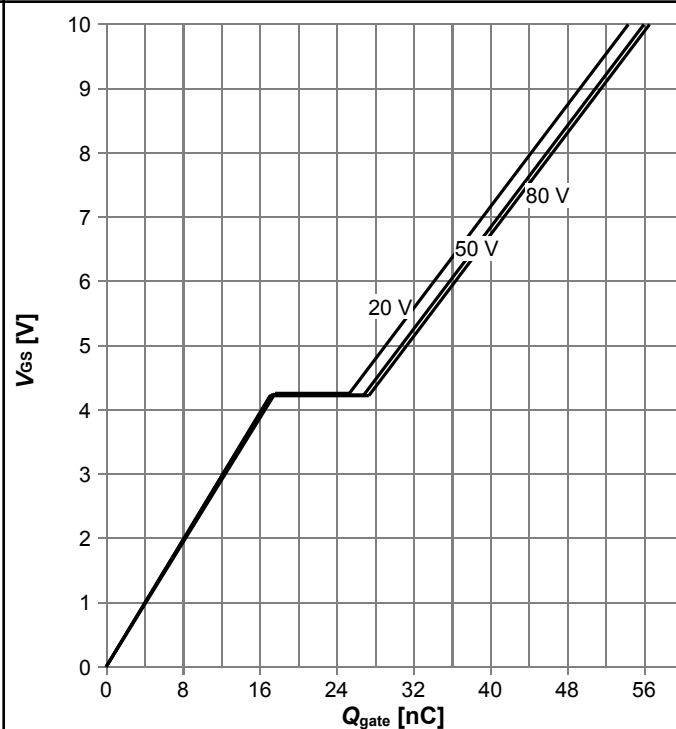
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



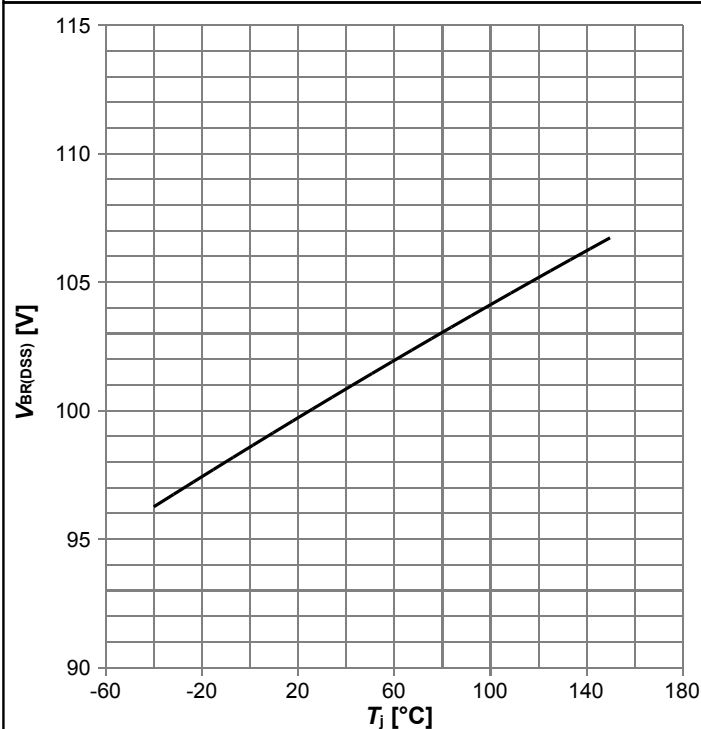
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



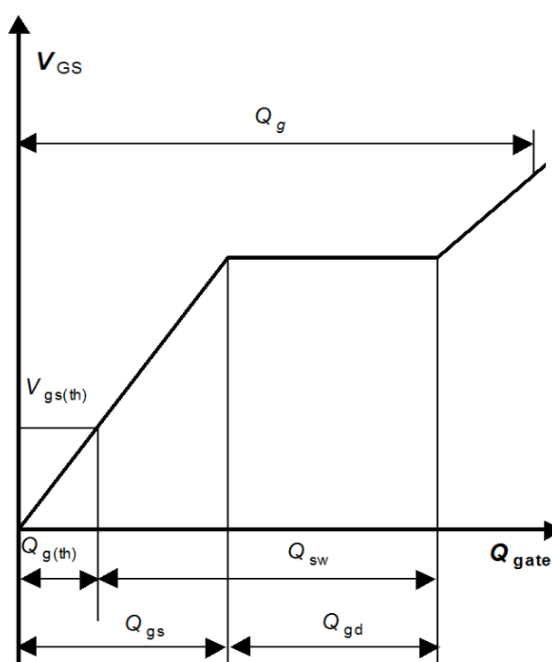
$V_{GS}=f(Q_{gate})$; $I_D=30\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_J)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines

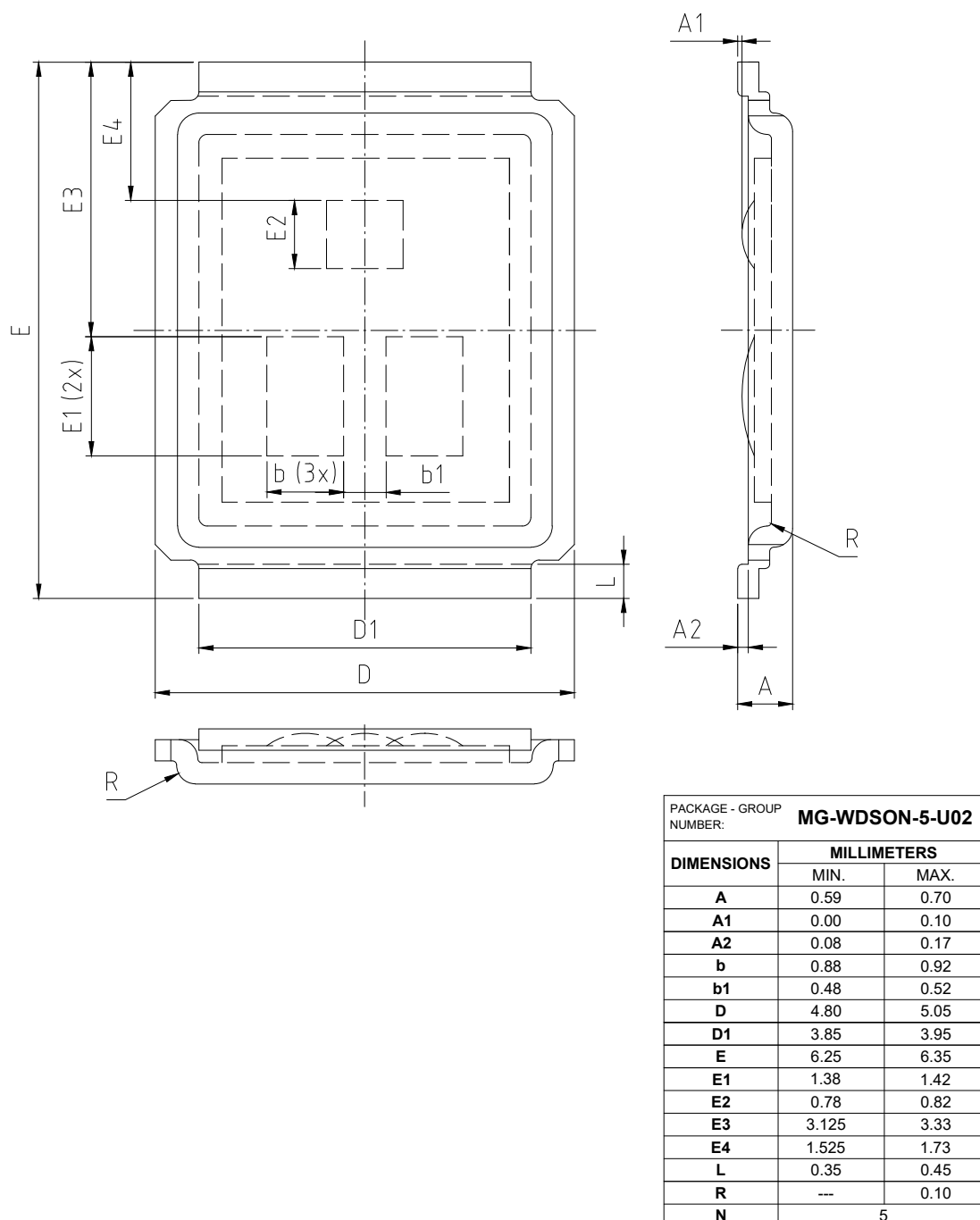
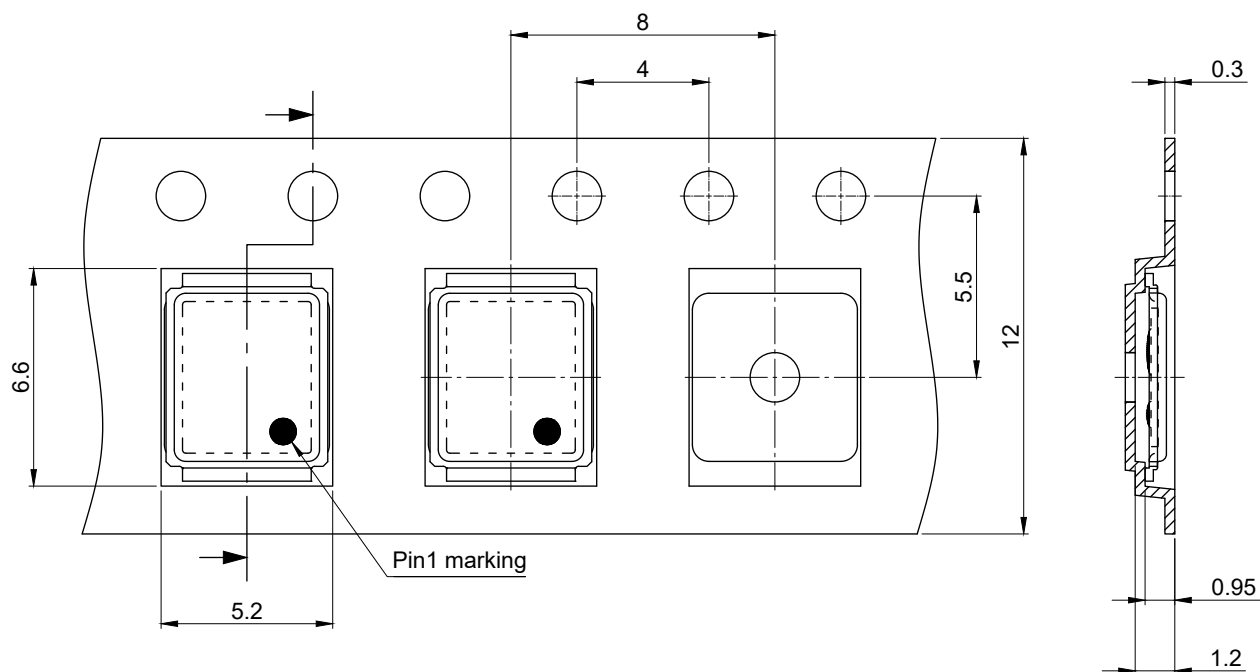


Figure 1 Outline MG-WDSO-5, dimensions in mm




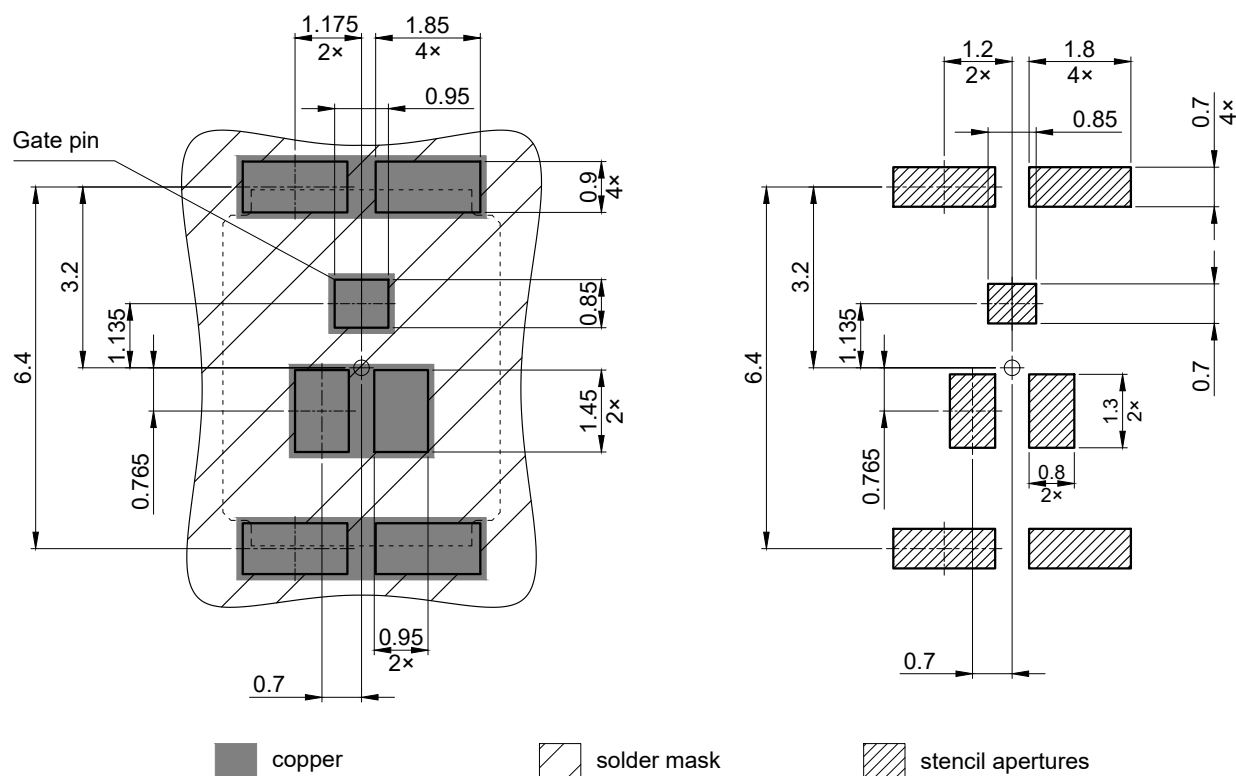
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 2 Outline Tape (MG-WDSO-5), dimensions in mm



All dimensions are in units mm
All pads are solder mask defined

Figure 3 Outline Footprint (MG-WDSO-5), dimensions in mm

Revision History

BSB056N10NN3 G

Revision: 2023-10-12, Rev. 2.6

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.6	2023-10-12	Update package nomenclature

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