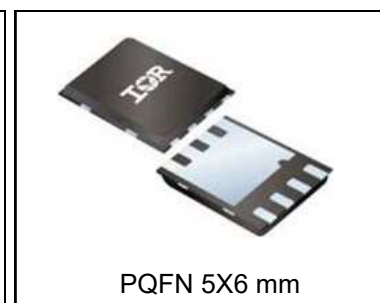
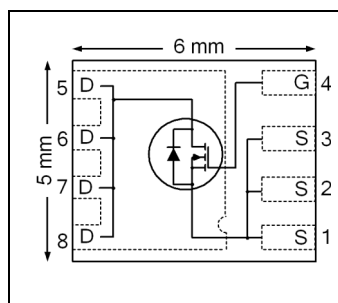


V_{DSS}	25	V
R_{DS(on)} max (@ V _{GS} = 10V)	0.95	mΩ
(@ V _{GS} = 4.5V)	1.60	
Qg (typical)	56	nC
I_D (@ T _{C (Bottom)} = 25°C)	324	A



Applications

- OR-ing MOSFET for 12V (typical) Bus in-Rush Current
- Battery Operated DC Motor Inverters

Features

Low R _{DS(on)} (<0.95mΩ)
Low Thermal Resistance to PCB (<0.8°C/W)
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Industrial Qualification

results in



Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH8201PbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH8201TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	49	A
I _D @ T _{C (Bottom)} = 25°C	Continuous Drain Current, V _{GS} @ 10V ⑤	324	
I _D @ T _{C (Bottom)} = 100°C	Continuous Drain Current, V _{GS} @ 10V ⑤	205	
I _{DM}	Pulsed Drain Current	1296	
P _D @ T _A = 25°C	Power Dissipation ④	3.6	W
P _D @ T _{C (Bottom)} = 25°C	Power Dissipation ④	156	
	Linear Derating Factor ④	0.029	W/°C
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 9

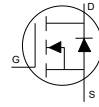
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	20	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.80	0.95	mΩ	V _{GS} = 10V, I _D = 50A ②
		—	1.20	1.60		V _{GS} = 4.5V, I _D = 50A ②
V _{GS(th)}	Gate Threshold Voltage	1.35	1.80	2.35	V	V _{DS} = V _{GS} , I _D = 150μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.1	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 20V, V _{GS} = 0V
		—	—	150		V _{DS} = 20V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	181	—	—	S	V _{DS} = 10V, I _D = 50A
Q _g	Total Gate Charge	—	111	—	nC	V _{GS} = 10V, V _{DS} = 13V, I _D = 50A
Q _g	Total Gate Charge	—	56	84	nC	V _{DS} = 13V V _{GS} = 4.5V I _D = 50A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	16	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	7.0	—		
Q _{gd}	Gate-to-Drain Charge	—	18	—		
Q _{godr}	Gate Charge Overdrive	—	15	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	25	—	nC	V _{DS} = 16V, V _{GS} = 0V
Q _{oss}	Output Charge	—	39	—		
R _G	Gate Resistance	—	1.1	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	27	—	ns	V _{DD} = 13V, V _{GS} = 4.5V I _D = 50A R _G = 4.7Ω
t _r	Rise Time	—	54	—		
t _{d(off)}	Turn-Off Delay Time	—	31	—		
t _f	Fall Time	—	22	—		
C _{iss}	Input Capacitance	—	7330	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1730	—		V _{DS} = 13V
C _{rss}	Reverse Transfer Capacitance	—	850	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ①	—	437	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	156	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)	—	—	1296		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	25	38	ns	T _J = 25°C, I _F = 50A, V _{DD} = 13V di/dt = 400A/μs ②
Q _{rr}	Reverse Recovery Charge	—	57	86	nC	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ③	0.5	0.8	°C/W
R _{θJC} (Top)	Junction-to-Case ③	—	21	
R _{θJA}	Junction-to-Ambient ④	—	35	
R _{θJA} (<10s)	Junction-to-Ambient ④	—	20	

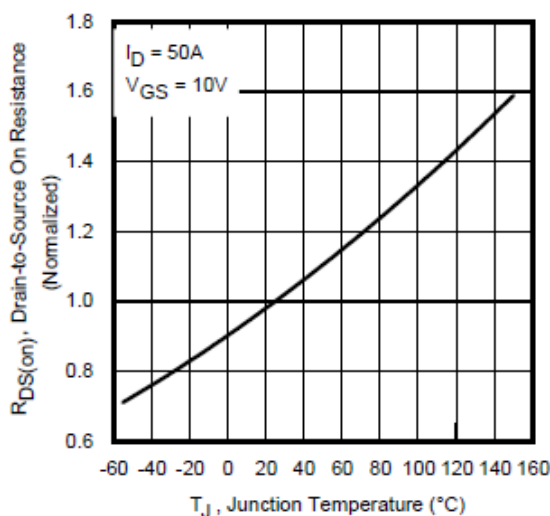
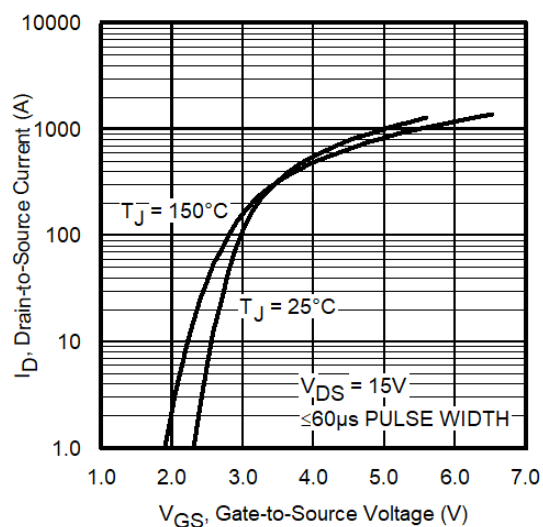
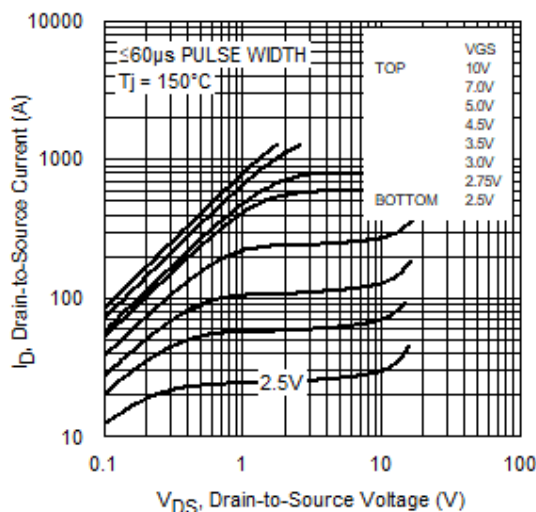
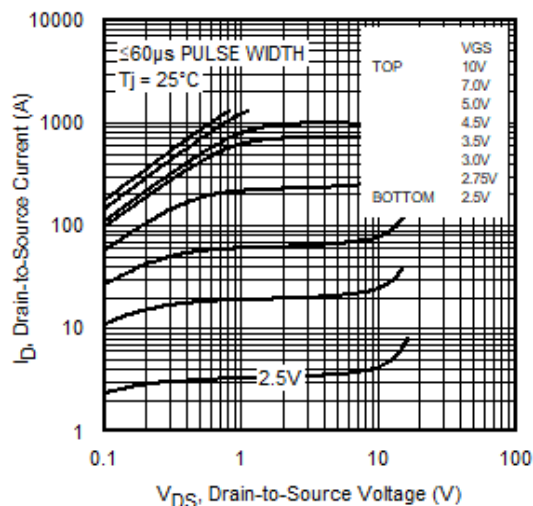


Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

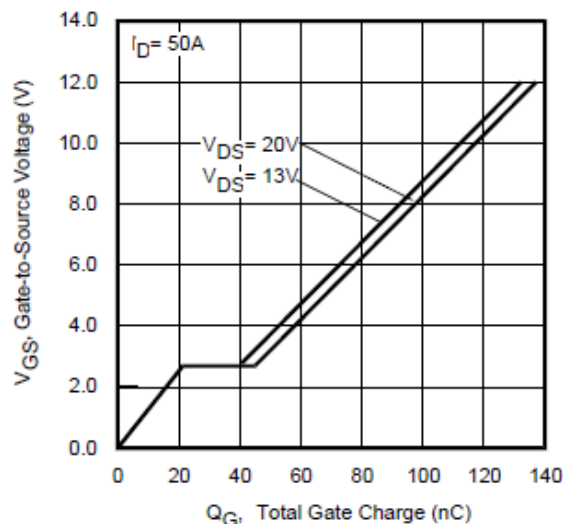
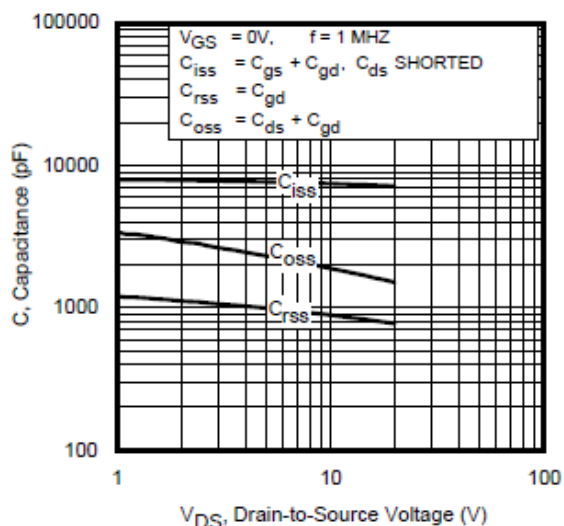
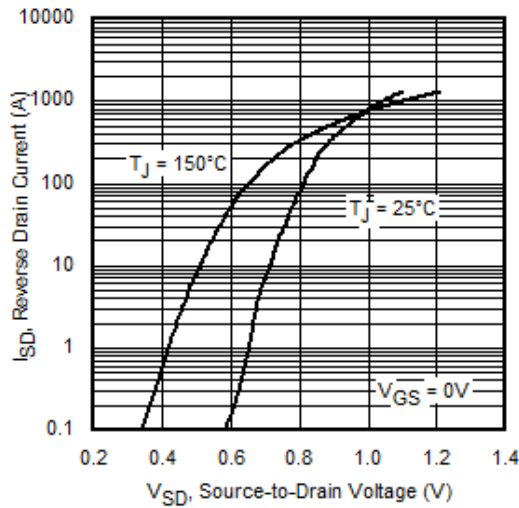
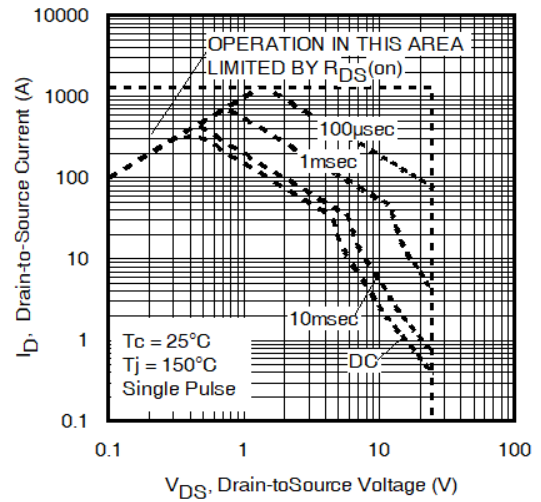
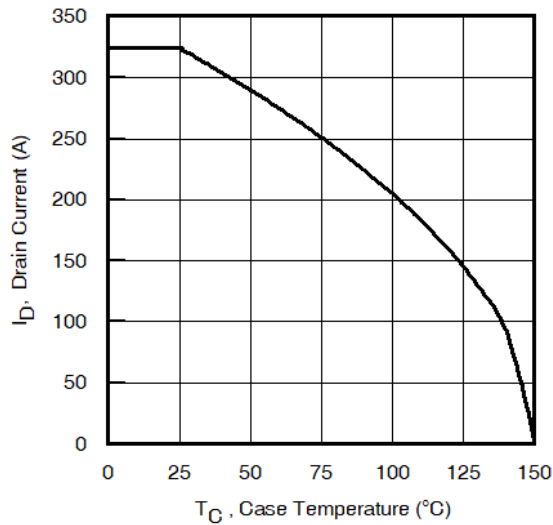
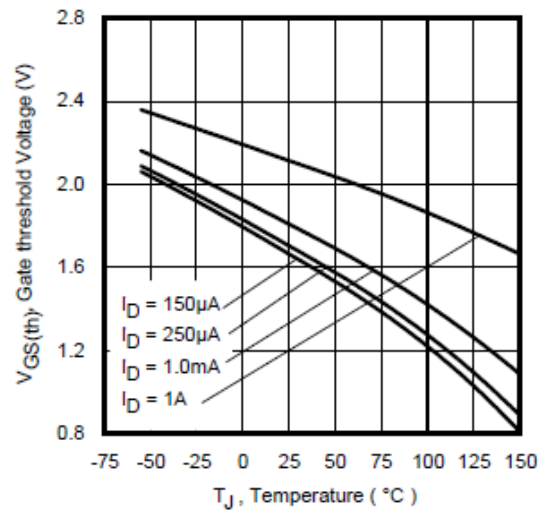
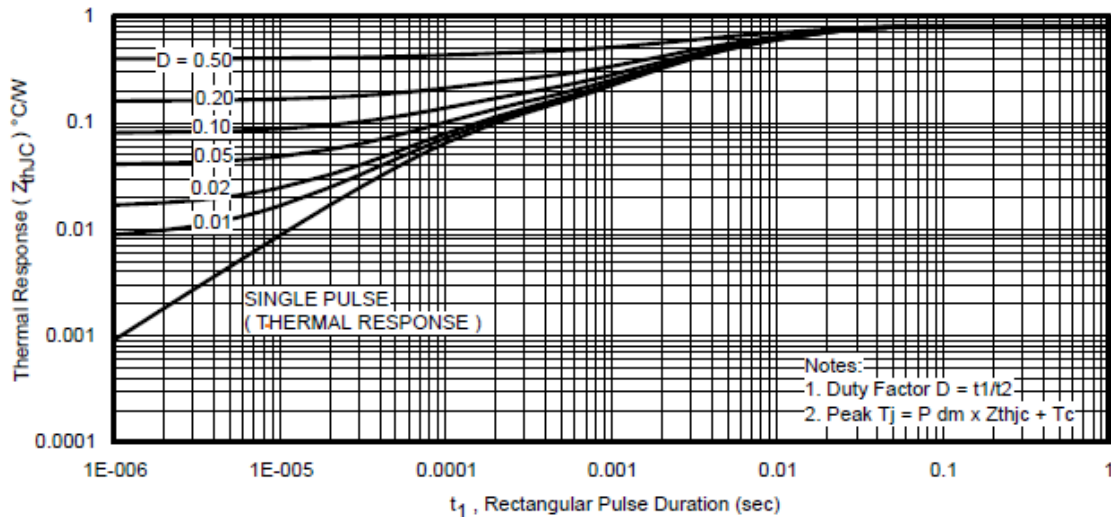
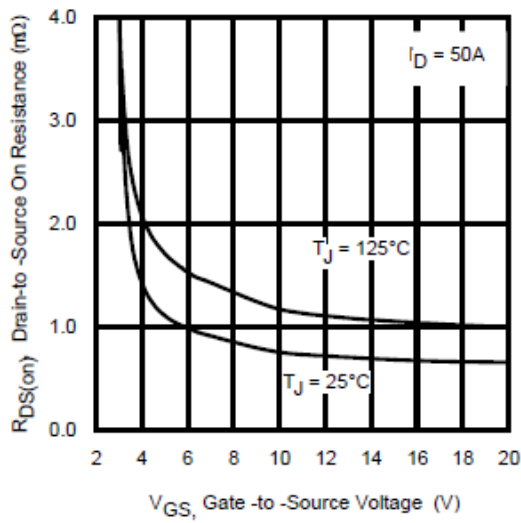
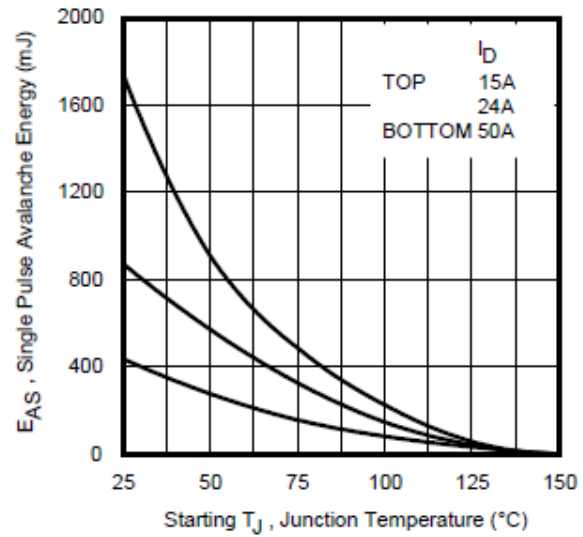
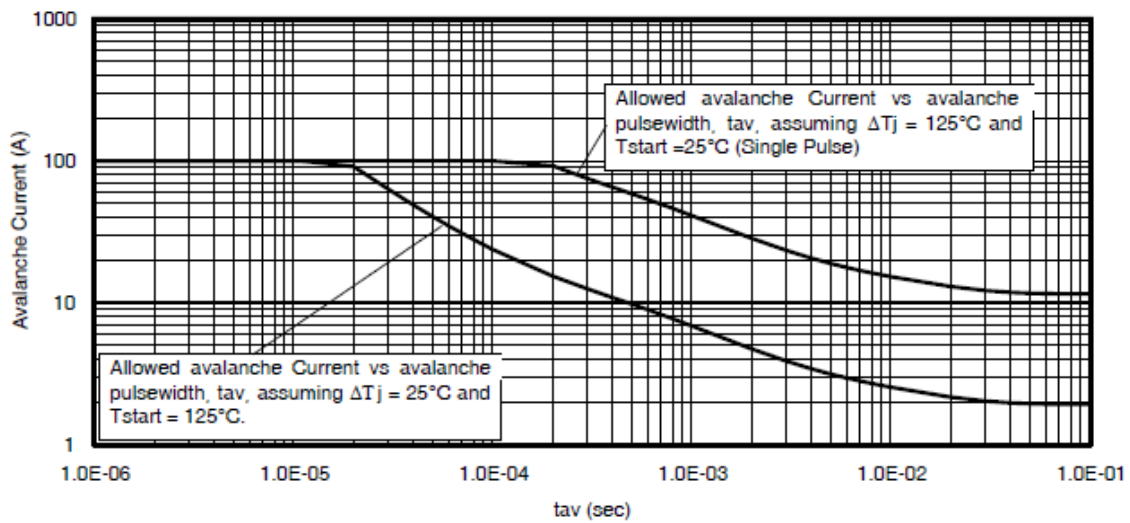


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage Vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width

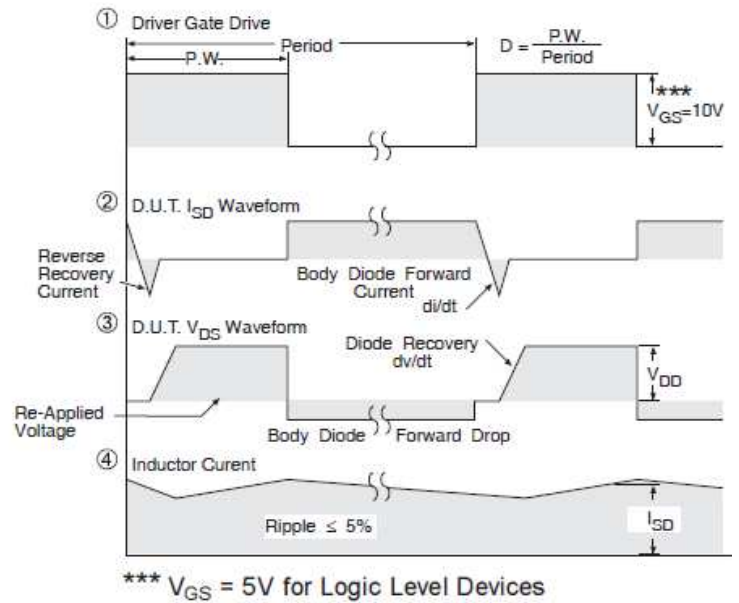
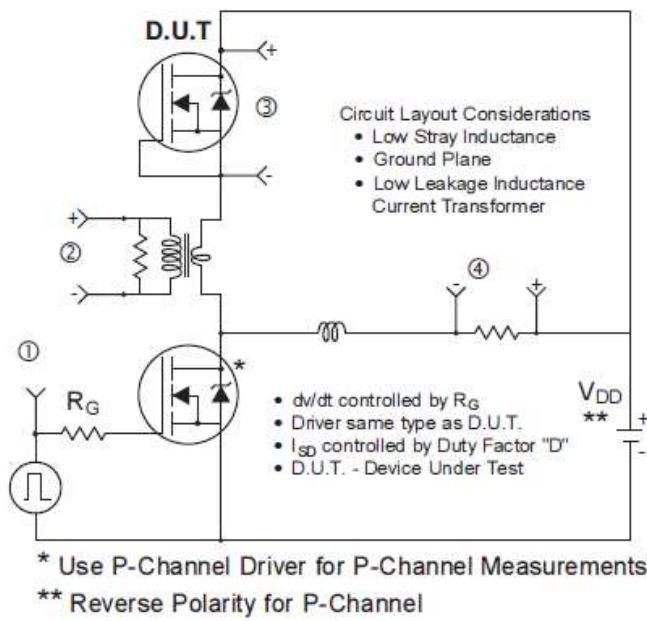


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

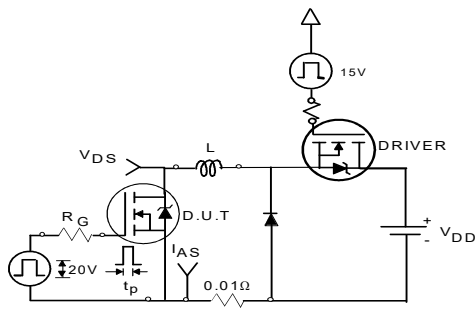


Fig 16a. Unclamped Inductive Test Circuit

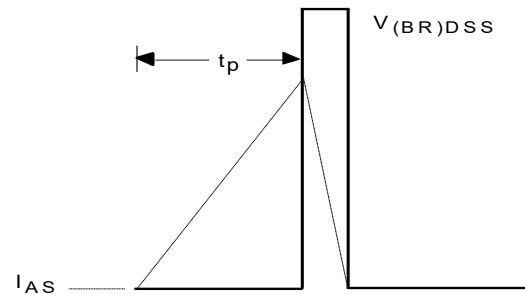


Fig 16b. Unclamped Inductive Waveforms

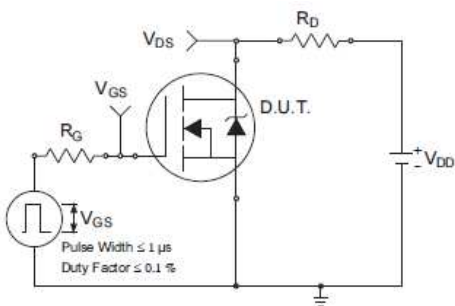


Fig 17a. Switching Time Test Circuit

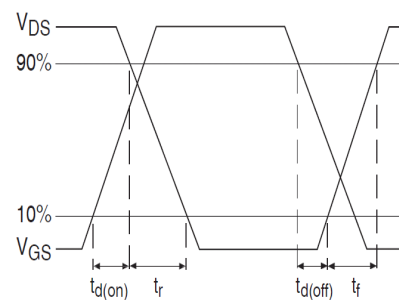


Fig 17b. Switching Time Waveforms

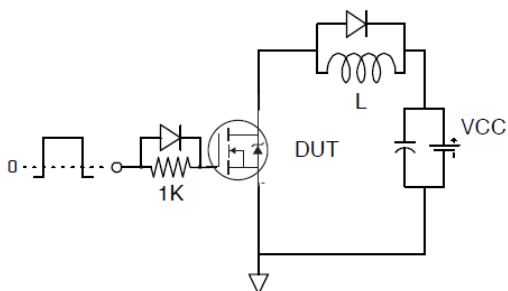


Fig 18a. Gate Charge Test Circuit

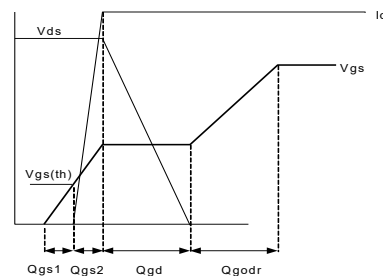
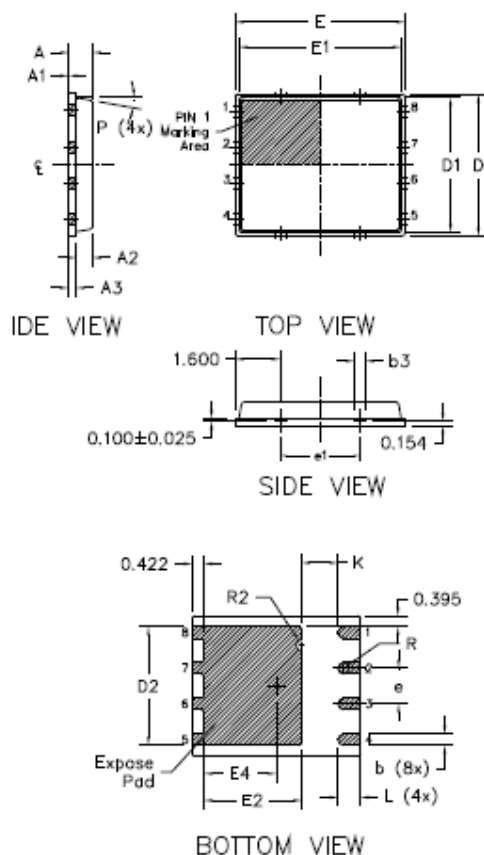


Fig 18b. Gate Charge Waveform

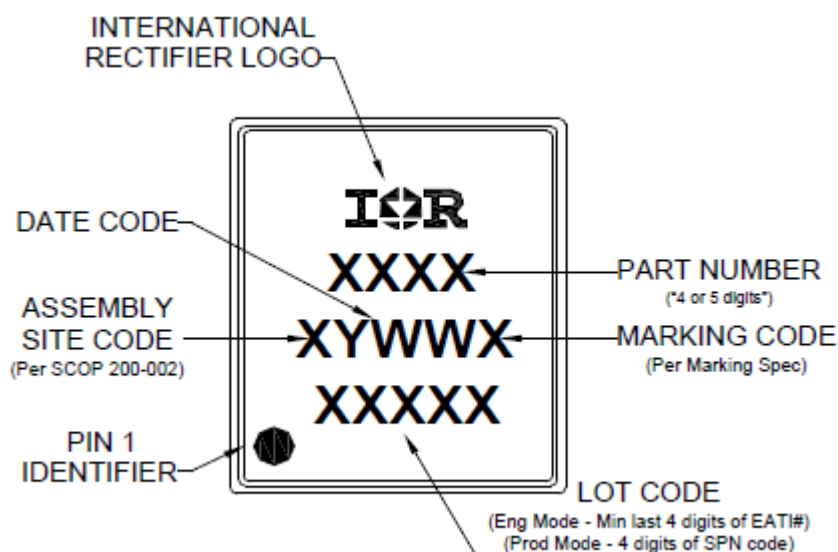
PQFN 5x6 Outline "B" Package Details


DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200	REF	0.0079	REF
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000	BSC	0.1969	BSC
D1	4.750	BSC	0.1870	BSC
D2	4.100	4.300	0.1614	0.1693
E	6.000	BSC	0.2362	BSC
E1	5.750	BSC	0.2264	BSC
E2	3.380	3.780	0.1331	0.1488
e	1.270	REF	0.0500	REF
e1	2.800	REF	0.1102	REF
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200	REF	0.0079	REF
R2	0.150	0.200	0.0059	0.0079

Note:

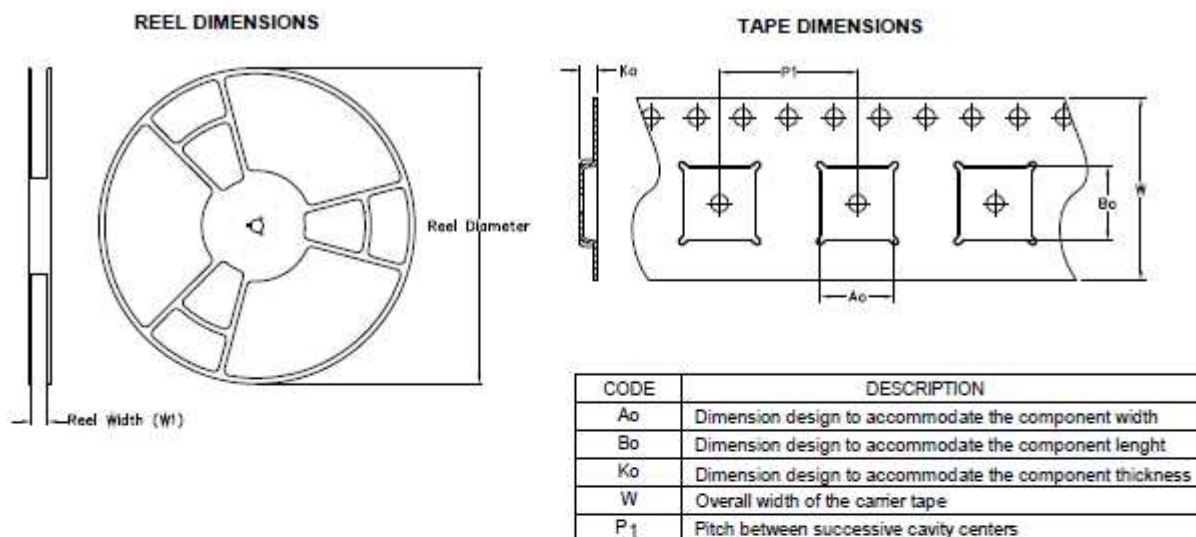
1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

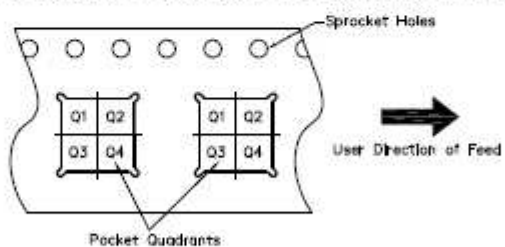
PQFN 5x6 Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/packaging>

PQFN 5x6 Tape and Reel



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at <http://www.irf.com/packaging>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F [†] guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D [†])
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Starting $T_J = 25^{\circ}\text{C}$, $L = 0.35\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ② Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ③ R_{θ} is measured at T_J of approximately 90°C .
- ④ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑤ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C . For higher case temperature please refer to Diagram 9. De-rating will be required based on the actual environmental conditions.

Revision History

Date	Rev.	Comments
10/23/2013	2.1	<ul style="list-style-type: none"> Added R_{dson} @ 4.5V-page1, 2
7/30/2014	2.2	<ul style="list-style-type: none"> Updated IDM from "400A" to "700A" on page1, 2. Updated Fig1, Fig2, Fig3, Fig7 & Fig8 on page 3, 4.
3/11/2015	2.3	<ul style="list-style-type: none"> Updated package outline and tape and reel on pages 7 and 8.
12/14/2020	2.4	<ul style="list-style-type: none"> Updated datasheet based on IFX template. Updated Datasheet based on new current rating and application note : App-AN_1912_PL51_2001_180356 Removed "HEXFET[®] Power MOSFET" -page1

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