

Automotive MOSFET

OptiMOS™ 5 Power-Transistor



Features

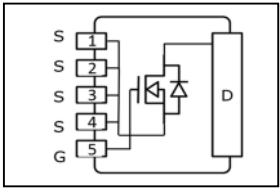
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	0.94	mΩ
I_D (chip limited)	200	A

Type	Package	Marking
IAUA200N04S5N010	PG-HSOF-5-1	5N04N010



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Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C = 25\text{ °C}, V_{GS} = 10\text{ V}^{1)}$	200	A
		$T_C = 100\text{ °C}, V_{GS} = 10\text{ V}^{2)}$	200	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C = 25\text{ °C}$	800	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D = 100\text{ A}$	280	mJ
Avalanche current, single pulse	I_{AS}	–	200	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C = 25\text{ °C}$	167	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	—	—	—	0.90	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ³⁾	—	—	60	

Electrical characteristics

at $T_j = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	40	—	—	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	2.2	2.8	3.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25\text{ °C}$	—	—	1	μA
		$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 125\text{ °C}^{2)}$	—	—	100	
Gate-source leakage current	I_{GSS}	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 7\text{ V}$, $I_D = 100\text{ A}$	—	0.90	1.20	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 100\text{ A}$	—	0.80	0.94	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V},$ $f = 1\text{ MHz}$	–	5750	7650	pF
Output capacitance	C_{oss}		–	1600	2130	
Reverse transfer capacitance	C_{rss}		–	80	120	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 200\text{ A}, R_G = 3.5\ \Omega$	–	11	–	ns
Rise time	t_r		–	6	–	
Turn-off delay time	$t_{d(off)}$		–	23	–	
Fall time	t_f		–	12	–	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD} = 32\text{ V}, I_D = 200\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$	–	28	37	nC
Gate to drain charge	Q_{gd}		–	21	32	
Gate charge total	Q_g		–	99	132	
Gate plateau voltage	$V_{plateau}$		–	4.7	–	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C = 25\text{ °C}$	–	–	200	A
Diode pulse current ²⁾	$I_{S,pulse}$		–	–	800	
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = 100\text{ A},$ $T_j = 25\text{ °C}$	–	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R = 20\text{ V}, I_F = 50\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	–	65	–	ns
Reverse recovery charge ²⁾	Q_{rr}		–	80	–	nC

¹⁾ Current is limited by package; with a $R_{thjc} = 0.9\text{ K/W}$ the chip is able to carry 300 A at 25°C.

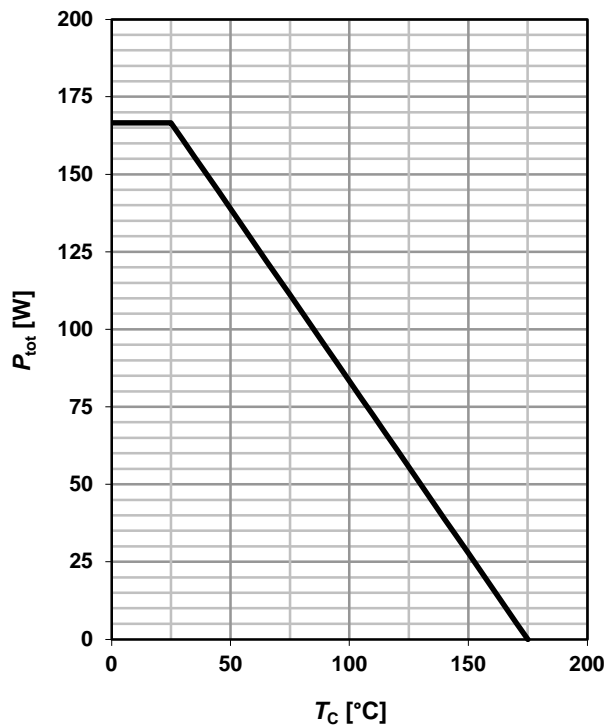
²⁾ The parameter is not subject to production test- verified by design/characterization.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Electrical characteristics diagrams

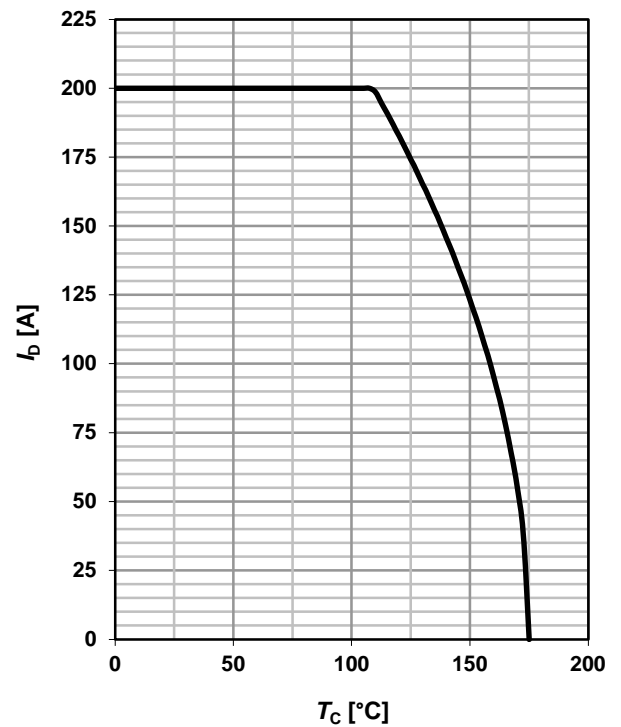
1 Power dissipation

$$P_{\text{tot}} = f(T_c); V_{\text{GS}} \geq 10 \text{ V}$$



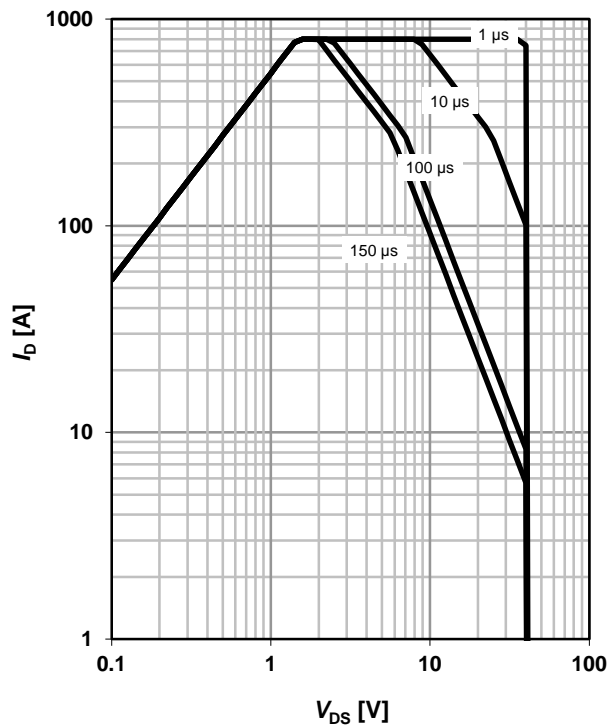
2 Drain current

$$I_D = f(T_c); V_{\text{GS}} \geq 10 \text{ V}$$



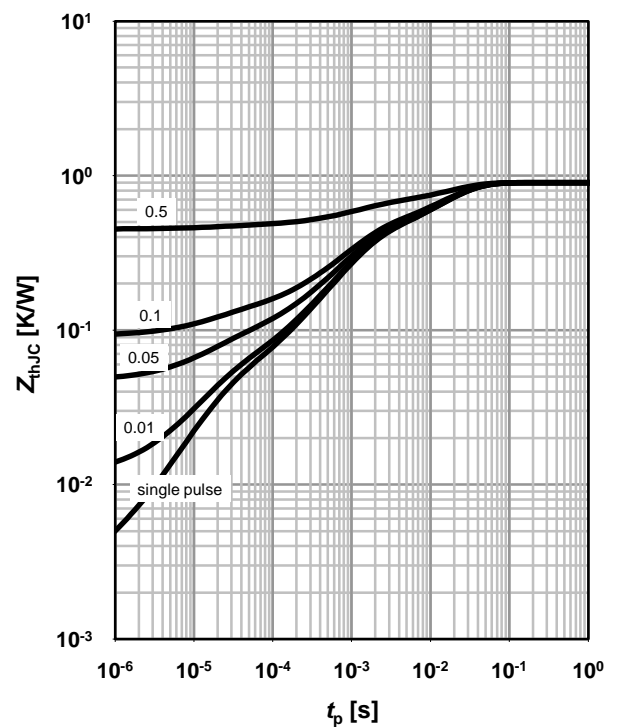
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_c = 25^{\circ}\text{C}; D = 0; \text{parameter: } t_p$$

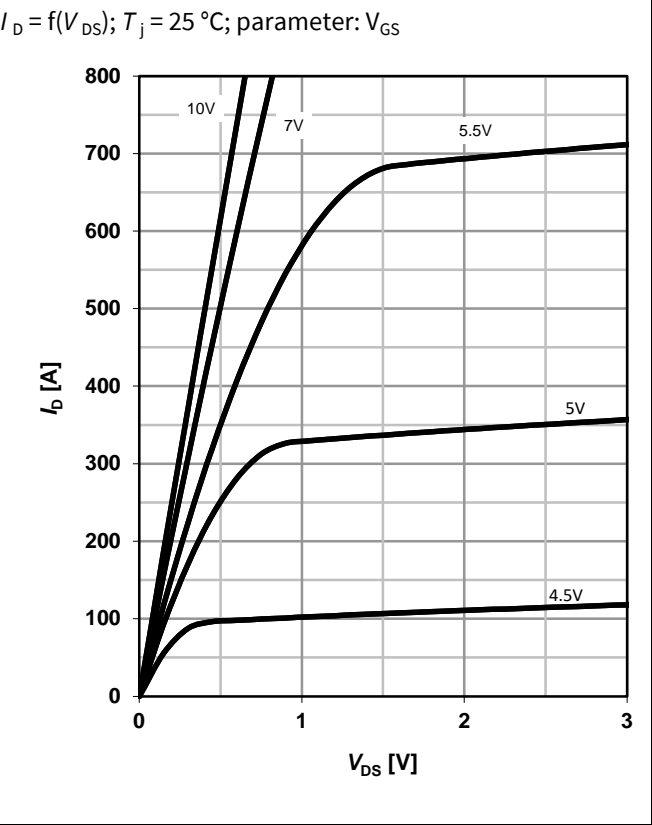


4 Max. transient thermal impedance

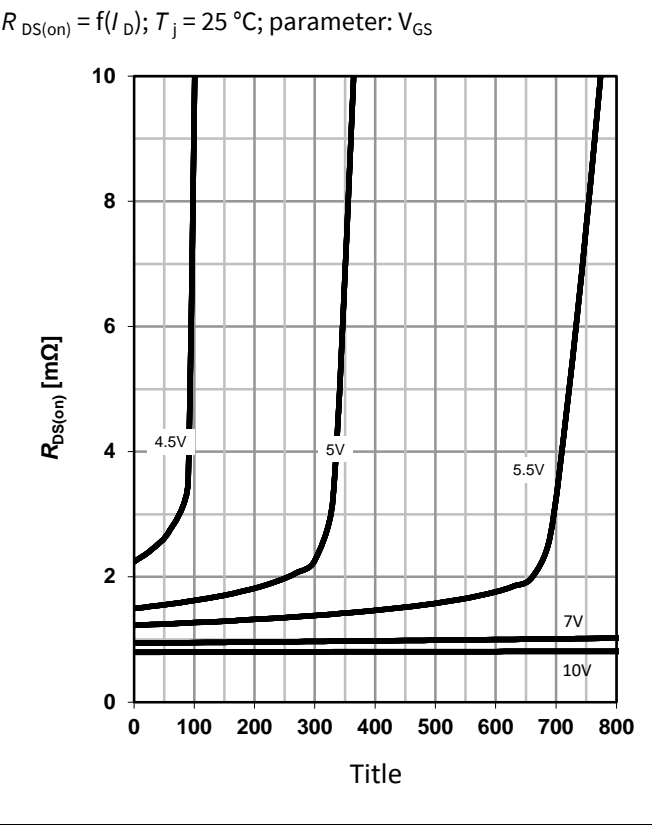
$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



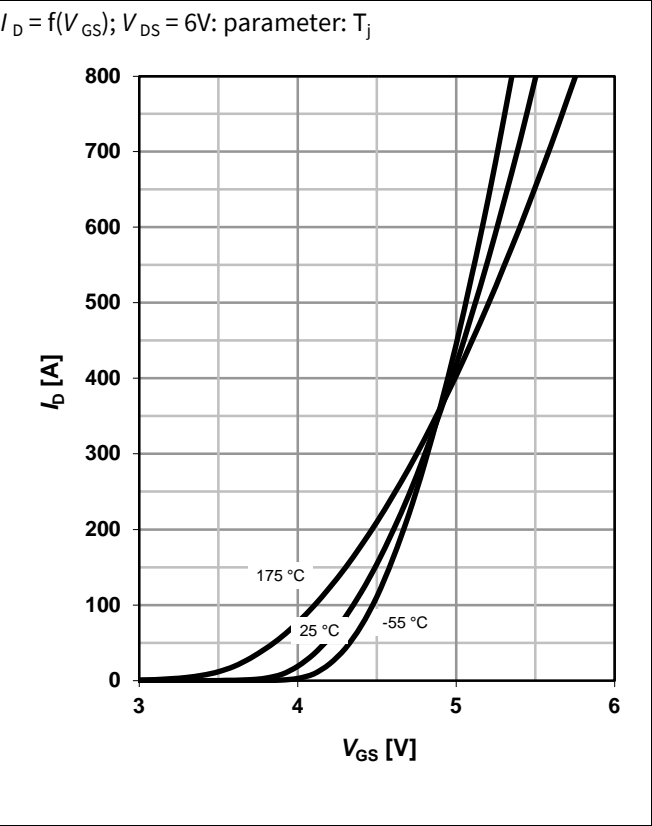
5 Typ. output characteristics



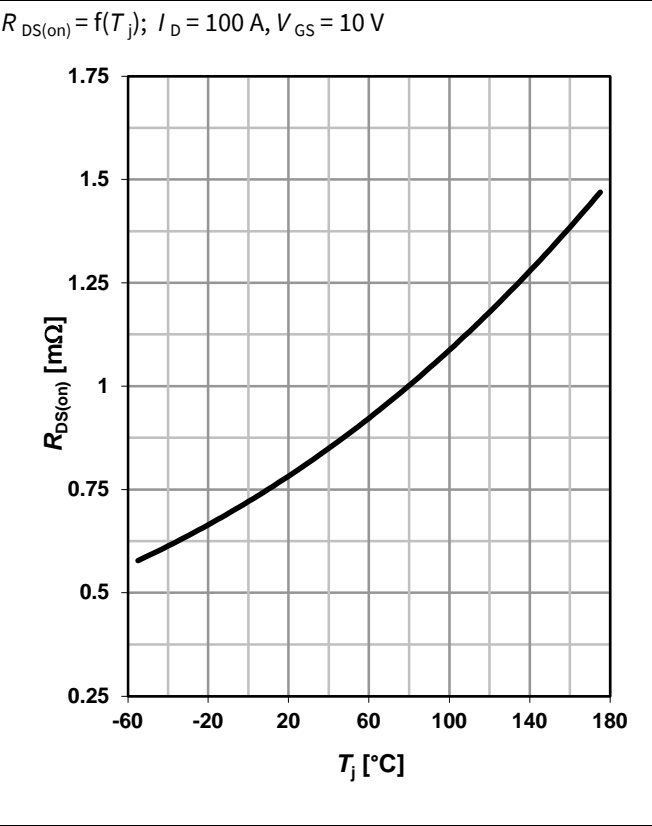
6 Typ. drain-source on-state resistance



7 Typ. transfer characteristics

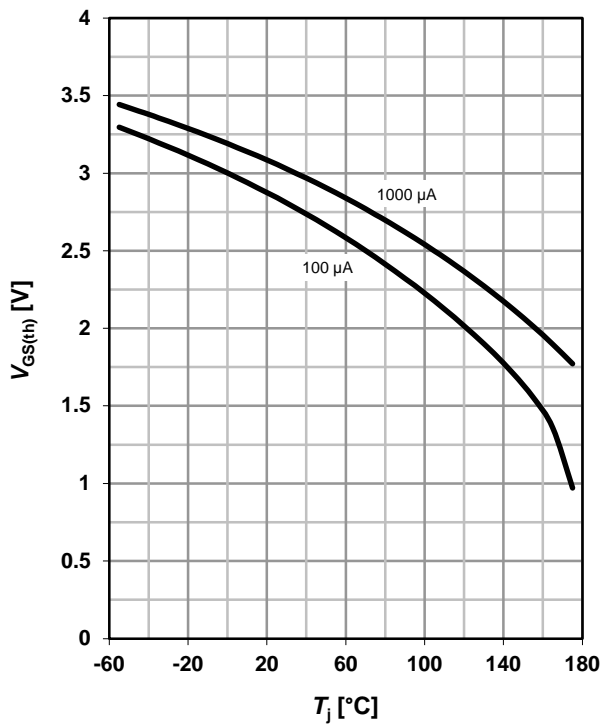


8 Typ. drain-source on-state resistance



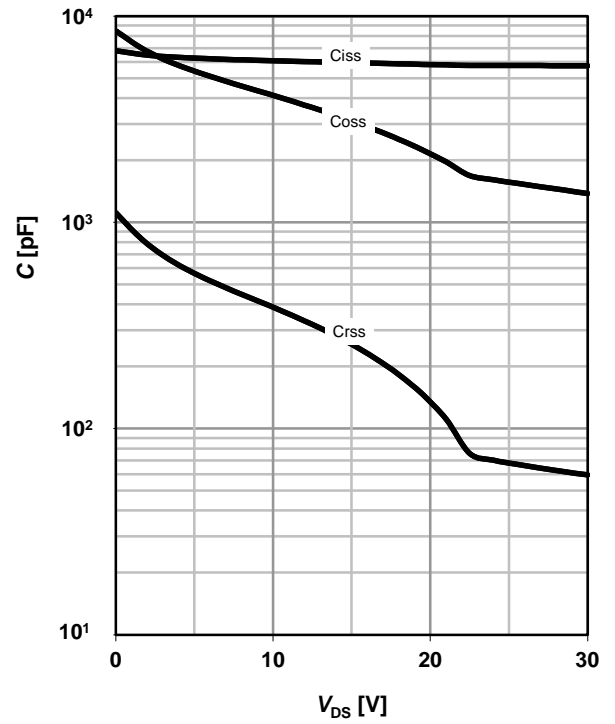
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



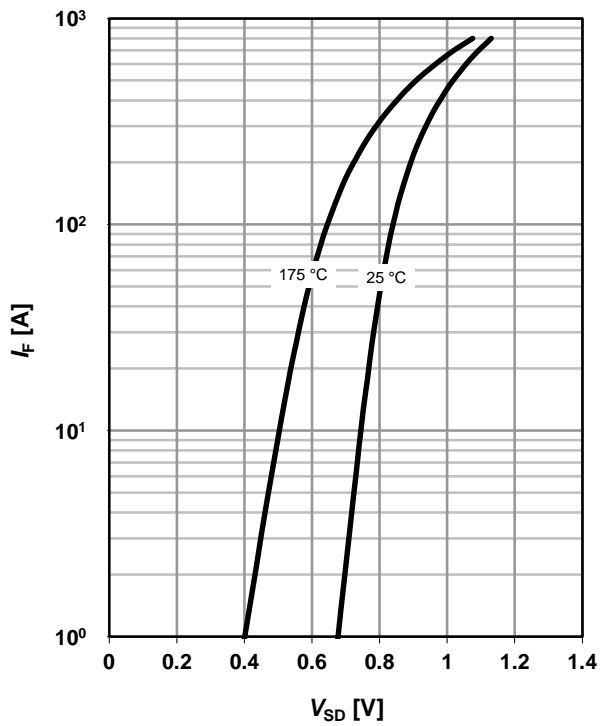
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0 V$; $f = 1 MHz$



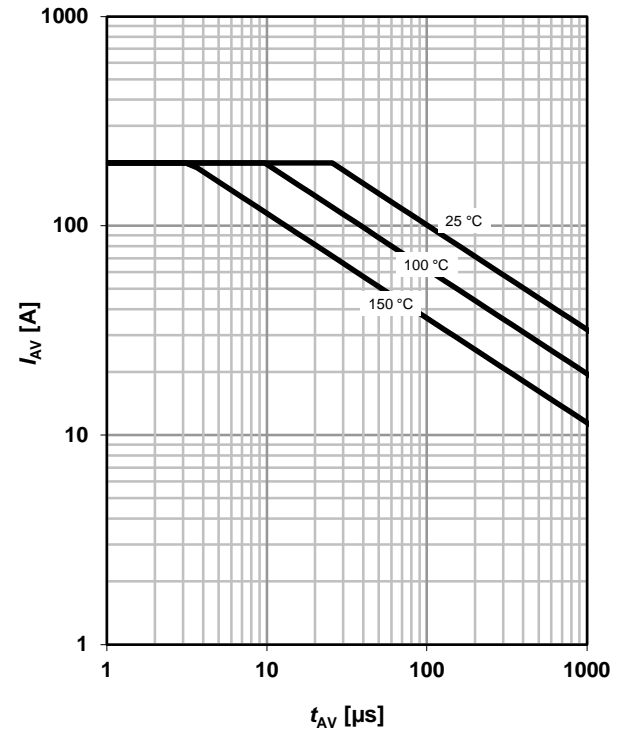
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



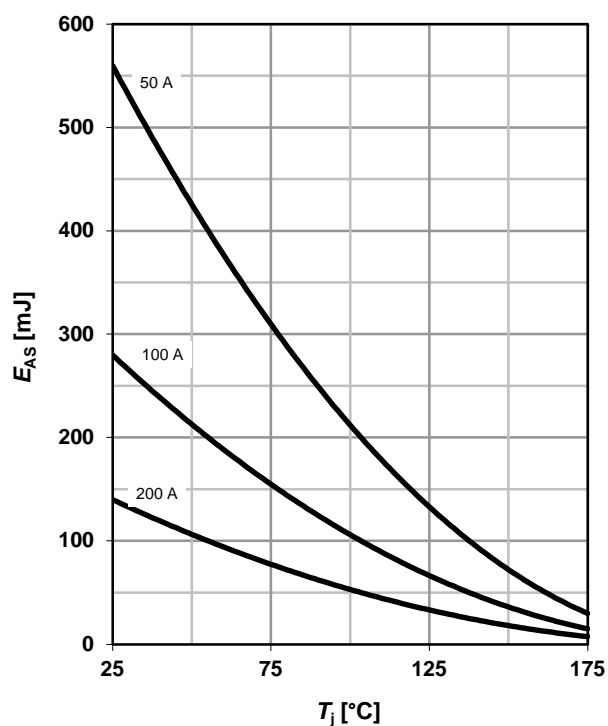
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



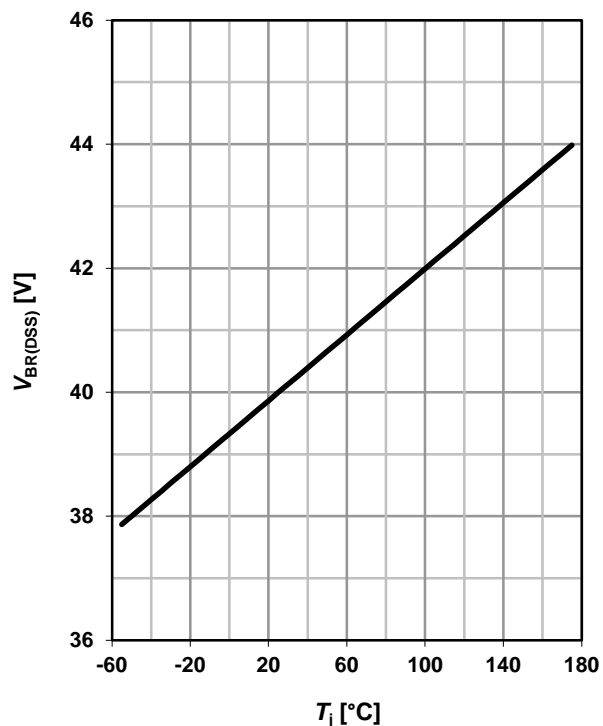
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



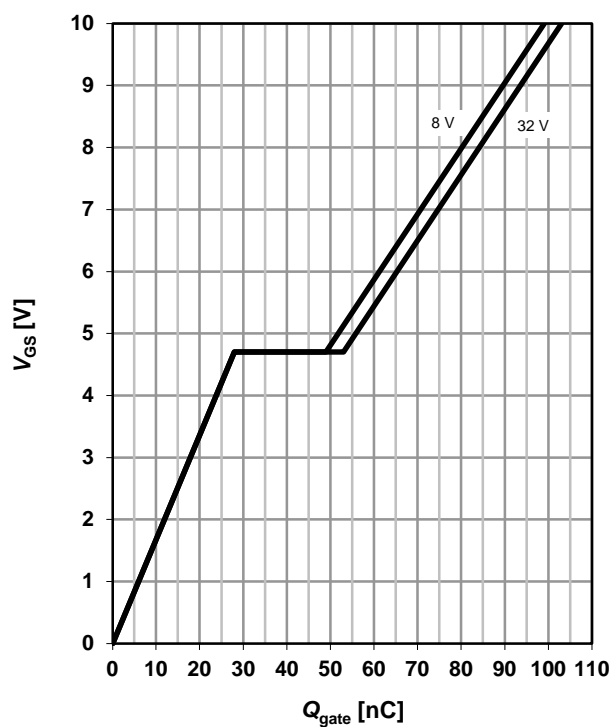
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_{D_typ} = 1$ mA

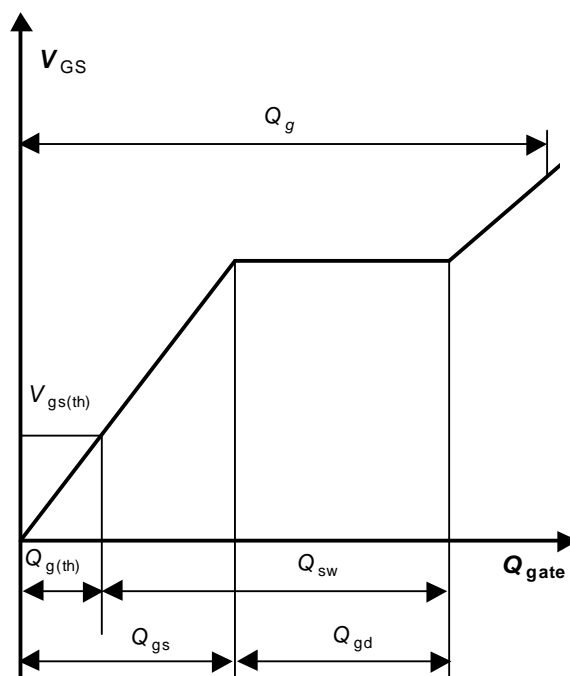


15 Typ. gate charge

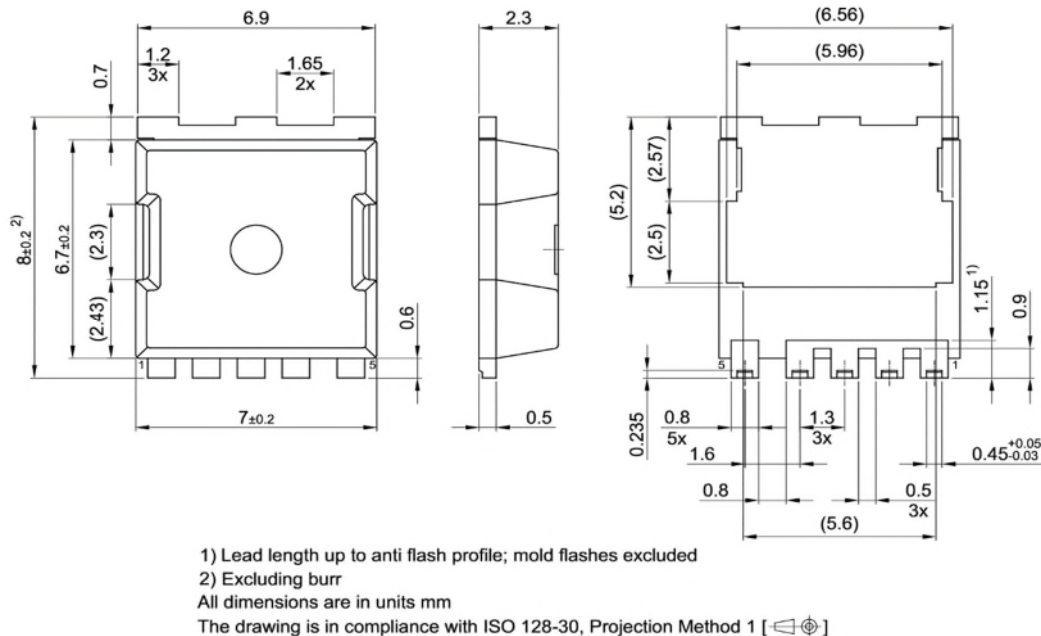
$V_{GS} = f(Q_{gate})$; $I_D = 200$ A pulsed; parameter: V_{DD}



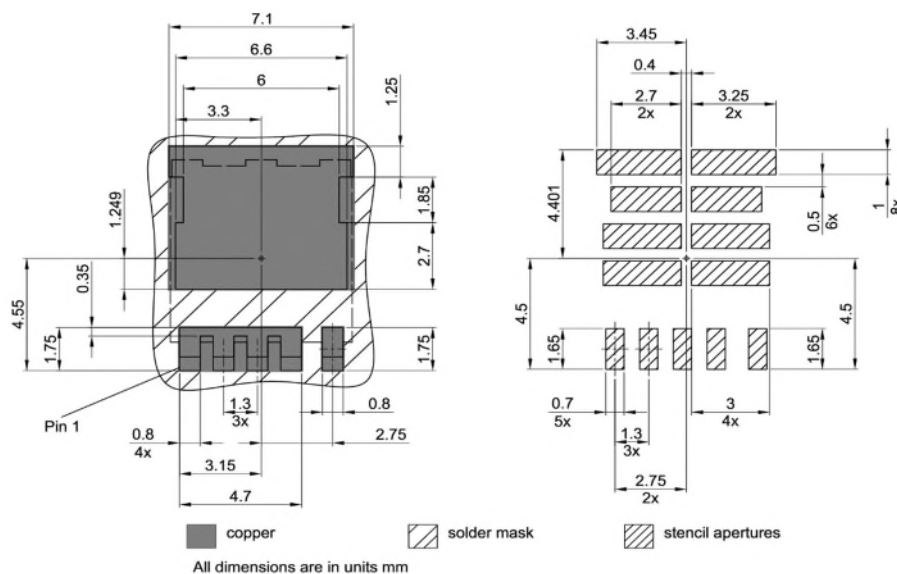
16 Gate charge waveforms



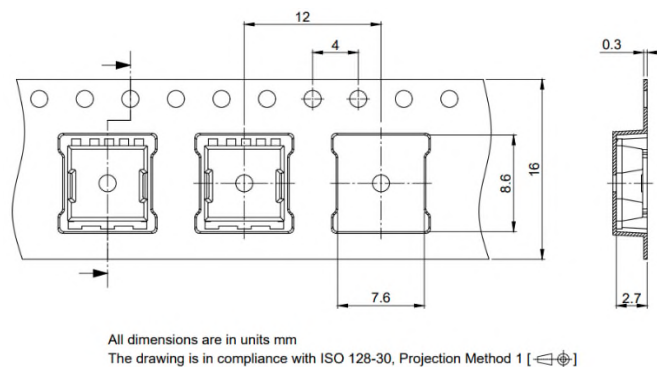
Package Outline



Footprint



Packaging



Revision History

Revision	Date	Changes
Revision 1.0	07.12.2017	Final Data Sheet
Revision 1.1	10.07.2018	Package name, SOA curve 10 μ s
Revision 1.2	14.04.2021	RDS(on) improved
Revision 1.3	24.01.2022	Editorial changes, package drawing added
Revision 1.4	11.09.2023	Corrected avalanche current Graph

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