

$\frac{\text{MOSFET}}{\text{UniFET}}$ – N-Channel, UniFET $^{\text{M}}$ 60 V, 55 A, 22 mΩ

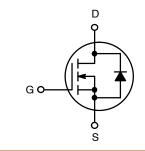
FDP55N06 / FDPF55N06

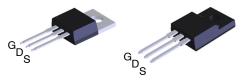
Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on–state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 22 \text{ m}\Omega \text{ (Typ.)} @ V_{GS} = 10 \text{ V}, I_D = 27.5 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{rss} (Typ. 60 pF)
- 100% Avalanche Tested

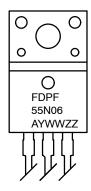




TO-220-3LD CASE 340AT

TO-220 Fullpack, 3-Lead / TO-220F-3SG CASE 221AT

MARKING DIAGRAM



FDP55N06,

FDPF55N06 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDP55N06	TO-220	1000 Units / Tube
FDPF55N06	TO-220F	1000 Units / Tube

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C unless otherwise noted)

Symbol	Paramet	er	FDP55N06	FDPF55N06	Unit
V _{DSS}	Drain to Source Voltage		60	60	V
Ι _D	Drain Current –	Continuous (T_C = 25°C)Continuous (T_C = 100°C)	55 34.8	55* 34.8*	Α
I _{DM}	Drain Current	- Pulsed (Note 1)	220	220*	Α
V_{GSS}	Gate-Source Voltage		±25	±25	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	480	480	mJ
I _{AR}	Avalanche Current (Note 1)		55	55	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		11.4	11.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	4.5	V/ns
P _D	Power Dissipation	(T _C = 25°C) – Derate Above 25°C	114 0.9	48 0.4	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	-55 to +150	°C
TL	Maximum Lead Temperature for Solderin	g, 1/8" from Case for 5 Second	300	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- *Drain current limited by maximum junction temperature 1. Repetitive Rating: Pulse width limited by maximum junction temperature. 2. L = 5.6 mH, I_{AS} = 55 A, V_{DD} = 50 V, R_{G} = 25 Ω , Starting T_{J} = 25°C 3. $I_{SD} \le$ 55 A, I_{J} = 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP55N06	FDPF55N06	Unit
Rejc	Thermal Resistance, Junction-to-Case, Max.	1.1	2.58	°C/W
R⊕JS	Thermal Resistance, Junction-to-sink, Typ.	0.5	-	°C/W
RеJA	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
OFF CHARACT	OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60	_	_	V		
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.05	-	V/°C		
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 60 V, V _{GS} = 0 V	-	_	1	μΑ		
		V _{DS} = 48 V, T _C = 150°C	-	-	10			
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	_	100	nA		
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	-	_	-100	nA		
ON CHARACTI	ON CHARACTERISTICS							
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.0	_	4.0	V		
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 27.5 A	-	0.018	0.022	Ω		
9FS	Forward Transconductance	V _{DS} = 25 V, I _D = 27.5 A	-	33	_	S		
DYNAMIC CHA	DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,	-	1160	1510	pF		
C _{oss}	Output Capacitance	f = 1 MHz	-	375	490	pF		
C _{rss}	Reverse Transfer Capacitance		-	60	90	pF		

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SWITCHING C	HARACTERISTICS		•		-	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 55 \text{ A},$	_	30	65	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$ (Note 4)	-	130	265	ns
t _{d(off)}	Turn-Off Delay Time]` ,	-	70	150	ns
t _f	Turn-Off Fall Time		_	95	195	ns
Q _{g(tot)}	Total Gate Charge at 10V	V _{DD} = 48 V, I _D = 55 A, V _{GS} = 10 V (Note 4)	_	30	37	nC
Q _{gs}	Gate-Source Gate Charge		_	6.5	_	nC
Q_{gd}	Gate-Drain Charge		_	7.5	_	nC
RAIN-SOUR	CE DIODE CHARACTERISTICS					
IS	Maximum Continuous Drain-Source Diode Forward Current		_	-	55	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		_	-	220	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 55 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 55 A	_	40	_	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	55	-	μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{4.} Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

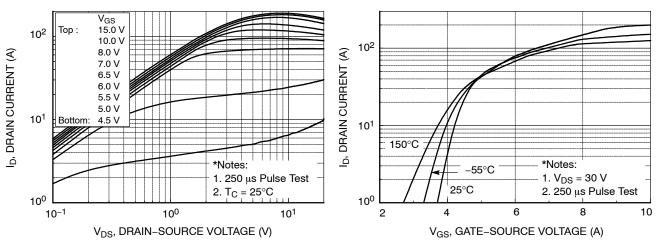


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

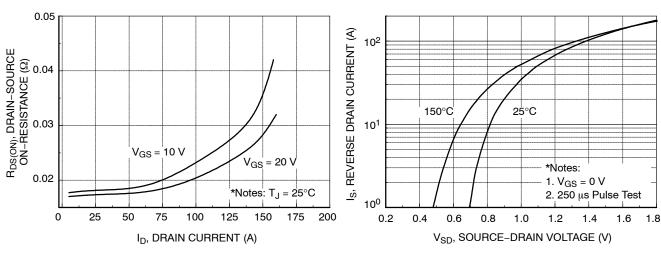


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

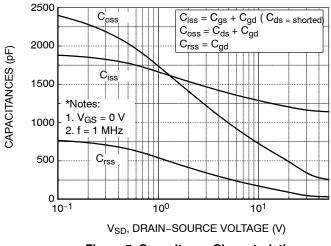


Figure 5. Capacitance Characteristics

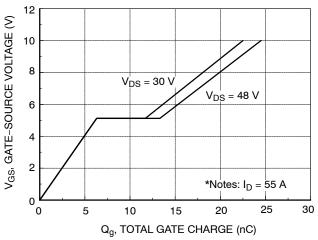


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

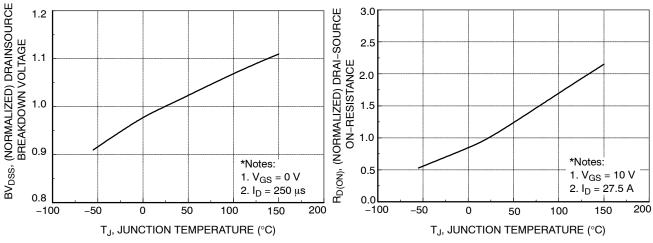


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On–Resistance Variation vs.
Temperature

100 μs

100

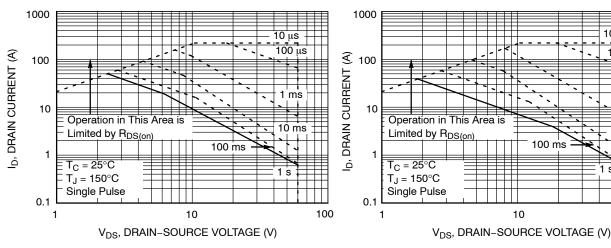


Figure 9-1. Maximum Safe Operating Area for FDP55N06

Figure 9–2. Maximum Safe Operating Area for FDPF55N06

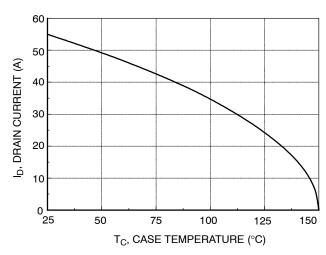


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

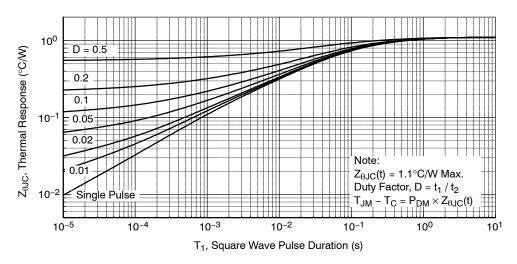


Figure 11-1. Transient Thermal Response Curve for FDP55N06

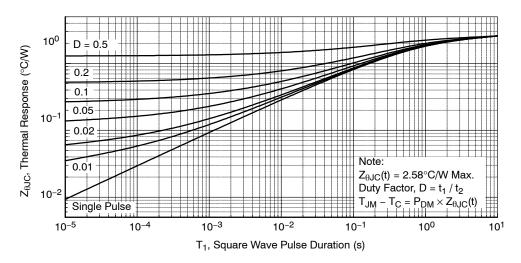


Figure 11-2. Transient Thermal Response Curve for FDPF55N06

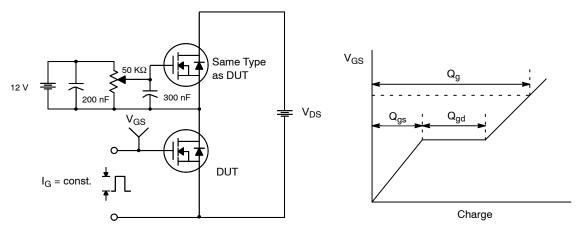


Figure 12. Gate Charge Test Circuit & Waveform

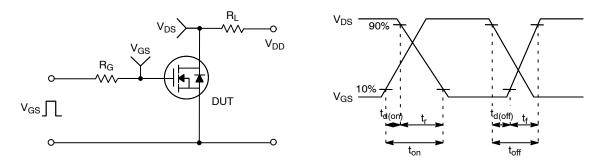


Figure 13. Resistive Switching Test Circuit & Waveforms

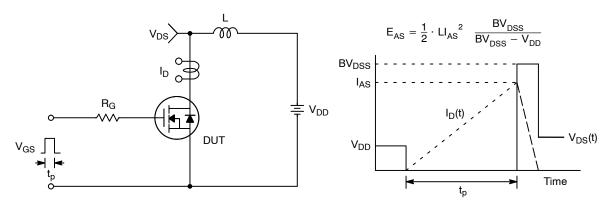


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

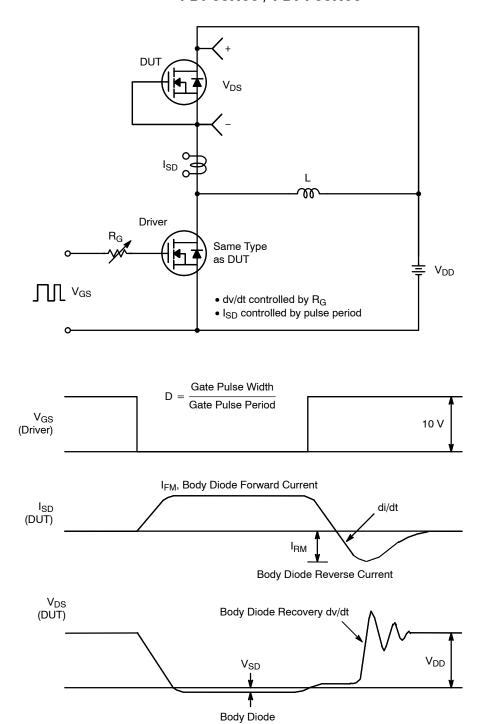
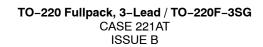


Figure 15. Peak Recovery dv/dt Test Circuit & Waveforms

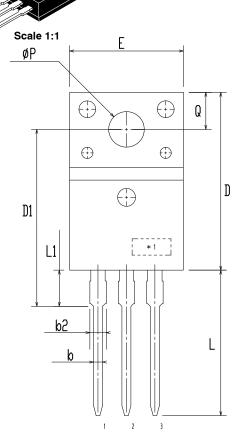
Forward Voltage Drop

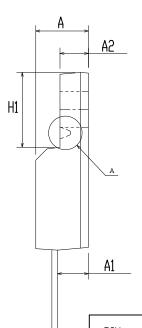
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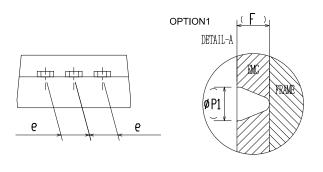




DATE 19 JAN 2021







DIM	LITE	LIUI I LNO			
ויונע	MIN	NDM	MAX		
Α	4.50	4.70	4.90		
A1	2.56	2.76	2.96		
A2	2.34	2.54	2.74		
b	0.70	0.80	0.90		
b2	~	2	1.47		
С	0.45	0.50	0.60		
D	15.67	15.87	16.07		
D1	15.60	15.80	16.00		
E	9.96	10.16	10.36		
е	2.34	2.54	2.74		
F	~	0.84	~		
H1	6.48	6.68	6.88		
L	12.78	12.98	13.18		
L1	3.03	3.23	3.43		
ØΡ	2.98	3.18	3.38		
ø P1	~	1.00	~		
Q	3.20	3.30	3.40		
20					

MILLIMITERS

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.

C

C. OPTION 1 - WITH SUPPORT PIN HOLE OPTION 2 - NO SUPPORT PIN HOLE

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TO-220-3LD CASE 340AT ISSUE B

DATE 08 AUG 2022



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