

Automotive MOSFET

OptiMOS™-5 Power-Transistor

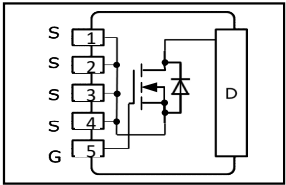
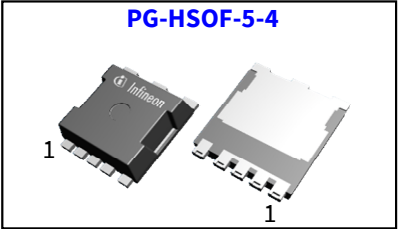


Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.



Product Summary

| | | |
|----------------------|-----|----|
| V_{DS} | 80 | V |
| $R_{DS(on)}$ | 1.8 | mΩ |
| I_D (Chip limited) | 250 | A |

| Type | Package | Marking |
|------------------|-------------|---------|
| IAUA250N08S5N018 | PG-HSOF-5-4 | 5N08018 |



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|---|--------------|------|
| Continuous drain current | I_D | $V_{GS}=10\text{ V}$, Chip limitation ¹⁾ | 250 | A |
| | | $V_{GS}=10\text{ V}$, DC current | 250 | |
| | | $T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)} | 35 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$ | 813 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D=125\text{ A}$ | 340 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 250 | A |
| Gate source voltage | V_{GS} | - | ± 20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 238 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

Thermal characteristics²⁾

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal resistance, junction - case | R_{thJC} | – | – | – | 0.63 | K/W |
| Thermal resistance, junction - ambient ³⁾ | R_{thJA} | – | – | 22.6 | – | |

Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|-----|-----|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ | 80 | – | – | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}$, $I_D=150\text{ }\mu\text{A}$ | 2.2 | 3 | 3.8 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ | – | 0.1 | 1 | μA |
| | | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$ | – | 1 | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ | – | – | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=6\text{ V}$, $I_D=60\text{ A}$ | – | 2.1 | 2.5 | m Ω |
| | | $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ | – | 1.5 | 1.8 | |
| Gate resistance ²⁾ | R_G | – | – | 1.4 | – | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|--|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$ | - | 6704 | 8715 | pF |
| Output capacitance | C_{oss} | | - | 1156 | 1502 | |
| Reverse transfer capacitance | C_{rss} | | - | 47 | 70 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\text{ }\Omega$ | - | 16 | - | ns |
| Rise time | t_r | | - | 11 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 32 | - | |
| Fall time | t_f | | - | 23 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=40\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$ | - | 32 | 41 | nC |
| Gate to drain charge | Q_{gd} | | - | 21 | 32 | |
| Gate charge total | Q_g | | - | 96 | 125 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 4.7 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|---|-----|-----|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 256 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | $T_C=25\text{ }^\circ\text{C}, t_p=100\text{ }\mu\text{s}$ | - | - | 813 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_J=25\text{ }^\circ\text{C}$ | - | 0.9 | 1.2 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=40\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$ | - | 60 | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 84 | - | nC |

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

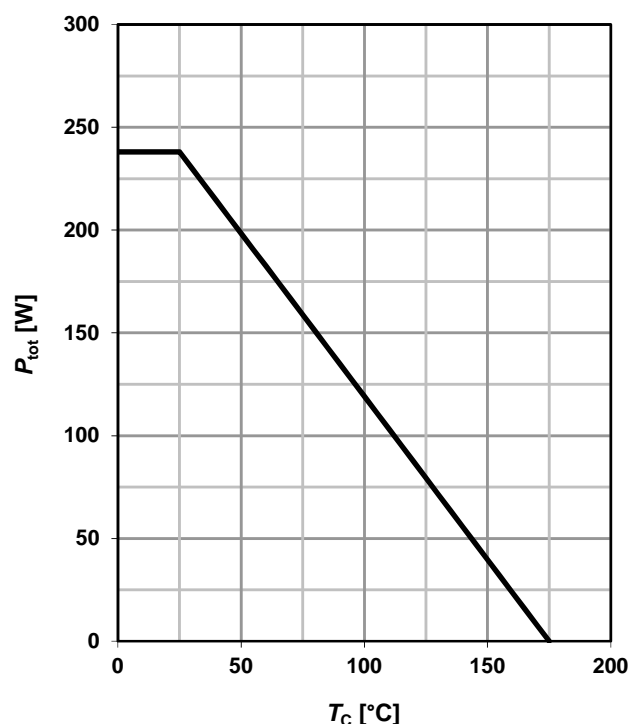
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

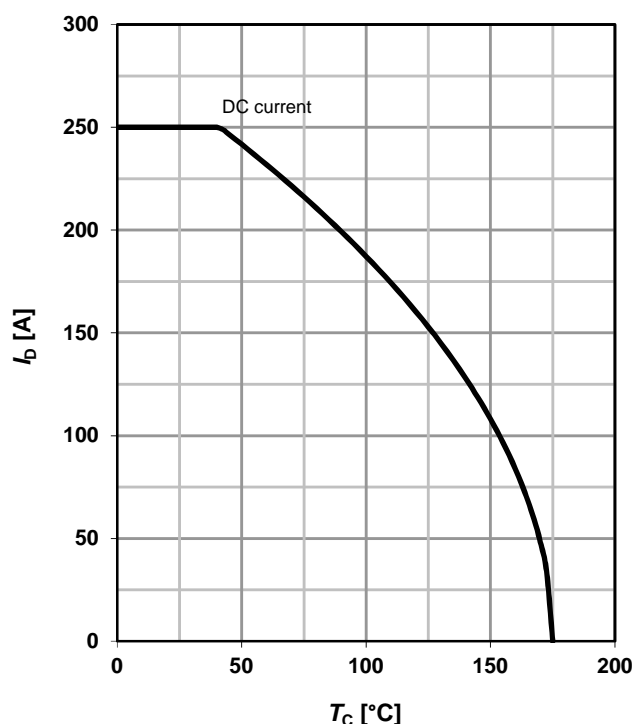
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



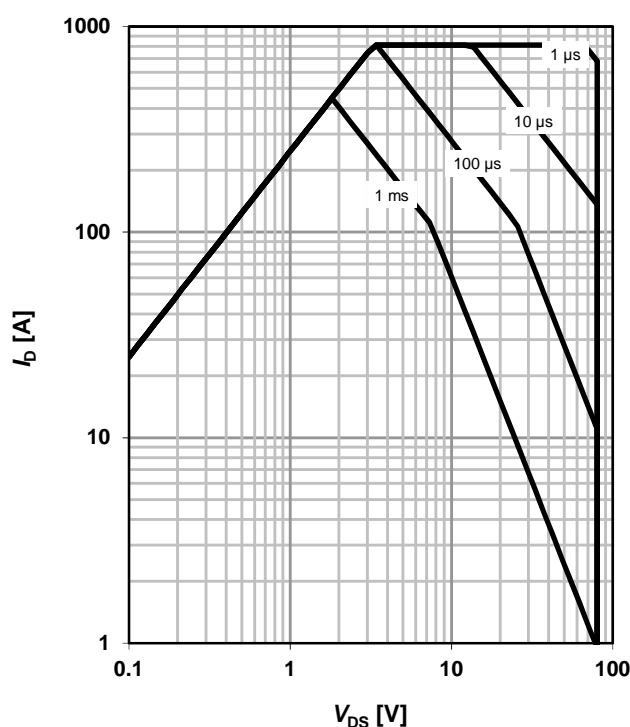
2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



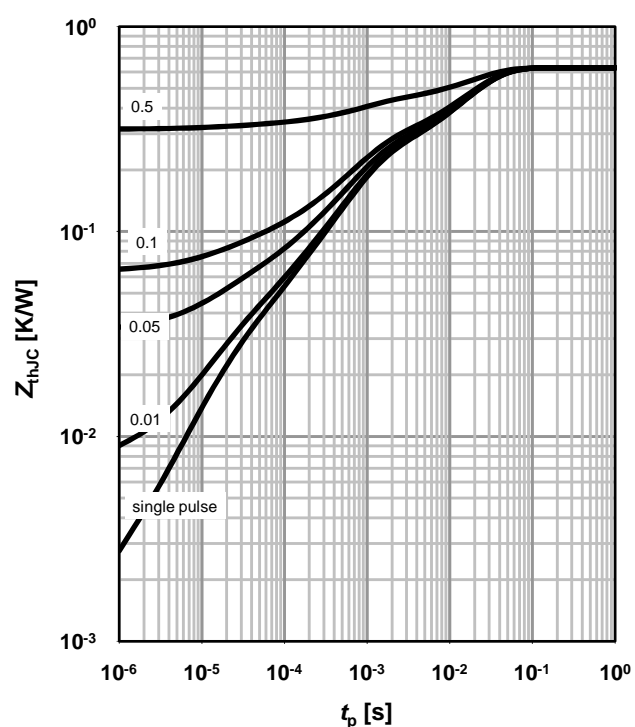
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$



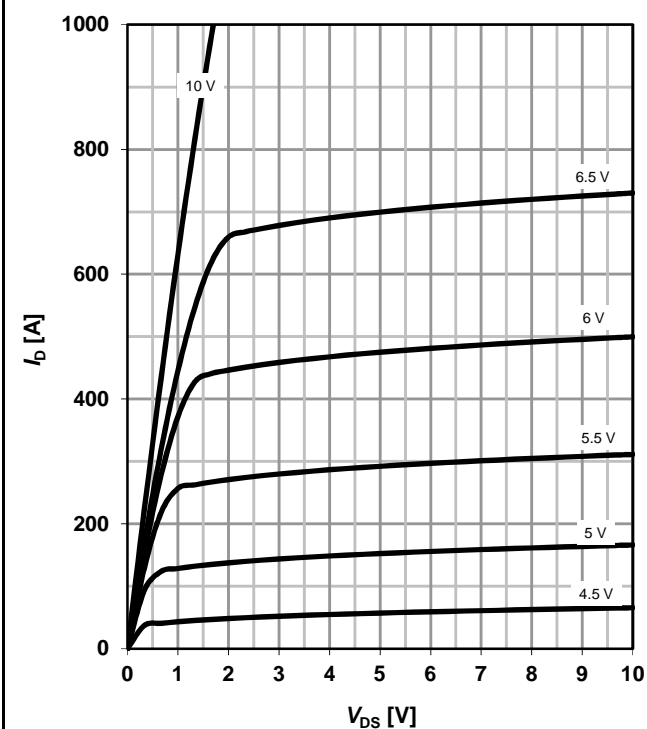
4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



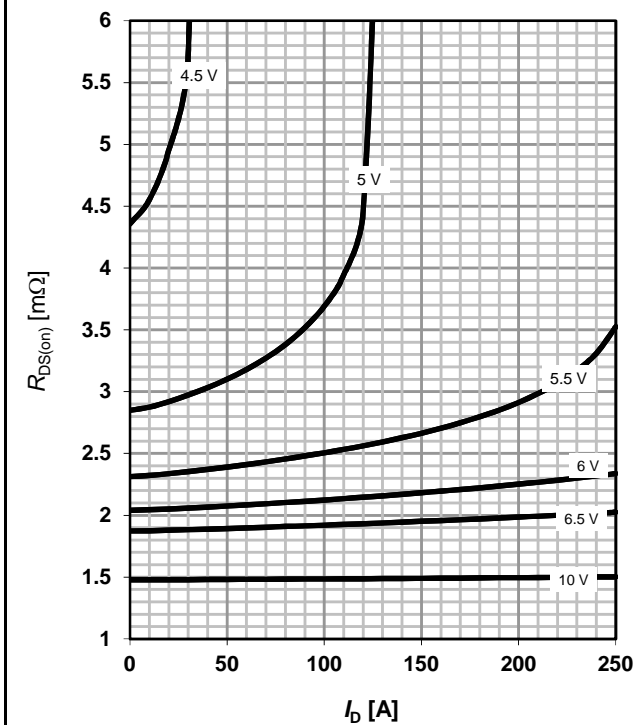
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



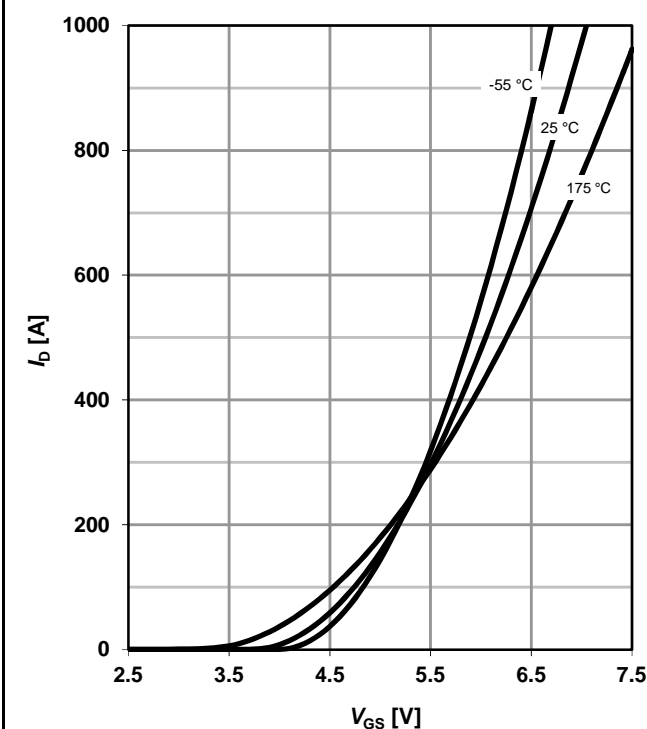
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



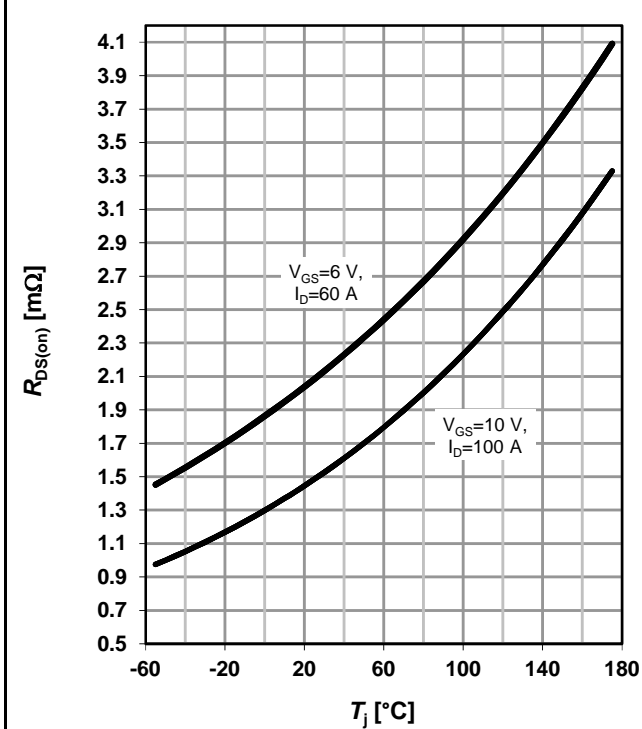
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{V}; \text{parameter: } T_j$



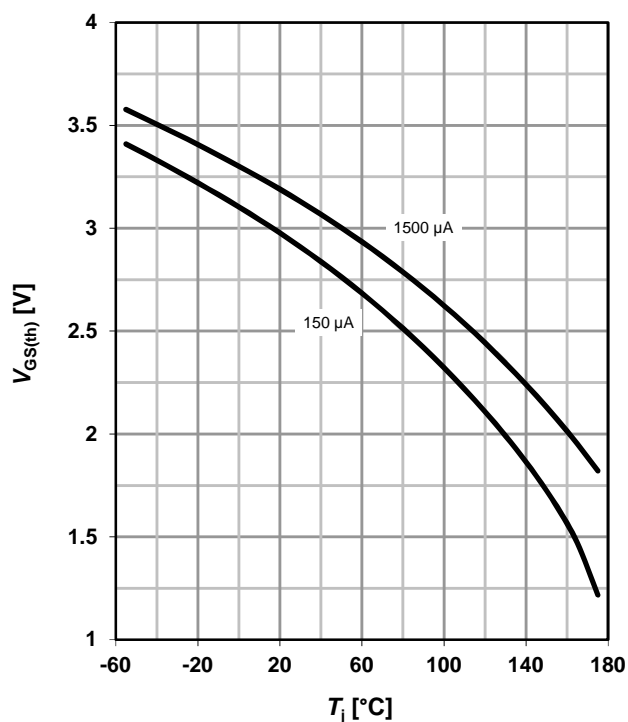
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



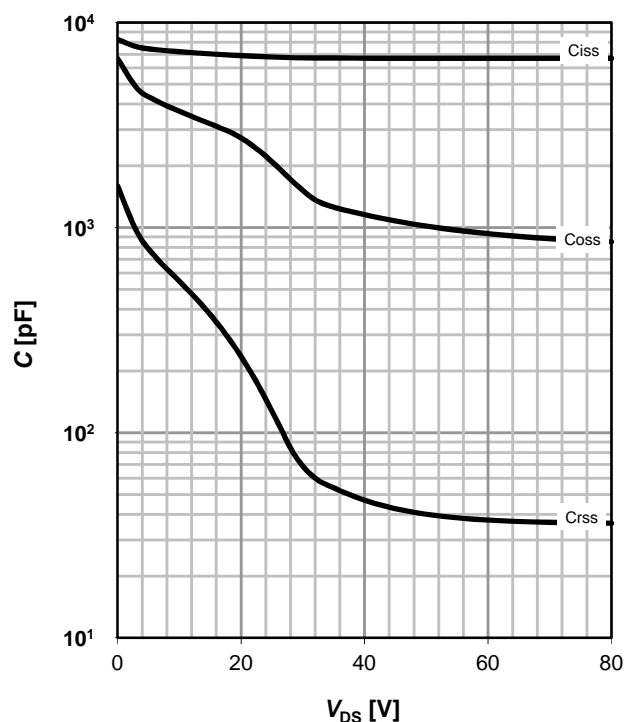
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



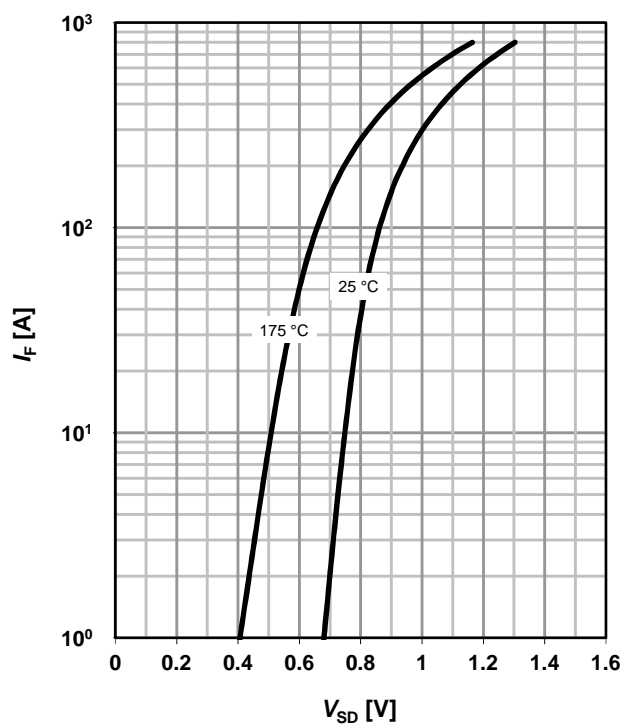
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0 V$; $f = 1 MHz$



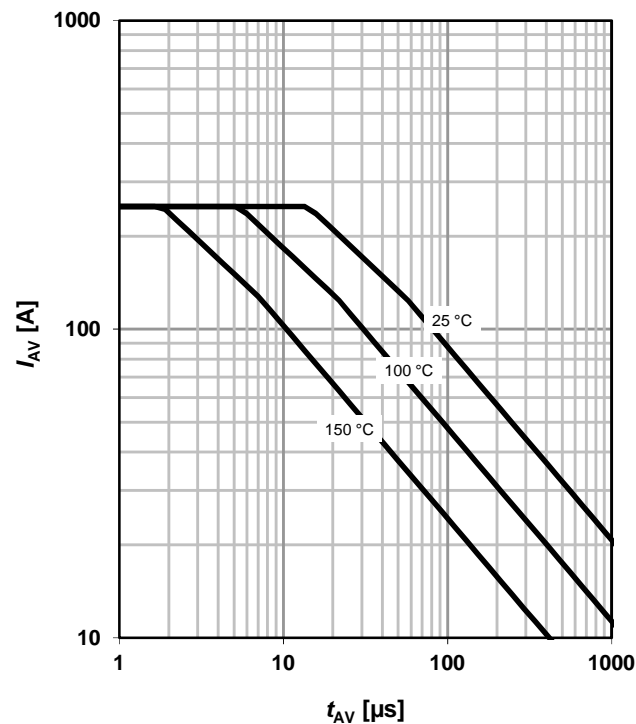
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



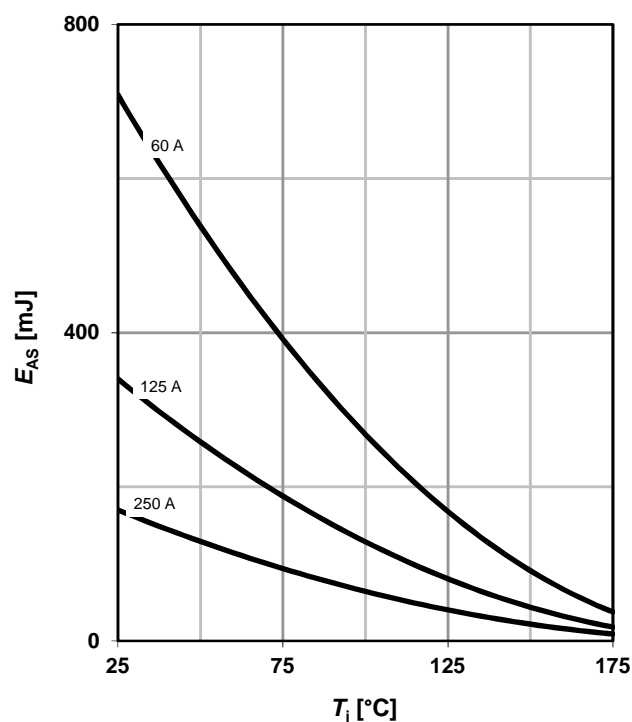
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



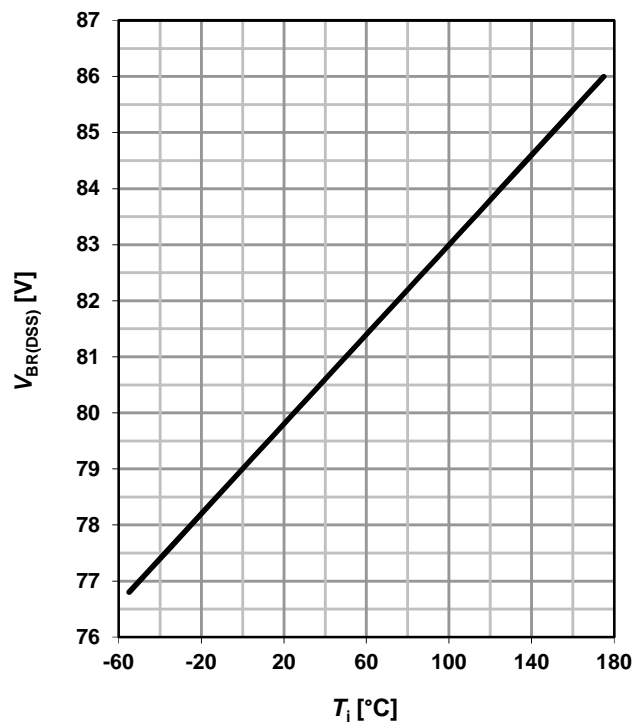
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



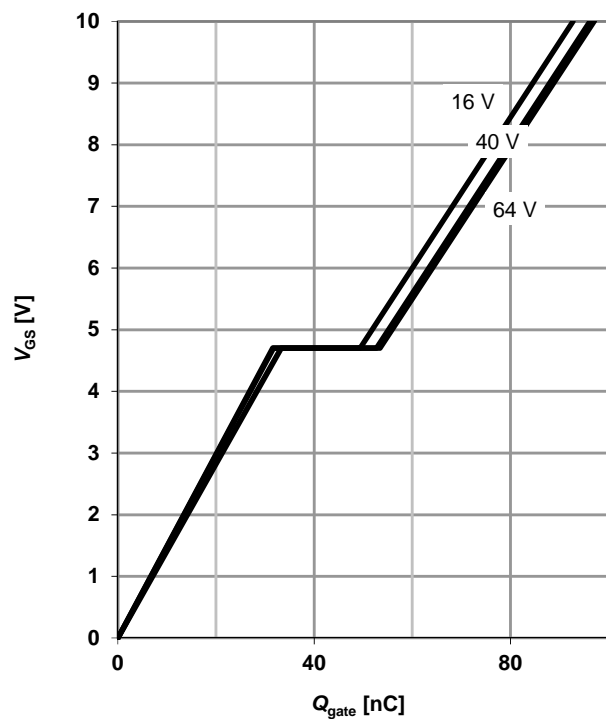
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_{D_typ} = 1$ mA

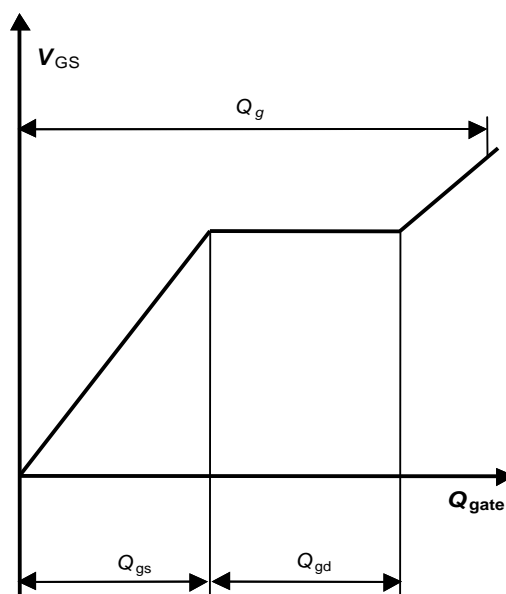


15 Typ. gate charge

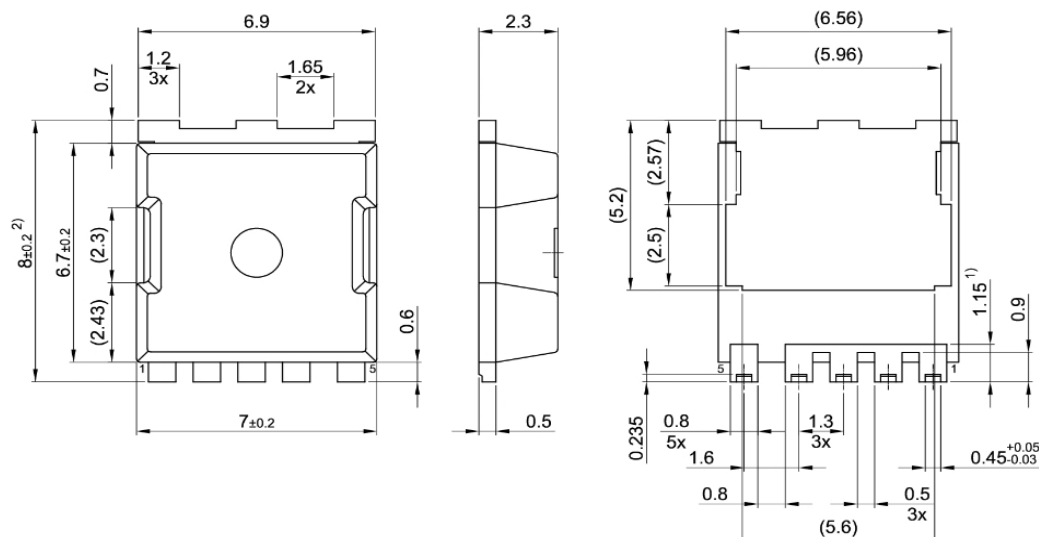
$V_{GS} = f(Q_{gate})$; $I_D = 100$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms



Package Outline



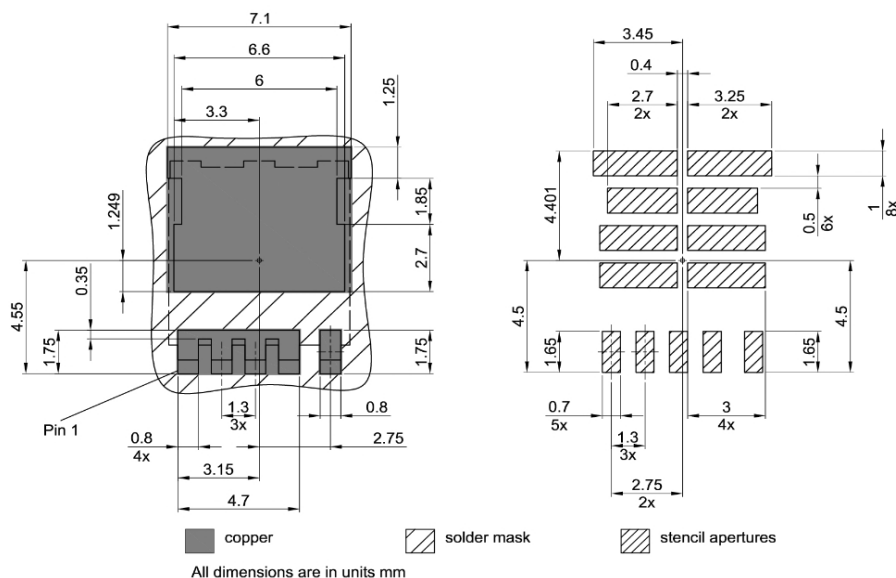
1) Lead length up to anti flash profile; mold flashes excluded

2) Excluding burr

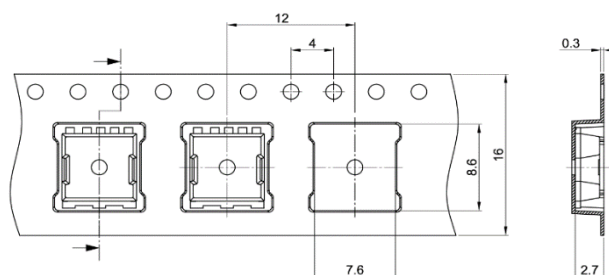
All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

Footprint



Packaging



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

Revision History

| Revision | Date | Changes |
|--------------|------------|-----------------|
| Revision 1.0 | 17.03.2021 | Final Datasheet |

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