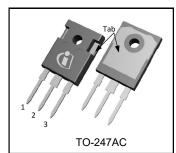


V _{DSS} min	250V
V _{DS (Avalanche)} typ.	300V
R _{DS(on)} typ.	29 mΩ
I _D	57A

Drain Pin 2, Tab Gate Pin 1 Source Pin 3



Features

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low E_{PULSE} Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low Q_G for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Description

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low E_{PULSE} rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications

Base Part Number	Packago Typo	Standard Pack		Orderable Part Number	
Base Fait Number	Package Type	Form	Quantity	Orderable Part Number	
IRFP4332PbF	TO-247AC	Tube	25	IRFP4332PbF	

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units	
V_{GS}	Gate-to-Source Voltage	± 30	V	
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, V _{GS} @ 10V	57		
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	40	A	
I _{DM}	Pulsed Drain Current ①	230		
I _{RP} @ T _C = 100°C	Repetitive Peak Current®®	120		
P _D @T _C = 25°C	Power Dissipation	360	10/	
P _D @T _C = 100°C	Power Dissipation	180	W	
	Linear Derating Factor	2.4	W/°C	
TJ	Operating Junction and	40 to 1.475		
T _{STG}	Storage Temperature Range	-40 to + 175	°C	
	Soldering Temperature, for 10 seconds (1.6mm from case)	300		
	Mounting torque, 6-32 or M3 screw	10lbf₊in (1.1N⋅m)		

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④		0.42	
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24		°C/W
$R_{\theta JA}$	Junction-to-Ambient		40	



Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250			V	$V_{GS} = 0V, I_D = 250\mu A$
	Breakdown Voltage Temp. Coefficient		170		mV/°C	Reference to 25°C, I _D = 1mA①
R _{DS(on)}	Static Drain-to-Source On-Resistance		29	33	mΩ	V _{GS} = 10V, I _D = 35A ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0		5.0	V	V - V I - 250::A
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient		-14		mV/°C	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
	Drain to Source Leakage Current			20	μA	$V_{DS} = 250V, V_{GS} = 0V$
I _{DSS}	Drain-to-Source Leakage Current			200	μΑ	$V_{DS} = 250V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
1	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
I _{GSS}	Gate-to-Source Reverse Leakage			-100	IIA	$V_{GS} = -20V$
gfs	Forward Transconductance	100			S	$V_{DS} = 25V, I_{D} = 35A$
Q_g	Total Gate Charge		99	150	nC	V_{DD} = 125V, I_{D} = 35A
Q_{gd}	Gate-to-Drain ("Miller") Charge		35		110	V _{GS} = 10V ③
t _{st}	Shoot Through Blocking Time	100			ns	V_{DD} = 200V, V_{GS} = 15V, R_{G} = 4.7 Ω
F	En annua de Dulas		520		1	L = 220nH,C = 0.3μ F, V_{GS} = 15V V_{DD} = 200V, R_{G} = 5.1Ω , T_{J} = 25°C
E _{PULSE}	Energy per Pulse		920		μJ	L = 220nH,C = 0.3μ F, V_{GS} = 15V V_{DD} = 200V, R_{G} = 5.1Ω , T_{J} = 100°C
C _{iss}	Input Capacitance		5860			V _{GS} = 0V
C _{oss}	Output Capacitance		530			$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance		130		pF	f = 1.0 MHz
C _{oss} eff.	Effective Output Capacitance		360		1	V_{GS} = 0V, V_{DS} = 0V to 200 V
L _D	Internal Drain Inductance		5.0		nH	Between lead,
L _S	Internal Source Inductance		13		1111	from package

Avalanche Characteristics

Avaiding ondirections					
	Parameter	Тур.	Max.	Units	
E _{AS}	Single Pulse Avalanche Energy ②		210	m l	
E _{AR}	Repetitive Avalanche Energy ①		36	mJ	
V _{DS(Avalanche)}	Repetitive Avalanche Voltage ①	300		V	
I _{AS}	Avalanche Current ②		35	Α	

Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current			E 7		MOSFET symbol
	(Body Diode)			57	Α	showing the
I _{SM}	Pulsed Source Current			230	۸	integral reverse
	(Body Diode) ①			230	Α	p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C$, $I_S = 35A$, $V_{GS} = 0V$ ③
t _{rr}	Reverse Recovery Time		190	290	ns	$T_J = 25^{\circ}C, I_F = 35A, V_{DD} = 50V$
Q _{rr}	Reverse Recovery Charge		820	1230	nC	di/dt = 100A/µs ③

- ① Repetitive rating; pulse width limited by max. Junction temperature.
- \odot Starting T_J = 25°C, L = 0.35mH, R_G = 25 Ω , I_{AS} = 35A.
- ③ Pulse width ≤ $400\mu s$; duty cycle ≤ 2%.

- ⊕ R₀ is measured at T₃ approximately 90°C.
 ⊕ Half sine wave with duty cycle = 0.25, ton=1µsec.
 ⊕ Applicable to Sustain and Energy Recovery applications.



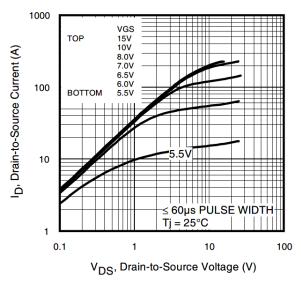


Fig 1. Typical Output Characteristics

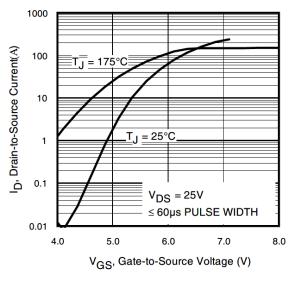


Fig 3. Typical Transfer Characteristics

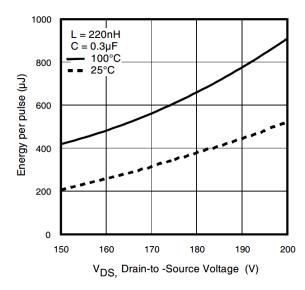


Fig 5. Typical E_{PULSE} vs. Drain-to-Source Voltage

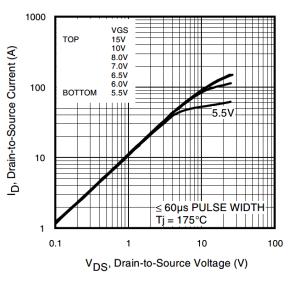


Fig 2. Typical Output Characteristics

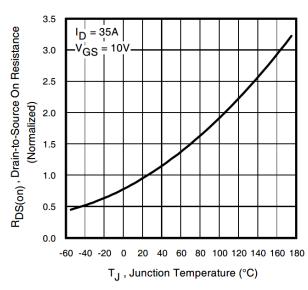


Fig 4. Normalized On-Resistance vs. Temperature

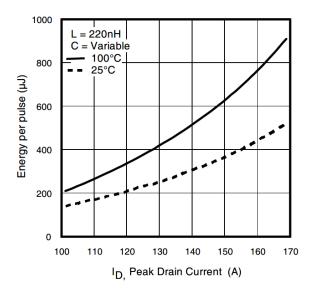


Fig 6. Typical E_{PULSE} vs. Drain Current



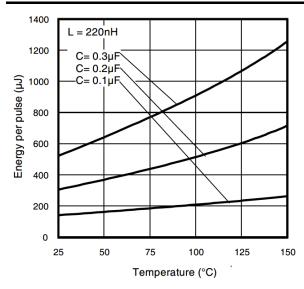


Fig 7. Typical E_{PULSE} vs. Temperature

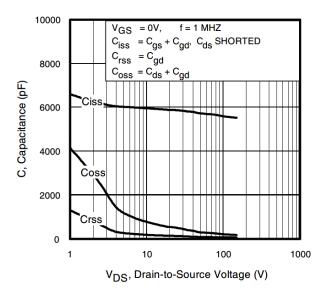


Fig 9. Typical Capacitance vs. Drain-to-Source Voltage

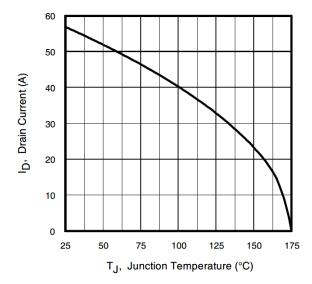


Fig 11. Maximum Drain Current vs. Case Temperature

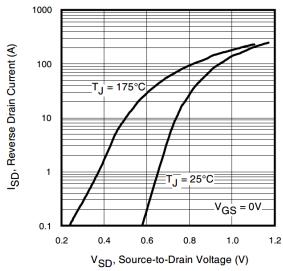


Fig 8. Typical Source-Drain Diode Forward Voltage

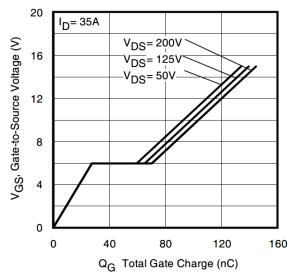


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

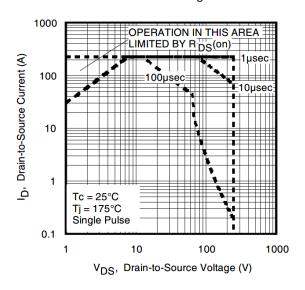


Fig 12. Maximum Safe Operating Area



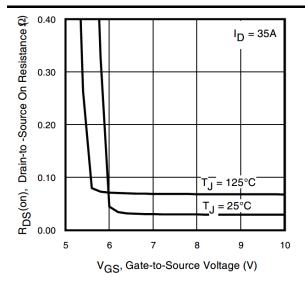


Fig 13. On-Resistance Vs. Gate Voltage

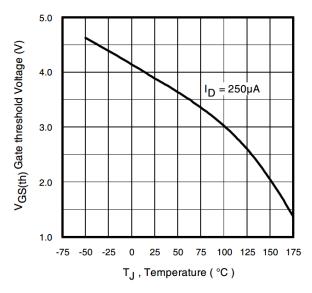


Fig 15. Threshold Voltage vs. Temperature

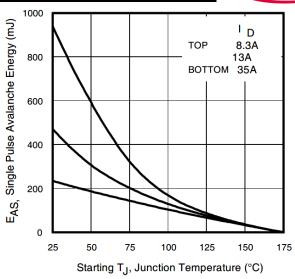


Fig 14. Maximum Avalanche Energy Vs. Temperature

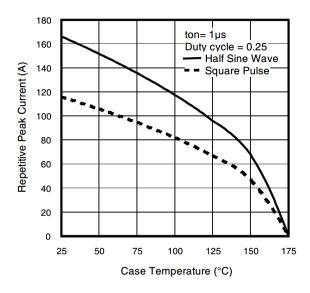


Fig 16. Typical Repetitive peak Current vs. Case temperature

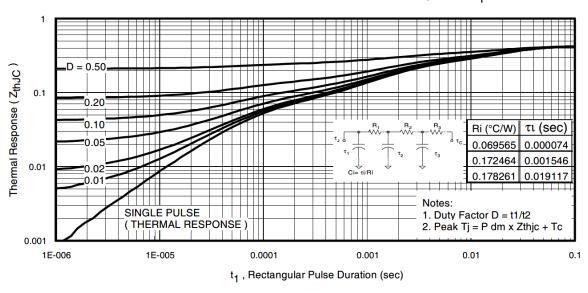


Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case



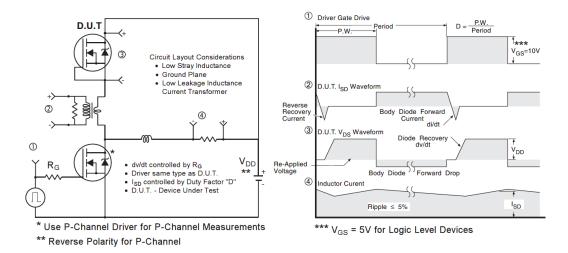


Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

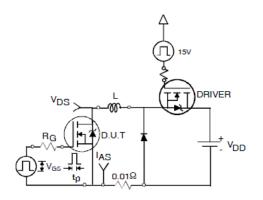


Fig 19a. Unclamped Inductive Test Circuit

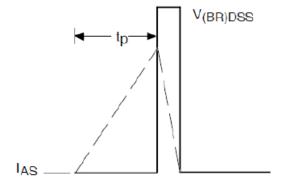


Fig 19b. Unclamped Inductive Waveforms

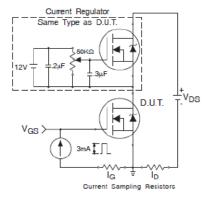


Fig 20a. Gate Charge Test Circuit

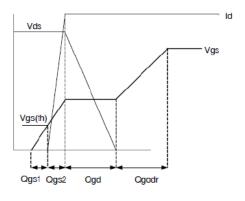
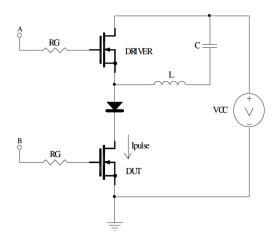


Fig 20b. Gate Charge Waveform





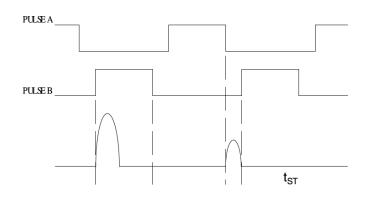


Fig 21a. $t_{\text{st}}\,\text{and}\,\,E_{\text{PULSE}}\,\text{Test}\,\,\text{Circuit}$

Fig 21b. t_{st} Test Waveforms

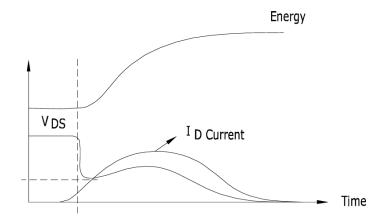
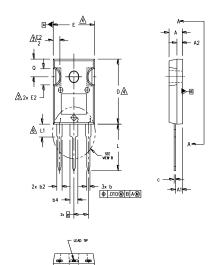
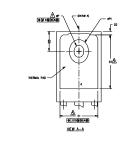


Fig 21c. E_{PULSE} Test Waveforms



TO-247AC Package Outline (Dimensions are shown in millimeters (inches))









NOTES:

- 1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
- 2. DIMENSIONS ARE SHOWN IN INCHES.

CONTOUR OF SLOT OPTIONAL.

DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127)

PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.

6. LEAD FINISH UNCONTROLLED IN L1.

ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 * TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

B. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

					_
		DIMEN	ISIONS		
SYMBOL	INC	HES	MILLIM	IETERS	
	MIN.	MAX.	MIN.	MAX.	NOTES
Α	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
С	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215	BSC	5.46	BSC	
Øk	.0	10	0.	25	
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØΡ	.140	.144	3.56	3.66	
øP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217	BSC	5.51	BSC	
					<u> </u>

LEAD ASSIGNMENTS

<u>HEXFET</u>

- 1.- GATE
- 2.- DRAIN 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

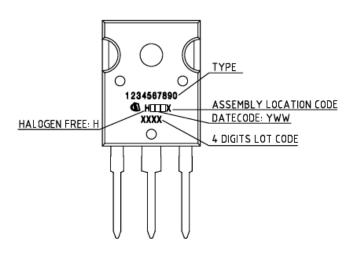
<u>DIODES</u>

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3. ANODE

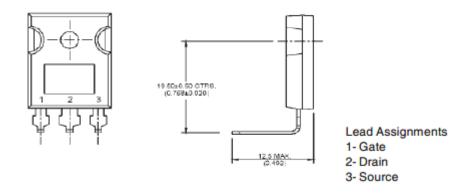
TO-247AC package is not recommended for Surface Mount Application.



TO-247AC Part Marking Information



TO-247AC Lead Option- 203 (Dimensions are shown in millimeters (inches))



TO-247AC package is not recommended for Surface Mount Application.



Revision History

Date	Rev.	Comments	
09/08/2008	2.1	Added—IRP spec "IRP max @Tc=100degC –page1	
12/15/2009	2.2	Added Part Marking drawing for Leadform -203 –pg9	
11/25/2024	2.3	 Update datasheet to Infineon format Updated Part marking –page 9 Added disclaimer on last page. 	

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