

MOSFET – Power, N-Channel**80 V, 1.75 mΩ****NVCR4LS1D7N08M7A****Features**

- Typical $R_{DS(on)} = 1.31\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$
- Typical $Q_{g(tot)} = 130\text{ nC}$ at $V_{GS} = 10\text{ V}$
- AEC-Q101 Qualified
- RoHS Compliant

DIMENSION (μm)

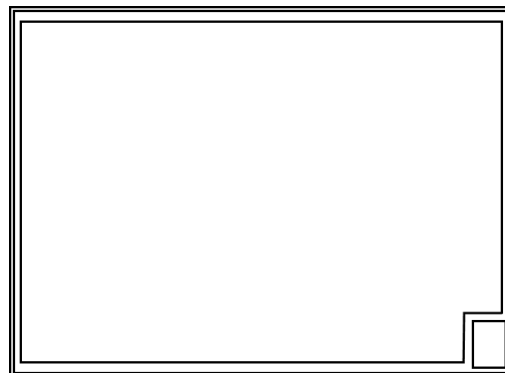
Die Size	5080 × 3683
Die Size (Sawn)	5060 ±15 × 3663 ±15
Source Attach Area	4874.7 × 3453.5
Gate Attach Area	359.9 × 483.5
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu
 Drain: Ti–NiV–Ag (back side of die)
 Passivation: Polyimide
 Wafer Diameter: 8 inch
 Wafer Sawn on UV Tape
 Bad Dice Identified in Inking
 Gross Die Counts: 1362

The Chip is 100% Probed to Meet the Conditions and Limits
 Specified at $T_J = 25^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	80	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	–	4.0	V
$*R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 5\text{ A}$, $V_{GS} = 10\text{ V}$	–	1.31	1.75	mΩ
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	–	–	1.2	V
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy	$L = 0.17\text{ mH}$, $I_{AS} = 70\text{ A}$	416	–	–	mJ

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

**ORDERING INFORMATION**

Device	Package
NVCR4LS1D7N08M7A	Wafer Sawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

NVCR4LS1D7N08M7A

MOSFET MAXIMUM RATINGS in Reference to the FDBL86363–F085 electrical data in TOLL
($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ ($V_{GS} = 10$) (Note 1) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	295 208	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	512	mJ
P_D	Power Dissipation $R_{\theta JC}$	357	W
	Derate Above 25°C	2.38	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by silicon.
- Starting $T_J = 25^\circ\text{C}$, $L = 0.25$ mH, $I_{AS} = 64$ A, $V_{DD} = 80$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

ELECTRICAL CHARACTERISTICS in Reference to the FDBL86363–F085 electrical data in TOLL
($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$ V	80	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 80$ V, $V_{GS} = 0$ V	$T_J = 25^\circ\text{C}$	–	–	μA
			$T_J = 175^\circ\text{C}$ (Note 4)	–	–	1 mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	$I_D = 80$ A, $V_{GS} = 10$ V	$T_J = 25^\circ\text{C}$	–	1.5	2.0 m Ω
			$T_J = 175^\circ\text{C}$ (Note 4)	–	3.1	4.1 m Ω

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40$ V, $V_{GS} = 0$ V, $f = 1$ MHz	–	10000	–	pF
C_{oss}	Output Capacitance		–	1540	–	pF
C_{rss}	Reverse Transfer Capacitance		–	70	–	pF
R_g	Gate Resistance	$f = 1$ MHz	–	2.8	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0$ to 10 V, $V_{DD} = 64$ V, $I_D = 80$ A	–	130	–	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V, $V_{DD} = 64$ V, $I_D = 80$ A	–	18	–	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 64$ V, $I_D = 80$ A	–	47	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	24	–	nC

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay	$V_{DD} = 40$ V, $I_D = 80$ A, $V_{GS} = 10$ V, $R_{GEN} = 6 \Omega$	–	39	–	ns
t_r	Rise Time		–	63	–	ns
$t_{d(off)}$	Turn-Off Delay		–	61	–	ns
t_f	Fall Time		–	33	–	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80$ A, $V_{GS} = 0$ V	–	–	1.25	V
		$I_{SD} = 40$ A, $V_{GS} = 0$ V	–	–	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 80$ A, $dI_{SD}/dt = 100$ A/ μs , $V_{DD} = 64$ V	–	83	–	ns
Q_{rr}	Reverse Recovery Charge		–	118	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

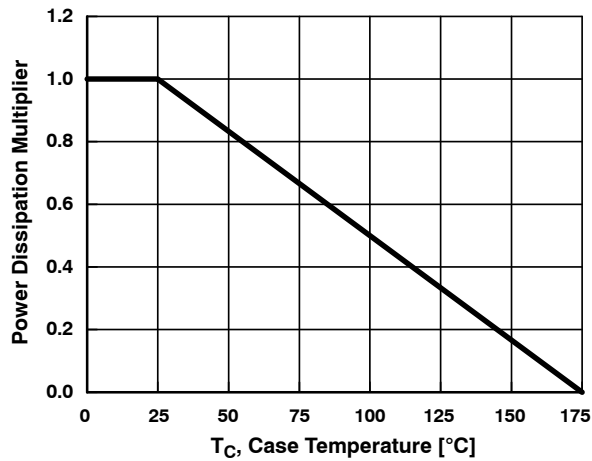


Figure 1. Normalized Power Dissipation vs. Case Temperature

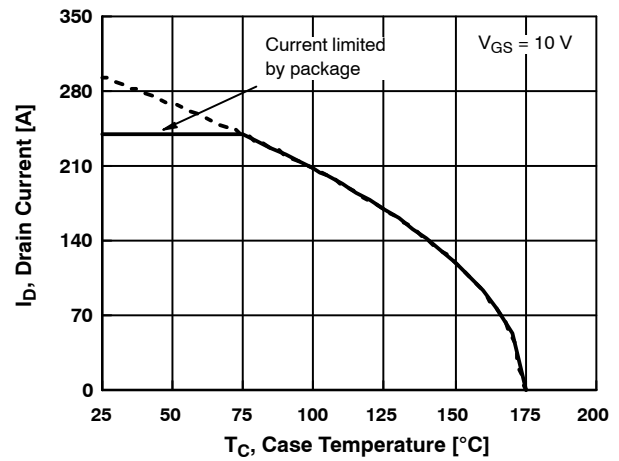


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

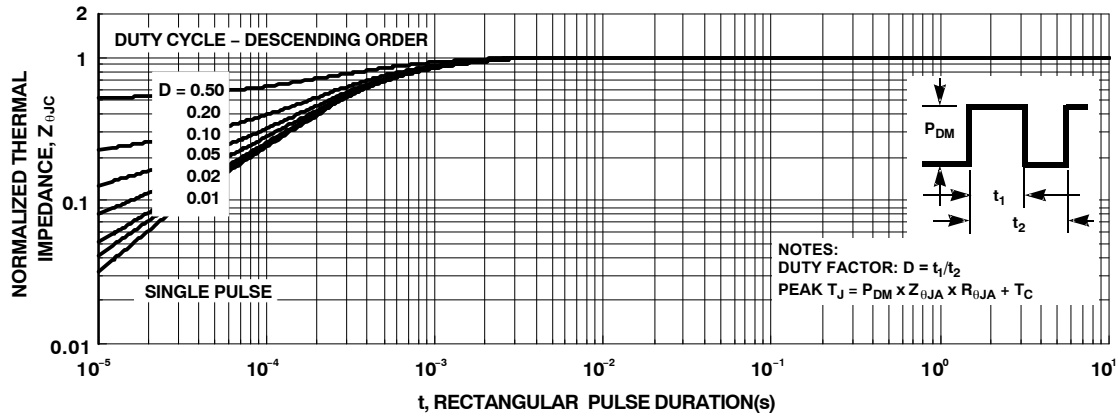


Figure 3. Normalized Maximum Transient Thermal Impedance

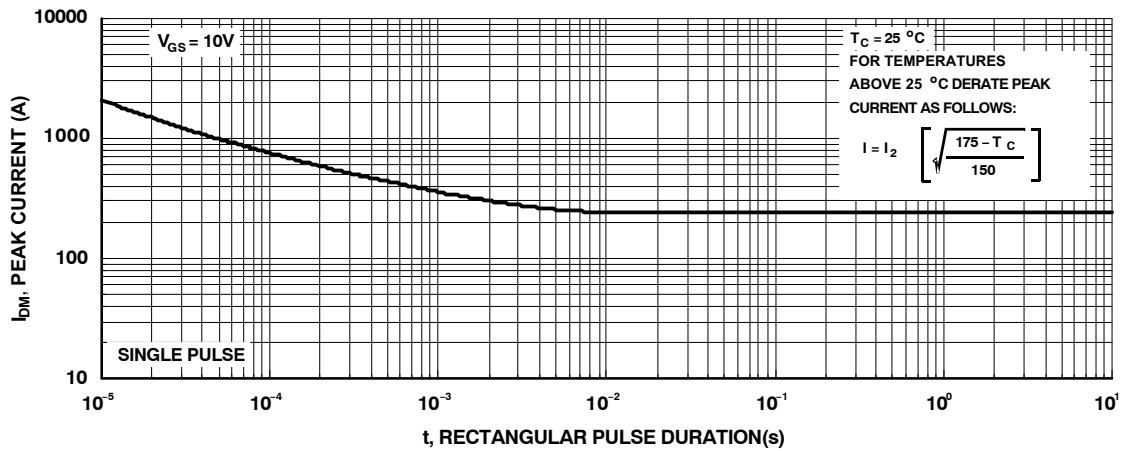


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

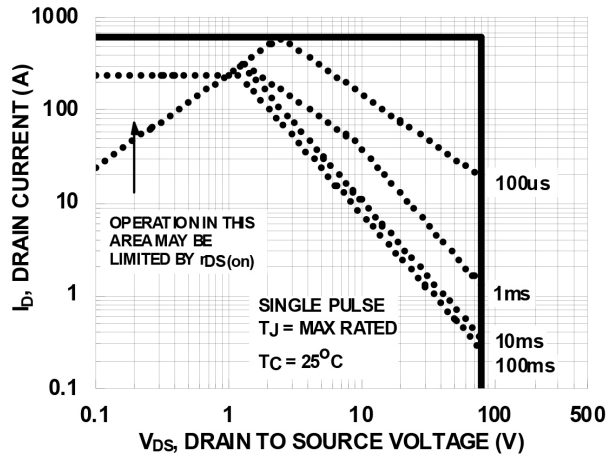


Figure 5. Forward Bias Safe Operating Area

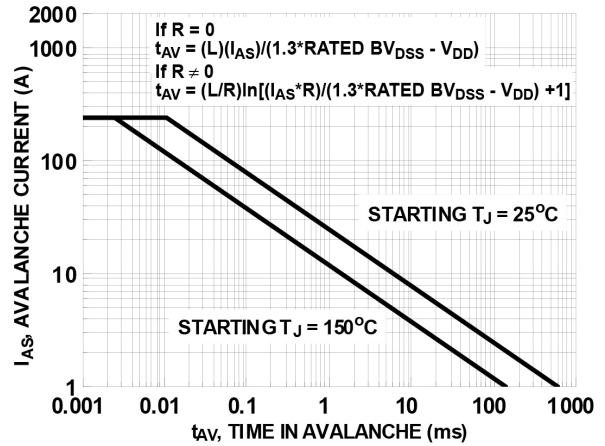


Figure 6. Unclamped Inductive Switching Capability

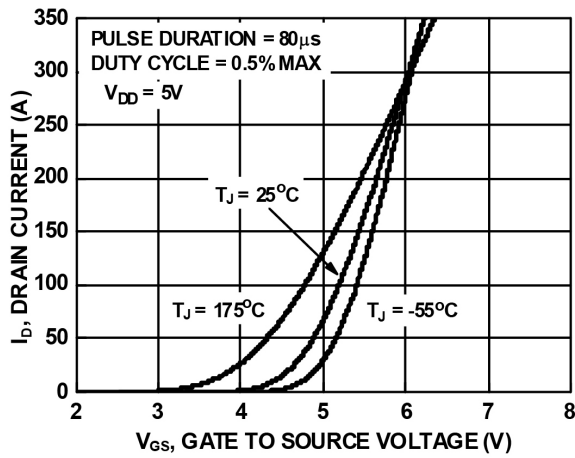


Figure 7. Transfer Characteristics

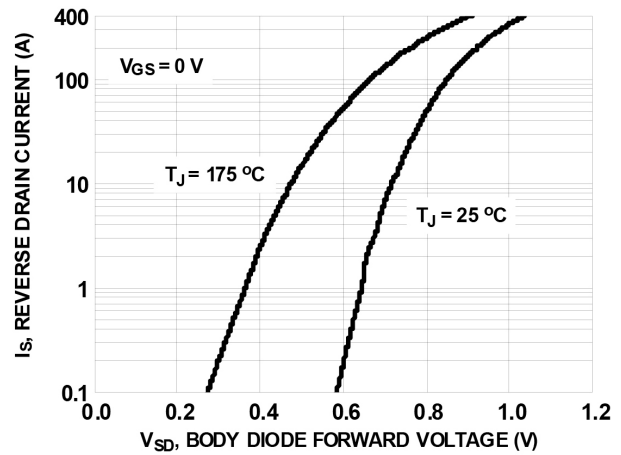


Figure 8. Forward Diode Characteristics

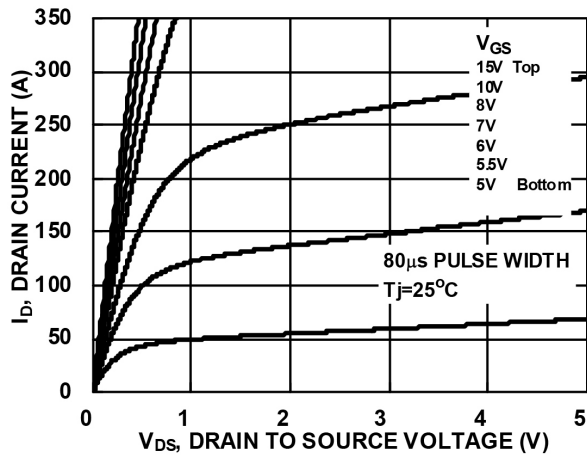


Figure 9. Saturation Characteristics

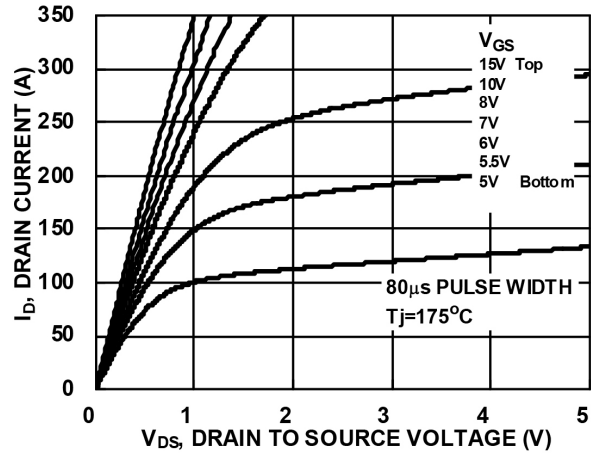


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

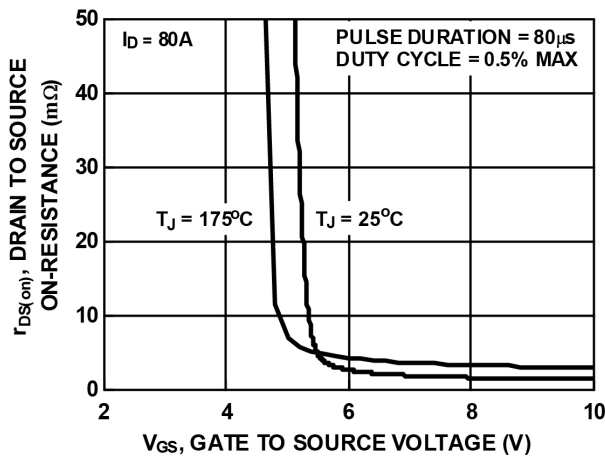


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

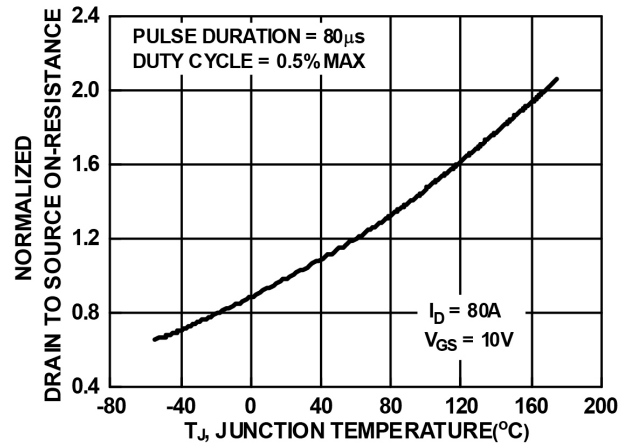


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

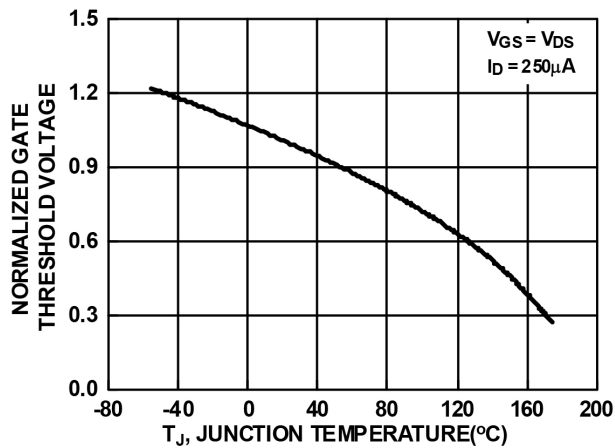


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

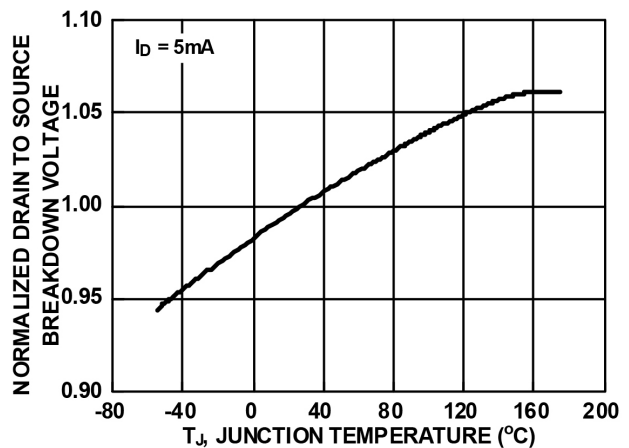


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

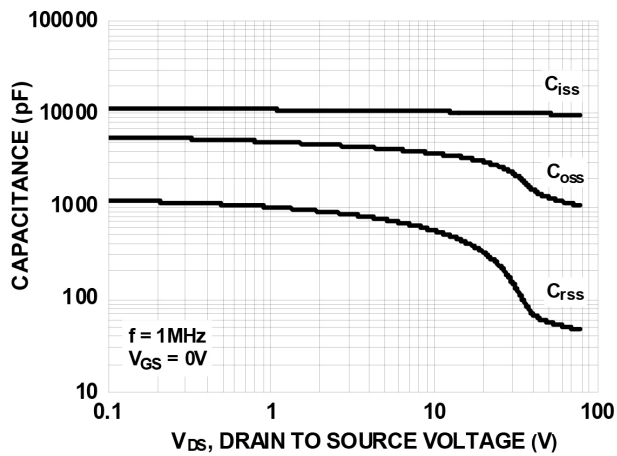


Figure 15. Capacitance vs. Drain to Source Voltage

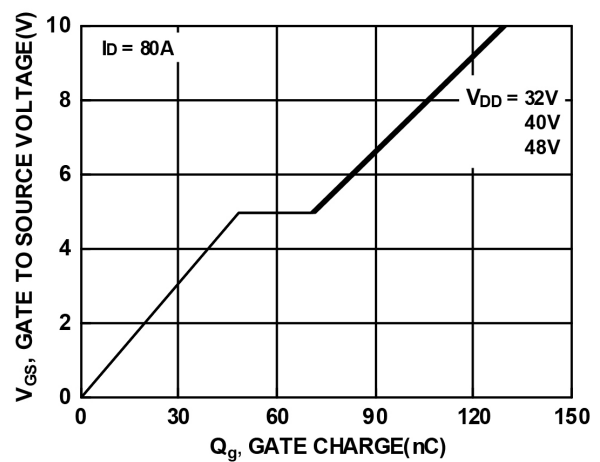


Figure 16. Gate Charge vs. Gate to Source Voltage

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales