

# MOSFET – Power, N-Channel, Ultrafet

100 V, 56 A, 25 mΩ

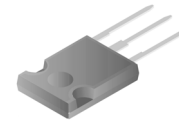
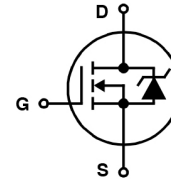
## HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

These N-Channel power MOSFETs are manufactured using the innovative Ultrafet process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

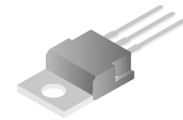
Formerly developmental type TA75639.

### Features

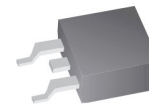
- 56 A, 100 V
- Simulation Models
  - ♦ Temperature Compensated PSPICE<sup>®</sup> and SABER<sup>™</sup> Electrical Models
  - ♦ Spice and Saber Thermal Impedance Models
  - ♦ [www.onsemi.com](http://www.onsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - ♦ TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



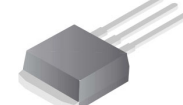
TO-247-3LD  
CASE 340CK



TO-220-3LD  
CASE 340AT

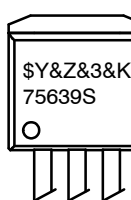
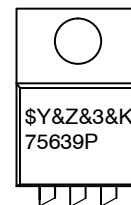
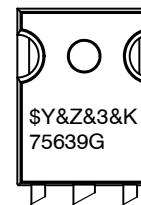


D2PAK-3  
CASE 418AJ



I2PAK  
CASE 418AV

### MARKING DIAGRAMS



&Y	= onsemi Logo
&Z	= Assembly Plant Code
&3	= 3-Digit Date Code
&K	= 2-Digit Lot Traceability Code
75639x	= Specific Device Code
x	= G/P/S

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

## ORDERING INFORMATION

PART NUMBER	PACKAGE	BRAND
HUF75639G3	TO-247	75639G
HUF75639P3	TO-220AB	75639P
HUF75639S3ST	TO-263AB	75639S
HUF75639S3	TO-262AA	75639S

## PACKAGING

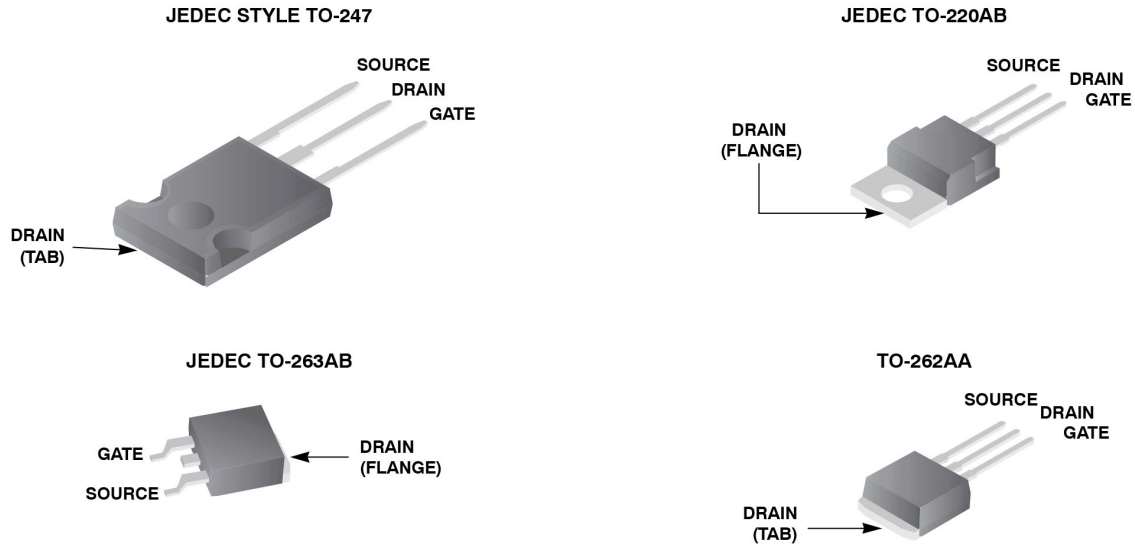


Figure 1.

## ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise specified

Description	Symbol	Ratings	Units
Drain to Source Voltage (Note 1)	$V_{DS}$	100 V	V
Drain to Gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ ) (Note 1)	$V_{DGR}$	100 V	V
Gate to Source Voltage	$V_{GS}$	$\pm 20\text{ V}$	V
Drain Current Continuous (Figure 2) Pulsed Drain Current	$I_D$ $I_{DM}$	56 Figure 4	A
Pulsed Avalanche Rating	$E_{AS}$	Figures 6, 14, 15	
Power Dissipation Derate Above $25^\circ\text{C}$	$P_D$	200 1.35	W W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{STG}$	$-55\text{ to }175^\circ\text{C}$	$^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6 mm) from Case for 10s Package Body for 10 s, See Techbrief 334	$T_L$ $T_{pkg}$	300 260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

# HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

**ELECTRICAL SPECIFICATION**  $T_J = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
--------	-----------	-----------------	-----	-----	-----	-------

## OFF STATE SPECIFICATIONS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$ (Figure 11)	100	–	–	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 95\ \text{V}$ , $V_{GS} = 0\ \text{V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 90\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_C = 150^\circ\text{C}$	–	–	250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	$\pm 100$	nA

## ON STATE SPECIFICATIONS

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$ (Figure 10)	2	–	4	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 56\ \text{A}$ , $V_{GS} = 10\ \text{V}$ (Figure 9)	–	21	25	m $\Omega$

## THERMAL SPECIFICATIONS

$R_{\theta JC}$	Thermal Resistance Junction to Case	(Figure 3)	–	–	0.74	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	TO-247	–	–	30	$^\circ\text{C/W}$
		TO-220, TO-263, TO-262	–	–	62	$^\circ\text{C/W}$

## SWITCHING SPECIFICATIONS ( $V_{GS} = 10\ \text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 50\ \text{V}$ , $I_D \cong 56\ \text{A}$ , $R_L = 0.89\ \Omega$ , $V_{GS} = 10\ \text{V}$ , $R_{GS} = 5.1\ \Omega$	–	–	110	ns
$t_{d(ON)}$	Turn-On Delay Time		–	15	–	ns
$t_r$	Rise Time		–	60	–	ns
$t_{d(OFF)}$	Turn-Off Delay Time		–	20	–	ns
$t_f$	Fall Time		–	25	–	ns
$t_{OFF}$	Turn-Off Time		–	–	70	ns

## GATE CHARGE SPECIFICATIONS

$Q_g(TOT)$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $20\ \text{V}$	$V_{DD} = 50\ \text{V}$ , $I_D \cong 56\ \text{A}$ , $R_L = 0.89\ \Omega$ , $I_{g(REF)} = 1.0\ \text{mA}$ (Figure 13)	–	110	130	nC
$Q_{g(10)}$	Gate Charge at $10\ \text{V}$	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$		–	57	75	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{V}$ to $2\ \text{V}$		–	3.7	4.5	nC
$Q_{gs}$	Gate to Source Gate Charge			–	9.8	–	nC
$Q_{gd}$	Gate to Drain “Miller” Charge			–	24	–	nC

## CAPACITANCE SPECIFICATIONS

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$ (Figure 12)	–	2000	–	pF
$C_{OSS}$	Output Capacitance		–	500	–	pF
$C_{RSS}$	Reverse Transfer Capacitance		–	65	–	pF

## SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 56\ \text{A}$	–	–	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 56\ \text{A}$ , $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	–	110	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 56\ \text{A}$ , $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	–	320	nC

TYPICAL PERFORMANCE CURVES

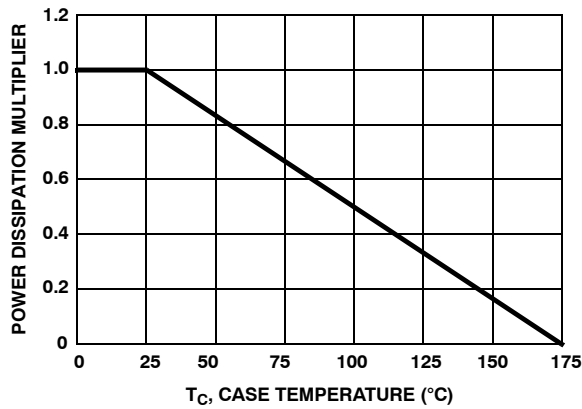


Figure 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

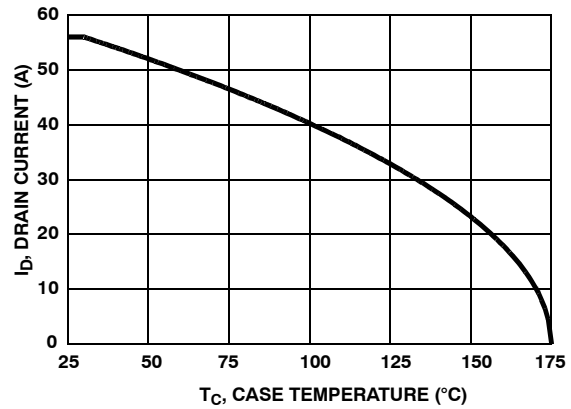


Figure 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

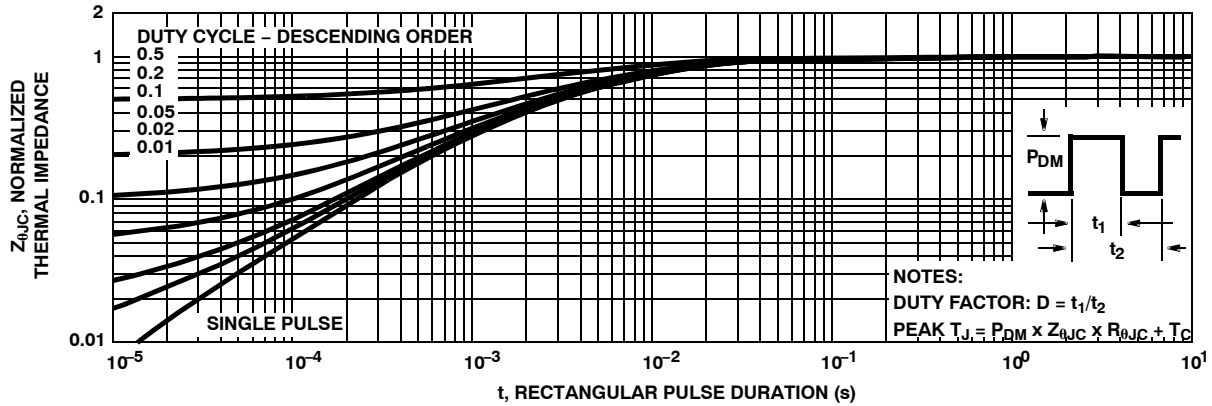


Figure 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

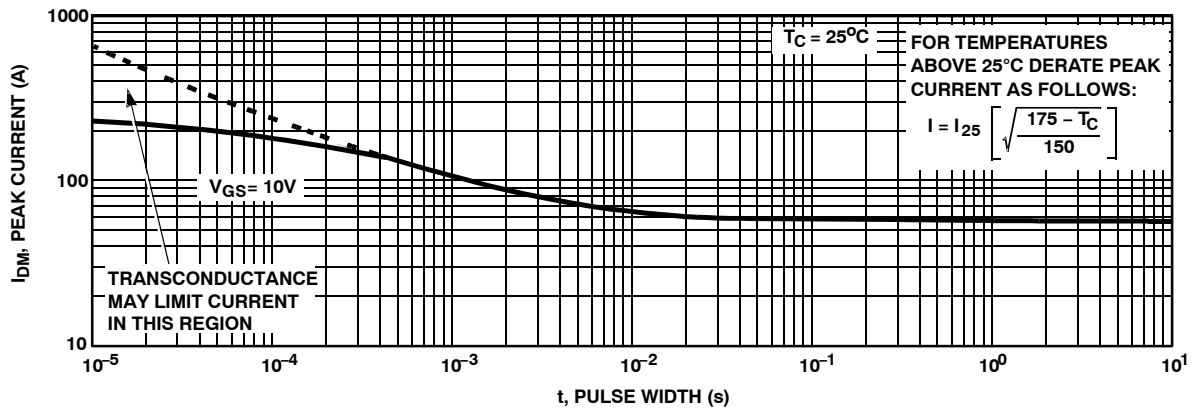


Figure 4. PEAK CURRENT CAPABILITY

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

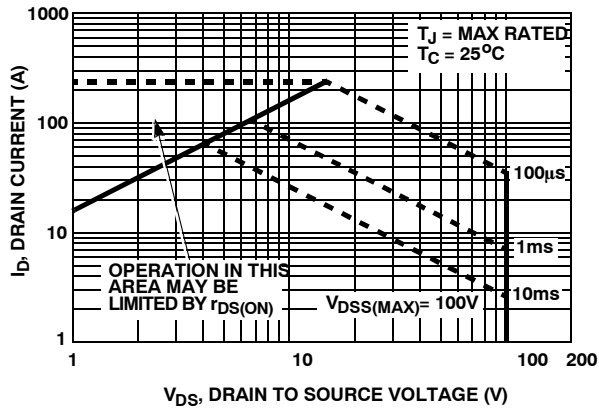


Figure 5. FORWARD BIAS SAFE OPERATING AREA

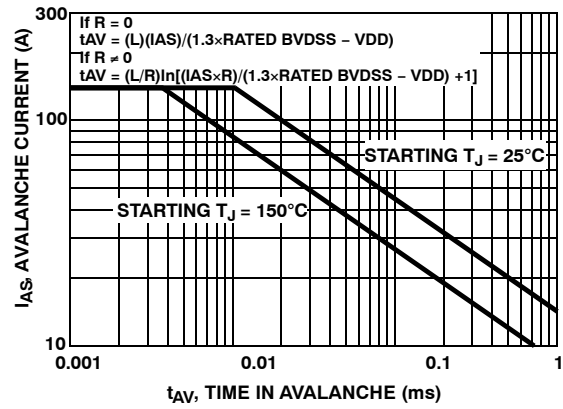


Figure 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

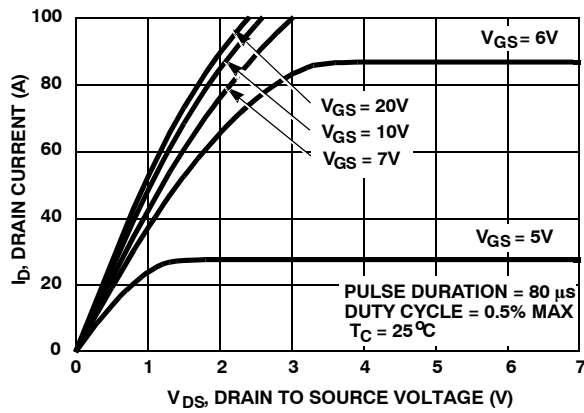


Figure 7. SATURATION CHARACTERISTICS

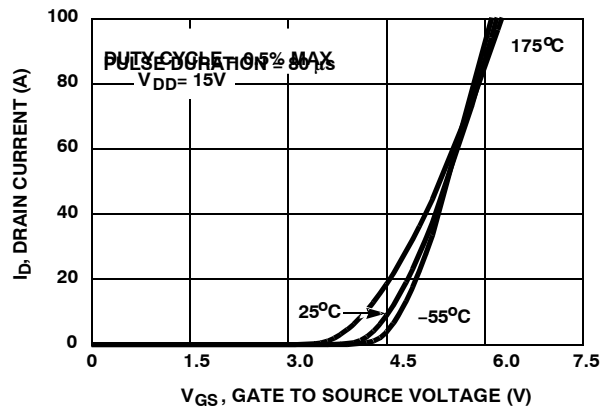


Figure 8. TRANSFER CHARACTERISTICS

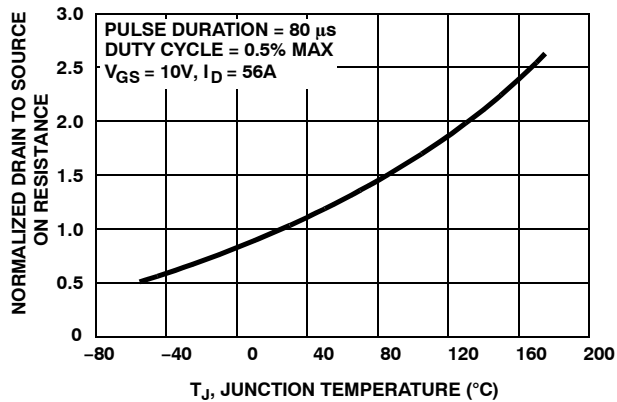


Figure 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

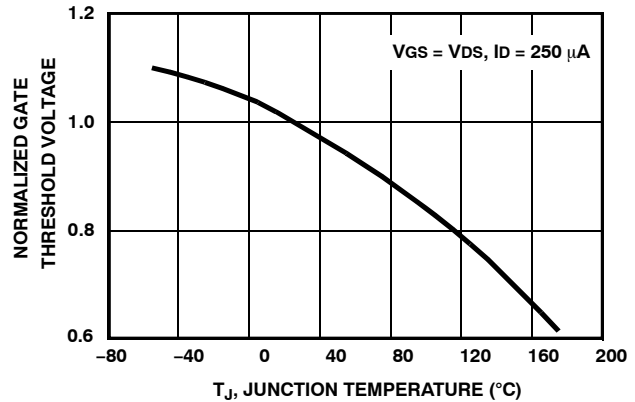


Figure 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

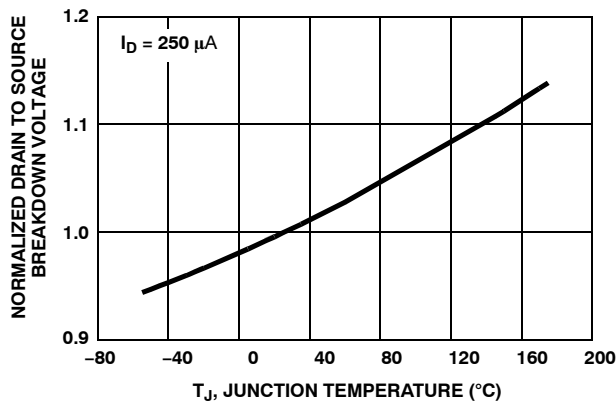


Figure 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

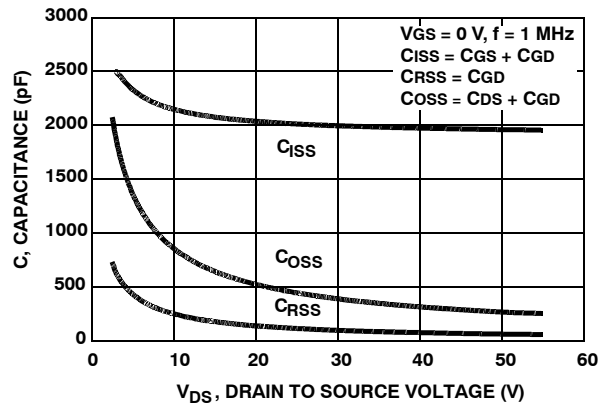


Figure 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

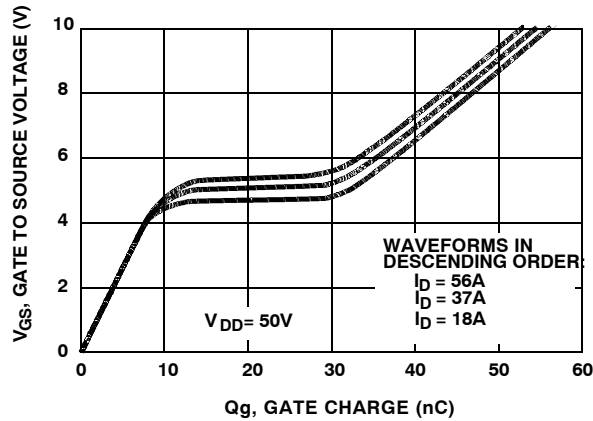


Figure 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

TEST CIRCUITS AND WAVEFORMS

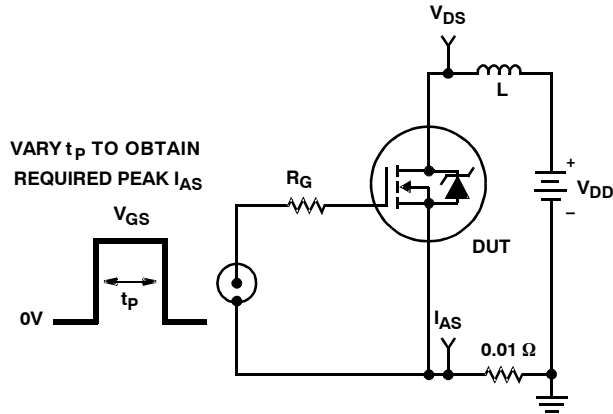


Figure 14. UNCLAMPED ENERGY TEST CIRCUIT

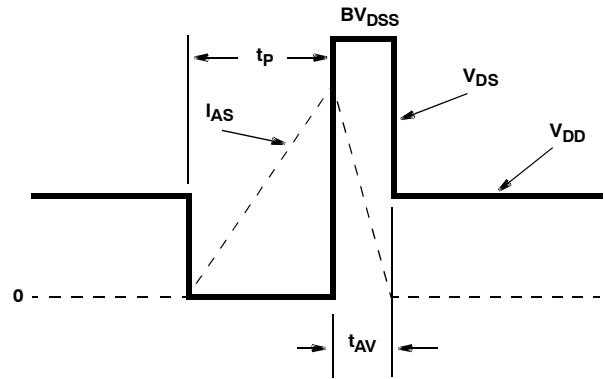


Figure 15. UNCLAMPED ENERGY WAVEFORMS

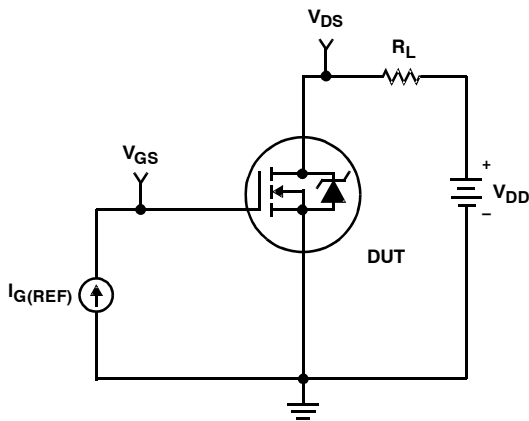


Figure 16. GATE CHARGE TEST CIRCUIT

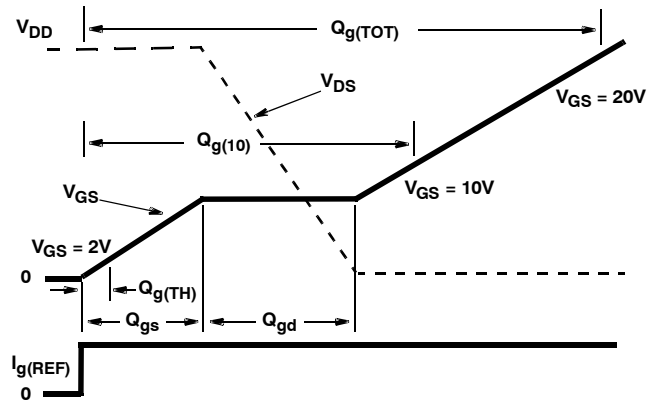


Figure 17. GATE CHARGE WAVEFORM

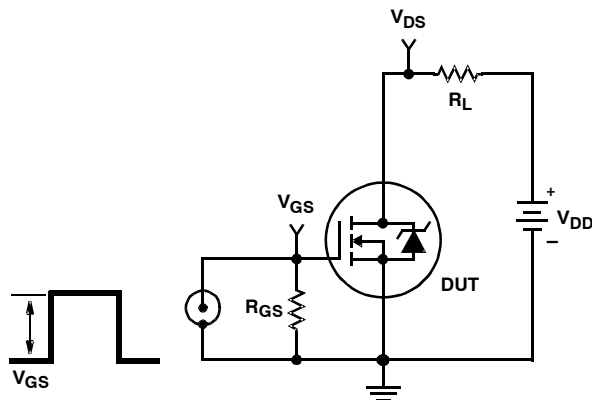


Figure 18. SWITCHING TIME TEST CIRCUIT

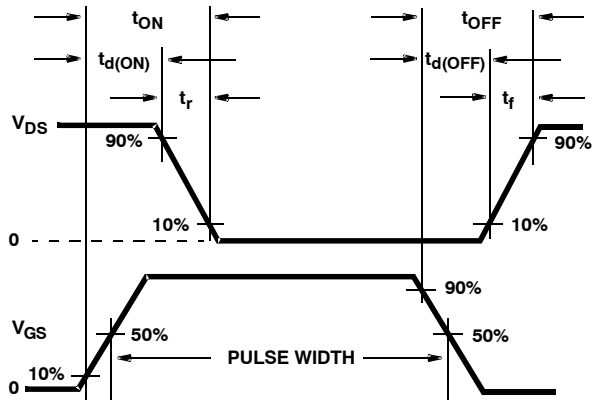


Figure 19. RESISTIVE SWITCHING WAVEFORMS

## PSPICE Electrical Model

SUBCKT HUF75639 2 1 3 ; rev Oct. 98  
 CA 12 8 2.8e-9  
 CB 15 14 2.65e-9  
 CIN 6 8 1.9e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 110  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 2e-9  
 LGATE 1 9 1e-9  
 LSGATE 3 7 0.47e-9  
 RLDRAIN 2 5 20  
 RLSOURCE 3 7 4.69

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 1.3e-2  
 RGATE 9 20 0.7  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSGATE 8 7 RSGATEMOD 4.5e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

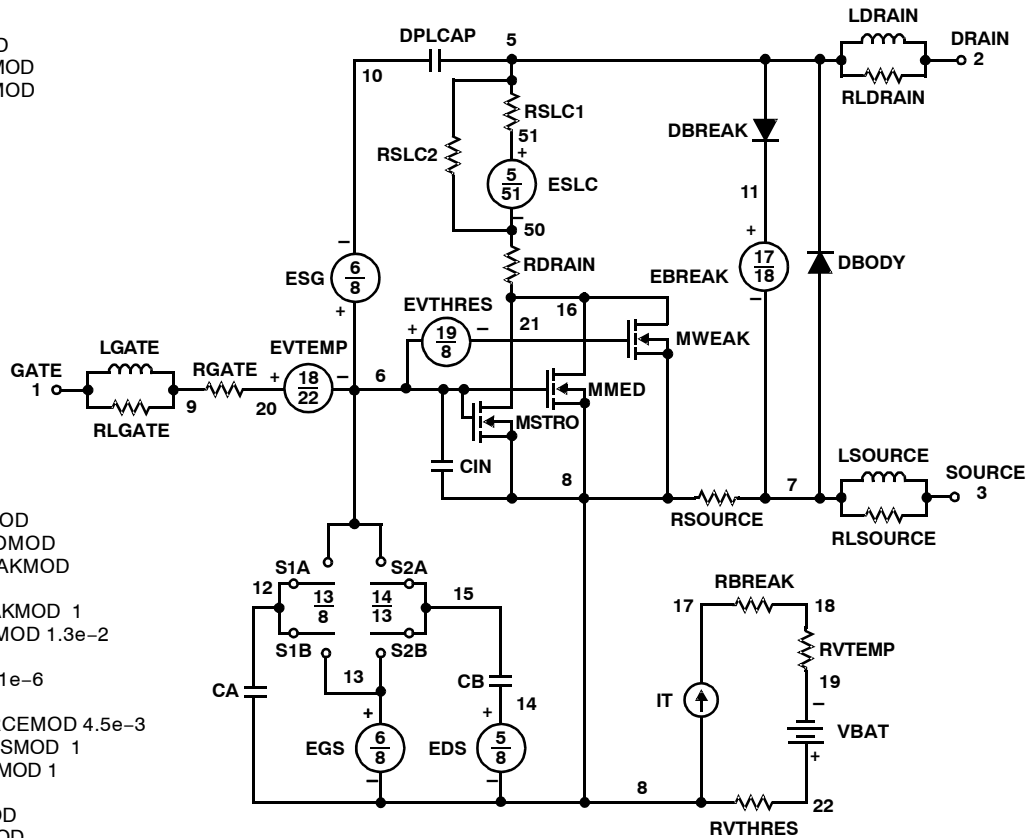
ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*115),4))}

.MODEL DBODYMOD D (IS = 1.4e-12 RS = 3.3e-3 XTI = 4.7 TRS1 = 2e-3 TRS2 = 0.1e-5 CJO = 3.3e-9 TT = 6.1e-8 M = 0.7)  
 .MODEL DBREAKMOD D (RS = 3.5e-1 TRS1 = 1e-3 TRS2 = 1e-6)  
 .MODEL DPLCAPMOD D (CJO = 2.2e-9 IS = 1e-3 ON = 10 M = 0.95 VJ = 1.0)  
 .MODEL MMEDMOD NMOS (VTO = 3.5 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Rg = 0.7)  
 .MODEL MSTROMOD NMOS (VTO = 3.97 KP = 56.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 3.11 KP = 0.085 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Rg = 7 RS = 0.1)  
 .MODEL RBREAKMOD RES (TC1 = 0.8e-3 TC2 = 1e-6)  
 .MODEL RDRAINMOD RES (TC1 = 1e-2 TC2 = 1.75e-5)  
 .MODEL RSLCMOD RES (TC1 = 2.8e-3 TC2 = 14e-6)  
 .MODEL RSGATEMOD RES (TC1 = 0 TC2 = 0)  
 .MODEL RVTHRESMOD RES (TC = -2.0e-3 TC2 = -1.75e-5)  
 .MODEL RVTEMPMOD RES (TC1 = -2.75e-3 TC2 = 0.05e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF = -3.5)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.5 VOFF = -6.0)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.5 VOFF = 4.95)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.95 VOFF = -2.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





## SABER Electrical Model

nom temp=25 deg c 100v Ultrafet

REV Oct. 98

template huf75639 n2,n1,n3  
electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is=1.4e-12, xti=4.7, cjo=33e-10, tt=6.1e-8, m=0.7)
d..model dbreakmod = ()
d..model dplcapmod = (cjo=22e-10, is=1e-30, n=10, m=0.95, vj=1.0)
m..model mmedmod = (type=_n, vto=3.5, kp=4.8, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto=3.97, kp=56.5, is=1e-30, tox=1)
m..model mweakmod = (type=_n, vto=3.11, kp=0.085, is=1e-30, tox=1)
sw_vcsp..model s1amod = (ron=1e-5, roff=0.1, von=-6.0, voff=-3.5)
sw_vcsp..model s1bmod = (ron=1e-5, roff=0.1, von=-3.5, voff=-6.0)
sw_vcsp..model s2amod = (ron=1e-5, roff=0.1, von=-2.5, voff=4.95)
sw_vcsp..model s2bmod = (ron=1e-5, roff=0.1, von=4.95, voff=-2.5)

c.ca n12 n8 = 28.5e-10
c.cb n15 n14 = 26.5e-10
c.cin n6 n8 = 19e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 2.0e-9
l.lgate n1 n9 = 1e-9
l.lsource n3 n7 = 4.69e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

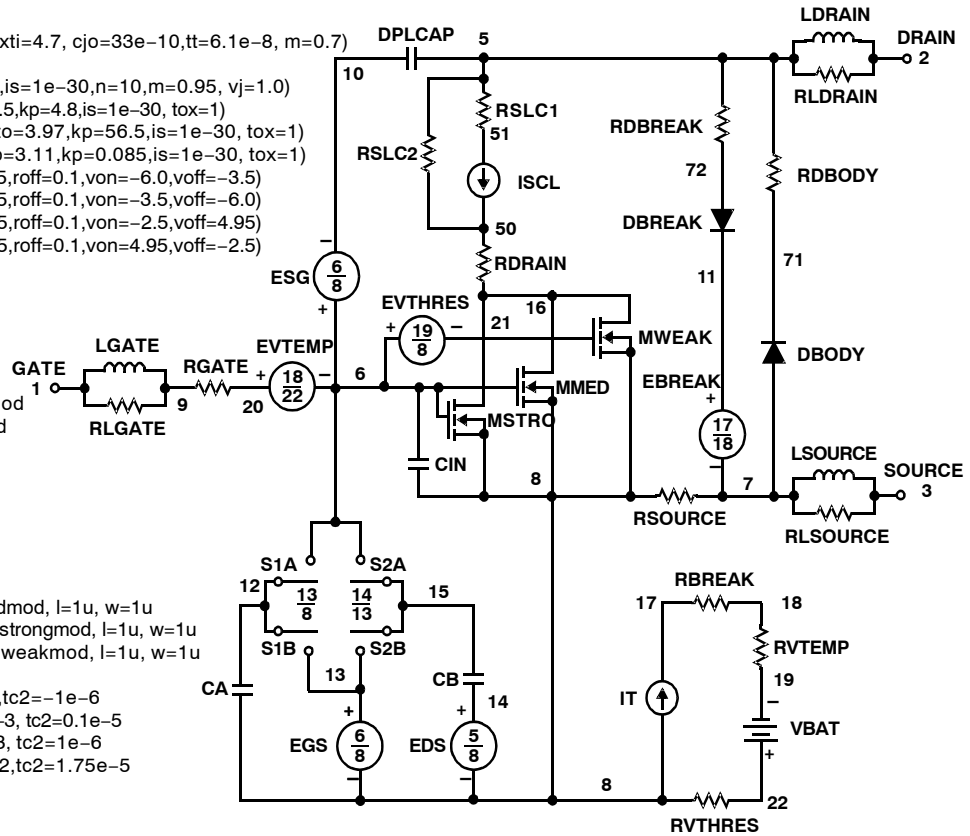
res.rbreak n17 n18 = 1, tc1=0.8e-3, tc2=-1e-6
res.rdbreak n71 n5 = 3.3e-3, tc1=2.0e-3, tc2=0.1e-5
res.rdrain n50 n16 = 13e-3, tc1=1e-2, tc2=1.75e-5
res.rgate n9 n20 = 0.7
res.rldrain n2 n5 = 20
res.rlgate n1 n9 = 10
res.rlsource n3 n7 = 4.69
res.rslc1 n5 n51 = 1e-6, tc1=2.8e-3, tc2=14e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4.5e-3, tc1=0, tc2=0
res.rvtemp n18 n19 = 1, tc1=-2.75e-3, tc2=0.05e-9
res.rvthres n22 n8 = 1, tc1=-2e-3, tc2=-1.75e-5

spe.ebreak n11 n7 n17 n18 = 110
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) += iscl
iscl: v(n51, n50) = ((v(n5, n51)/(1e-9+abs(v(n5, n51))))*((abs(v(n5, n51))*1e6/115))** 4))
}
}
```



## Spice Thermal Model

REV APRIL 1998

HUF75639

CTHERM1 TH 6 2.8e-3  
 CTHERM2 6 5 4.6e-3  
 CTHERM3 5 4 5.5e-3  
 CTHERM4 4 3 9.2e-3  
 CTHERM5 3 2 1.7e-2  
 CTHERM6 2 TL 4.3e-2

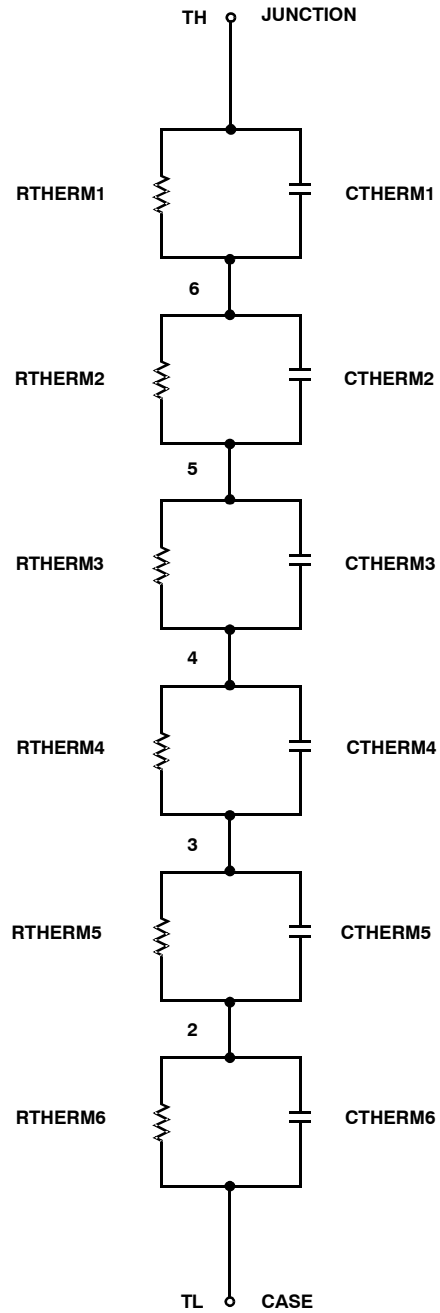
RTHERM1 TH 6 5.0e-4  
 RTHERM2 6 5 1.5e-3  
 RTHERM3 5 4 2.0e-2  
 RTHERM4 4 3 9.0e-2  
 RTHERM5 3 2 1.9e-1  
 RTHERM6 2 TL 2.9e-1

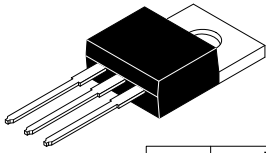
## Saber Thermal Model

Saber thermal model HUF75639

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 2.8e-3
    ctherm.ctherm2 6 5 = 4.6e-3
    ctherm.ctherm3 5 4 = 5.5e-3
    ctherm.ctherm4 4 3 = 9.2e-3
    ctherm.ctherm5 3 2 = 1.7e-2
    ctherm.ctherm6 2 tl = 4.3e-2

    rtherm.rtherm1 th 6 = 5.0e-4
    rtherm.rtherm2 6 5 = 1.5e-3
    rtherm.rtherm3 5 4 = 2.0e-2
    rtherm.rtherm4 4 3 = 9.0e-2
    rtherm.rtherm5 3 2 = 1.9e-1
    rtherm.rtherm6 2 tl = 2.9e-1
}
```

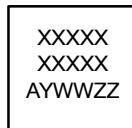



**TO-220-3LD**  
**CASE 340AT**  
**ISSUE B**

DATE 08 AUG 2022

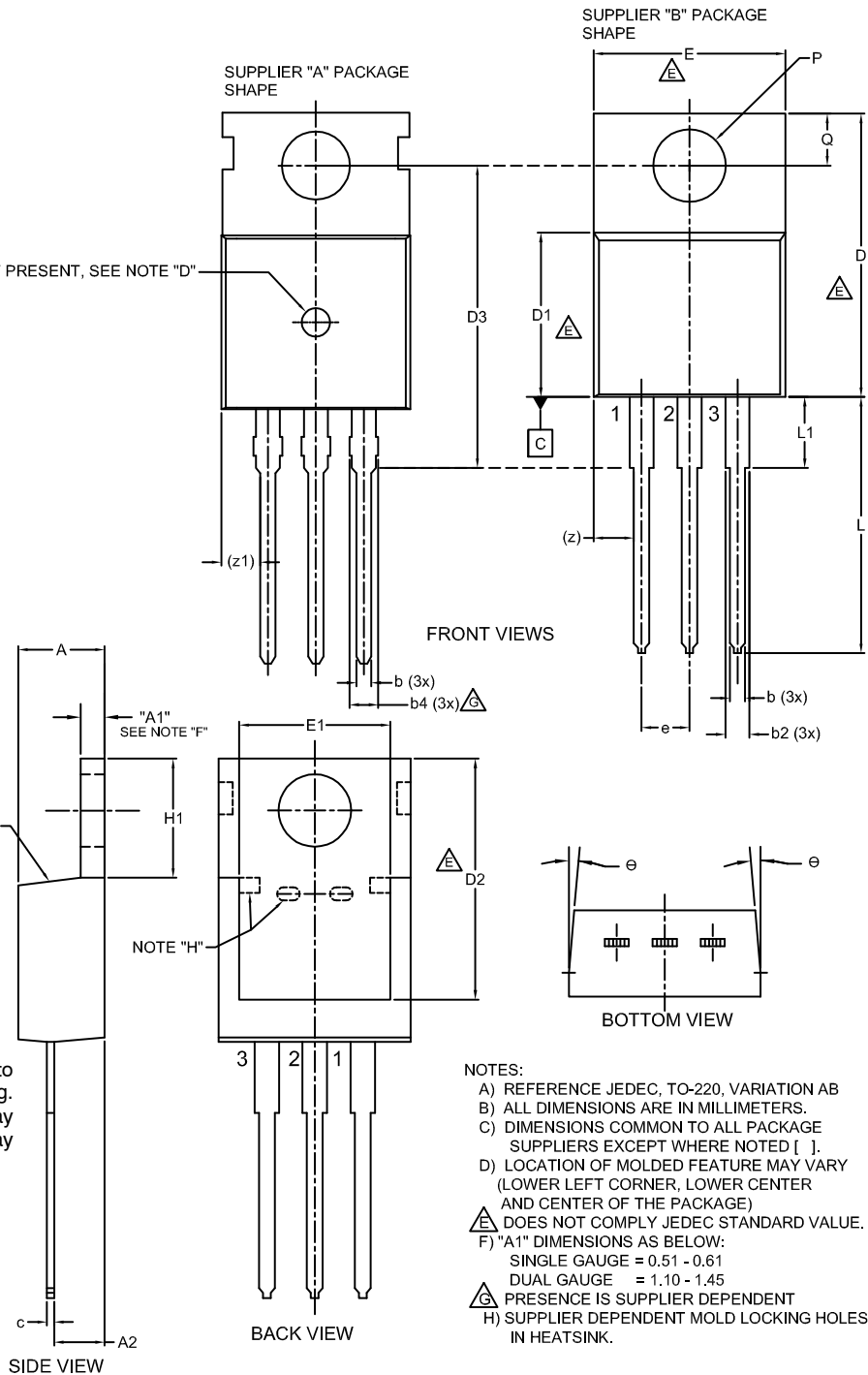
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

IF PRESENT, SEE NOTE "D"

**GENERIC**  
**MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.


**NOTES:**

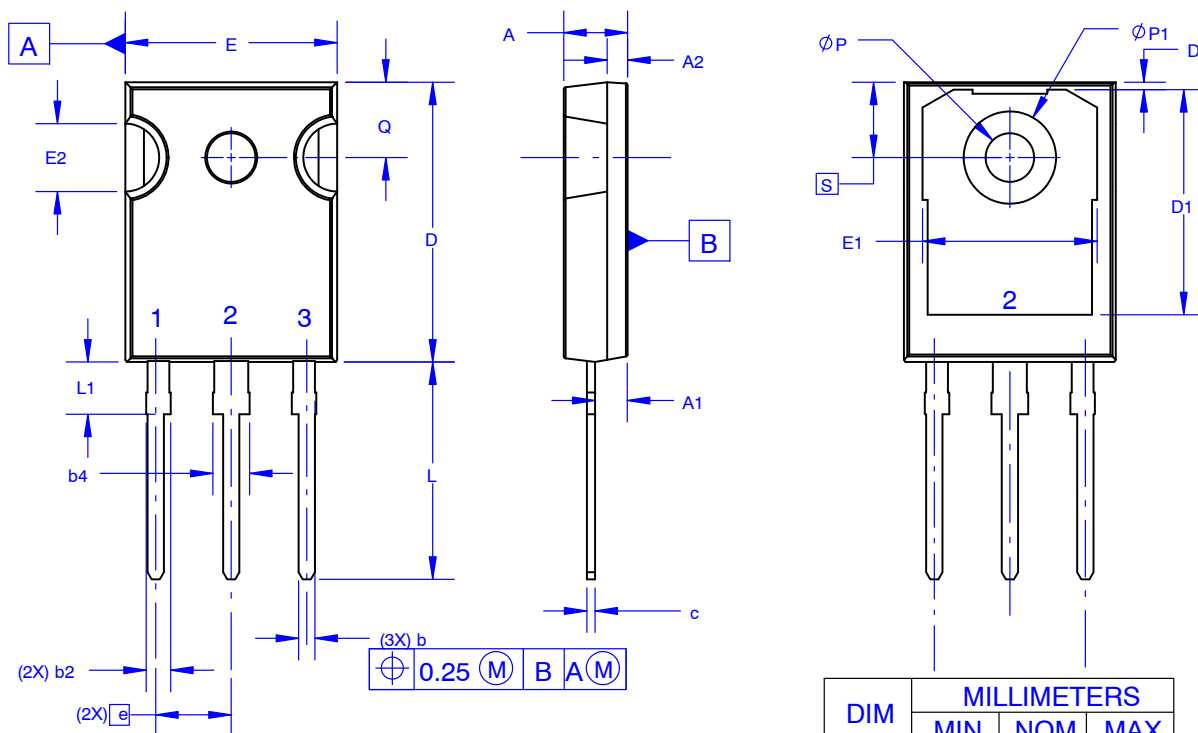
- REFERENCE JEDEC, TO-220, VARIATION AB
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- DOES NOT COMPLY JEDEC STANDARD VALUE.
- "A1" DIMENSIONS AS BELOW:  
SINGLE GAUGE = 0.51 - 0.61  
DUAL GAUGE = 1.10 - 1.45
- PRESENCE IS SUPPLIER DEPENDENT
- SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

<b>DOCUMENT NUMBER:</b>	<b>98AON13818G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-220-3LD</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**TO-247-3LD SHORT LEAD**  
**CASE 340CK**  
**ISSUE A**

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.  
B. ALL DIMENSIONS ARE IN MILLIMETERS.  
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.  
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.  
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

**GENERIC**  
**MARKING DIAGRAM\***

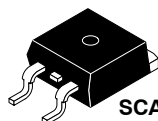

XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
$\phi P$	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

<b>DOCUMENT NUMBER:</b>	<b>98AON13851G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-247-3LD SHORT LEAD</b>	<b>PAGE 1 OF 1</b>

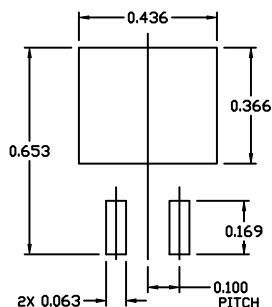
onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

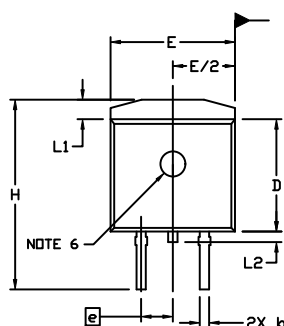
**D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)**  
CASE 418AJ  
ISSUE F

DATE 11 MAR 2021



**RECOMMENDED  
MOUNTING FOOTPRINT**

For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM1.

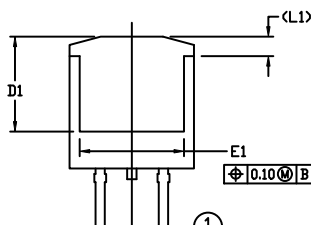
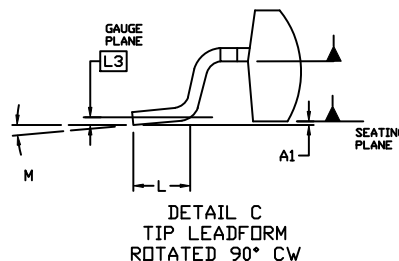
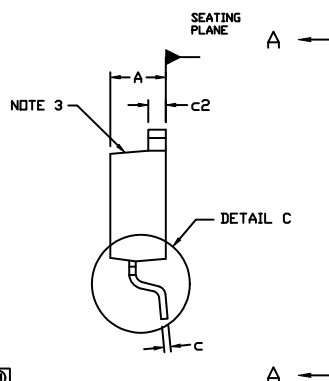


0.100 BSC 0.100 BSC

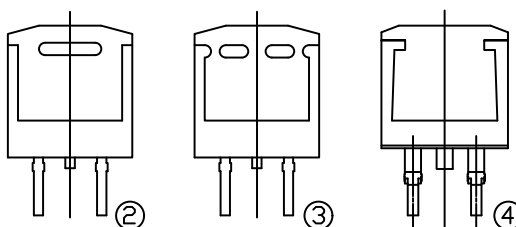
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC	---	2.54 BSC	---
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC	---	0.25 BSC	---
M	0°	8°	0°	8°

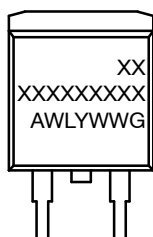


VIEW A-A

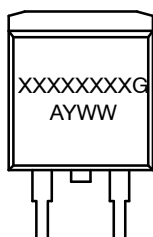


VIEW A-A  
OPTIONAL CONSTRUCTIONS

**GENERIC MARKING DIAGRAMS\***



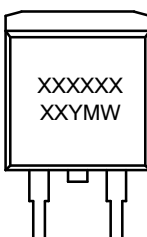
IC



Standard



Rectifier



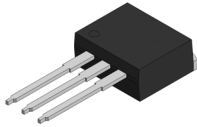
SSG

XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
W = Week Code (SSG)  
M = Month Code (SSG)  
G = Pb-Free Package  
AKA = Polarity Indicator

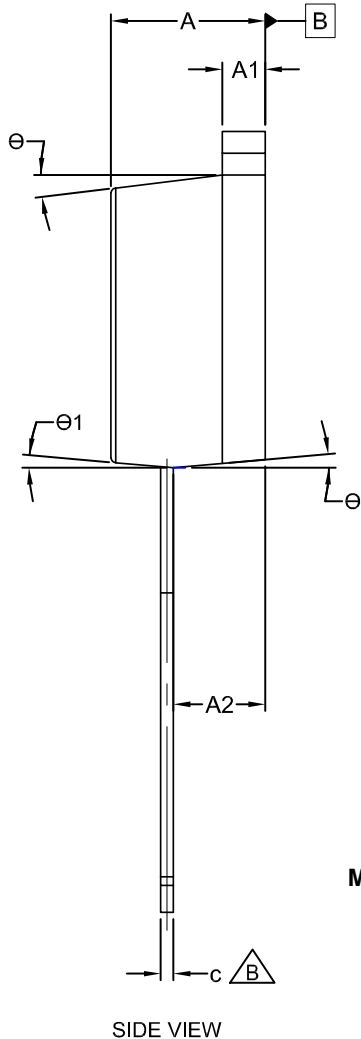
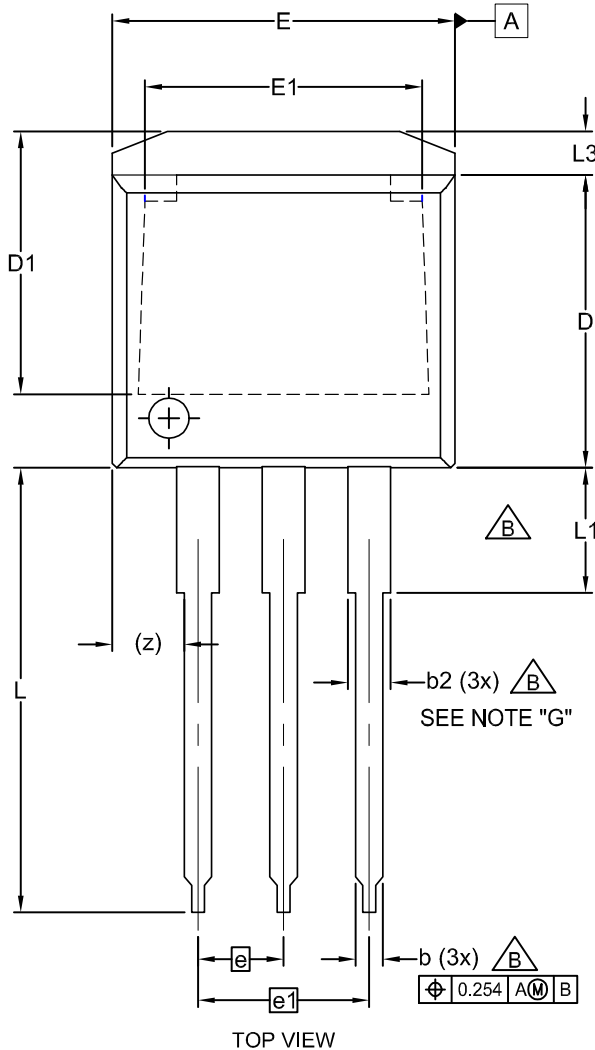
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98AON56370E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)</b>	<b>PAGE 1 OF 1</b>

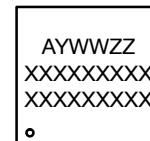
onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.


**I2PAK (TO-262 3 LD)**  
CASE 418AV  
ISSUE A

DATE 30 AUG 2022



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.06	4.45	4.83
A1	1.14	1.27	1.40
A2	2.03	2.41	2.79
b	0.64	0.77	0.90
b2	1.14	1.46	1.78
c	0.33	0.49	0.64
D	8.64	9.15	9.65
D1	6.86	7.37	7.88
E	9.65	9.97	10.29
E1	6.22	7.28	8.33
e	2.54 BSC		
e1	5.08 BSC		
L	12.70	13.72	14.73
L1	2.80	3.38	3.96
L3	1.00	1.20	1.40
z	2.13 REF		
θ	0°	--	7°
θ1	0°	--	5°

**GENERIC MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

**NOTES:**

- EXCEPT WHERE NOTED CONFORMS TO T262 JEDEC VARIATION AA.
- DOES NOT COMPLY JEDEC STD. VALUE.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

<b>DOCUMENT NUMBER:</b>	<b>98AON13814G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>I2PAK (TO-262 3 LD)</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)