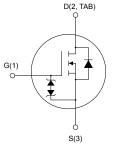


N-channel 650 V, 36 m Ω typ., 68 A MDmesh DM6 Power MOSFET in a TO-247 long leads package







Features

Order code	V _{DS}	R _{DS(on) max} .	l _D	
STWA70N65DM6	650 V	40 mΩ	68 A	

- Fast-recovery body diode
- Lower R_{DS(on)} per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

Switching applications

Description

AM01476v1 tab

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link	
STWA70N65DM6	

Product summary		
Order code STWA70N65DN		
Marking	70N65DM6	
Package	TO-247 long leads	
Packing	Tube	



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	68	Α
I _D	Drain current (continuous) at T _C = 100 °C	43	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	260	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	450	W
dv/dt (2)	Peak diode recovery voltage slope	100	V/ns
di/dt ⁽²⁾	Peak diode recovery current slope	1000	A/µs
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	100	V/ns
T _{STG}	Storage temperature range	55 to 150	°C
T _J	Operating junction temperature range	-55 to 150	°C

^{1.} Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	0.28	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (t _p limited by T _J max)	8	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$; $V_{DD} = 50$ V) 1.8		J

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^{2.} $I_{SD} \le 68 \text{ A}, V_{DS (peak)} < V_{(BR)DSS}, V_{DD} = 400 \text{ V}.$

^{3.} $V_{DS} \le 520 \text{ V}$.



2 Electrical characteristics

 T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
	Zono moto vielto no duois oviment	V _{GS} = 0 V, V _{DS} = 650 V			10	
IDSS	I _{DSS} Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V, T_{C} = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±5	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	3.25	4	4.75	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 34 A		36	40	mΩ

^{1.} Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	Input capacitance		4900	-	
C _{oss}	Output capacitance $V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$		-	280	-	
C _{rss}	Reverse transfer capacitance	9		3	-	pF
Coss eq. (1)	Equivalent output capacitance	ent output capacitance $V_{DS} = 0$ to 520 V, $V_{GS} = 0$ V		859	-	
R _G	Intrinsic gate resistance f = 1 MHz, I _D = 0 A		-	2.3	-	Ω
Qg	Total gate charge V _{DD} = 520 V, I _D = 68 A, V _{GS} = 0 to 10 V		-	125	-	
Q _{gs}	Gate-source charge	(see Figure 14. Test circuit for gate charge behavior)		33	-	nC
Q _{gd}	Gate-drain charge			56	-	

^{1.} $C_{\text{oss eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 34 A,	-	30.4	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	-	52	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and		107	-	ns
t _f	Fall time	Figure 18. Switching time waveform)	-	10.8	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		68	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		260	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 68 A	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 68 A, di/dt = 100 A/μs, V _{DD} = 60 V	-	170	-	ns
Q _{rr}	Reverse recovery charge	(see Figure 15. Test circuit for inductive	-	1.08	-	μC
I _{RRM}	Reverse recovery current	load switching and diode recovery times)		12.7	-	Α
t _{rr}	Reverse recovery time	I _{SD} = 68 A, di/dt = 100 A/μs,	-	308	-	ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V, T _J = 150 °C	-	4.16	-	μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	27	-	Α

^{1.} Pulse width is limited by safe operating area.

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^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.



2.1 Electrical characteristics (curves)

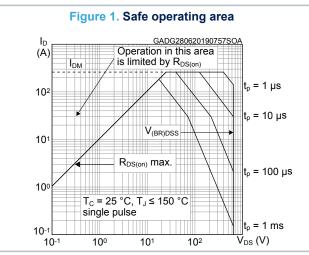


Figure 2. Maximum transient thermal impedance $\begin{array}{c|c} Z_{thj\text{-c}} \\ \hline (°C/W) \\ \hline \hline 10^{-1} \\ \hline \end{array}$

Figure 3. Typical output characteristics

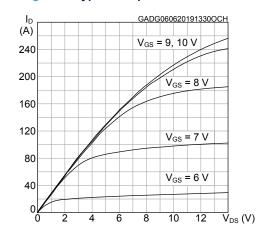


Figure 4. Typical transfer characteristics

10-3

10-2

t_p (s)

10-4

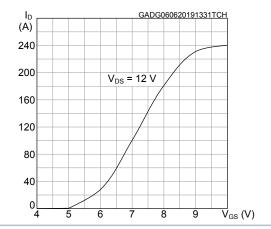


Figure 5. Typical gate charge characteristics

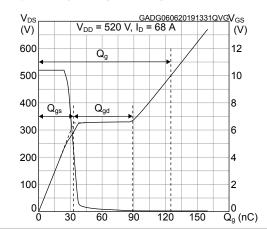
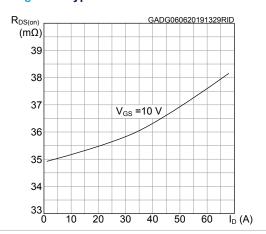


Figure 6. Typical drain-source on-resistance



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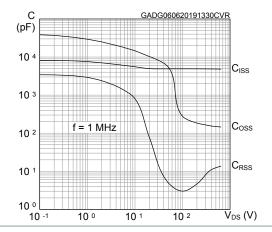


Figure 8. Typical output capacitance stored energy

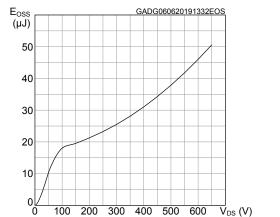


Figure 9. Normalized gate threshold vs temperature

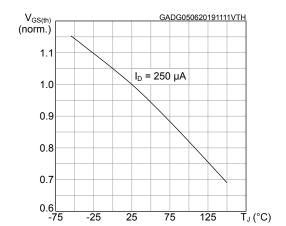


Figure 10. Normalized on-resistance vs. temperature

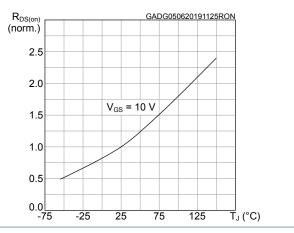


Figure 11. Normalized breakdown voltage vs temperature

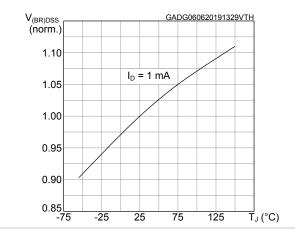
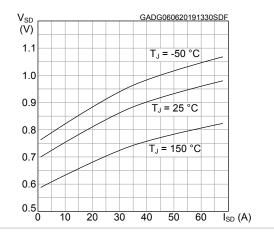


Figure 12. Typical reverse diode forward characteristics



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3 Test circuits

Figure 13. Test circuit for resistive load switching times

V_D

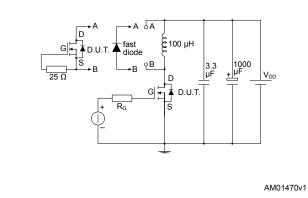
V_D

D.U.T.

AM01468v1

Figure 14. Test circuit for gate charge behavior $\begin{array}{c} V_{GS} \\ V_{GS} \\ \hline \\ V_{G$

Figure 15. Test circuit for inductive load switching and diode recovery times



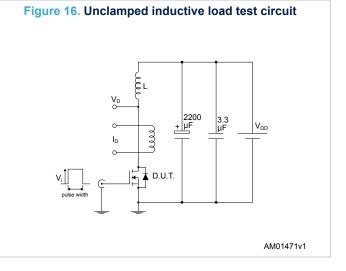


Figure 17. Unclamped inductive waveform

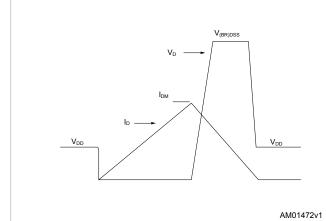
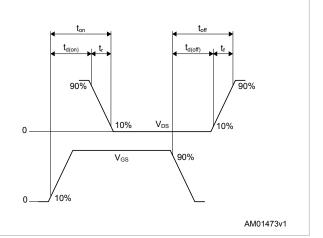


Figure 18. Switching time waveform



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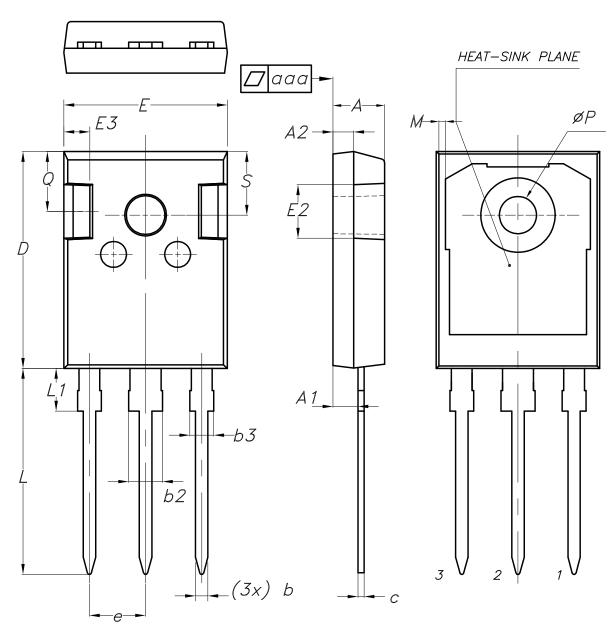


4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline



BACK VIEW

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Table 8. TO-247 long leads package mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
С	c 0.59		0.66
D	20.90 21.00		21.10
Е	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
е	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
Р	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

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Revision history

Table 9. Document revision history

Date	Version	Changes
06-Dec-2017	1	Initial release.
09-Jul-2019	2	Update <i>Table 1, Table 3, Table 4, Table 5, Table 6</i> and <i>Table 7</i> . Added <i>Section 2.1</i> Update <i>Figure 14</i> .
21-Feb-2020	3	The part number STW70N65DM6 have been moved to a separate datasheet and the document has been updated accordingly.
16-Mar-2020	4	Updated Table 7. Source-drain diode.
02-Jul-2020	5	Updated Table 1. Absolute maximum ratings.
03-Nov-2024	6	Updated Section 4.1: TO-247 long leads package information. Minor text changes.

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