



Description

The SQD50P04-13L_T4GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -40V$ $I_D = -40A$

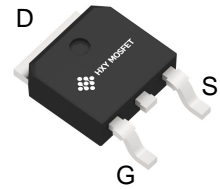
$R_{DS(ON)} < 19\text{ m}\Omega$ @ $V_{GS}=10V$

Application

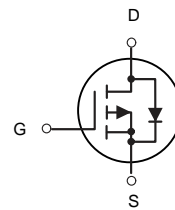
Battery protection

Load switch

Uninterruptible power supply



**TO-252-2L
(TO-252(DPAK))**



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
SQD50P04-13L_T4GE3	TO-252-2L(TO-252(DPAK))	40P04 XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 10V ¹	-40	A
$I_D@T_C=100^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 10V ¹	-22	A
I_{DM}	Pulsed Drain Current ²	-140	A
$P_D@T_C=25^{\circ}\text{C}$	Total Power Dissipation ⁴	40.3	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	66	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	3.1	$^{\circ}\text{C/W}$



Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	-	-	V
Gate-body Leakage current		I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_J=25^{\circ}C$	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$	-	-	-1	μA
	$T_J=100^{\circ}C$			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.5	-2.2	V
Drain-Source On-Resistance ⁴		$R_{DS(on)}$	$V_{GS} = -10V, I_D = -20A$	-	13.5	19	mΩ
			$V_{GS} = -4.5V, I_D = -15A$	-	19.5	25	
Forward Transconductance ⁴		g_{fs}	$V_{DS} = -10V, I_D = -20A$	-	44	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C_{iss}	$V_{DS} = -20V, V_{GS} = 0V, f = 1MHz$	-	2525	-	pF
Output Capacitance		C_{oss}		-	190	-	
Reverse Transfer Capacitance		C_{rss}		-	172	-	
Gate Resistance		R_g	$f = 1MHz$	-	10	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q_g	$V_{GS} = -10V, V_{DS} = -20V, I_D = -20A$	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	5.5	-	
Gate-Drain Charge		Q_{gd}		-	8	-	
Turn-On Delay Time		$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -20V, R_G = 3\Omega, I_D = -20A$	-	14.5	-	ns
Rise Time		t_r		-	20.2	-	
Turn-Off Delay Time		$t_{d(off)}$		-	32	-	
Fall Time		t_f		-	10	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V_{SD}	$I_S = -20A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$T_C=25^{\circ}C$	I_S	-	-	-	-40	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1mH, I_{AS} = -34A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

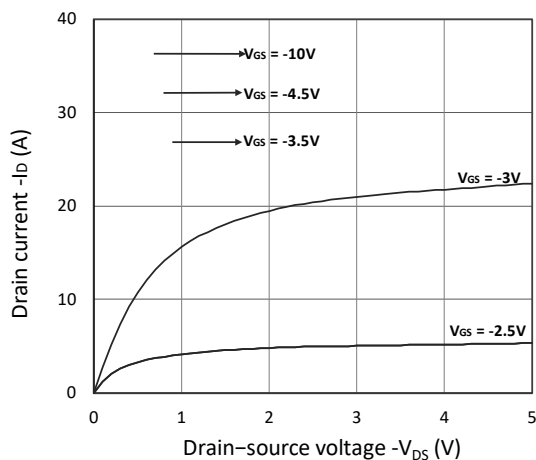


Figure 1. Output Characteristics

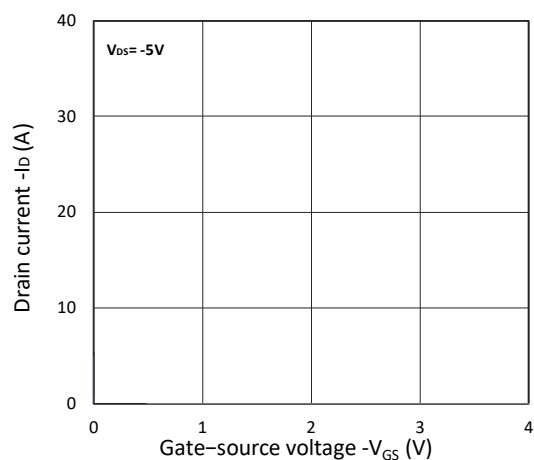


Figure 2. Transfer Characteristics

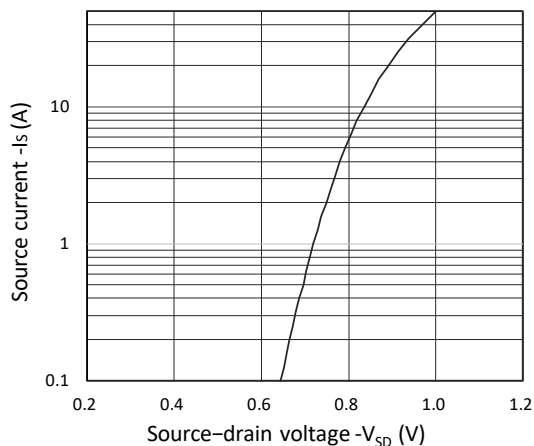


Figure 3. Forward Characteristics of Reverse

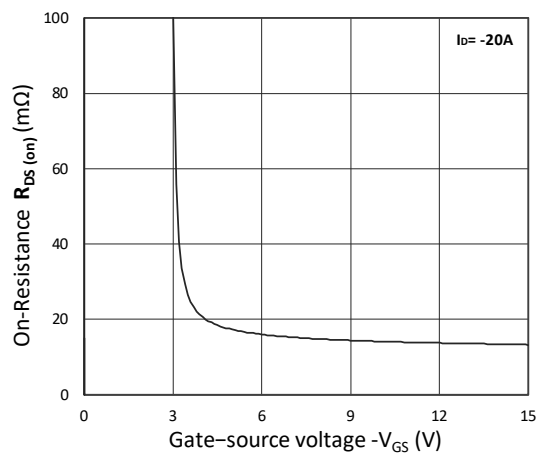


Figure 4. $R_{DS(on)}$ vs. V_{GS}

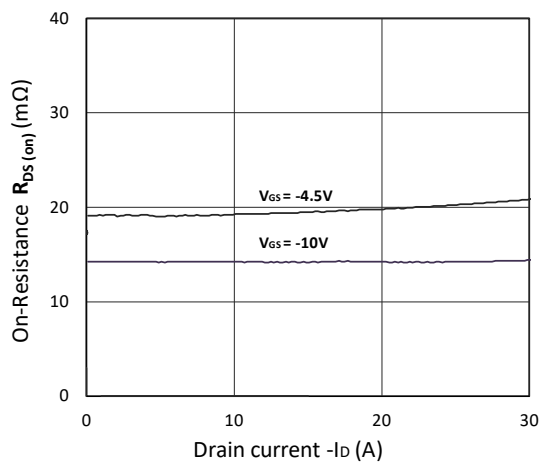


Figure 5. $R_{DS(on)}$ vs. I_D

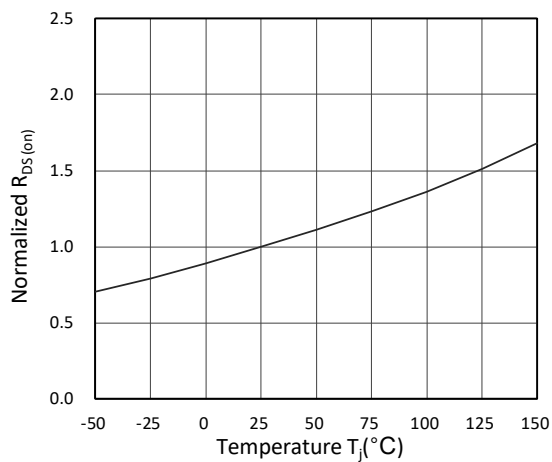


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

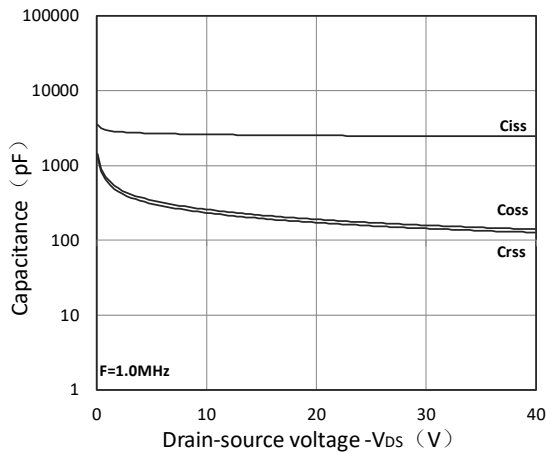


Figure 7. Capacitance Characteristics

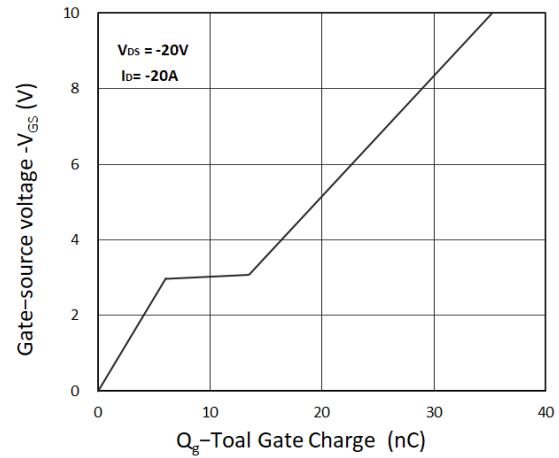


Figure 8. Gate Charge Characteristics

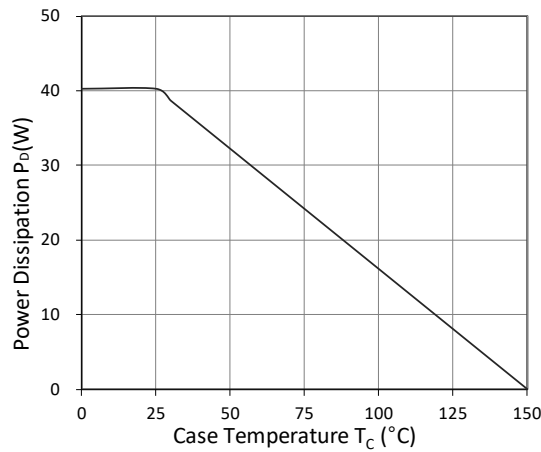


Figure 9. Power Dissipation

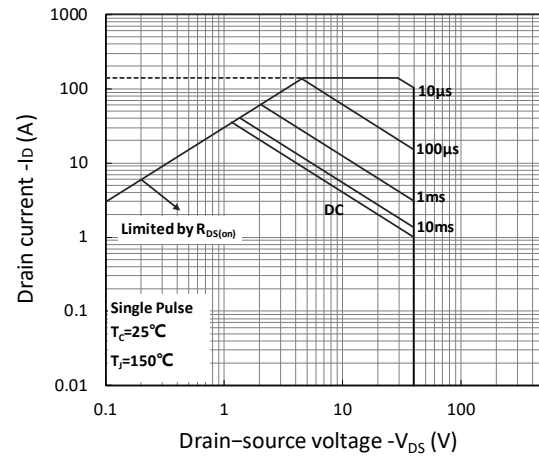


Figure 10. Safe Operating Area

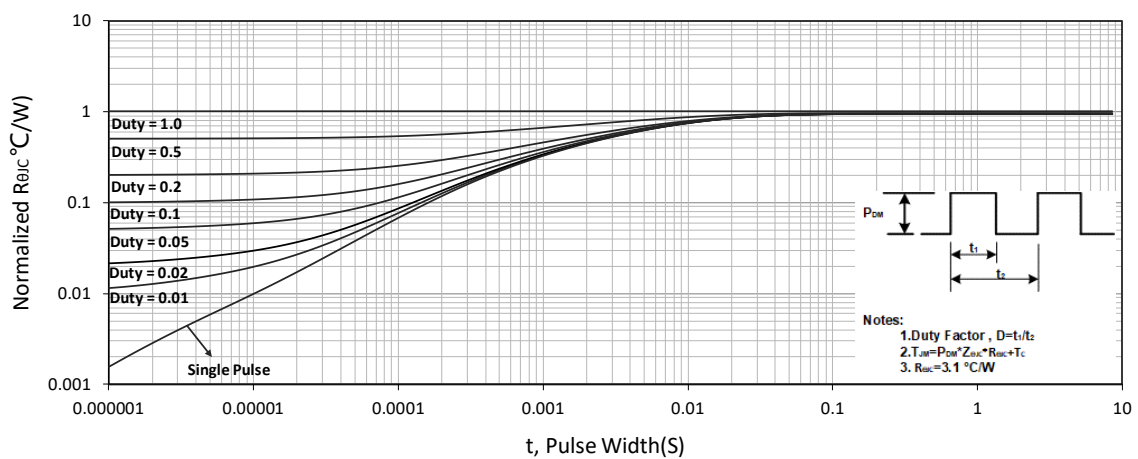


Figure 11. Normalized Maximum Transient Thermal Impedance



Test Circuit

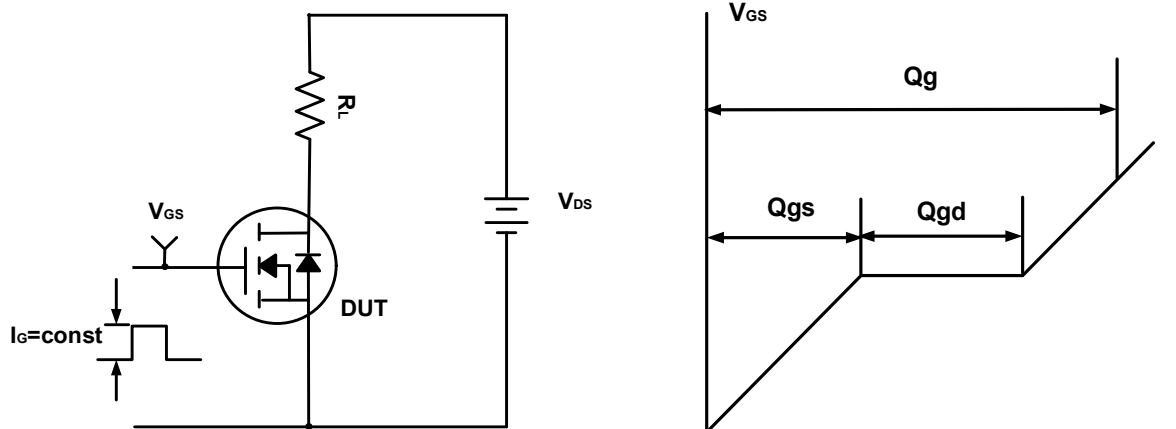


Figure A. Gate Charge Test Circuit & Waveforms

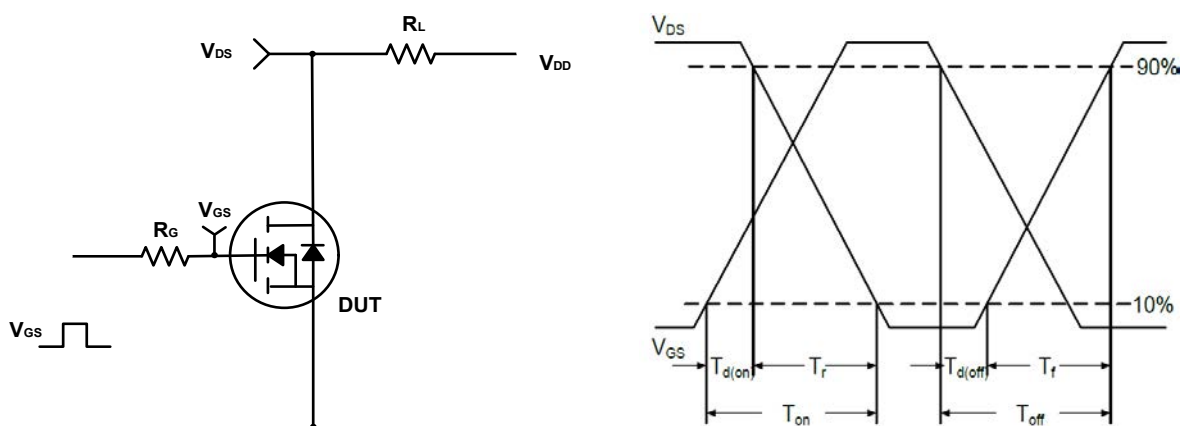


Figure B. Switching Test Circuit & Waveforms

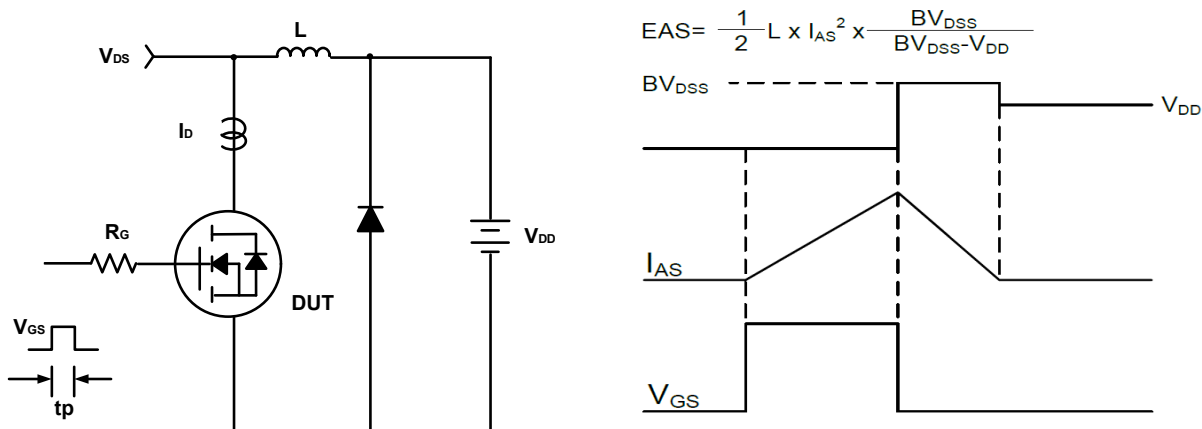


Figure C. Unclamped Inductive Switching Circuit & Waveforms



SQD50P04-13L_T4GE3
P-Channel Enhancement Mode MOSFET

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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