MOSFET

StrongIRFET™ 2 PowerTransistor, 30 V

Features

- Optimized for wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Drain
Pin 2, Tab

Gate
Pin 1

Source
Pin 3

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	2.05	mΩ
I_D	143	A
Q_{oss}	54	nC
Q_G (0V..4.5V)	33	nC
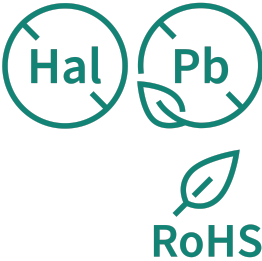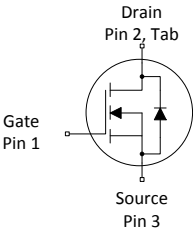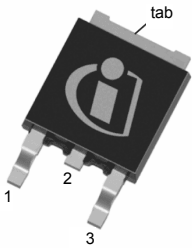
Type/Ordering Code	Package	Marking	Related Links
IPD020N03LF2S	PG-TO252-3	020N03F2	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2   Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	143 110 30	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	572	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	338 676	mJ	I_D=70 A, R_{GS}=25 Ω I_D=35 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	136 3	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1]   Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2]   Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3]   See Diagram 3 for more detailed information

[4]   See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3   Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.1	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5]	R_{thJA}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	75	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4   Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=2 mA
Gate threshold voltage	$V_{GS(th)}$	1.35	1.85	2.35	V	V_{DS}=V_{GS}, I_D=80 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.7 2.0	2.05 2.7	mΩ	V_{GS}=10 V, I_D=70 A V_{GS}=4.5 V, I_D=35 A
Gate resistance	R_G	-	2.2	-	Ω	-
Transconductance [6]	g_{fs}	100	-	-	S	$|V_{DS}|{\geq}2|I_D|R_{DS(on)max}$, I_D=70 A

[6] Defined by design. Not subject to production test.

Table 5   Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4700	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	910	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	235	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	24	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	11	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=70 A, $R_{G,ext}$=1.6 Ω

Table 6   Gate charge characteristics [7]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	15.3	-	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	8.4	-	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	10	-	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	17	-	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V
Gate charge total [8]	Q_g	-	33	50	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V

Table 6   Gate charge characteristics [7]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	$V_{plateau}$	-	3.3	-	V	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 4.5 V
Gate charge total [8]	Q_g	-	69	104	nC	V_{DD}=15 V, I_D=70 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET [8]	$Q_{g(sync)}$	-	29	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge [8]	Q_{oss}	-	54	-	nC	V_{DS}=15 V, V_{GS}=0 V

[7] See "Gate charge waveforms" for parameter definition

[8] Defined by design. Not subject to production test.

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	106	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	572	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.0	V	V_{GS}=0 V, I_F=70 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	21	-	ns	V_R=15 V, I_F=70 A, di_F/dt=500 A/µs
Reverse recovery charge	Q_{rr}	-	71	-	nC	V_R=15 V, I_F=70 A, di_F/dt=500 A/µs

4 Electrical characteristics diagrams

Diagram 1: Power dissipation	Diagram 2: Drain current

P_{tot}=f(T_C)

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Z_{thJC}=f(t_p); parameter: D=t_p/T
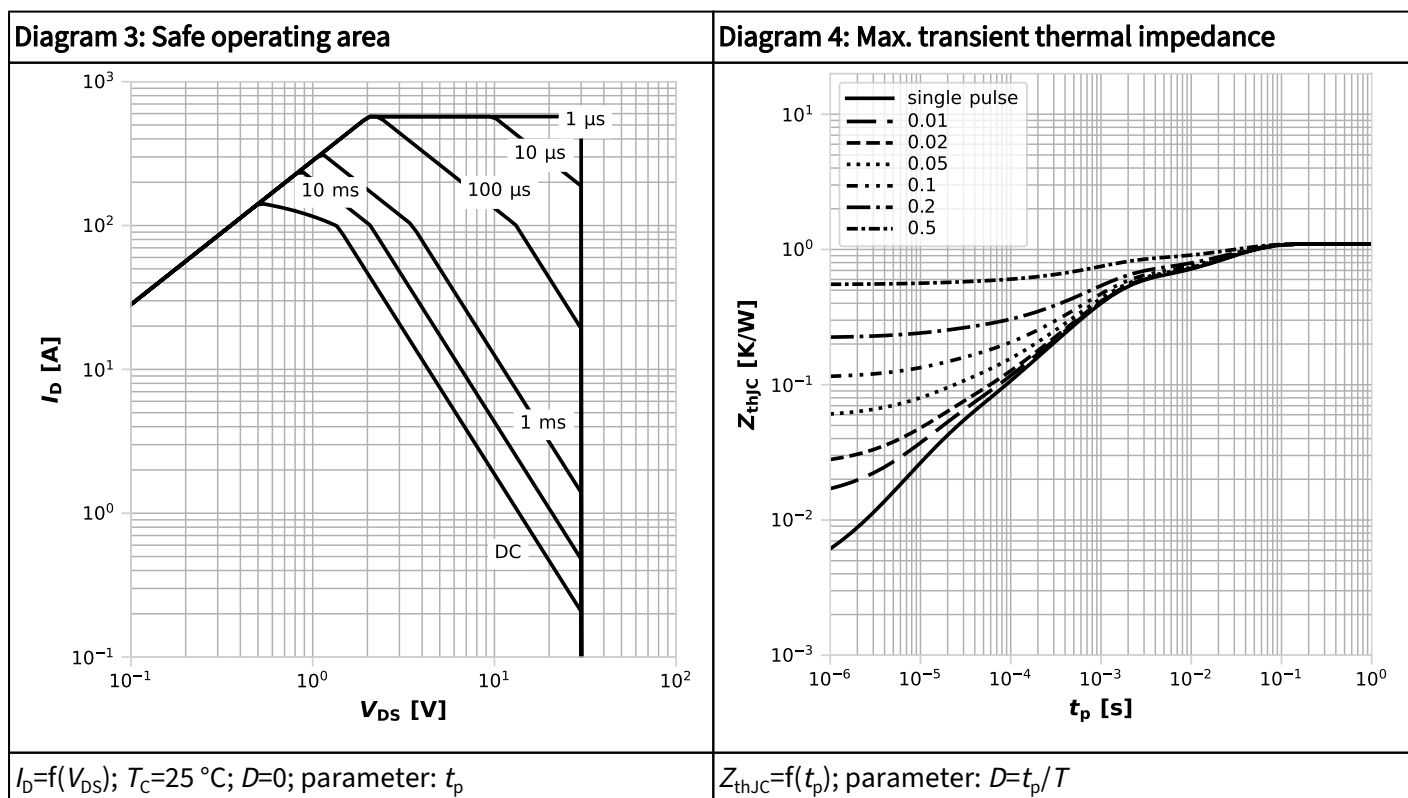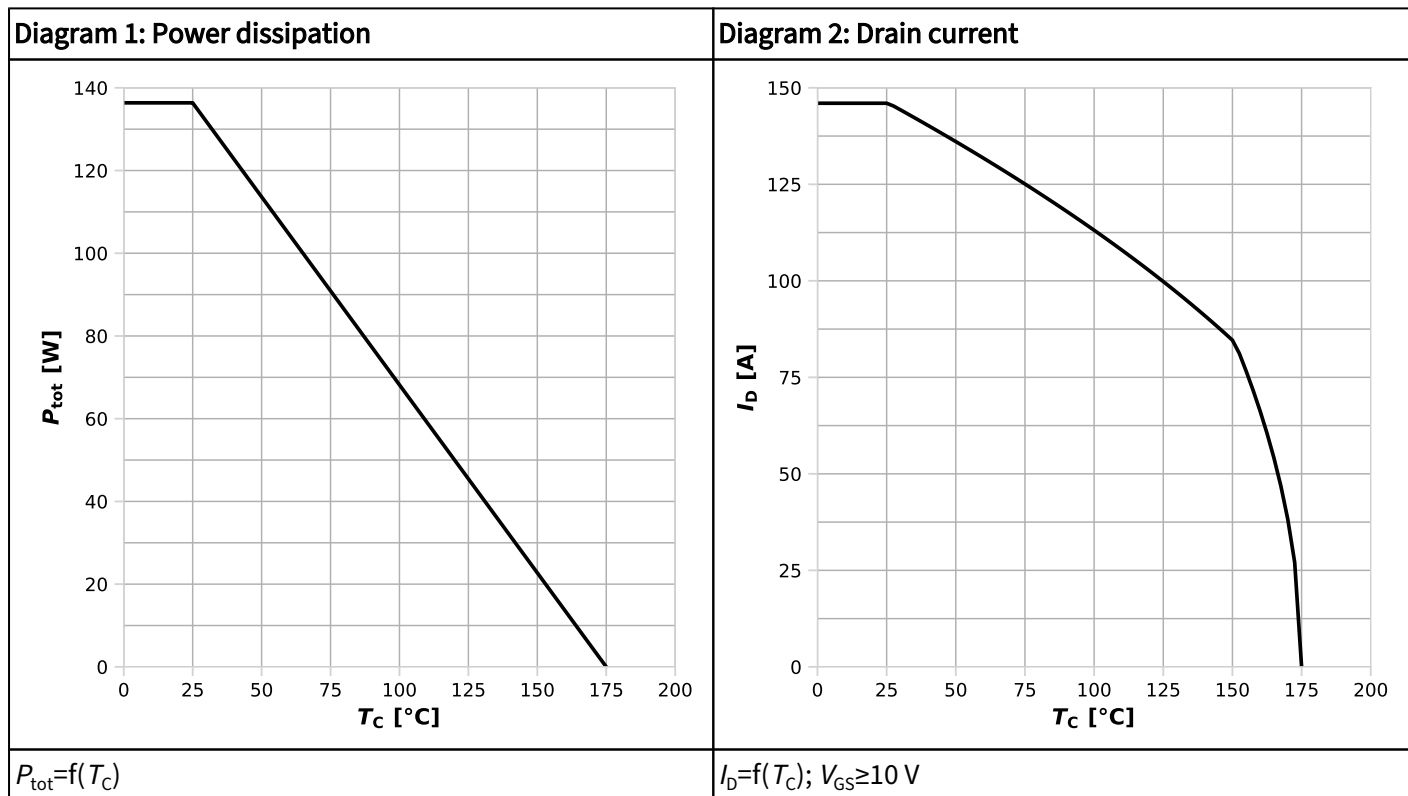
Diagram 5: Typ. output characteristics
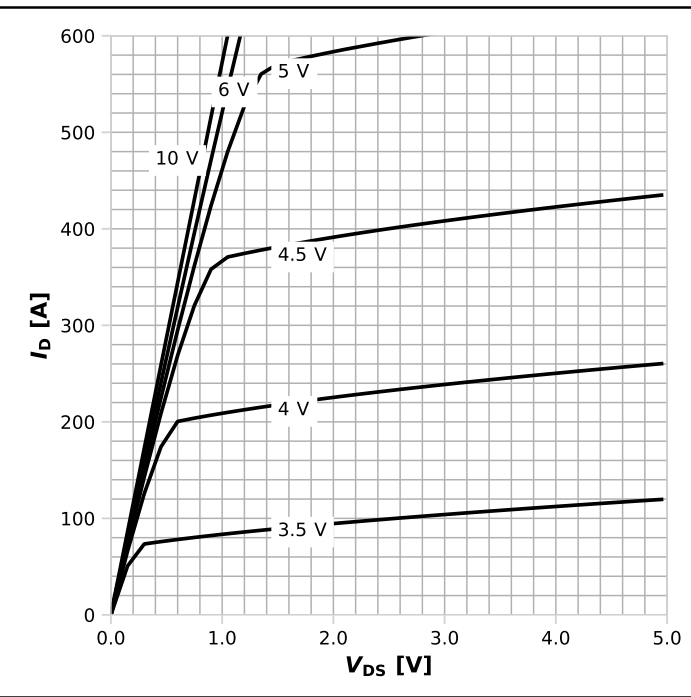
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
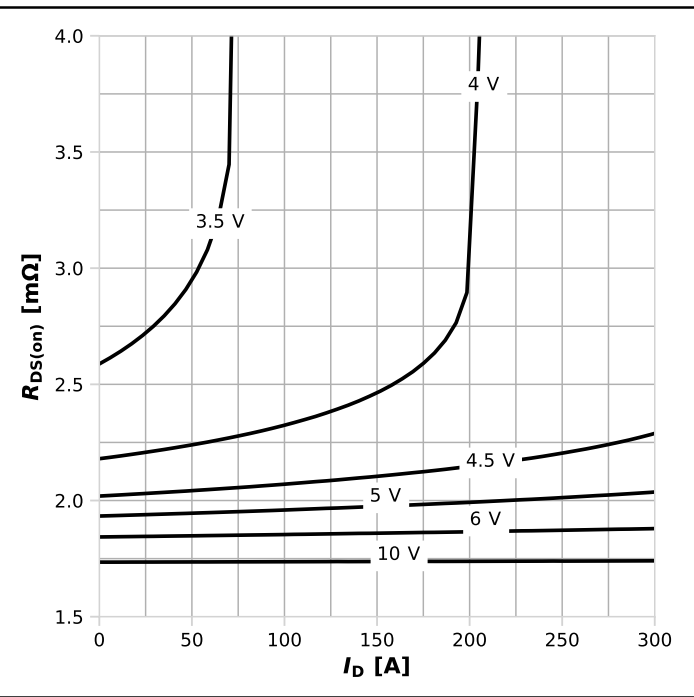
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
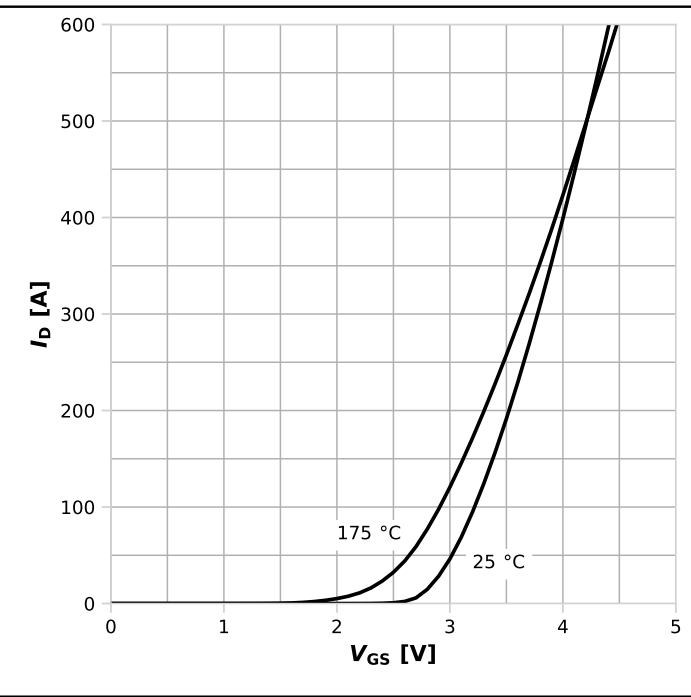
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance
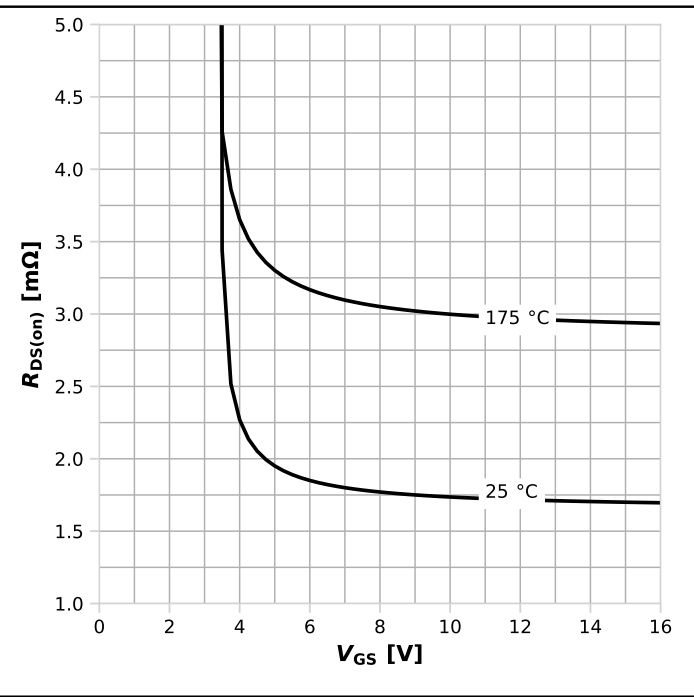
$R_{DS(on)}$=f(V_{GS}), I_D=70 A; parameter: T_j

Infineon

Diagram 9: Normalized drain-source on resistance
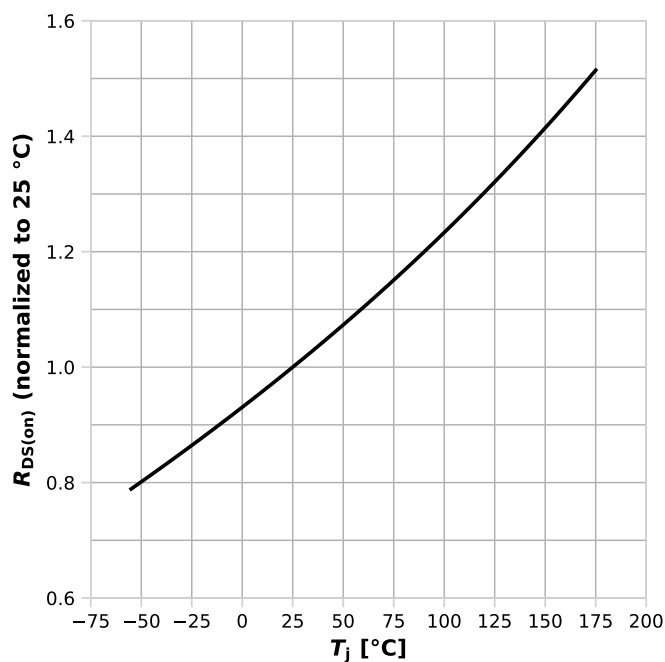
$R_{DS(on)}$=f(T_j), I_D=70 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
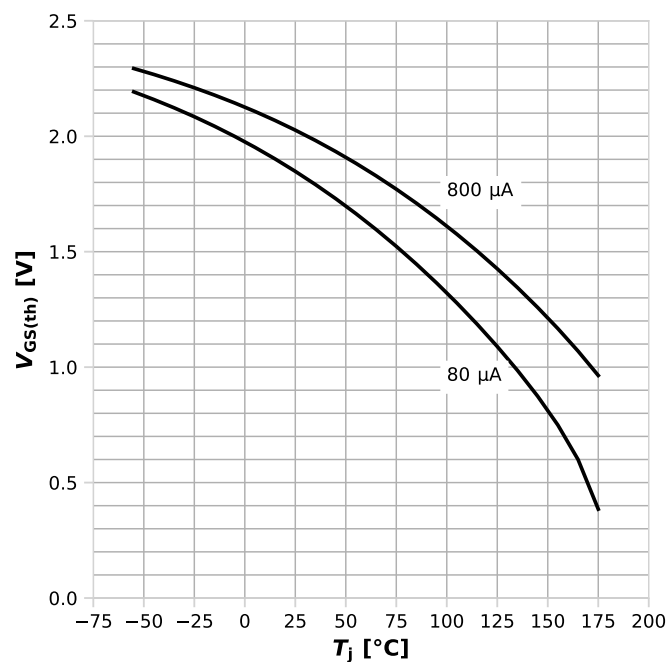
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances
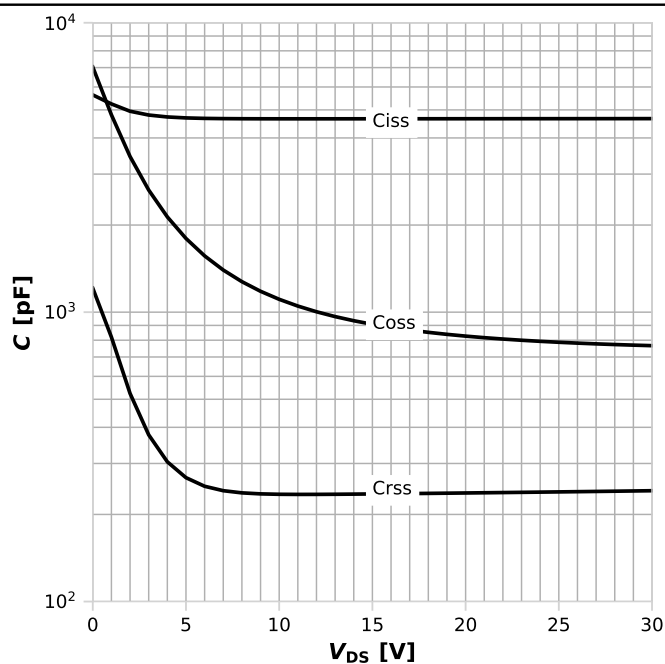
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
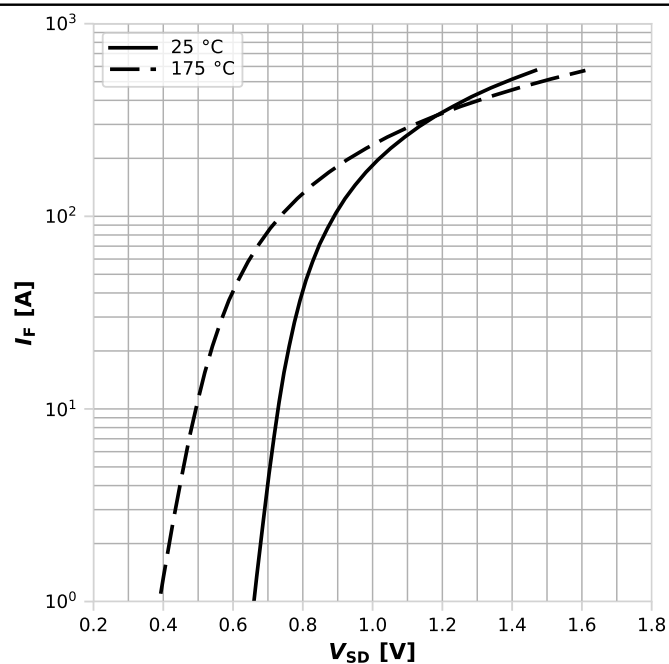
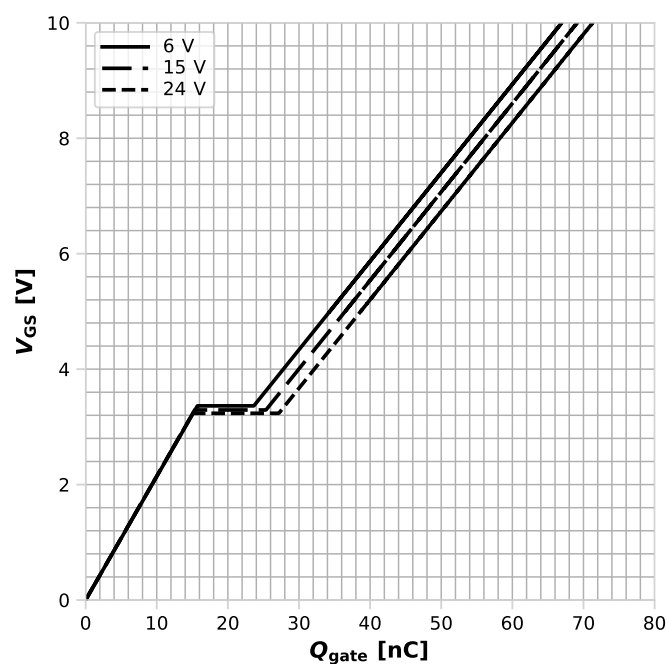I_F=f(V_{SD}); parameter: T_j
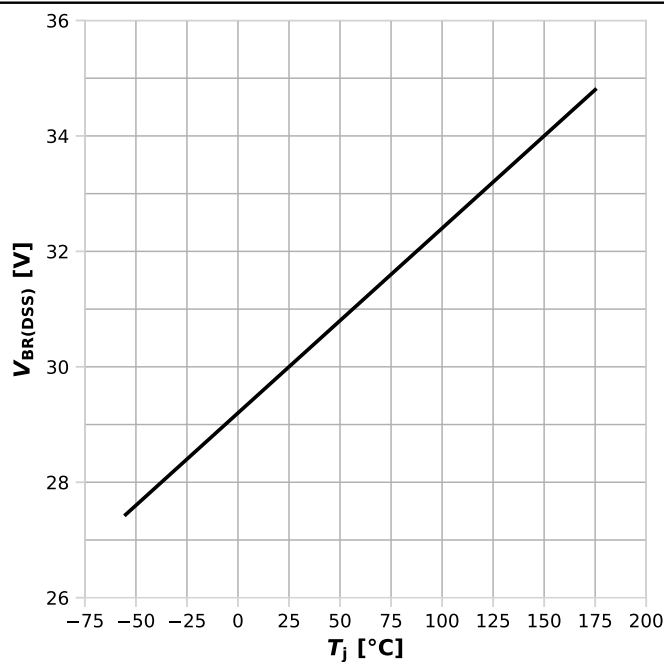
Diagram 13: Avalanche characteristics
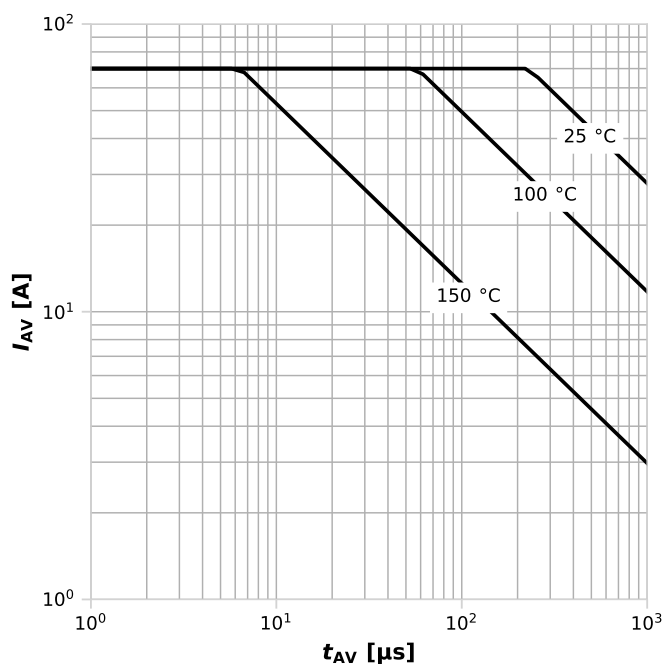
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$
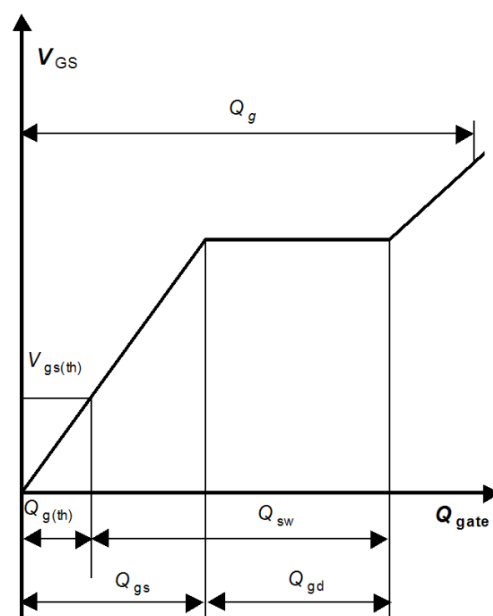
Diagram 14: Typ. gate charge

V_{GS}=f(Q_{gate}), I_D=70 A pulsed, T_j=25 °C; parameter: V_{DD}
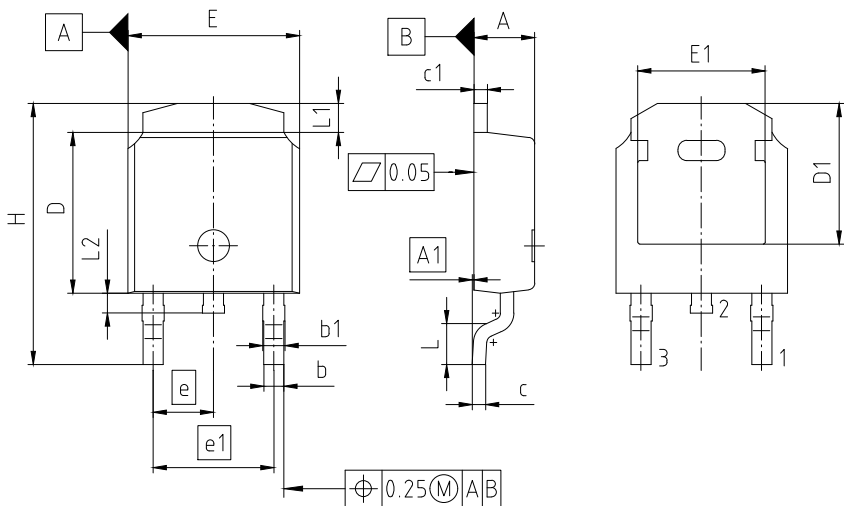
Diagram 15: Drain-source breakdown voltage

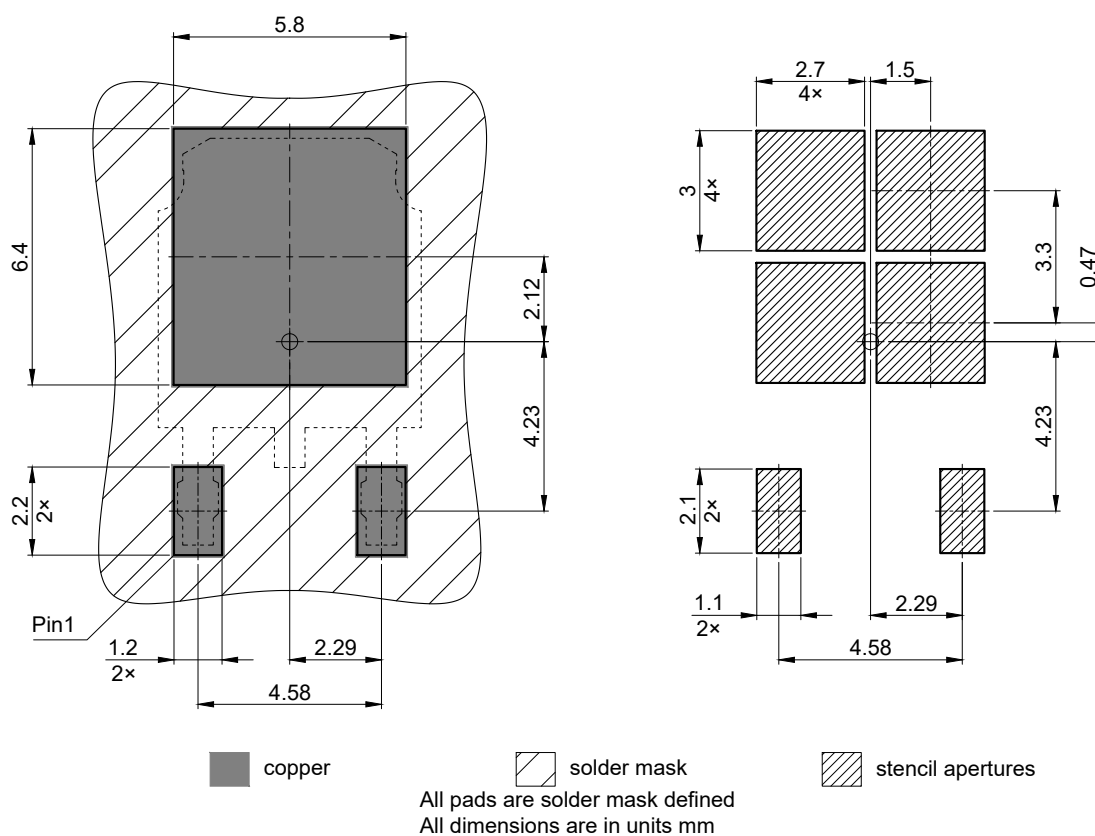$V_{BR(DSS)}$=f(T_j); I_D=2 mA

Gate charge waveforms

-

5   Package Outlines

PACKAGE - GROUP NUMBER:	**PG-TO252-3-U01**	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	2.18	2.39
A1	0.00	0.13
b	0.64	0.89
b1	0.76	1.14
c	0.46	0.61
c1	0.40	0.89
D	5.97	6.22
D1	5.21	---
E	6.35	6.73
E1	4.32	---
e	2.29	
e1	4.58	
N	3	
H	9.40	10.41
L	1.40	1.78
L1	0.89	1.27
L2	0.50	1.02

Figure 1   Outline PG-TO252-3, dimensions in mm

Figure 2   Footprint Drawing PG-TO252-3, dimensions in mm

Revision History

IPD020N03LF2S

Revision 2024-09-20, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-09-20	Release of final

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.