MOSFET

## OptiMOS^{TM} 5 Power-Transistor, 150 V

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Very low reverse recovery charge (Q_{rr})
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Ideal for high-frequency switching and synchronous rectification

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	7.4	mΩ
I_D	114	A
Q_{oss}	116	nC
Q_{rr}	23	nC

TSON-8-3

S 1   8 D
S 2   7 D
S 3   6 D
G 4   5 D
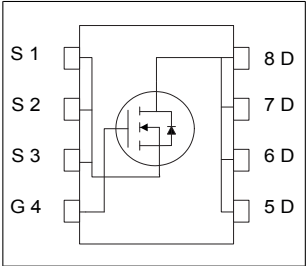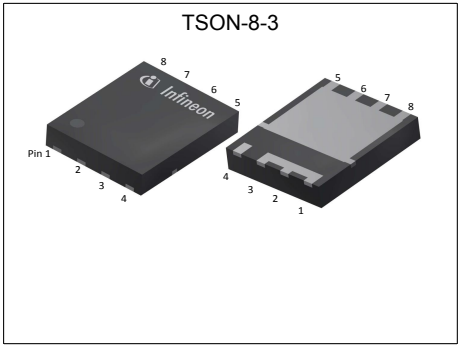
Type / Ordering Code	Package	Marking	Related Links
BSC074N15NS5	TSON-8-3	074N15N	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	114 80	A	V_{GS}=10 V, T_C=25 °C[1] V_{GS}=10 V, T_C=100 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	456	A	T_A=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	210	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	214	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.4	0.7	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm² cooling area[4]	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher Tcase please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	V_{DS}=V_{GS}, I_D=136 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	6.0 6.6	7.4 8.1	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=8 V, I_D=25 A
Gate resistance[1]	R_G	-	1.0	1.5	Ω	-
Transconductance	g_{fs}	41	81	-	S	$\lvert V_{DS}\rvert{\geq}2\lvert I_D\rvert R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	3100	4000	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	770	1000	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	19	33	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	18	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	12	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	9	13	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	14	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	41	52	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	116	154	nC	V_{DS}=75 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See ″Gate charge waveforms″ for parameter definition

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	179	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	456	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	29	58	ns	V_R=75 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	23	46	nC	V_R=75 V, I_F=50 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test.

4   Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot}=f(T_C)

Diagram 2: Drain current

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance

Z_{thJC}=f(t_p); parameter: D=t_p/T
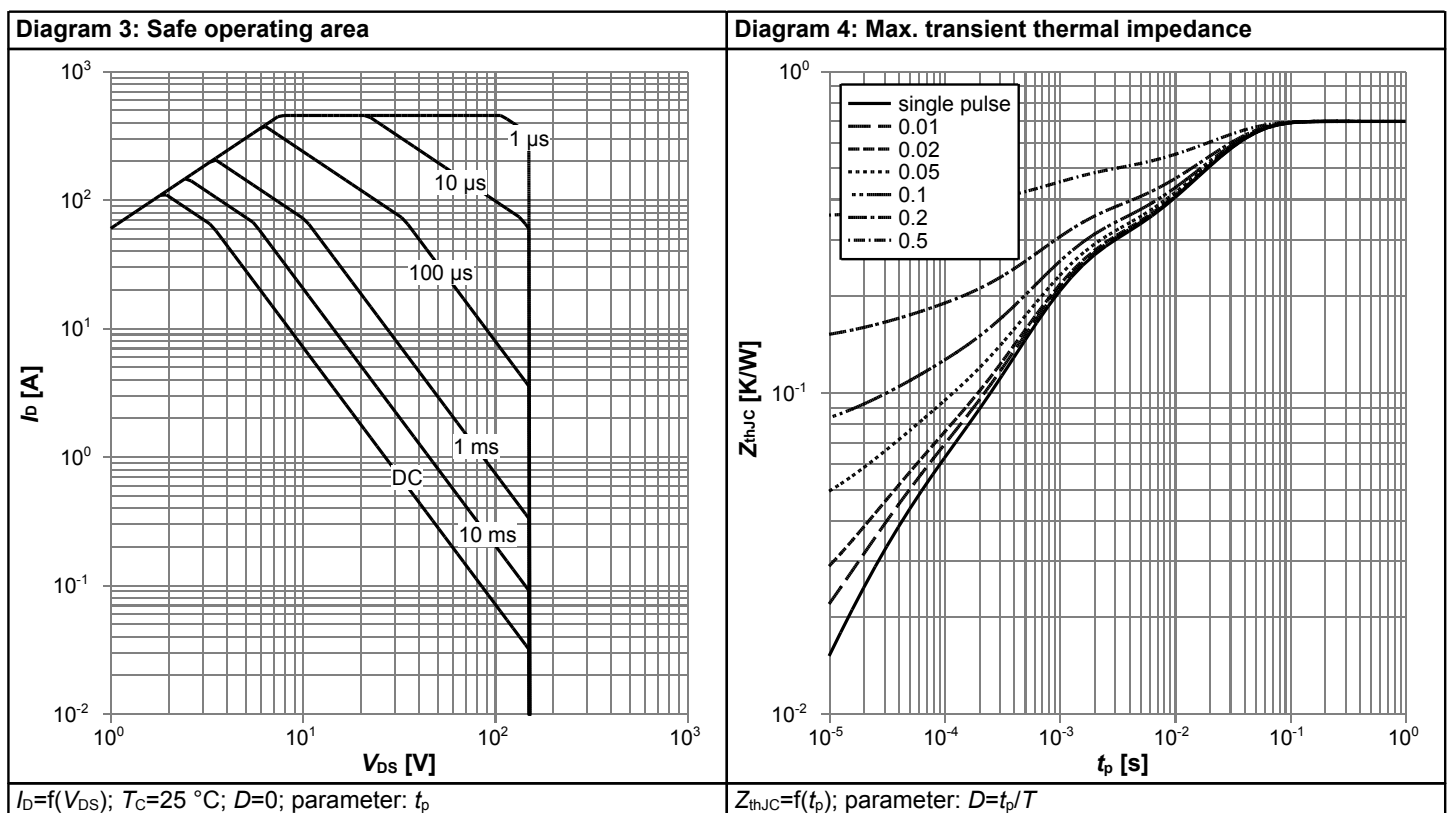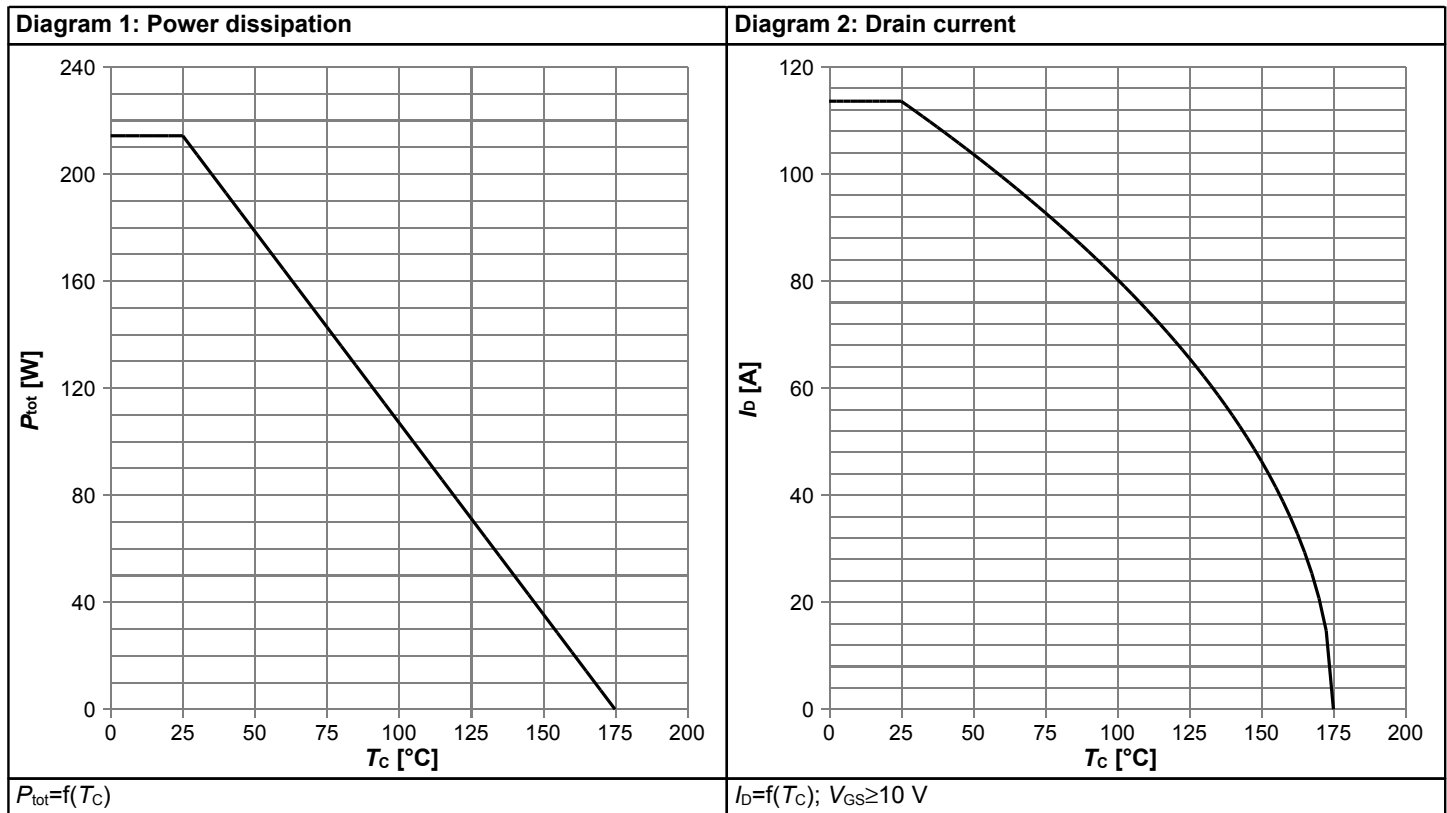
Diagram 5: Typ. output characteristics
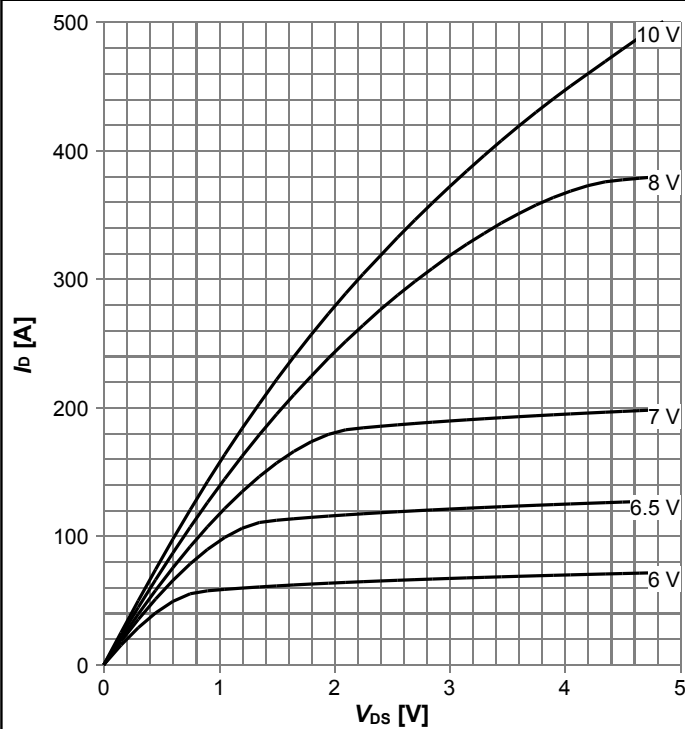
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
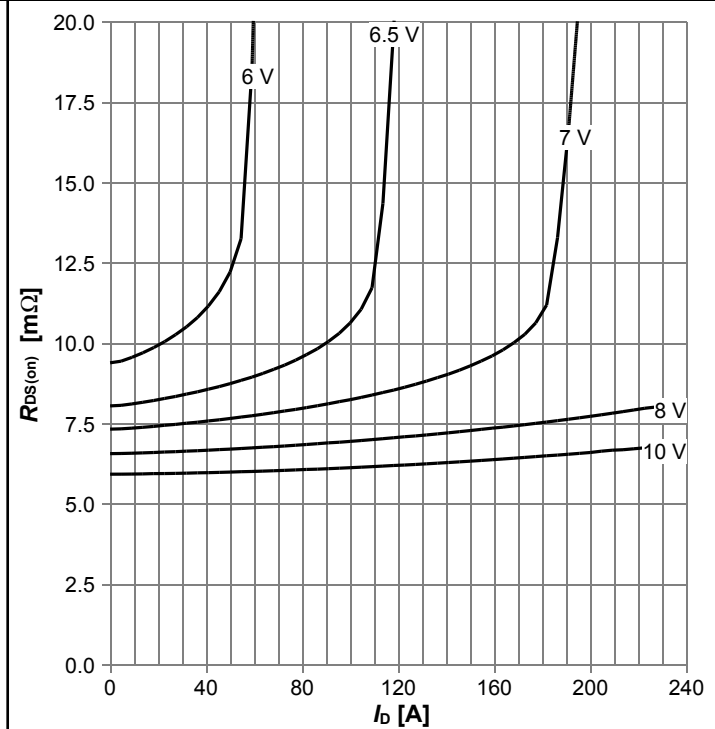
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
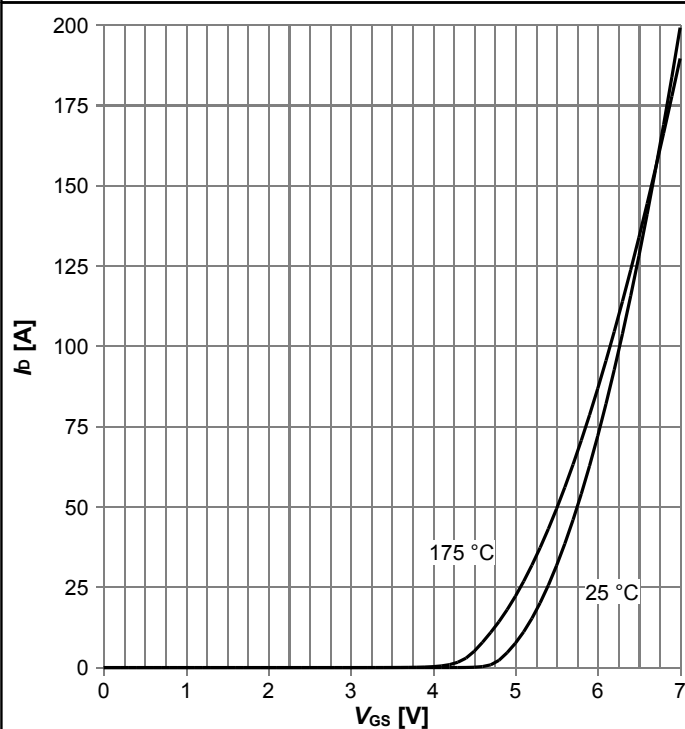
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance
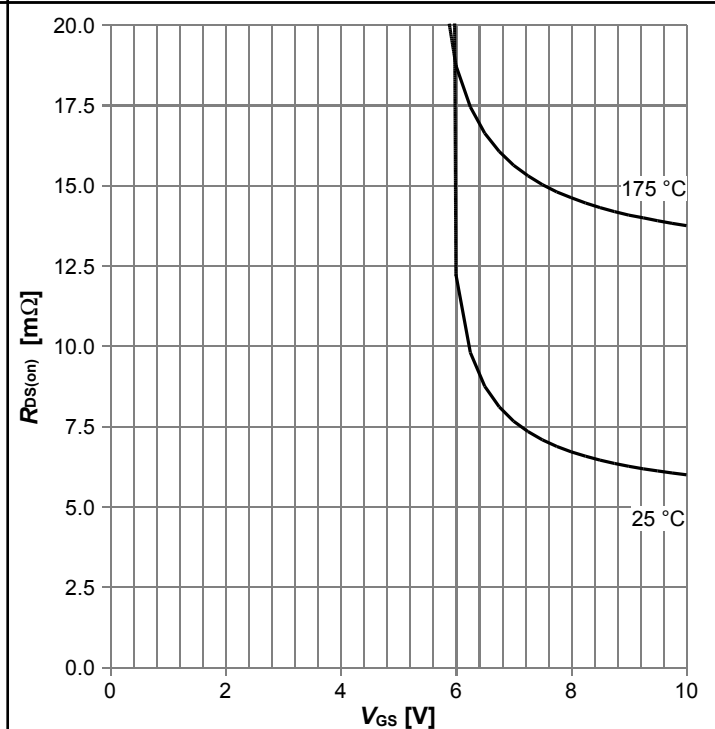
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance
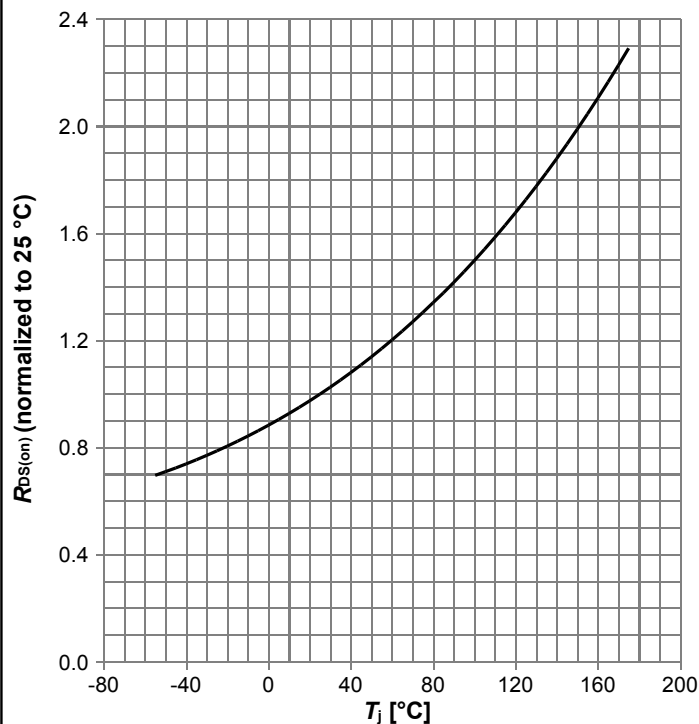
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
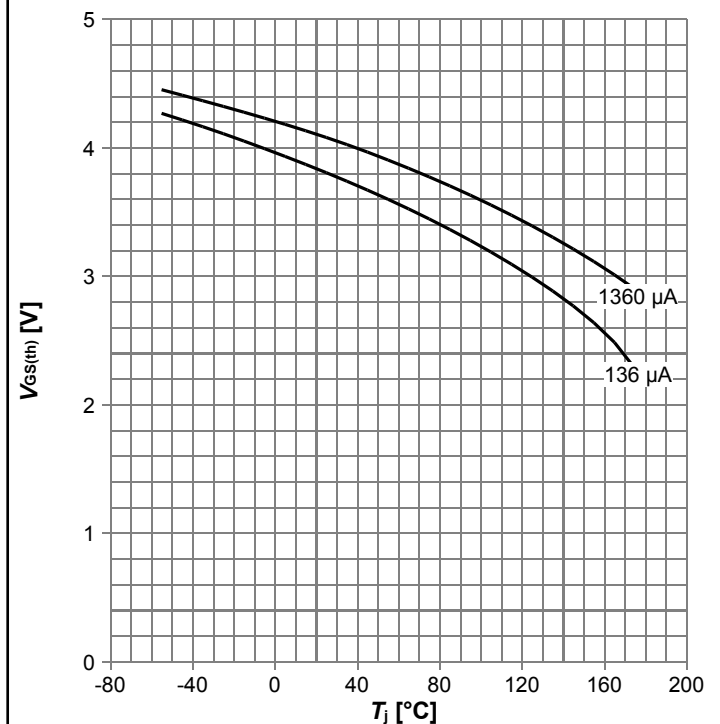
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances
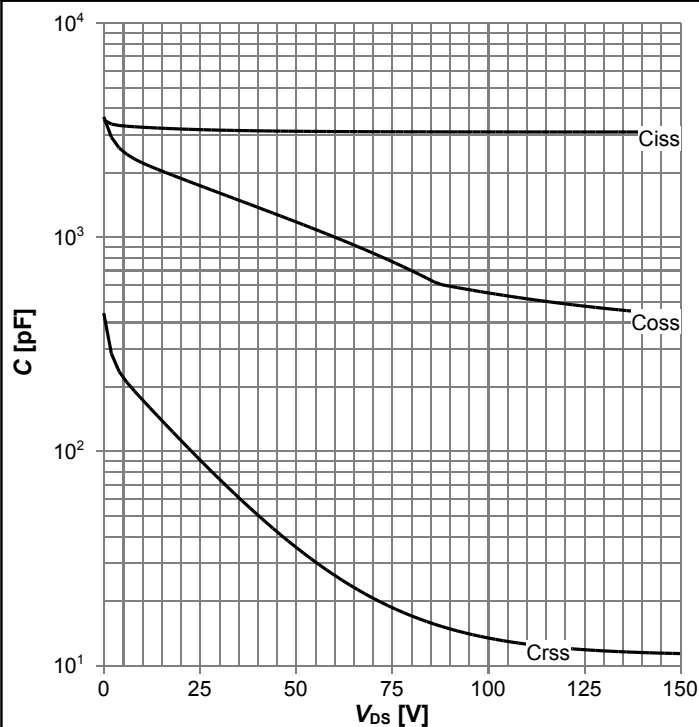
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
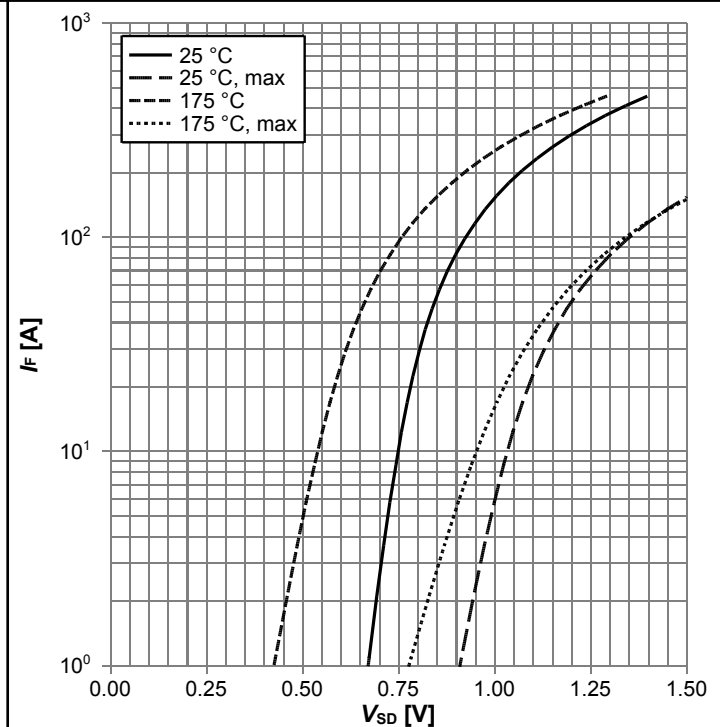
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics
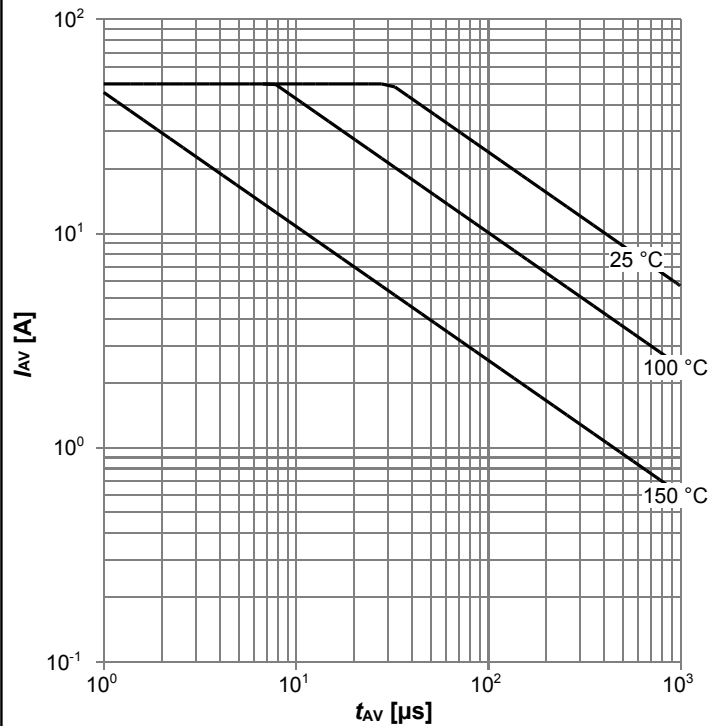
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge
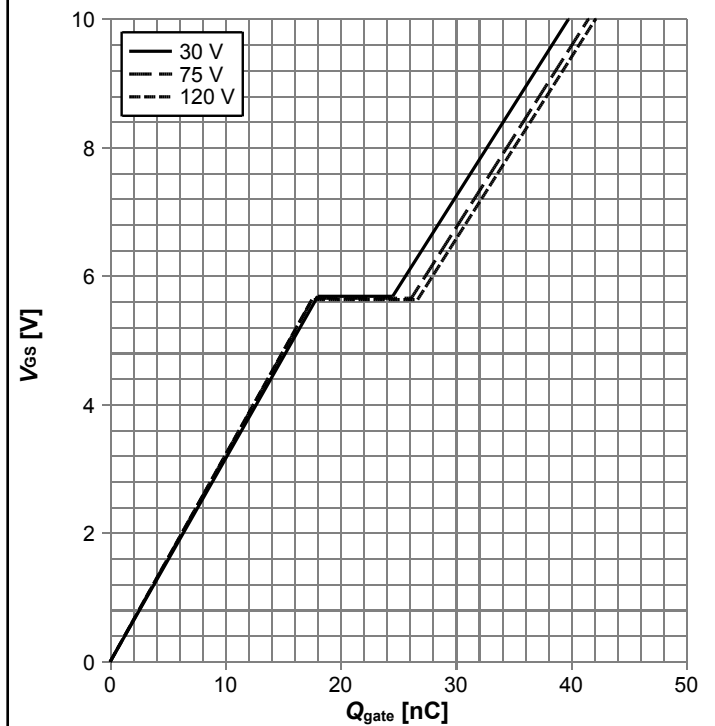
V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage
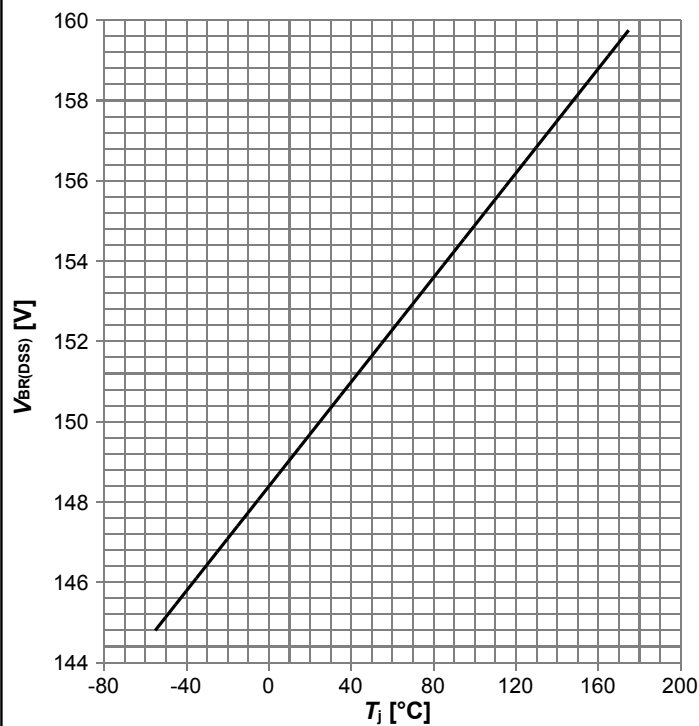
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms
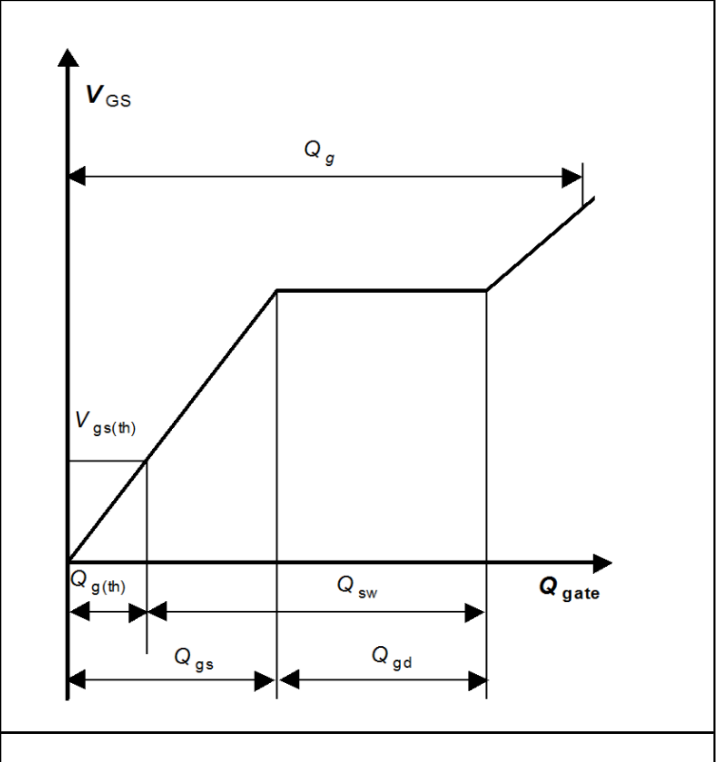
5 Package Outlines
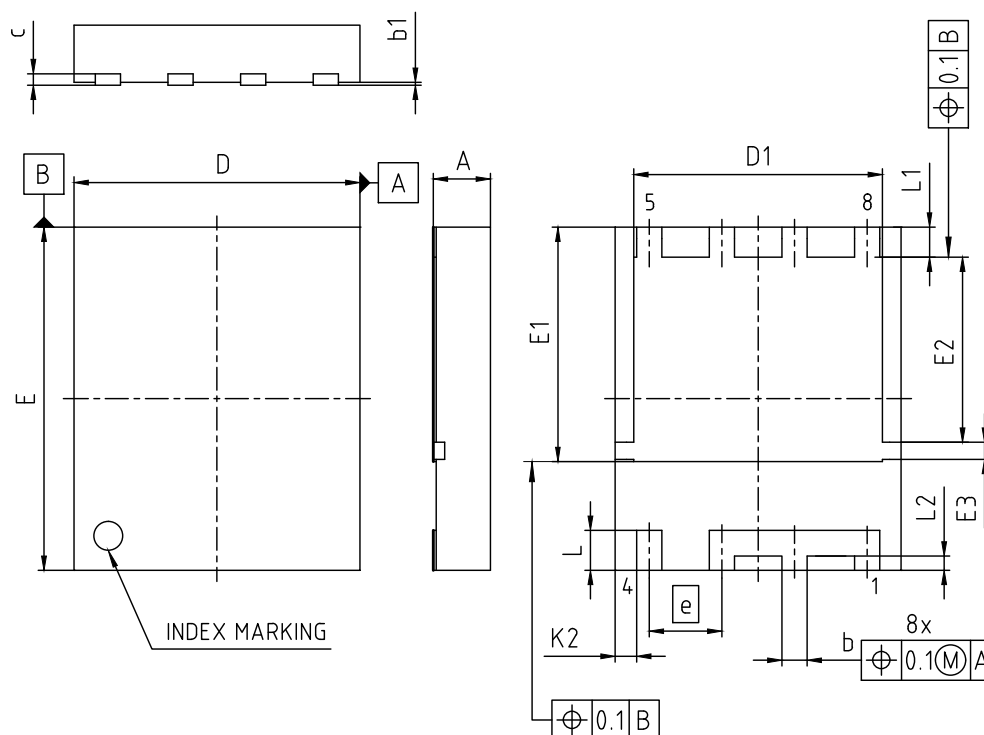
DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	-	1.10
b	0.34	0.54
b1	-	0.05
c	0.20	
D	4.90	5.10
D1	4.25	4.45
E	5.90	6.10
E1	4.00	4.20
E2	3.14	3.34
E3	0.20	0.40
e	1.27	
K2	(0.37)	
L	0.60	0.80
L1	0.43	0.63
L2	(0.25)	

DOCUMENT NO.
Z8B00187559
REVISION
01
SCALE   10:1
0   1   2mm
EUROPEAN PROJECTION
ISSUE DATE
14.12.2017

Figure 1   Outline TSON-8-3, dimensions in mm/inches

Revision History

BSC074N15NS5

Revision: 2019-09-18, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-09-18	Release of final version

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com