

# MOSFET - Power, Single N-Channel, DUAL COOL<sup>®</sup>, DFN8 5x6 40 V, 0.85 mΩ, 313 A

## NTMFSC0D9N04CL

### Features

- Advanced Dual-Sided Cooled Packaging
- Ultra Low  $R_{DS(on)}$  to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Orring FET/Load Switching
- Synchronous Rectifier
- DC-DC Conversion

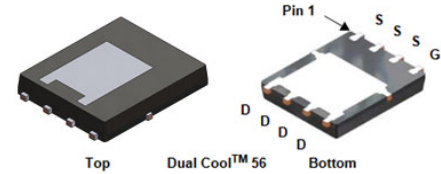
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	40	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	313	A
Power Dissipation R <sub>θJC</sub> (Note 2)			P <sub>D</sub>	167	W
Continuous Drain Current R <sub>θJA</sub> (Note 1, 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	49.5	A
Power Dissipation R <sub>θJA</sub> (Note 1, 2)			P <sub>D</sub>	3.8	W
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	900	A
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	169	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 29 A)			E <sub>AS</sub>	706	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

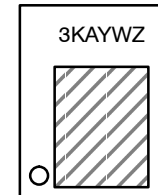
- Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{SSS}$	$R_{SS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.85 mΩ @ 10 V	313 A
	1.3 mΩ @ 4.5 V	



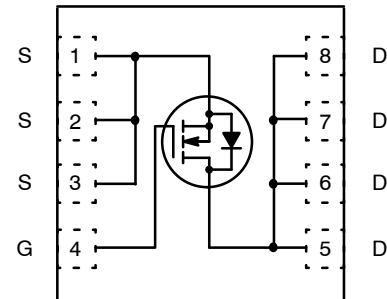
DFN8 5x6  
CASE 506EG

### MARKING DIAGRAM



3K = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
Z = Assembly Lot Code

### N-Channel MOSFET



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case (Bottom) – Steady State (Note 3)	0.9	°C/W
$R_{\theta JC}$	Junction-to-Case (Top) – Steady State (Note 3)	1.4	
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	39	

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		21.2		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate – to – Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

**ON CHARACTERISTICS** (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		-5.8		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.65	0.85	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		1	1.3	
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		1.8		$\Omega$

**CHARGES & CAPACITANCES**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		8500		pF
Output Capacitance	$C_{OSS}$			3400		
Reverse Transfer Capacitance	$C_{RSS}$			110		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}$		61		nC
Total Gate Charge	$Q_{G(TOT)}$			143		
Gate-to-Source Charge	$Q_{GS}$			27		
Gate-to-Drain Charge	$Q_{GD}$			19		
Plateau Voltage	$V_{GP}$			2.7		V

**SWITCHING CHARACTERISTICS** (Note 4)

Turn – On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 32\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		20.2		ns
Rise Time	$t_r$			94.6		
Turn – Off Delay Time	$t_{d(OFF)}$			77.8		
Fall Time	$t_f$			111		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.2	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$			92		ns
Reverse Recovery Charge	$Q_{RR}$				170		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

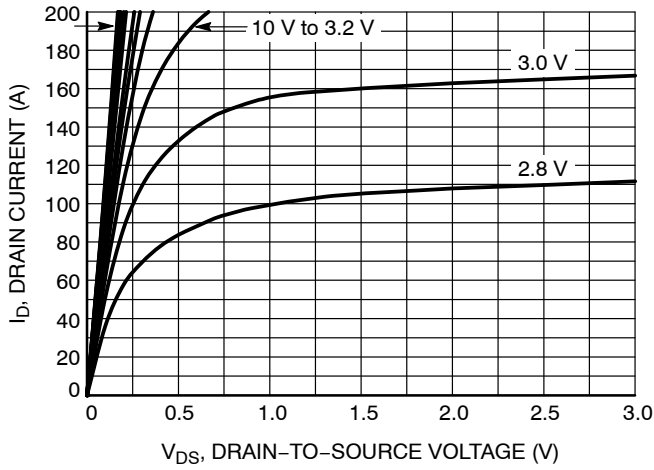


Figure 1. On-Region Characteristics

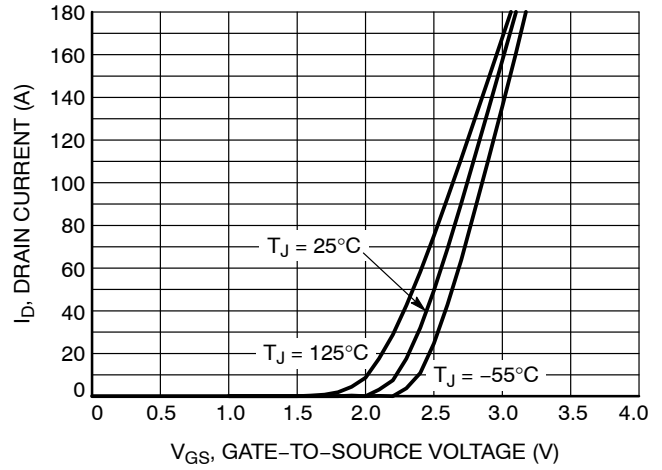


Figure 2. Transfer Characteristics

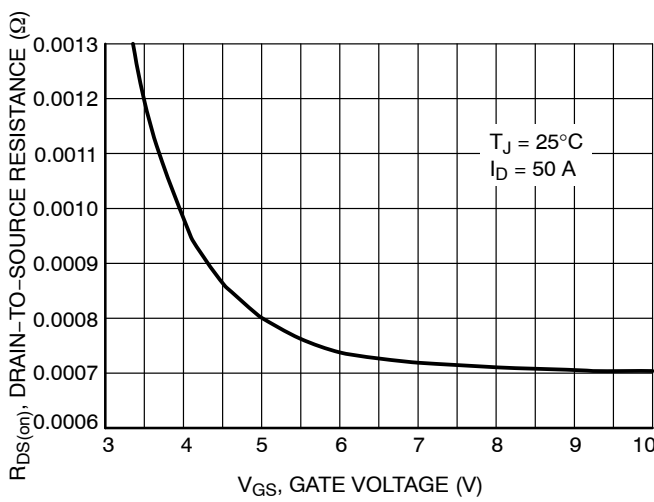


Figure 3. On-Resistance vs. Gate-to-Source Voltage

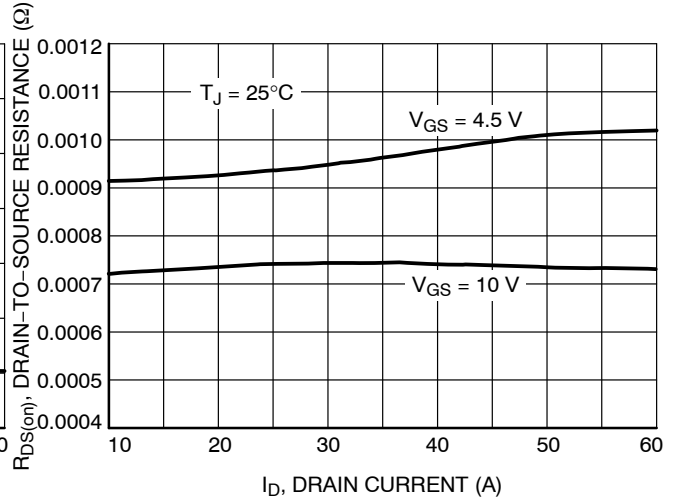


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

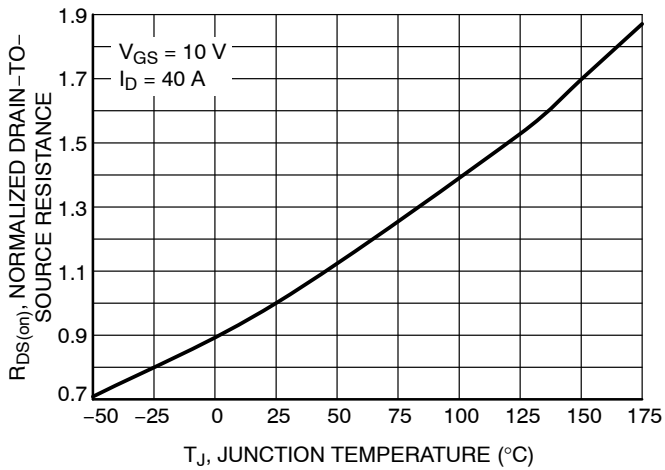


Figure 5. On-Resistance Variation with Temperature

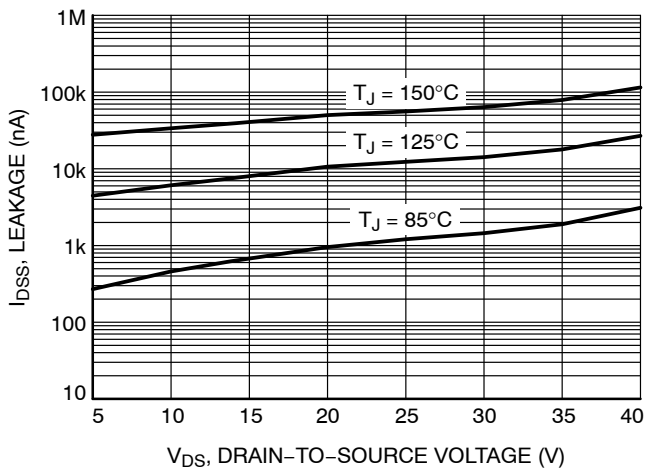


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

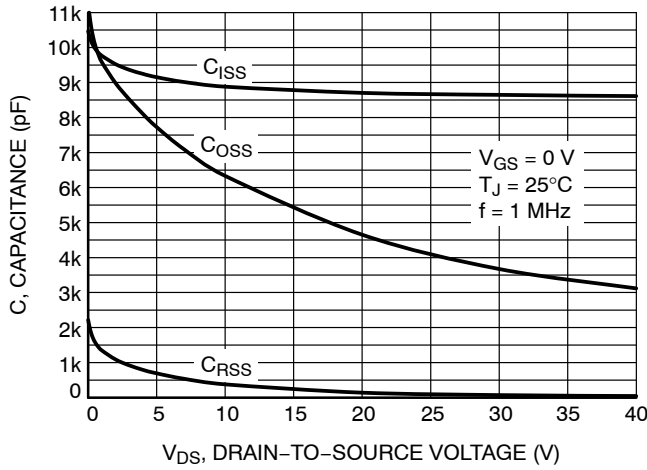


Figure 7. Capacitance Variation

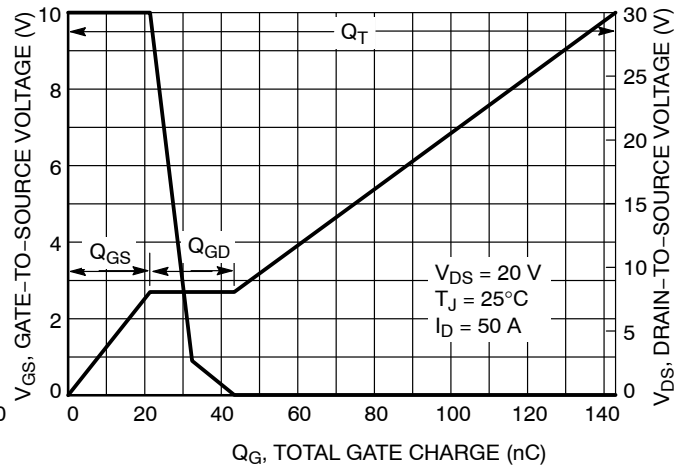


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

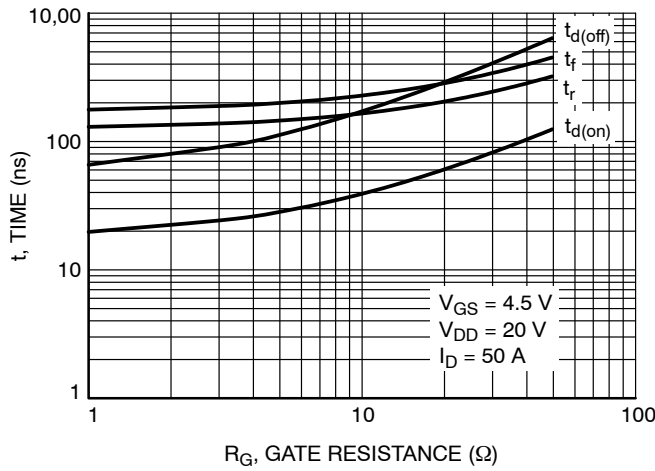


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

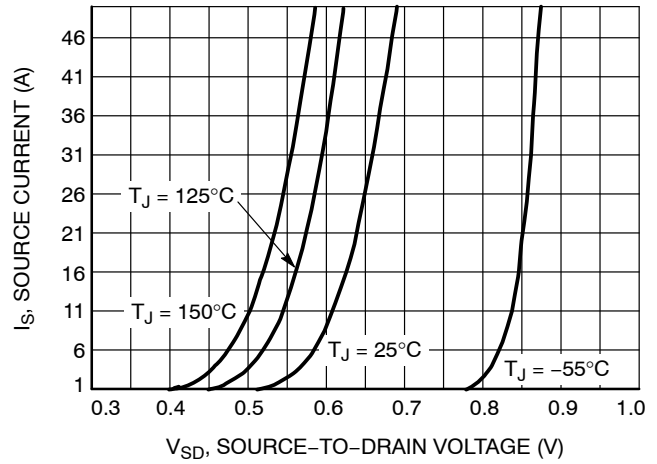


Figure 10. Diode Forward Voltage vs. Current

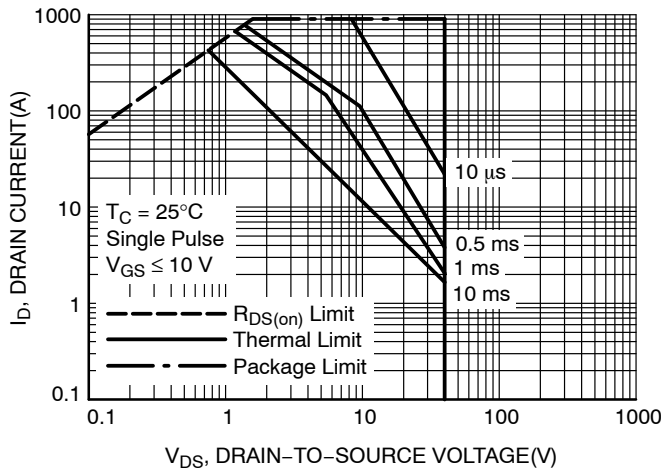


Figure 11. Safe Operating Area

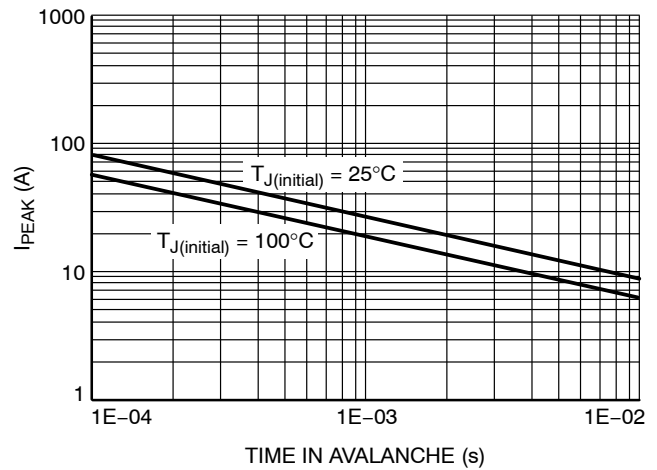


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

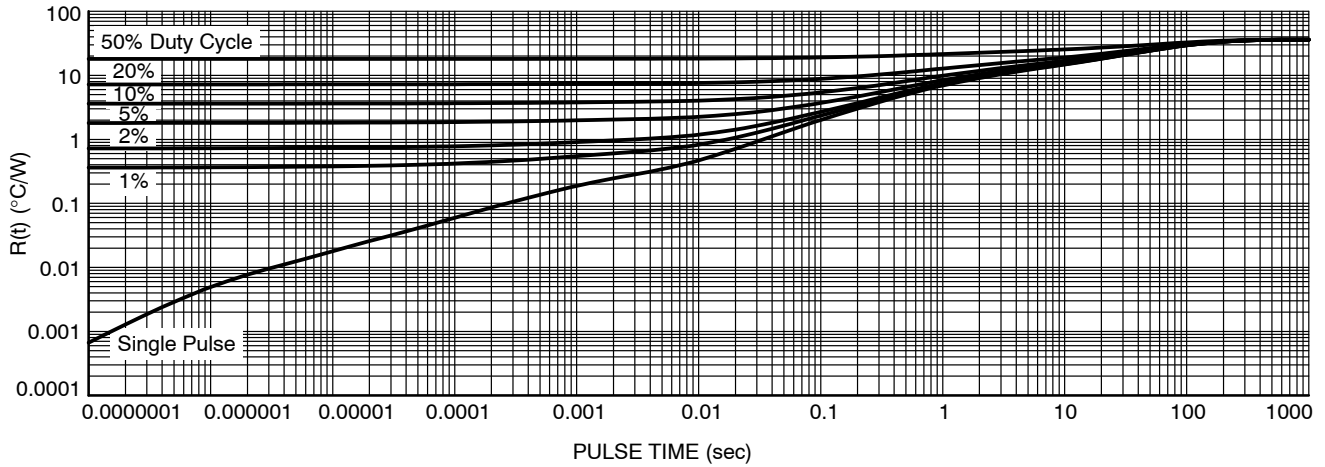


Figure 13. Thermal Characteristics –  $R_{\theta JA}(t)$  ( $^{\circ}\text{C}/\text{W}$ )

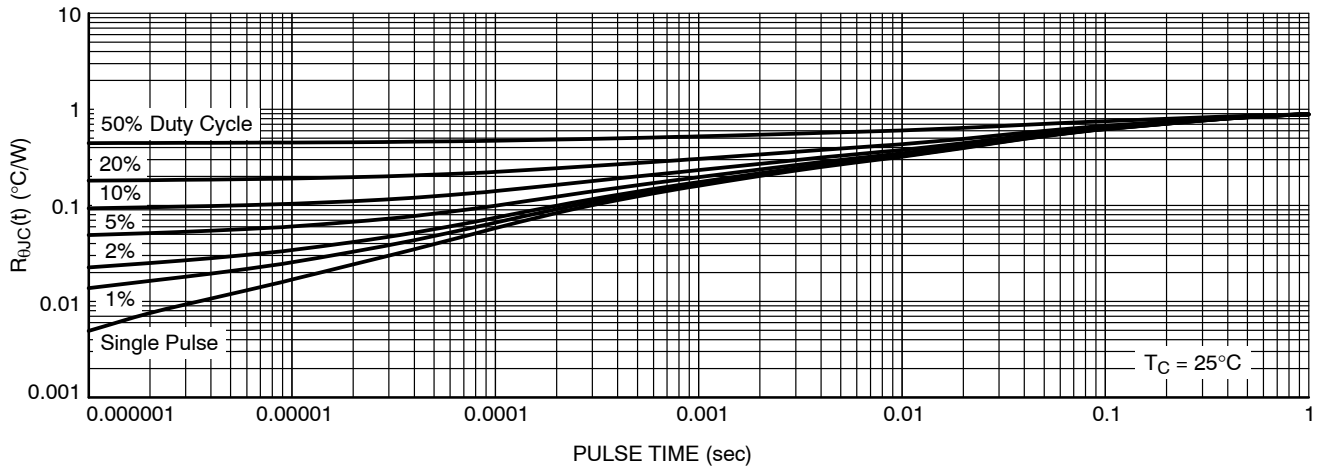


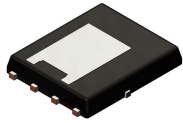
Figure 14. Thermal Characteristics –  $R_{\theta JC}(t)$  ( $^{\circ}\text{C}/\text{W}$ )

### ORDERING INFORMATION

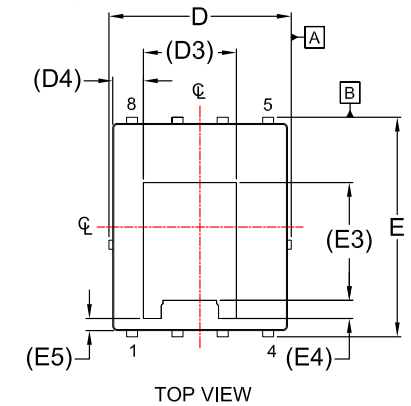
Device	Device Marking	Package	Shipping <sup>†</sup>
NTMFSC0D9N04CL	3K	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

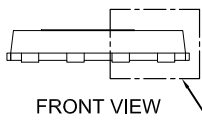
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**DFN8 5x6.15, 1.27P, DUAL COOL**  
**CASE 506EG**  
**ISSUE D**

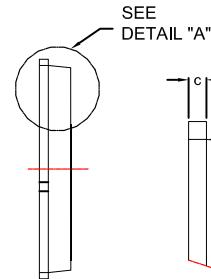
DATE 25 AUG 2020



TOP VIEW



FRONT VIEW

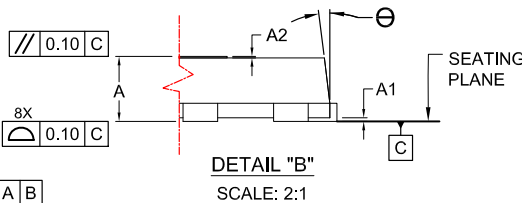
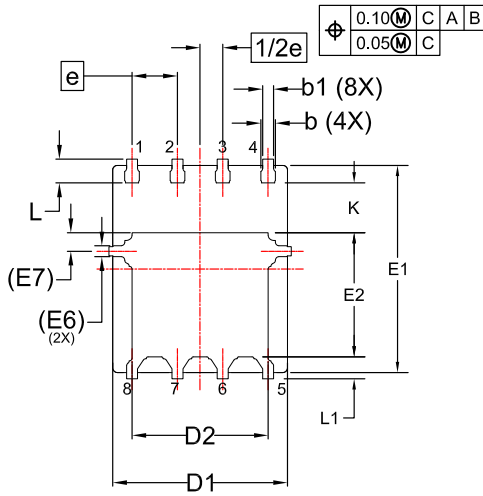


SIDE VIEW

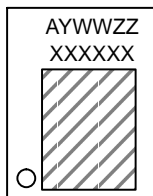
DETAIL "A"  
SCALE: 2:1

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


DETAIL "B"  
SCALE: 2:1


BOTTOM VIEW

**GENERIC**  
**MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

LAND PATTERN  
RECOMMENDATION  
\*FOR ADDITIONAL INFORMATION ON OUR  
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PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>DFN8 5x6.15, 1.27P, DUAL COOL</b>	<b>PAGE 1 OF 1</b>

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