

## **MOSFET**

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor IPx65R110CFD

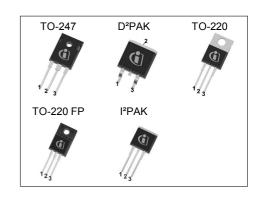
## **Data Sheet**

Rev. 2.6 Final



### 1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler



#### **Features**

- · Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM Rdson\*Qg and Eoss
- · Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- · Pb-free plating, Halogen free mold compound



650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server,Telecom and Solar.



Parameter	Value	Unit
V <sub>DS</sub> @ T <sub>j max</sub>	700	V
RDS(on),max	0.11	Ω
Qg,typ	118	nC
ID,pulse	99.6	A
Eoss @ 400V	9.2	μJ
Body diode di/dt	900	A/µs
Qrr	0.8	μC
trr	150	ns
Irrm	8.3	A

	drain pin 2
gate_ pin 1	
	source pin 3







Type / Ordering Code	Package	Marking	Related Links			
IPW65R110CFD	PG-TO 247					
IPB65R110CFD	PG-TO 263					
IPP65R110CFD	PG-TO 220	65F6110	see Appendix A			
IPA65R110CFD	PG-TO 220 FullPAK					
IPI65R110CFD	PG-TO 262					

Final Data Sheet 2 Rev. 2.6, 2011-09-26



### **Table of Contents**

Description	. 2
Table of Contents	. 3
Maximum ratings	. 4
Thermal characteristics	. 5
Electrical characteristics	. 6
Electrical characteristics diagrams	. 8
Test Circuits	13
Package Outlines	14
Appendix A	19
Revision History	20
Disclaimer	20



## **2 Maximum ratings** at $T_j = 25$ °C, unless otherwise specified

Table 2 **Maximum ratings** 

Parameter	0	Values			11:4		
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Continuous drain current1)	/ <sub>D</sub>			31.2	Α	<i>T</i> <sub>C</sub> = 25°C	
				19.7		T <sub>C</sub> = 100°C	
Pulsed drain current <sup>2)</sup>	/ <sub>D,pulse</sub>			99.6	А	<i>T</i> <sub>C</sub> = 25°C	
Avalanche energy, single pulse	<i>E</i> <sub>AS</sub>			845	mJ	<i>l</i> <sub>D</sub> = 6.2A, <i>V</i> <sub>DD</sub> = 50V	
Avalanche energy, repetitive	<i>E</i> <sub>AR</sub>			1.30	mJ	$I_D = 6.2A, \ V_{DD} = 50V$	
Avalanche current, repetitive	/ <sub>AR</sub>			6.2	Α		
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	V <sub>DS</sub> = 0 400V	
Gate source voltage	V <sub>GS</sub>	-20		20	V	static	
		-30		30		AC (f > 1 Hz)	
Power dissipation (non FullPAK) TO-247, TO-220, l²PAK	P <sub>tot</sub>			277.8	W	<i>T</i> <sub>C</sub> = 25°C	
Power dissipation (FullPAK) TO-220 FP	P <sub>tot</sub>			34.7	W	<i>T</i> <sub>C</sub> = 25°C	
Operating and storage temperature	$T_{\rm j}, T_{\rm stg}$	-55		150	°C		
Mounting torque (non FullPAK) TO-247, TO-220, I <sup>2</sup> PAK				60	Ncm	M3 and M3.5 screws	
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws	
Continuous diode forward current	/s			31.2	Α	<i>T</i> <sub>C</sub> = 25°C	
Diode pulse current	/S,pulse			99.6	А	<i>T</i> <sub>C</sub> = 25°C	
Reverse diode dv/dt <sup>3)</sup>	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400 \text{V}, \ k_{SD} \le k_{D},$	
Maximum diode commutation speed	di <sub>f</sub> /dt			900	A/µs	$T_{\rm j}$ = 25°C	

Final Data Sheet Rev. 2.6, 2011-09-26

 $<sup>^{1)}</sup>$  Limited by T<sub>j max</sub>. Maximum  $^{2)}$  Pulse width t<sub>p</sub> limited by T<sub>j max</sub>  $^{3)}$  V<sub>peak</sub><V<sub>(BR)DSS</sub>, T<sub>j</sub><T<sub>j max</sub>, identical low side and high side switch with same Rg



### 3 Thermal characteristics

Table 3 Thermal characteristics TO-247, TO-220, I<sup>2</sup>PAK

Parameter	Cumbal	Values			11:4	Note / Took Condition
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Thermal resistance, junction - case	<i>R</i> thJC			0.45	°C/W	
Thermal resistance, junction - ambient	$R_{thJA}$			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	$\mathcal{T}_{sold}$			260	°C	1.6 mm (0.063 in.) from case for 10s

### Table 4 Thermal characteristics TO-220 FP

Parameter	Cumbal	Values			11	Note / Test Condition
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Thermal resistance, junction - case	<i>R</i> thJC			3.6	°C/W	
Thermal resistance, junction - ambient	$R_{thJA}$			80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	$\mathcal{T}_{sold}$			260	°C	1.6 mm (0.063 in.) from case for 10s

#### Table 5 Thermal characteristics D<sup>2</sup>PAK

Dougraphou	C. mah al	Values			11	Note / Test Condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Thermal resistance, junction - case	RthJC			0.45	°C/W	
Thermal resistance, junction - ambient <sup>1)</sup>	$R_{thJA}$			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wave- & reflowsoldering allowed	$\mathcal{T}_{sold}$			260	°C	reflow MSL

Final Data Sheet 5 Rev. 2.6, 2011-09-26

<sup>&</sup>lt;sup>1)</sup> Device on 40mm\*40mm\*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70μm) for drain connection. PCB is vertical without air stream cooling.



### **Electrical characteristics**

at  $T_j = 25$ °C, unless otherwise specified

Table 6 Static characteristics

Parameter	0	Values			l	
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Drain-source breakdown voltage	V(BR)DSS	650			V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Gate threshold voltage	VGS(th)	3.5	4	4.5	V	$V_{DS} = V_{GS}$ , $I_D = 1.3 \text{mA}$
Zero gate voltage drain current	/ <sub>DSS</sub>			1.5	μΑ	$V_{DS} = 650V$ , $V_{GS} = 0V$ , $T_j = 25^{\circ}C$
			400			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150°C$
Gate-source leakage current	/ <sub>GSS</sub>			100	nA	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0V
Drain-source on-state resistance	R <sub>DS(on)</sub>		0.099	0.11	Ω	$V_{GS} = 10V$ , $I_D = 12.7A$ , $T_j = 25^{\circ}C$
			0.257			$V_{GS} = 10V$ , $I_D = 12.7A$ , $T_j = 150^{\circ}C$
Gate resistance	<i>R</i> <sub>G</sub>		1.3		Ω	f= 1MHz, open drain

Table 7 **Dynamic characteristics** 

Parameter	0		Values	3		Nata (Tant Canalities
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Input capacitance	Ciss		3240		pF	$V_{GS} = 0V$ , $V_{DS} = 100V$ , $f = 1MHz$
Output capacitance	Coss		160		pF	
Effective output capacitance, energy related <sup>1)</sup>	$C_{ m o(er)}$		118		pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0 400V
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$		582		pF	$I_D$ = constant, $V_{GS}$ = 0V, $V_{DS}$ = 0 400V
Turn-on delay time	<i>t</i> d(on)		16		ns	$V_{DD} = 400 \text{V}, V_{GS} = 13 \text{V},$
Rise time	<i>t</i> r		11		ns	$h_0 = 19.1 \text{A}, R_G = 1.8 \Omega$
Turn-off delay time	t <sub>d(off)</sub>		68		ns	
Fall time	<i>t</i> f		6		ns	

Table 8 Gate charge characteristics

Parameter	0	Values				Note (Tool Occality
	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Gate to source charge	<b>Q</b> gs		21		nC	V <sub>DD</sub> = 480V, √ <sub>D</sub> = 19.1A,
Gate to drain charge	$Q_{ m gd}$		64		nC	$V_{GS} = 0$ to 10V
Gate charge total	$Q_{g}$		118		nC	
Gate plateau voltage	V <sub>plateau</sub>		6.4		V	

Final Data Sheet Rev. 2.6, 2011-09-26

 $<sup>^{1)}</sup>$   $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V  $^{2)}$   $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V



### Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Тур.	Max.	Oilit	Note / Test Condition
Diode forward voltage	V∕sD		0.9		V	$V_{GS} = 0V$ , $I_F = 19.1A$ , $T_j = 25^{\circ}C$
Reverse recovery time	<i>t</i> rr		150		ns	V <sub>R</sub> = 400V, / <sub>F</sub> = 19.1A,
Reverse recovery charge	Q <sub>rr</sub>		0.8		μC	d <i>i</i> ⊧/d <i>t</i> = 100A/μs
Peak reverse recovery current	/ <sub>rrm</sub>		8.3		А	

Final Data Sheet 7 Rev. 2.6, 2011-09-26

### 5 Electrical characteristics diagrams

Table 10

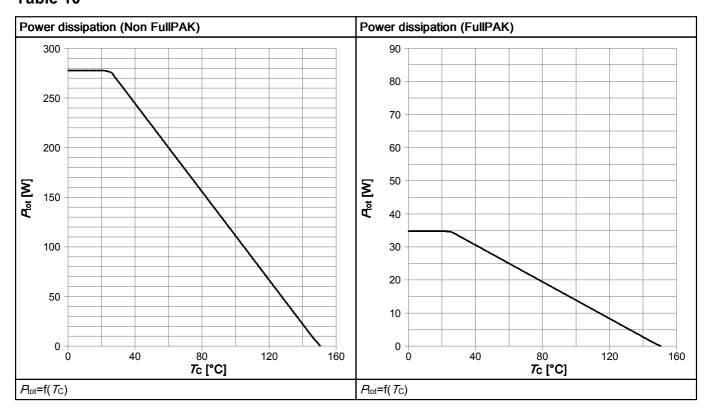
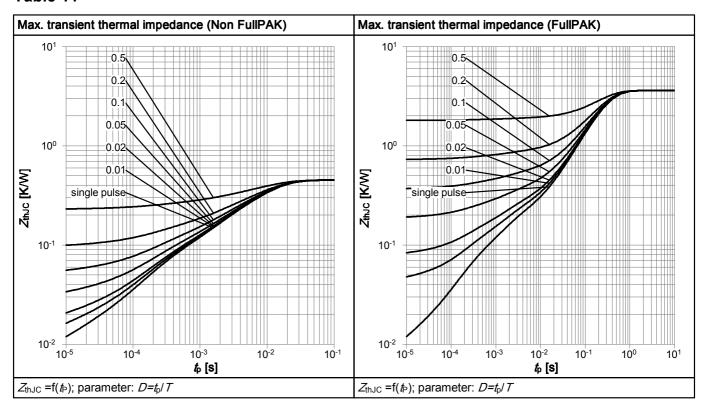


Table 11



Final Data Sheet 8 Rev. 2.6, 2011-09-26

#### Table 12

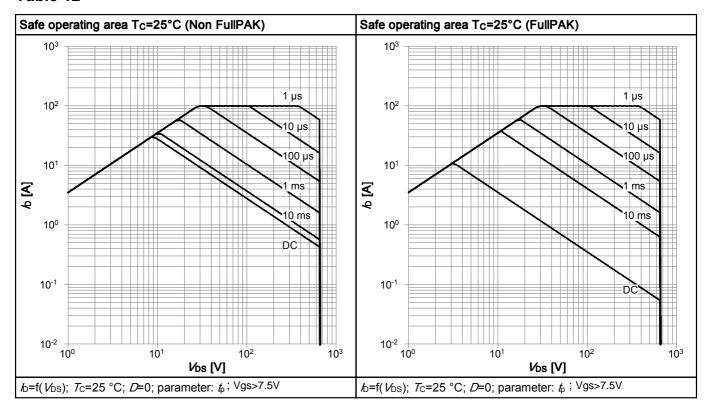
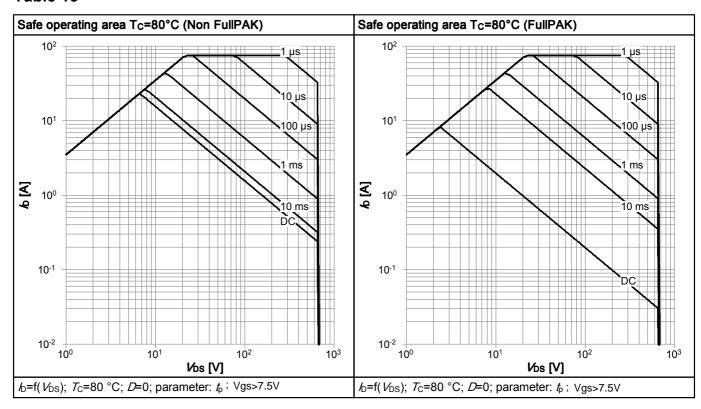
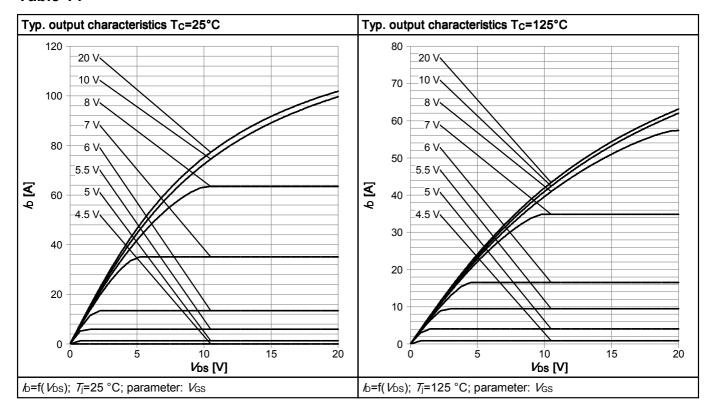


Table 13

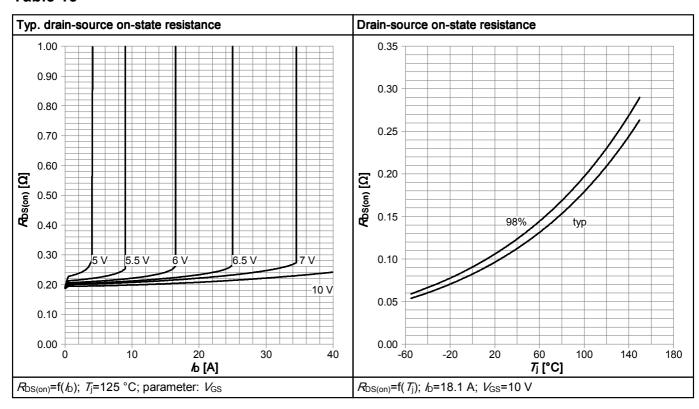


Final Data Sheet 9 Rev. 2.6, 2011-09-26

#### Table 14



#### Table 15



Final Data Sheet 10 Rev. 2.6, 2011-09-26

#### Table 16

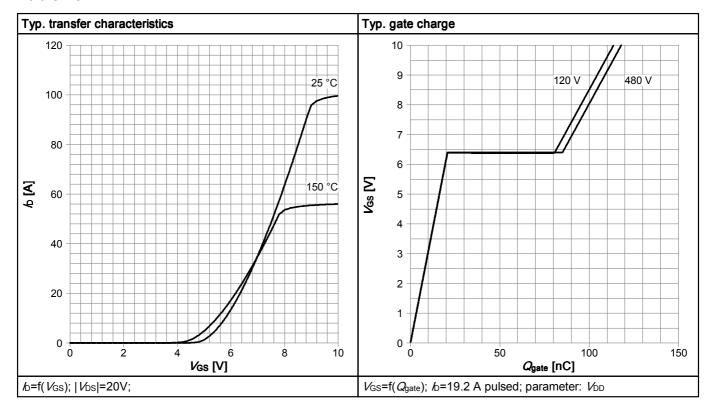
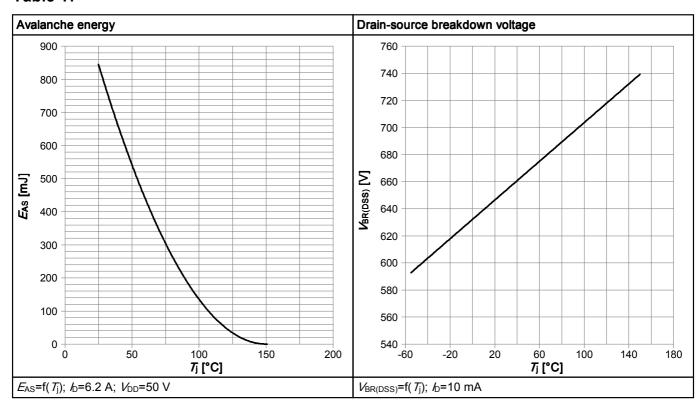
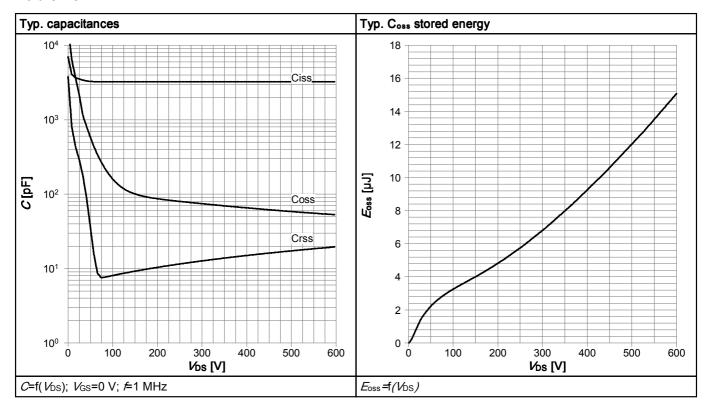


Table 17

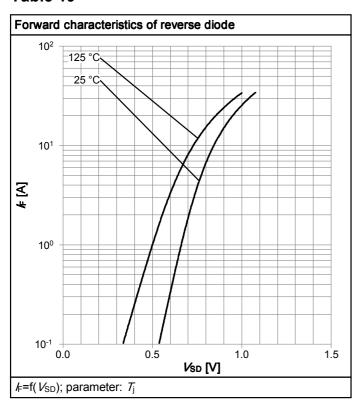


Final Data Sheet 11 Rev. 2.6, 2011-09-26

#### Table 18



#### Table 19



Final Data Sheet 12 Rev. 2.6, 2011-09-26

### 6 Test Circuits

Table 20 Diode\_characteristics

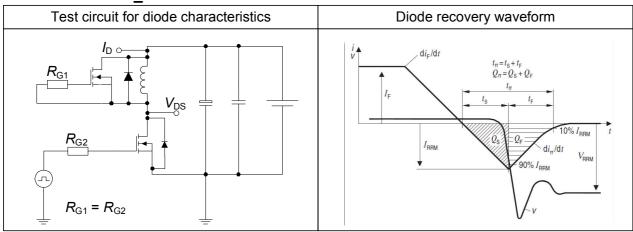


Table 21 Switching\_times

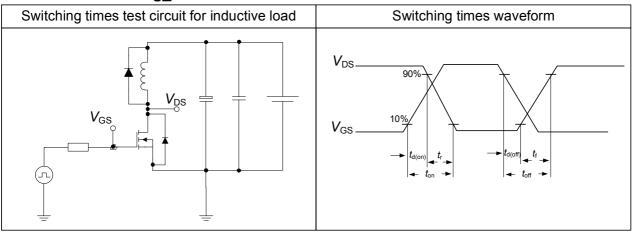
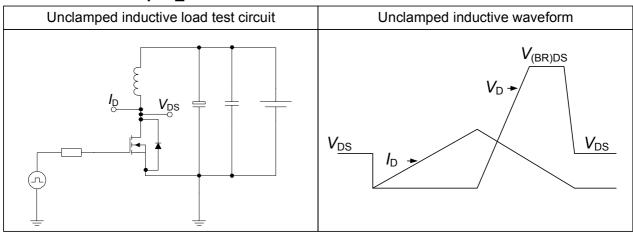


Table 22 Unclamped\_inductive



### 7 Package Outlines

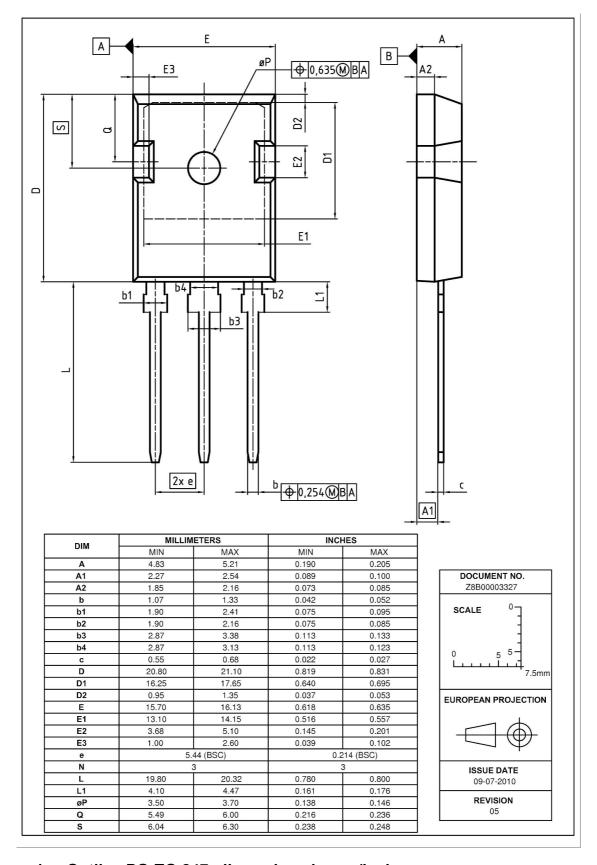


Figure 1 Outline PG-TO 247, dimensions in mm/inches

Final Data Sheet 14 Rev. 2.6, 2011-09-26

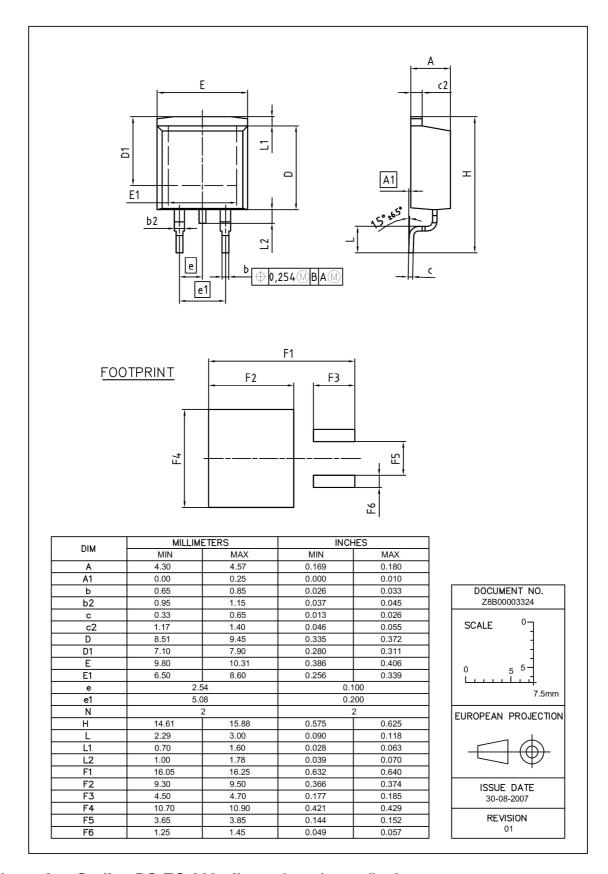


Figure 2 Outline PG-TO 263, dimensions in mm/inches

Final Data Sheet 15 Rev. 2.6, 2011-09-26



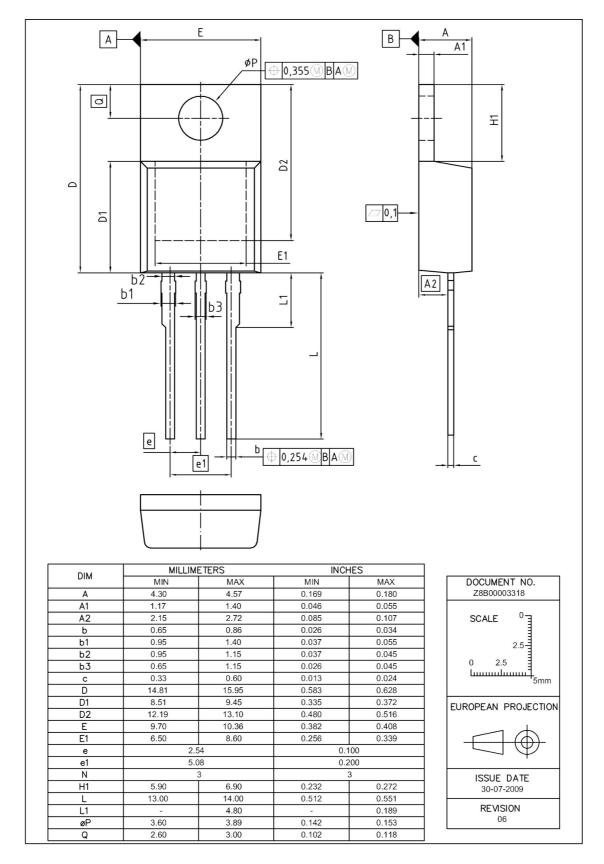


Figure 3 Outline PG-TO 220, dimensions in mm/inches

Final Data Sheet 16 Rev. 2.6, 2011-09-26



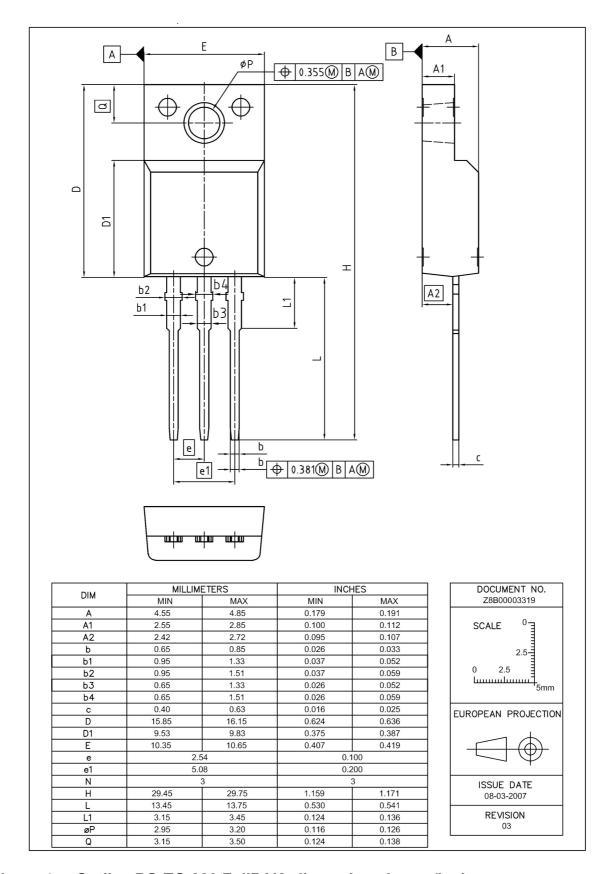


Figure 4 Outline PG-TO 220 FullPAK, dimensions in mm/inches

Final Data Sheet 17 Rev. 2.6, 2011-09-26

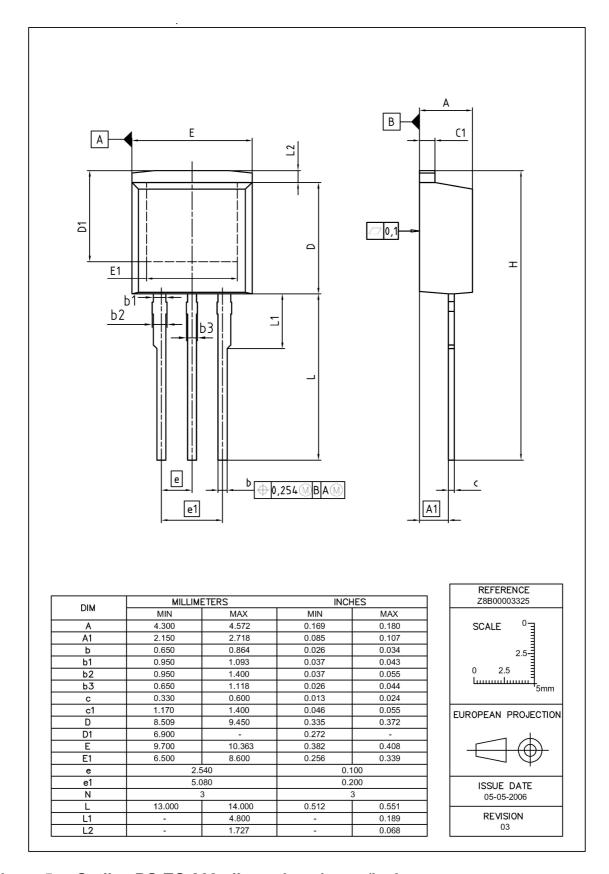


Figure 5 Outline PG-TO 262, dimensions in mm/inches

Final Data Sheet 18 Rev. 2.6, 2011-09-26



### 8 Appendix A

#### Table 23 Related Links

- IFX Design Tools: http://www.infineon.com/cms/en/product/promopages/designtools/index.html
- IFX CoolMOS Webpage: http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8

Final Data Sheet 19 Rev. 2.6, 2011-09-26



#### **Revision History**

IPW65R110CFD, IPB65R110CFD, IPP65R110CFD, IPA65R110CFD, IPI65R110CFD

Revision: 2011-09-26, Rev. 2.6

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.1	2011-06-07	Release the final datasheet
2.2	2011-06-22	-
2.3	2011-08-30	update to CFD2 standard
2.4	2011-09-14	update pin naming
2.5	2011-09-16	release of new pin naming
2.6	2011-09-26	update the Igss test condition

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com** 

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Final Data Sheet 20 Rev. 2.6, 2011-09-26