MOSFET – N-Channel POWERTRENCH®

100 V, 39 A, 14.8 mΩ

FDMS3662

PQFN8 5X6, 1.27P
CASE 483AE

Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

Features

- Max $R_{DS(on)}$ = 14.8 mΩ at V_{GS} = 10 V, I_D = 8.9 A
- Advanced Package and Silicon combination for low $R_{DS(on)}$
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
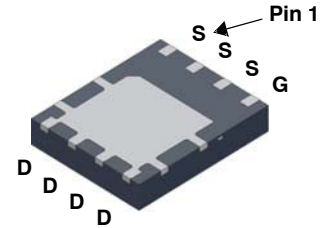- These Device is Pb−Free and RoHS Compliant

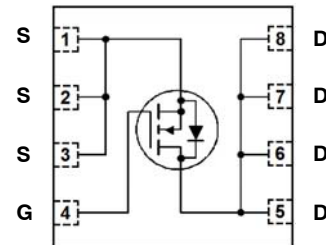### Typical Applications

- DC−DC Conversion

MARKING DIAGRAM

&Z&3&K
3662

&Z   = Assembly Plant Code
&3   = Numeric Date Code
&K   = 2−Digit Lot Code
3662 = Specific Device Code

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

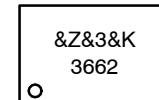| Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous T_C = 25°C – Continuous T_A = 25°C (Note 1a) – Pulsed	 39 8.9 90	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	384	mJ
P_D	Power Dissipation T_C = 25°C	104	W
	Power Dissipation T_A = 25°C (Note 1a)	2.5	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDMS3662	PQFN−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDMS3662

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS $T_J = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25°C	–	74	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 0\ V$, $V_{DS} = 80\ V$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm20\ V$, $V_{DS} = 0\ V$	–	–	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$	2.5	3.5	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 380\ \mu A$, Referenced to 25°C	–	–10.8	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\ V$, $I_D = 8.9\ A$ $V_{GS} = 10\ V$, $I_D = 8.9\ A$, $T_J = 125°C$	–	11.4 19.0	14.8 24.7	mΩ
g_{FS}	Forward Transconductance	$V_{DD} = 10\ V$, $I_D = 8.9\ A$	–	37	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 50\ V$, $V_{GS} = 0\ V$, $f = 1\ MHz$	–	3470	4620	pF
C_{oss}	Output Capacitance		–	245	325	pF
C_{rss}	Reverse Transfer Capacitance		–	110	165	pF
R_g	Gate Resistance	$f = 1\ MHz$	–	1.4	–	Ω
Switching Characteristics						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 50\ V$, $I_D = 8.9\ A$, $V_{GS} = 10\ V$, $R_{GEN} = 6\ \Omega$	–	25	40	ns
t_r	Rise Time		–	15	26	ns
$t_{d(off)}$	Turn–Off Delay Time		–	32	52	ns
t_f	Fall Time		–	6	10	ns
Q_g	Total Gate Charge at 10 V	$V_{DD} = 50\ V$, $I_D = 8.9\ A$	–	54	75	nC
Q_{gs}	Gate to Source Charge		–	18	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	18	–	nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ V$, $I_S = 8.9\ A$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\ V$, $I_S = 2.1\ A$ (Note 2)	–	0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 8.9\ A$, $di/dt = 100\ A/\mu s$	–	45	73	ns
Q_{rr}	Reverse Recovery Charge		–	71	115	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
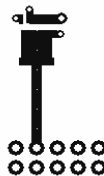
FDMS3662

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
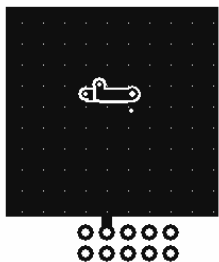
a).50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b).125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = 16 A, V_{DD} = 100 V, V_{GS} =10 V.

TYPICAL CHARACTERISTICS Tc = 25 °C unless otherwise noted
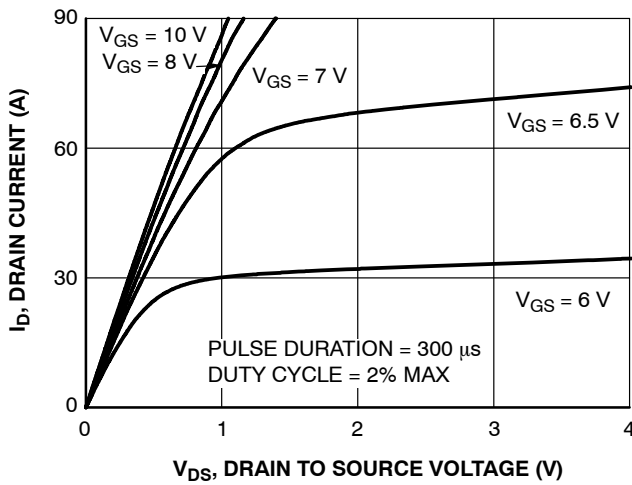
Figure 1. On−Region Characteristics
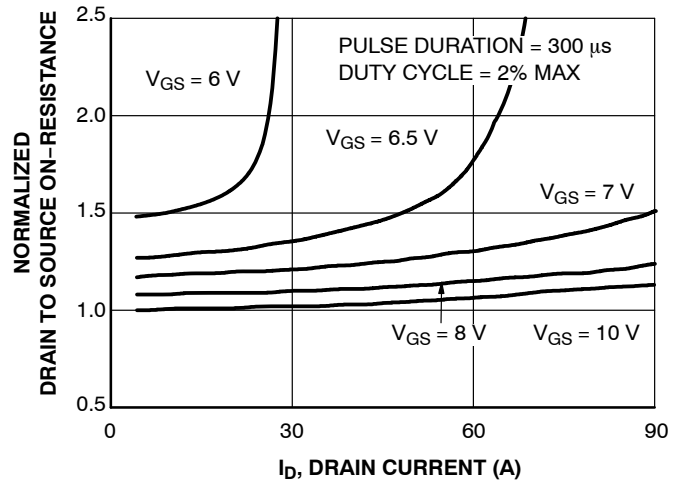
Figure 2. Normalized On−Resistance vs.
Drain Current and Gate Voltage
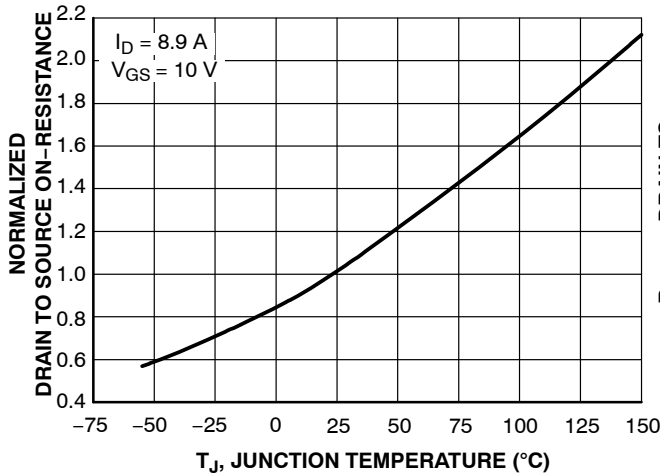
Figure 3. Normalized On−Resistance vs
Junction Temperature
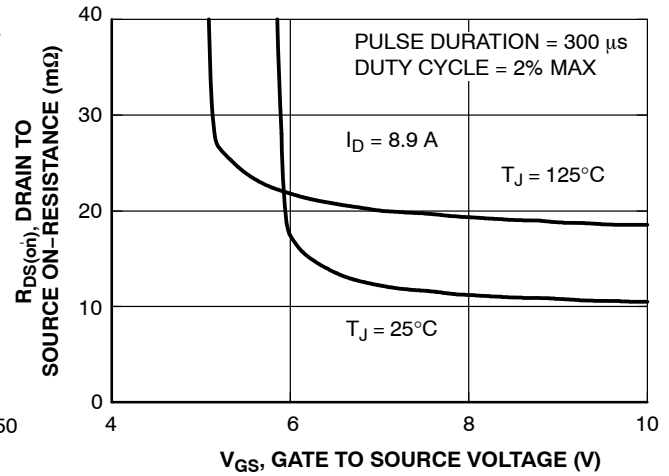
Figure 4. On−Resistance vs Gate to
Source Voltage
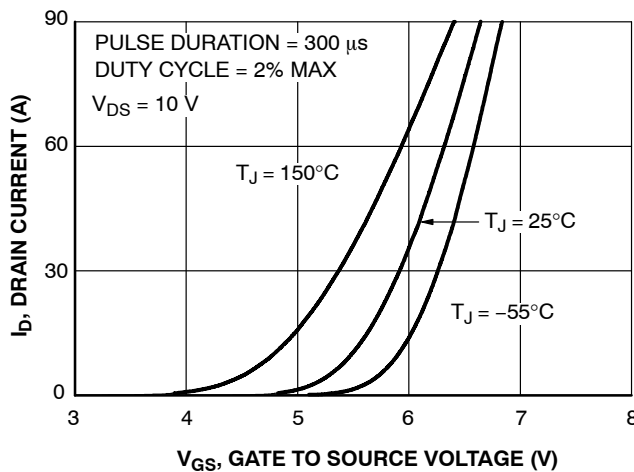
Figure 5. Transfer Characteristics
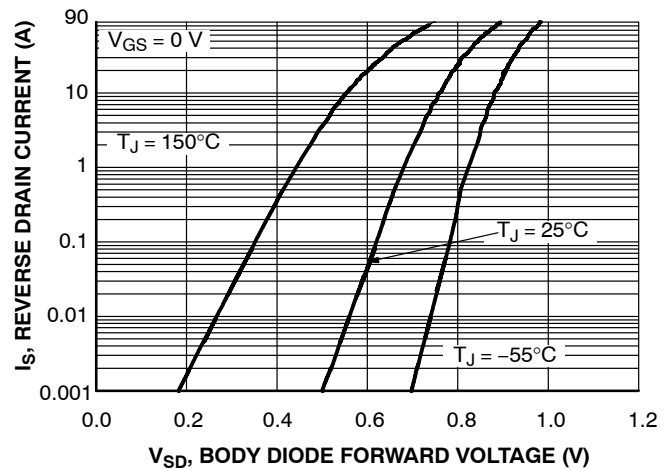
Figure 6. Source to Drain Diode Forward Voltage vs
Source Current

TYPICAL CHARACTERISTICS Tc = 25 °C unless otherwise noted (CONTINUED)
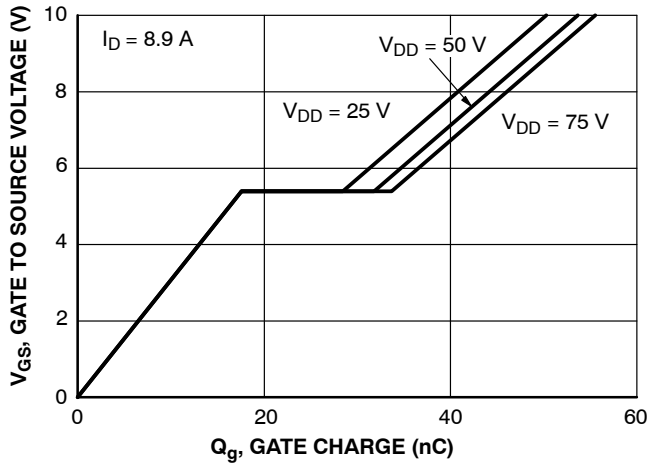
Figure 7. Gate Charge Characteristics
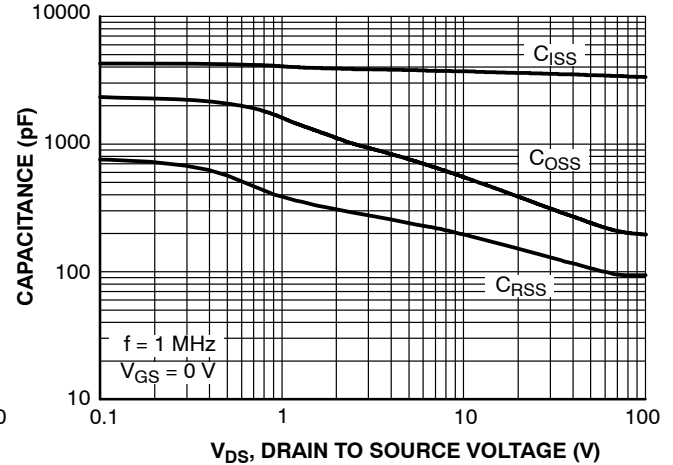
Figure 8. Capacitance vs Drain to Source Voltage
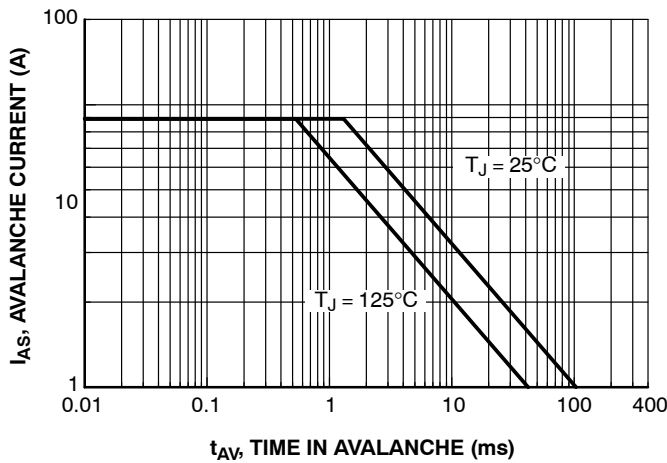
Figure 9. Unclamped Inductive Switching Capability
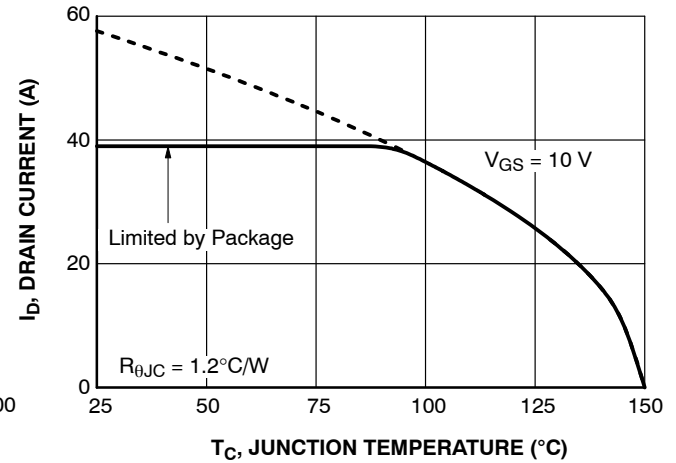
Figure 10. Maximum Continuous Drain Current vs. Case Temperature
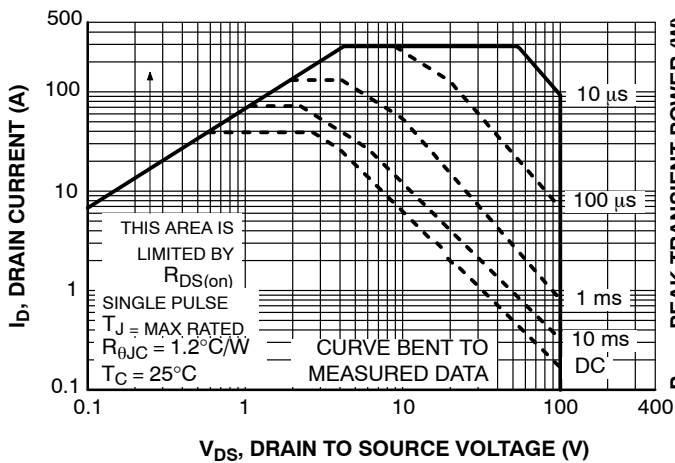
Figure 11. Forward Bias Safe Operating Area
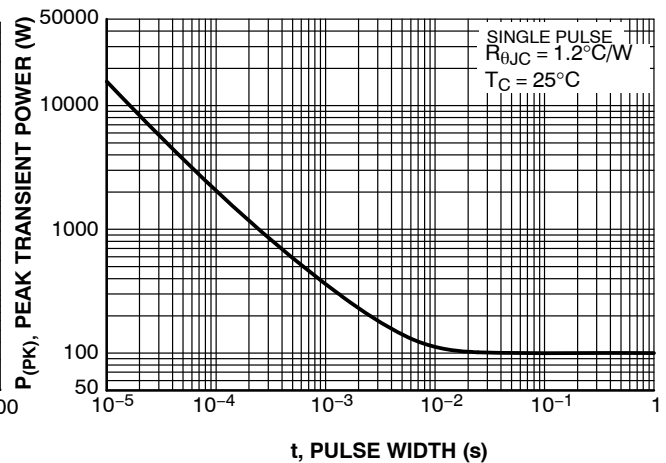
Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS Tc = 25 °C unless otherwise noted (CONTINUED)

Figure 13. Transient Thermal Response Curve

The graph axes:
- Y-axis: r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE
- X-axis: t, RECTANGULAR PULSE DURATION (s)

DUTY CYCLE–DESCENDING ORDER

D = 0.5, 0.2, 0.1, 0.05, 0.02, 0.01

SINGLE PULSE

NOTES:
$Z_{\theta JC}(t) = r(t) \times R_{\theta JC}$
$R_{\theta JC} = 1.2$ °C/W
PEAK $T_J = P_{DM} \times Z_{\theta JC}(t) + T_C$
DUTY CYCLE, $D = t_1/t_2$
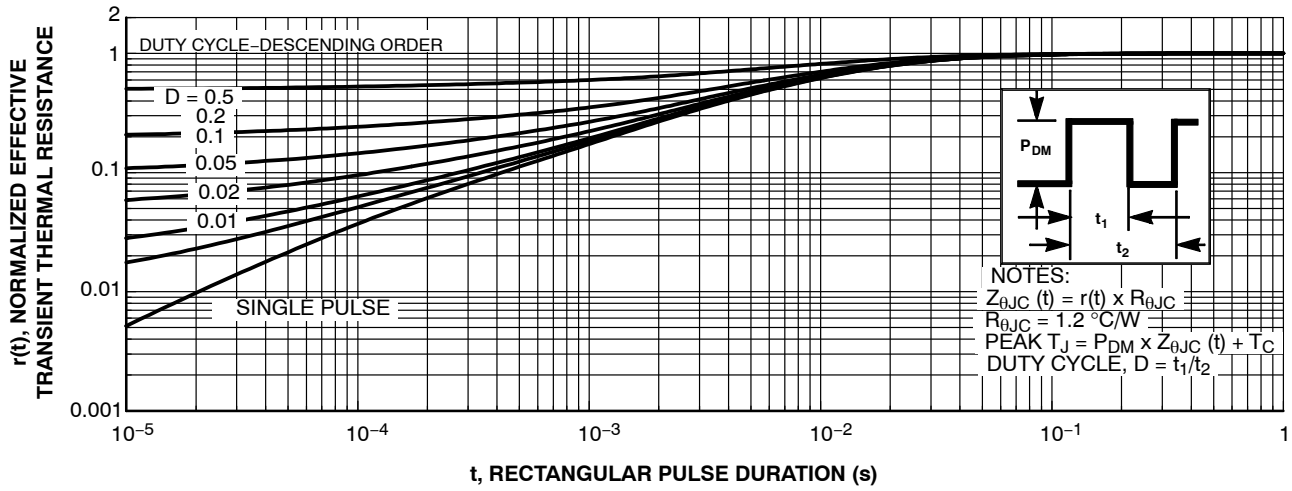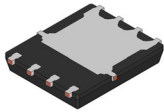
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

TOP VIEW

SEE
DETAIL B
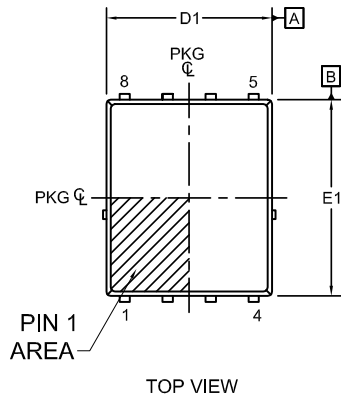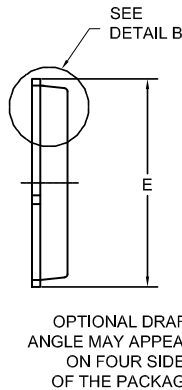
OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

PIN 1
AREA

SEE
DETAIL C

SIDE VIEW

DETAIL C
SCALE: 2:1

SEATING
PLANE
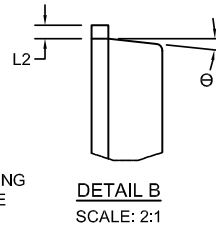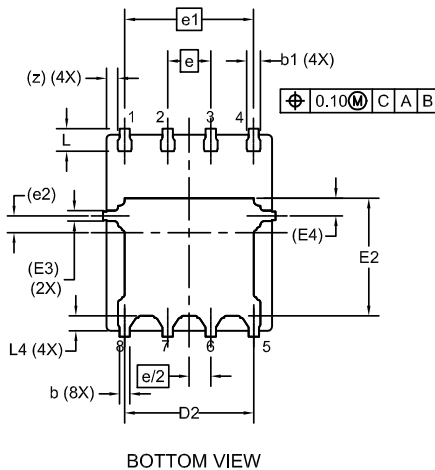
DETAIL B
SCALE: 2:1

BOTTOM VIEW
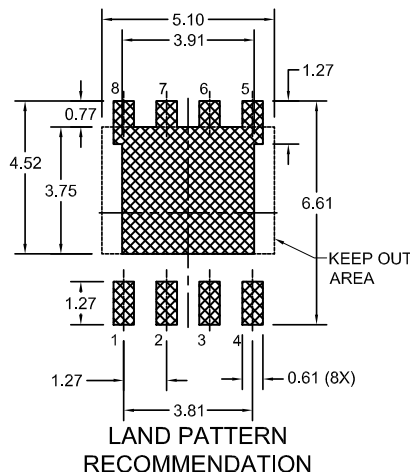
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING
DETAILS, PLEASE DOWNLOAD THE ON
SEMICONDUCTOR SOLDERING AND
MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

KEEP OUT
AREA

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

DOCUMENT NUMBER:	98AON13655G	
DESCRIPTION:	**PQFN8 5X6, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

◊