

PSMN012-100YS

N-channel 100V 12m Ω standard level MOSFET in LFPAK

Rev. 04 — 23 February 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 25 °C; see <u>Figure 1</u>	-	-	60	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	130	W
Tj	junction temperature		-55	-	175	°C
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 60 A; $V_{sup} \le$ 100 V; R_{GS} = 50 Ω; unclamped	-	-	170	mJ
Dynamic	characteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 45 \text{ A};$	-	19	-	nC
$Q_{G(tot)}$	total gate charge	V _{DS} = 50 V; see <u>Figure 14</u> and <u>15</u>	-	64	-	nC



Table 1. Quick reference ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	aracteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 100 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{}$	-	-	23	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure } 13}{\text{Figure } 13}$	-	10	12	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		_
2	S	source	mb	D
3	S	source		
4	G	gate	Q	<u> </u>
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 Ś
			SOT669 (LFPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN012-100YS	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V_{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{mb} = 100 °C; see <u>Figure 1</u>	-	43	Α
		T _{mb} = 25 °C; see <u>Figure 1</u>	-	60	Α
I_{DM}	peak drain current	$t_p \le 10 \mu s$; pulsed; $T_{mb} = 25 \text{ °C}$; see Figure 3	-	242	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	130	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-dr	ain diode				
Is	source current	T _{mb} = 25 °C	-	60	Α
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	242	Α
Avalanche	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 60 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; unclamped	-	170	mJ

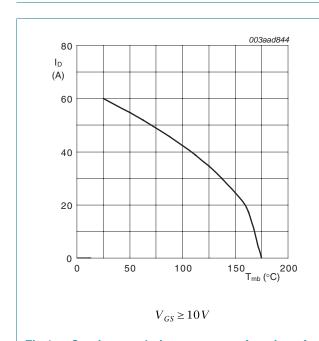


Fig 1. Continuous drain current as a function of mounting base temperature

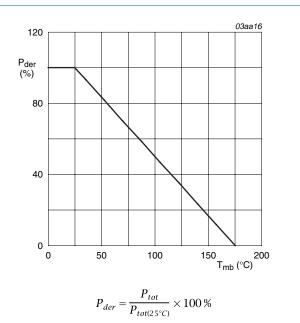
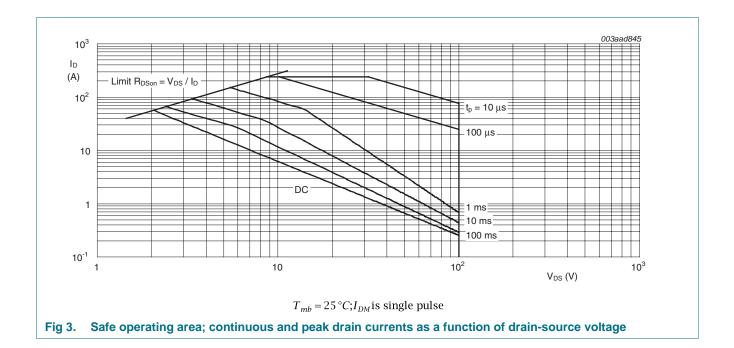


Fig 2. Normalized total power dissipation as a function of mounting base temperature



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.5	1.1	K/W

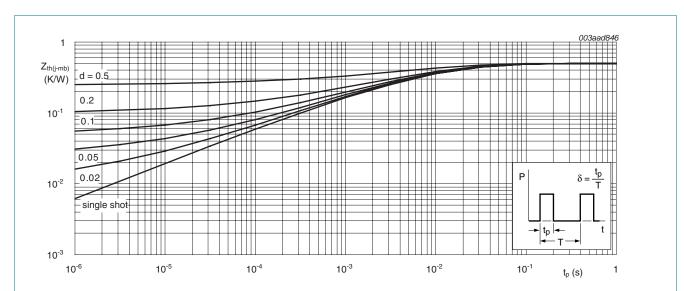


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

6. Characteristics

Table 6. Characteristics

Table 0.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	90	-	-	V
	breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
$V_{\text{GS(th)}}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175 \text{ °C}$; see Figure 10	0.95	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 11</u> and <u>10</u>	2	3	4	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 10	-	-	4.6	V
I _{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.06	5	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ °C};$ see <u>Figure 12</u>	-	-	23	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12	-	27	35.8	mΩ
		$V_{GS} = 10 \text{ V; } I_D = 15 \text{ A; } T_j = 25 \text{ °C;}$ see Figure 13	-	10	12	mΩ
R_{G}	internal gate resistance (AC)	f = 1 MHz	-	0.7	-	Ω
Dynamic o	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	51	-	nC
		I _D = 45 A; V _{DS} = 50 V; V _{GS} = 10 V;	-	64	-	nC
Q_{GS}	gate-source charge	see <u>Figure 14</u> and <u>15</u>	-	14.9	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	$I_D = 45 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	10.2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	4.7	-	nC
Q_{GD}	gate-drain charge	$I_D = 45 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; see <u>Figure 14</u> and <u>15</u>	-	19	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V}$; see <u>Figure 14</u> and <u>15</u>	-	4.4	-	V
C _{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ °C};$	-	3500	-	pF
C _{oss}	output capacitance	see Figure 16	-	246	-	pF
C _{rss}	reverse transfer capacitance		-	149	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 1.1 \Omega; V_{GS} = 10 \text{ V};$	-	23	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \ \Omega; T_j = 25 \ ^{\circ}C$	-	31	-	ns
t _{d(off)}	turn-off delay time		-	52.5	-	ns
t _f	fall time		-	25	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dr	ain diode					
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see <u>Figure 17</u>	-	8.0	1.2	V
t _{rr}	reverse recovery time	$I_S = 15 \text{ A}$; $dI_S/dt = 100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	56	-	ns
Q _r	recovered charge	$V_{DS} = 50 \text{ V}$	-	129	-	nC

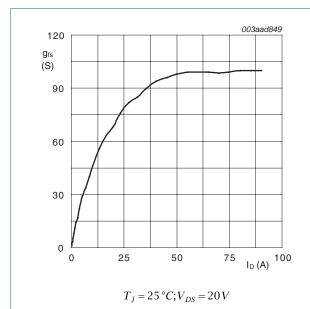


Fig 5. Forward transconductance as a function of drain current; typical values

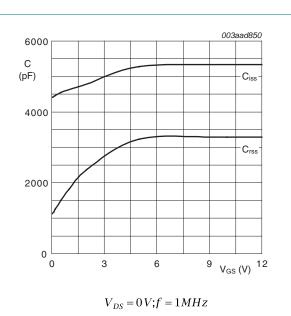


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

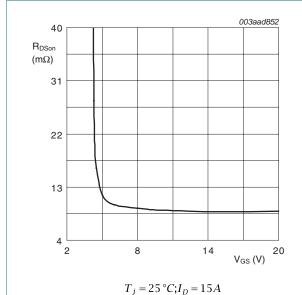


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

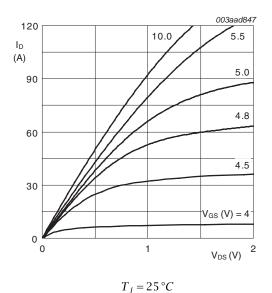


Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values

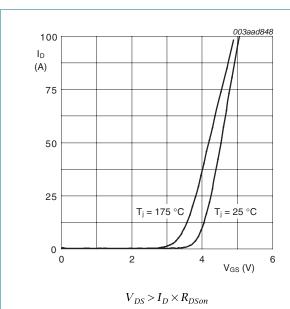
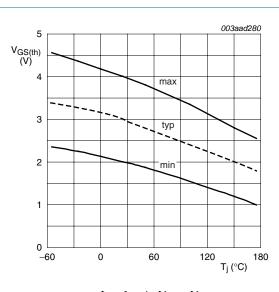
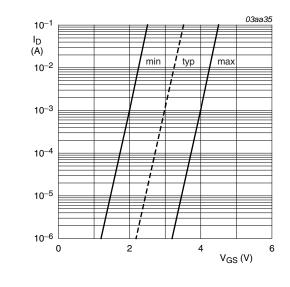


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



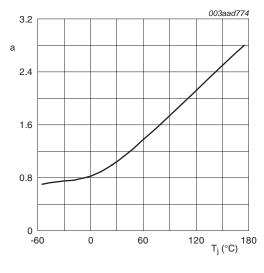
 $I_D = 1$ mA; $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$=\frac{R_{DSon}}{R_{DSon(25\,^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

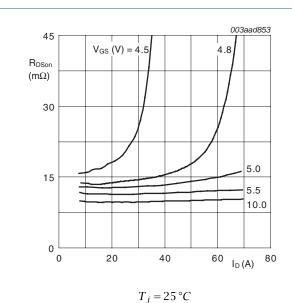


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

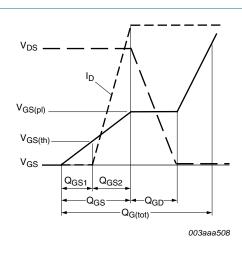


Fig 14. Gate charge waveform definitions

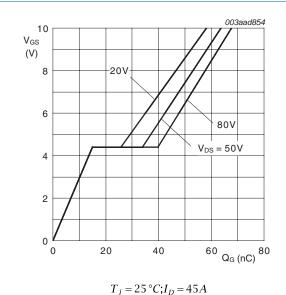
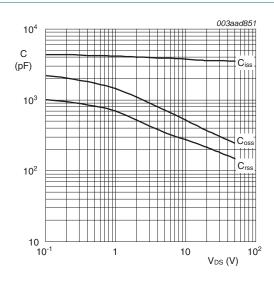
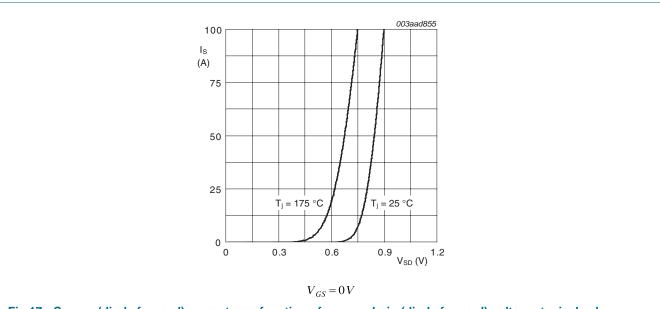


Fig 15. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

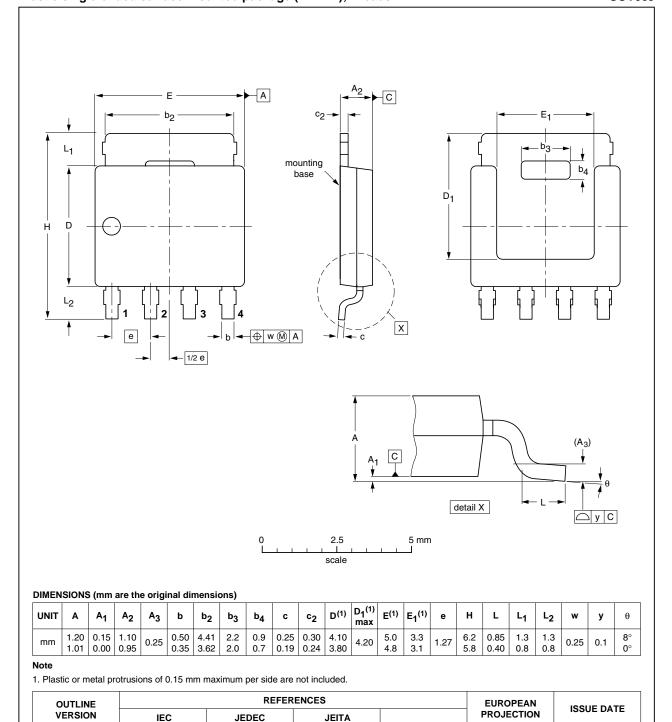


Fig 18. Package outline SOT669 (LFPAK)

PSMN012-100YS_4

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MO-235

04-10-13

06-03-16

SOT669

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN012-100YS_4	20100223	Product data sheet	-	PSMN012-100YS_3
Modifications:	 Status char 	nged from objective to pro	duct.	
PSMN012-100YS_3	20100107	Product data sheet	-	PSMN012-100YS_2
PSMN012-100YS_2	20091214	Objective data sheet	-	PSMN012-100YS_1
PSMN012-100YS_1	20091022	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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PSMN012-100YS

Nexperia

N-channel 100V 12m Ω standard level MOSFET in LFPAK

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