

OptiMOS®-T2 Power-Transistor





Features

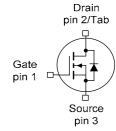
- N-channel Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

$V_{ m DS}$	40	٧
$R_{\mathrm{DS(on),max}}$	4.1	mΩ
I _D	90	Α

PG-TO252-3-313





Type Package Marking IPD90N04S4-04 PG-TO252-3-313 4N0404

Maximum ratings, at T_j =25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit	
Continuous drain current ¹⁾	ID	T _C =25°C, V _{GS} =10V	90	Α	
		$T_{\rm C}$ =100°C, $V_{\rm GS}$ =10 $V^{2)}$	81		
Pulsed drain current ²⁾	I _{D,pulse}	T _C =25°C	360		
Avalanche energy, single pulse ²⁾	E _{AS}	I _D =45A	95	mJ	
Avalanche current, single pulse	IAS	-	90	А	
Gate source voltage	V_{GS}	-	±20	V	
Power dissipation	P _{tot}	T _C =25°C	71	W	
Operating and storage temperature	$T_{\rm j},T_{\rm stg}$	-	-55 + 175	°C	
IEC climatic category; DIN IEC 68-1	-	-	55/175/56		



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics ²⁾						
Thermal resistance, junction - case	$R_{ m thJC}$	-	-	-	2.1	K/W
Thermal resistance, junction - ambient, leaded	R _{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	1
		6 cm ² cooling area ³⁾	-	-	40	1

Electrical characteristics, at $T_{\rm j}$ =25 °C, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0V, I _D = 1mA	40	-	-	V
Gate threshold voltage	$V_{\rm GS(th)}$	$V_{\rm DS} = V_{\rm GS}$, $I_{\rm D} = 35 \mu A$	2.0	3.0	4.0	
Zero gate voltage drain current	IDSS	V _{DS} =40V, V _{GS} =0V	-	0.02	1	μΑ
		$V_{\rm DS}$ =18V, $V_{\rm GS}$ =0V, $T_{\rm j}$ =85°C ²⁾	1	1	20	
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V	-	-	100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10V, I _D =90A	-	3.7	4.1	mΩ



Parameter	Symbol Conditions		Values			Unit	
			min.	typ.	max.		
Dynamic characteristics ²⁾							
Input capacitance	C iss		-	2650	3440	pF	
Output capacitance	C _{oss}	V _{GS} =0 V, V _{DS} =25 V, f=1 MHz	-	650	840		
Reverse transfer capacitance	C _{rss}		-	20	46		
Turn-on delay time	t _{d(on)}		-	10	-	ns	
Rise time	$t_{\rm r}$	V _{DD} =30V, V _{GS} =10V,	-	11	-		
Turn-off delay time	$t_{d(off)}$	$I_{\rm D}$ =90A, $R_{\rm G}$ =3.5 Ω	-	9	-		
Fall time	t _f		-	11	-		
Gate Charge Characteristics ²⁾							
Gate to source charge	Q _{gs}		-	16	20	nC	
Gate to drain charge	Q _{gd}	V _{DD} =32V, I _D =90A,	-	5	12		
Gate charge total	Q _g	V _{GS} =0 to 10V	-	33	43		
Gate plateau voltage	$V_{ m plateau}$		-	5.8	-	V	
Reverse Diode							
Diode continous forward current ²⁾	Is	T 05°0	-	-	90	Α	
Diode pulse current ²⁾	I _{S,pulse}	-T _C =25°C	-	-	360		
Diode forward voltage	V _{SD}	V _{GS} =0V, I _F =90A, T _j =25°C	-	0.9	1.3	V	
Reverse recovery time ²⁾	t _{rr}	V_R =20V, I_F =50A, d i_F /d t =100A/ μ s	-	39	-	ns	
Reverse recovery charge ²⁾	Qn		-	35	-	nC	

¹⁾ Current is limited by bondwire; with an $R_{\rm thJC}$ = 2.1K/W the chip is able to carry 99A at 25°C.

²⁾ Defined by design. Not subject to production test.

 $^{^{3)}}$ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm 2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



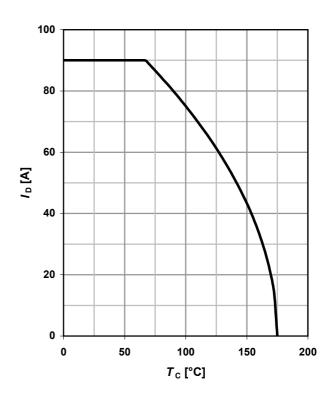
1 Power dissipation

$$P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} \ge 6 \text{ V}$$

80 70 60 50 40 30 20 10 0 50 100 150 200 T_C [°C]

2 Drain current

$$I_D = f(T_C); V_{GS} \ge 6 \text{ V}$$



3 Safe operating area

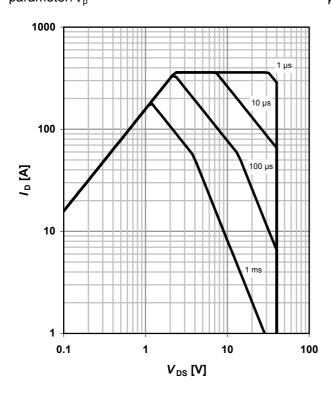
$$I_D = f(V_{DS}); T_C = 25 \,^{\circ}C; D = 0$$

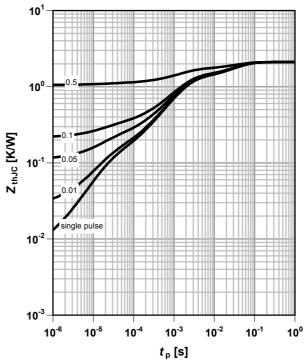
parameter: t_p

4 Max. transient thermal impedance

$$Z_{\rm thJC} = f(t_{\rm p})$$

parameter: $D = t_p/T$



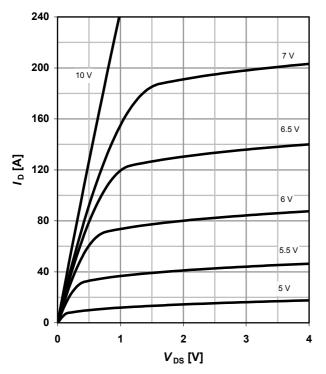




5 Typ. output characteristics

 $I_{\rm D} = f(V_{\rm DS}); T_{\rm j} = 25 \,{}^{\circ}{\rm C}$

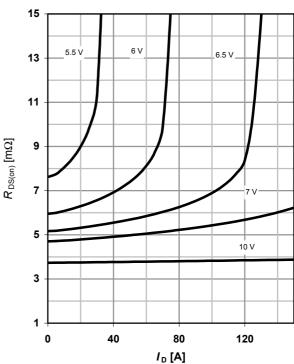
parameter: $V_{\rm GS}$



6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25 \text{ °C}$

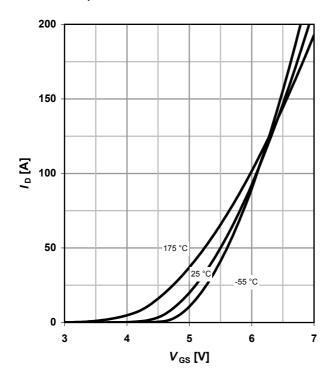
parameter: V_{GS}



7 Typ. transfer characteristics

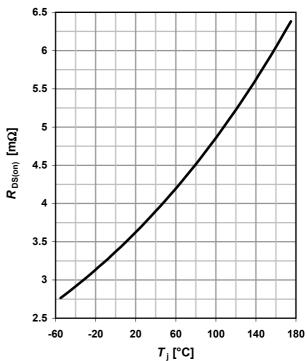
 $I_D = f(V_{GS}); V_{DS} = 6V$

parameter: T_i



8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 90 \text{ A}; V_{GS} = 10 \text{ V}$$





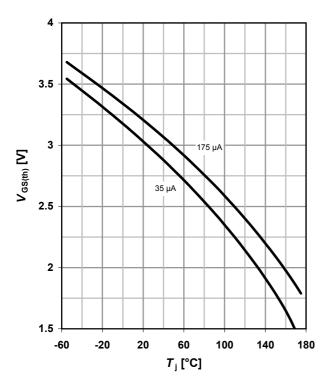
9 Typ. gate threshold voltage

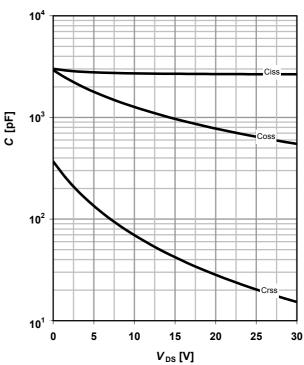
 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D

10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$





11 Typical forward diode characteristicis

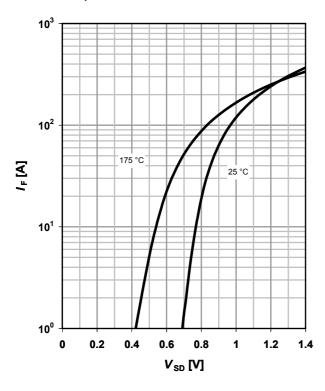
 $IF = f(V_{SD})$

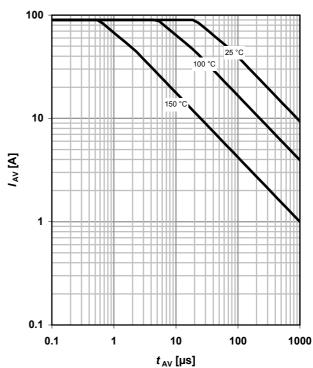
parameter: T_i

12 Avalanche characteristics

 $I_{AS} = f(t_{AV})$

parameter: T_{j(start)}







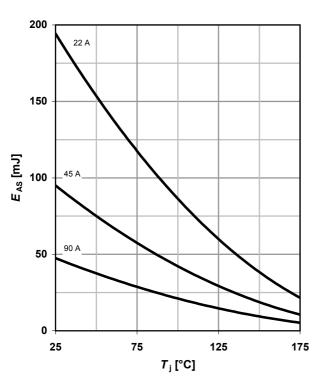
13 Avalanche energy

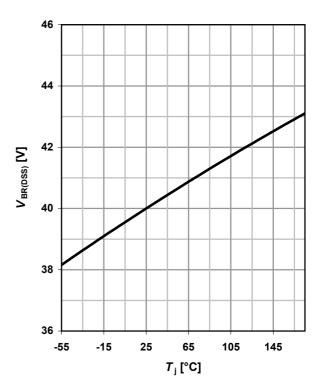
 $E_{AS} = f(T_i)$

parameter: I_D

14 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

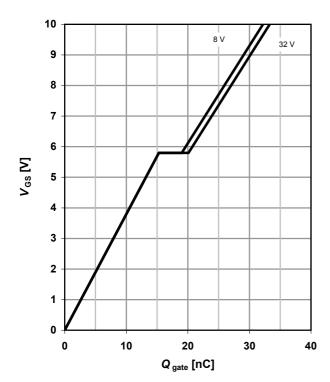




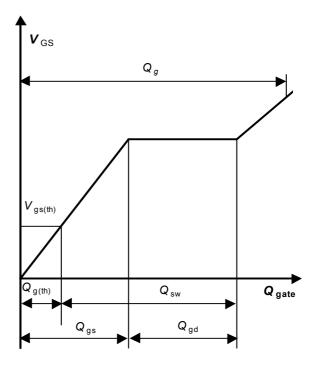
15 Typ. gate charge

 $V_{\rm GS}$ = f(Q $_{\rm gate}$); $I_{\rm D}$ = 90 A pulsed

parameter: $V_{\rm DD}$



16 Gate charge waveforms



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Revision History

Version	Date		Changes
Revision 1.0		06.04.2010	Final Data Sheet