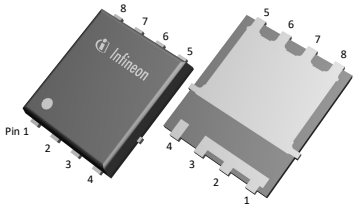
MOSFET

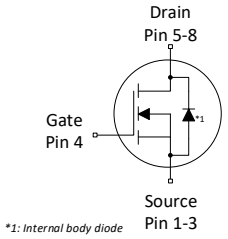
PG-TDSON-8

StrongIRFET™ 2 Power-Transistor, 30 V



Features

- Optimized for a wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified according to JEDEC Standard

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	1.28	mΩ
I_D	270	A
Q_{oss}	54	nC
Q_G (0V..4.5V)	33	nC

Type / Ordering code	Package	Marking	Related links
ISC012N03LF2S	PG-TDSON-8	012N03F2	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	270 191 43	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1080	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	473 946	mJ	I_D=50 A, R_{GS}=25 Ω I_D=25 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167 3	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.9	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	
Thermal resistance, junction - ambient, minimal footprint [5)]	R_{thJA}	-	-	50	°C/W	

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=2 mA
Gate threshold voltage	$V_{GS(th)}$	1.35	1.85	2.35	V	V_{DS}=V_{GS}, I_D=80 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.09 1.39	1.28 2.10	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=25 A
Gate resistance	R_G	-	2.3	-	Ω	-
Transconductance [6]	g_{fs}	95	-	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4700	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	910	-	pF	
Reverse transfer capacitance	C_{rss}	-	240	-	pF	
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	17	-	ns	
Turn-off delay time	$t_{d(off)}$	-	22	-	ns	
Fall time	t_f	-	12	-	ns	

Table 6 Gate charge characteristics [7]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	15	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	8.6	-	nC	
Gate to drain charge	Q_{gd}	-	9.8	-	nC	
Switching charge	Q_{sw}	-	16	-	nC	
Gate charge total [8]	Q_g	-	33	50	nC	
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	
Gate charge total [8]	Q_g	-	69	104	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	29	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Output charge	Q_{oss}	-	54	-	nC	V_{DS}=15 V, V_{GS}=0 V

[7)] See "Gate charge waveforms" for parameter definition

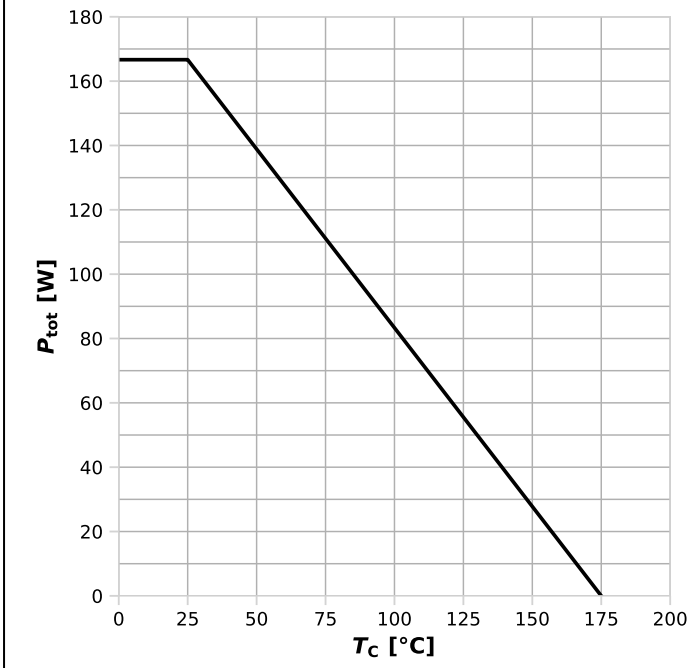
[8)] Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	152	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1080	A	
Diode forward voltage	V_{SD}	-	0.79	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	20	-	ns	V_R=15 V, I_F=50 A, di_F/dt=500 A/µs
Reverse recovery charge	Q_{rr}	-	68	-	nC	

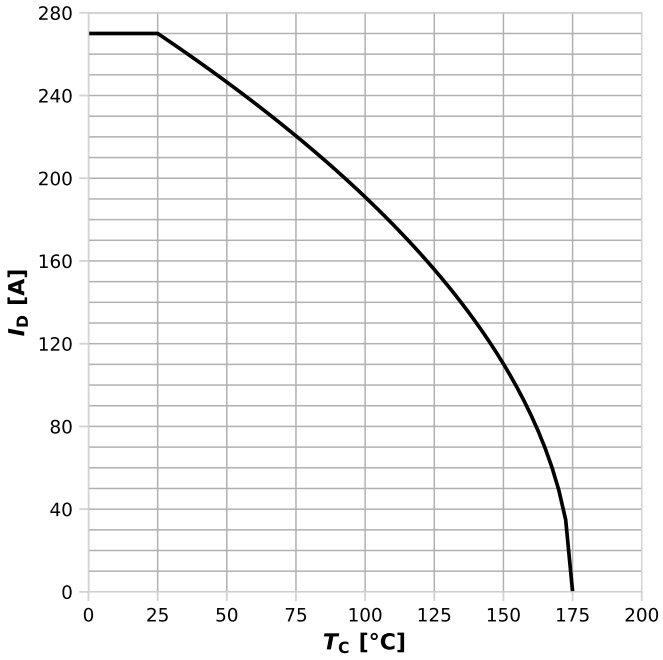
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



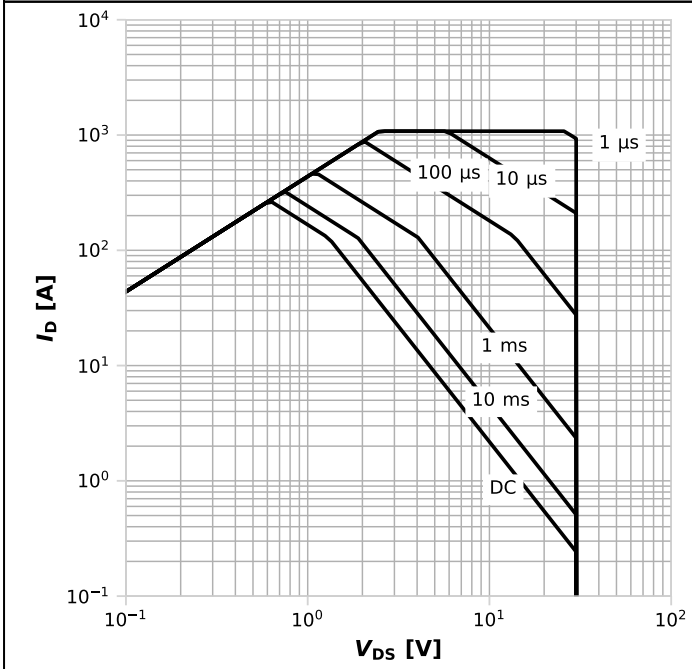
P_{tot}=f(T_C)

Diagram 2: Drain current



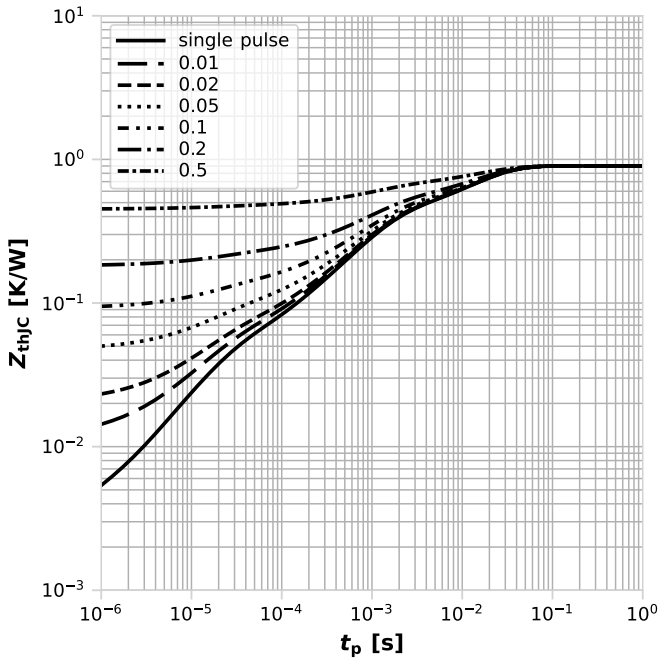
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



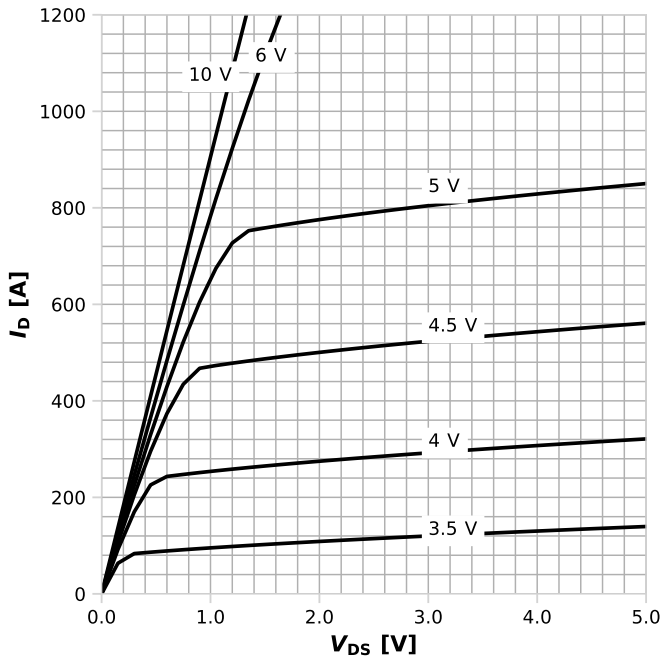
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



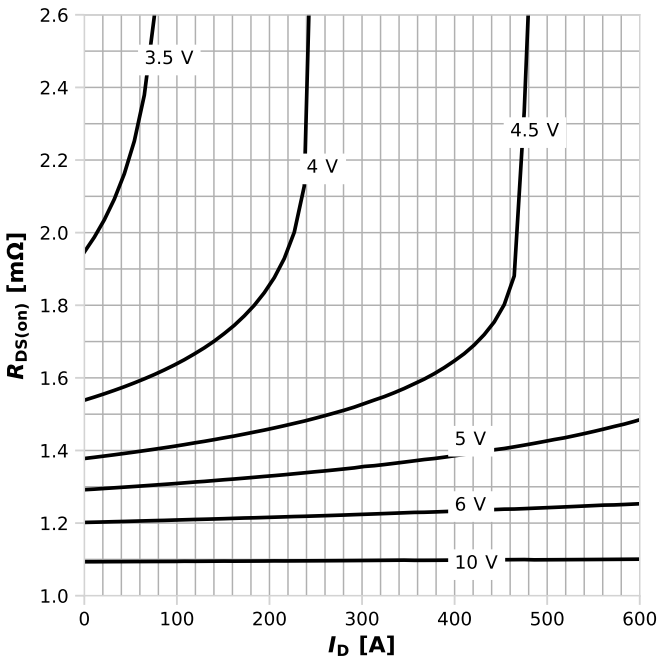
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



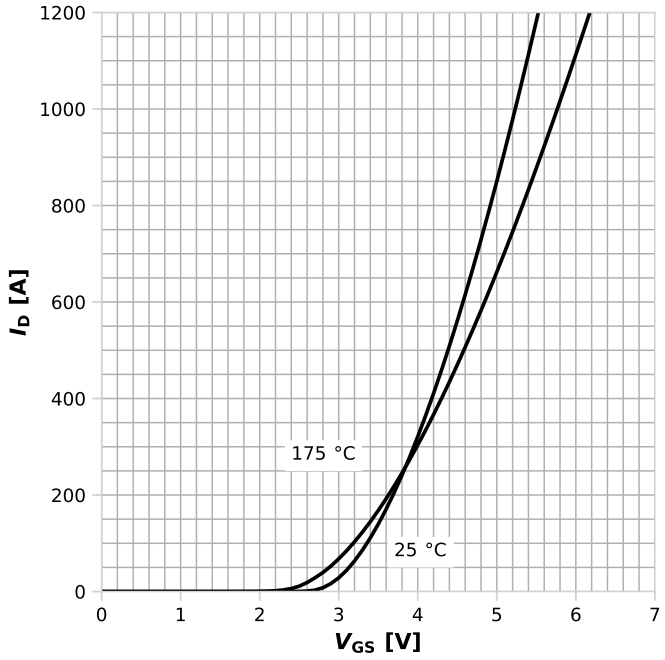
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



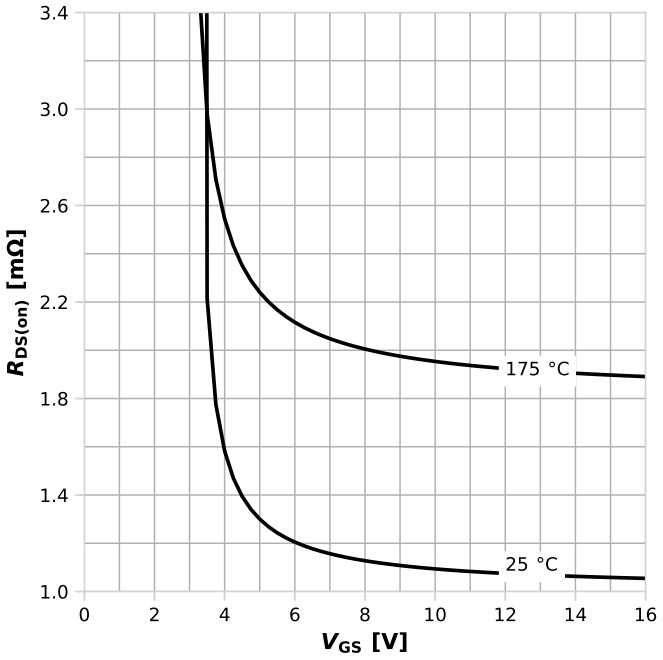
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

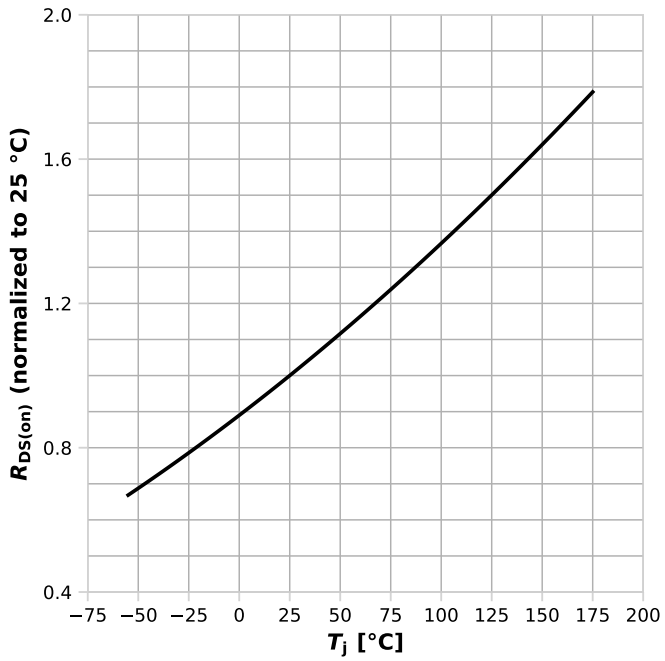
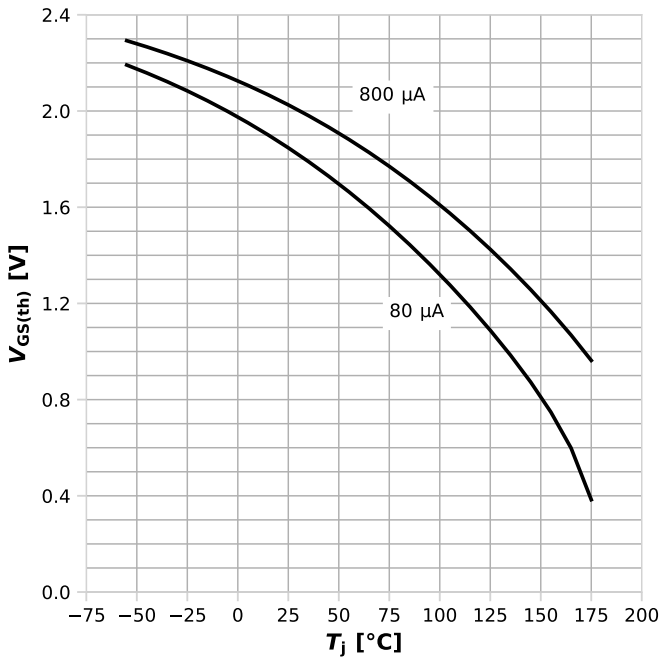
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

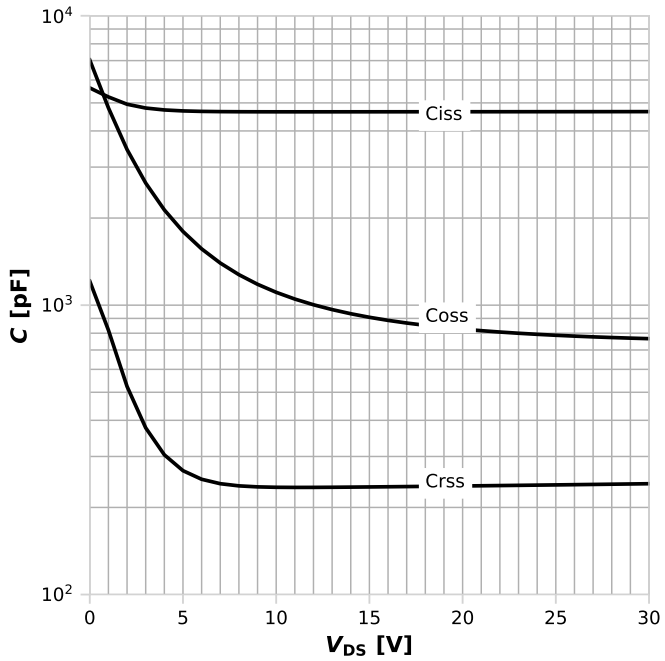
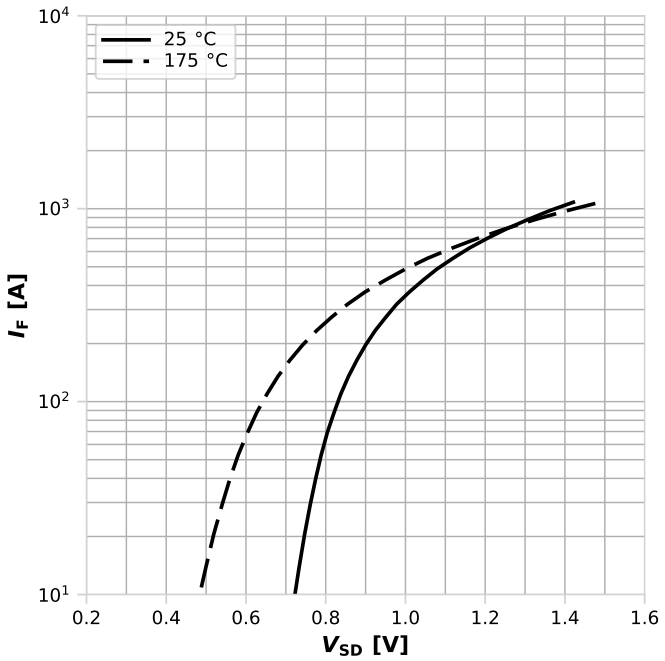
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

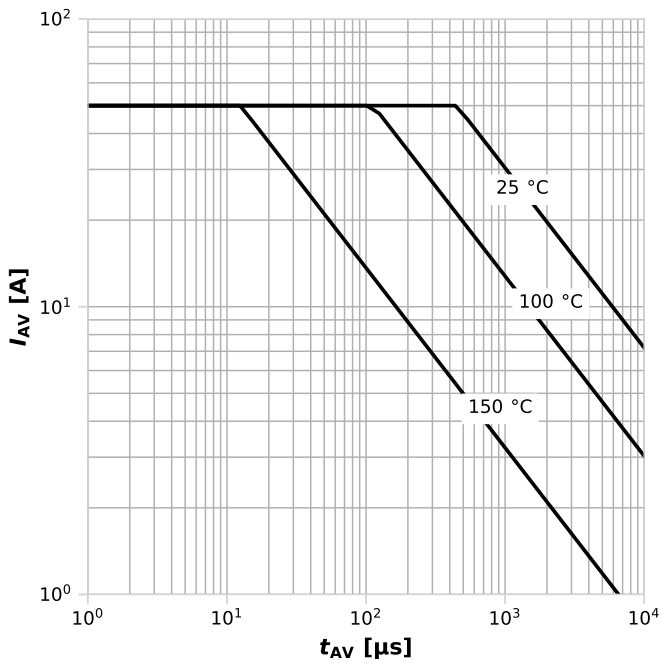
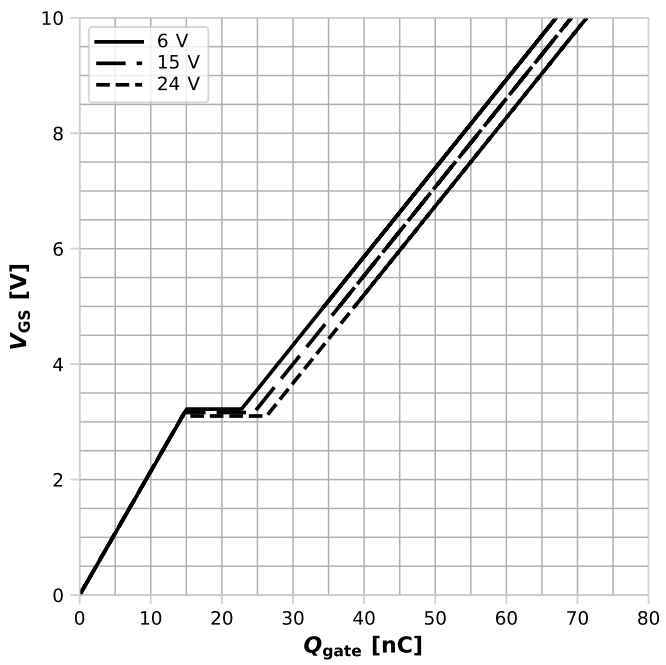
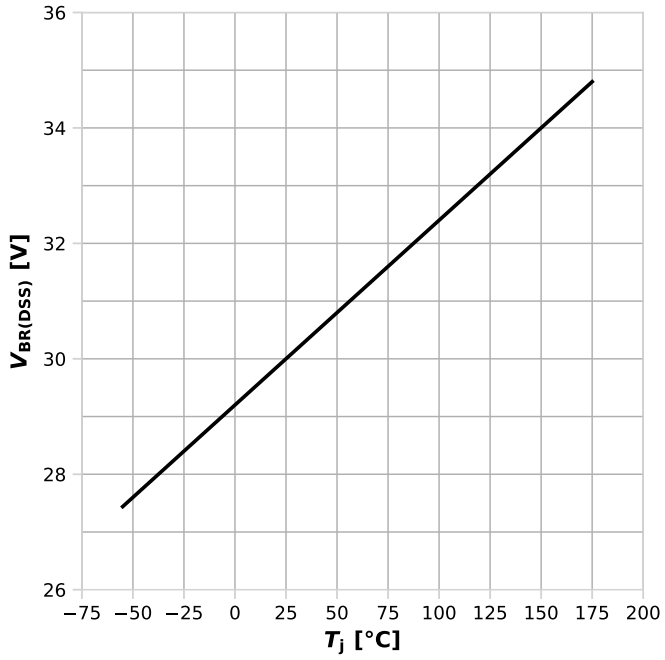
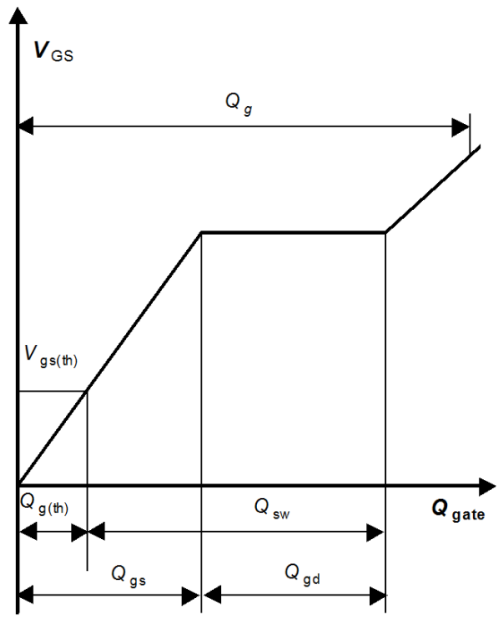
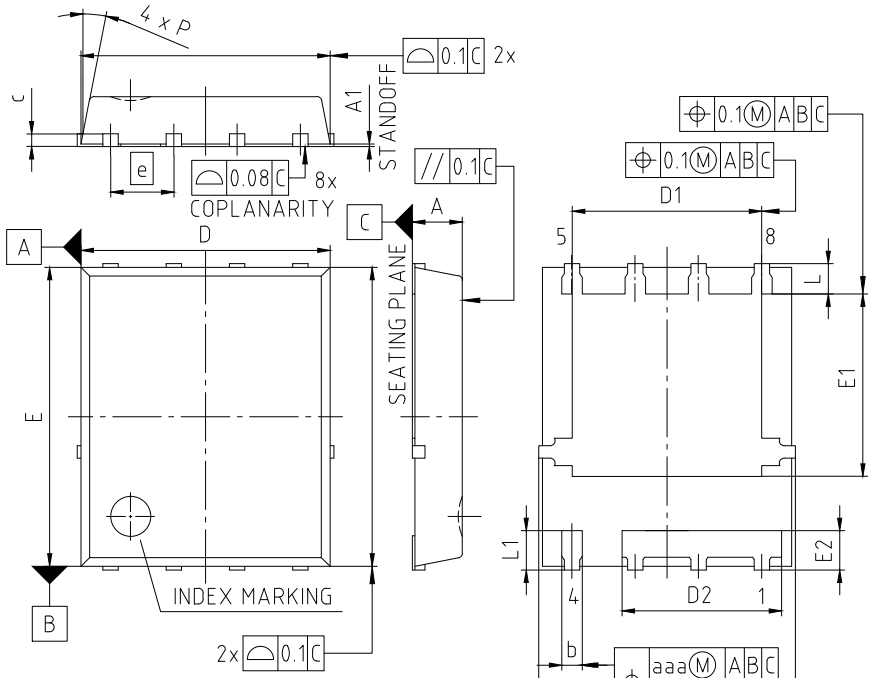
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=2 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0	0.05
b	0.26	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.70	4.40
D2	2.94	3.25
D3	4.80	5.15
E	5.70	6.10
E1	3.40	3.76
E2	0.69	0.90
e	1.27	
L	0.45	0.72
L1	0.69	0.90
aaa	0.10	0.25
P	8°	12°

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4) ALL METAL SURFACES ARE PLATED,
   EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

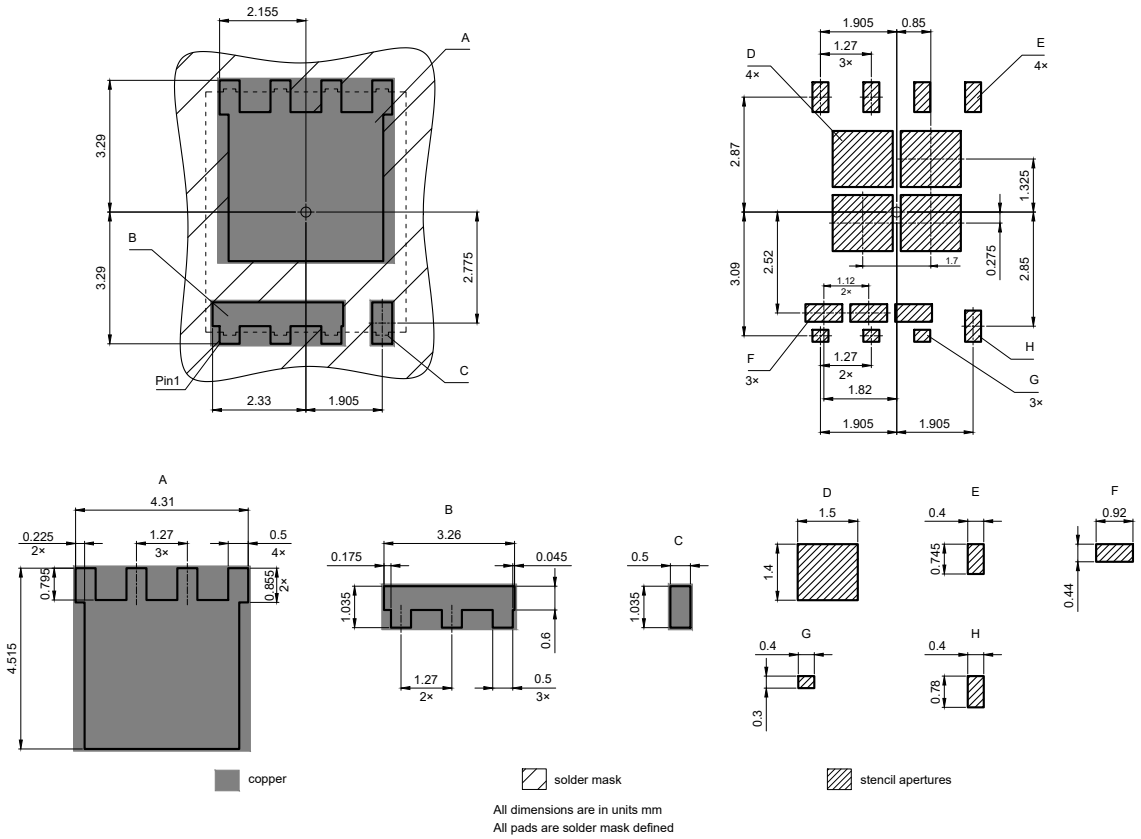


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

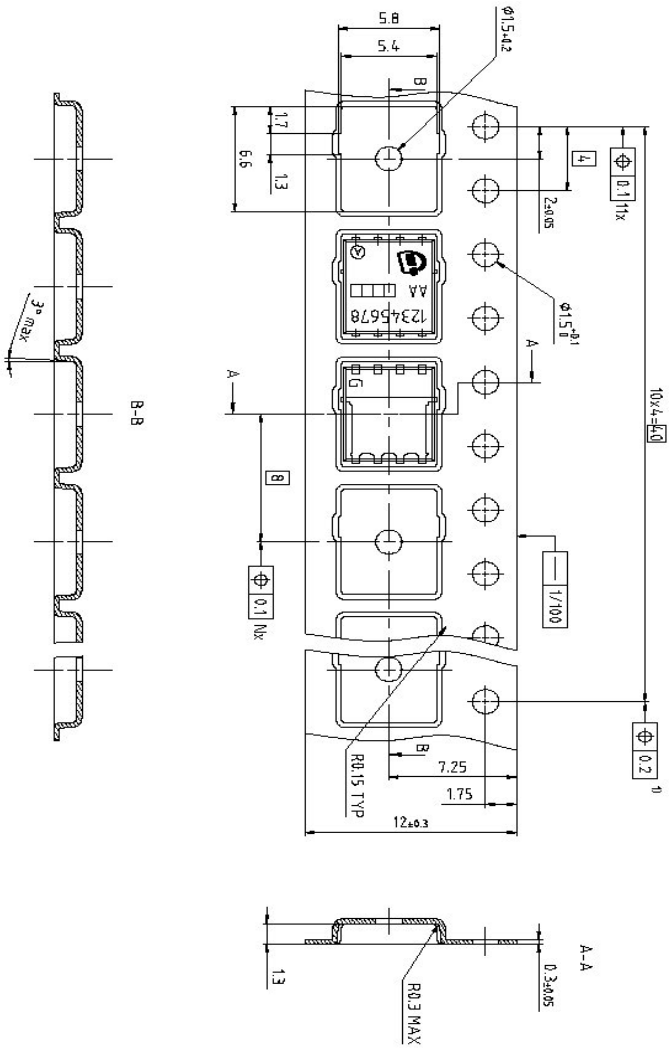


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

ISC012N03LF2S

Revision 2024-11-25, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-08	Release of final
1.1	2024-11-25	updated product validation to "JEDEC standard" and Package outline

Published by
Infineon Technologies AG
81726 München, Germany