

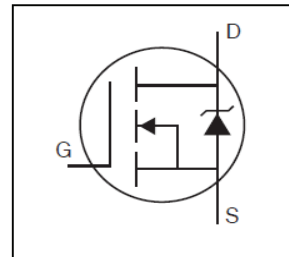
**Features**

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $E_{PULSE}$  Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $Q_G$  for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 150°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

HEXFET® Power MOSFET

**Key Parameters**

$V_{DS}$ max	250	V
$V_{DS}$ (Avalanche) typ.	300	V
$R_{DS(ON)}$ typ. @ 10V	38	mΩ
$I_{RP}$ max @ $T_C = 100^\circ\text{C}$	32	A
$T_J$ max	150	°C



TO-220 Full-Pak

<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low  $E_{PULSE}$  rating. Additional features of this MOSFET are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI4229PbF	TO-220 Full-Pak	Tube	50	IRFI4229PbF

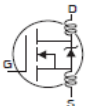
**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	± 30	V
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	19	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	12	
$I_{DM}$	Pulsed Drain Current ①	72	
$I_{RP}$ @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	32	W
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	46	
$P_D$ @ $T_C = 100^\circ\text{C}$	Maximum Power Dissipation	18	
	Linear Derating Factor	0.37	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	2.73	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	340	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	38	46	m $\Omega$	$V_{GS} = 10V, I_D = 11A$
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	—	-12	—	mV/ $^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 250V, V_{GS} = 0V$
		—	—	200		$V_{DS} = 250V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Trans conductance	26	—	—	S	$V_{DS} = 25V, I_D = 11A$
$Q_g$	Total Gate Charge	—	73	110	nC	$I_D = 11A, V_{DS} = 125V$
$Q_{gd}$	Gate-to-Drain Charge	—	24	—		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 125V, V_{GS} = 10V$
$t_r$	Rise Time	—	17	—		$I_D = 11A$
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		$R_G = 2.4\Omega$
$t_f$	Fall Time	—	13	—		See Fig. 22
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 200V, V_{GS} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	770	—	$\mu J$	$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DD} = 200V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	1380	—		$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DD} = 200V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	4480	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	400	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	100	—		$f = 1.0MHz$
$C_{oss\text{ eff.}}$	Effective Output Capacitance	—	270	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 200V$
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact : 
$L_S$	Internal Source Inductance	—	7.5	—		

**Avalanche Characteristics**

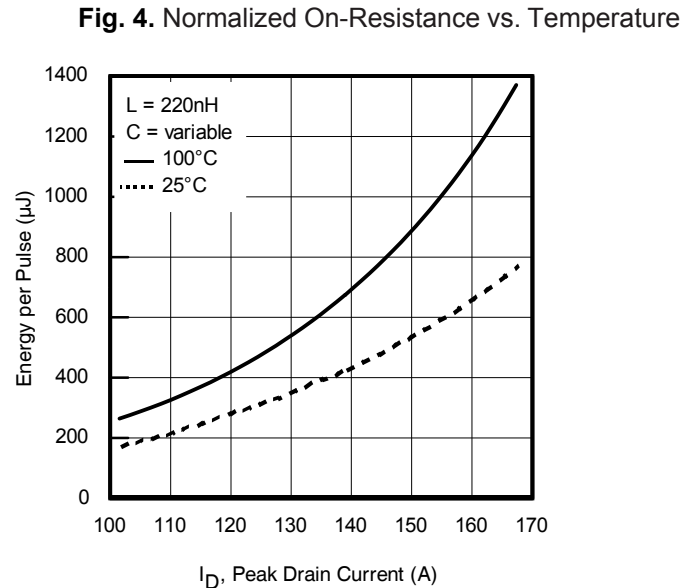
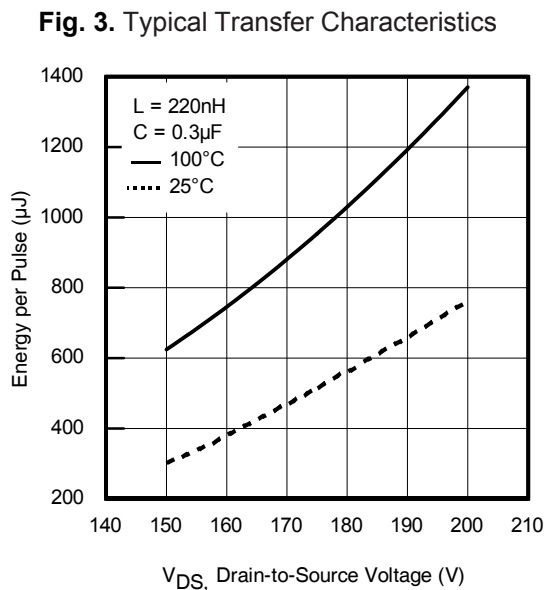
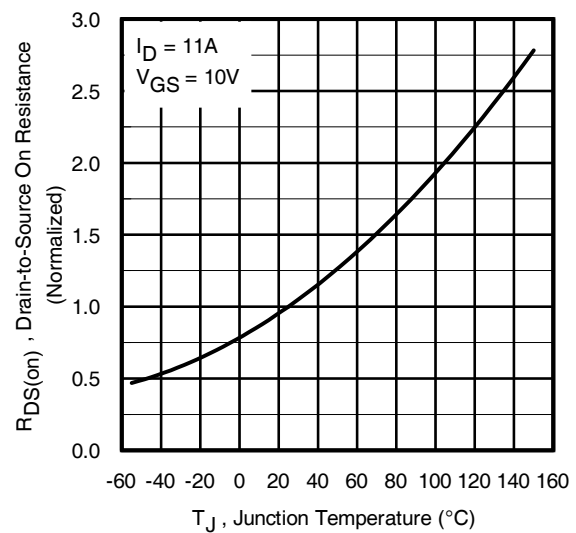
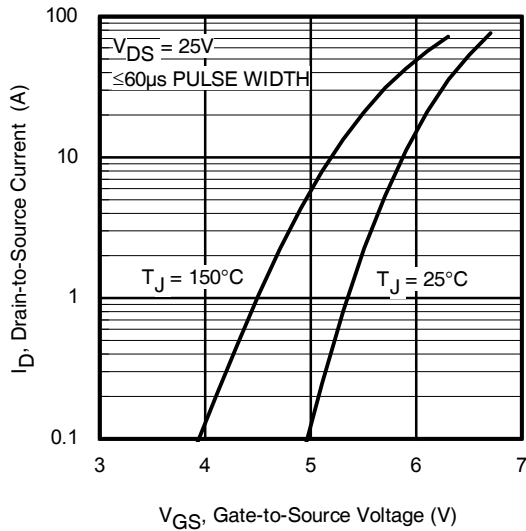
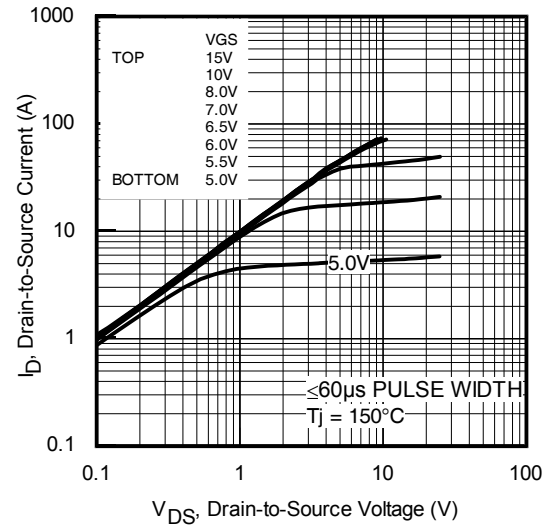
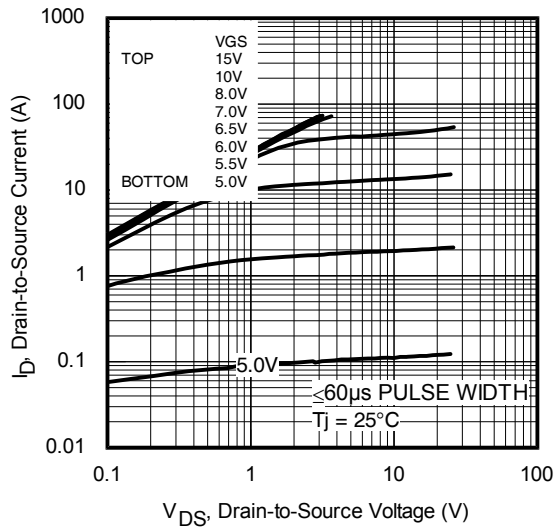
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	110	mJ
$E_{AR}$	Repetitive Avalanche Energy ①	—	4.6	
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	300	—	V
$I_{AS}$	Avalanche Current ②	—	11	A

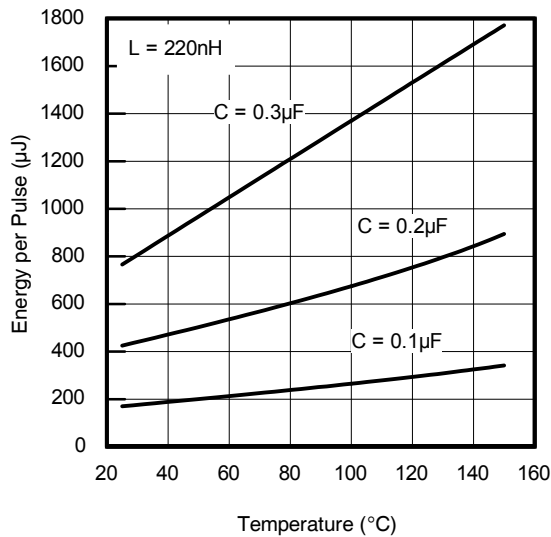
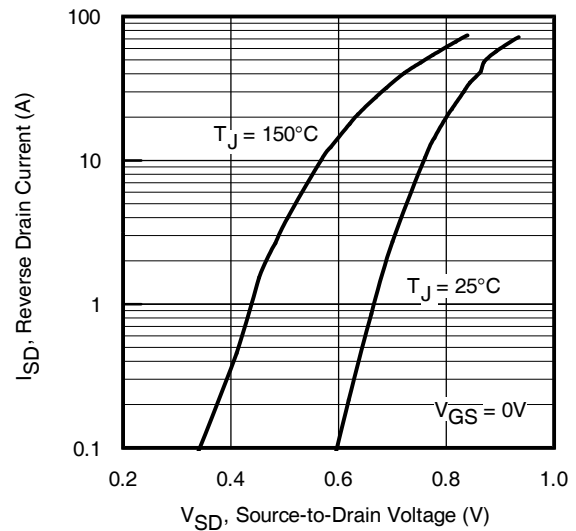
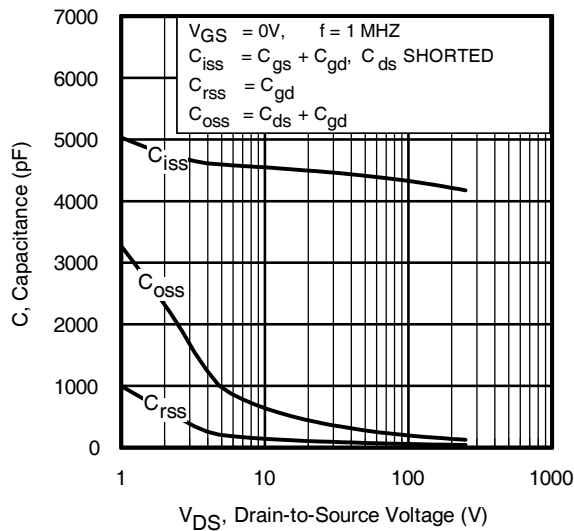
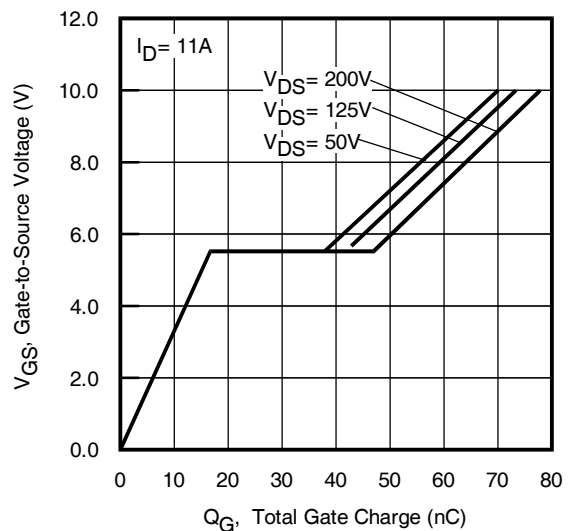
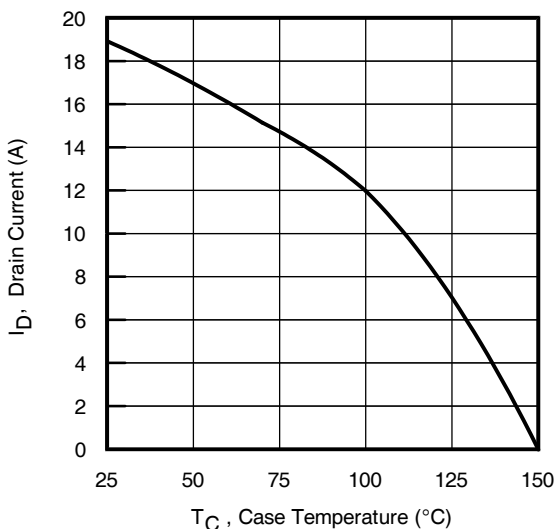
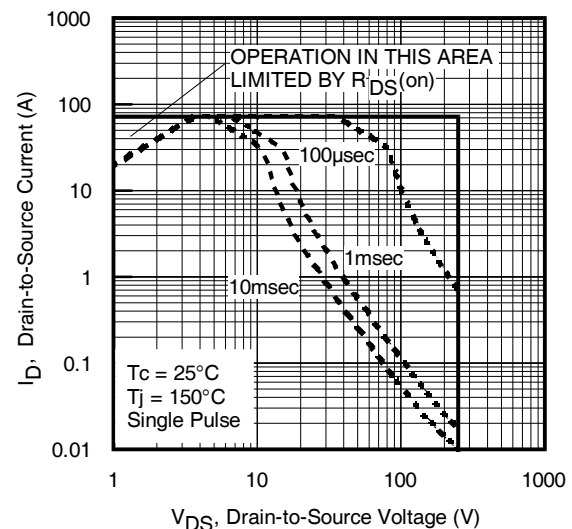
**Diode Characteristics**

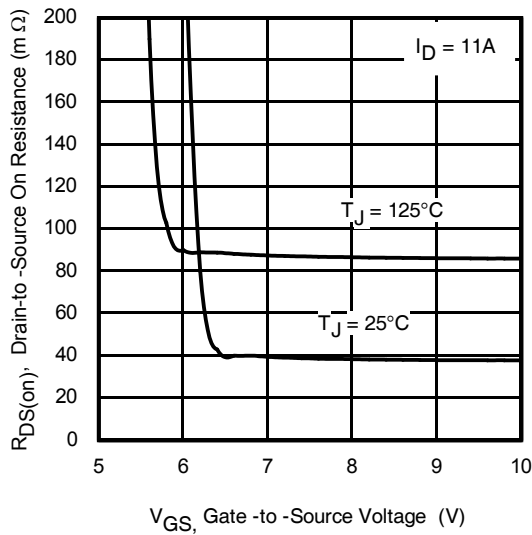
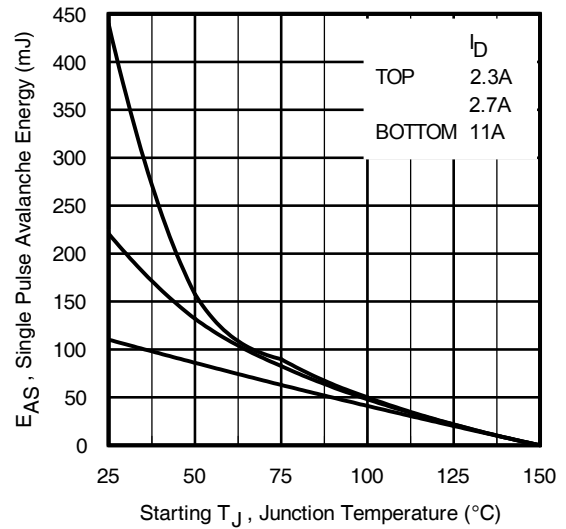
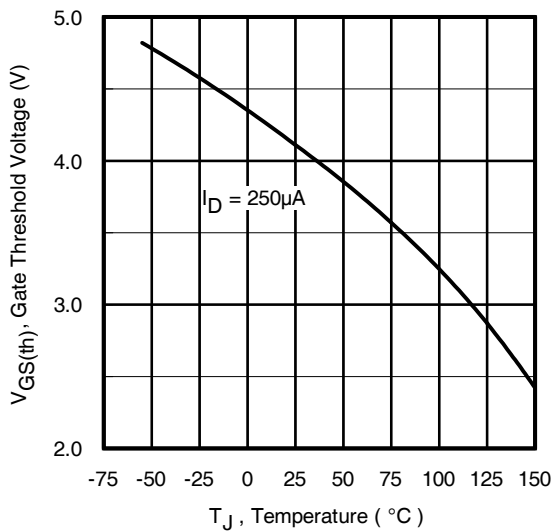
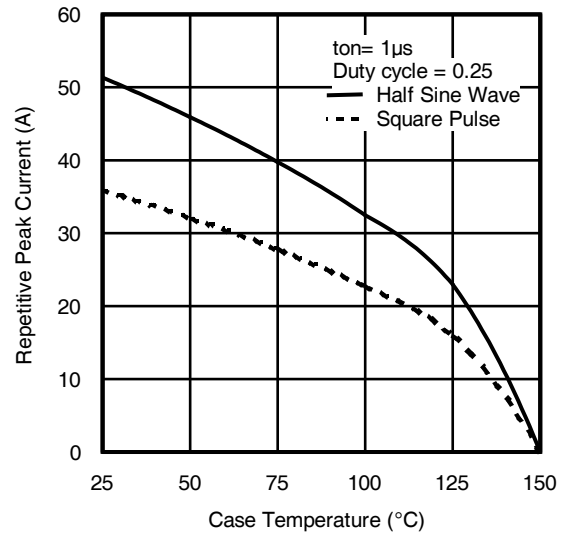
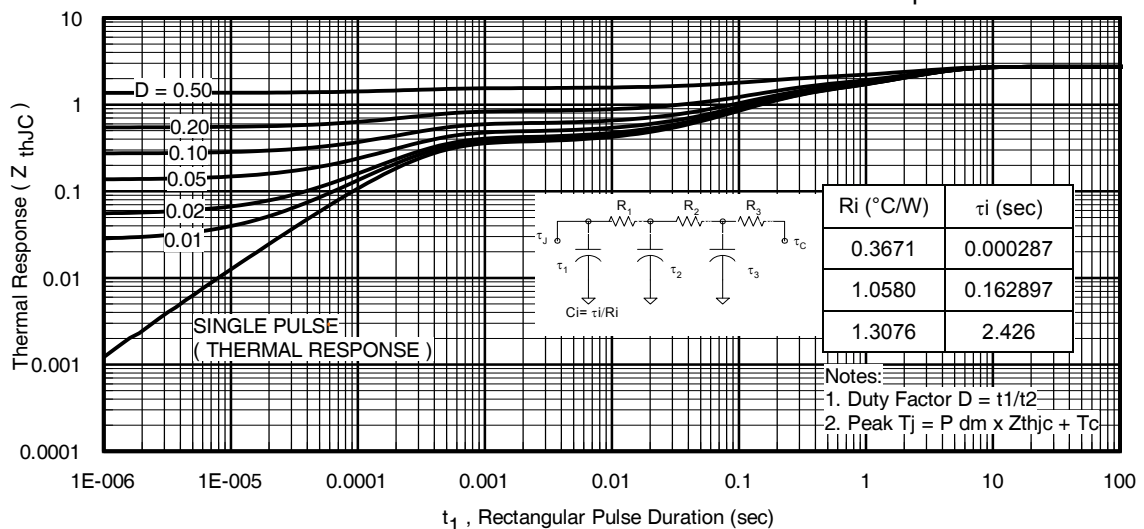
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	72		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	120	180	ns	$T_J = 25^\circ\text{C}, I_F = 11A, V_{DD} = 50V$
$Q_{rr}$	Reverse Recovery Charge	—	540	810	nC	$di/dt = 100A/\mu s$ ③

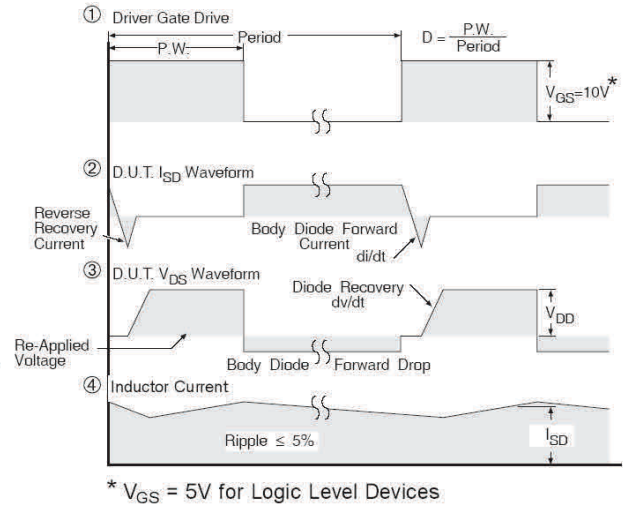
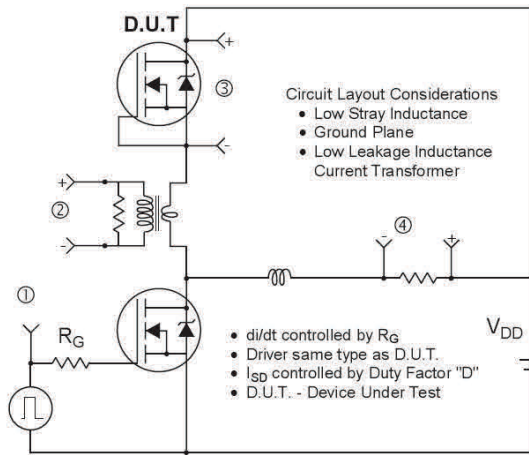
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.9mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 11A$ .
- ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ Half sine wave with duty cycle = 0.25,  $t_{on} = 1\mu sec$ .

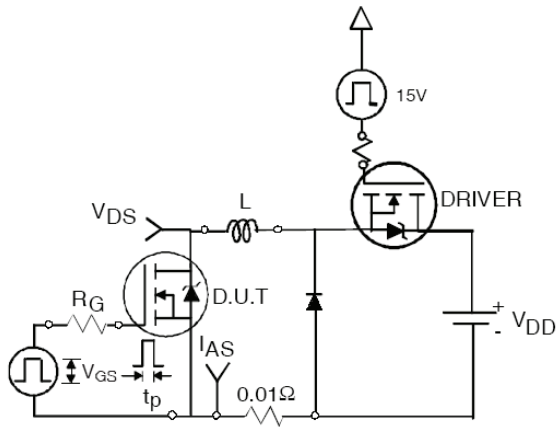



**Fig. 7.** Typical  $E_{PULSE}$  vs. Temperature

**Fig. 8.** Typical Source-Drain Diode Forward Voltage

**Fig. 9.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig. 10.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig. 11.** Maximum Drain Current vs. Case Temperature

**Fig. 12.** Maximum Safe Operating Area

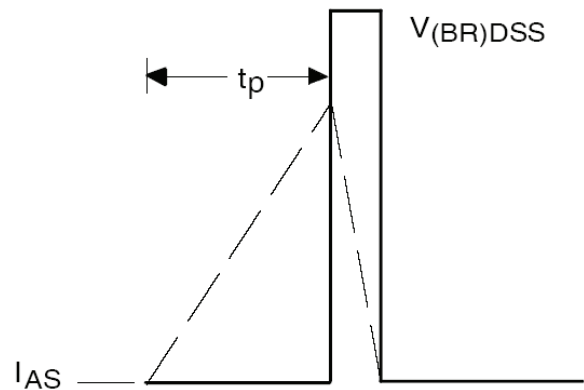

**Fig. 13.** On-Resistance Vs. Gate Voltage

**Fig. 14.** Maximum Avalanche Energy Vs. Temperature

**Fig. 15.** Threshold Voltage vs. Temperature

**Fig. 16.** Typical Repetitive peak Current vs. Case temperature

**Fig 17.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



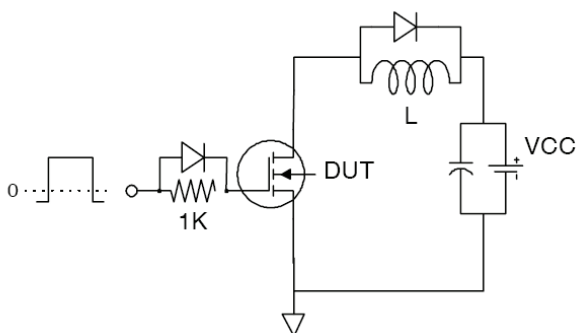
**Fig 18.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs



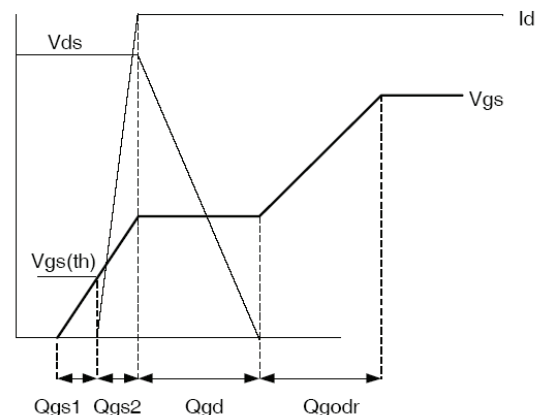
**Fig 19a.** Unclamped Inductive Test Circuit



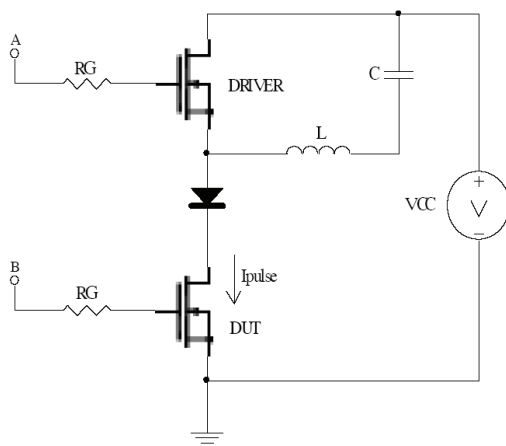
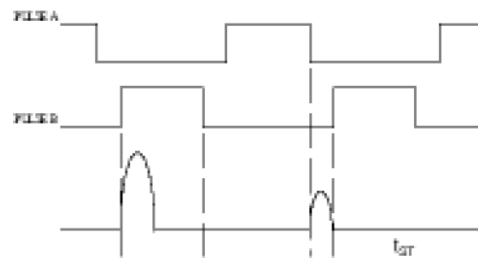
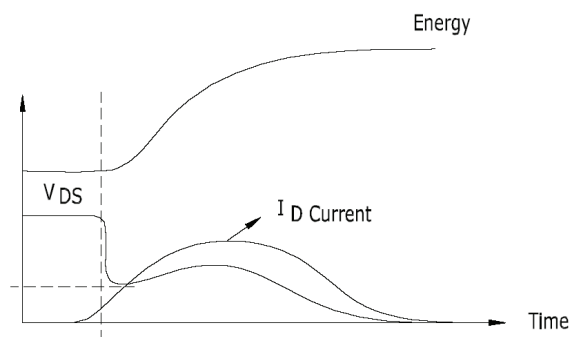
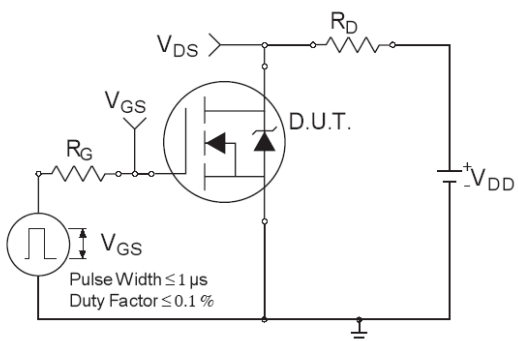
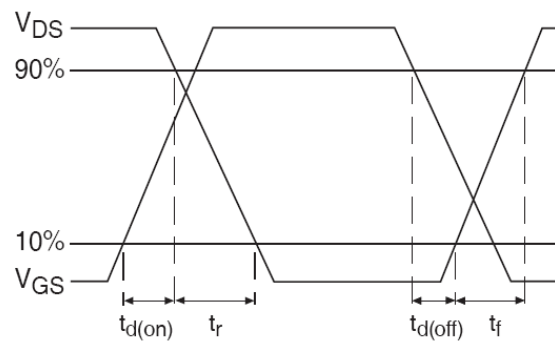
**Fig 19b.** Unclamped Inductive Waveforms

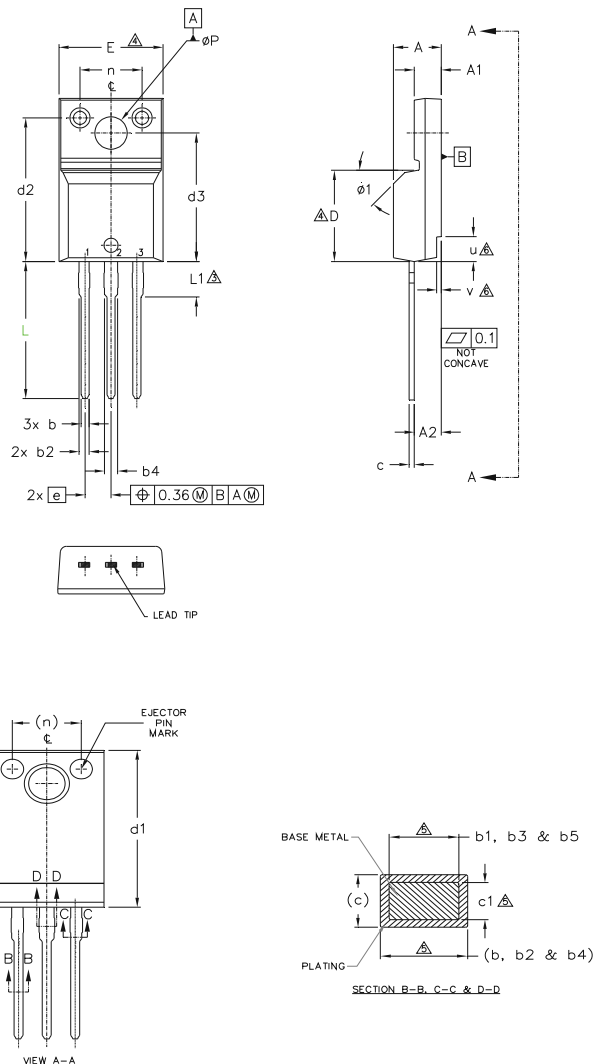


**Fig 20a.** Gate Charge Test Circuit



**Fig 20b.** Gate Charge Waveform


**Fig 21a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit

**Fig 21b.**  $t_{st}$  Test Waveforms

**Fig 21c.**  $E_{PULSE}$  Test Waveforms

**Fig 22a.** Switching Time Test Circuit

**Fig 22b.** Switching Time Waveforms

**TO-220 Full-Pak Package Outline** (Dimensions are shown in millimeters (inches))

**NOTES:**

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	5
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	5
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	5
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	5
c1	0.33	0.58	.013	.023	
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	4
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	4
e	2.54	BSC	.100	BSC	
L	13.21	13.72	.520	.540	3
L1	3.10	3.68	.122	.145	
n	6.05	6.60	.238	.260	
øP	3.05	3.45	.120	.136	6
u	2.39	2.49	.094	.098	
v	0.41	0.51	.016	.020	6
ø1	—	45°	—	45°	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

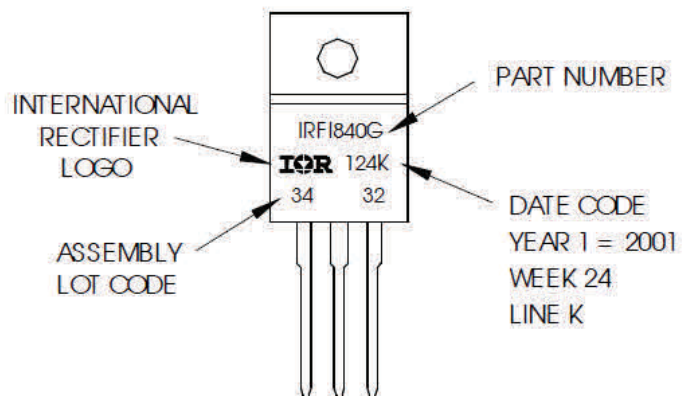
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

**TO-220 Full-Pak Part Marking Information**

**EXAMPLE:** THIS IS AN IRFI840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24, 2001  
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>



## Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) <sup>†</sup>	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
RoHS Compliant	Yes	

<sup>†</sup> Applicable version of JEDEC standard at the time of product release.

## Revision History

Date	Comments
04/27/2017	<ul style="list-style-type: none"> <li>Changed datasheet with Infineon logo - all pages.</li> <li>Corrected Package Outline on page 8.</li> <li>Added disclaimer on last page.</li> </ul>

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**Document reference**  
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