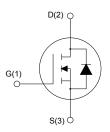


N-channel 250 V, 41 m Ω typ., 45 A STripFET II Power MOSFET in a TO-220FP package





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STPOWER

Product status link STF75NF25

Product summary			
Order code	STF75NF25		
Marking	75NF25		
Package	TO-220FP		
Packing	Tube		

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF75NF25	250 V	50 mΩ	45 A	31 W

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V _{GS}	Gate-source voltage	±25	V
. (1)	Drain current (continuous) at T _C = 25 °C	45	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	28	_ A
I _{DM} (2)	Drain current (pulsed)	150	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	31	W
dv/dt (3)	Peak diode recovery voltage slope	12	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	40	V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2.5	kV
TJ	T _J Operating junction temperature range		°C
T _{stg}	Storage temperature range	-55 to 150	

- 1. Limited by maximum junction temperature.
- 2. Pulse width limited by safe operating area.
- 3. $I_{SD} \le 45~A,~di/dt \le 400~A/\mu s,~V_{DS~(peak)} \le V_{(BR)DSS},~V_{DD} = 80\%~V_{(BR)DSS}.$
- 4. $V_{DS} \le 200 \ V$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	4	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	29	Α
E _{AS} ⁽¹⁾	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	416	mJ

Energy during avalanche per single pulse is defined as the maximum energy that can be dissipated in the device, during a single avalanche operation, at the I_{AR} and initial junction temperature of 25 °C, to bring the junction temperature to the maximum value of 150 °C.

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	250			V
I	Zana mata waltana duain ayunant	V _{GS} = 0 V, V _{DS} = 250 V			1	μA
I _{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 250 V, T_{C} = 125 °C ⁽¹⁾			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 22.5 A		41	50	mΩ

^{1.} Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	3084	-	pF
C _{oss}	utput capacitance $V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$		-	263	-	pF
C _{rss}	Reverse transfer capacitance		-	44	-	pF
Coss eq. (1)	Equivalent output capacitance V_{DS} = 0 to 200 V, V_{GS} = 0 V	-	338	-	pF	
Rg	Gate input resistance	$f = 1$ MHz, $I_D = 0$ A $V_{DD} = 200$ V, $I_D = 45$ A, $V_{GS} = 0$ to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	1.7	-	Ω
Qg	Total gate charge		-	88	-	nC
Q _{gs}	Gate-source charge		-	20	-	nC
Q _{gd}	Gate-drain charge		-	43	-	nC

C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 125 V, I _D = 22.5 A,	-	23	-	ns
t _r	Rise time	R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	35	-	ns
t _{d(off)}	Turn-off delay time		-	57	-	ns
t _f	Fall time		-	17	-	ns

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Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		45	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		150	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 45 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 45 A, di/dt = 100 A/μs,	-	212		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 200 V	-	2.07		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	16.5		Α
t _{rr}	Reverse recovery time	I _{SD} = 45 A, di/dt = 100 A/μs,	-	280		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 200 V, T _J = 150 °C	-	3.5		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	21		Α

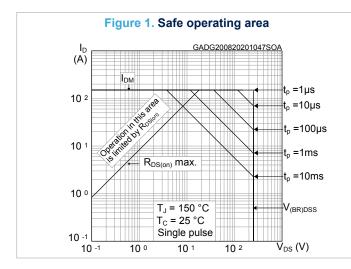
^{1.} Pulse width limited by safe operating area.

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^{2.} Pulsed: pulse duration = $300 \mu s$, duty cycle 1.5%.



2.1 Electrical characteristics (curves)



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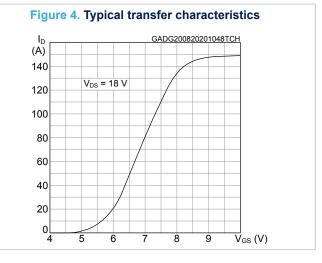
10 -6

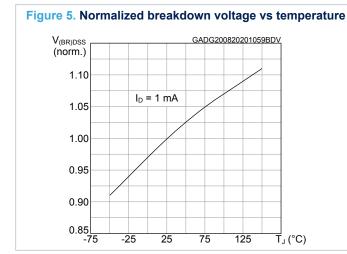
10 -6

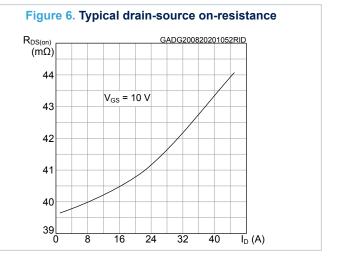
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Figure 3. Typical output characteristics GADG200820201048OCH Ι_D (A) V_{GS} = 9,10 V 140 8 V 120 100 80 60 40 6 V 20 8 12 16 $\vec{V}_{DS}(V)$







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Figure 7. Typical gate charge characteristics

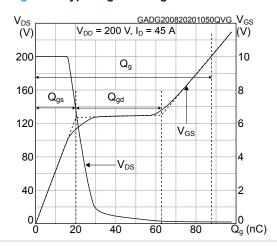


Figure 8. Typical capacitance characteristics

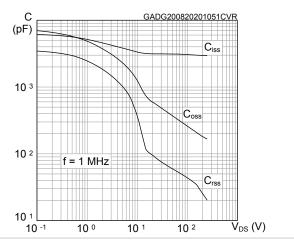


Figure 9. Normalized gate threshold vs temperature

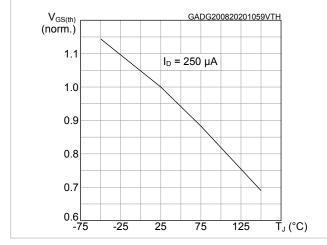


Figure 10. Normalized on-resistance vs temperature

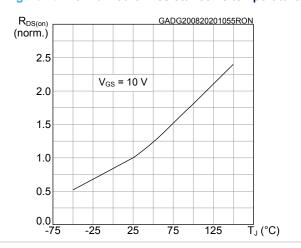


Figure 11. Typical reverse diode forward characteristics

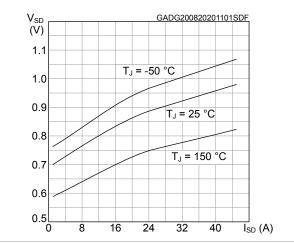
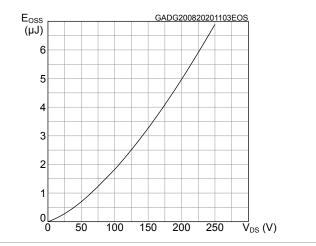


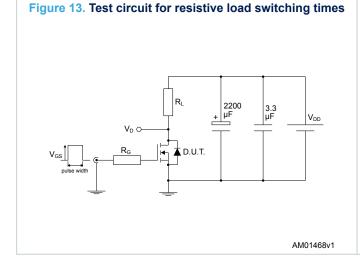
Figure 12. Typical output capacitance stored energy



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3 Test circuits



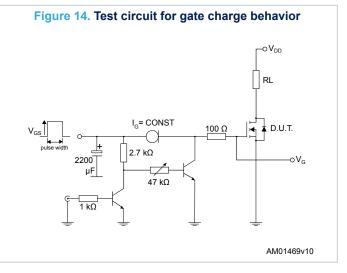
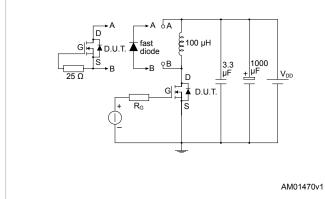


Figure 15. Test circuit for inductive load switching and diode recovery times



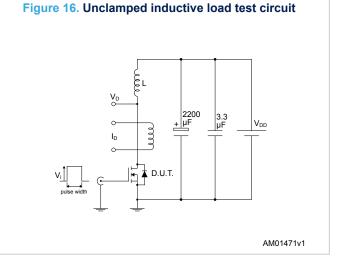


Figure 17. Unclamped inductive waveform

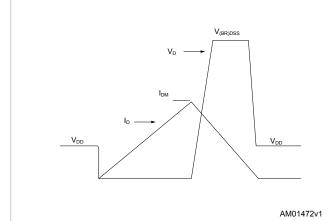
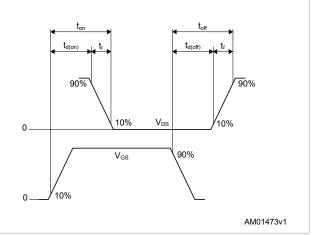


Figure 18. Switching time waveform



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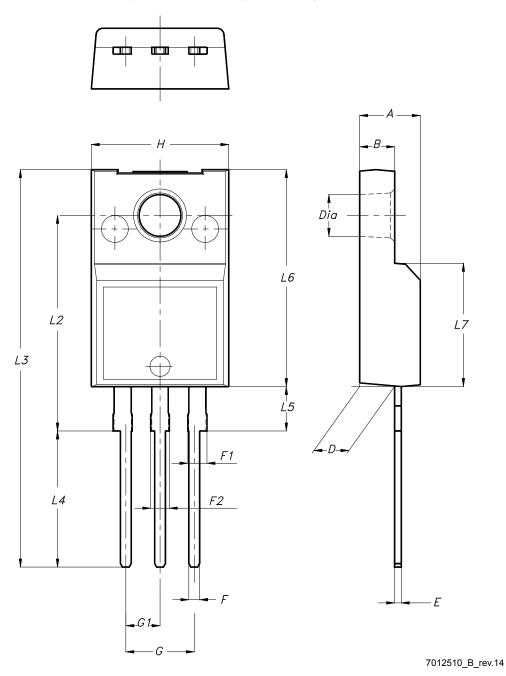


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline



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Table 8. TO-220FP type B package mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
А	4.40		4.60
В	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
Н	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

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Revision history

Table 9. Document revision history

Date	Version	Changes
04-Apr-2019	1	First release.
		Updated Title and Features in cover page.
		Updated Section 1 Electrical ratings.
21-Aug-2020	2	Updated Section 2 Electrical characteristics.
		Added Section 2.1 Electrical characteristics (curves).
		Updated Figure 14. Test circuit for gate charge behavior.
		Updated Table 2. Thermal data, Table 3. Avalanche characteristics.
09-Oct-2023	3	Updated Figure 1. Safe operating area.
		Updated Section 4.1 TO-220FP type B package information.

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