

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

SSM3J35MFV

○ High-Speed Switching Applications

○ Analog Switch Applications

- 1.2 V drive
- Low ON-resistance : $R_{on} = 44 \Omega$ (max) (@ $V_{GS} = -1.2$ V)
 : $R_{on} = 22 \Omega$ (max) (@ $V_{GS} = -1.5$ V)
 : $R_{on} = 11 \Omega$ (max) (@ $V_{GS} = -2.5$ V)
 : $R_{on} = 8 \Omega$ (max) (@ $V_{GS} = -4.0$ V)

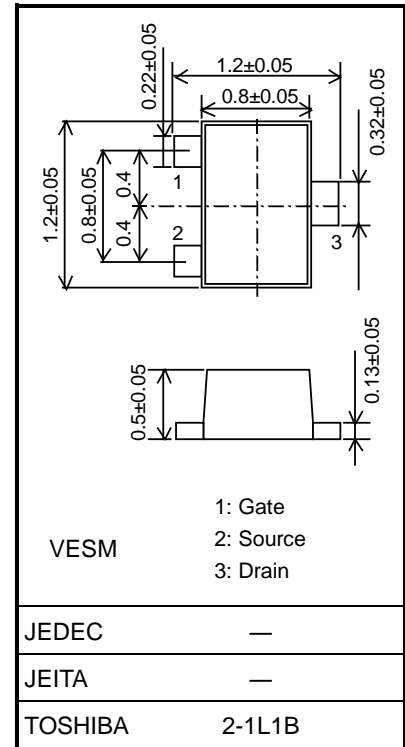
Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 10	V
Drain current	DC	I_D	mA
	Pulse	I_{DP}	
Drain power dissipation	P_D (Note 1)	150	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

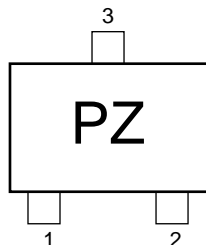
Note 1: Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm²)

Unit: mm

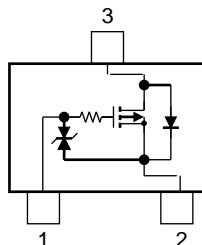


Weight: 1.5 mg (typ.)

Marking



Equivalent Circuit (top view)



Start of commercial production
2008-01

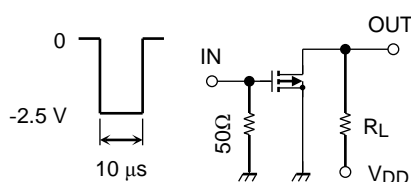
Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 10\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -0.1\text{ mA}, V_{GS} = 0\text{ V}$	-20	—	—	V
Drain cutoff current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	—	—	-1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3\text{ V}, I_D = -1\text{ mA}$	-0.4	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -50\text{ mA}$ (Note 2)	77	—	—	mS
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -50\text{ mA}, V_{GS} = -4\text{ V}$ (Note 2)	—	4.3	8	Ω
		$I_D = -50\text{ mA}, V_{GS} = -2.5\text{ V}$ (Note 2)	—	5.6	11	
		$I_D = -5\text{ mA}, V_{GS} = -1.5\text{ V}$ (Note 2)	—	8.2	22	
		$I_D = -2\text{ mA}, V_{GS} = -1.2\text{ V}$ (Note 2)	—	11	44	
Input capacitance	C_{iss}	$V_{DS} = -3\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	12.2	—	pF
Reverse transfer capacitance	C_{rss}		—	6.5	—	
Output capacitance	C_{oss}		—	10.4	—	
Switching time	Turn-on time	$V_{DD} = -3\text{ V}, I_D = -50\text{ mA},$	—	175	—	ns
	Turn-off time	$V_{GS} = 0\text{ to }-2.5\text{ V}$	—	251	—	
Drain-source forward voltage	V_{DSF}	$I_D = 100\text{ mA}, V_{GS} = 0\text{ V}$ (Note 2)	—	0.83	1.2	V

Note 2: Pulse test

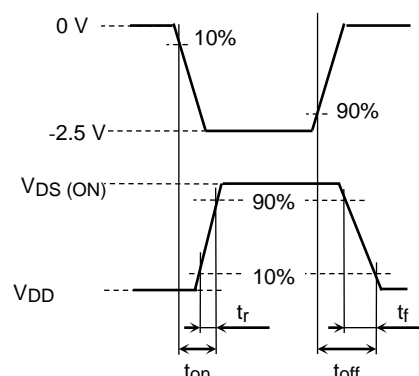
Switching Time Test Circuit

(a) Test Circuit



$V_{DD} = -3\text{ V}$
Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
($Z_{out} = 50\ \Omega$)
Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



(c) V_{OUT}

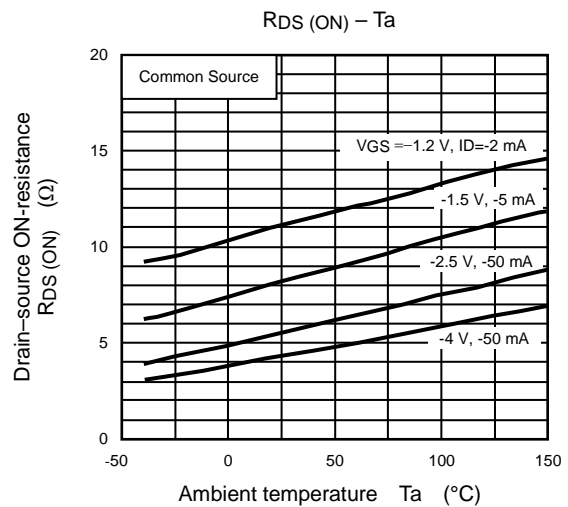
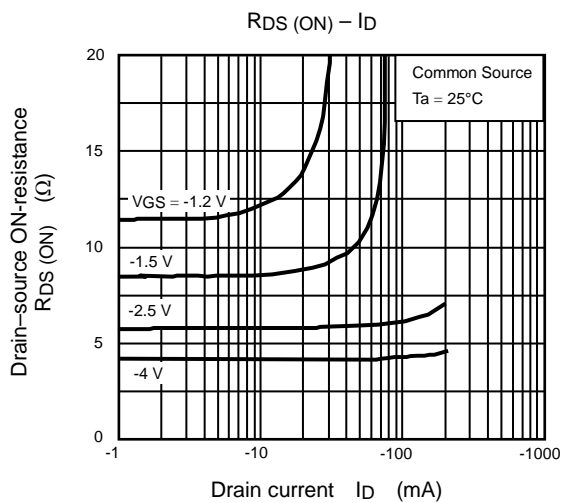
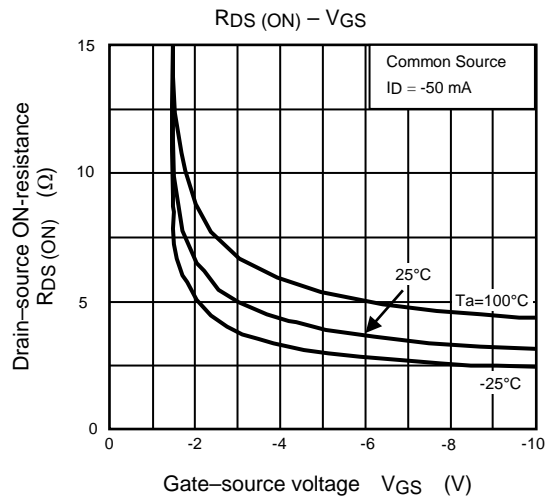
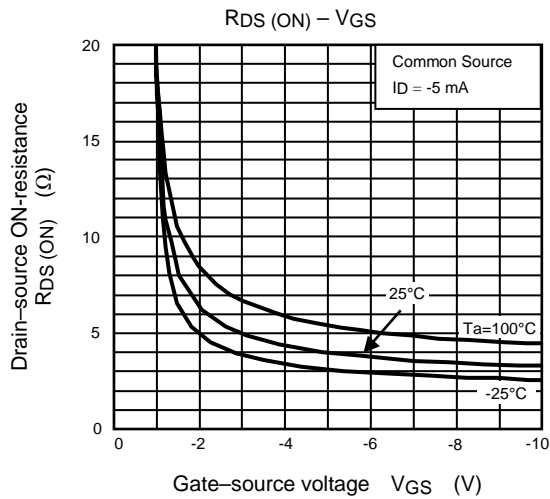
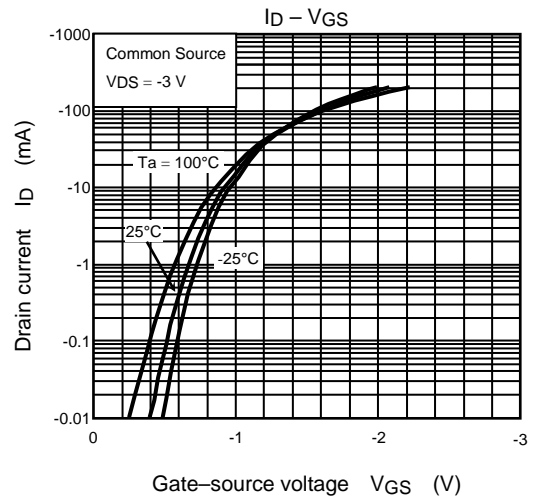
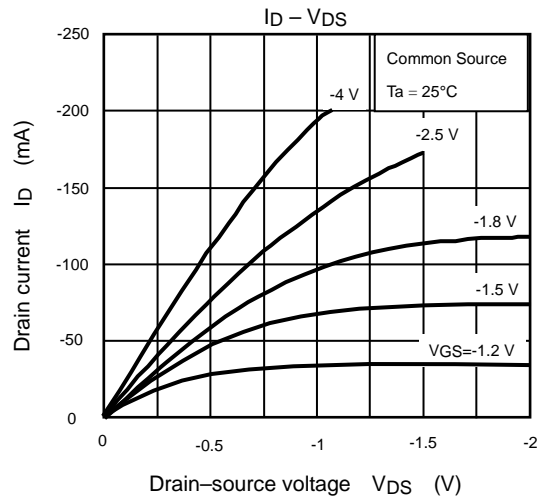
Usage Considerations

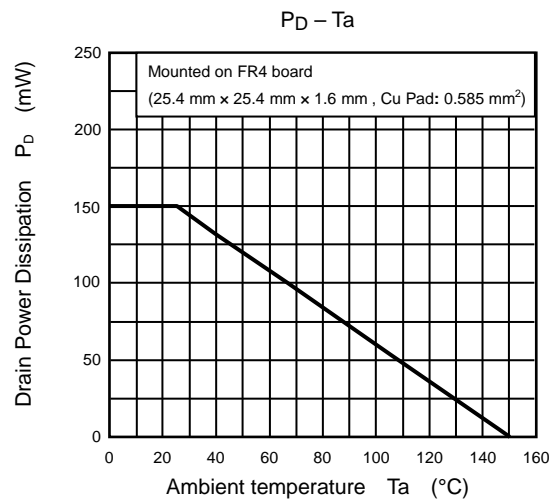
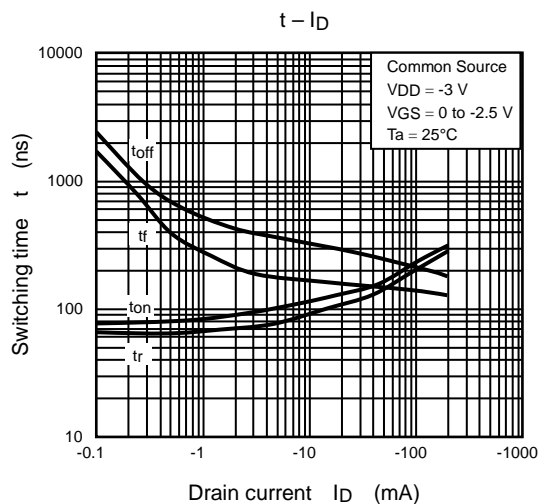
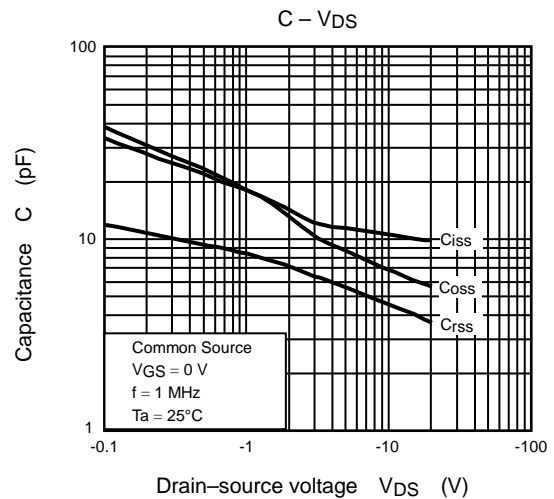
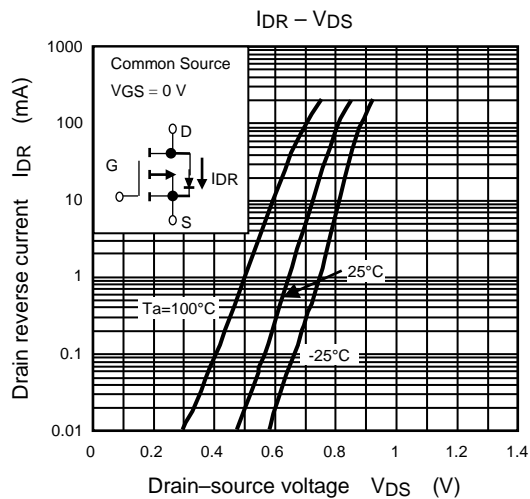
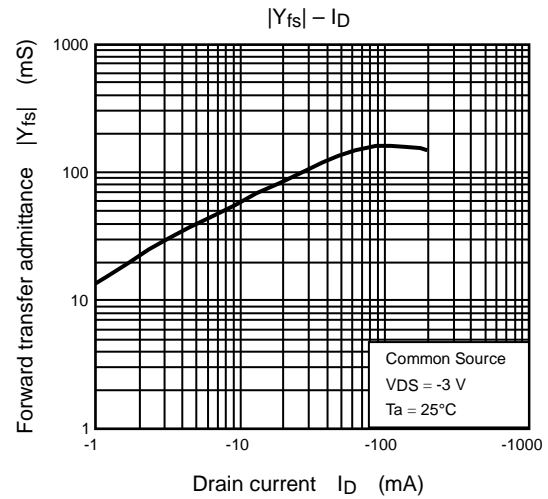
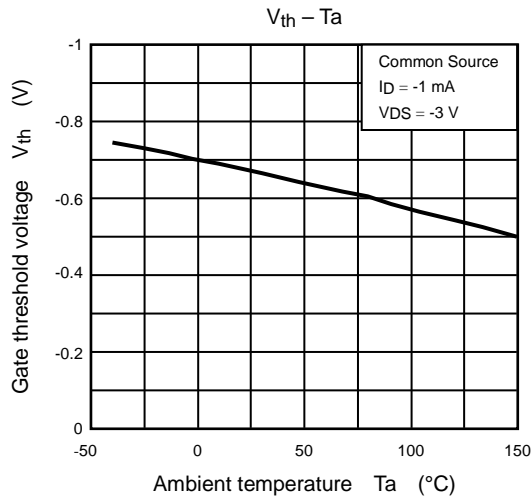
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM3J35MFV). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.





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