

# MOSFET – N-Channel, UltraFET Trench

200 V, 3.9 A, 70 mΩ

## FDS2672

### General Description

This single N-Channel MOSFET is produced using onsemi's advanced UltraFET Trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- Max  $r_{DS(on)}$  = 70 mΩ at  $V_{GS} = 10$  V,  $I_D = 3.9$  A
- Max  $r_{DS(on)}$  = 80 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.5$  A
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- These Device is Pb-Free, Halide Free and are RoHS Compliant

### Applications

- DC-DC Conversion

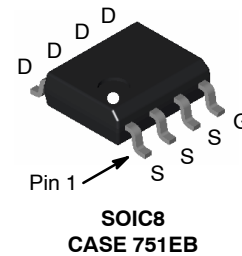
### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	200	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	3.9 50	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	37.5	mJ
$P_D$	Power Dissipation (Note 1a) (Note 1b)	2.5 1.0	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

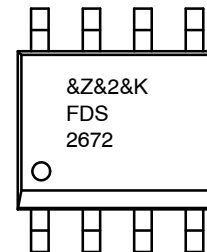
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	50 125	$^\circ\text{C/W}$

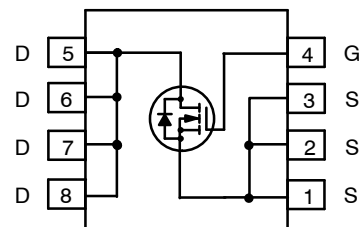


### MARKING DIAGRAM



&Z = Assembly Plant Code  
 &2 = Numeric Date Code  
 &K = Lot Code  
 FDS2672 = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping
FDS2672	SOIC8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

**ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	200	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	206	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\ \text{V}$ , $V_{GS} = 0\ \text{V}$ $V_{DS} = 200\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 55^\circ\text{C}$	–	–	1 10	$\mu\text{A}$
$I_{GSSF}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	$\pm 100$	nA

**ON CHARACTERISTICS** (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	–11	–	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 3.9\ \text{A}$ $V_{GS} = 6\ \text{V}$ , $I_D = 3.5\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $I_D = 3.9\ \text{A}$ , $T_J = 125^\circ\text{C}$	–	58 63 124	70 80 148	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}$ , $I_D = 3.9\ \text{A}$	–	15	–	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 100\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	–	1905	2535	pF
$C_{oss}$	Output Capacitance		–	100	135	pF
$C_{rss}$	Reverse Transfer Capacitance		–	30	45	pF
$R_g$	Gate Resistance	$f = 1\ \text{MHz}$	–	0.7	–	$\Omega$

**SWITCHING CHARACTERISTICS**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\ \text{V}$ , $I_D = 3.9\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GS} = 6\ \Omega$	–	22	35	ns
$t_r$	Rise Time		–	10	20	ns
$t_{d(off)}$	Turn-Off Delay Time		–	35	56	ns
$t_f$	Fall Time		–	10	20	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{DS} = 100\ \text{V}$ , $I_D = 3.9\ \text{A}$	–	33	46	nC
$Q_{gs}$	Gate to Source Gate Charge		–	11	–	nC
$Q_{gd}$	Gate to Drain Charge		–	7	–	nC

**DRAIN-SOURCE DIODE CHARACTERISTICS**

$V_{SD}$	Source to Drain Diode Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 3.9\ \text{A}$	–	0.75	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.9\ \text{A}$ , $dI_F / dI = 100\ \text{A}/\mu\text{s}$	–	67	101	ns
$Q_{rr}$	Reverse Recovery Charge		–	179	269	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  (10 s)  $62.5^\circ\text{C}/\text{W}$   
steady state when mounted on  
a 1 in<sup>2</sup> pad of 2 oz copper.



b)  $125^\circ\text{C}/\text{W}$  when mounted  
on a minimum pad.

Scale 1:1 on letter size paper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2%.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\ \text{mH}$ ,  $I_{AS} = 5\ \text{A}$ ,  $V_{DD} = 100\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

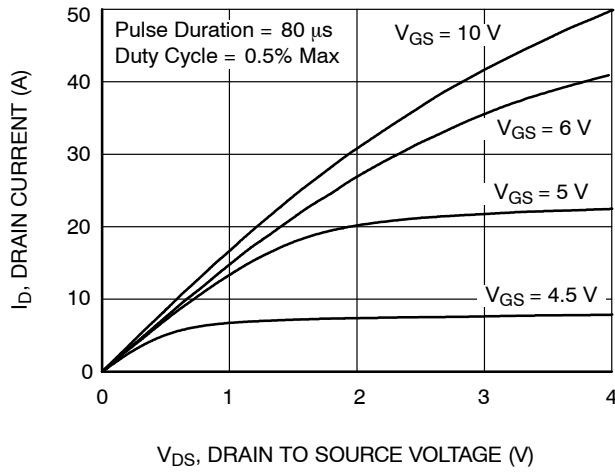
TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

Figure 1. On-Region Characteristics

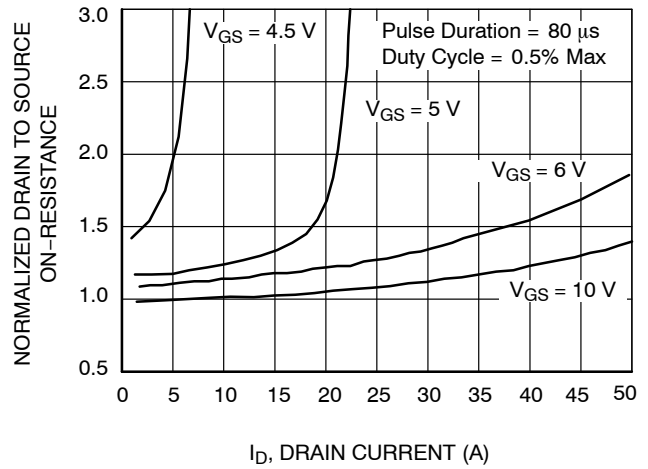


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

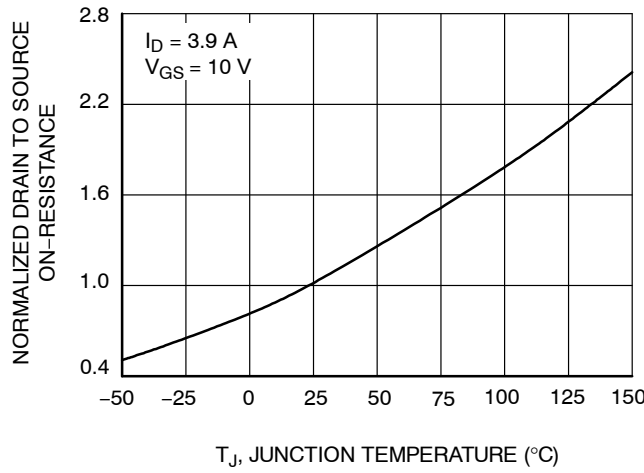


Figure 3. Normalized On-Resistance vs. Junction Temperature

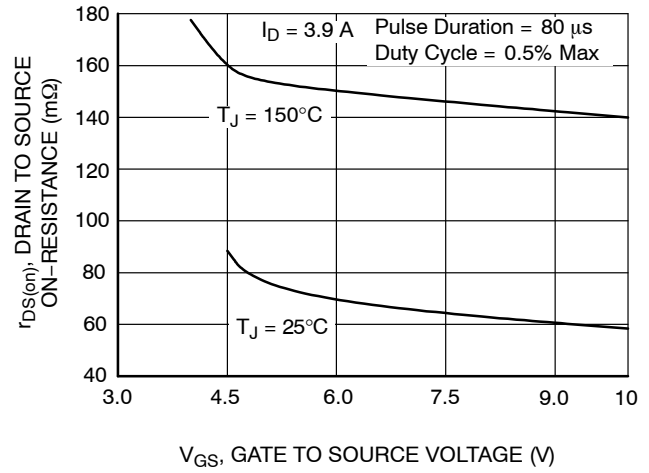


Figure 4. On-Resistance vs. Gate to Source Voltage

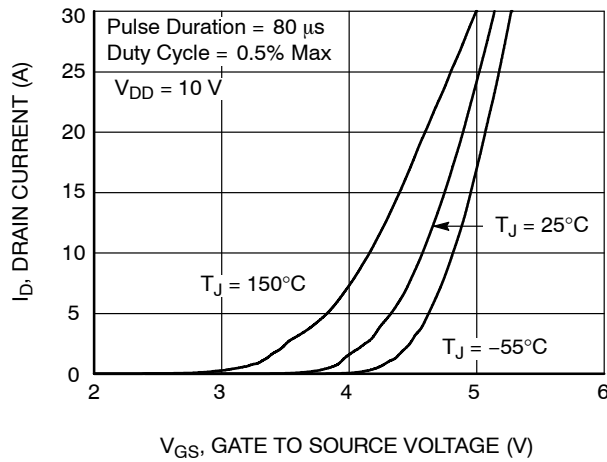


Figure 5. Transfer Characteristics

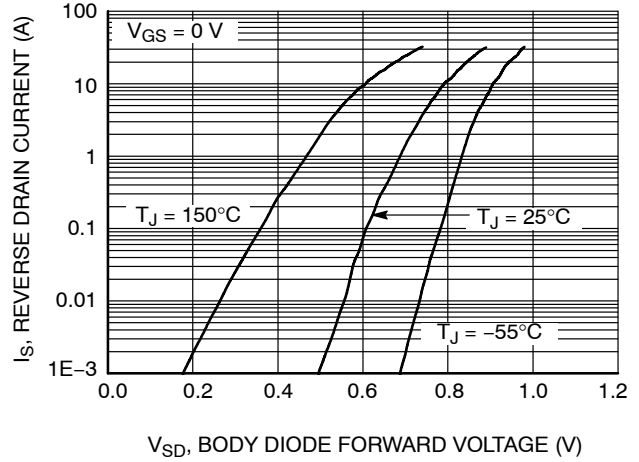
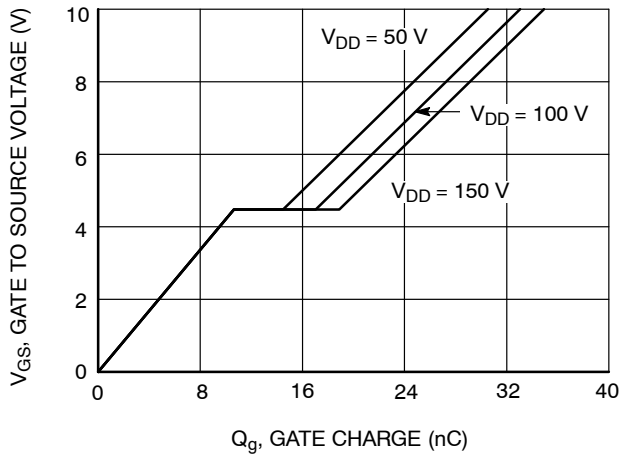
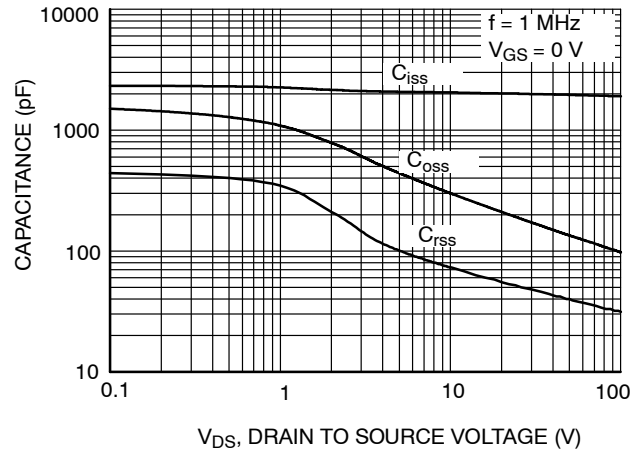


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

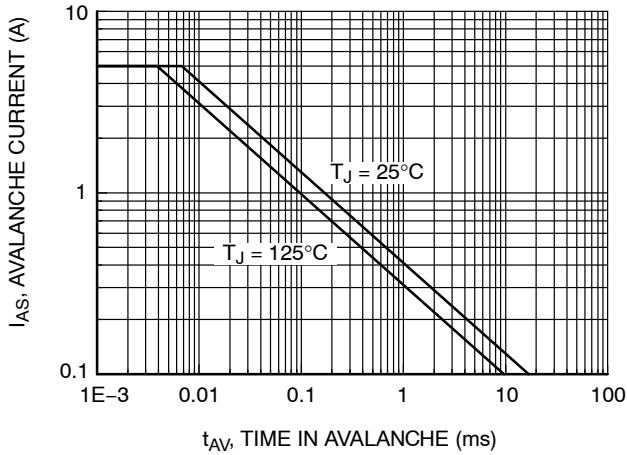
**TYPICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED) (CONTINUED)



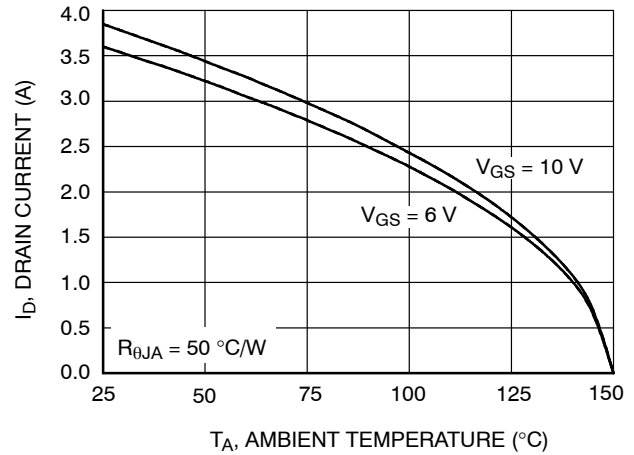
**Figure 7. Gate Charge Characteristics**



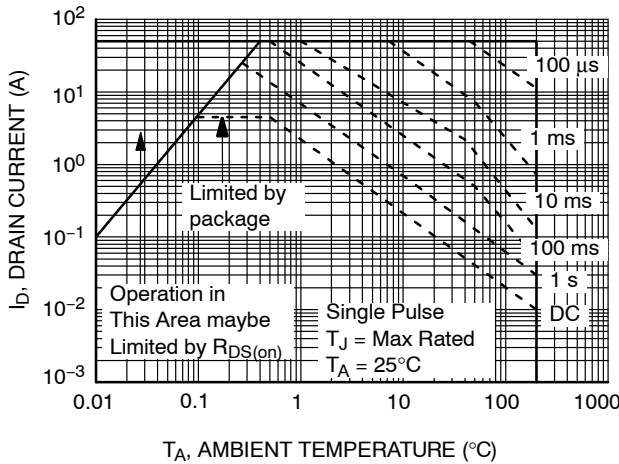
**Figure 8. Capacitance vs. Drain to Source Voltage**



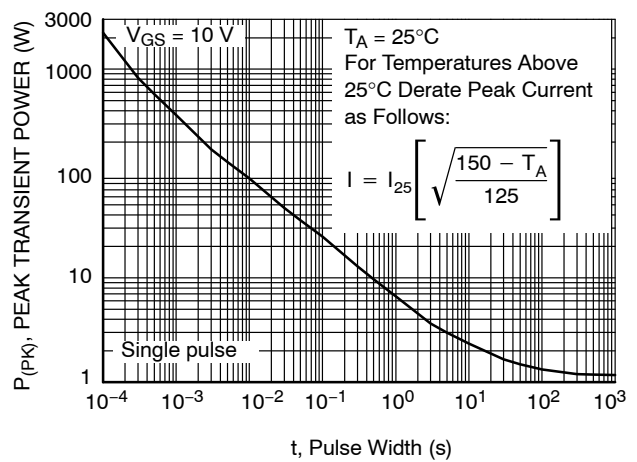
**Figure 9. Unclamped Inductive Switching Capability**



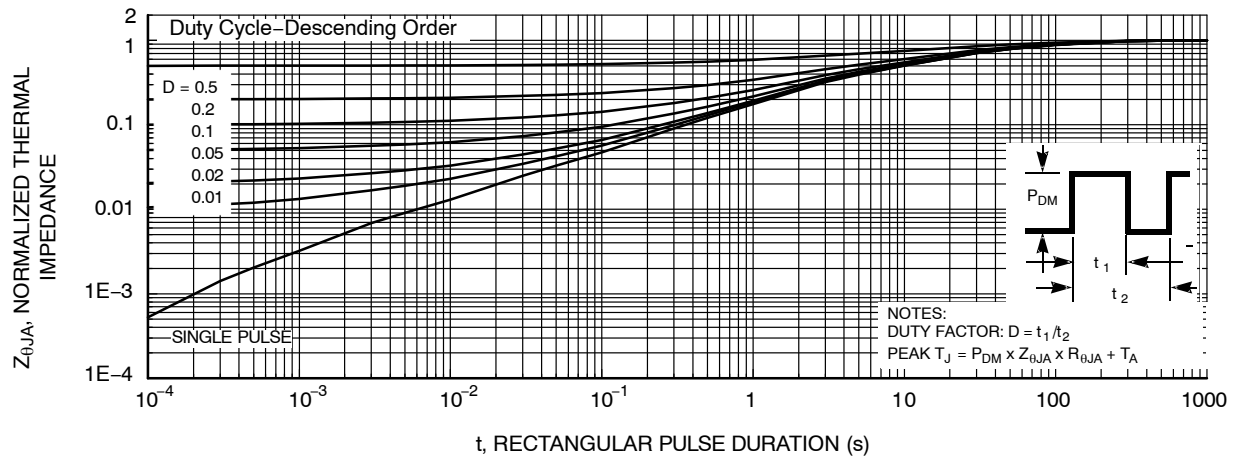
**Figure 10. Ambient Continuous Drain Current vs Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



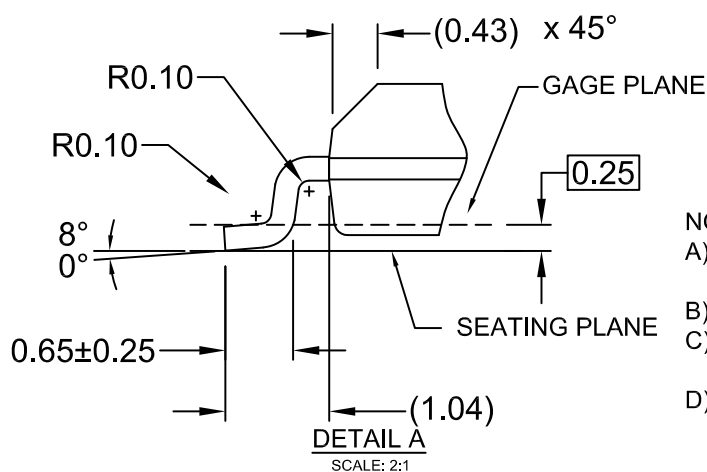
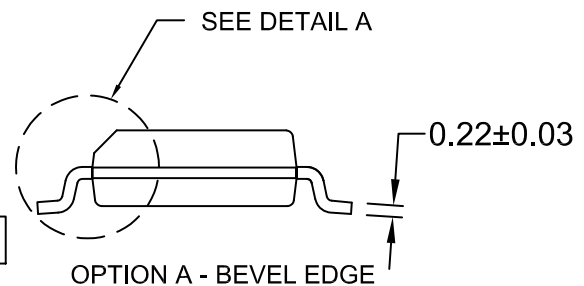
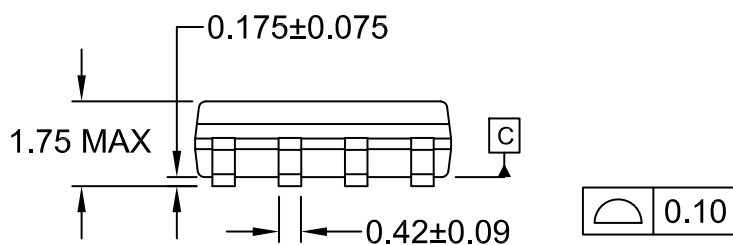
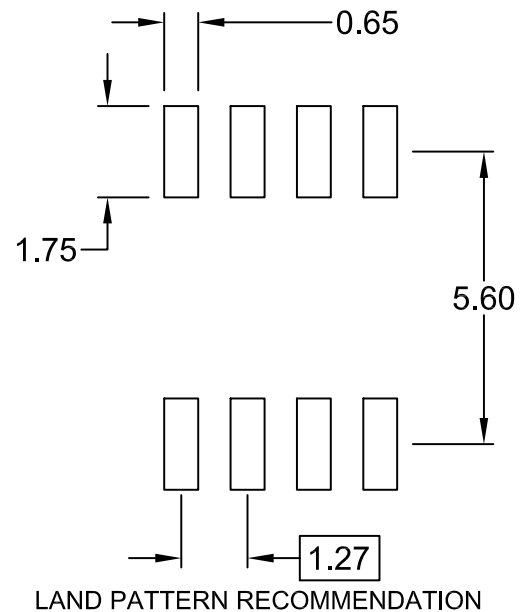
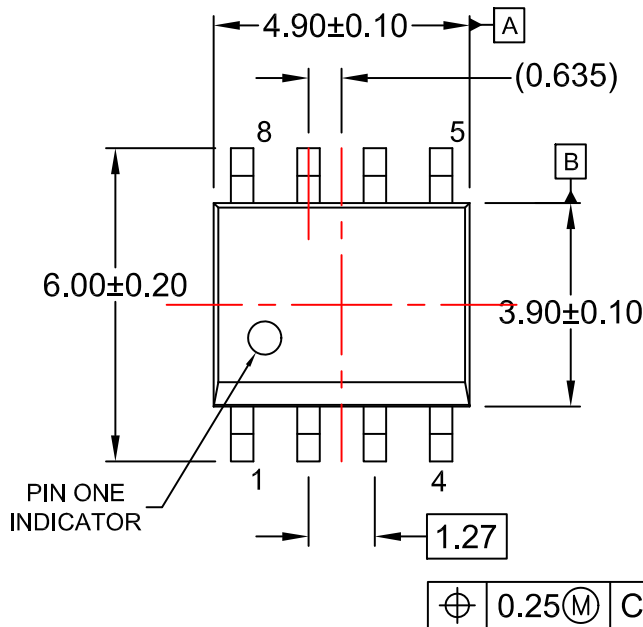
**Figure 12. Single Pulse Maximum Power Dissipation**

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED) (CONTINUED)**Figure 13. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1b.  
 Transient thermal response will change depending on the circuit board design.

**SOIC8**  
**CASE 751EB**  
**ISSUE A**

DATE 24 AUG 2017



**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

<b>DOCUMENT NUMBER:</b>	<b>98AON13735G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC8</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)