

## Applications

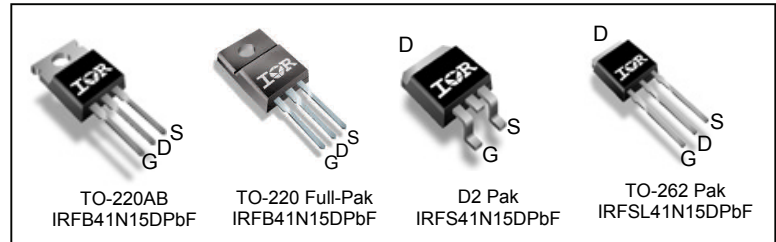
- High frequency DC-DC converters

## Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

HEXFET® Power MOSFET

$V_{DS}$	150V
$R_{DS(on)}$ max	0.045 $\Omega$
$I_D$	41A



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB41N15DPbF	TO-220	Tube	50	IRFB41N15DPbF
IRFSL41N15DPbF	TO-262	Tube	50	IRFSL41N15DPbF
IRFIB41N15DPbF	TO-220 Full-Pak	Tube	50	IRFIB41N15DPbF
IRFS41N15DPbF	D2-Pak	Tube	50	IRFS41N15DPbF
		Tape and Reel Left	800	IRFS41N15DTRLpbF

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	41	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	29	
$I_{DM}$	Pulsed Drain Current ①	164	
$P_D$ @ $T_A = 25^\circ\text{C}$	Maximum Power Dissipation D2-Pak	3.1	W
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation TO-220	200	
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation TO-220 Full-Pak	48	
	Linear Derating Factor TO-220	1.3	W/ $^\circ\text{C}$
	Linear Derating Factor TO-220 Full-Pak	0.32	
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	2.7	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case, TO-220 Full-Pak	—	3.14	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient, D2-Pak ⑦	—	40	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 Full-Pak	—	65	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.045	$\Omega$	$V_{GS} = 10V, I_D = 25A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

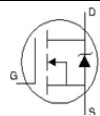
**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

$g_{fs}$	Forward Trans conductance	18	—	—	S	$V_{DS} = 50V, I_D = 25A$
$Q_g$	Total Gate Charge	—	72	110	nC	$I_D = 25A$
$Q_{gs}$	Gate-to-Source Charge	—	21	31		$V_{DS} = 120V$
$Q_{gd}$	Gate-to-Drain Charge	—	35	52		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 75V$
$t_r$	Rise Time	—	63	—		$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	14	—		$V_{GS} = 10V$ ④
$C_{iss}$	Input Capacitance	—	2520	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	510	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	110	—		$f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	3090	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	230	—		$V_{GS} = 0V, V_{DS} = 120V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	250	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤

**Avalanche Characteristics**

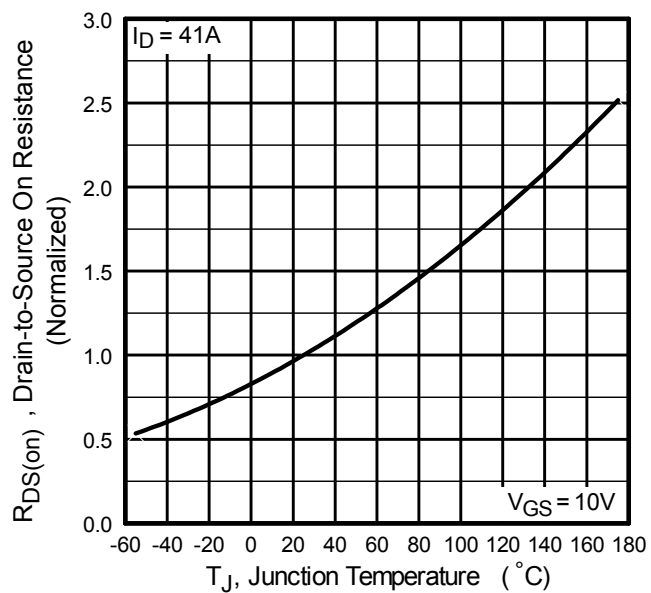
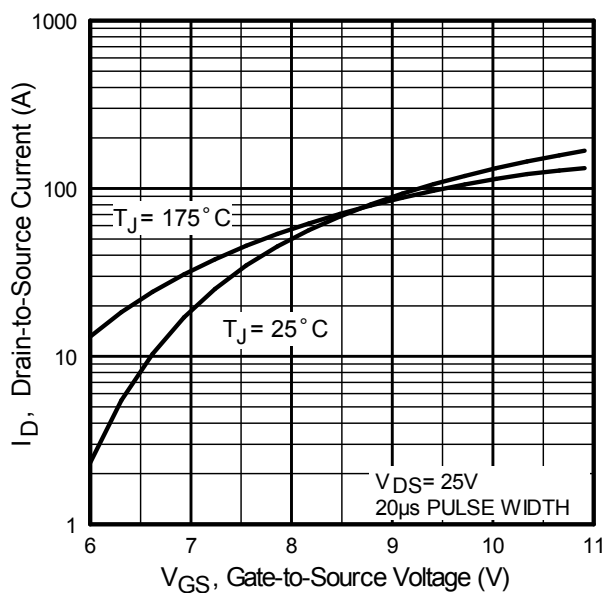
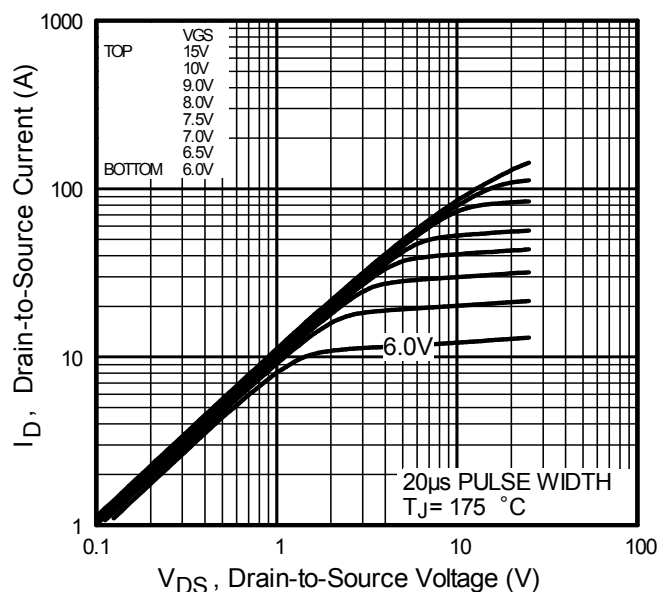
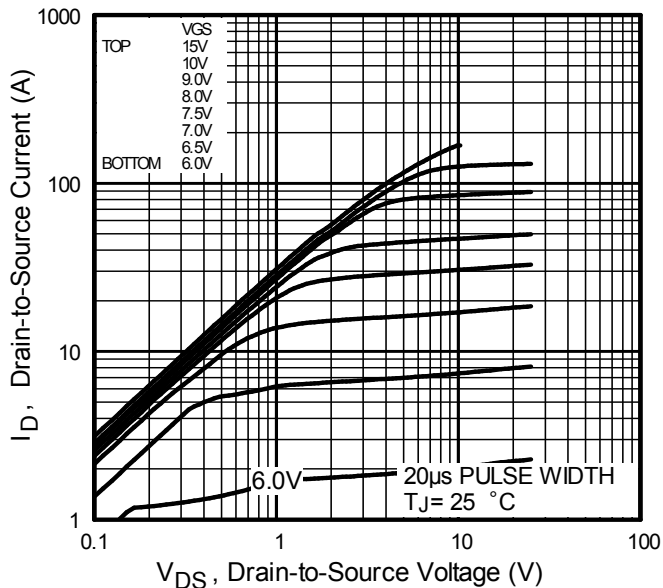
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	470	mJ
$I_{AR}$	Avalanche Current ①	—	25	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	20	mJ

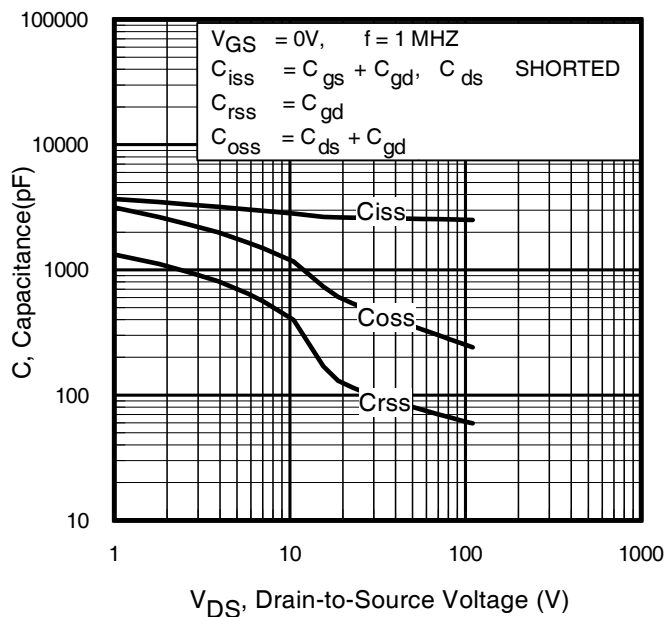
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	41	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	164		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	170	260	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
$Q_{rr}$	Reverse Recovery Charge	—	1.3	1.9	$\mu C$	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

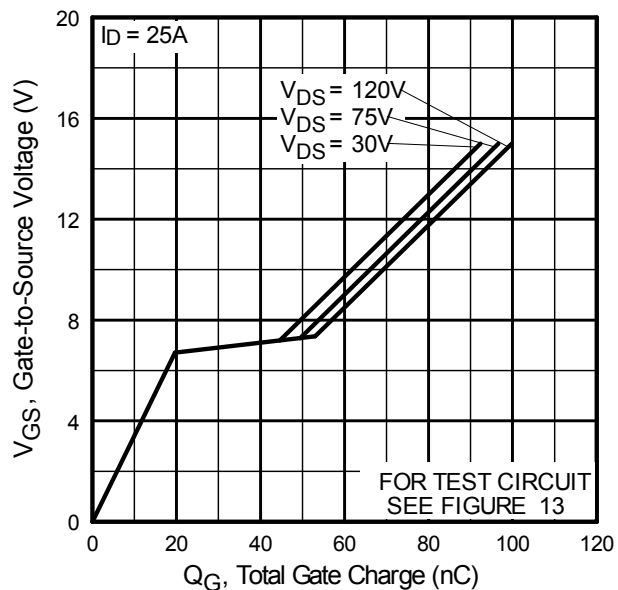
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.5mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 25A$ .
- ③  $I_{SD} \leq 25A$ ,  $di/dt \leq 340A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

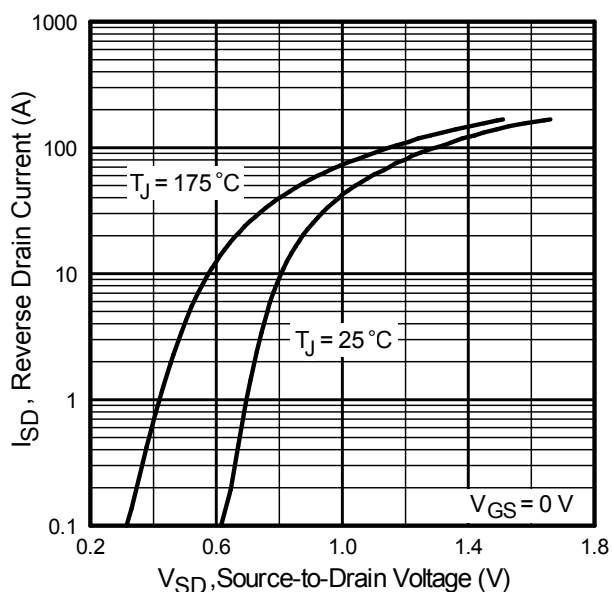




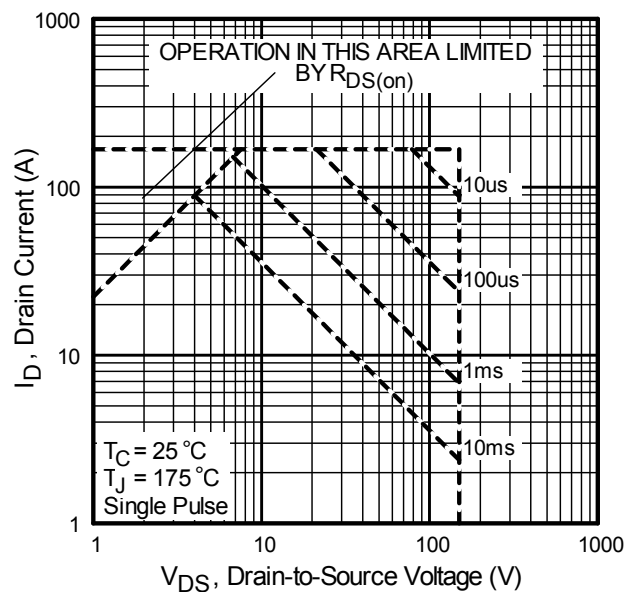
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



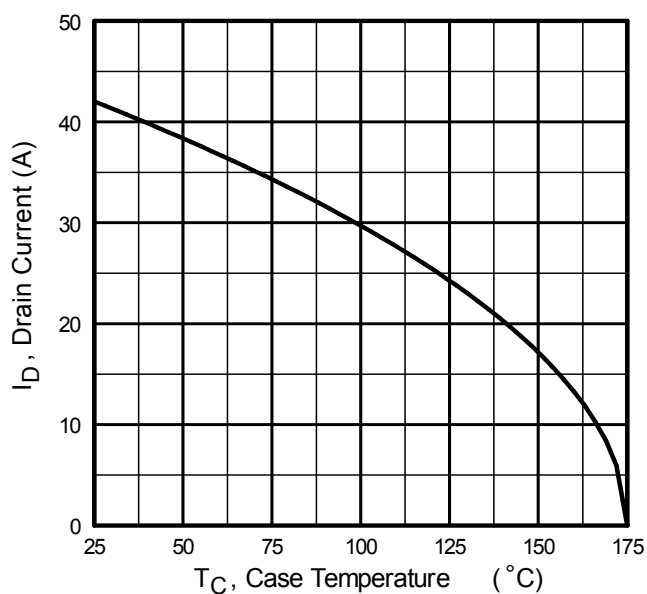
**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



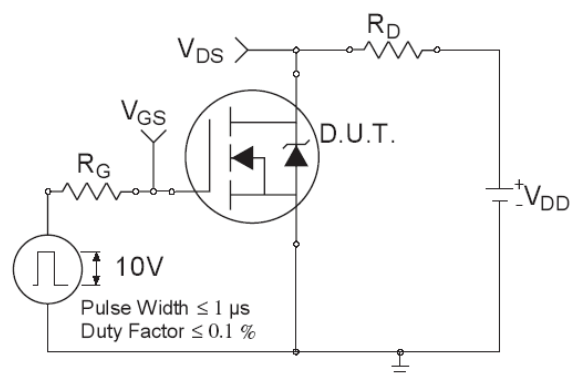
**Fig. 7** Typical Source-to-Drain Diode  
Forward Voltage



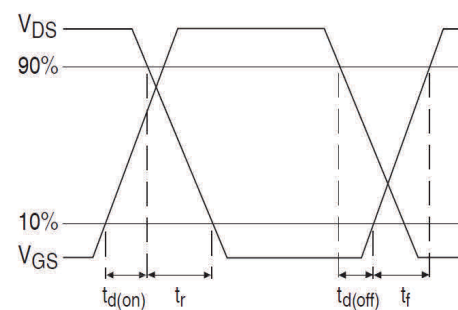
**Fig 8.** Maximum Safe Operating Area



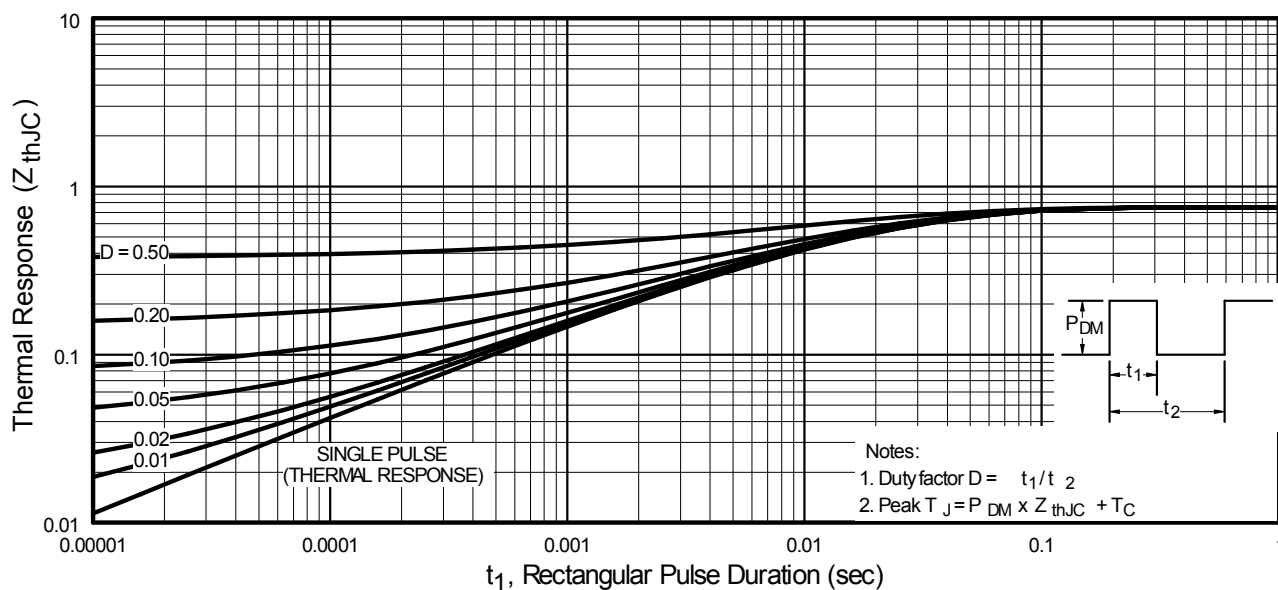
**Fig 9.** Maximum Drain Current vs. Case Temperature



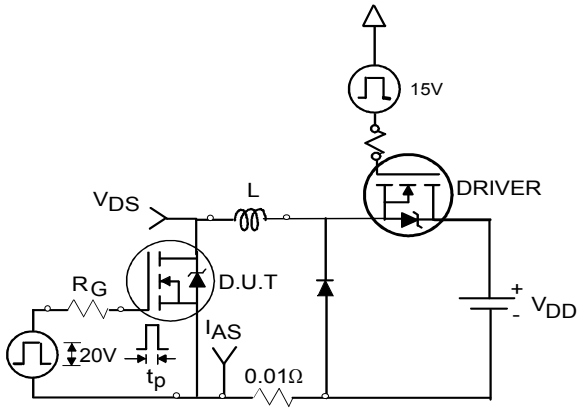
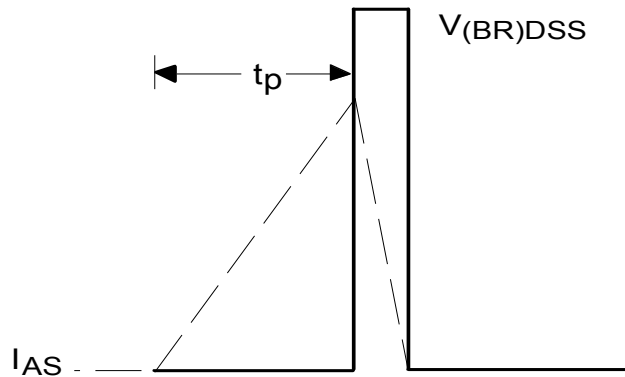
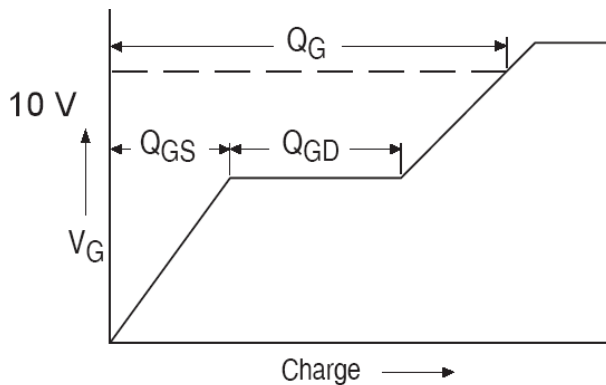
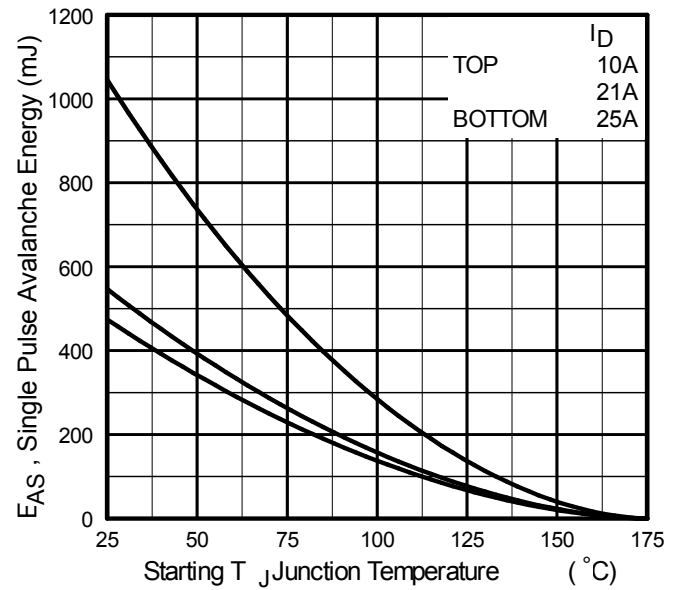
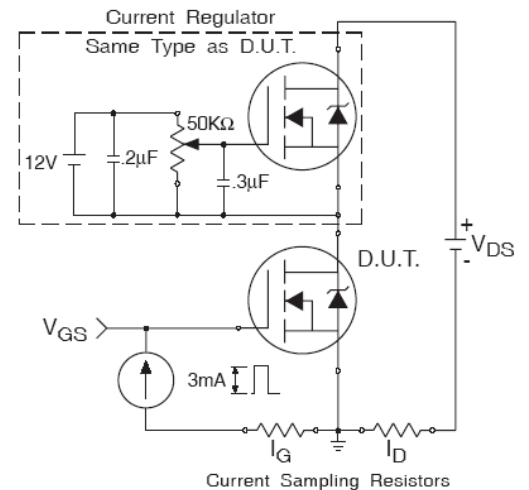
**Fig 10a.** Switching Time Test Circuit



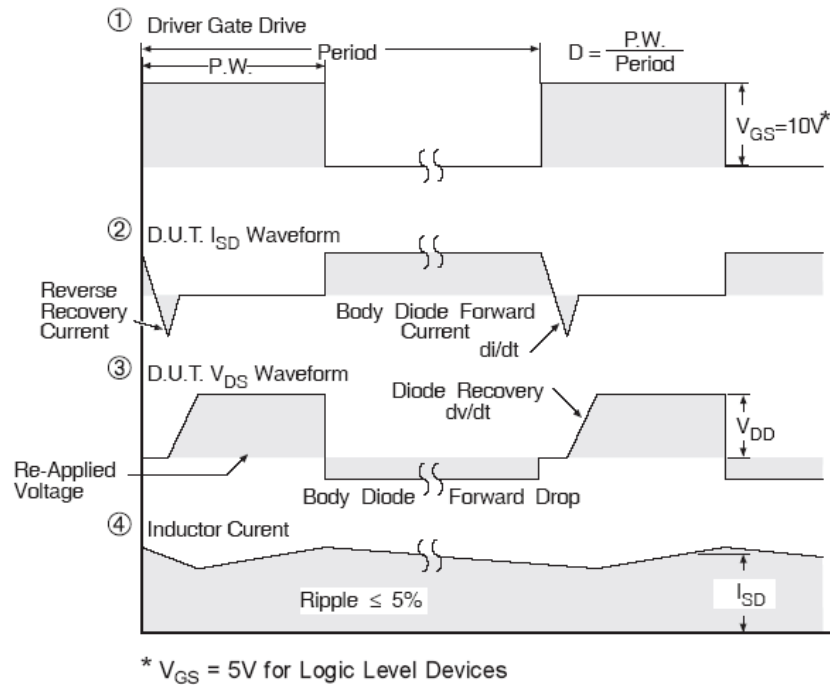
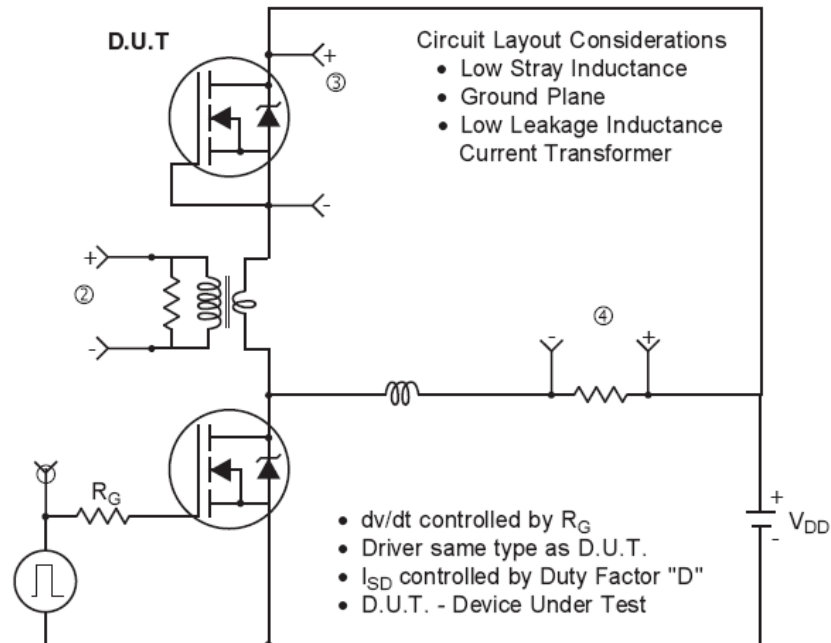
**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

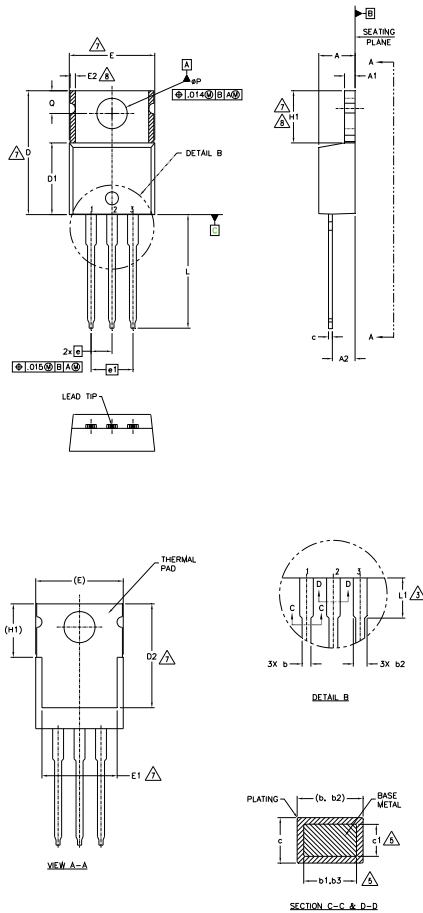

**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 13a.** Gate Charge Waveform

**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



**Fig 14.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

### TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTACT OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	5
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	7
D2	11.68	12.88	.460	.507	
E	9.65	10.67	.380	.420	
E1	6.86	8.89	.270	.350	4,7
E2	—	0.76	—	.030	7
e	2.54 BSC		.100 BSC		8
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	
L	12.70	14.73	.500	.580	7,8
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

### LEAD ASSIGNMENTS

## HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

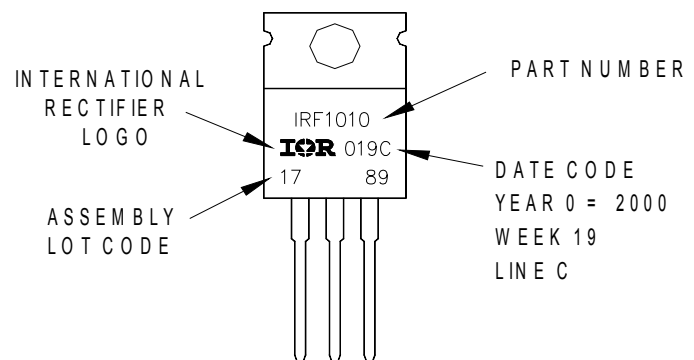
## DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead - Free"

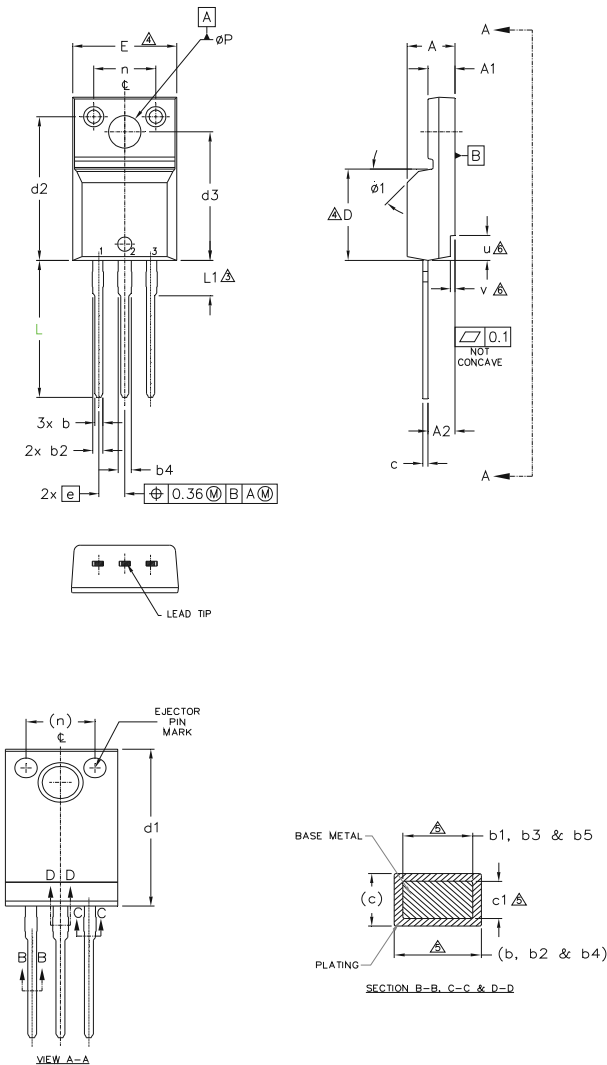


TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>



## TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	5
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	5
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	5
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	4
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	3
L1	3.10	3.68	.122	.145	
n	6.05	6.60	.238	.260	
øP	3.05	3.45	.120	.136	
u	2.39	2.49	.094	.098	6
v	0.41	0.51	.016	.020	6
ø1	—	45°	—	45°	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.— GATE
- 2.— DRAIN
- 3.— SOURCE

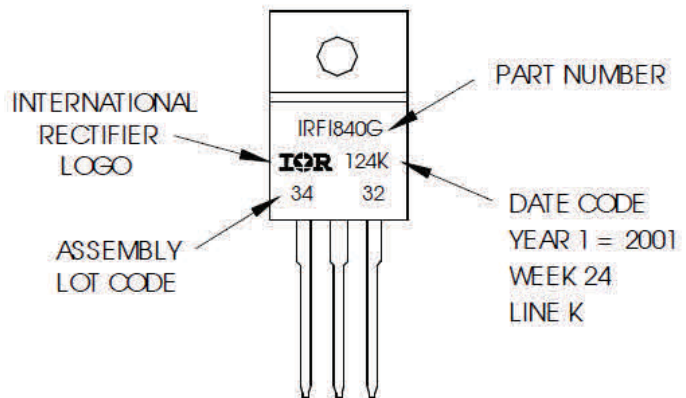
#### IGBTs, CoPACK

- 1.— GATE
- 2.— COLLECTOR
- 3.— EMITTER

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24, 2001  
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
indicates "Lead-Free"

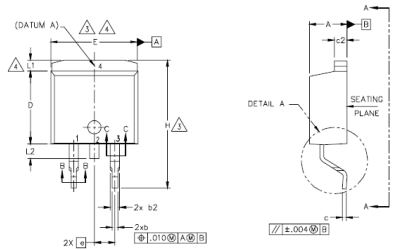


TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

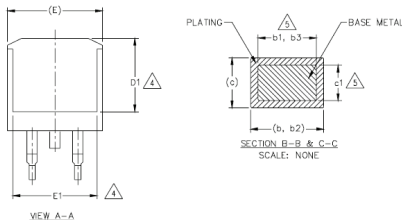
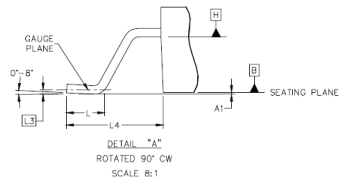
## D2-Pak (TO-263AB) Package Outline shown in millimeters (inches))

(Dimensions are



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3, 4
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		4
L4	4.78	5.28	.188	.208	

### LEAD ASSIGNMENTS

#### DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

#### HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

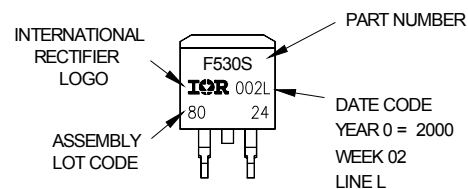
#### IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

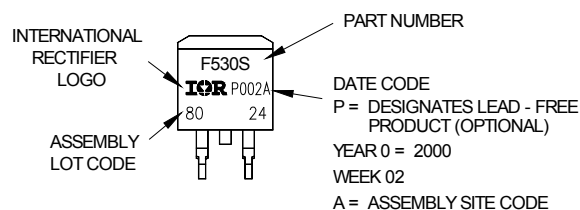
## D2-Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON VWV 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"

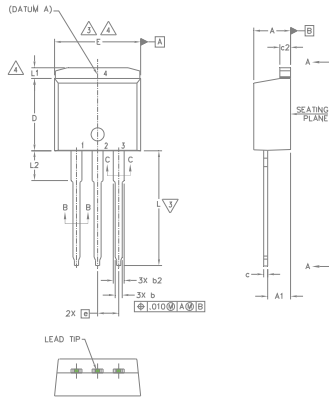


OR



Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

### LEAD ASSIGNMENTS

#### IGBTs, CoPACK

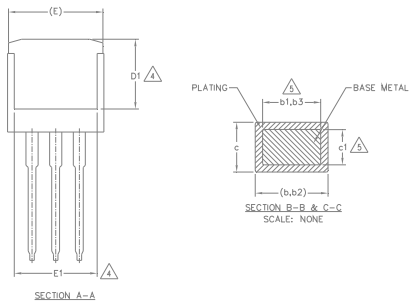
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

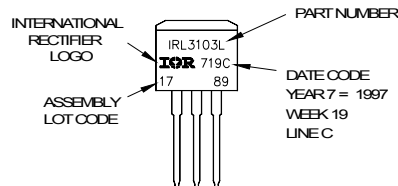


S Y M B O L	DIMENSIONS				N O T E
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	

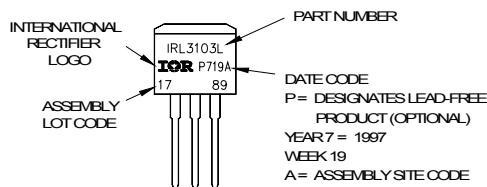
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW19, 1997  
IN THE ASSEMBLY LINE "C"

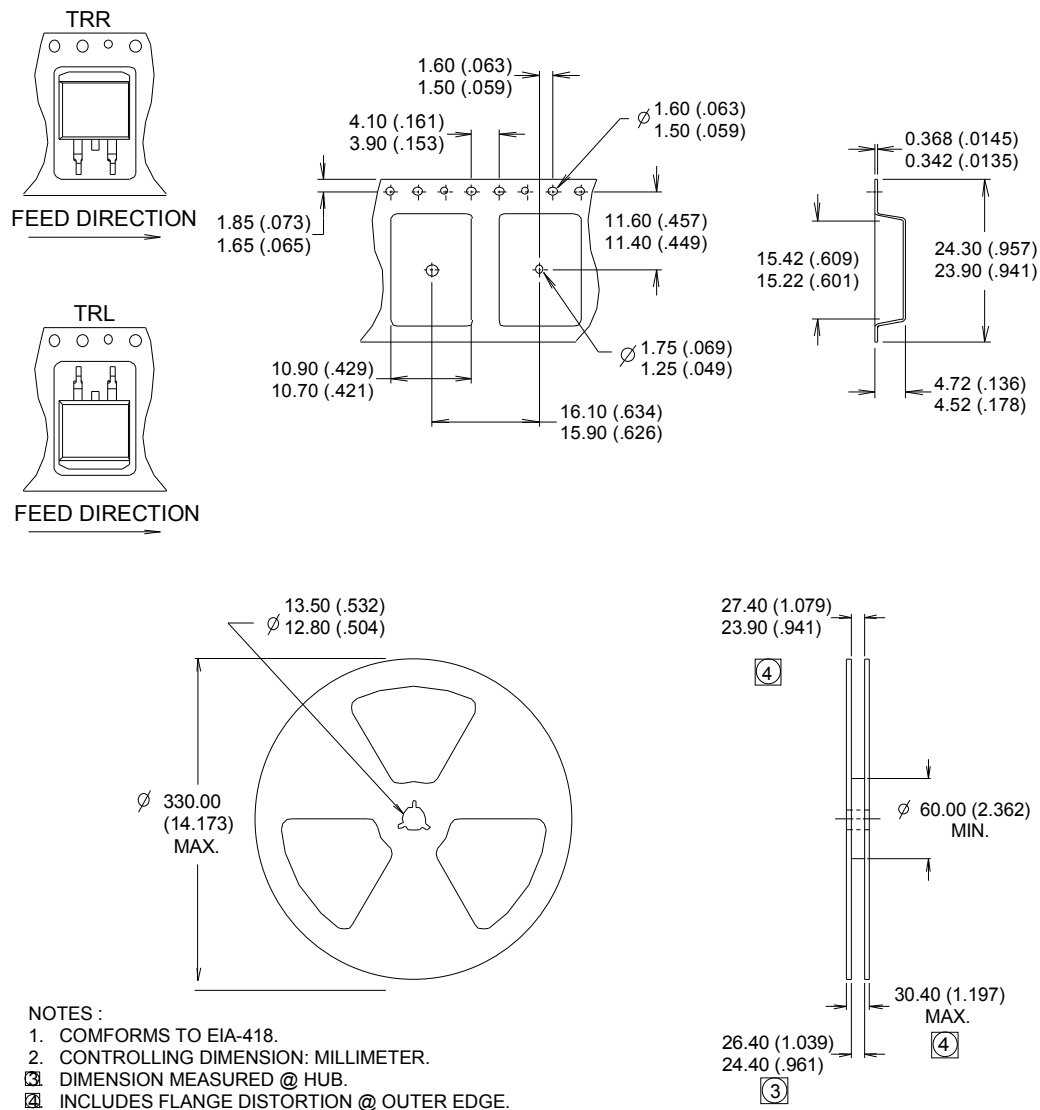
Note: "P" in assembly line position  
indicates "Lead - Free"



OR



Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

**D2-Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) <sup>†</sup>	
Moisture Sensitivity Level	TO-220AB	N/A
	TO-220 Full-Pak	
	TO-262	
	D2-Pak	MSL1 (per JEDEC J-STD-020D) <sup>††</sup>
RoHS Compliant	Yes	

<sup>†</sup> Applicable version of JEDEC standard at the time of product release.

## Revision History

Date	Comments
04/27/2017	<ul style="list-style-type: none"> <li>Changed datasheet with Infineon logo - all pages.</li> <li>Corrected Package Outline on page 8,9,10,11.</li> <li>Added disclaimer on last page.</li> </ul>

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