



PerF≝T[™]Power Transistor

FEATURES

- Excellent FOM
- Reliability meets AEC-Q101 requirements
- Wettable flank leads for enhanced AOI
- 100% UIS and Rg tested
- 175°C operating junction temperature
- RoHS Compliant
- Halogen-free

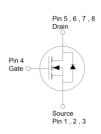
KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
V _{DS}		100	V	
	V _{GS} = 10V	7.5	0	
R _{DS(on)} (max)	V _{GS} = 4.5V	10.5	mΩ	
Qg	$V_{GS} = 4.5V$	18	nC	



APPLICATIONS

- Solenoid and motor drivers
- DC-DC converters
- Load Switch
- SMPS





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V_{GS}	±20	V	
Continuous Drain Current, Silicon limited	T _C = 25°C	I _D	113	Α	
Continuous Drain Current (Note 1)	T _C = 25°C	I _D	100	А	
	T _C = 100°C		80		
	T _A = 25°C		13		
Pulsed Drain Current (Note 2)		Ідм	400	А	
Single Pulse Avalanche Current (Note 3)		I _{AS}	19.8	А	
Single Pulse Avalanche Energy (Note 3)		Eas	59	mJ	
Total Power Dissipation	$T_C = 25^{\circ}C$	P _D	214	W	
	Tc = 125°C		71		
Operating Junction and Storage Temperature Range		TJ, TSTG	- 55 to +175	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	Rejc	0.7	°C/W	
Junction to Ambient Thermal Resistance (Note 4)	Reja	50	°C/W	

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Notes:

- 1. Package current limit.
- 2. Pulse Width ≤ 100µs.
- 3. L = 0.3mH, VGS = 10V, RG = 25 Ω , Starting TJ = 25 $^{\circ}$ C.
- 4. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.



PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 1mA$	BV _{DSS}	100			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V _{GS(TH)}	1.4	1.8	2.2	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA
	V _{GS} = 0V, V _{DS} = 100V	I _{DSS}			1	μA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 100V T _J = 125°C				100	
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 50A		-	5.4	7.5	mΩ
(Note 5)	$V_{GS} = 4.5V, I_D = 50A$	R _{DS(on)}		6.9	10.5	
Forward Transconductance (Note 5)	$V_{DS} = 10V, I_D = 12.5A$	G fs		70		S
Dynamic (Note 6)						
Total Gate Charge	$V_{DS} = 50V, I_{D} = 13A,$ $V_{GS} = 4.5V$	Qg		18		nC
Total Gate Charge		Qg		36		
Gate-Source Charge	$V_{DS} = 50V, I_D = 13A,$	Q _{gs}		6.7		nC
Gate-Drain Charge	V _{GS} = 10V	Q _{gd}		6.8		
Input Capacitance		Ciss		2110		
Output Capacitance	$V_{DS} = 60V$, $V_{GS} = 0V$,	Coss	-	327		pF
Reverse Transfer Capacitance	f = 1.0MHz	Crss	-	31		
Gate Resistance	f = 1.0MHz	Rg		0.5		Ω
Switching (Note 7)						
Turn-On Delay Time		t _{d(on)}		11		
Turn-On Rise Time	$V_{DD} = 50V, R_G = 6\Omega,$ $I_D = 13A, V_{GS} = 10V$	t _r		25		
Turn-Off Delay Time		t _{d(off)}		37		ns
Turn-Off Fall Time		t _f		53		
Source-Drain Diode						
Forward Voltage (Note 5)	I _S = 50A, V _{GS} = 0V	VsD			1.1	V
Reverse Recovery Time	Is = 13A,	t _{rr}		67		ns
Reverse Recovery Charge	di/dt = 100A/µs	Qrr		102		nC

Notes:

- 5. Pulse test: Pulse Width \leq 300 μ s, duty cycle \leq 2%.
- 6. Defined by design. Not subject to production test.
- 7. Switching time is essentially independent of operating temperature.

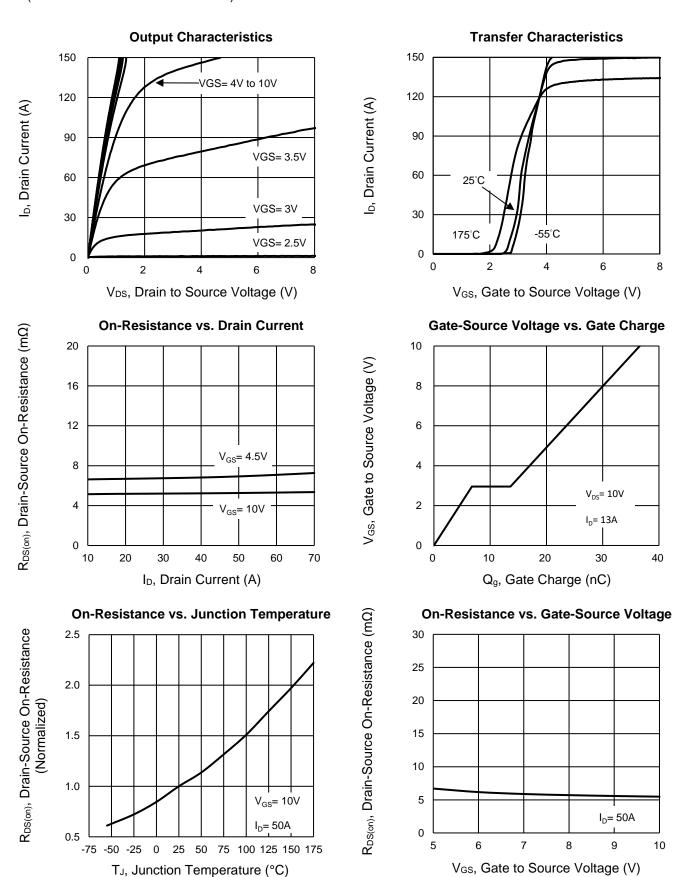
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM075NH10LCR RLG	PDFN56U	2,500pcs / 13" Reel



CHARACTERISTICS CURVES

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$



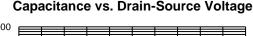


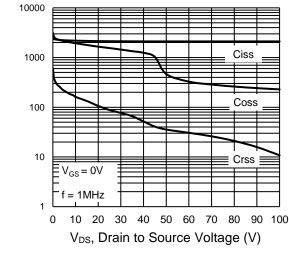
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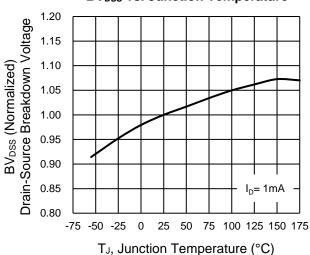
C, Capacitance (pF)

Normalized Effective Transient Thermal Impedance, Zeuc

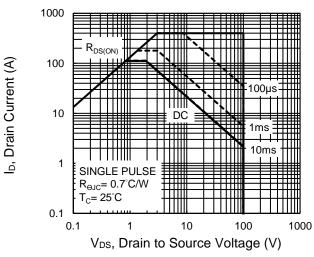




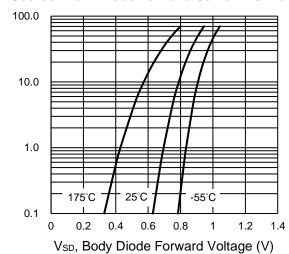
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area, Junction-to-Case



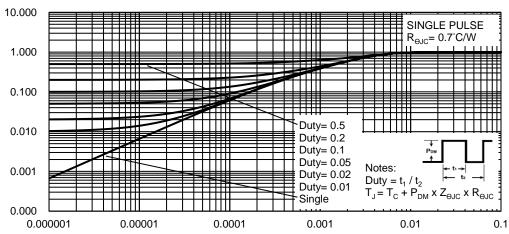
Source-Drain Diode Forward Current vs. Voltage



Normalized Thermal Transient Impedance, Junction-to-Case

Reverse Drain Current (A)

Ś



t, Square Wave Pulse Duration (sec)

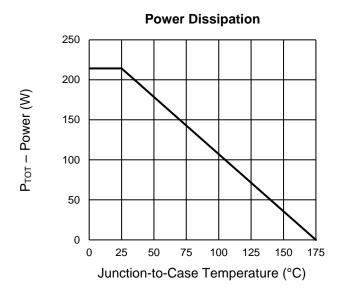
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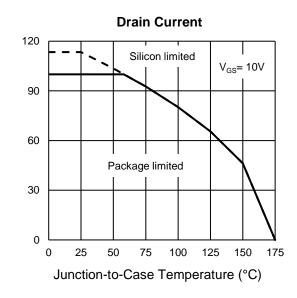


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CHARACTERISTICS CURVES

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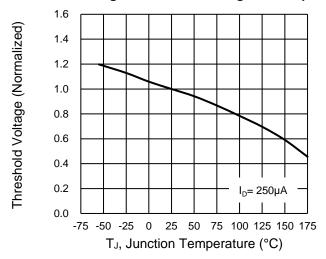




I_D-Drain Current (A)

5

Normalized gate threshold voltage vs Temperature

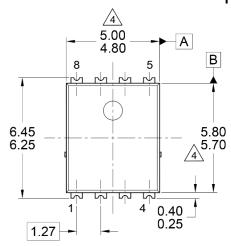


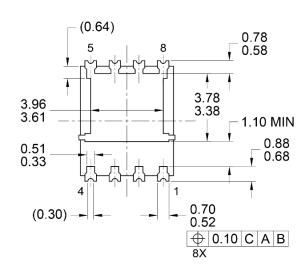


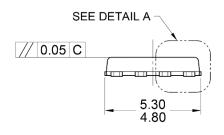


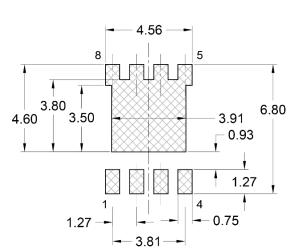
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U









SUGGESTED PAD LAYOUT

(REFERENCE ONLY)

0.90MIN 1.10 0.90 ○ 0.05 C 0.30 0.05 С 0.20 0.00 PLATED AREA SEATING PLANE **DETAIL A**

(SCALE 2:1)

5 **TSC** 075NH10L **YWWLF** DOT MARKING, PIN #1 ID

NOTES: UNLESS OTHERWISE SPECIFIED

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
- MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

MARKING DIAGRAM

075NH10L = Device marking Υ = Year code

WW = Week code (01~52) L = Lot code $(1\sim9,A\sim Z)$ F = Factory code



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