

n-Channel Power MOSFET

OptiMOS™ BSB280N15NZ3 G

Data Sheet

2.5, 2011-09-16 Final

Industrial & Multimarket



1 Description

OptiMOS™150V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate- and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 150V the best choice for the demanding requirements of voltage regulator solutions in Solar, Drives, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space- efficiency and cost.



Features

- · Optimized for high switching frequency DC/DC converter
- Very low on-resistance R_{DS(on)}
- Qualified according to JEDEC¹⁾ for target applications
- Excellent gate charge x R_{DS(on)} product (FOM)
- · Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double sided cooling
- Compatible with DirectFET® package MZ footprint and outline
- Low parasitic inductance
- Low profile (<0.7 mm)

Applications

- Synchronous rectification
- · Primary side switches
- · Power managment for high performance computing
- High power density point of load converters







Table 1 Key Performance Parameters

Parameter	Value	Unit	Related Links			
V_{DS}	150	V	IFX OptiMOS webpage			
R _{DS(on),max}	28	mΩ	IFX OptiMOS product brief			
I_{D}	30	А	IFX OptiMOS spice models			
Q _{OSS}	38	nC	IFX Design tools			
$Q_{g \cdot typ}$	15					

Туре	Package	Marking
BSB280N15NZ3 G	MG-WDSON-2	0215

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¹⁾ J-STD20 and JESD22



2 Maximum ratings

at T_i = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Тур.	Max.		
Continuous drain current	I _D	-	-	30	Α	V _{GS} =10 V, T _C =25 °C
				19		V _{GS} =10 V, T _C =100 °C
				9		V _{GS} =10 V, T _A =25 °C, R _{thJA} =45 K/W) ¹⁾
Pulsed drain current ²⁾	I _{D,pulse}	-	-	120		<i>T</i> _C =25 °C
Avalanche energy, single pulse	E _{AS}	-	-	120	mJ	$I_{\rm D}$ =30 A, $R_{\rm GS}$ =25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P _{tot}	-	-	57	W	<i>T</i> _C =25 °C
				2.8		T _A =25 °C, R _{thJA} =45 K/W
Operating and storage temperature	$T_{\rm j}, T_{\rm stg}$	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/15	0/56	-		

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air.

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol		Value	s	Unit	Note / Test Condition
		Min.	Тур.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.2	K/W	top
			1	-		bottom
Device on PCB	R_{thJA}	-	-	45		6 cm ² cooling area ¹⁾

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µ, thick) copper area for drain conneciton. PCB is vertical in still air.

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²⁾ See figure 3 for more detailed information



Electrical characteristics

4 Electrical characteristics

Electrical characteristics, at *T*j=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Тур.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{\rm GS}$ =0 V, $I_{\rm D}$ =1.0 mA
Gate threshold voltage	$V_{\rm GS(th)}$	2	3	4		$V_{\rm DS} = V_{\rm GS}$, $I_{\rm D} = 60~\mu{\rm A}$
Zero gate voltage drain current	I _{DSS}	-	0.1	10	μΑ	$V_{\rm DS}$ =120 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =25 °C
		-	10	100		$V_{\rm DS}$ =120 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =125 °C
Gate-source leakage current	I _{GSS}	-	10	100	nA	V _{GS} =20 V, V _{DS} =0 V
Drain-source on-state resistance	$R_{\rm DS(on)}$	-	24	28	mΩ	$V_{\rm GS}$ =10 V, $I_{\rm D}$ =30A
			24	32		$V_{GS} = 8 \text{ V}, I_{D} = 15 \text{A}$
Gate resistance	R_{G}	-	0.6	-	Ω	
Transconductance	g_{fs}	18	37		S	$ V_{\rm DS} > 2 I_{\rm D RDS(on)max},$ $I_{\rm D} = 30 \text{ A}$

 Table 5
 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note /	
		Min.	Тур.	Max.		Test Condition	
Input capacitance	C _{iss}	-	1200	1600	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 75 \text{ V},$	
Output capacitance	Coss	-	180	240		f=1 MHz	
Reverse transfer capacitance	C _{rss}	-	4	-			
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{\rm DD} = 75 \text{V}, \ V_{\rm GS} = 10 \text{V},$	
Rise time	t _r	-	6	-		$I_{\rm D}$ =30 A, $R_{\rm G}$ = 1.6 Ω	
Turn-off delay time	$t_{\sf d(off)}$	-	16	-			
Fall time	t _f	-	3	-			



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Electrical characteristics

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol		Values			Note /
		Min.	Тур.	Max.		Test Condition
Gate to source charge	Q_{gs}	-	7	-	nC	V _{DD} =75 V,
Gate to drain charge	$Q_{ m gd}$	-	2.6	-		$I_{\rm D}$ =30 A, $V_{\rm GS}$ =0 to 10 V
Switching charge	$Q_{\rm sw}$	-	7	-		$V_{\rm GS}$ =0 to 10 V
Gate charge total	Q_{g}	-	15	21		
Gate plateau voltage	V _{plateau}	-	5.6	-	V	
Output charge	Q _{oss}		41	55		$V_{\rm DD}$ =75 V, $V_{\rm GS}$ =0 V

¹⁾ See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Diode continuous forward current	I _s			47	Α	<i>T</i> _C =25 °C
Diode pulse current	I _{S,pulse}			120		
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{\rm GS}$ =0 V, $I_{\rm F}$ =47 A, $T_{\rm j}$ =25 °C
Reverse recovery time	t _{rr}	-	100	-	nC	V_{R} =75 V, I_{F} =30A,
Reverse recovery charge	Q _{rr}		314			d <i>i</i> _F /d <i>t</i> =100 A/μs



Electrical characteristics diagrams

Table 8

5

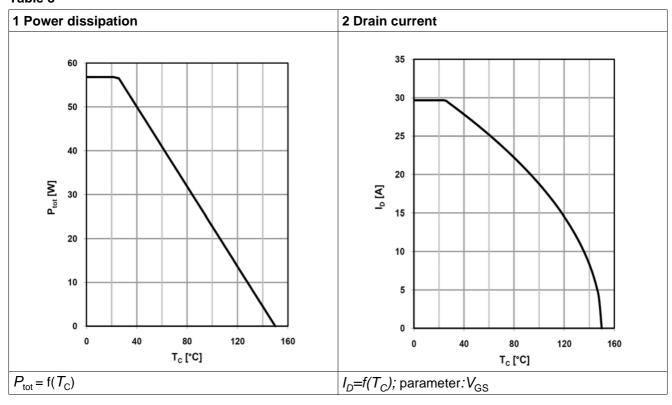


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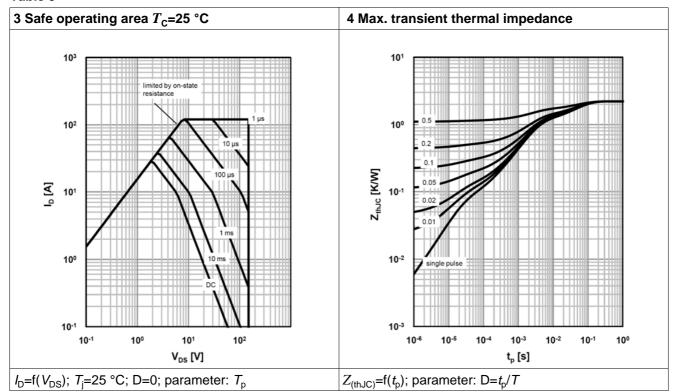




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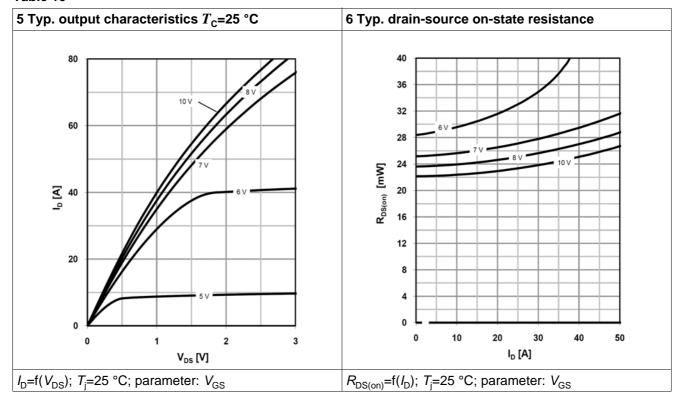


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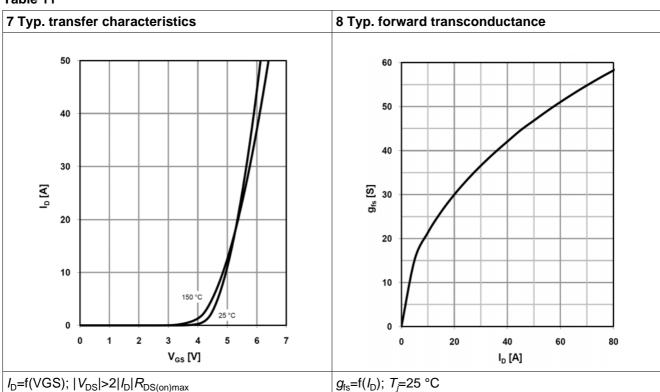




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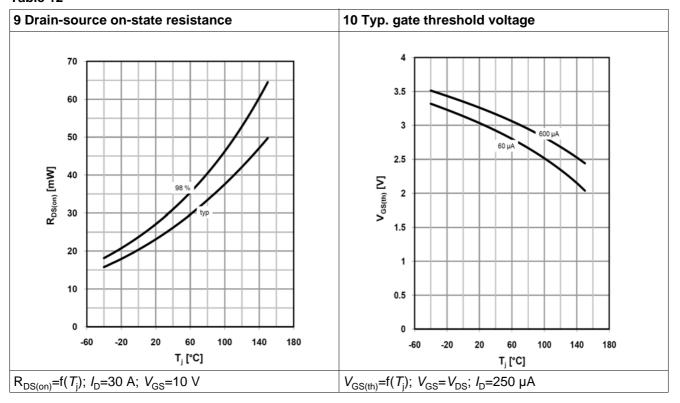


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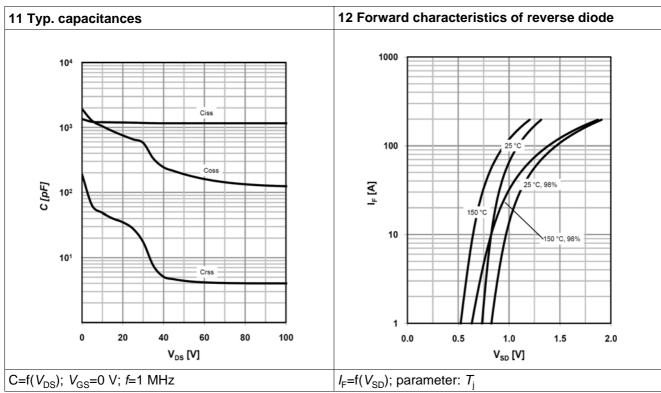




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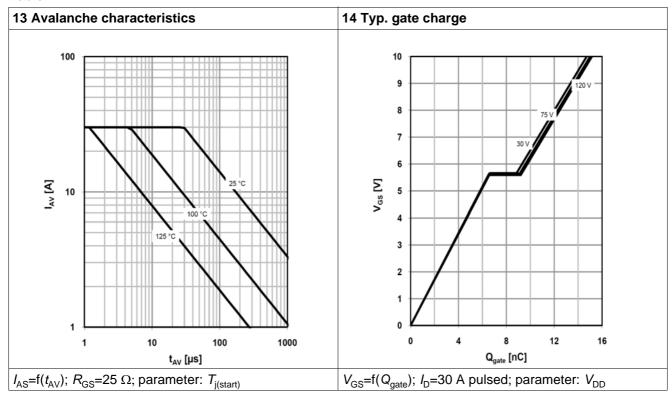
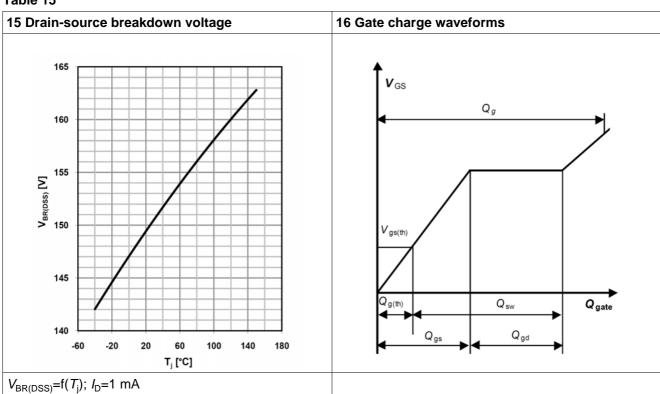


Table 15





Package outlines

6 Package outlines

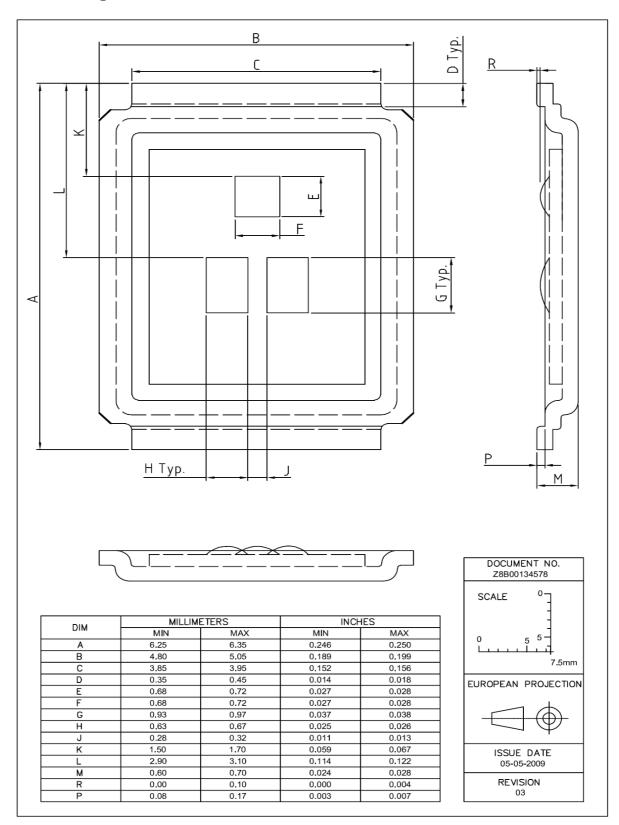


Figure 1 Outlines MG-WDSON-2, dimensions in mm/inches



Package outlines

7 Package outlines

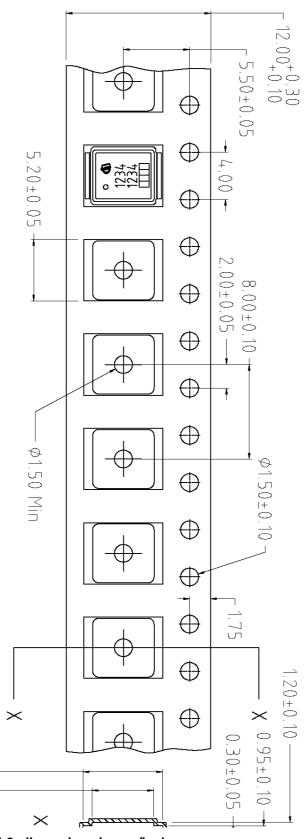


Figure 2 Outlines MG-WDSON-2, dimensions in mm/inches



Package outlines

8 Package outlines

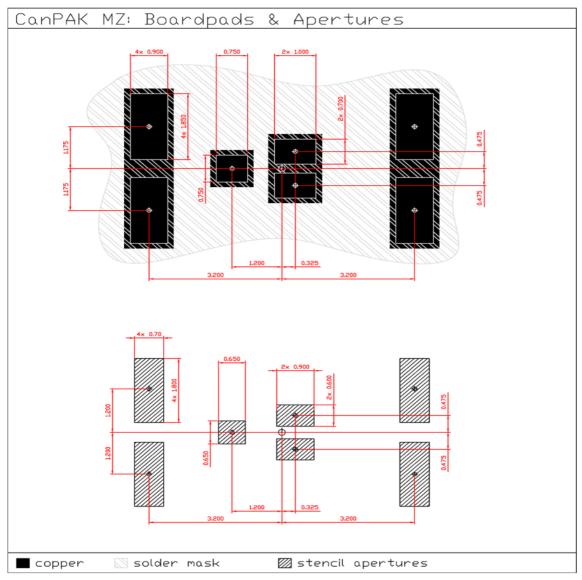
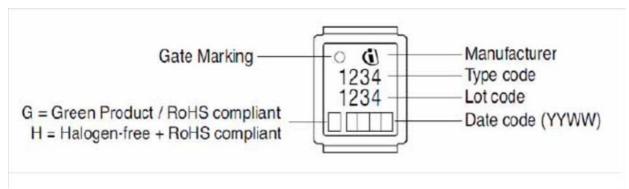


Figure 3 Outlines MG-WDSON-2, dimensions in mm/inches

9 Marking layout





Revision History

9 Revision History

Revision History: 2011-09-16, 2.5

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
2.2	Release Final version
2.3	Formating
2.4	DirectFET Disclaimer expired

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