

MOSFET

OptiMOS™ 5 Power-Transistor, 150 V

Features

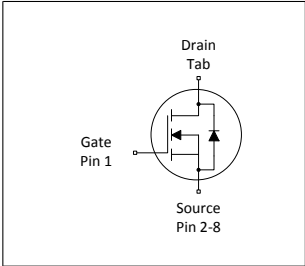
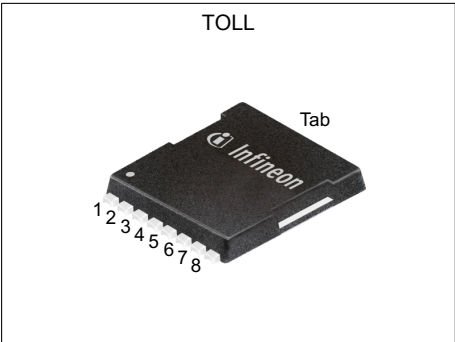
- N-channel
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	4.4	mΩ
$I_D$	179	A
$Q_{oss}$	188	nC
$Q_G$	67	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPT044N15N5	PG-HSOF-8	044N15N5	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	179 127 119 19.4	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=8\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^{2)}$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	716	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	189	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	319 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^{2)}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.47	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	$V_{DS}=V_{GS}$ , $I_D=221\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1.0 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.8 4.2	4.4 5.0	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=8\text{ V}$ , $I_D=25\text{ A}$
Gate resistance	$R_G$	-	0.9	-	$\Omega$	-
Transconductance	$g_{fs}$	-	100	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	5000	6500	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	1200	1950	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	29	51	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17.0	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	5.0	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25.1	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	6.4	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	27	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	19.2	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	13.5	20	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	22	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	67	84	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	188	250	nC	$V_{DS}=75\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

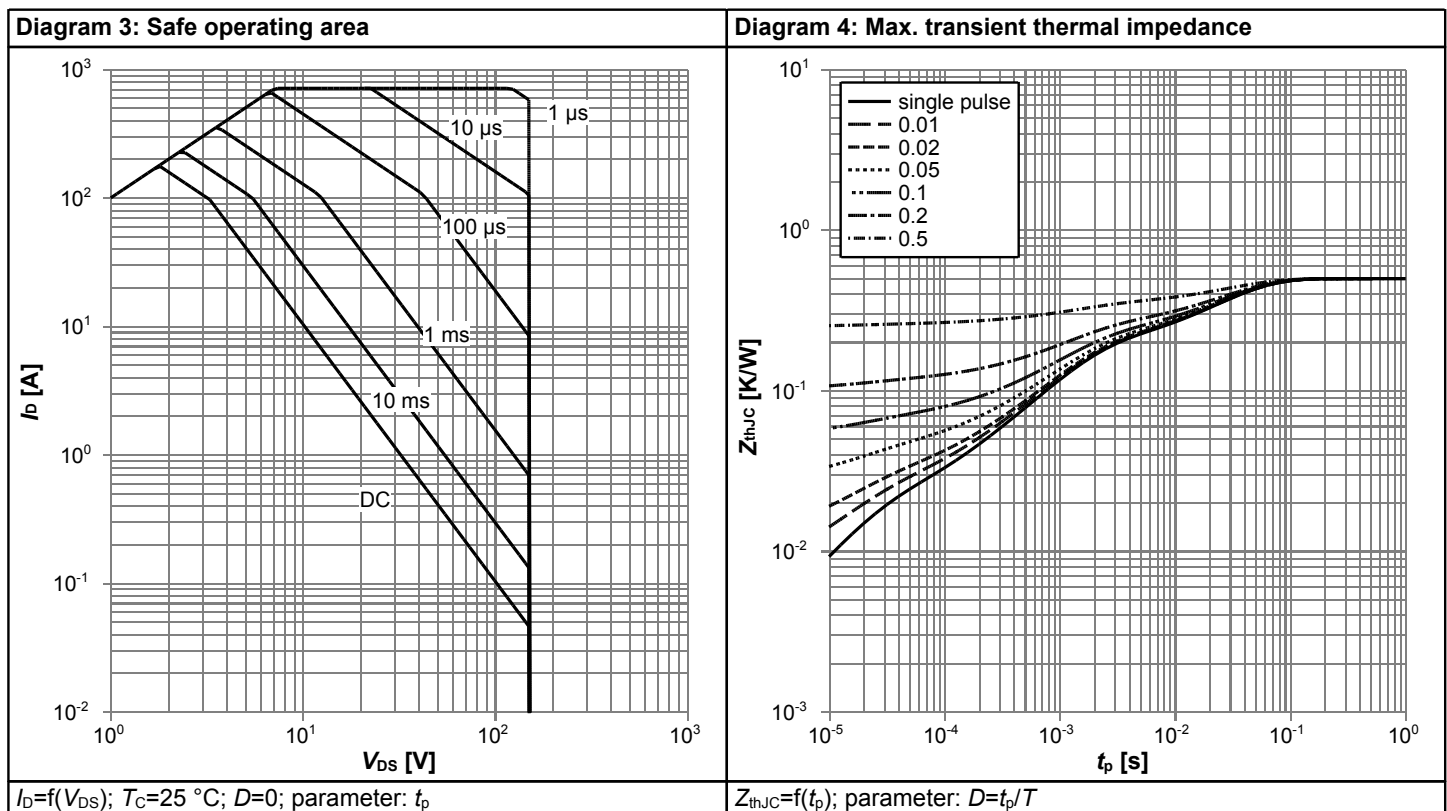
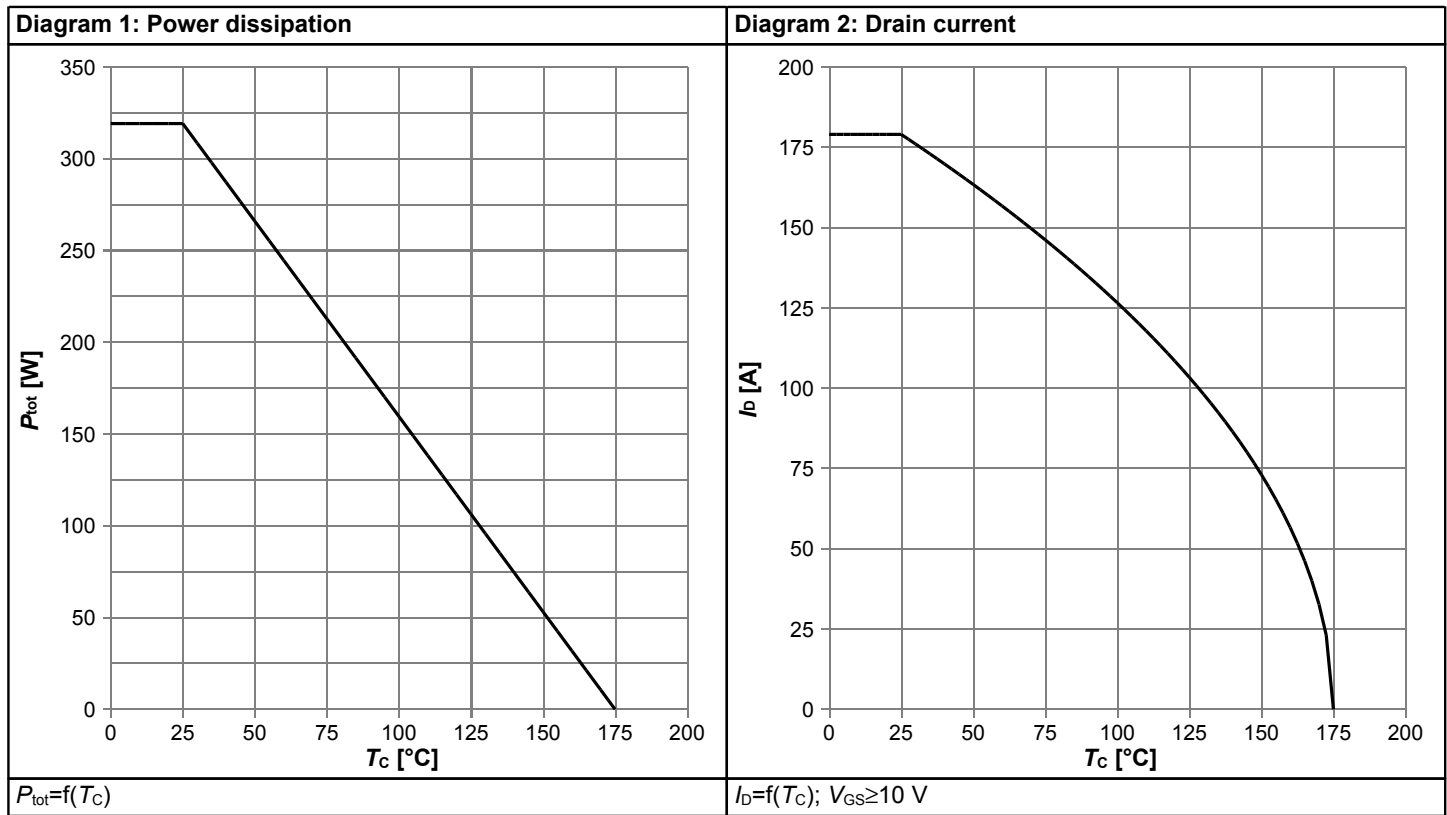
<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	179	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	716	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.82	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=50\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	45.2	90.4	ns	$V_R=75\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A/}\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	49.0	98.0	nC	$V_R=75\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A/}\mu\text{s}$

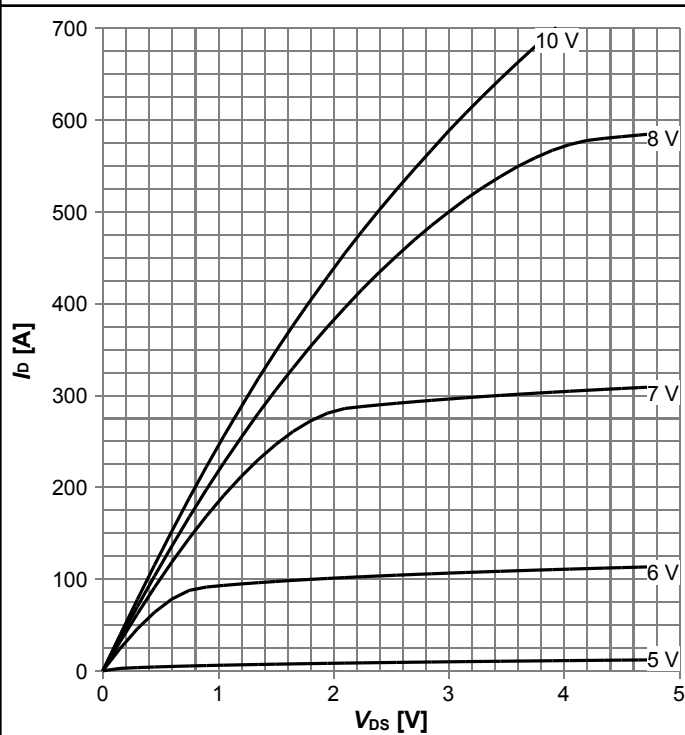
<sup>1)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams



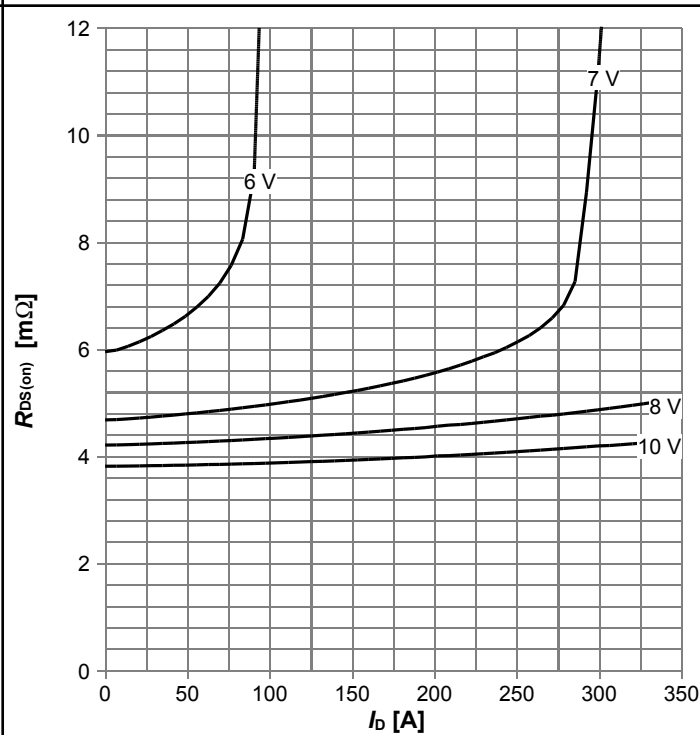
OptiMOS™ 5 Power-Transistor, 150 V  
IPT044N15N5

Diagram 5: Typ. output characteristics



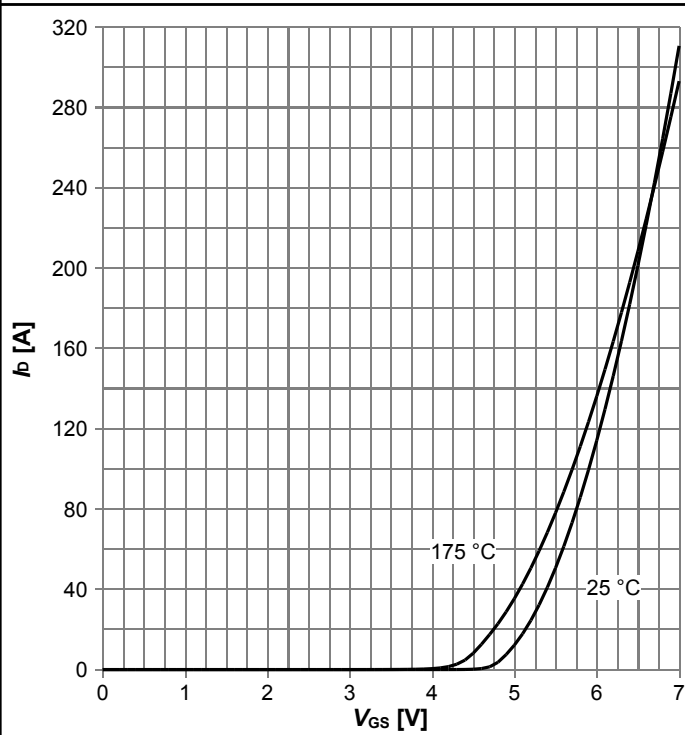
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



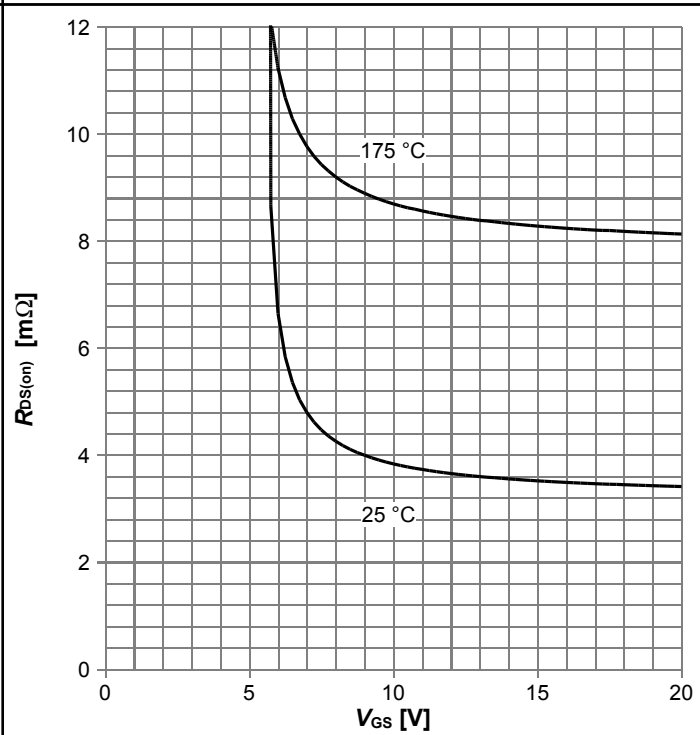
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



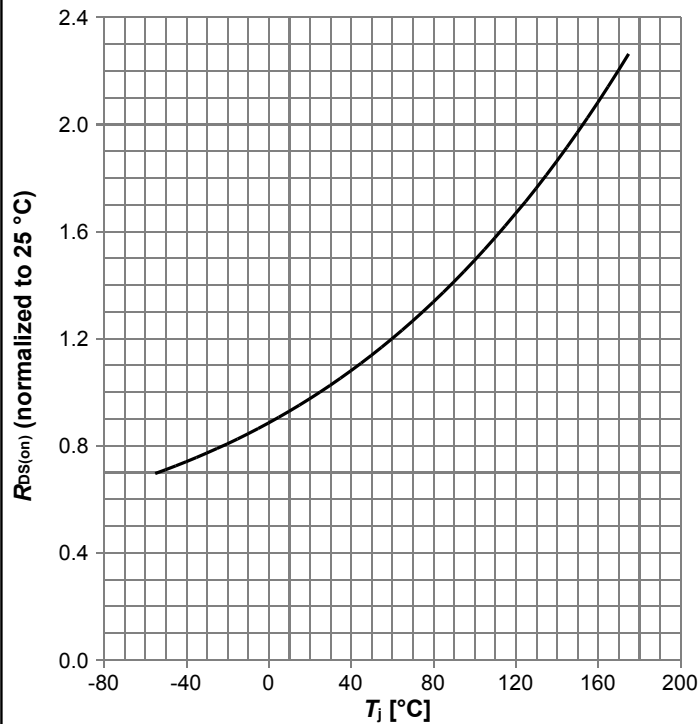
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)\max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



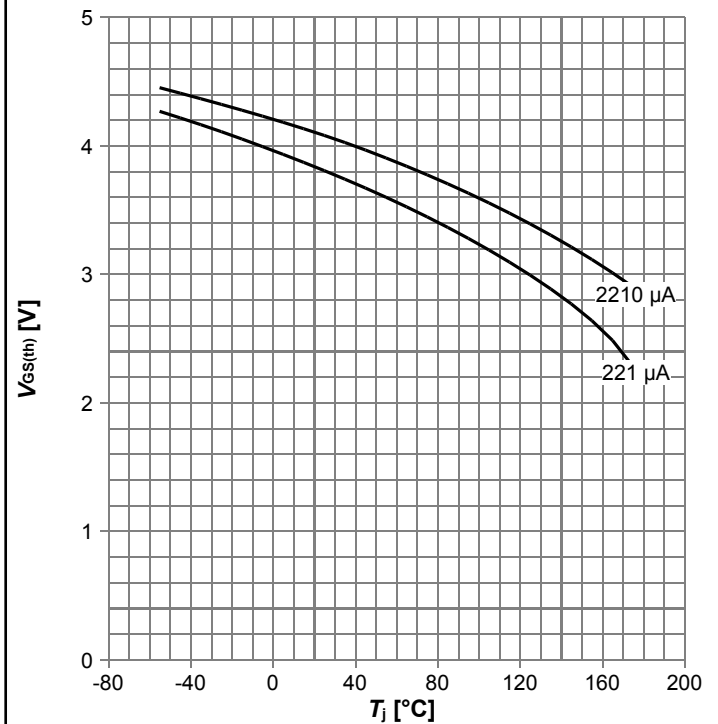
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 50$  A; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



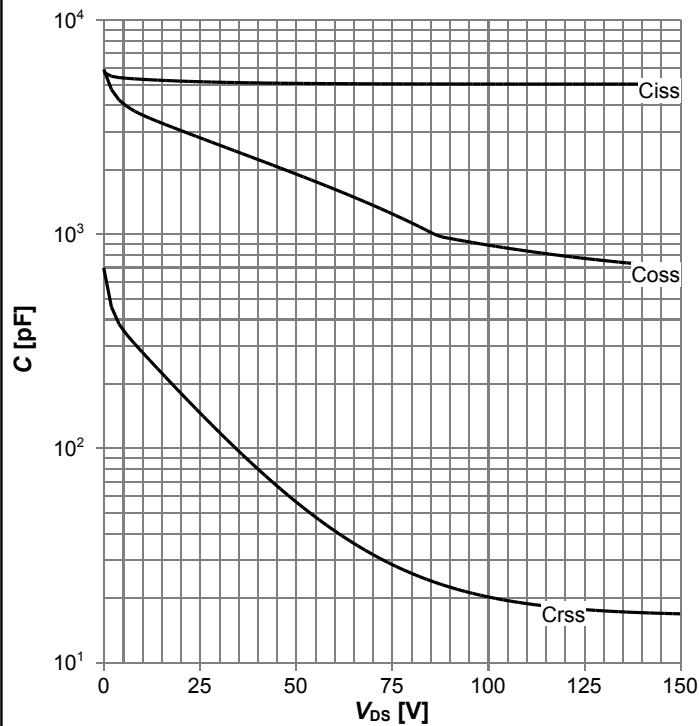
$R_{DS(on)} = f(T_j)$ ,  $I_D = 50$  A,  $V_{GS} = 10$  V

Diagram 10: Typ. gate threshold voltage



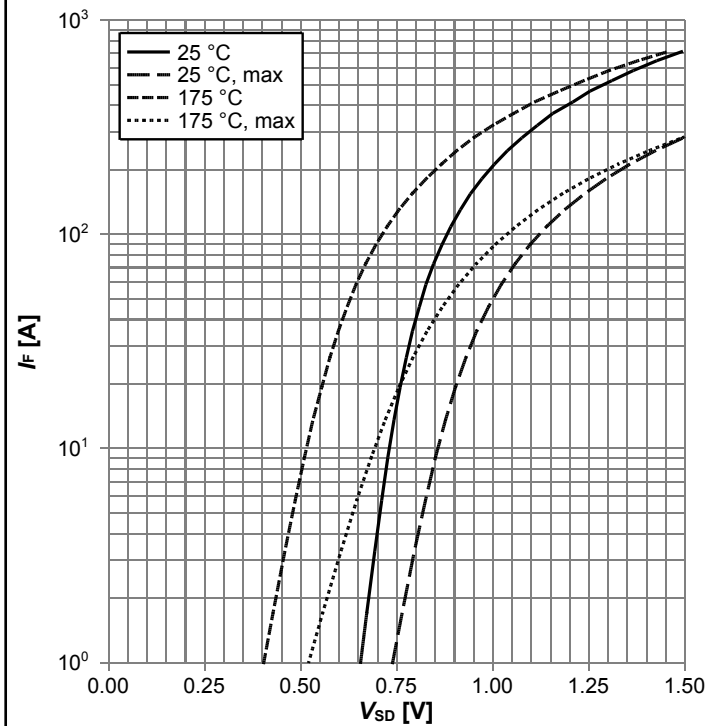
$V_{GS(th)} = f(T_j)$ ,  $V_{GS} = V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C = f(V_{DS})$ ;  $V_{GS} = 0$  V;  $f = 1$  MHz

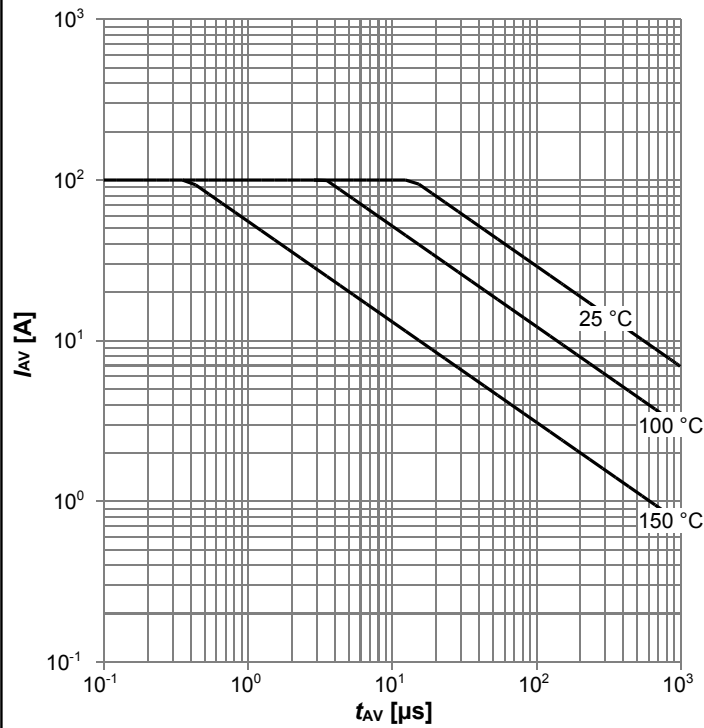
Diagram 12: Forward characteristics of reverse diode



$I_F = f(V_{SD})$ ; parameter:  $T_j$

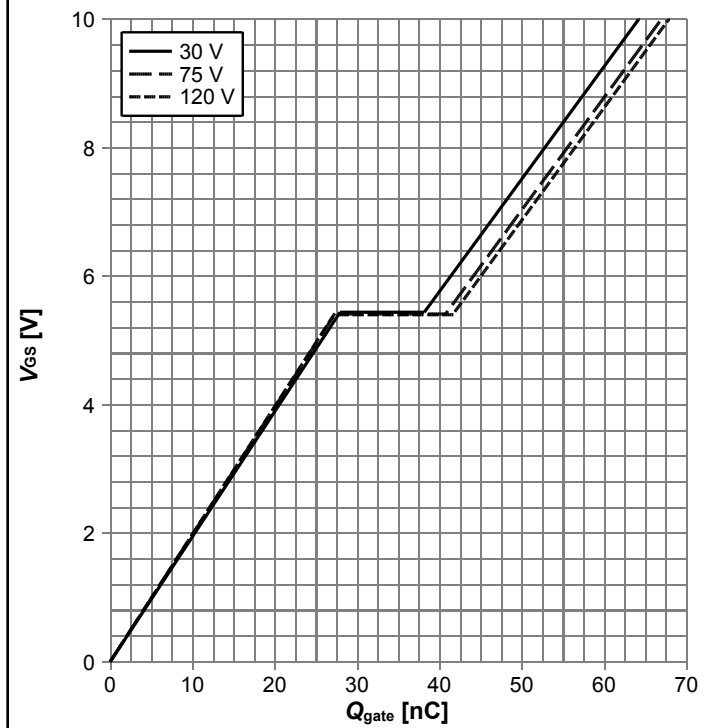


Diagram 13: Avalanche characteristics



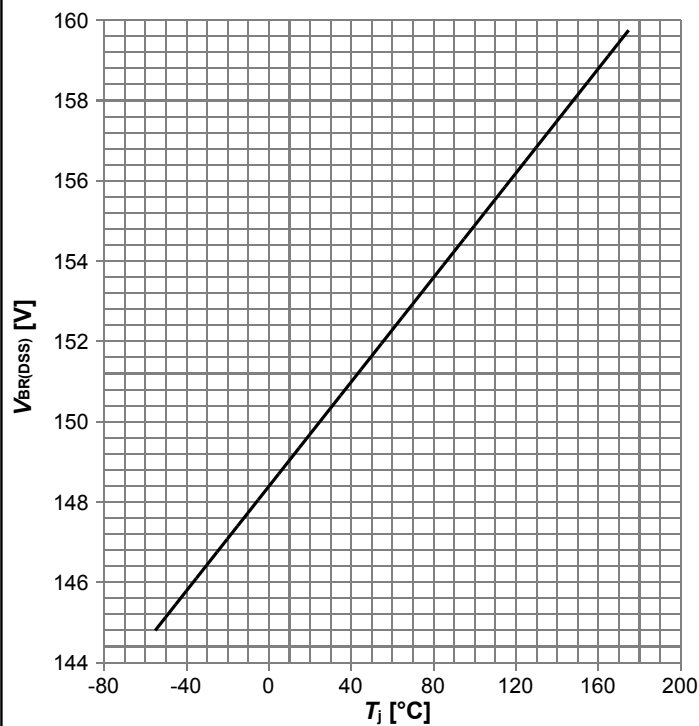
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



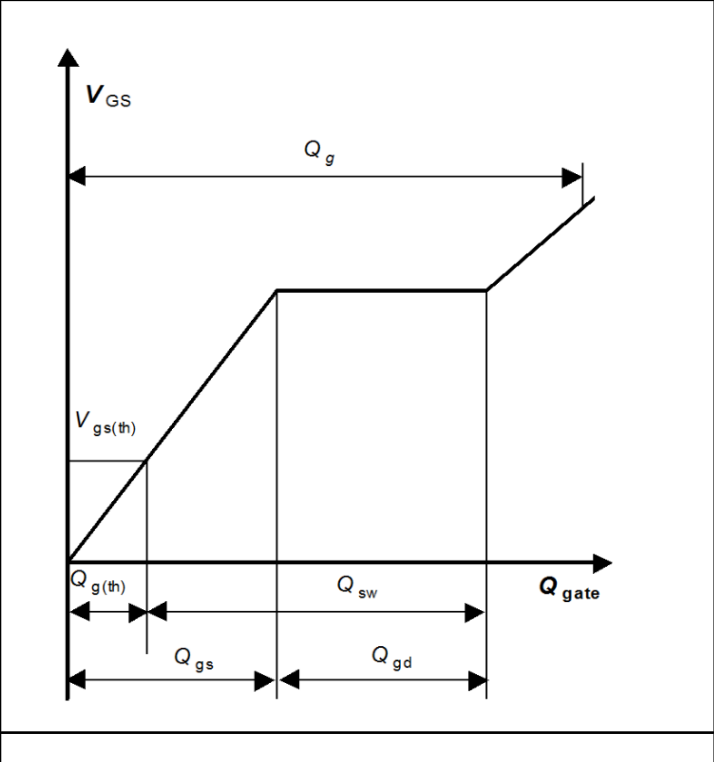
$V_{GS}=f(Q_{gate})$ ,  $I_D=50\text{ A}$  pulsed,  $T_j=25\text{ °C}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

Diagram Gate charge waveforms



## 5 Package Outlines

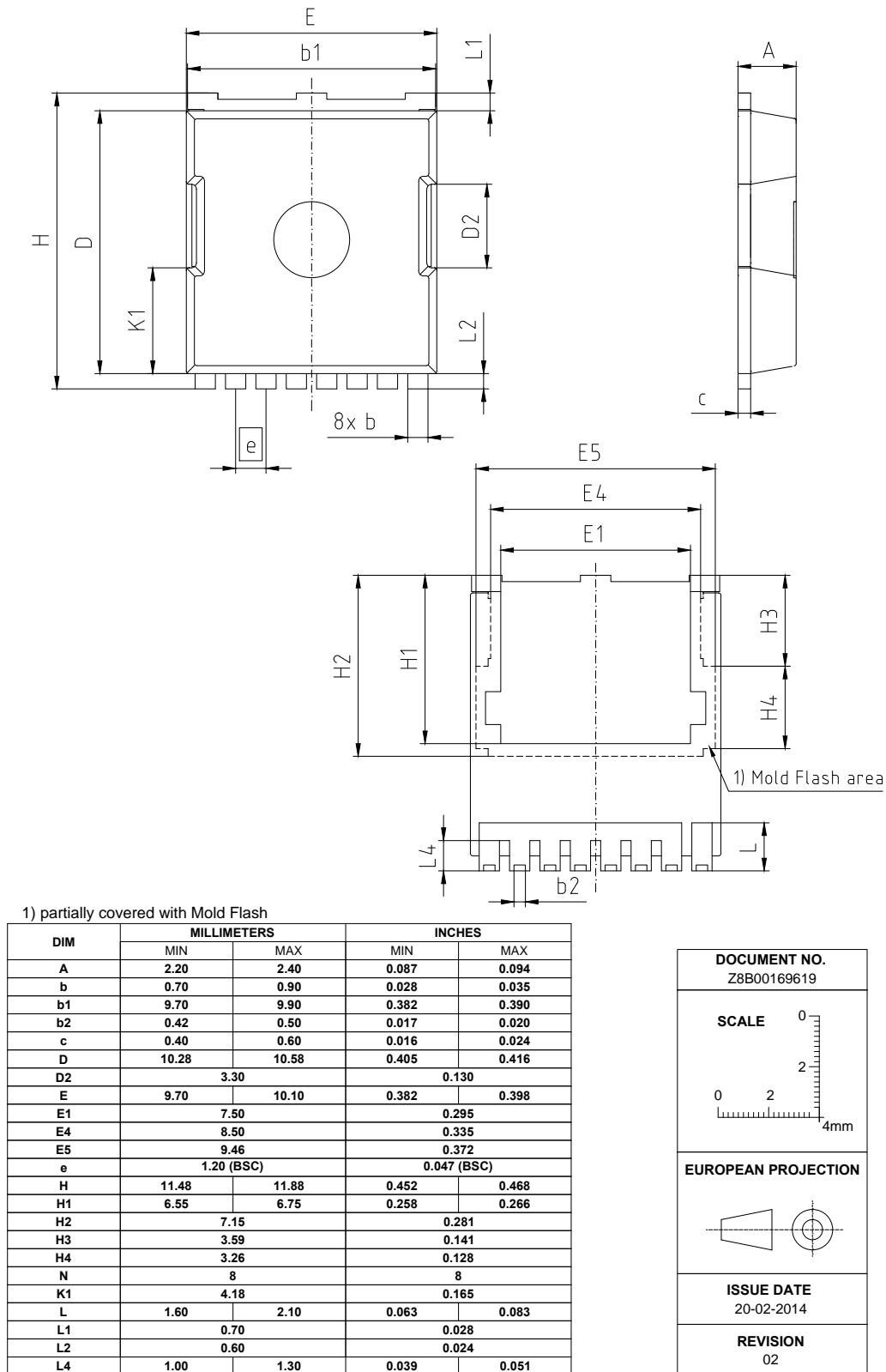


Figure 1 Outline PG-HSOF-8, dimensions in mm/inches

## Revision History

IPT044N15N5

**Revision: 2023-09-11, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-09-10	Release of final version
2.1	2023-03-13	Update Coss max
2.2	2023-09-11	Update RthJC

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