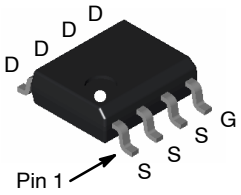
# MOSFET – N-Channel, UltraFET Trench

## 200 V, 3.9 A, 70 mΩ

# FDS2672




**SOIC8**
**CASE 751EB**

### General Description

This single N−Channel MOSFET is produced using **onsemi**'s advanced UItraFET Trench process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

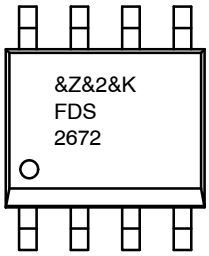
### Features

- Max $r_{DS(on)}$ = 70 mΩ at $V_{GS}$ = 10 V, $I_D$ = 3.9 A
- Max $r_{DS(on)}$ = 80 mΩ at $V_{GS}$ = 6 V, $I_D$ = 3.5 A
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- These Device is Pb−Free, Halide Free and are RoHS Compliant

### Applications

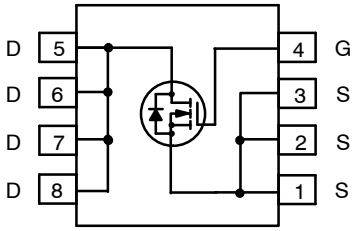
- DC−DC Conversion

### MARKING DIAGRAM




&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code
FDS2672 = Specific Device Code

### PIN ASSIGNMENT




### ABSOLUTE MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 200 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>– Continuous (Note 1a)<br>– Pulsed | <br>3.9<br>50 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 37.5 | mJ |
| $P_D$ | Power Dissipation<br>(Note 1a)<br>(Note 1b) | <br>2.5<br>1.0 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case | (Note 1) | 25 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient | (Note 1a)<br>(Note 1b) | 50<br>125 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| FDS2672 | SOIC8<br>(Pb−Free) | 2500 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

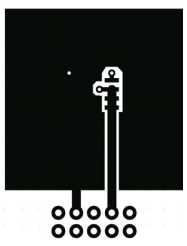
**ELECTRICAL CHARACTERISTICS** $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 200 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | 206 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = 200 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | – | – | 1<br>10 | μA |
| $I_{GSSF}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2 | 2.9 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | −11 | – | mV/°C |
| $r_{DS(on)}$ | Drain to Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.9 A<br>$V_{GS}$ = 6 V, $I_D$ = 3.5 A,<br>$V_{GS}$ = 10 V, $I_D$ = 3.9 A, $T_J$ = 125°C | –<br>–<br>– | 58<br>63<br>124 | 70<br>80<br>148 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3.9 A | – | 15 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 1905 | 2535 | pF |
| $C_{oss}$ | Output Capacitance | | – | 100 | 135 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 30 | 45 | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | – | 0.7 | – | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 100 V, $I_D$ = 3.9 A, $V_{GS}$ = 10 V, $R_{GS}$ = 6 Ω | – | 22 | 35 | ns |
| $t_r$ | Rise Time | | – | 10 | 20 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 35 | 56 | ns |
| $t_f$ | Fall Time | | – | 10 | 20 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at 10 V | $V_{DS}$ = 100 V, $I_D$ = 3.9 A | – | 33 | 46 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | – | 11 | – | nC |
| $Q_{gd}$ | Gate to Drain Charge | | – | 7 | – | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.9 A | – | 0.75 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 3.9 A, $d_{if}$ / $d_t$ = 100 A/ μs | – | 67 | 101 | ns |
| $Q_{rr}$ | Reverse Recovery Change | | – | 179 | 269 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W (10 s) 62.5°C/W steady state when mounted on a 1in$^2$ pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%.
3. Starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = 5 A, $V_{DD}$ = 100 V, $V_{GS}$ = 10 V.

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C UNLESS OTHERWISE NOTED)

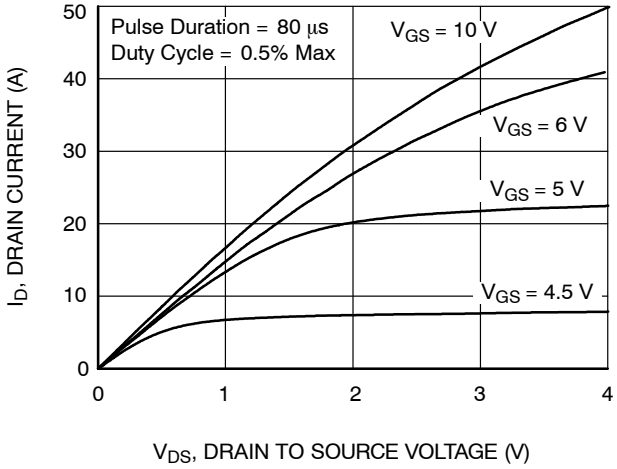



**Figure 1. On−Region Characteristics**

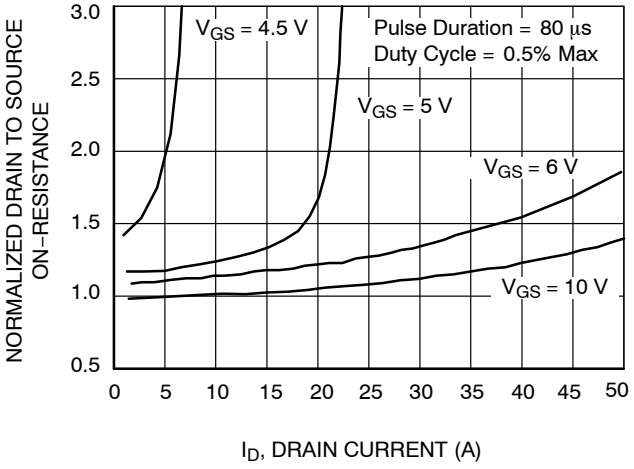



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

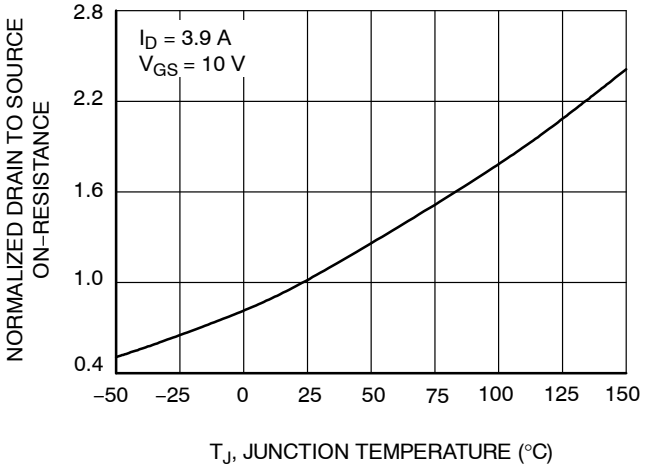



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

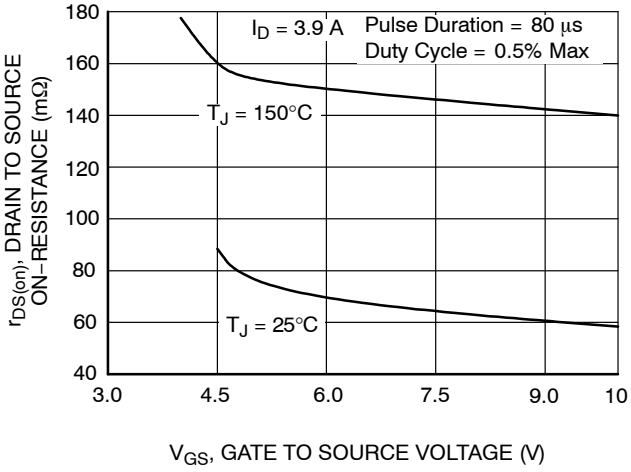



**Figure 4. On−Resistance vs. Gate to Source Voltage**

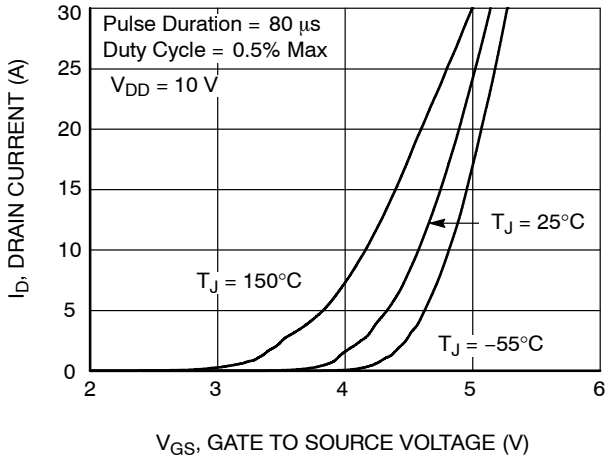



**Figure 5. Transfer Characteristics**

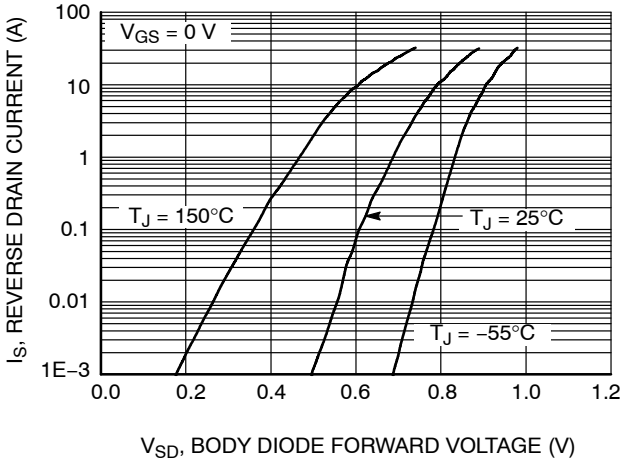



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

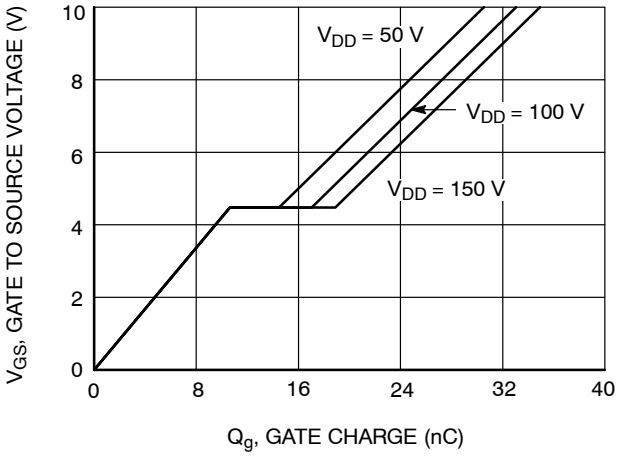



**Figure 7. Gate Charge Characteristics**

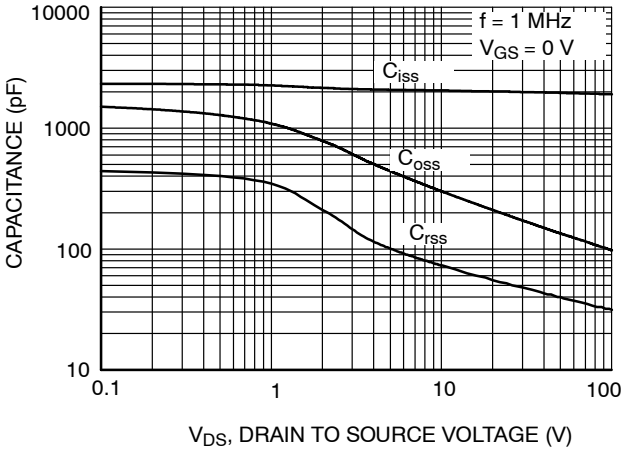



**Figure 8. Capacitance vs. Drain to Source Voltage**

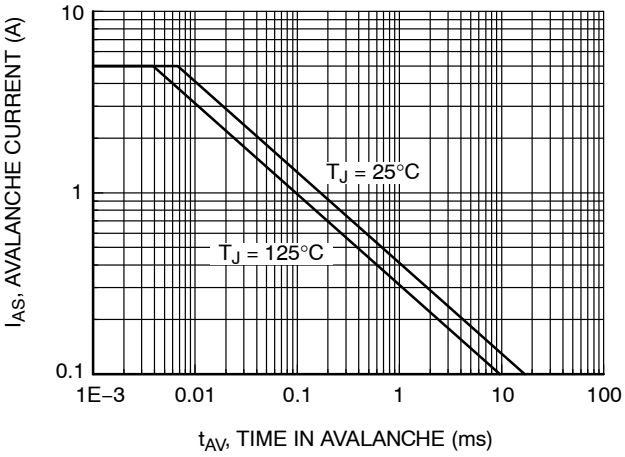



**Figure 9. Unclamped Inductive Switching Capability**

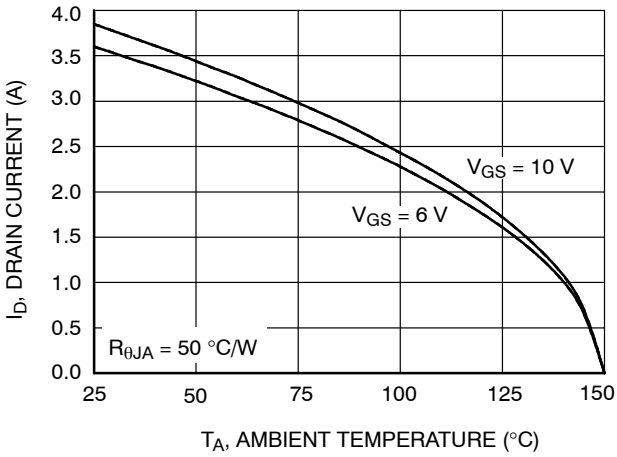



**Figure 10. Ambient Continuous Drain Current vs Case Temperaturee**

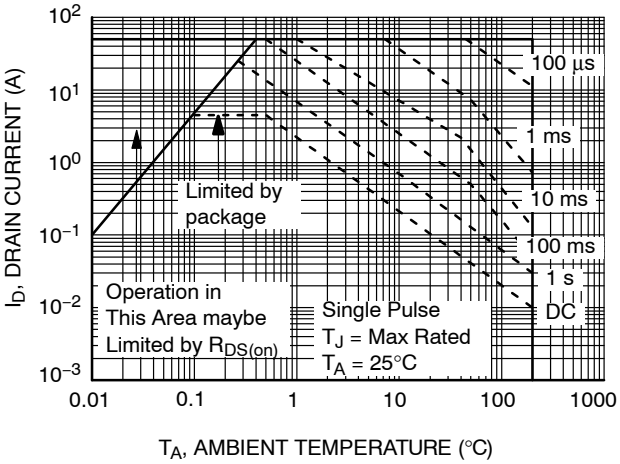



**Figure 11. Forward Bias Safe Operating Area**

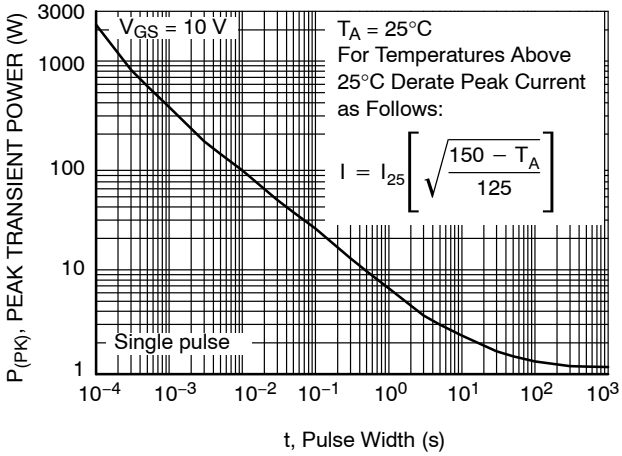



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

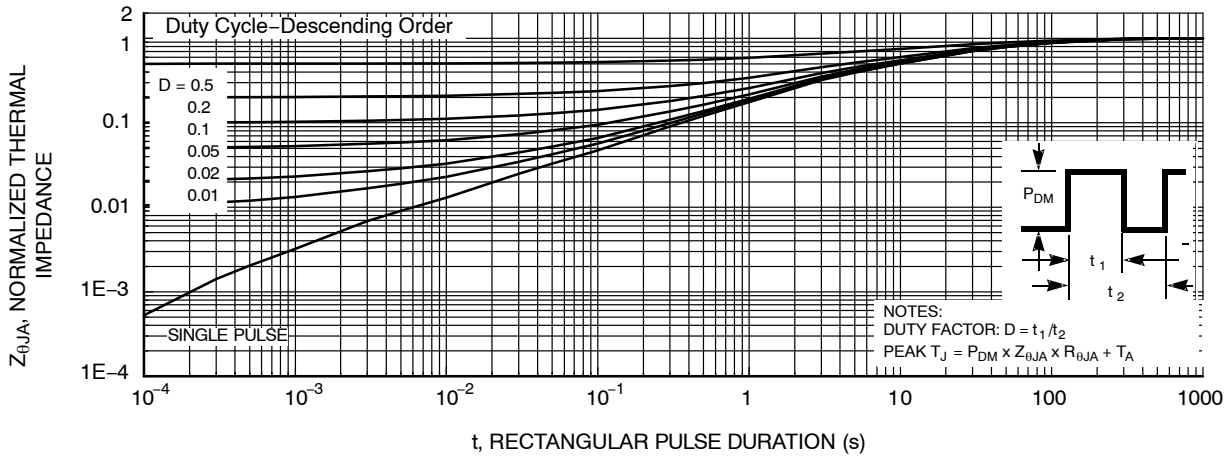
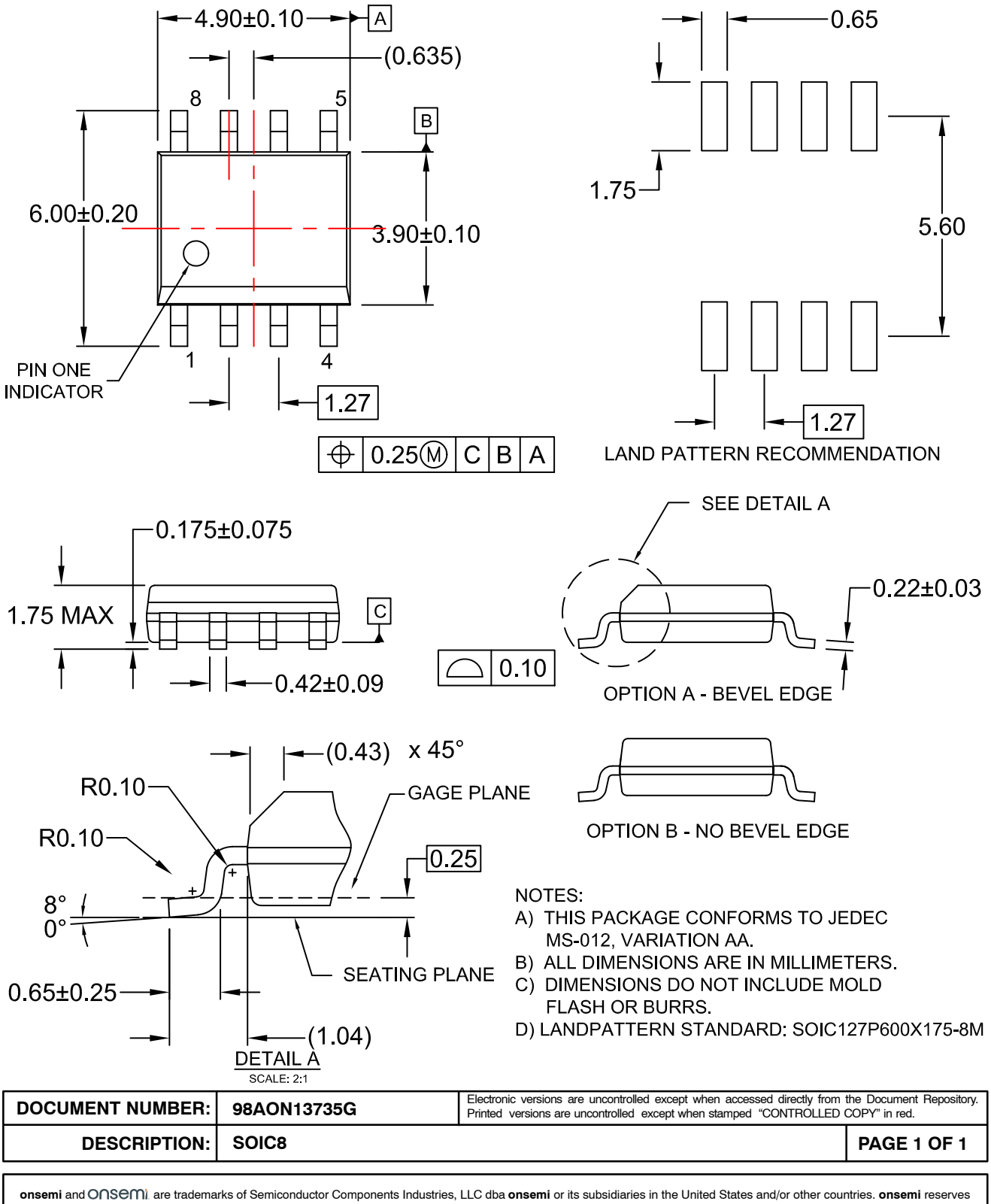



**Figure 13. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

**SOIC8**
CASE 751EB
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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