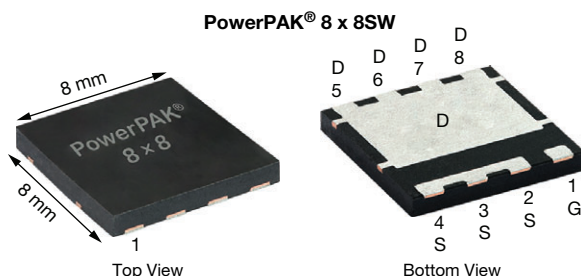


# N-Channel 80 V (D-S) 175 °C MOSFET



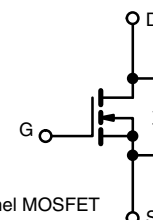
**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## FEATURES

- TrenchFET® Gen III power MOSFET
- Wettable flanks enhances solderability
- Fully lead (Pb)-free device
- Very low  $R_{DS(on)}$
- Very low  $R_{thJC}$
- PowerPAK® 8 x 8 with fuse lead to increase current density
- 100 %  $R_g$  and UIS tested
- Up to 322 A maximum continuous drain current
- Optimized safe operating area / SOA
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- Hot swap
- Load switch
- Oring
- Motor drive
- Battery management



N-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	80
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00175
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.00250
$Q_g$ typ. (nC)	154
$I_D$ (A) <sup>a</sup>	322
Configuration	Single

## ORDERING INFORMATION

Package	PowerPAK® 8 x 8SW
Lead (Pb)-free and halogen-free	SiEH3812EW-T1-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	80	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 175$ °C)	$T_C = 25$ °C	322	A
	$T_C = 70$ °C	269	
	$T_A = 25$ °C	29 <sup>b</sup>	
	$T_A = 70$ °C	24 <sup>b</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	800	A
Continuous source-drain diode current	$T_C = 25$ °C	379	
	$T_A = 25$ °C	3.1 <sup>b</sup>	
Single pulse avalanche current	$L = 0.1$ mH	92	
Single pulse avalanche energy	$E_{AS}$	430	mJ
Maximum power dissipation	$T_C = 25$ °C	417	W
	$T_C = 70$ °C	292	
	$T_A = 25$ °C	3.4 <sup>b</sup>	
	$T_A = 70$ °C	2.4 <sup>b</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	33	44	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	0.27	0.36	

### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	50	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-7	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 μA	1	-	3	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> =0 V	-	-	1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00140	0.00175	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	0.00195	0.00250	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A	-	130	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	7780	-	pF
Output capacitance	C <sub>oss</sub>		-	3145	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	150	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	154	231	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> =20 A	-	74	111	
Gate-drain charge	Q <sub>gd</sub>		-	30	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.8	4	8	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≡ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	16	32	ns
Rise time	t <sub>r</sub>		-	22	45	
Turn-off delay time	t <sub>d(off)</sub>		-	137	275	
Fall time	t <sub>f</sub>		-	49	100	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≡ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	96	195	
Rise time	t <sub>r</sub>		-	166	330	
Turn-off delay time	t <sub>d(off)</sub>		-	96	195	
Fall time	t <sub>f</sub>		-	52	105	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	379	A
Pulse diode forward current	I <sub>SM</sub>		-	-	800	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.72	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	98	200	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	285	570	nC
Reverse recovery fall time	t <sub>a</sub>		-	60	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	38	-	

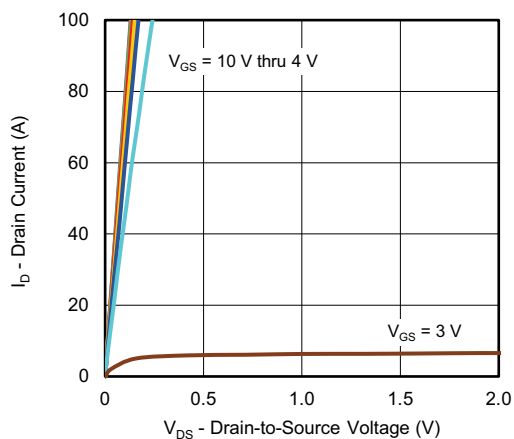
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

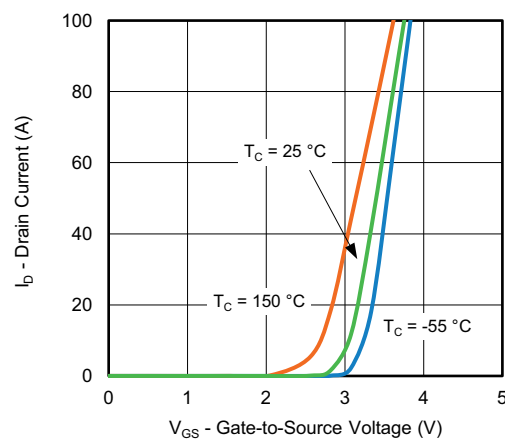
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



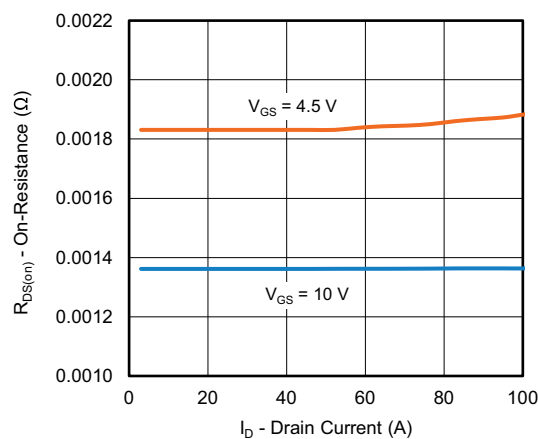
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



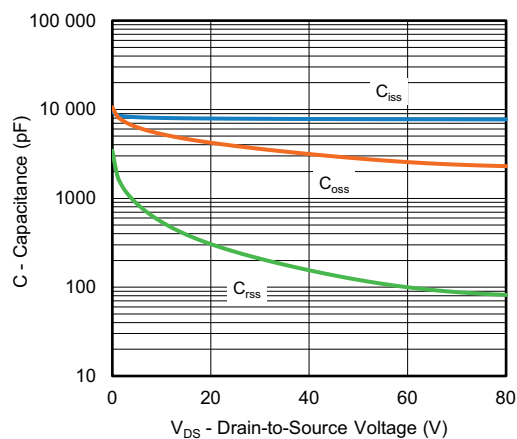
**Output Characteristics**



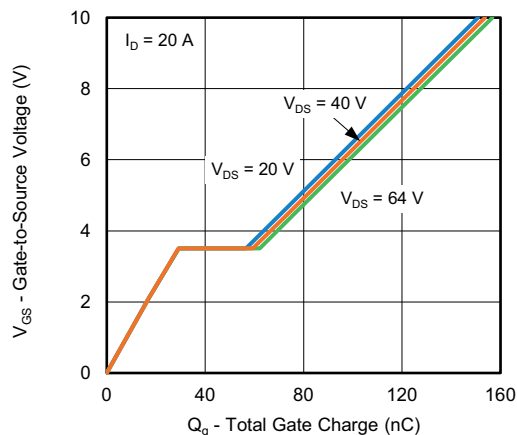
**Transfer Characteristics**



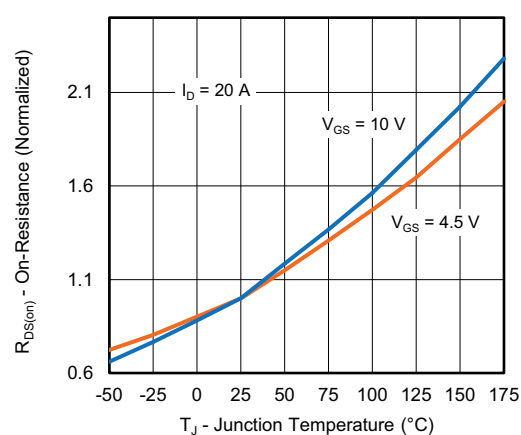
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



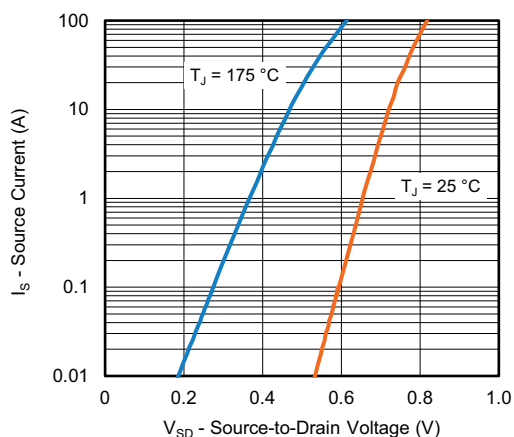
**Gate Charge**



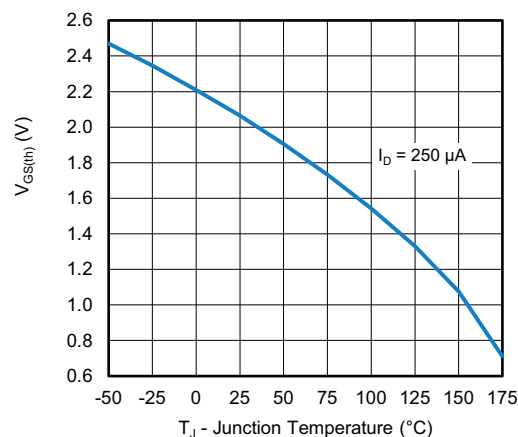
**On-Resistance vs. Junction Temperature**



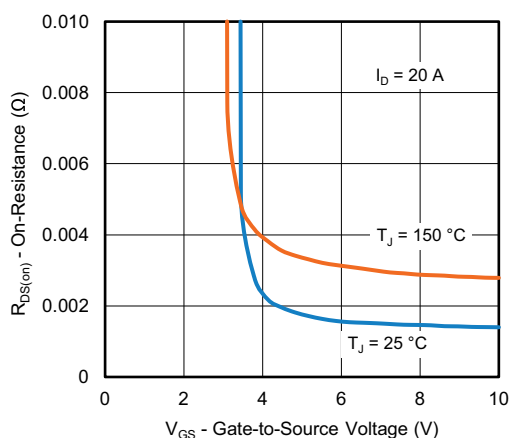
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



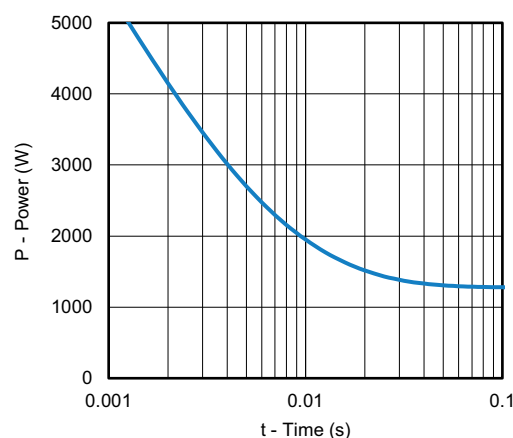
**Source-Drain Diode Forward Voltage**



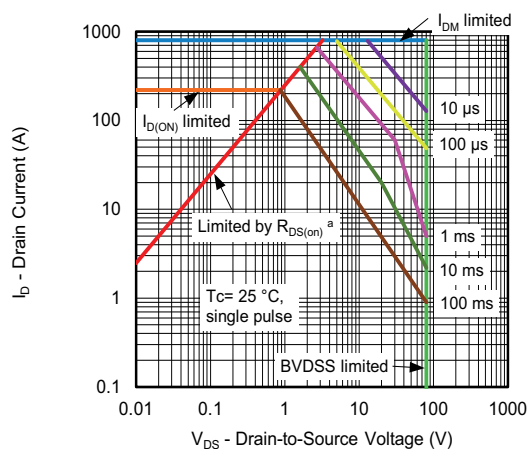
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Case**



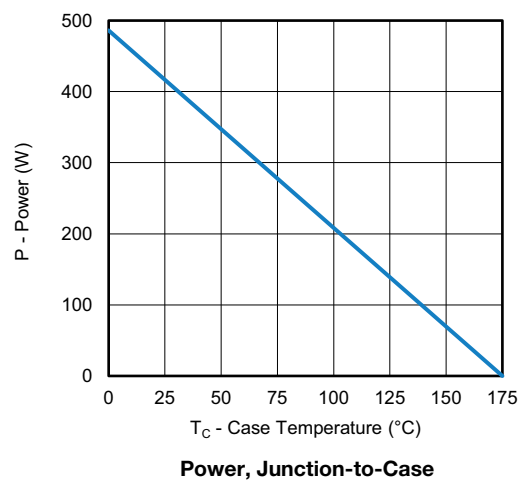
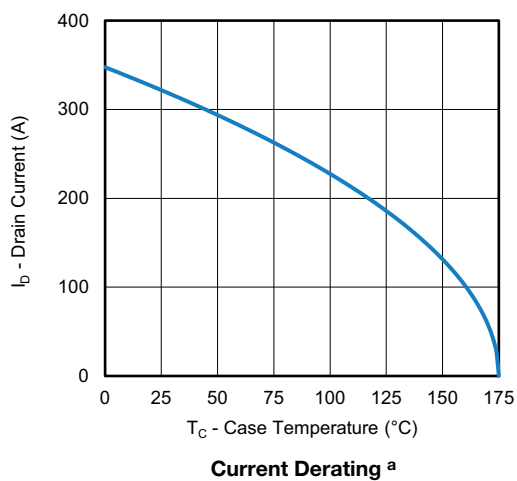
**Safe Operating Area, Junction-to-Case**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

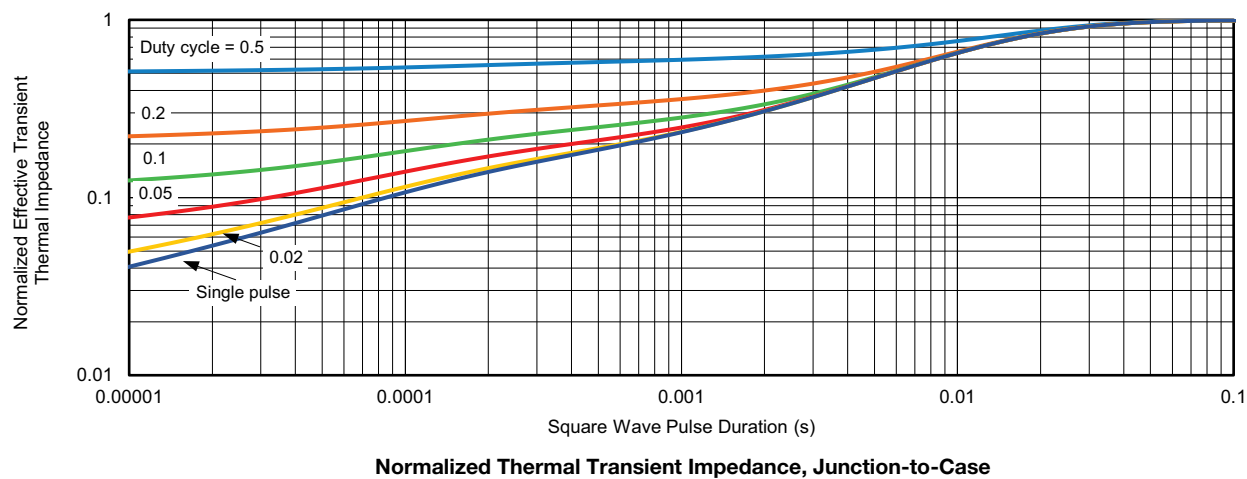


**Note**

- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



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