



PSMN1R0-80CSE

N-channel, 80 V, 0.95 mOhm, MOSFET with enhanced SOA in CCPAK1212i package

6 December 2024

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a CCPAK1212i package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN1R0-80CSE delivers very low $R_{DS(on)}$ and enhanced safe operating area performance in a high-reliability copper-clip package (CCPAK1212i).

PSMN1R0-80CSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DS(on)}$ for low I^2R conduction losses
- CCPAK1212i package for applications that demand the highest performance and reliability
- Inverted package, suitable for top-side cooling

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

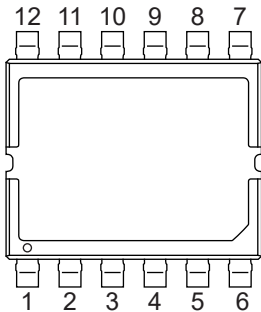
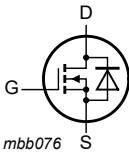
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	495	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	1.55	kW
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.76	0.95	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	13	42.5	98	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/μs}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	-	101	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>sot8005a_sv</p> <p>CCPAK1212i (SOT8005A)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	G	gate		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-80CSE	CCPAK1212i	Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body	SOT8005A

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-80CSE	XP1E0S80C

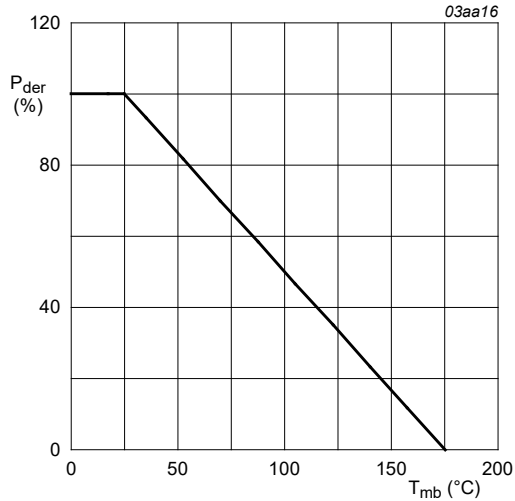
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

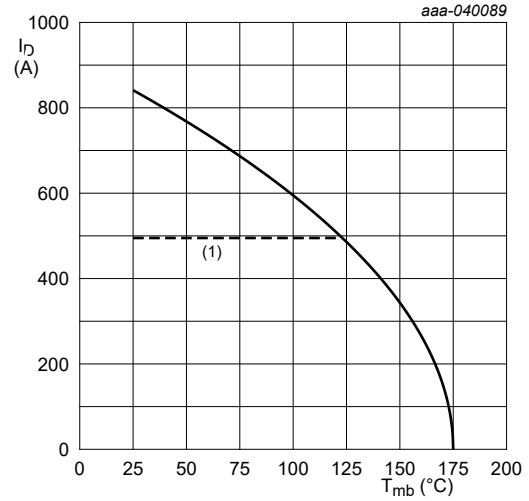
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	80	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	1.55	kW
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2		-	495	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	495	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	3365	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	420	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	3365	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 129\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 282\text{ }\mu\text{s}$; Fig. 4	[1]	-	1890	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	129	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

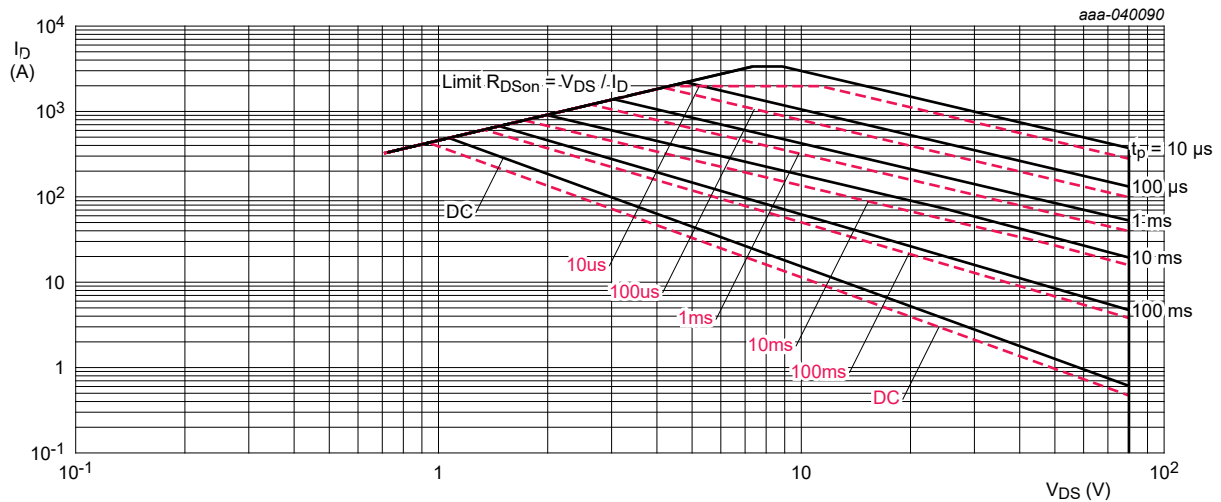
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

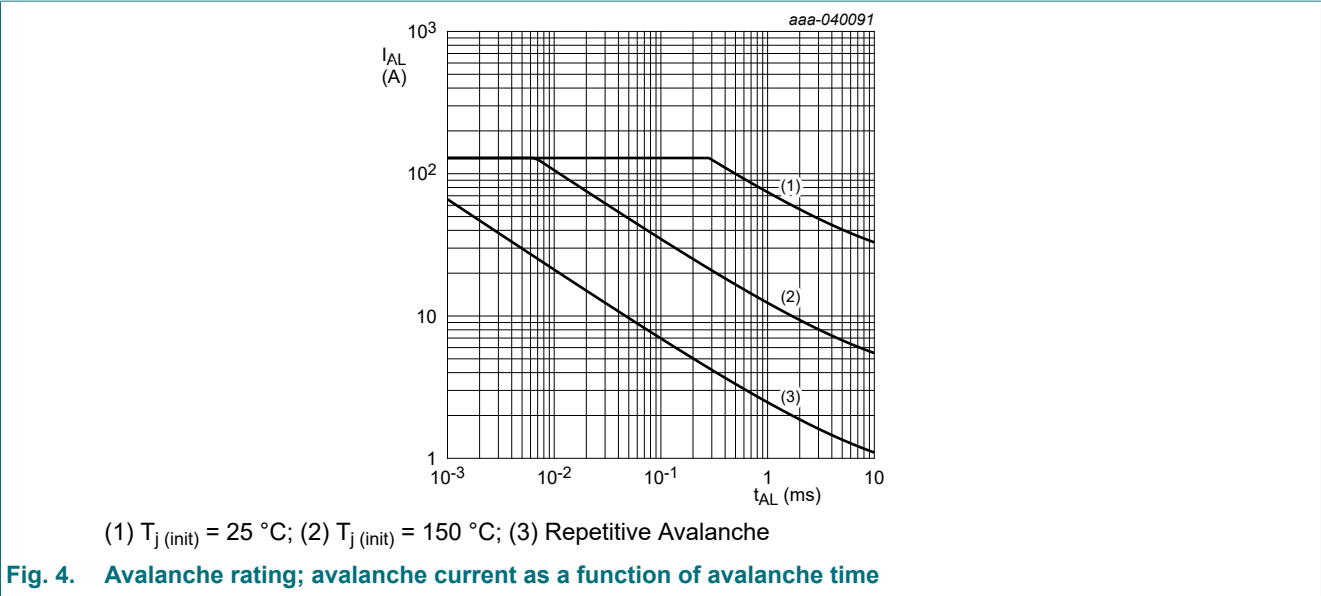
(1) 495 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25\text{ }^\circ\text{C}$ (solid black line); $T_{mb} = 125\text{ }^\circ\text{C}$ (red dashed line); I_{DM} is a single pulse

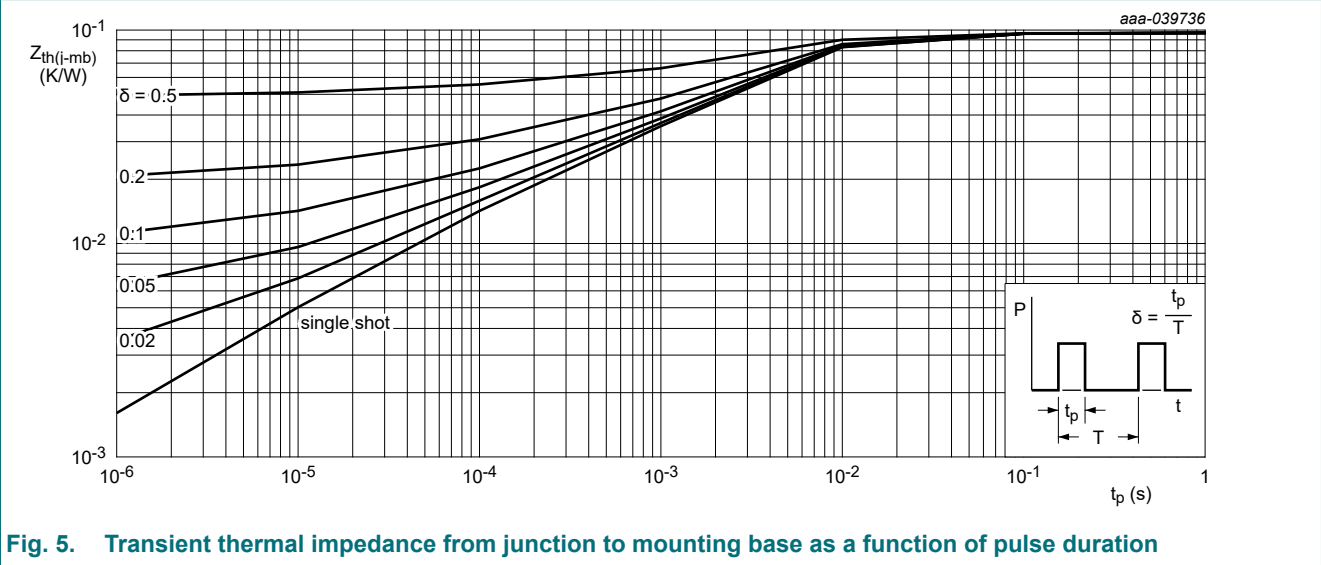
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

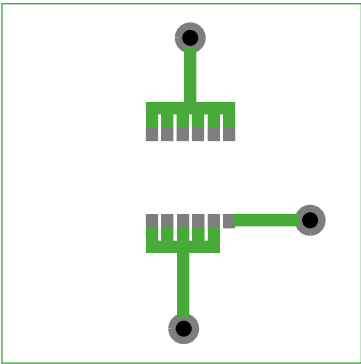


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.075	0.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	58	-	K/W
		Fig. 7		-	29	-	K/W

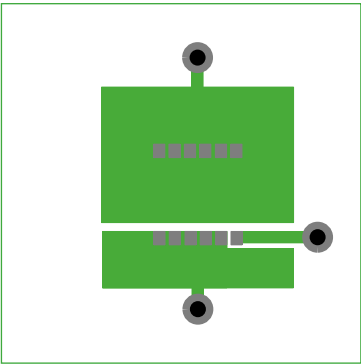




aaa-040399

70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



aaa-040400

Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		80	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		72	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C		2	2.8	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C		-	1.71	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C		-	3.2	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C		-	-6.92	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _J = 25 °C		-	0.19	2	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 125 °C		-	42	200	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 11		-	0.76	0.95	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 12		-	1.2	1.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 12		-	1.6	2.2	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.67	1.35	2.69	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		168	336	504	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C		-	305	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		68	113	158	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	74.5	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	38	-	nC
Q _{GD}	gate-drain charge			13	42.5	98	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	4.5	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 0.5 MHz; T _J = 25 °C; Fig. 15		15772	26287	36802	pF
C _{oss}	output capacitance			3684	6139	9823	pF
C _{rss}	reverse transfer capacitance			16	163	489	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	95	-	ns
t _r	rise time			-	84	-	ns
t _{d(off)}	turn-off delay time			-	205	-	ns
t _f	fall time			-	107	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.76	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	75	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	101	-	nC

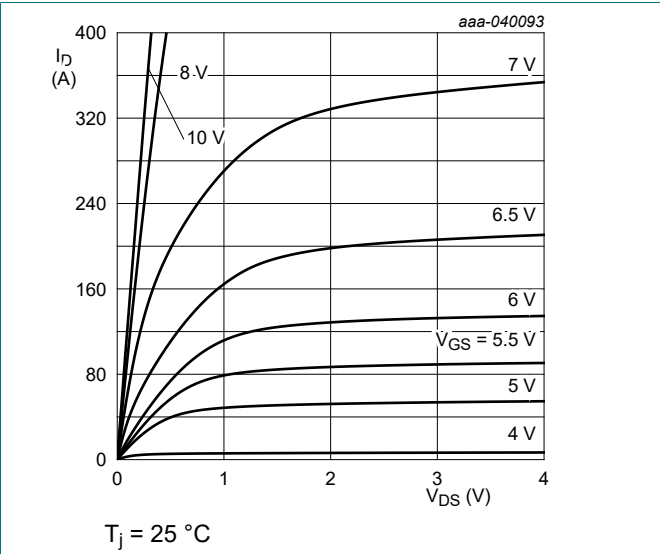


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

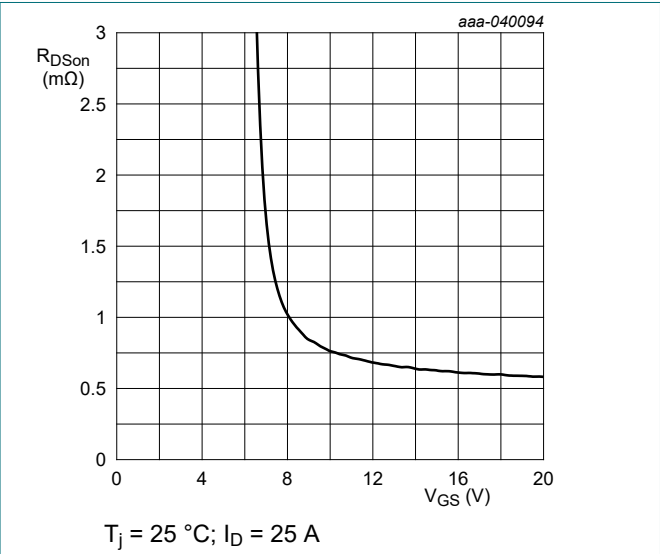


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

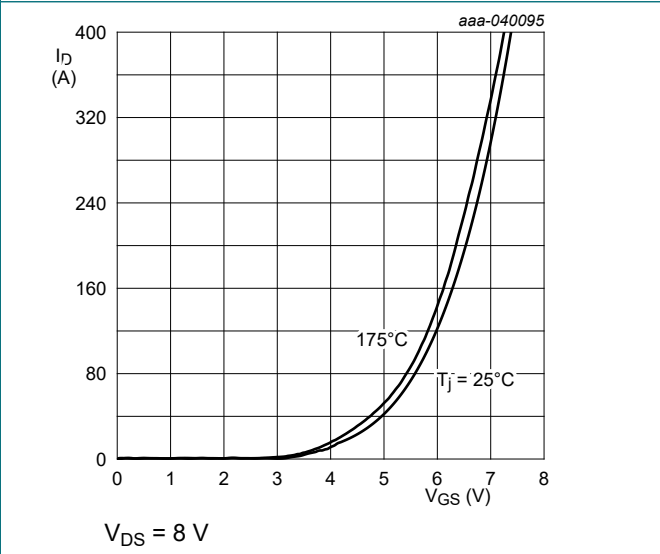


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

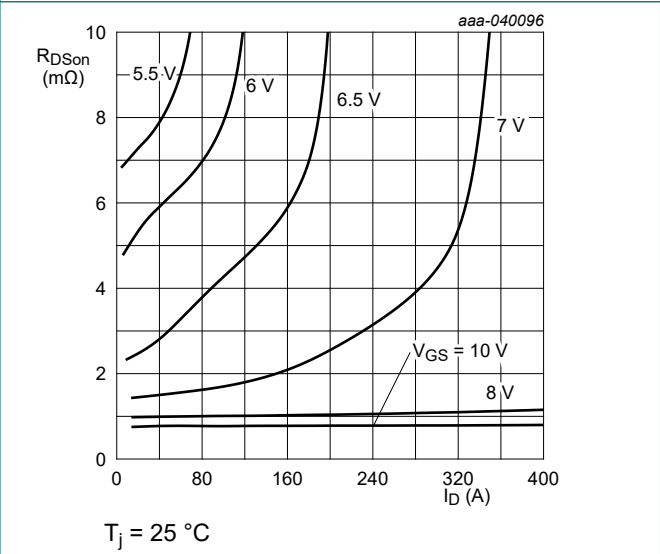


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

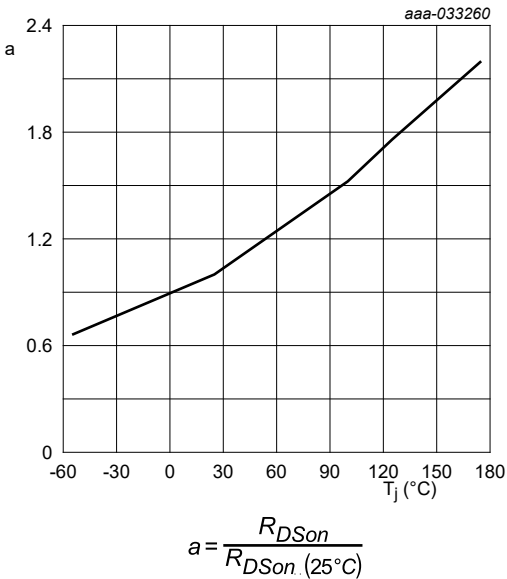


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

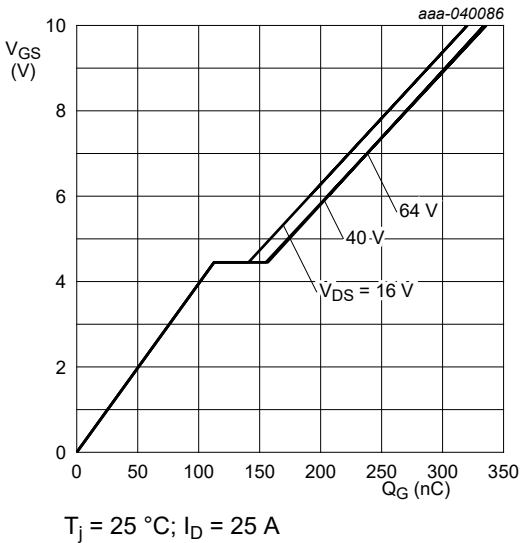


Fig. 13. Gate-source voltage as a function of gate charge; typical values

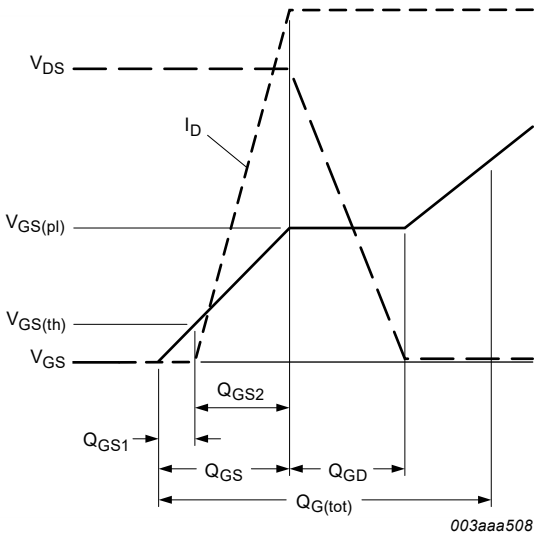


Fig. 14. Gate charge waveform definitions

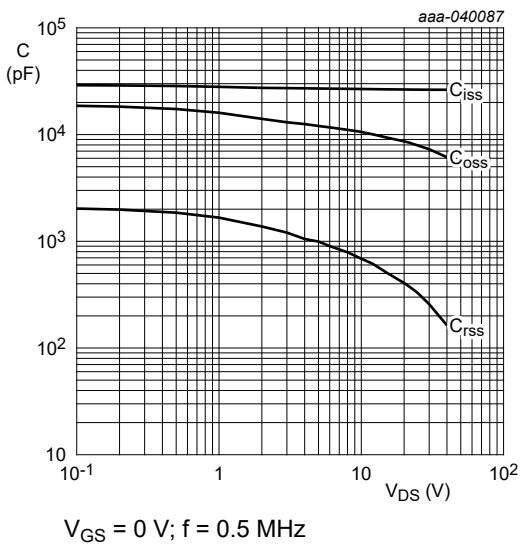


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

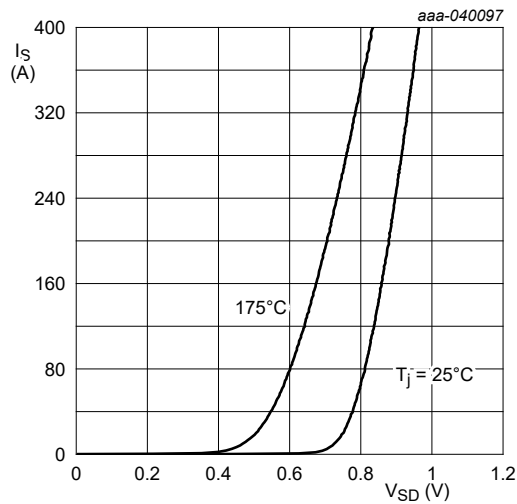


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

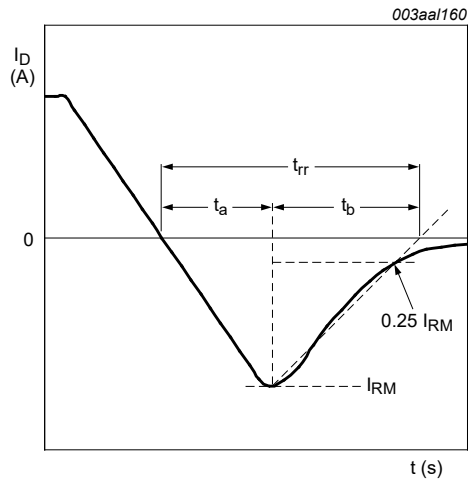
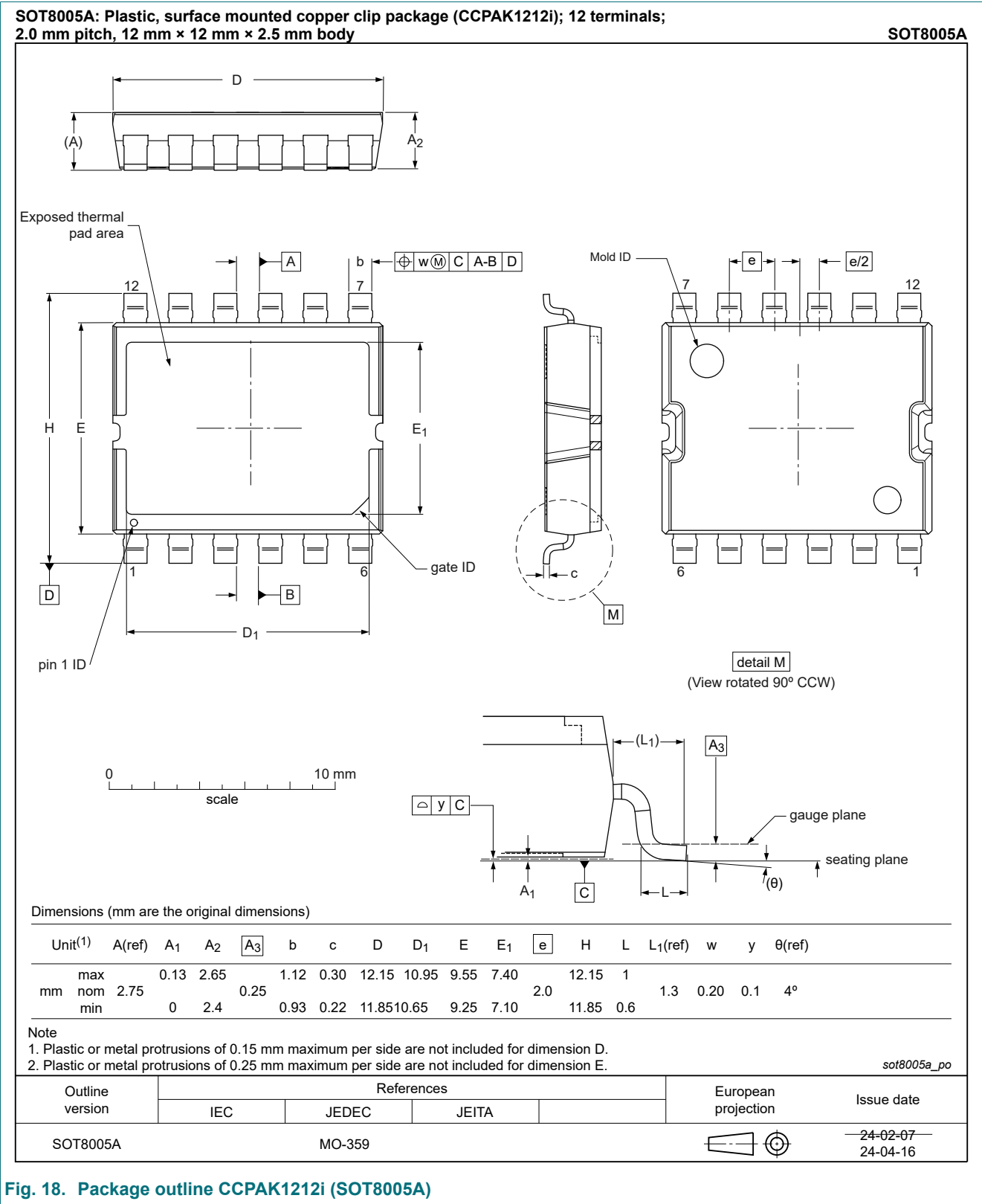


Fig. 17. Reverse recovery timing definition

11. Package outline



12. Soldering

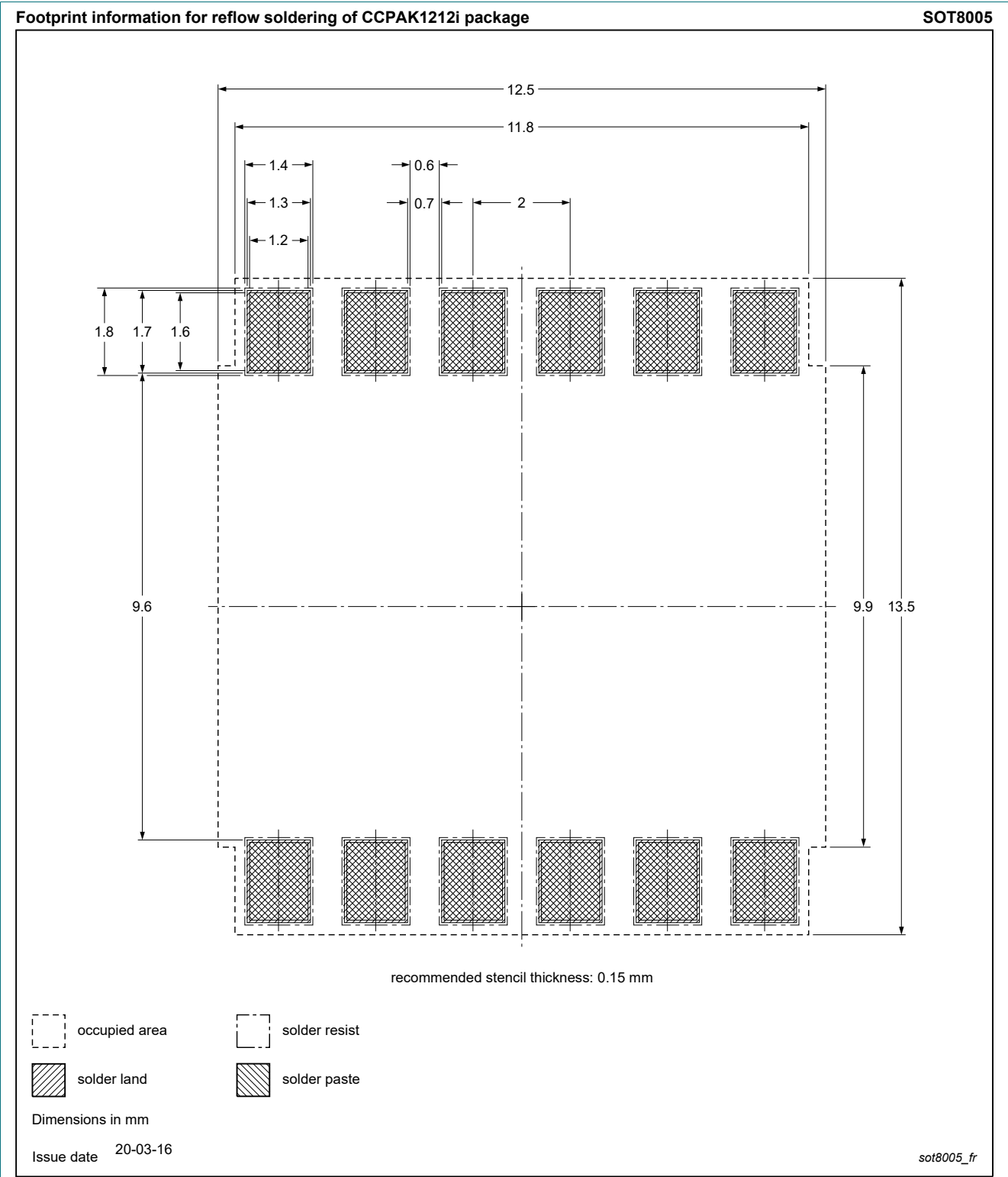


Fig. 19. Reflow soldering footprint for CCPAK1212i (SOT8005A)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking..... 3

8. Limiting values..... 3

9. Thermal characteristics..... 5

10. Characteristics..... 7

11. Package outline..... 11

12. Soldering..... 12

13. Legal information.....13

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