

OptiMOS™-5 Power-Transistor



Features

- N-channel - Enhancement mode - Logic level
- AEC qualified
- MSL1 up to 260°C peak reflow
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

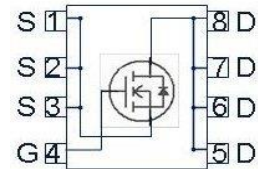
Product Summary

V_{DS}	100	V
$R_{DS(on)}$	4	mΩ
I_D	100	A

PG-TDSON-8



Type	Package	Marking
IAUC100N10S5L040	PG-TDSON-8	5N10L040



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	100	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}$	100	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	400	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$	150	mJ
Avalanche current, single pulse	I_{AS}	-	86	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$, $T_J=175\text{ °C}$	167	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	-	-	-	0.9	K/W
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=90\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125\text{ °C}^{2)}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=50\text{ A}$	-	4.3	5.7	m Ω
		$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	3.3	4	
Gate resistance ²⁾	R_G		-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	4000	5200	pF
Output capacitance	C_{oss}		-	660	860	
Reverse transfer capacitance	C_{rss}		-	28	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\Omega$	-	6	-	ns
Rise time	t_r		-	3	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	21	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=50\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	13	16	nC
Gate to drain charge	Q_{gd}		-	11	16	
Gate charge total	Q_g		-	60	78	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V

Reverse Diode

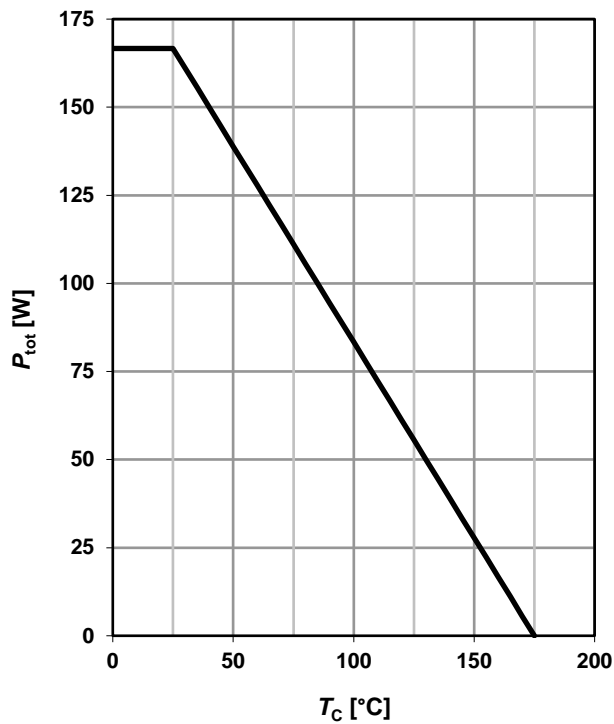
Diode continuous forward current ²⁾	I_S	$T_C=25^\circ\text{C}$	-	-	100	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_J=25^\circ\text{C}$	-	0.9	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	61	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	92	-	nC

¹⁾ Current is limited by package; with an $R_{thJC}=0.9\text{ K/W}$ the chip is able to carry 140A at 25°C.

²⁾ Defined by design. Not subject to production test.

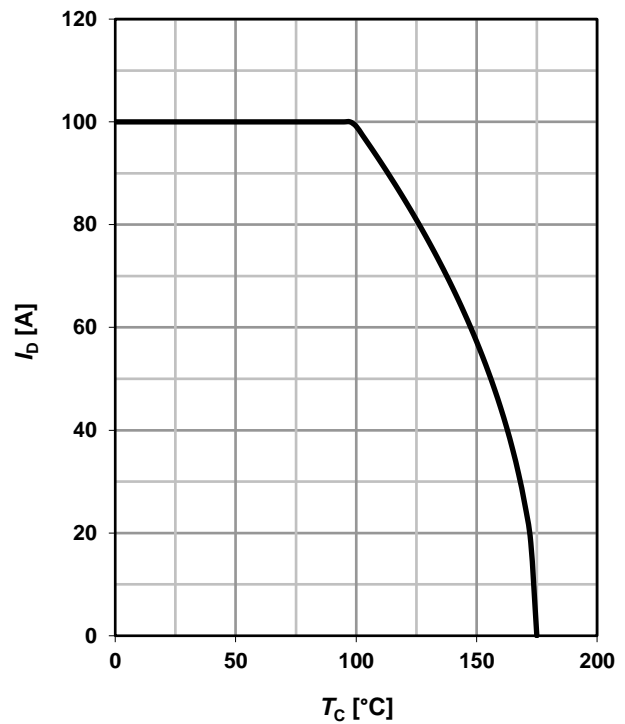
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

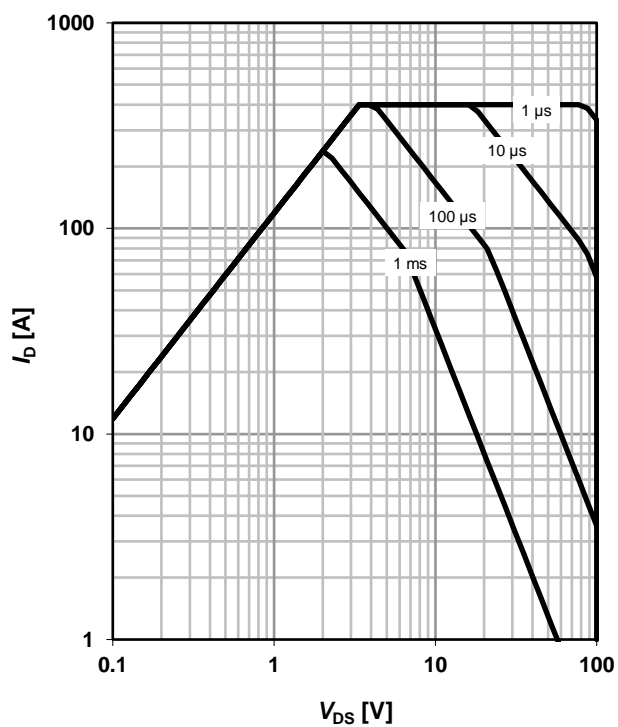
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

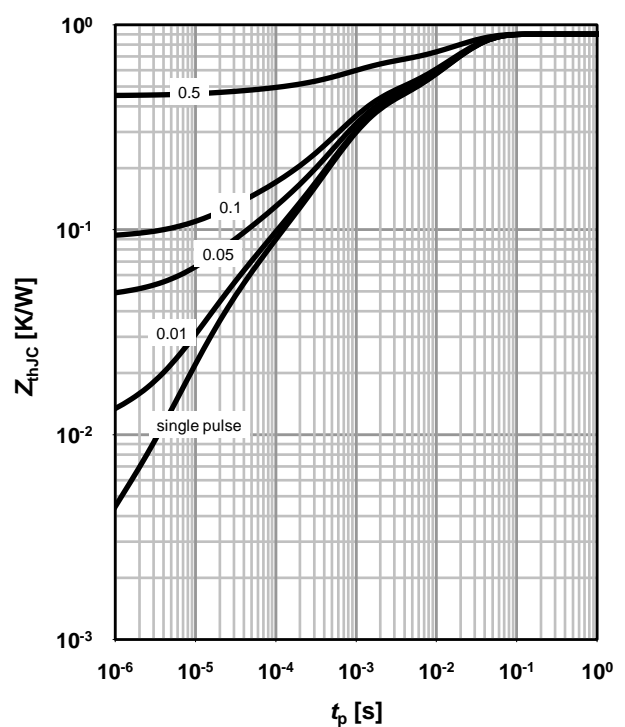
parameter: t_p



4 Max. transient thermal impedance

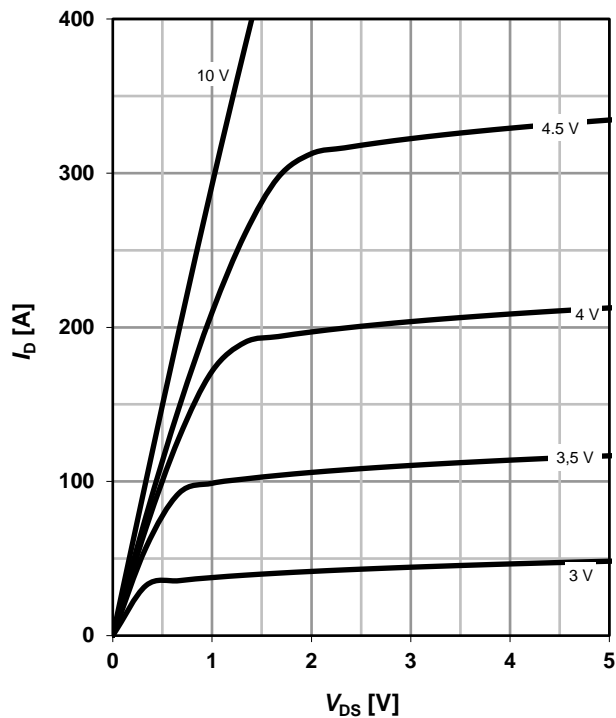
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



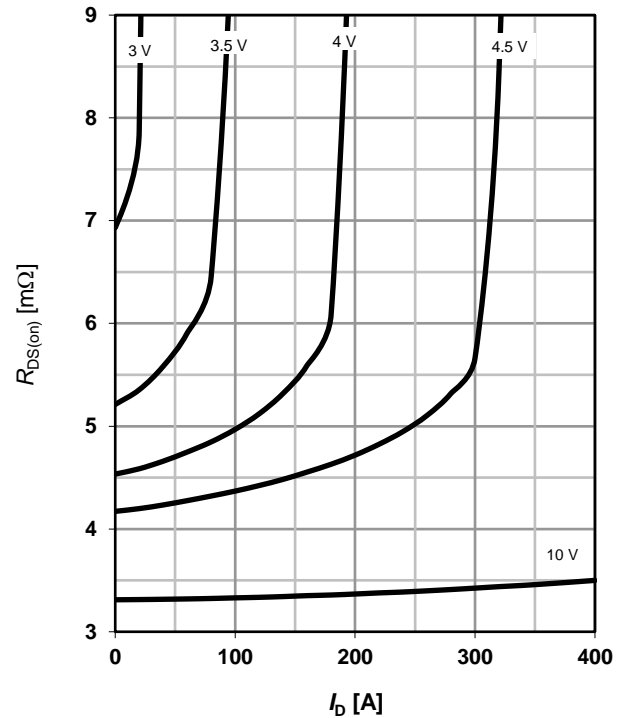
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


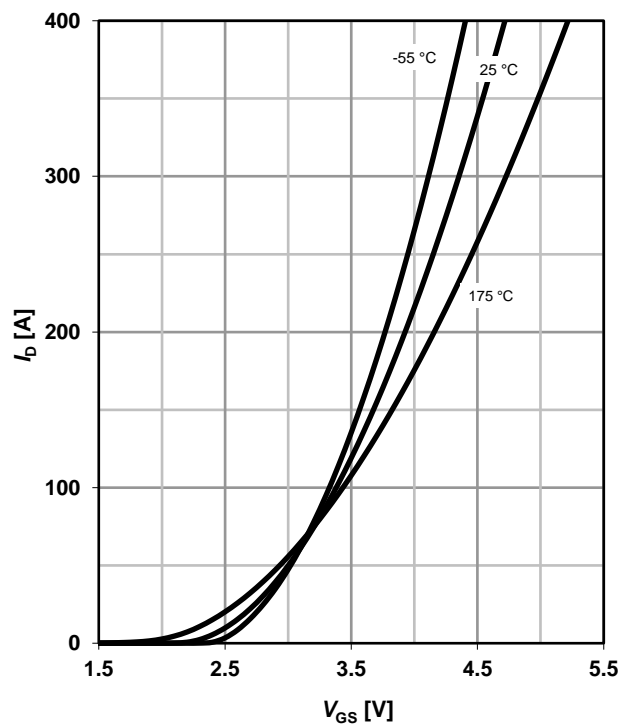
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


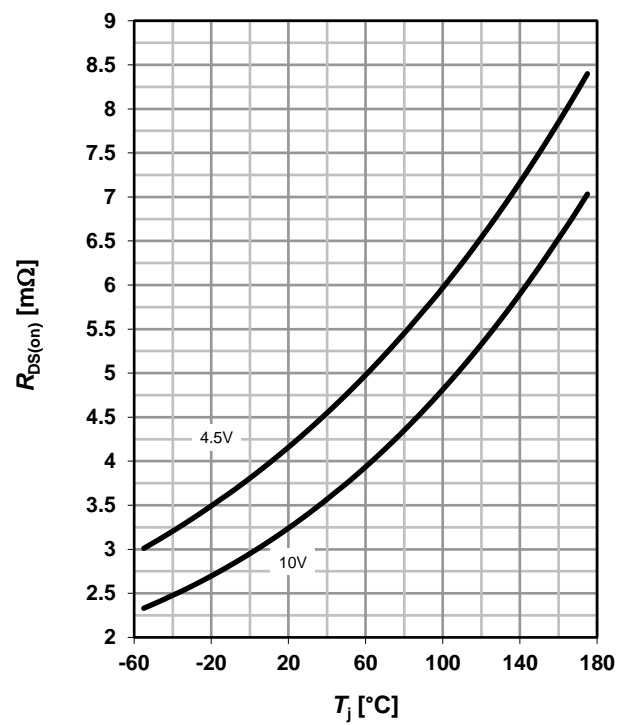
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


8 Typ. drain-source on-state resistance

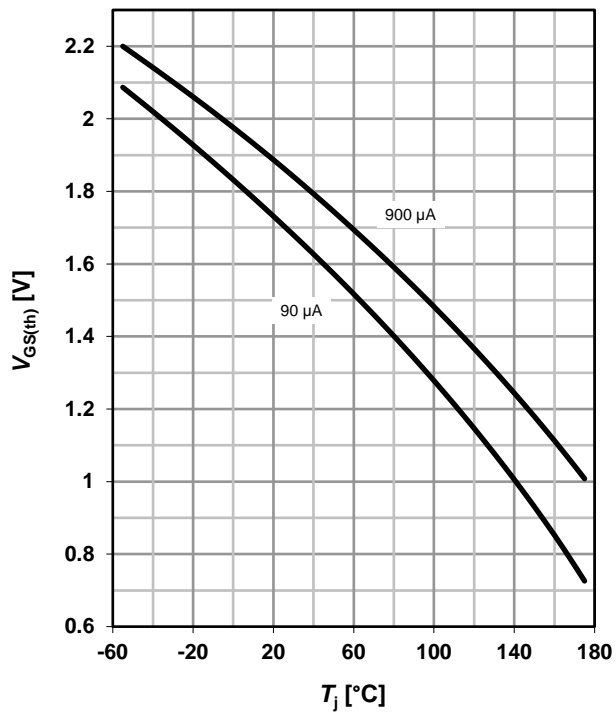
 $R_{DS(on)} = f(T_j); I_D = 50\text{ A}$

parameter: V_{GS}


9 Typ. gate threshold voltage

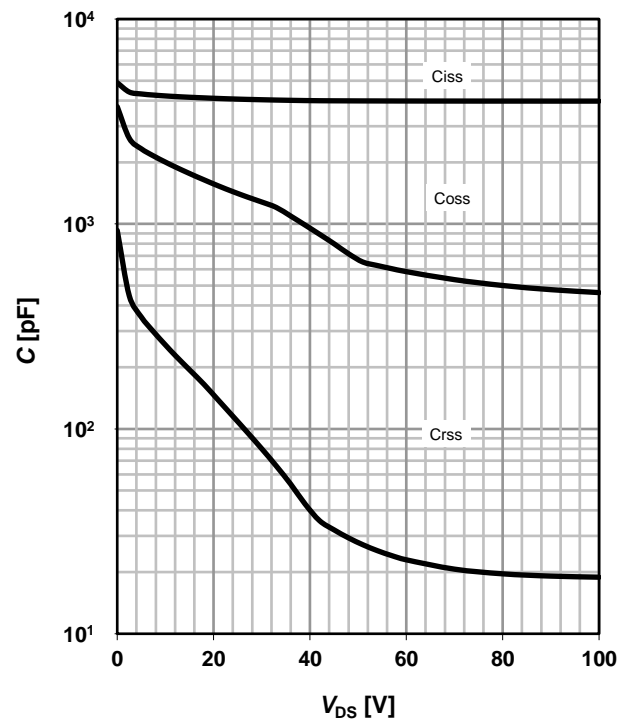
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

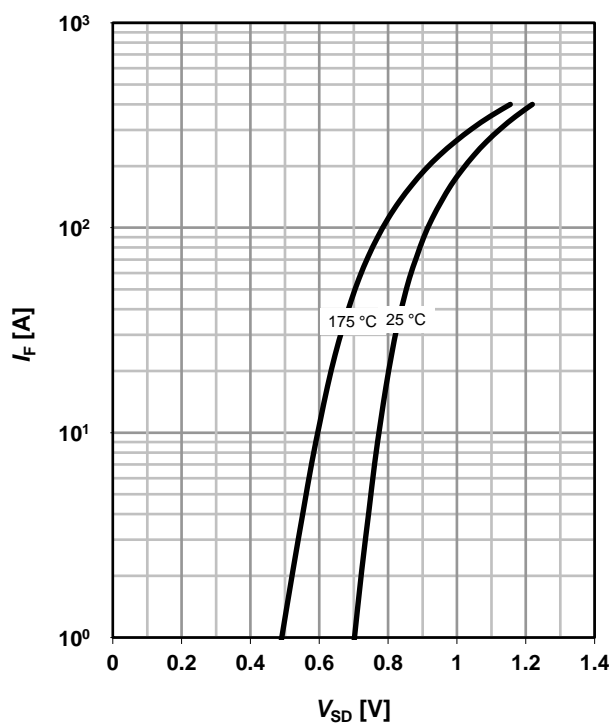
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

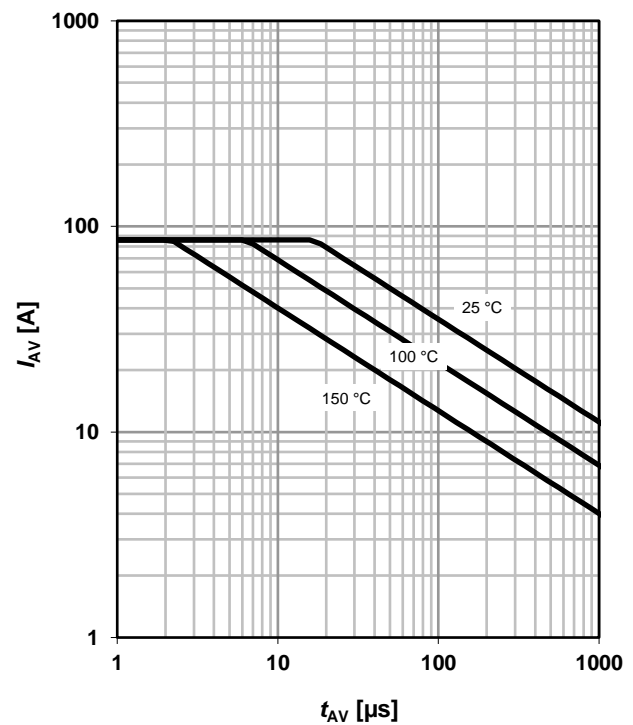
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

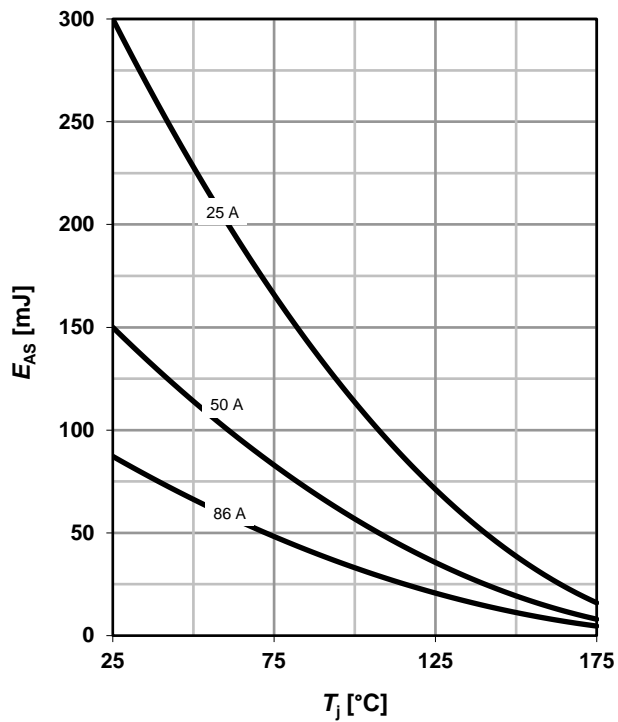
parameter: $T_{j(start)}$



13 Typical avalanche energy

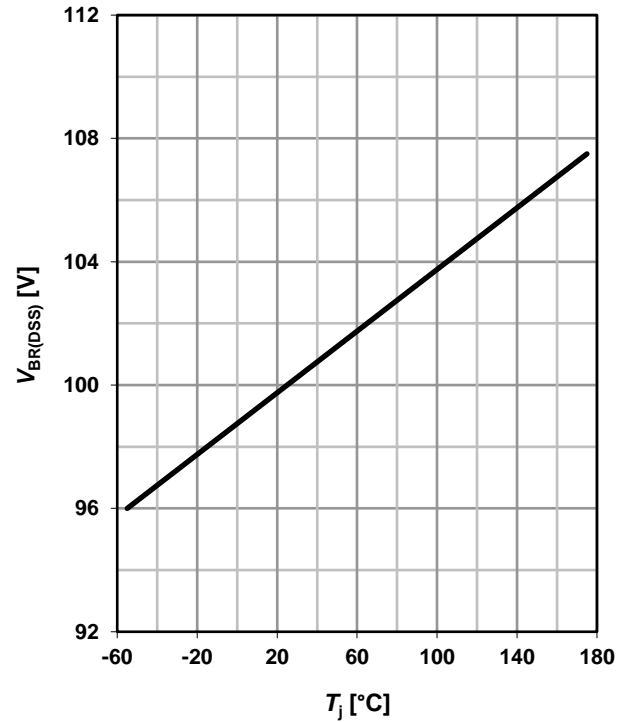
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

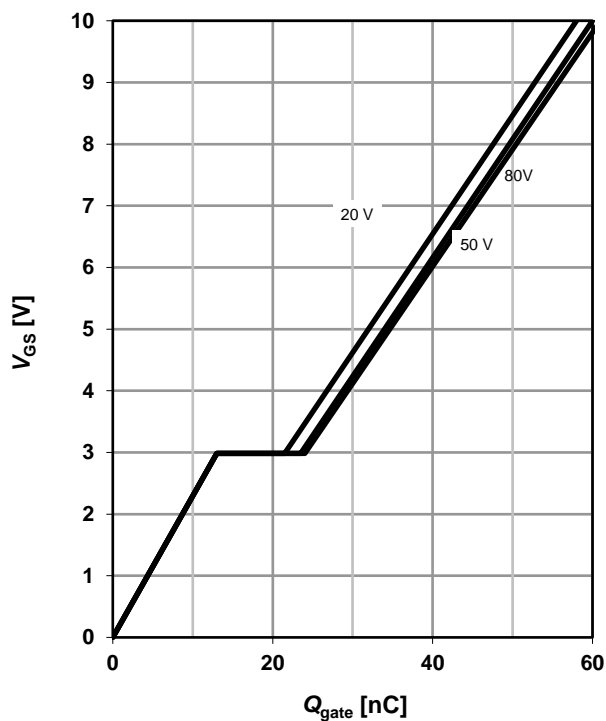
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



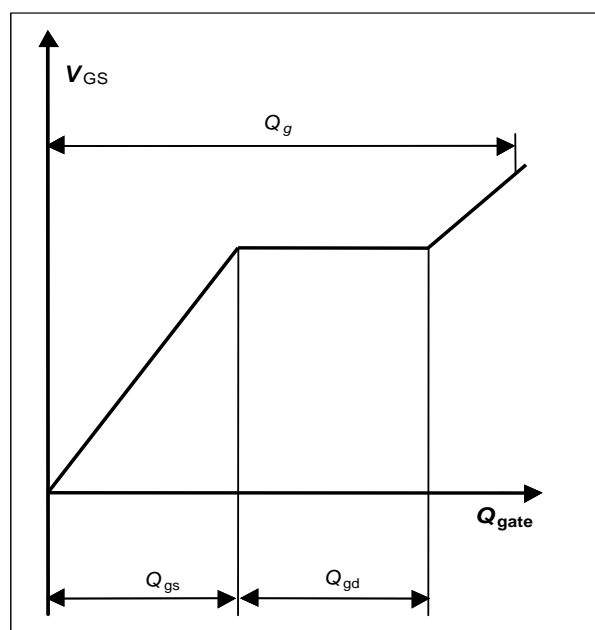
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	12.06.2018	Final Data Sheet