

# RJK0853DPB

80V, 40A, 8.0mΩ max.

Silicon N Channel Power MOS FET

Power Switching

R07DS0081EJ0300

Rev.3.00

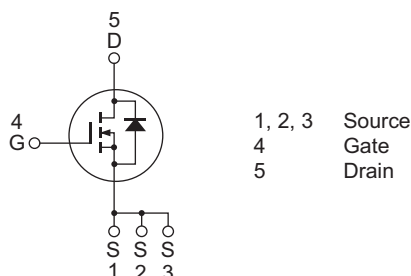
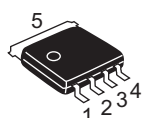
Apr 09, 2013

## Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 6.2 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )
- Pb-free
- Halogen-free

## Outline

RENESAS Package code: PTZZ0005DA-A  
(Package name: LPAK)



## Application

- Switching Mode Power Supply

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	80	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	40	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	160	A
Body-drain diode reverse drain current	$I_{DR}$	40	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	20	A
Avalanche energy	$E_{AS}$ <sup>Note 2</sup>	53.3	mJ
Channel dissipation	$P_{ch}$ <sup>Note 3</sup>	65	W
Channel to Case Thermal Resistance	$\theta_{ch-C}$	1.92	$^\circ\text{C/W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
2. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
3.  $T_c = 25^\circ\text{C}$

This product is for the low voltage drive ( $\leq 10\text{V}$ ).

If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ( $V_{GS(off)}$ ) which characteristics has been improved.

## Electrical Characteristics

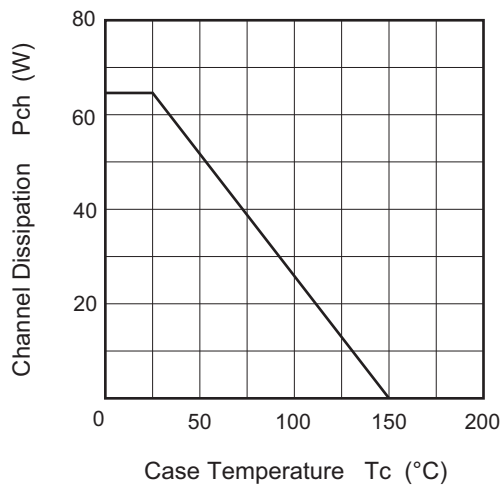
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	80	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0 \text{ V}$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 80 \text{ V}$ , $V_{GS} = 0 \text{ V}$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.2	8.0	$\text{m}\Omega$	$I_D = 20 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	6.7	9.2	$\text{m}\Omega$	$I_D = 20 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	100	—	S	$I_D = 20 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	6170	—	pF	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	600	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	235	—	pF	
Gate Resistance	$R_g$	—	0.5	—	$\Omega$	
Total gate charge	$Q_g$	—	40	—	nC	$V_{DD} = 25 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$ , $I_D = 40 \text{ A}$
Gate to source charge	$Q_{gs}$	—	19	—	nC	
Gate to drain charge	$Q_{gd}$	—	11	—	nC	
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$ , $V_{DD} \cong 30 \text{ V}$ , $R_L = 1.5 \Omega$ , $R_g = 4.7 \Omega$
Rise time	$t_r$	—	7.2	—	ns	
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	$t_f$	—	12	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.82	1.1	V	$I_F = 40 \text{ A}$ , $V_{GS} = 0 \text{ V}$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	42	—	ns	$I_F = 40 \text{ A}$ , $V_{GS} = 0 \text{ V}$ , $di_F/dt = 100 \text{ A}/\mu\text{s}$

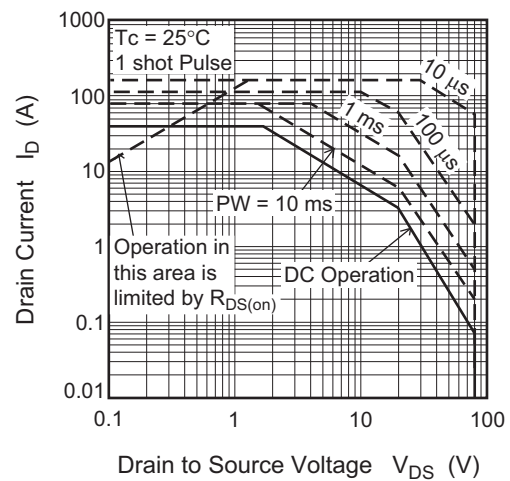
Notes: 4. Pulse test

## Main Characteristics

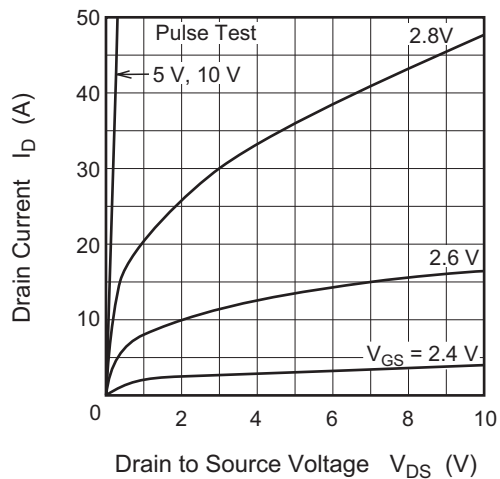
Power vs. Temperature Derating



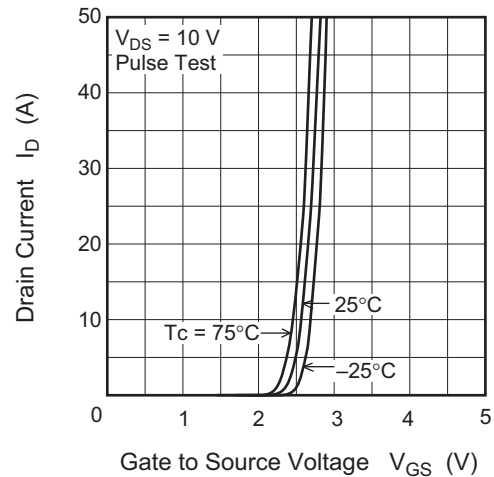
Maximum Safe Operation Area



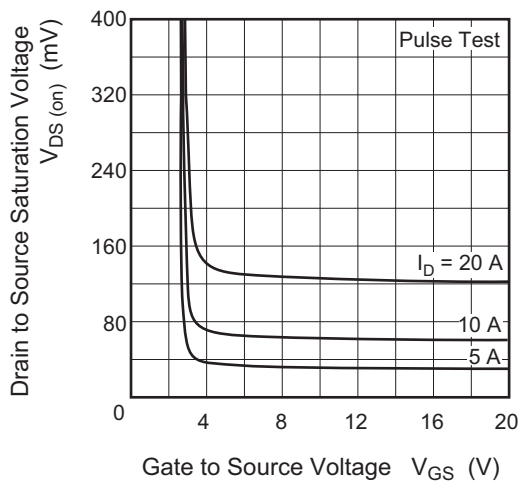
Typical Output Characteristics



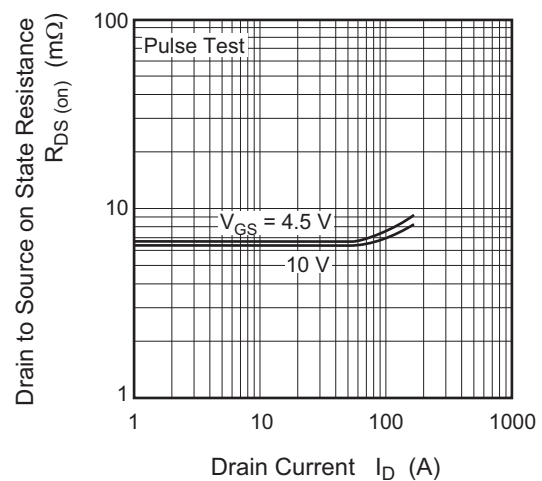
Typical Transfer Characteristics



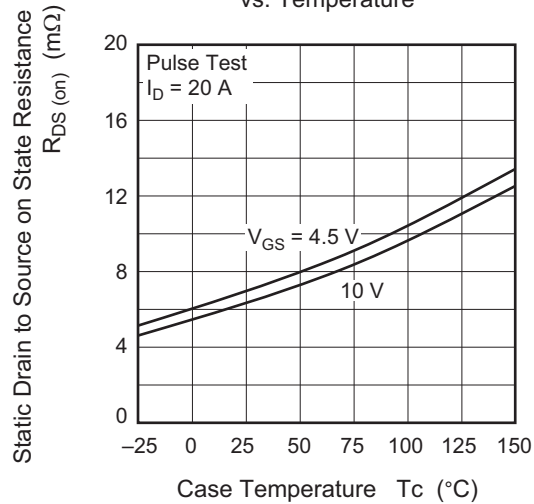
Drain to Source Saturation Voltage vs. Gate to Source Voltage



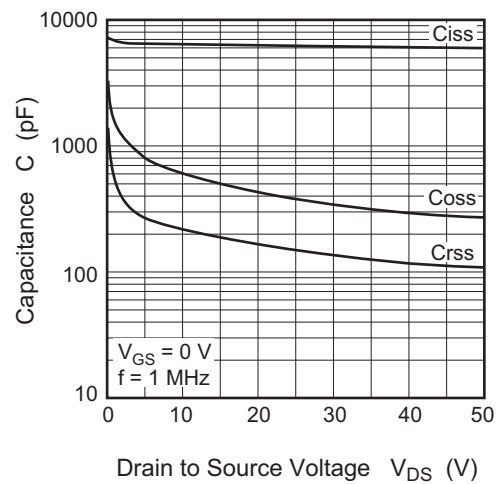
Static Drain to Source on State Resistance vs. Drain Current



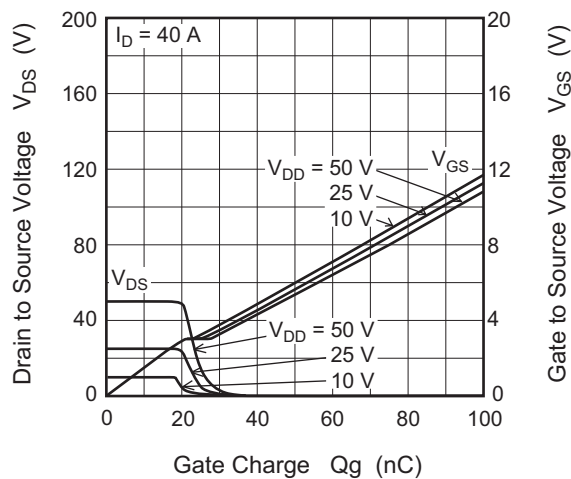
Static Drain to Source on State Resistance vs. Temperature



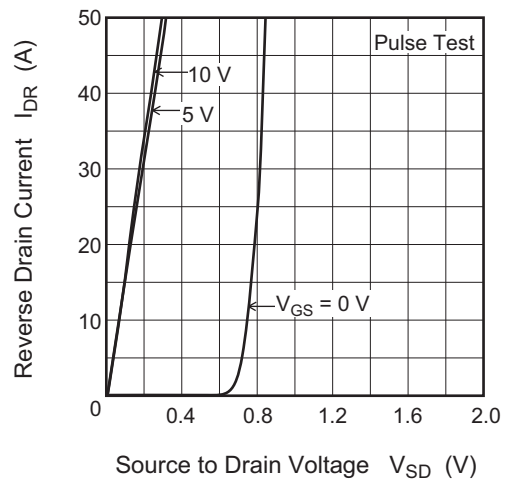
Typical Capacitance vs. Drain to Source Voltage



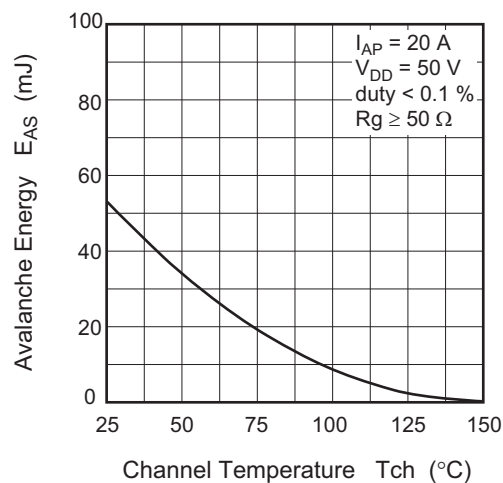
Dynamic Input Characteristics



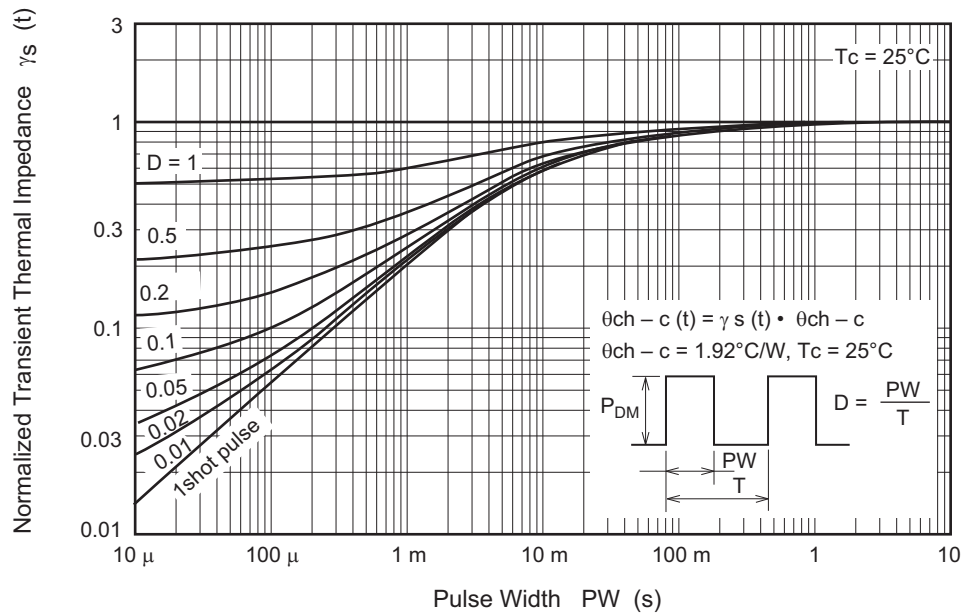
Reverse Drain Current vs. Source to Drain Voltage



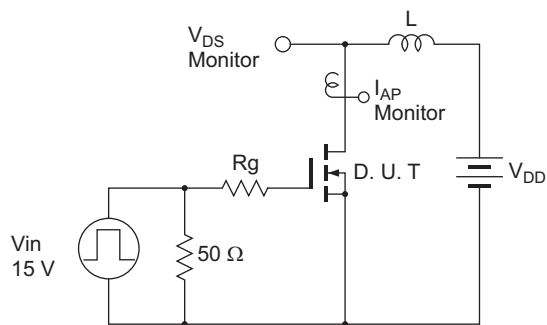
Maximum Avalanche Energy vs. Channel Temperature Derating



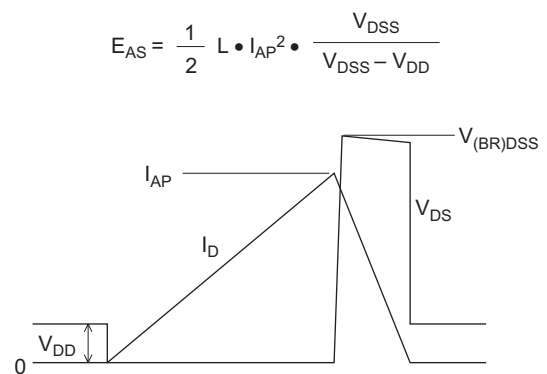
Normalized Transient Thermal Impedance vs. Pulse Width



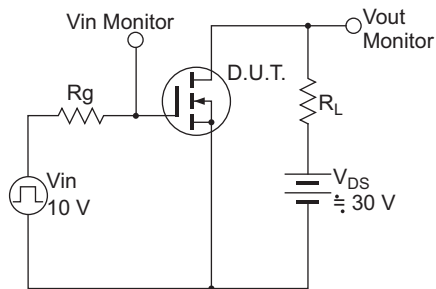
Avalanche Test Circuit



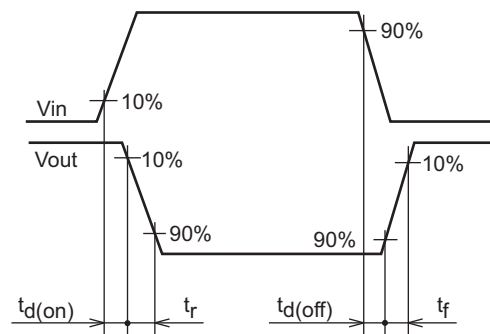
Avalanche Waveform



Switching Time Test Circuit



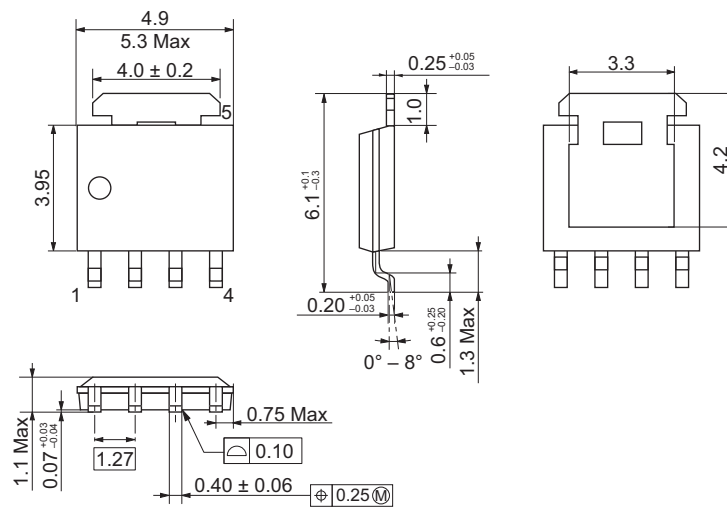
Switching Time Waveform



## Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LPAK	SC-100	PTZZ0005DA-A	LPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

## Ordering Information

Part No.	Quantity	Shipping Container
RJK0853DPB-00-J5	2500 pcs	Taping

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