

# **MOSFET** - Power, Single N-Channel, STD Gate, SO8FL

40 V, 0.6 m $\Omega$ , 384 A

# **NVMFWS0D63N04XM**

MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	40	V
Gate-to-Source Voltage	DC	V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>C</sub> = 25°C	I <sub>D</sub>	384	Α
	T <sub>C</sub> = 100°C		271	
Power Dissipation	T <sub>C</sub> = 25°C	$P_{D}$	157	W
Continuous Drain Current	T <sub>C</sub> = 25°C	I <sub>D</sub>	60	Α
$R_{ heta JA}$	T <sub>C</sub> = 100°C		42	
Pulsed Drain Current	$T_{C} = 25^{\circ}C,$ $t_{p} = 10 \ \mu s$	I <sub>DM</sub>	900	Α
Operating Junction and Store Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 175	°C	
Source Current (Body Diode)		I <sub>S</sub>	131	Α
Single Pulse Avalanche Energy	I <sub>PK</sub> = 26.5 A	E <sub>AS</sub>	585	mJ
Lead Temperature for Solder (1/8" from case for 10 s)	TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

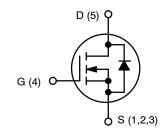
#### THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.95	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	39	

- 1. Surface mounted on FR4 board using 650 mm², 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX	
40 V	$0.6~\text{m}\Omega$ @ $V_{GS}$ = $10~\text{V}$	384 A	

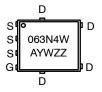
#### **N-CHANNEL MOSFET**





DFNW5 (SO-8FL) CASE 507BA

#### **MARKING DIAGRAM**



063N4W= Specific Device Code A = Assembly Location

Y = Year

W = Work Week
ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		•	•	•	•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	40			٧
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/ \Delta T_J$	I <sub>D</sub> = 1 mA, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 25°C			10	μΑ
		V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125°C			100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}, T_J = 25^{\circ}\text{C}$		0.54	0.6	mΩ
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 230 \mu A, T_J = 25^{\circ}C$	2.5		3.5	٧
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/$ $\Delta T_J$	$V_{GS} = V_{DS}, I_D = 230 \mu A$		-7.24		mV/°C
Forward Trans-conductance	9FS	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 30 A		174		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE					
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		5862		pF
Output Capacitance	C <sub>OSS</sub>			3760		1
Reverse Transfer Capacitance	C <sub>RSS</sub>			50		
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{DD} = 32 \text{ V}, I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$		92.2		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			17.2		
Gate-to-Source Charge	Q <sub>GS</sub>			25.8		
Gate-to-Drain Charge	$Q_{GD}$			17.4		
Gate Resistance	R <sub>G</sub>	f = 1 MHz		0.60		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t <sub>d(ON)</sub>	Resistive Load,		28		ns
Rise Time	t <sub>r</sub>	$V_{GS} = 0/10 \text{ V}, V_{DD} = 32 \text{ V},$ $I_{D} = 50 \text{ A}, R_{G} = 0 \Omega$		9		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			47		
Fall Time	t <sub>f</sub>			7.3		
SOURCE TO DRAIN DIODE CHARACTE	RISTICS					
Forward Diode Voltage	V <sub>SD</sub>	$I_S = 30 \text{ A}, V_{GS} = 0 \text{ V}, T_J = 25^{\circ}\text{C}$		0.78		V
		I <sub>S</sub> = 30 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C		0.63		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } I_{S} = 50 \text{ A,}$		83		ns
Charge Time	ta	dI/dt = 100 A/μs, V <sub>DD</sub> = 32 V		47		
Discharge Time	t <sub>b</sub>			36		
Reverse Recovery Charge	$Q_{RR}$			246		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **TYPICAL CHARACTERISTICS**

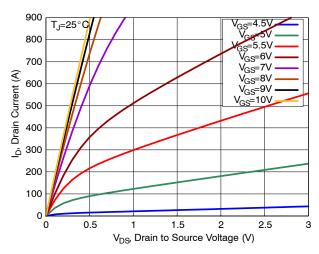


Figure 1. On-Region Characteristics

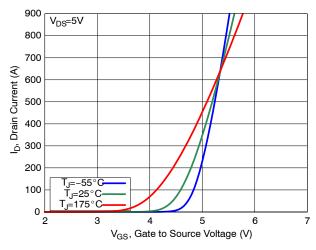


Figure 2. Transfer Characteristics

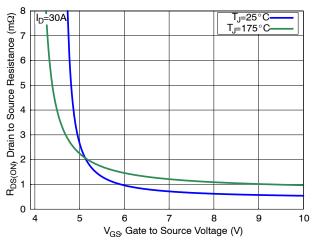


Figure 3. On-Resistance vs. Gate Voltage

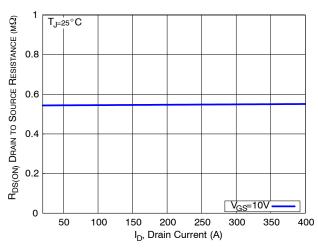


Figure 4. On-Resistance vs. Drain Current

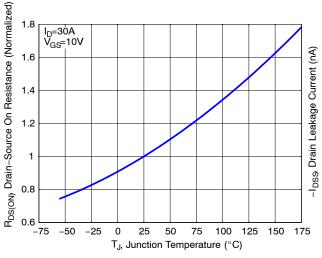


Figure 5. Normalized On-Resistance vs. Junction Temperature

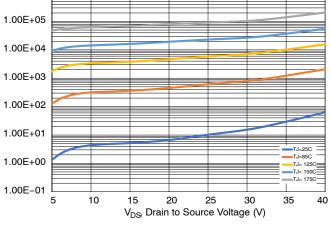


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

1.00E+06

# TYPICAL CHARACTERISTICS (continued)

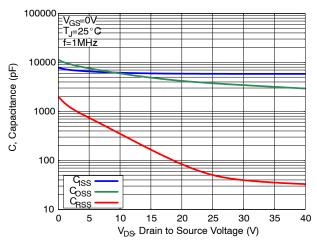


Figure 7. Capacitance Characteristics

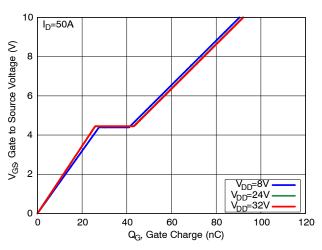


Figure 8. Gate Charge Characteristics

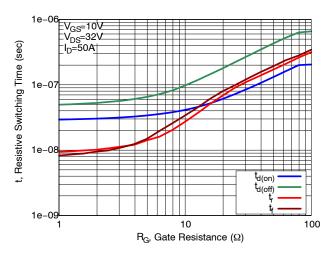


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

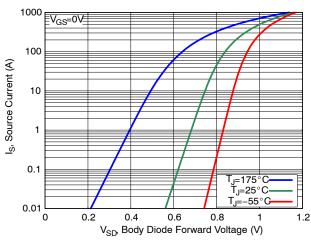


Figure 10. Diode Forward Voltage vs. Current

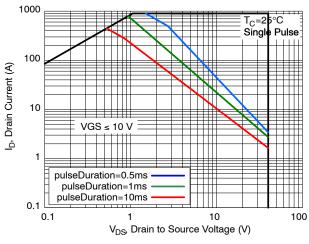


Figure 11. Safe Operating Area (SOA)

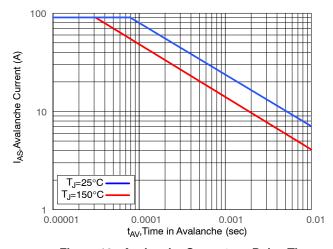


Figure 12. Avalanche Current vs. Pulse Time (UIS)

# TYPICAL CHARACTERISTICS (continued)

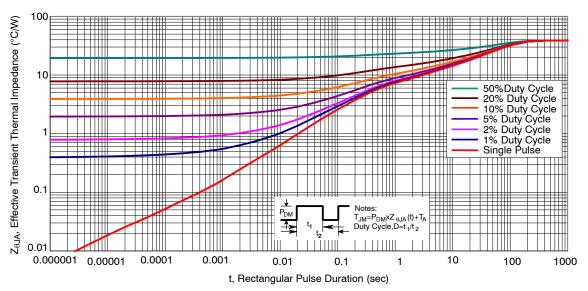


Figure 13. Thermal Characteristics

#### **ORDERING INFORMATION**

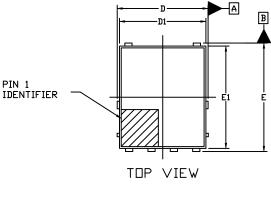
Device	Marking	Package	Shipping <sup>†</sup>
NVMFWS0D63N04XMT1G	063N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

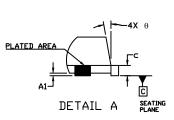
# DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA **ISSUE A** 

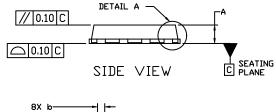




- TES:
  DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  CONTROLLING DIMENSION: MILLIMETERS
  DIMENSIONS DI AND EI DO NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR GATE BURRS.
  THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN
  FEATURES TO AID IN FILLET FORMATION ON THE LEADS
  DURING MOUNTING.



	MILLIMETERS		
DTM			
DIM	MIN.	N□M.	MAX.
Α	0.90	1.00	1.10
A1	0.00		0.05
b	0.33	0.41	0.51
С	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
е	1.27 BSC		
G	0.51	0.575	0.71
К	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
М	3.00	3.40	3.80



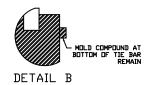
e e/2

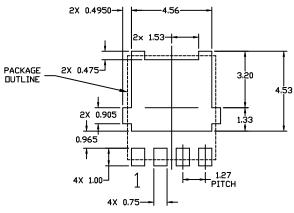
BOTTOM VIEW

-DETAIL B

⊕ 0.10 C A B 0.05 C

PIN 5 (EXPOSED PAD)





θ

0\*

12\*

# RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

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