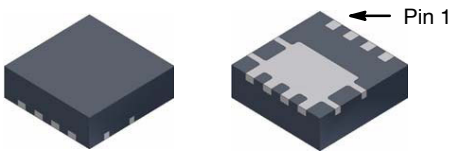
# MOSFET – N-Channel, POWERTRENCH®, SyncFET™

## 25 V, 40 A, 2 mΩ

# FDMC7570S




**Power 33**
**PQFN8**
**CASE 483AK**

### General Description

The FDMC7570S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

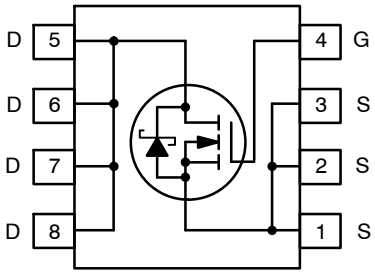
### Features

- Max $R_{DS(on)}$ = 2 mΩ at $V_{GS}$ = 10 V, $I_D$ = 27 A
- Max $R_{DS(on)}$ = 2.9 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 21.5 A
- Advanced Package and Combination for Low $R_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

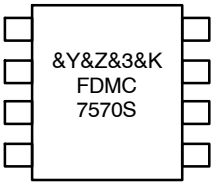
### Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

### PIN ASSIGNMENT




### MARKING DIAGRAM




| | |
|---|---|
| &Y | = **onsemi** Logo |
| &Z | = Assembly Plant Code |
| &3 | = 3−Digit Data Code |
| &K | = 2−Digit Lot Traceability Code |
| FDMC7570S | = Specific Device Code |

### MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Drain to Source Voltage | $V_{DS}$ | 25 | V |
| Gate to Source Voltage (Note 4) | $V_{GS}$ | ±20 | V |
| Drain Current<br>– Continuous (Package limited) $T_C$ = 25°C<br>– Continuous (Silicon limited) $T_C$ = 25°C<br>– Continuous $T_A$ = 25°C (Note 1a)<br>– Pulsed | $I_D$ | <br>40<br>132<br>27<br>120 | A |
| Single Pulse Avalanche Energy (Note 3) | $E_{AS}$ | 144 | mJ |
| Power Dissipation $T_C$ = 25°C | $P_D$ | 59 | W |
| Power Dissipation $T_A$ = 25°C (Note 1a) | | 2.3 | |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{STG}$ | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMC7570S | PQFN8<br>(Pb−Free) | 3,000 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 2.1 | °C/W |
| Thermal Resistance, Junction to Ambient (Note 1a) | $R_{\theta JA}$ | 53 | |

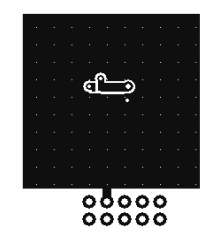
## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTIC** | | | | | | |
| Drain to Source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | $BV_{DSS}$ | 25 | | | V |
| Breakdown Voltage Temperature Coefficient | $I_D$ = 10 mA, referenced to 25°C | $\Delta BV_{DSS}$ / $\Delta T_J$ | | 21 | | mV/°C |
| Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | $I_{DSS}$ | | | 500 | μA |
| Gate to Source Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | $I_{GSS}$ | | | 100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA | $V_{GS(th)}$ | 1.2 | 1.7 | 3 | V |
| Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 10 mA, referenced to 25°C | $\Delta V_{GS(th)}$ / $\Delta T_J$ | | −4 | | mV/°C |
| Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 27 A | $R_{DS(on)}$ | | 1.6 | 2 | mΩ |
| | $V_{GS}$ = 4.5 V, $I_D$ = 21.5 A | | | 2.4 | 2.9 | |
| | $V_{GS}$ = 10 V, $I_D$ = 27 A, $T_J$ = 125°C | | | 2.2 | 2.8 | |
| Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 27 A | $g_{FS}$ | | 154 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | $V_{DS}$ = 13 V, $V_{GS}$ = 0 V, f = 1 MHz | $C_{iss}$ | | 3315 | 4410 | pF |
| Output Capacitance | | $C_{oss}$ | | 1010 | 1345 | pF |
| Reverse Transfer Capacitance | | $C_{rss}$ | | 168 | 255 | pF |
| Gate Resistance | | $R_g$ | | 1.2 | 2.1 | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn−On Delay Time | $V_{DD}$ = 13 V, $I_D$ = 27 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | $t_{d(on)}$ | | 14 | 26 | ns |
| Rise Time | | $t_r$ | | 6.8 | 14 | ns |
| Turn−Off Delay Time | | $t_{d(off)}$ | | 34 | 55 | ns |
| Fall Time | | $t_f$ | | 4.5 | 10 | ns |
| Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 13 V | $Q_{g(TOT)}$ | | 49 | 68 | nC |
| Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V, $V_{DD}$ = 13 V | $Q_{g(TOT)}$ | | 22 | 31 | nC |
| Gate to Source Gate Charge | $I_D$ = 27 A | $Q_{gs}$ | | 10.8 | | nC |
| Gate to Drain “Miller” Charge | | $Q_{gd}$ | | 5.5 | | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 27 A (Note 2) | $V_{SD}$ | | 0.78 | 1.2 | V |
| | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 2) | | | 0.43 | 0.8 | |
| Reverse Recovery Time | $I_F$ = 27 A, di/dt = 300 A/μs | $t_{rr}$ | | 30 | 48 | ns |
| Reverse Recovery Charge | | $Q_{rr}$ | | 29 | 46 | nC |

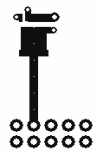
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. $E_{AS}$ of 144 mJ is based on starting $T_J$ = 25°C, L = 1 mH, $I_{AS}$ = 17 A, $V_{DD}$ = 23 V, $V_{GS}$ = 10 V. 100% test at L = 0.3 mH, $I_{AS}$ = 25 A.
4. As an N−ch device, the negative Vgs rating is for lower duty cycle pulse occurrence only. No continuous rating is implied.

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

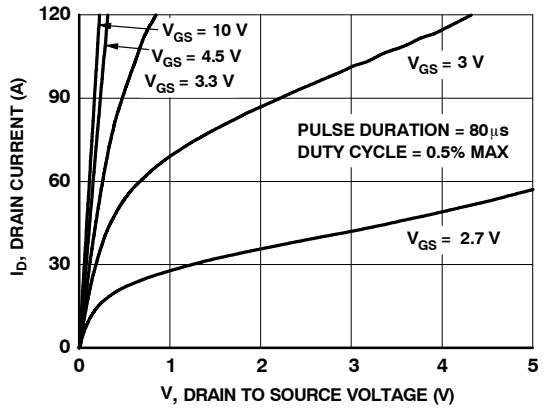



**Figure 1. On−Region Characteristics**

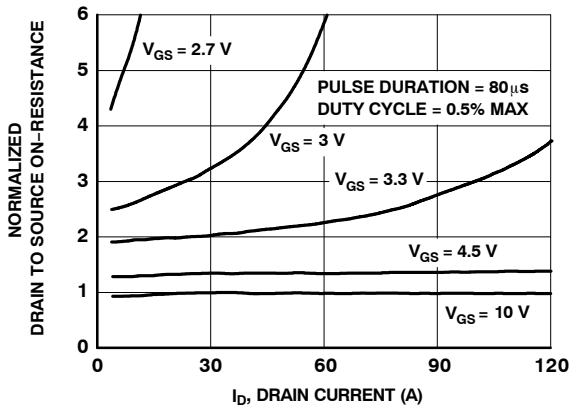



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

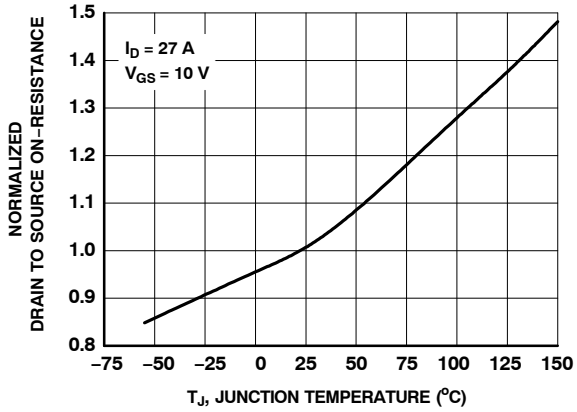



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

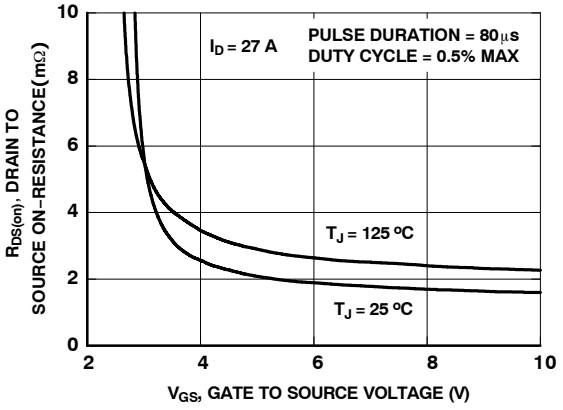



**Figure 4. On−Resistance vs. Gate to Source Voltage**

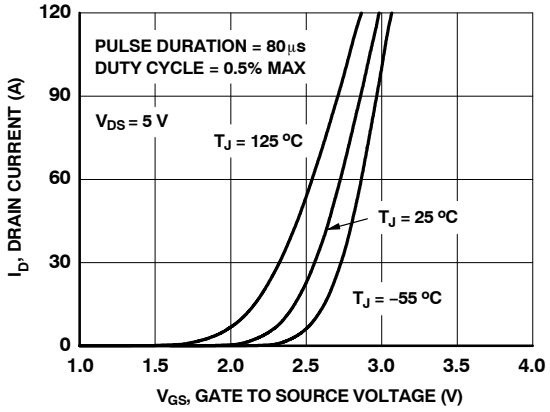



**Figure 5. Transfer Characteristics**

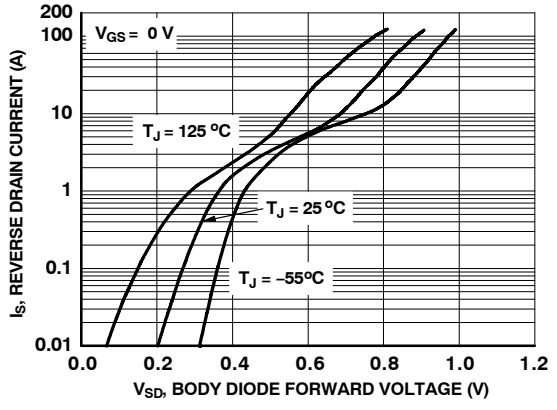



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

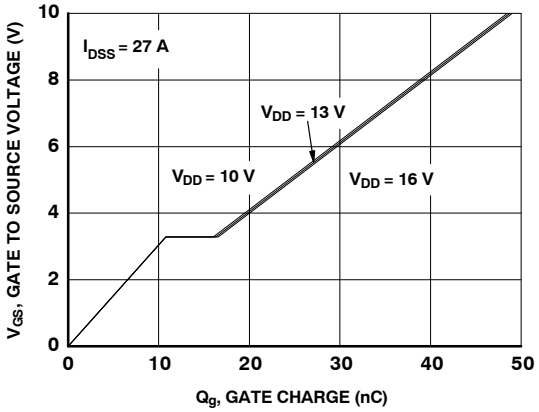



**Figure 7. Gate Charge Characteristics**

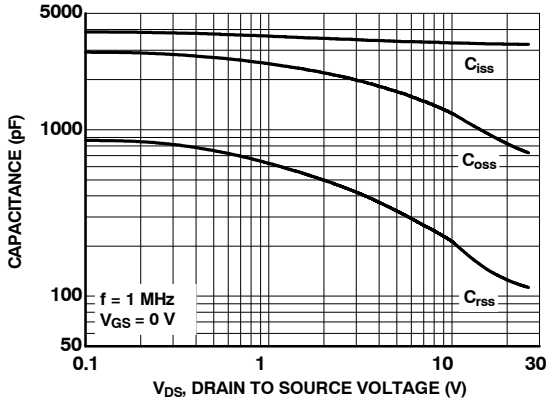



**Figure 8. Capacitance vs Drain to Source Voltage**

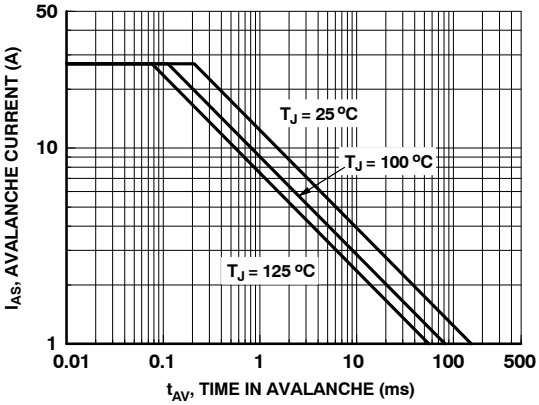



**Figure 9. Unclamped Inductive Switching Capability**

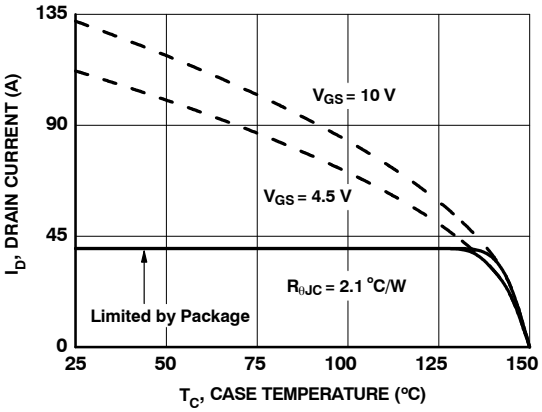



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

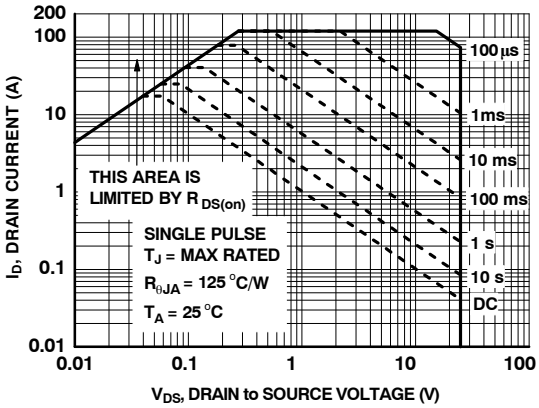



**Figure 11. Forward Bias Safe Operating Area**

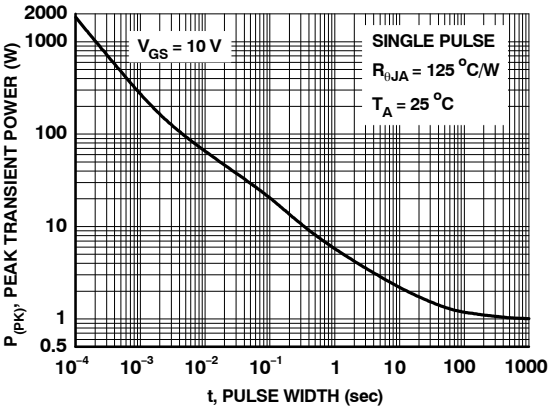



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

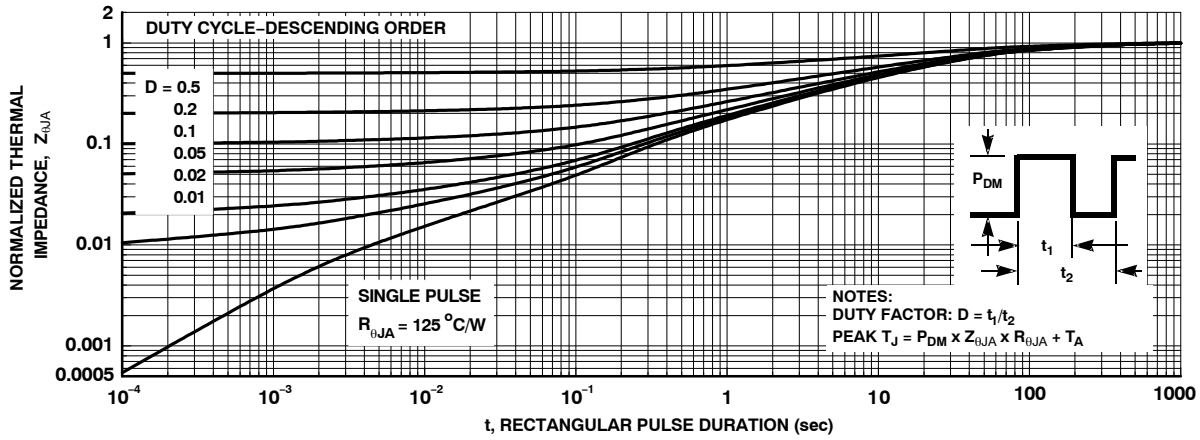



**Figure 13. Junction−to−Ambient Transient Thermal Response Curve**

## SyncFET SCHOTTKY BODY DIODE CHARACTERISTICS

**onsemi**'s SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverses recovery characteristic of the FDMC7570S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

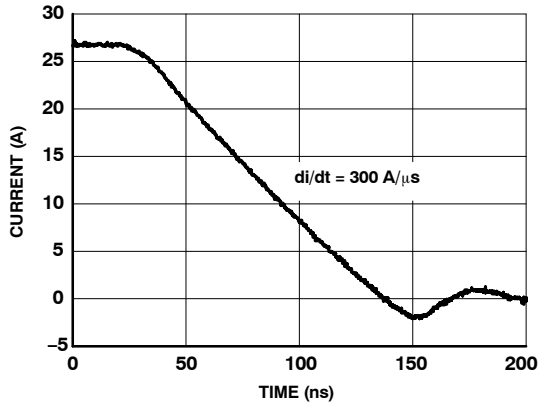



**Figure 14. FDMC7570S SyncFET Body Diode Reverse Recovery Characteristic**

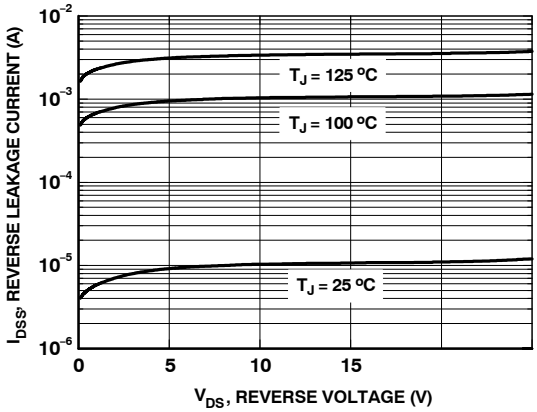
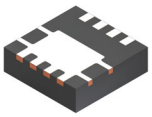
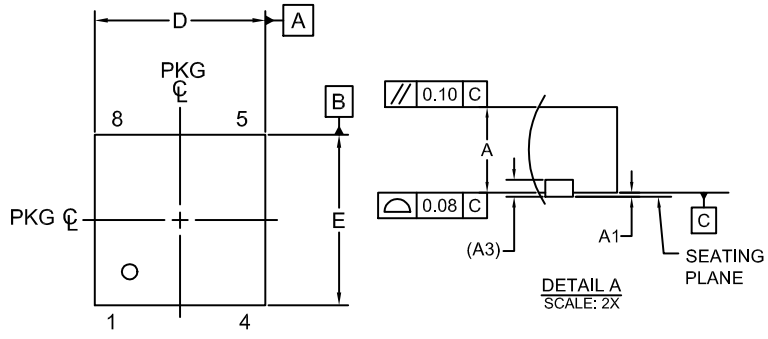



**Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage**

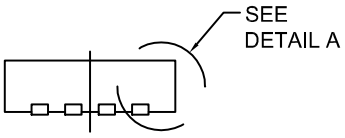


**PQFN8 3.3X3.3, 0.65P**
CASE 483AK
ISSUE B

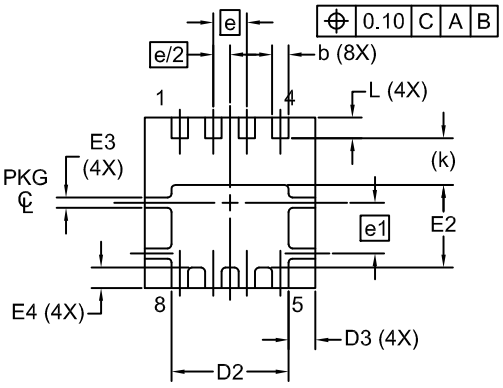
DATE 12 OCT 2021



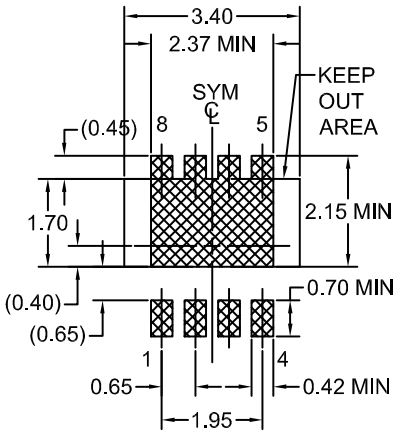

TOP VIEW




FRONT VIEW




BOTTOM VIEW




LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.27 | 0.32 | 0.37 |
| D | 3.20 | 3.30 | 3.40 |
| D2 | 2.17 | 2.27 | 2.37 |
| D3 | 0.42 | 0.52 | 0.62 |
| E | 3.20 | 3.30 | 3.40 |
| E2 | 1.50 | 1.60 | 1.70 |
| E3 | 0.10 | 0.20 | 0.30 |
| E4 | 0.29 | 0.39 | 0.49 |
| e | 0.65 BSC | | |
| e/2 | 0.325 BSC | | |
| e1 | 0.98 BSC | | |
| k | 0.91 REF | | |
| L | 0.30 | 0.40 | 0.50 |

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|---|---|---|---|
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**onsemi Website:** www.onsemi.com

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales