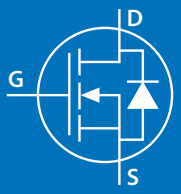
EPC2091 – Enhancement Mode Power Transistor

V_{DS} , 100 V

$R_{DS(on)}$, 1.5 mΩ typical, 2 mΩ max

I_D , 350 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised September 3, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate
- Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

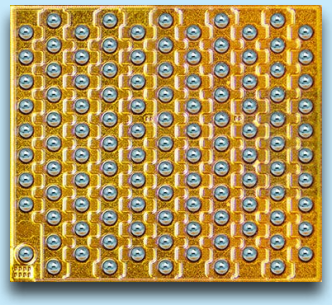
Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous ($T_J \leq 125$°C)	126	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	350	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.08	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.135 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.013	0.135	mA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 90 °C		0.06	0.5	
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	3	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.85	4	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.08	1.4	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 12 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 45 A		1.5	2	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.5		V

Defined by design. Not subject to production test.



Die size: 3.23 x 2.88 mm

EPC2091 eGaN® FETs are supplied in passivated die form with copper pillars.

Applications

- Copper pillars for package integration
- DC-DC converters
- Isolated DC-DC converters
- Lidar
- Sync rectification for AC-DC and DC-DC
- Point-of-Load converters
- USB-C
- Class-D audio
- LED lighting
- eMobility

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V , V_{GS} = 0 V		2893	4167	pF
C_{RSS}	Reverse Transfer Capacitance			8.8		
C_{OSS}	Output Capacitance			1035	1423	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		1223		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			1547		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 45 A		20	29	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 50 V, I_D = 45 A		6.7		
Q_{GD}	Gate to Drain Charge			2		
$Q_{G(TH)}$	Gate Charge at Threshold			4.8		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		77	104	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Figure 1: Typical Output Characteristics at 25°C

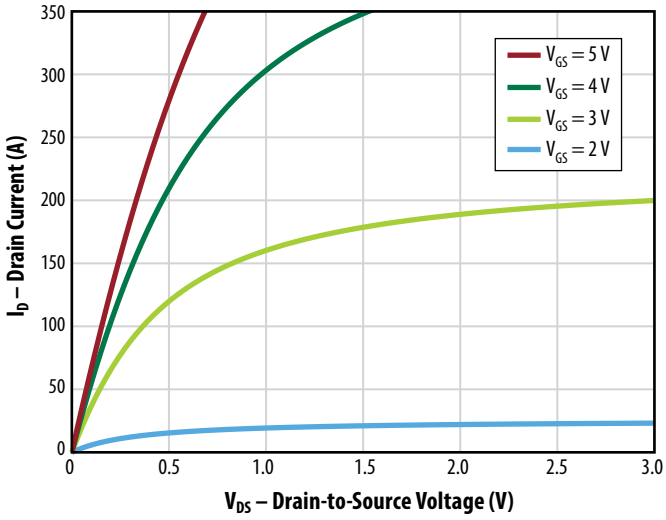


Figure 2: Typical Transfer Characteristics

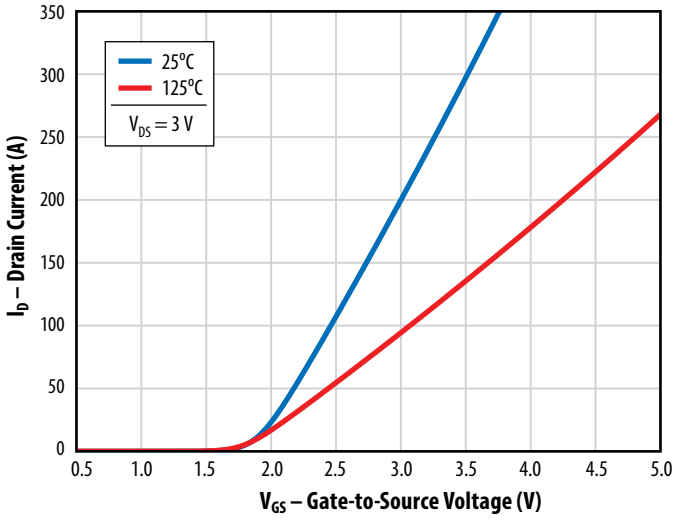


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Currents

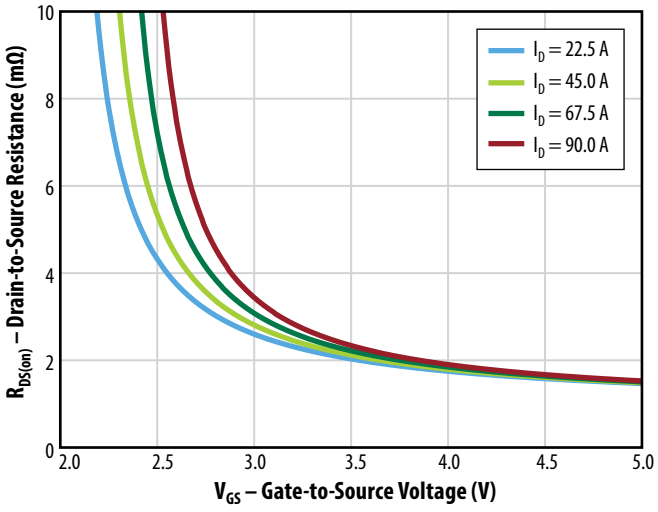


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

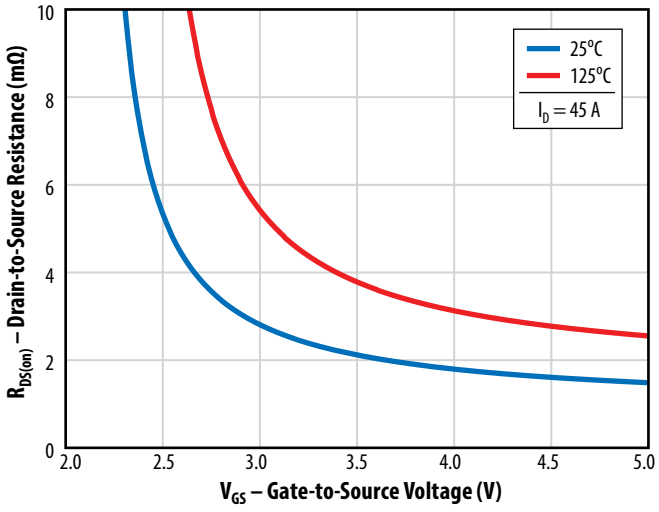


Figure 5a: Typical Capacitance (Linear Scale)

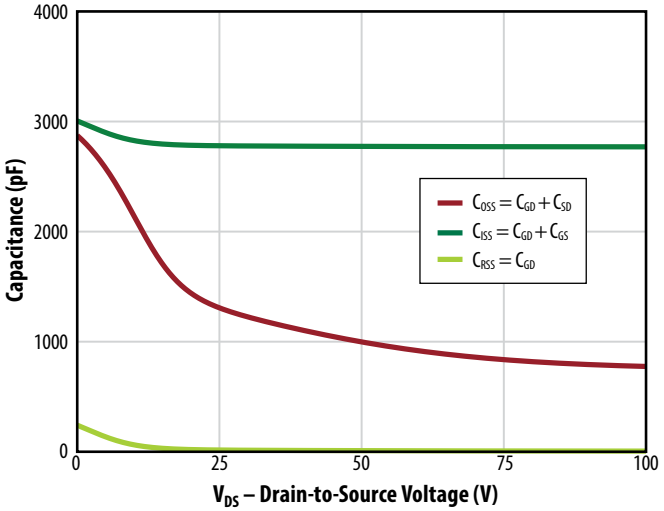


Figure 5b: Typical Capacitance (Log Scale)

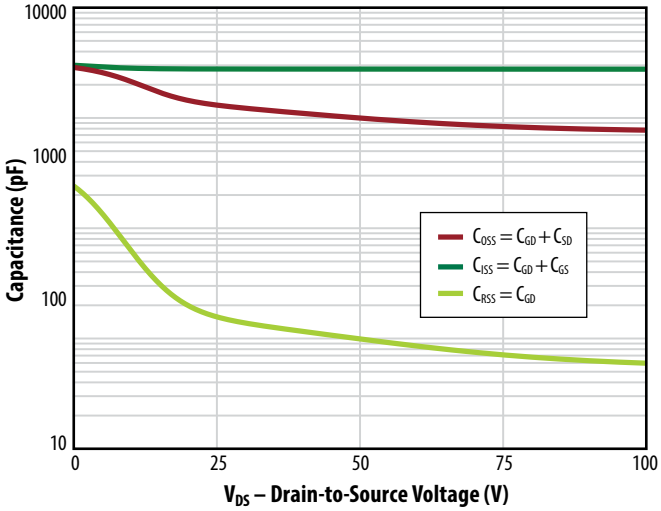


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

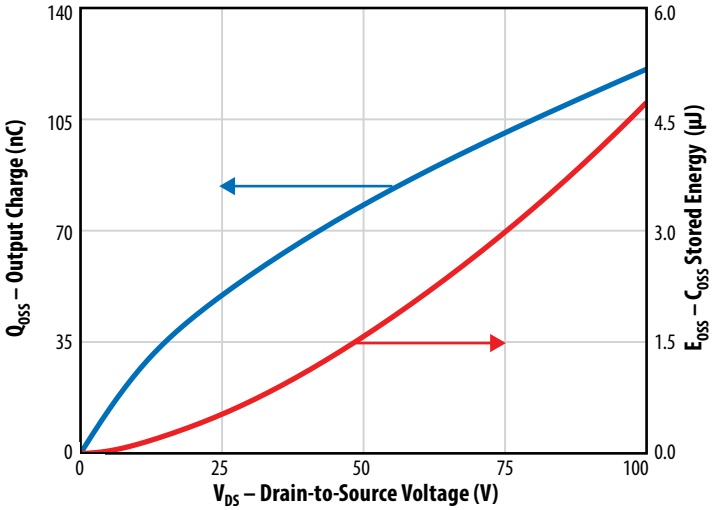


Figure 7: Typical Gate Charge

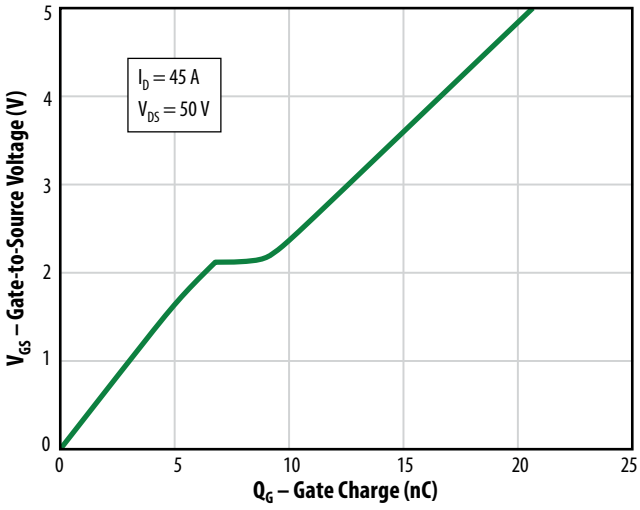


Figure 8: Typical Reverse Drain-Source Characteristics

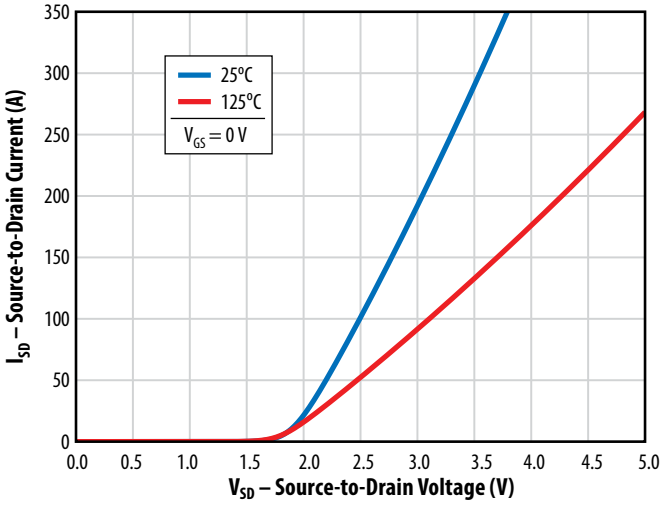
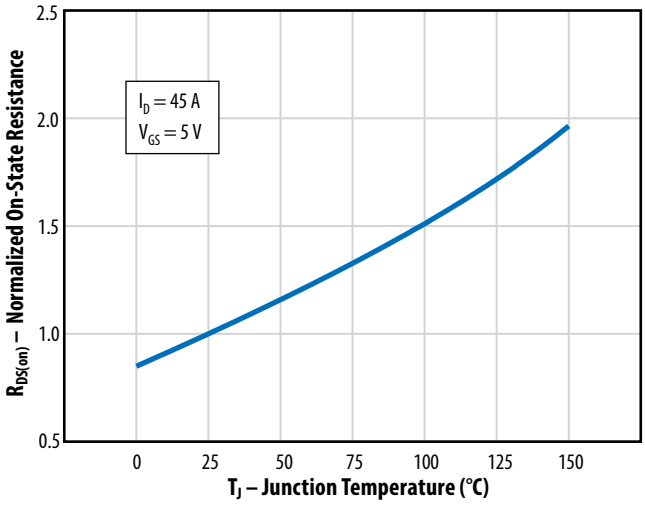


Figure 9: Typical Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temperature

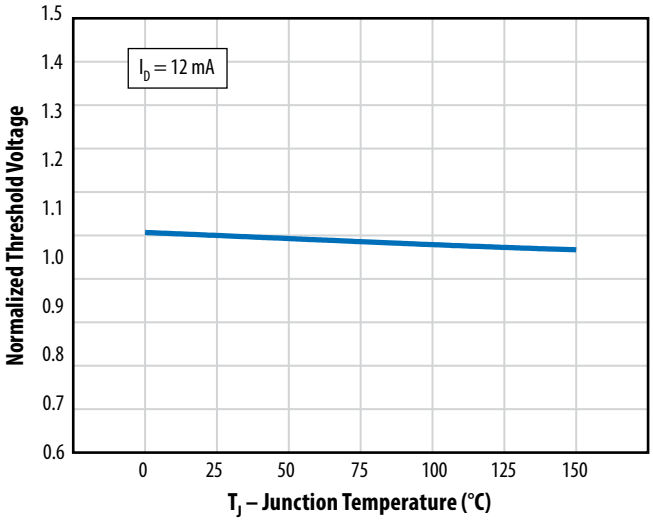
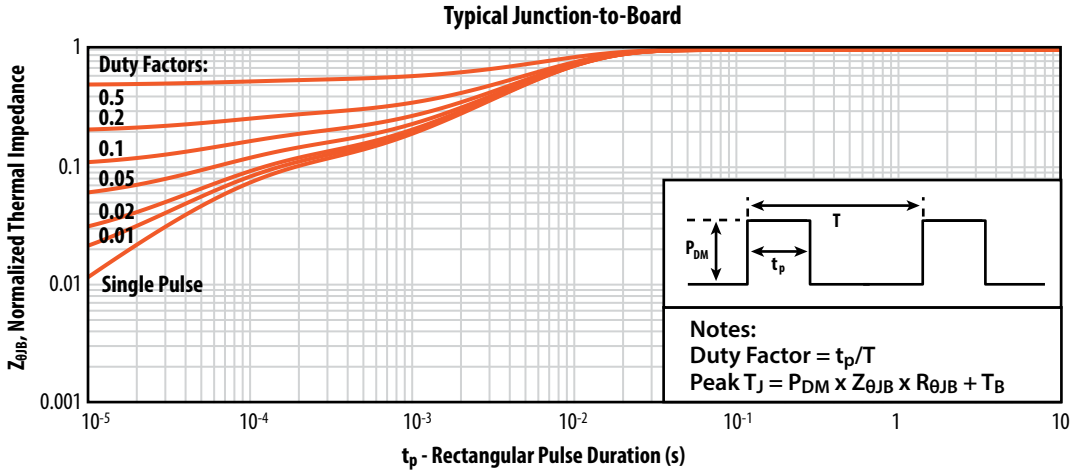


Figure 11: Typical Transient Thermal Response Curves



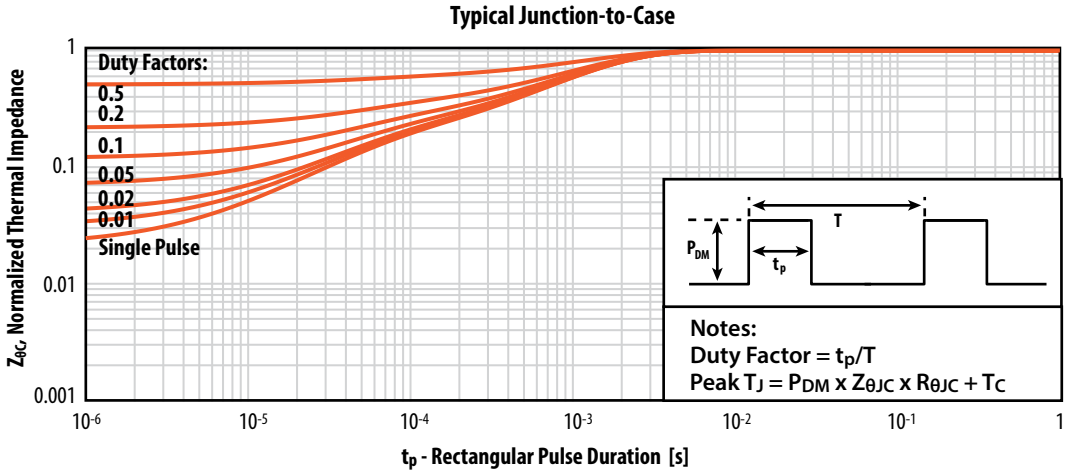
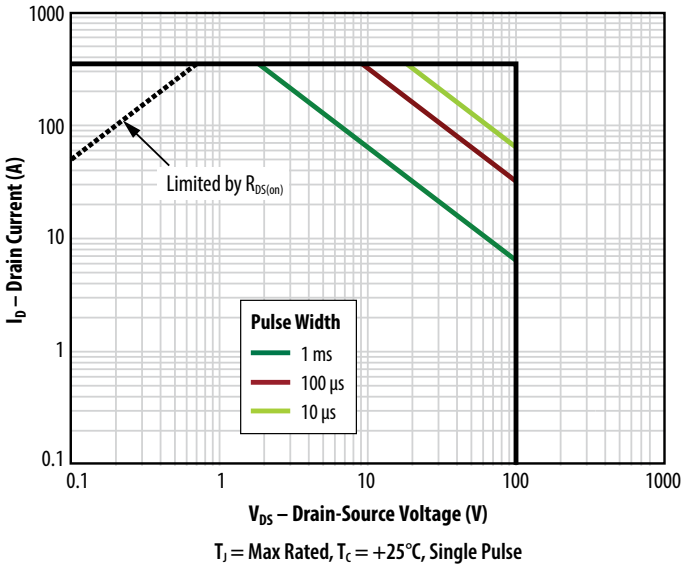


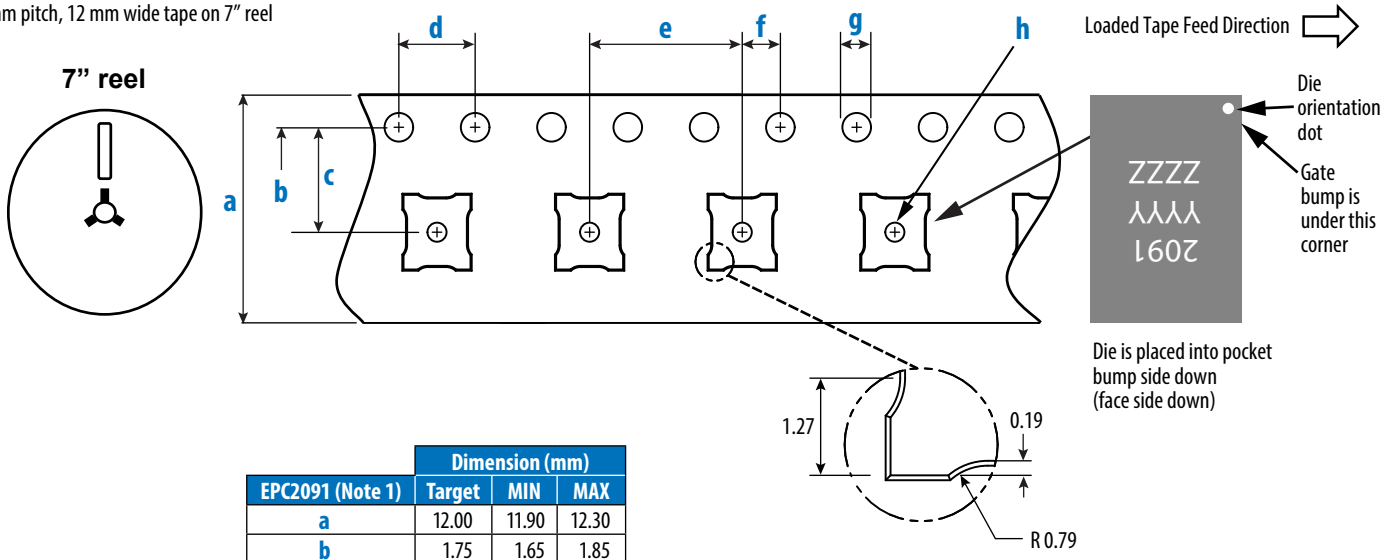
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

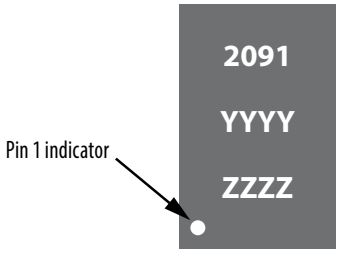


EPC2091 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

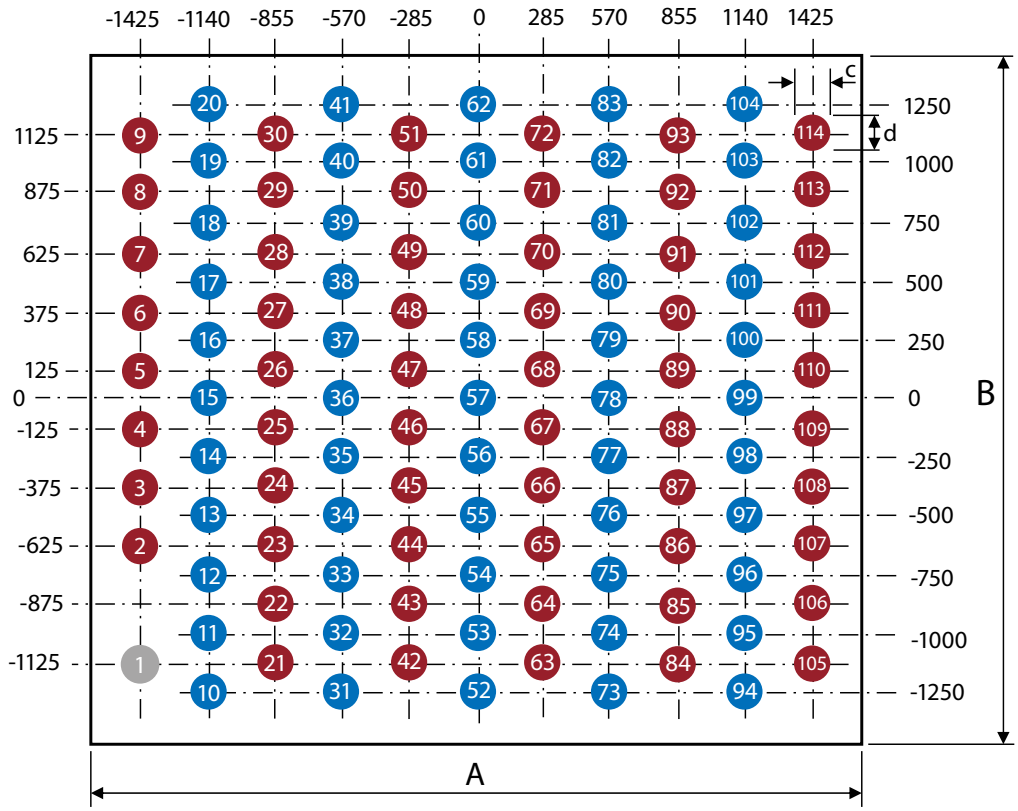
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2091	2091	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



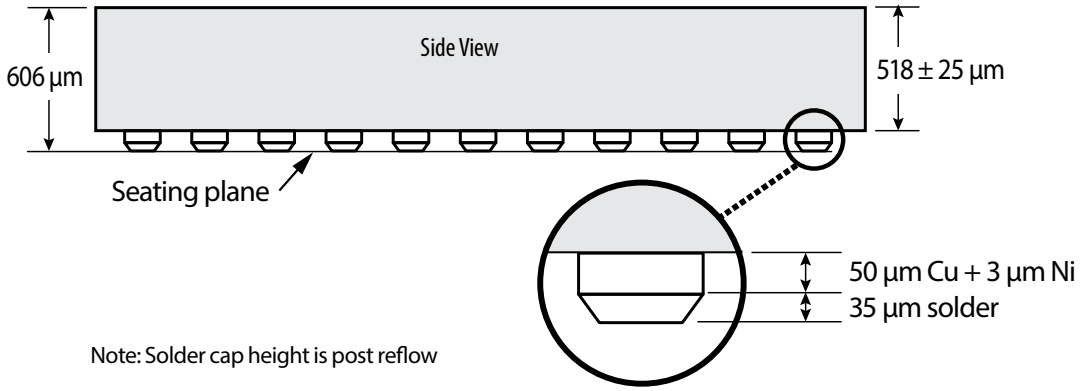
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3200	3230	3260
B	2850	2880	2910
c		150	
d		150	

Pad 1 is Gate;

Pads 2-9, 21-30, 42-51, 63-72, 84-93, 105-114 are Source;

Pads 10-20, 31-41, 52-62, 73-83, 94-104 are Drain.

Note: All pads are 150 x 150 µm



Note: Solder cap height is post reflow

Note: Cu pillar dies are not intended for mounting on a PCB, they are intended for use in a package. Terms of die usage: The die represented by this data sheet are intended for initial evaluation for integration to buyer defined package. EPC does not guarantee reliability in the buyer specific package. To ensure reliability, the die may need redesign to be optimized to buyers specific package. NRE may apply

LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

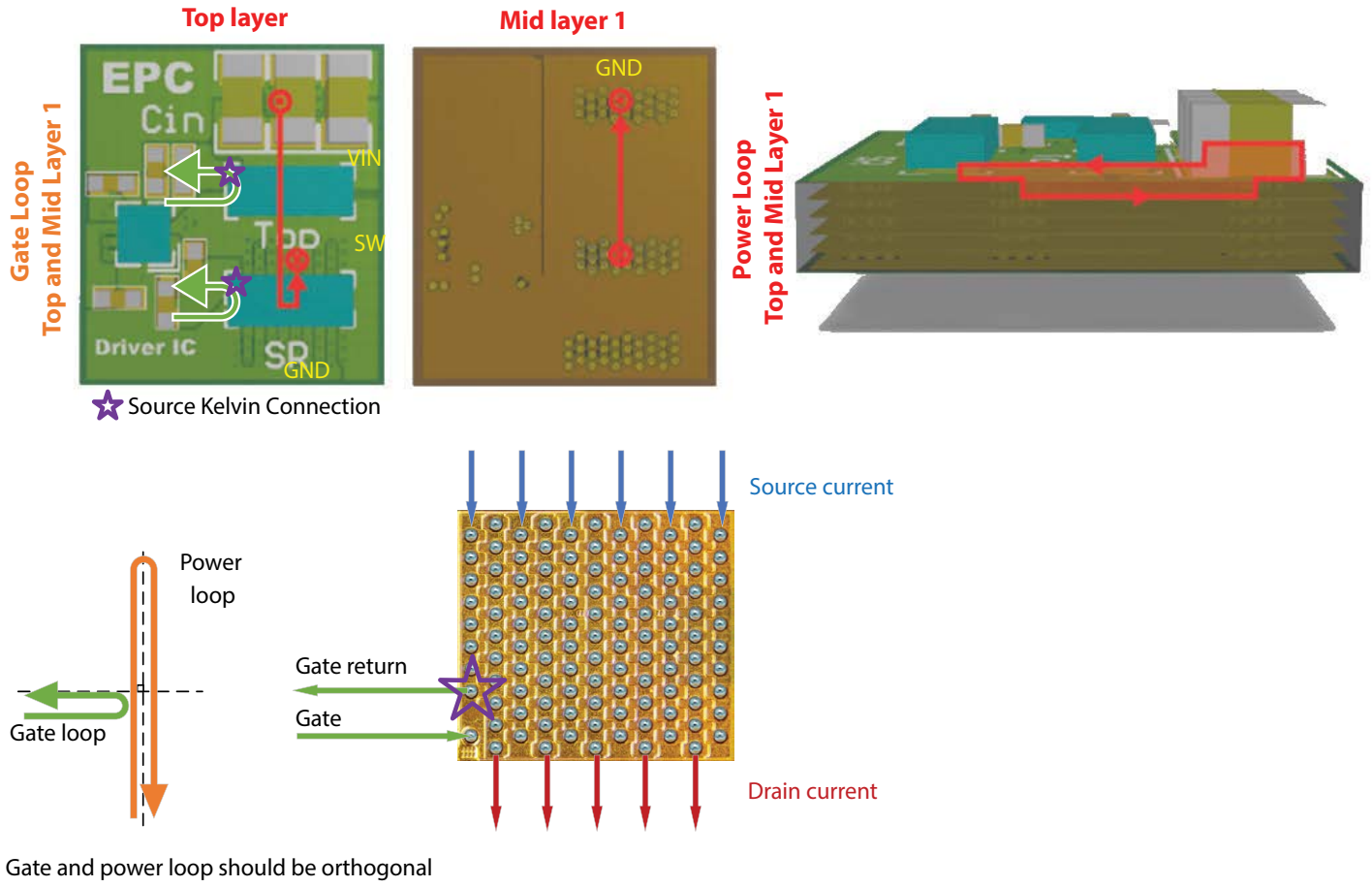


Figure 13: Inner vertical layout for power and gate loops

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**

TYPICAL THERMAL CONCEPT

The EPC2091 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

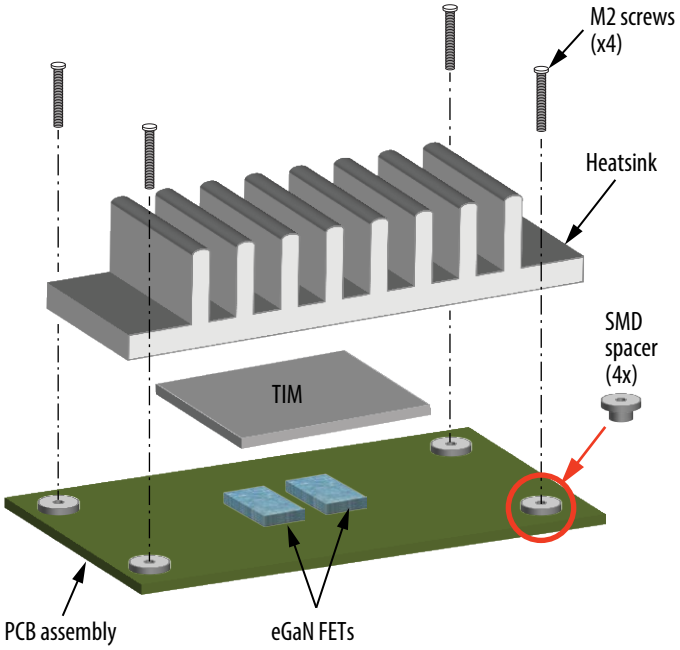


Figure 14: Exploded view of heatsink assembly using screws

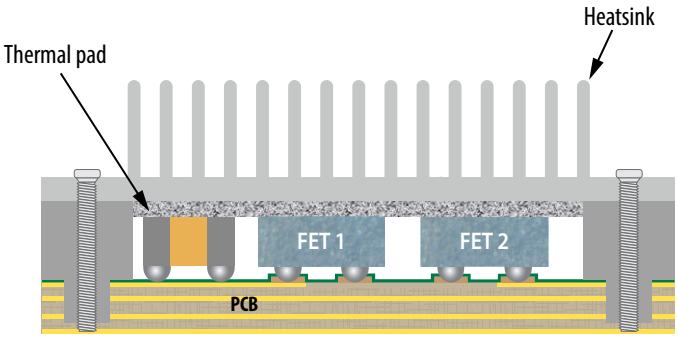


Figure 15: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)