MOSFET

OptiMOS™ 6 Power-Transistor, 100 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Optimized for high frequency switching and synchronous rectification
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
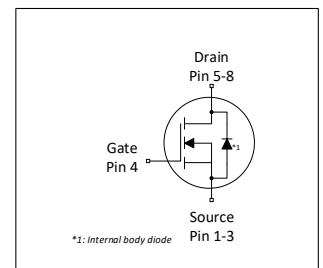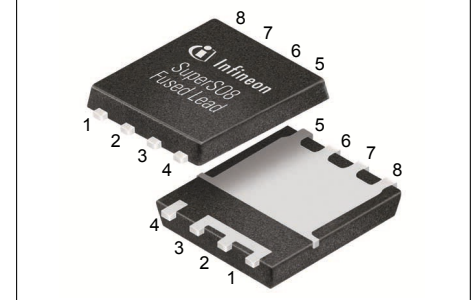- MSL 1 classified according to J-STD-020

Product validation

Fully qualified according to JEDEC for Industrial Applications

TDSON-8 FL (enlarged source interconnection)

Drain
Pin 5-8

Gate
Pin 4

Source
Pin 1-3

*1: Internal body diode

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	3.0	mΩ
I_D	179	A
Q_{oss}	101	nC
Q_G(0V...10V)	55	nC
Q_{rr} (100A/µs)	56	nC

Type / Ordering Code	Package	Marking	Related Links
ISC030N10NM6	PG-TDSON-8 FL	030N10N6	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	179 127 110 21	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=8 V, T_C=100 °C V_{GS}=10V, T_A=25°C, R_{thJA}=50°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	716	A	T_A=25 °C
Avalanche current, single pulse[4]	I_{AS}	-	-	50	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	988	mJ	I_D=18 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	208 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.36	0.72	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3   Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4   Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.3	2.8	3.3	V	V_{DS}=V_{GS}, I_D=109 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C[1]
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.6 3.1	3.0 4.0	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=8 V, I_D=25 A
Gate resistance	R_G	0.52	1.05	1.56	Ω	-
Transconductance	g_{fs}	41	82	-	S	$|V_{DS}|{\geq}2|I_D|R_{DS(on)max}$, I_D=50 A

Table 5   Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4000	5200	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	900	1100	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	15	22	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=25 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4.5	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=25 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	22.5	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=25 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	5.3	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=25 A, $R_{G,ext}$=1.6 Ω

Table 6   Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[1]	Q_{gs}	-	18	24	nC	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge at threshold[1]	$Q_{g(th)}$	-	11	14	nC	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	9.1	14	nC	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	16	-	nC	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	55	69	nC	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	50	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	101	126	nC	V_{DS}=50 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	179	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	716	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.82	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	46.5	70	ns	V_R=50 V, I_F=25 A, di_F/dt=100 A/μs
Reverse recovery charge[1]	Q_{rr}	-	56	84	nC	V_R=50 V, I_F=25 A, di_F/dt=100 A/μs
Reverse recovery time[1]	t_{rr}	-	25.5	38	ns	V_R=50 V, I_F=25 A, di_F/dt=1000 A/μs
Reverse recovery charge[1]	Q_{rr}	-	266	399	nC	V_R=50 V, I_F=25 A, di_F/dt=1000 A/μs

[1] Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot}=f(T_C)

Diagram 2: Drain current

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance

single pulse
0.01
0.02
0.05
0.1
0.2
0.5

Z_{thJC}=f(t_p); parameter: D=t_p/T

infineon
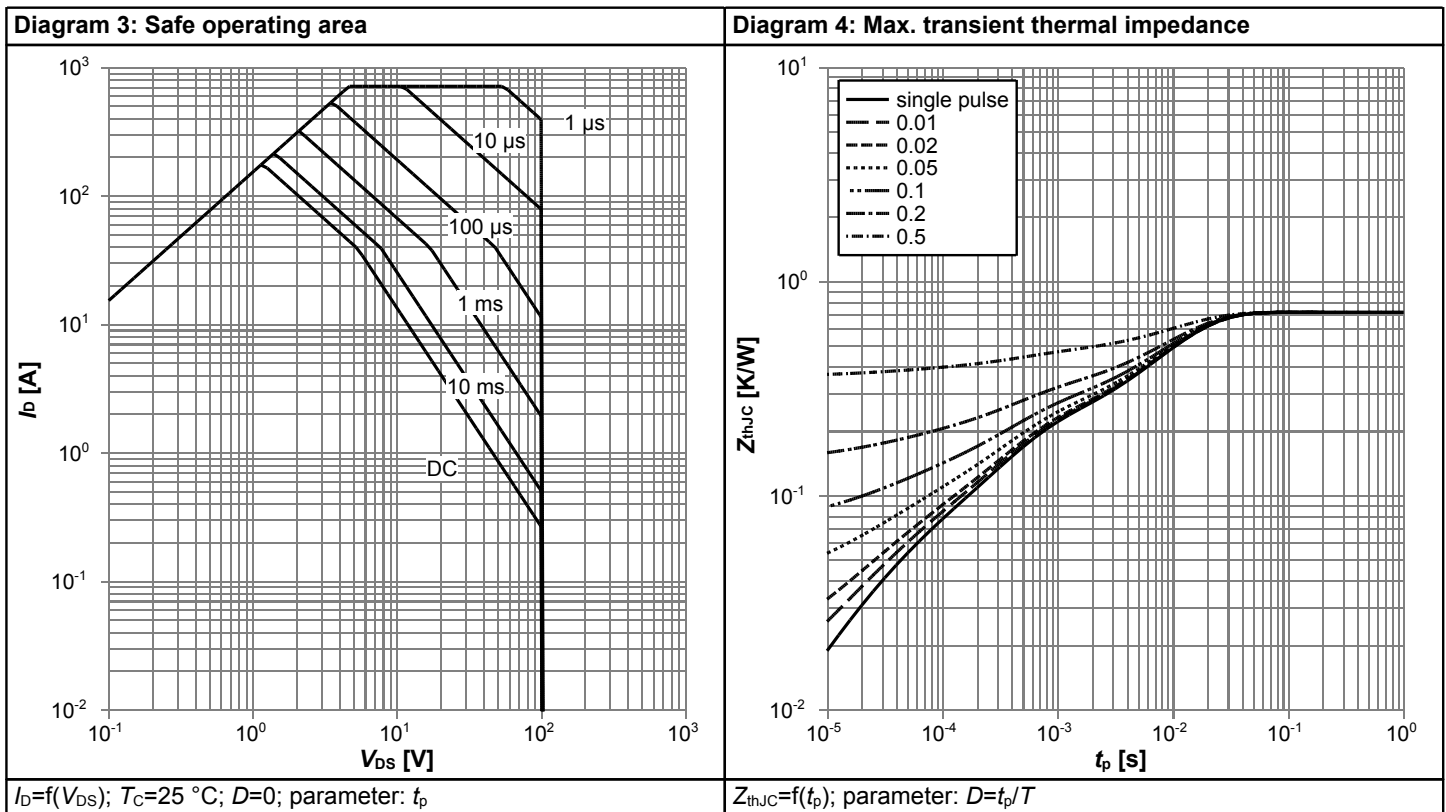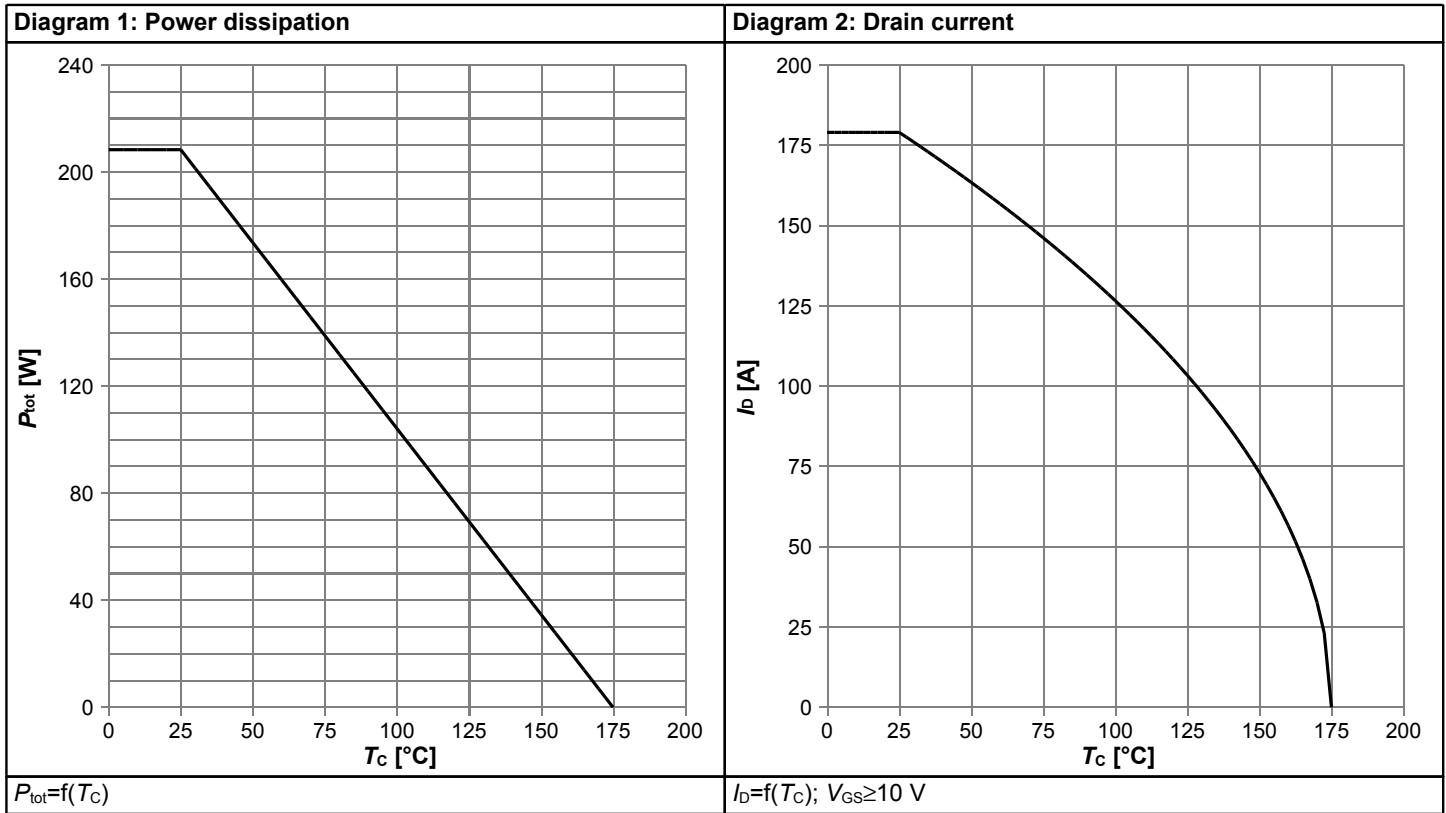
Diagram 5: Typ. output characteristics
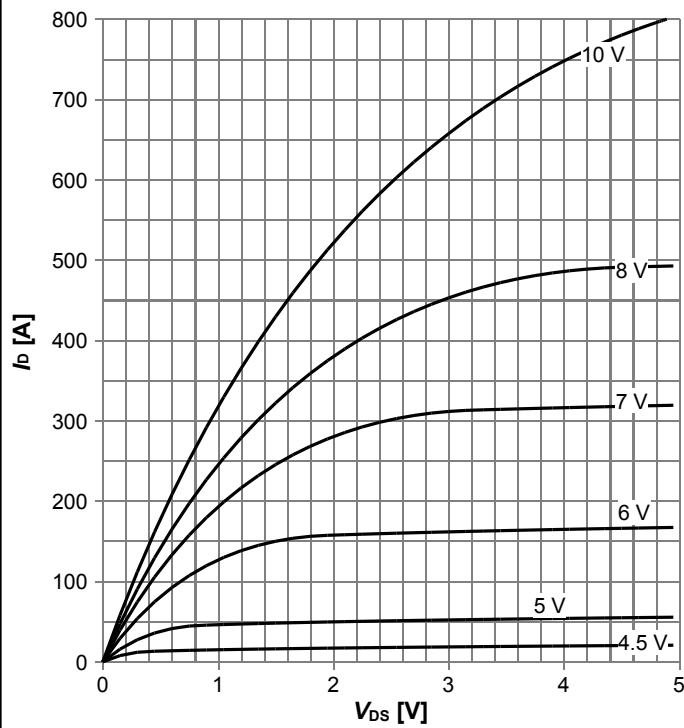
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
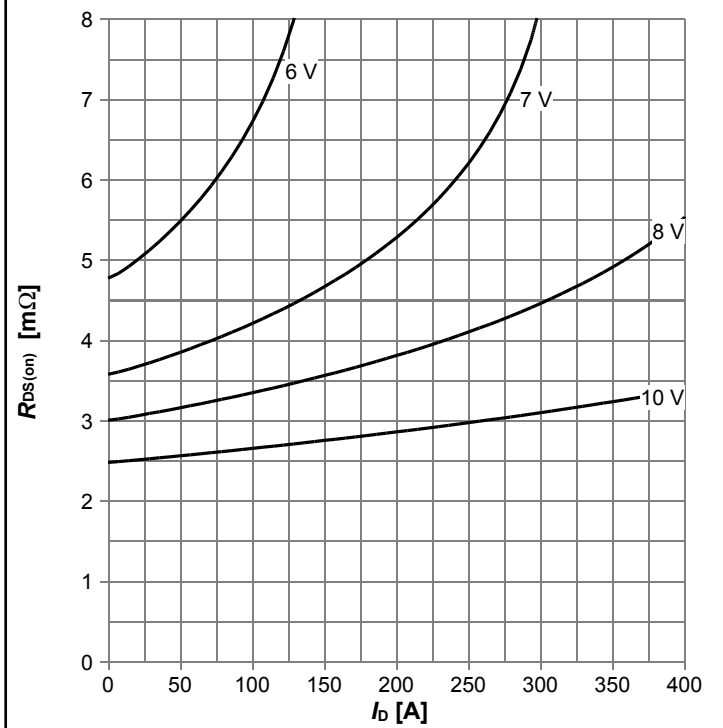
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
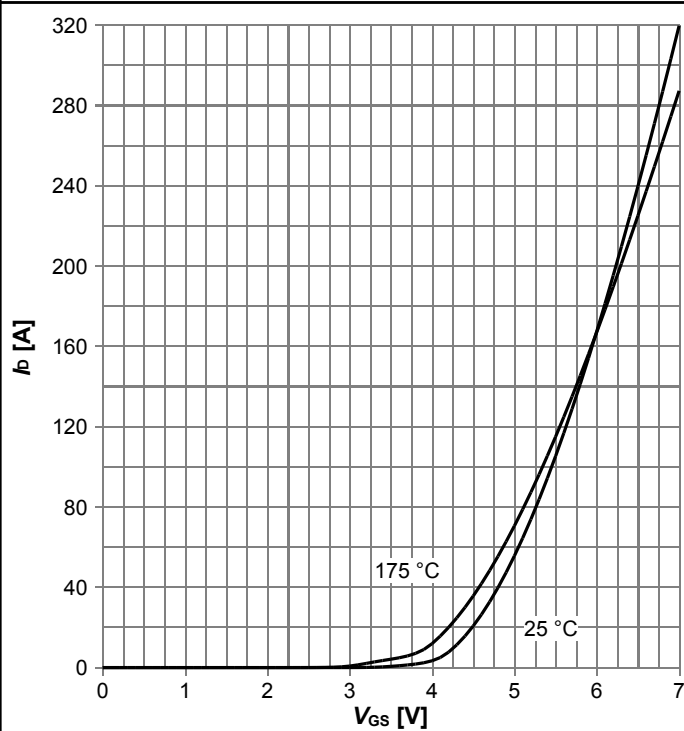
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance
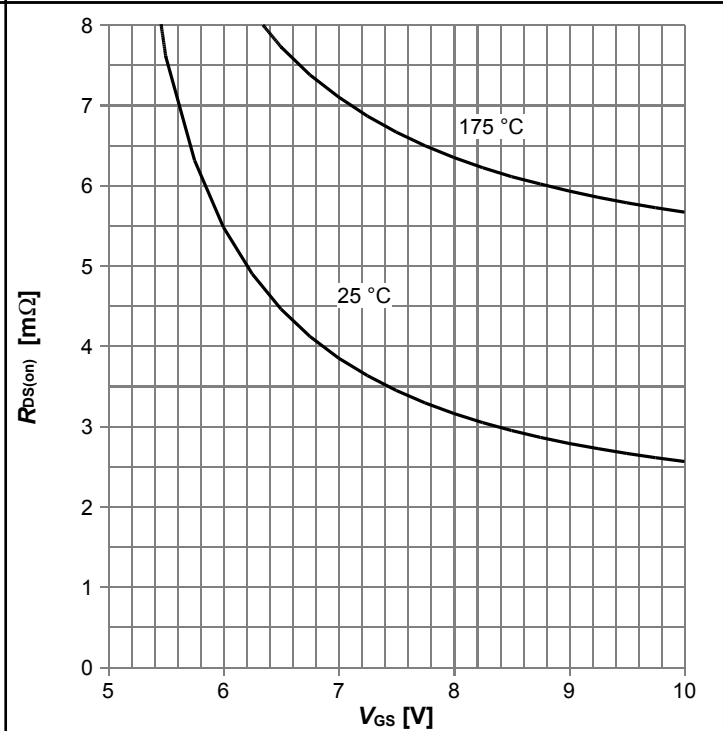
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance
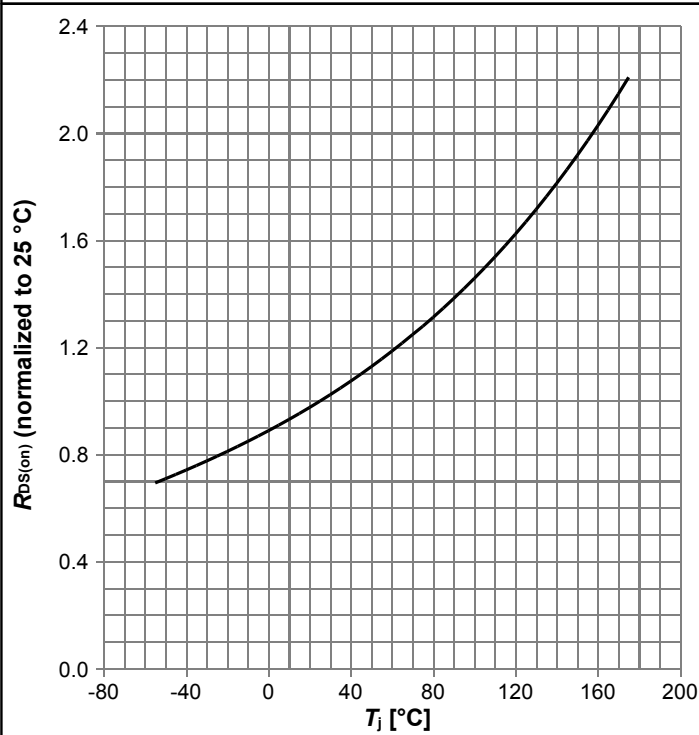
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage

1090 µA

109 µA
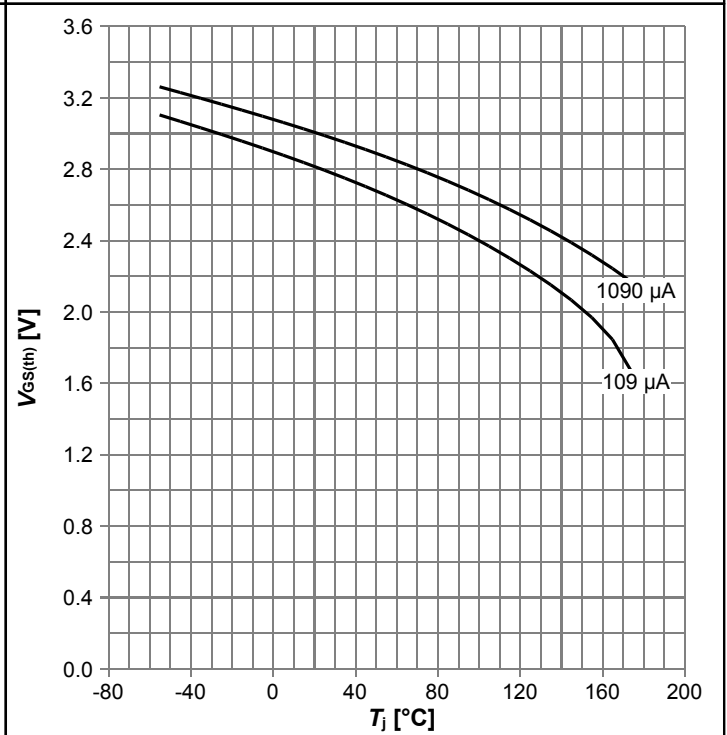
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances

Ciss

Coss

Crss
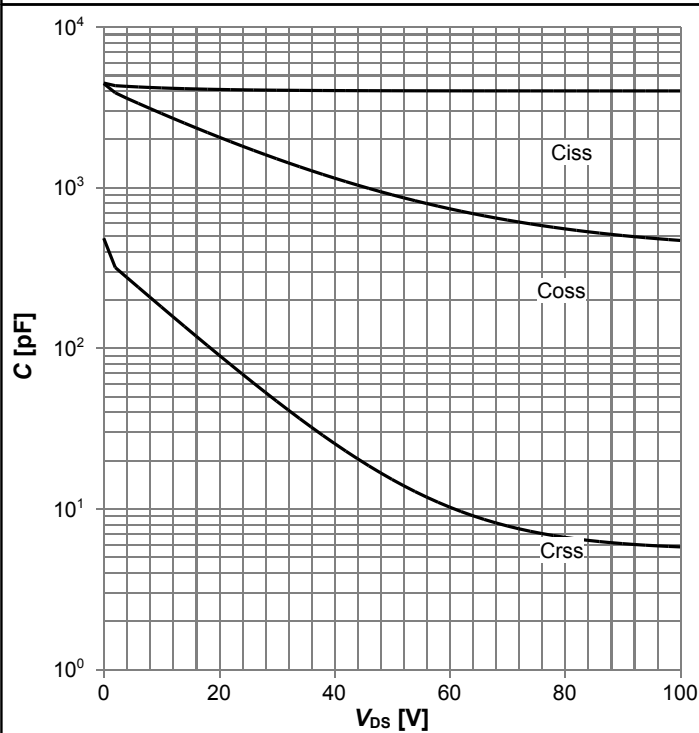
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode

- —— 25 °C
- – – 25 °C, max
- – – – 175 °C
- ···· 175 °C, max
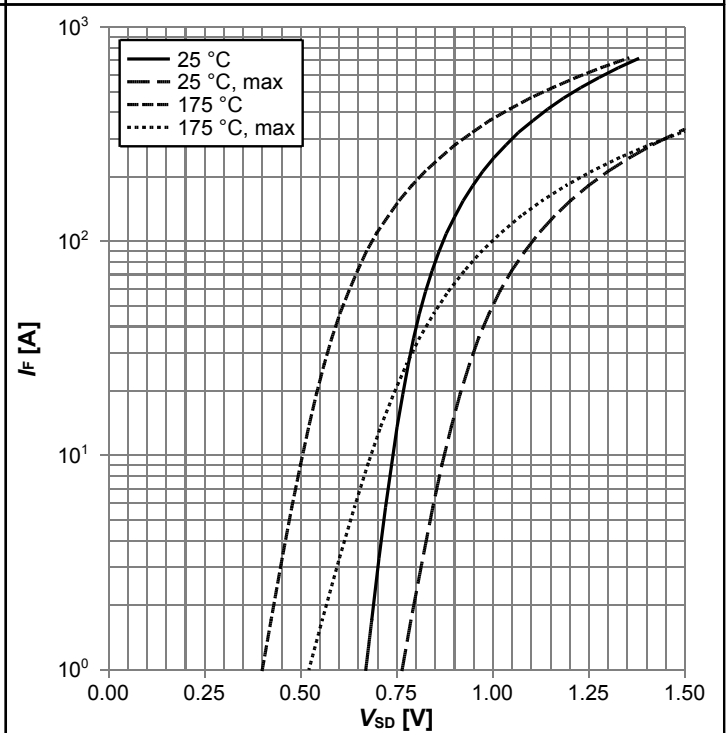
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics
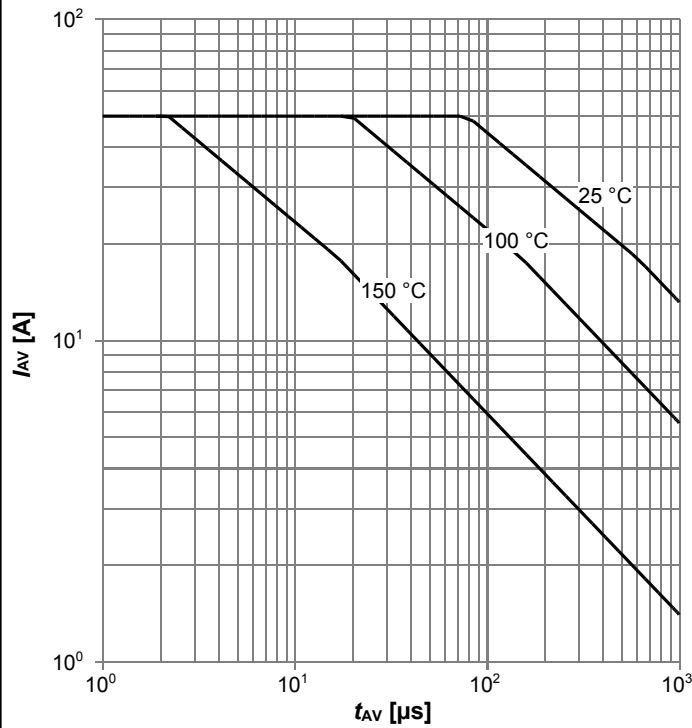
$I_{AS}=f(t_{AV})$; R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge
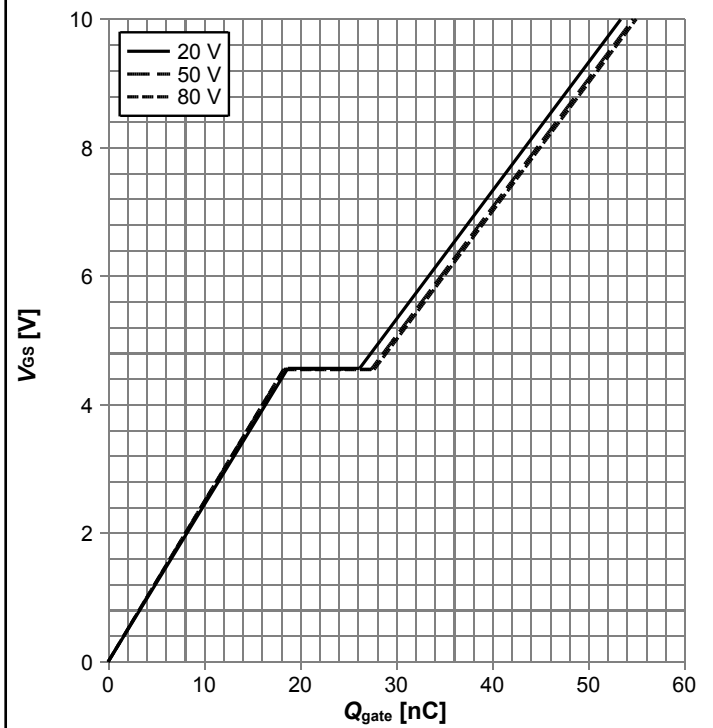
$V_{GS}=f(Q_{gate})$, I_D=25 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage
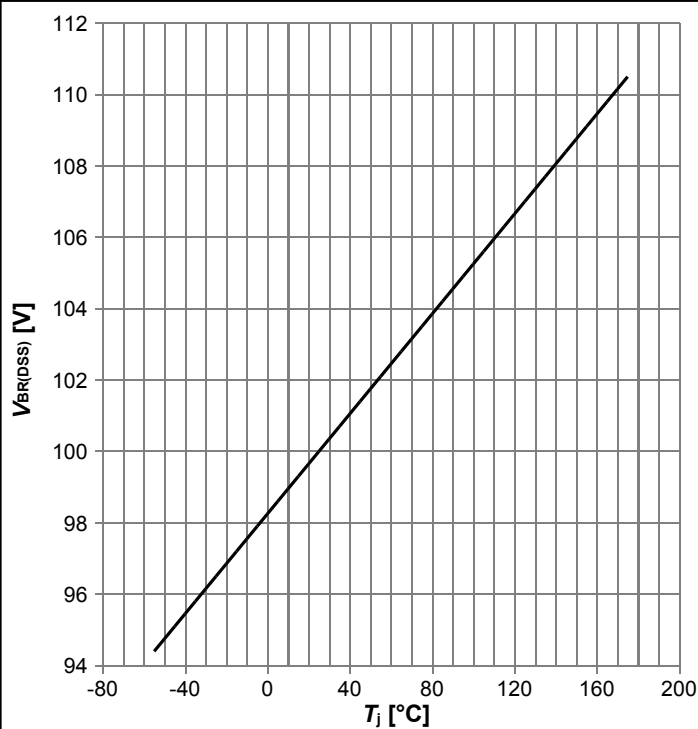
$V_{BR(DSS)}=f(T_j)$; I_D=10 mA

Diagram Gate charge waveforms

5 Package Outlines
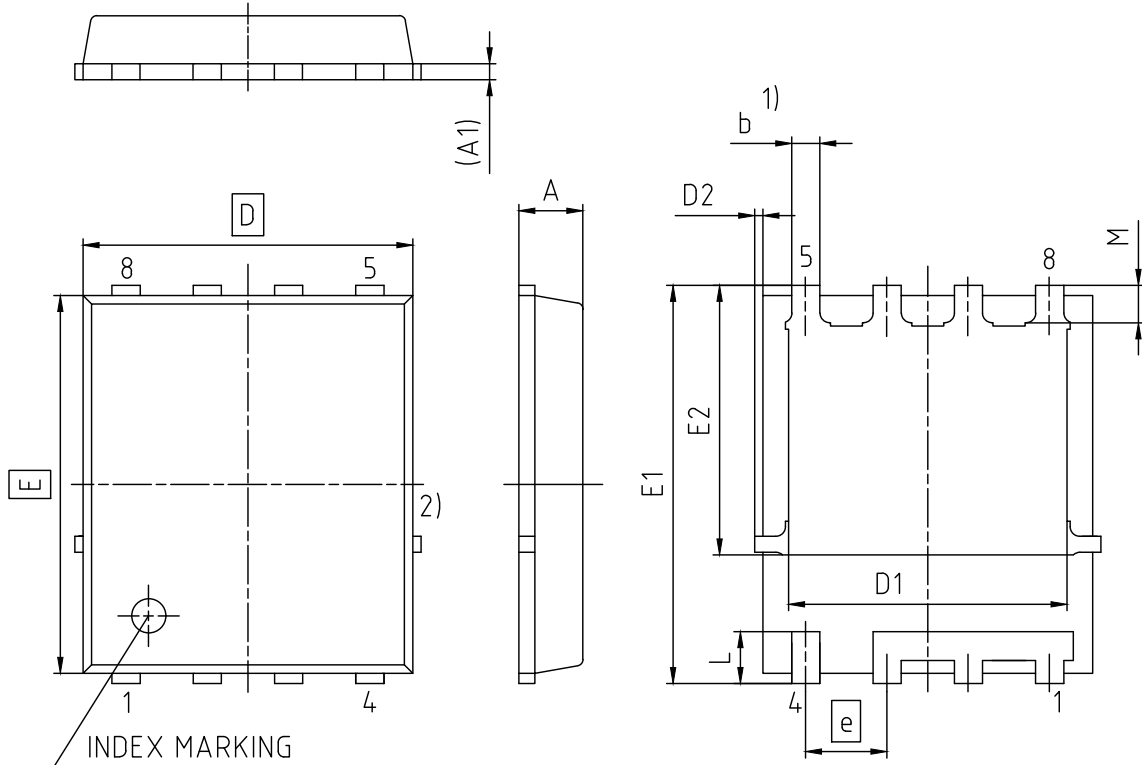
1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.26	0.54
D	4.80	5.35
D1	3.70	4.40
D2	0.00	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.42
e	1.27	
L	0.69	0.90
M	0.45	0.69

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0   1   2   3mm
EUROPEAN PROJECTION
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Figure 1   Outline PG-TDSON-8 FL, dimensions in mm

PG-TDSON-8-FL: Recommended Boardpads & Apertures
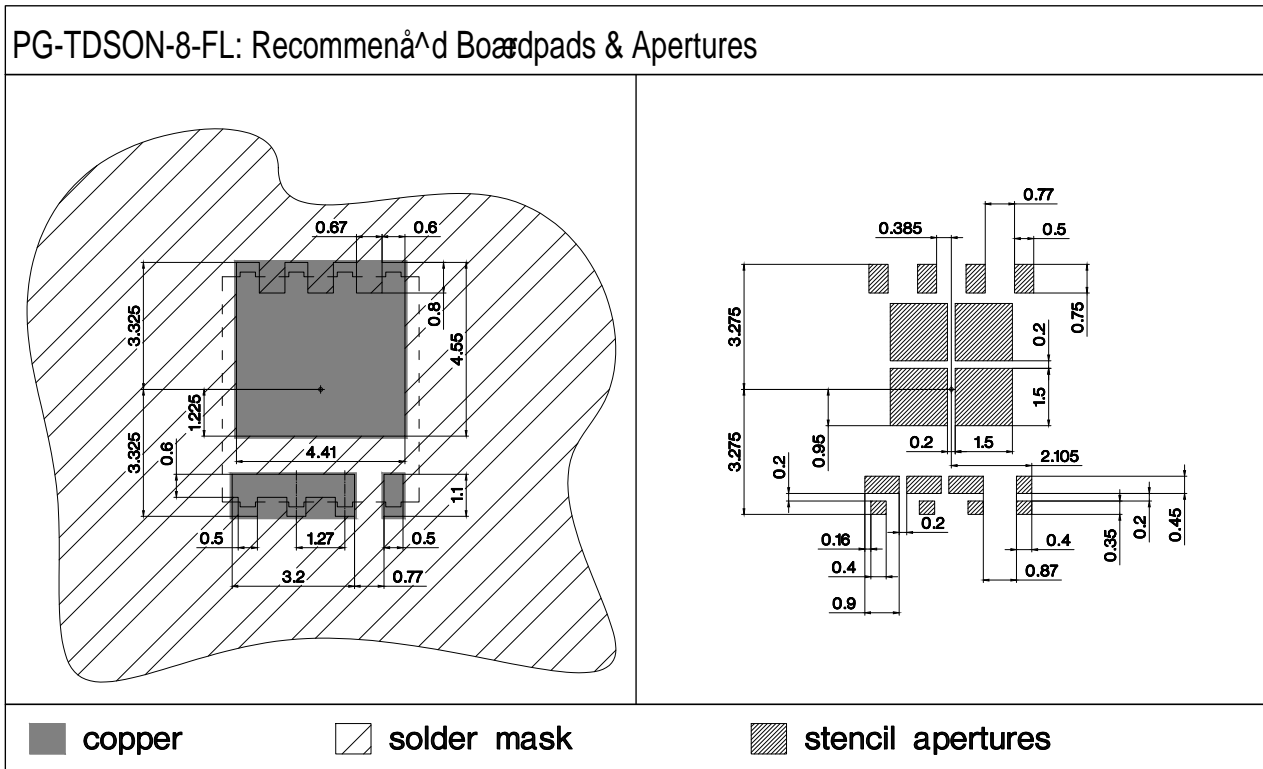
Figure 2   Outline Boardpads (TDSON-8 FL)

Revision History

ISC030N10NM6

Revision: 2023-02-14, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-07-05	Release of final version
2.1	2021-07-20	Update Diagram 10
2.2	2023-02-14	Update SOA Diagram

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