

PSMN059-150Y

N-channel TrenchMOS SiliconMAX standard level FET 3 October 2013 Product data sheet

1. General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

3. Applications

- · Class D amplifier
- DC-to-DC converters
- Motion control
- Switched-mode power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C		-	-	150	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u> ; <u>Fig. 3</u>		-	-	43	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	113	W
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 12 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 9; Fig. 10		-	46	59	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 12 A; V _{DS} = 75 V; Fig. 11; Fig. 12		-	9.1	-	nC



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	[q]	G
4	G	gate	و ق ق ق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN059-150Y	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN059-150Y	059150

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	150	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 150$ °C; $R_{GS} = 20$ Ω	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1</u> ; <u>Fig. 3</u>	-	43	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 1</u>	-	27.7	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$; Fig. 3	-	129	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	113	W
T _{stg}	storage temperature		-55	150	°C

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Symbol	Parameter	Conditions	M	/lin	Max	Unit
Tj	junction temperature		-:	55	150	°C
Source-dra	in diode					-
I _S	source current	T _{mb} = 25 °C	-		52	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-		208	Α
Avalanche	ruggedness					-
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_{D} = 12.1 A; V_{sup} ≤ 150 V; unclamped; t_{p} = 0.21 ms; R_{GS} = 50 Ω	-		255	mJ

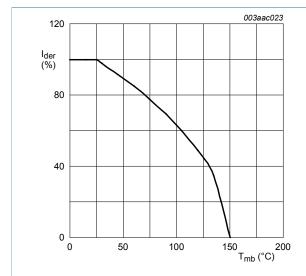


Fig. 1. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

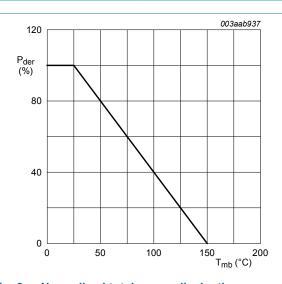


Fig. 2. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \,\%$$

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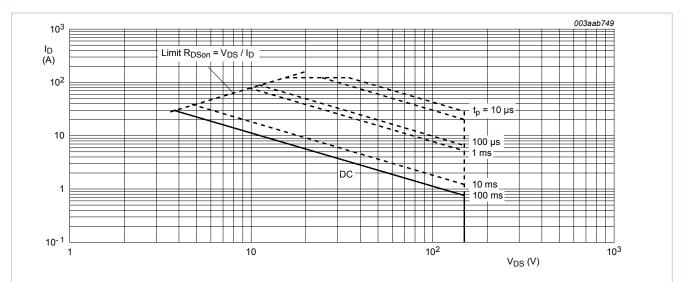


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25 \,^{\circ}C; I_{DM}$$
 is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	mounted on a printed-circuit board; vertical in still air; Fig. 4	-	-	1.1	K/W

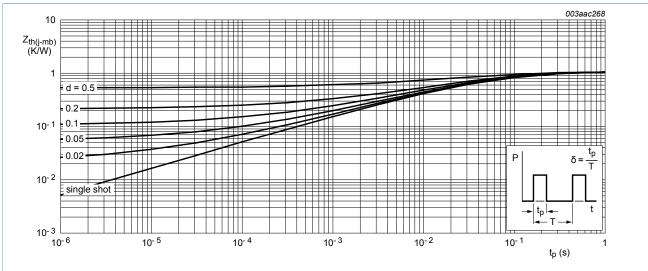


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	150	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	133	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 7; Fig. 8	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C; Fig. 7; Fig. 8	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 7; Fig. 8	-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 120 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 120 V; V _{GS} = 0 V; T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
200	drain-source on-state resistance	V _{GS} = 10 V; I _D = 12 A; T _j = 25 °C; Fig. 9; Fig. 10	-	46	59	mΩ
		V _{GS} = 10 V; I _D = 12 A; T _j = 150 °C; Fig. 9; Fig. 10	-	101	135	mΩ
R _G	gate resistance	f = 1 MHz	-	1.1	-	Ω
Dynamic ch	naracteristics		1	'	'	,
Q _{G(tot)}	total gate charge	I _D = 12 A; V _{DS} = 75 V; V _{GS} = 10 V;	-	27.9	-	nC
Q _{GS}	gate-source charge	Fig. 11; Fig. 12	-	6.3	-	nC
Q_{GD}	gate-drain charge		-	9.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I _D = 12 A; V _{DS} = 75 V; <u>Fig. 11</u> ; <u>Fig. 12</u>	-	4.8	-	V
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz;	-	1529	-	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 13</u>	-	208	-	pF
C _{rss}	reverse transfer capacitance		-	66	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 75 V; R_L = 3 Ω ; V_{GS} = 10 V;	-	14.2	-	ns
t _r	rise time	$R_{G(ext)} = 5.6 \Omega$	-	42	-	ns
t _{d(off)}	turn-off delay time		-	54.2	-	ns
t _f	fall time		-	11.1	-	ns
Source-dra	in diode				-	
V _{SD}	source-drain voltage	I _S = 12 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 14</u>	-	0.9	1.2	V

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{rr}	reverse recovery time	I_S = 12 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 30 V	-	67	-	ns
Q_r	recovered charge	I_S = 12 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V	-	226	-	nC

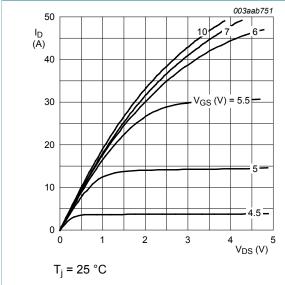


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

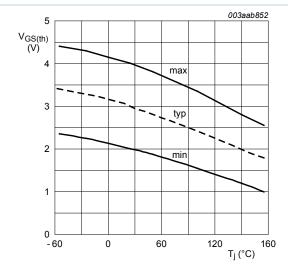
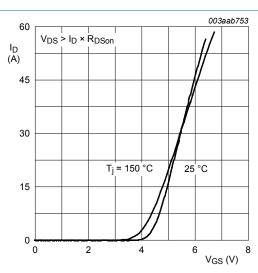


Fig. 7. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$



 T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

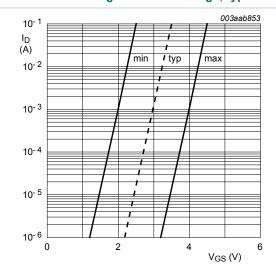


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$$T_j=25\,^{\circ}C; V_{DS}=5\,V$$

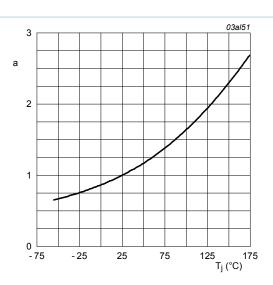


Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

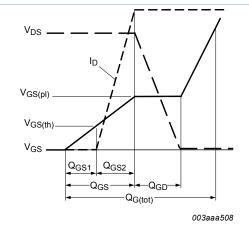


Fig. 11. Gate charge waveform definitions

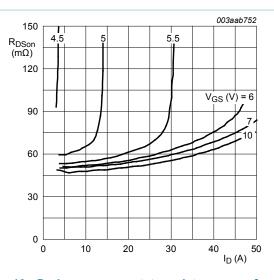


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$$T_j=25\,^{\circ}C$$

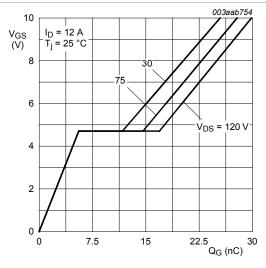


Fig. 12. Gate-source voltage as a function of gate charge; typical values

$$I_D = 12A$$
; $V_{DS} = 30,75$ and $120V$

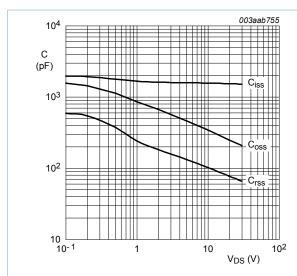
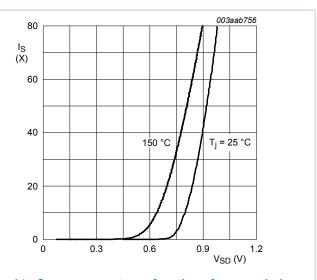


Fig. 13. Input, output and reverse transfer capacitances | Fig. 14. Source current as a function of source-drain as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$



voltage; typical values

$$T_j = 25 \,{}^{\circ}C \, and 150 \,{}^{\circ}C; \, V_{GS} = 0 \, V$$

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11. Package outline

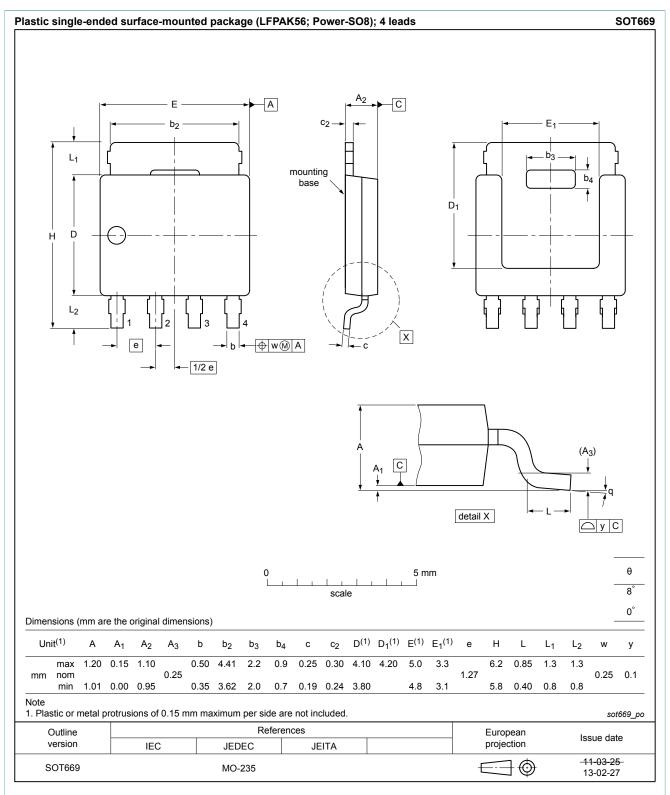


Fig. 15. Package outline LFPAK56; Power-SO8 (SOT669)

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