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S E M I C O N D U C T O R
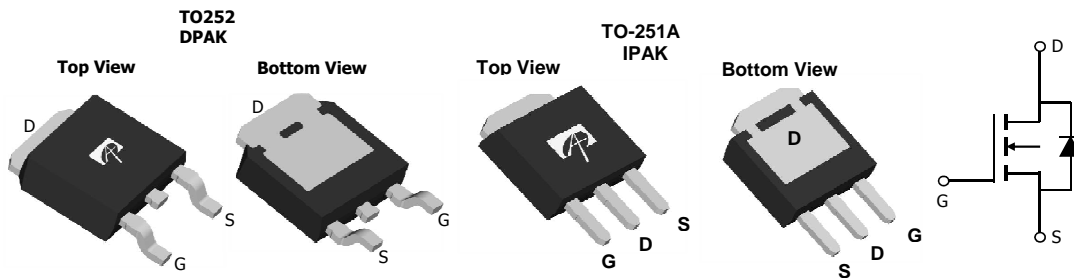
AOD4126/AOI4126
100V N-Channel MOSFET
SDMOS™

General Description

The AOD4126&AOI4126 are fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge.The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

V_{DS}	100V
I_D (at V_{GS}=10V)	43A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 24mΩ
$R_{DS(ON)}$ (at V_{GS} = 7V)	< 30mΩ

100% UIS Tested
100% R_g Tested

Green Product

TO252 DPAK — Top View, Bottom View

TO-251A IPAK — Top View, Bottom View

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current ^{B}	T_C=25°C	I_D	43	A
	T_C=100°C		30	
Pulsed Drain Current ^{C}		I_{DM}	100	
Continuous Drain Current ^{A}	T_A=25°C	I_{DSM}	7.5	A
	T_A=70°C		6	
Avalanche Current ^{C}		I_{AS}, I_{AR}	28	A
Avalanche energy L=0.1mH ^{C}		E_{AS}, E_{AR}	39	mJ
Power Dissipation ^{B}	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Power Dissipation ^{A}	T_A=25°C	P_{DSM}	3	W
	T_A=70°C		1.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A}	t ≤ 10s	$R_{θJA}$	8	10	°C/W
Maximum Junction-to-Ambient $^{A D}$	Steady-State		35	42	°C/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	1	1.5	°C/W

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Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		100			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=100V, V$_{GS}$=0V				10	µA
			T$_J$=55℃			50	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±25V				100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250µA		2	3.3	4	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		100			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=20A			19	24	mΩ
			T$_J$=125℃		36	43	
		V$_{GS}$=7V, I$_D$=15A			23.5	30	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=20A			34		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.66	1	V
I$_S$	Maximum Body-Diode Continuous Current					40	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=50V, f=1MHz		1400	1770	2200	pF
C$_{oss}$	Output Capacitance			115	165	214	pF
C$_{rss}$	Reverse Transfer Capacitance			33	55	80	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		0.3	0.65	1.0	Ω
SWITCHING PARAMETERS							
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=50V, I$_D$=20A		14	28	42	nC
Q$_{gs}$	Gate Source Charge			4	9	14	nC
Q$_{gd}$	Gate Drain Charge			6	10	14	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=50V, R$_L$=2.5Ω, R$_{GEN}$=3Ω			12		ns
t$_r$	Turn-On Rise Time				4		ns
t$_{D(off)}$	Turn-Off DelayTime				17		ns
t$_f$	Turn-Off Fall Time				5		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=20A, dI/dt=500A/µs		12	20	26	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=20A, dI/dt=500A/µs		60	82	110	nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25° C. The Power dissipation P$_{DSM}$ is based on R$_{θJA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T$_J$=25° C.
D. The R$_{θJA}$ is the sum of the thermal impedence from junction to case R$_{θJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25° C.

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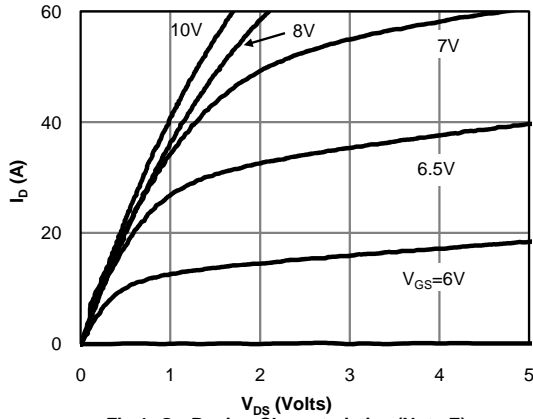**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

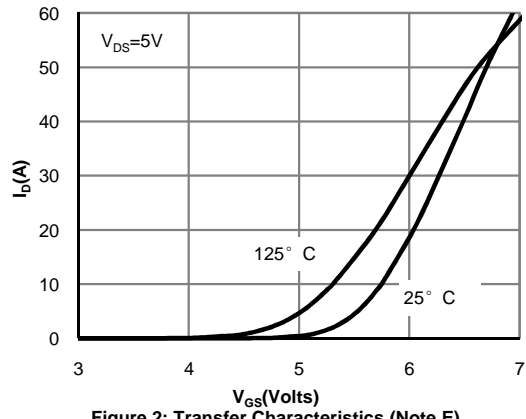Fig 1: On-Region Characteristics (Note E)
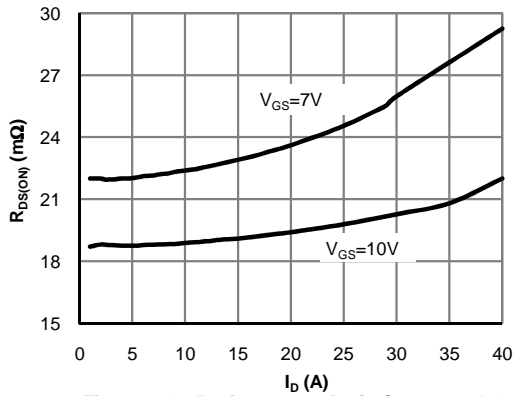
Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)
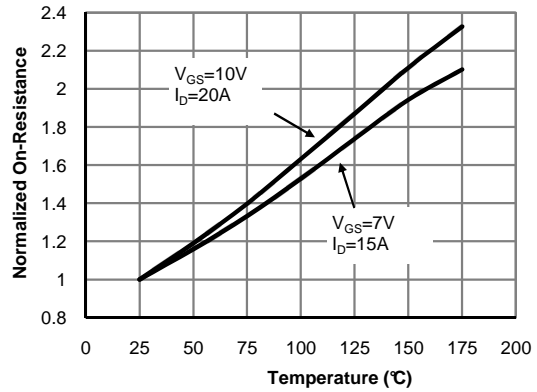
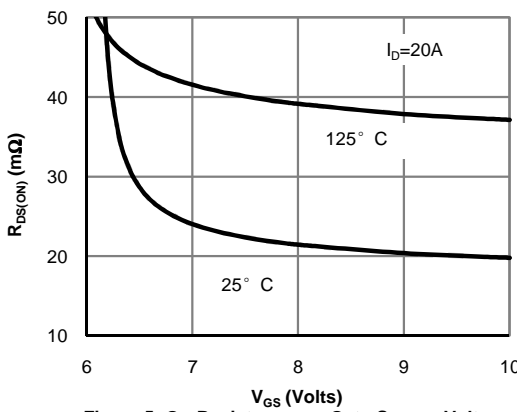Figure 4: On-Resistance vs. Junction Temperature (Note E)

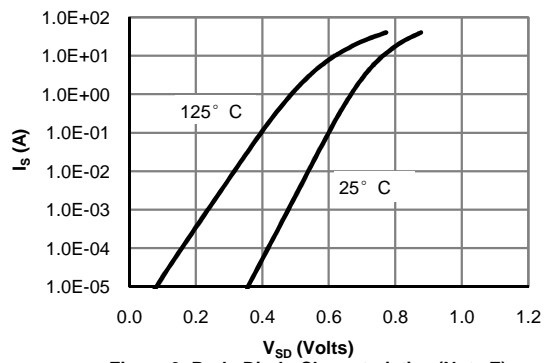Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

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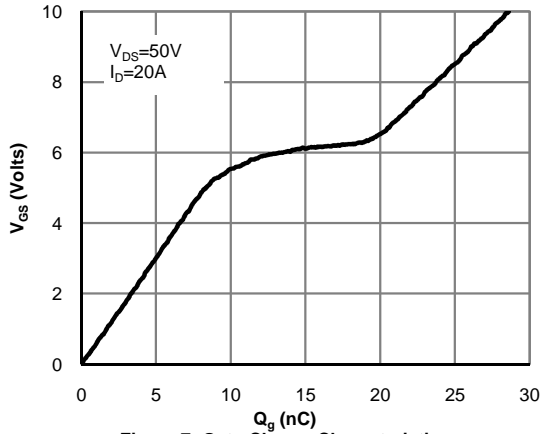
Figure 7: Gate-Charge Characteristics
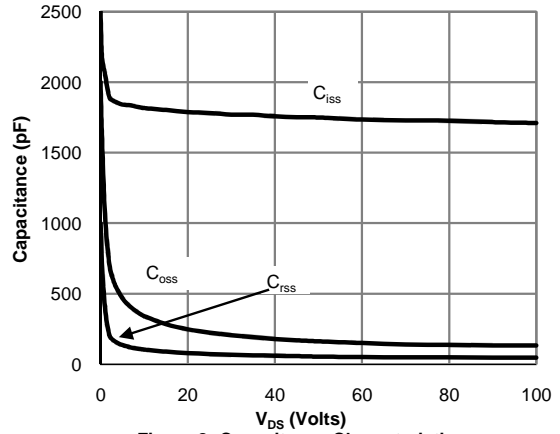
Figure 8: Capacitance Characteristics
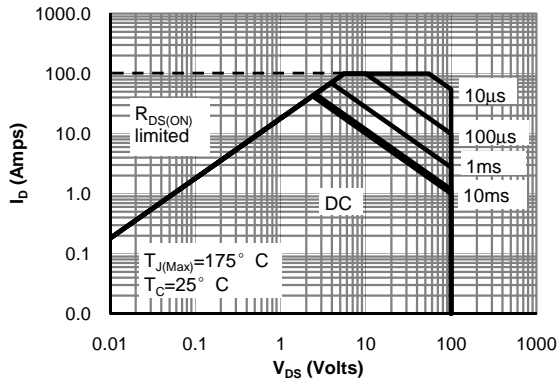
Figure 9: Maximum Forward Biased Safe
Operating Area (Note F)
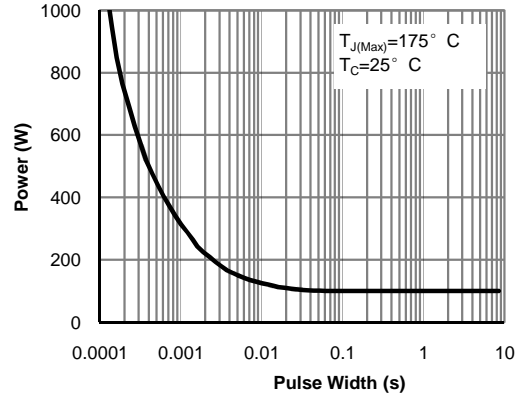
Figure 10: Single Pulse Power Rating Junction-to-
Case (Note F)
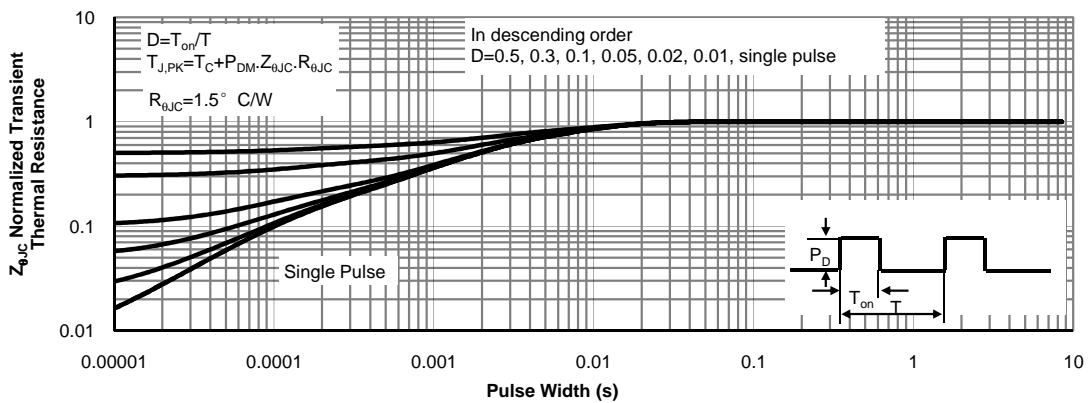
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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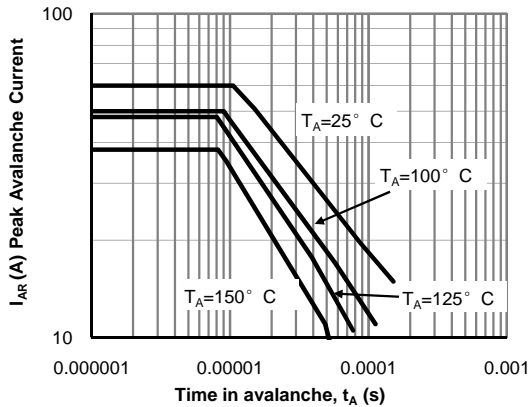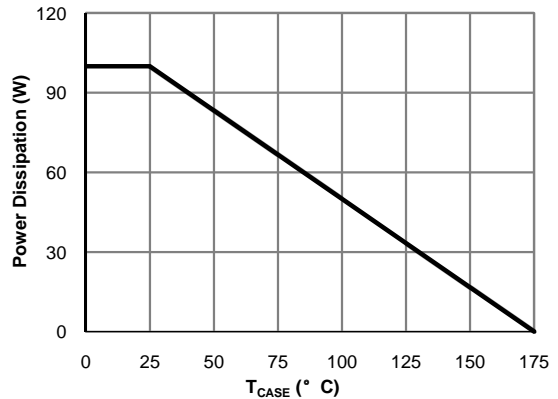

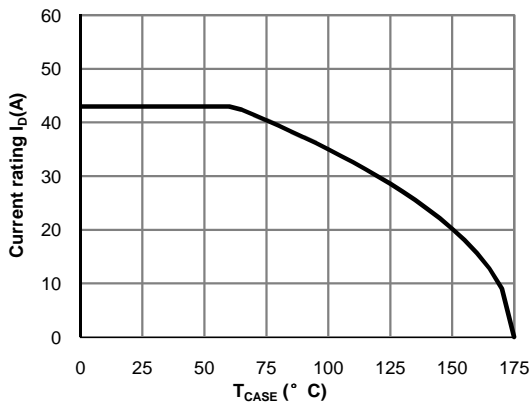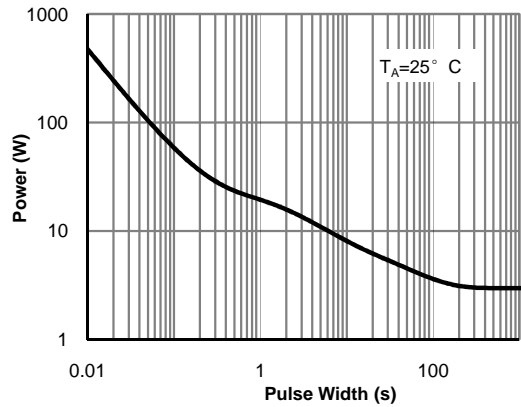Figure 12: Single Pulse Avalanche capability (Note C)

Figure 13: Power De-rating (Note F)

Figure 14: Current De-rating (Note F)

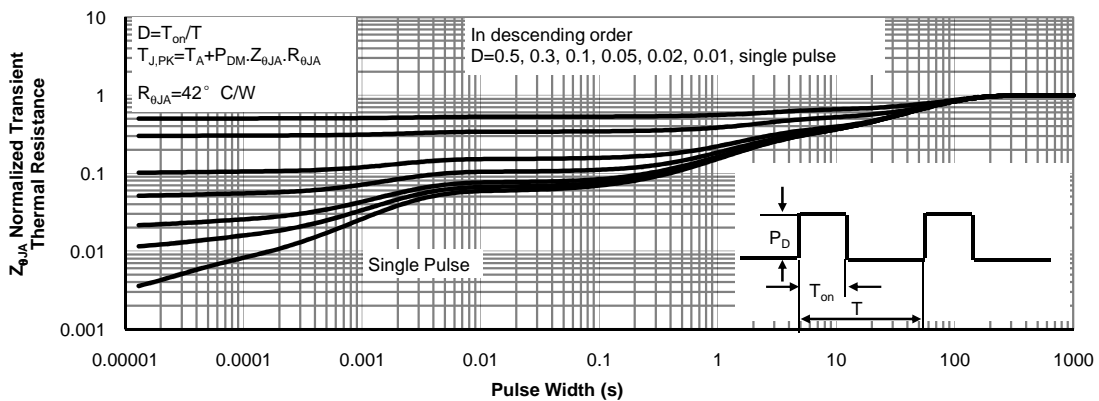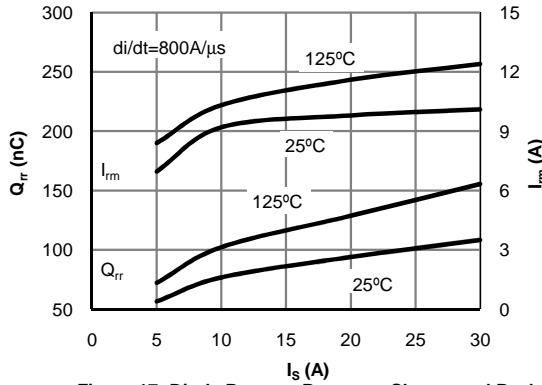Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA}=42°$ C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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Figure 17: Diode Reverse Recovery Charge and Peak
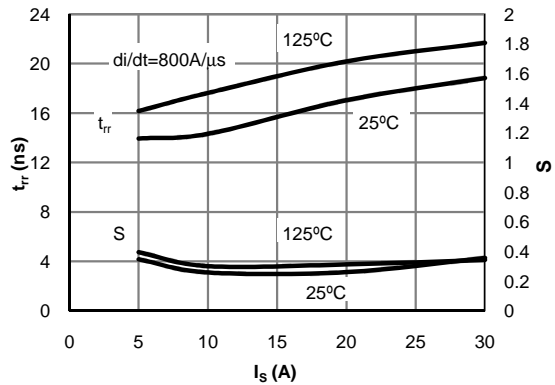Current vs. Conduction Current

Figure 18: Diode Reverse Recovery Time and
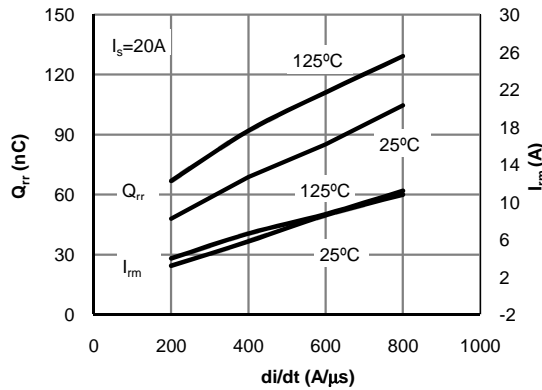Softness Factor vs. Conduction Current

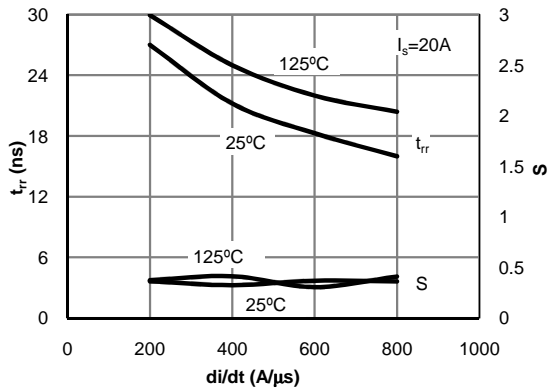Figure 19: Diode Reverse Recovery Charge and Peak
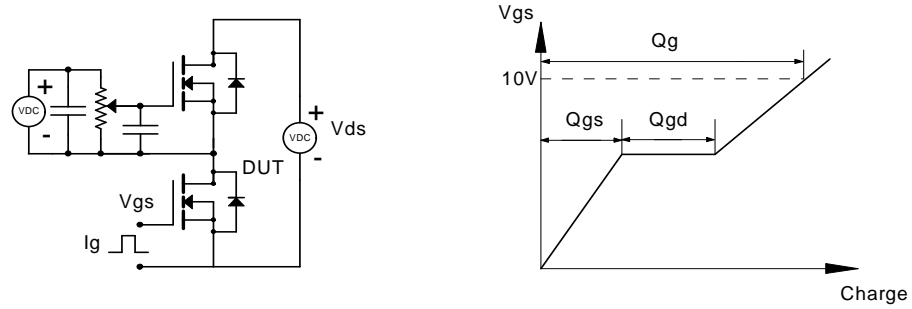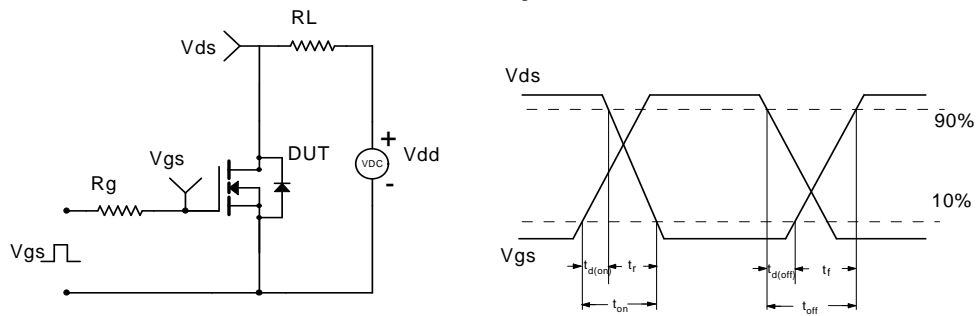Current vs. di/dt

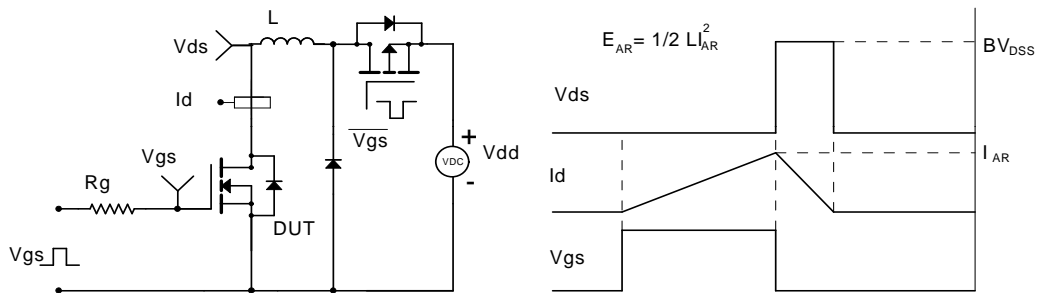Figure 20: Diode Reverse Recovery Time and
Softness Factor vs. di/dt

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Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \, LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$