

MOSFET, N-Channel, POWERTRENCH®

40 V, 18.6 A, 4.5 mΩ

FDS8840NZ

General Description

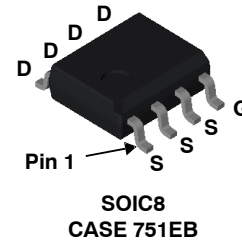
The FDS8840NZ has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.

Features

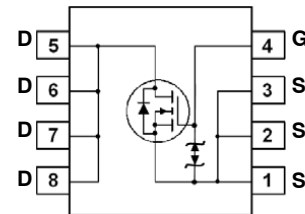
- Max $r_{DS(on)}$ = 4.5 mΩ at V_{GS} = 10 V, I_D = 18.6 A
- Max $r_{DS(on)}$ = 6.0 mΩ at V_{GS} = 4.5 V, I_D = 14.9 A
- HBM ESD Protection Level of 6 kV Typical (Note 3)
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$ and Fast Switching
- High Power and Current Handling Capability
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

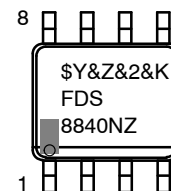
- Synchronous Buck for Vcore and Server
- Notebook Battery Pack
- Load Switch



PIN ASSIGNMENT



MARKING DIAGRAM



\$Y	= onsemi Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
FDS8840NZ	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDS8840NZ

ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping [†]
FDS8840NZ	FDS8840NZ	SOIC8 (Pb-Free / Halogen Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DS}	Drain to Source Voltage	40	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current Continuous	18.6	A
	Drain Current Pulsed	63	
E _{AS}	Single Pulse Avalanche Energy (Note 4)	600	mJ
P _D	Power Dissipation, T _A = 25°C (Note 1a)	2.5	W
	Power Dissipation, T _A = 25°C (Note 1b)	1.0	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		31		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		–6		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 18.6 A		3.9	4.5	mΩ
		V _{GS} = 4.5 V, I _D = 14.9 A		4.6	6.0	
		V _{GS} = 10 V, I _D = 18.6 A, T _J = 125°C		5.9	7.0	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 18.6 A		83		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		5665	7535	pF
C _{oss}	Output Capacitance			650	865	pF
C _{rss}	Reverse Transfer Capacitance			445	670	pF
R _g	Gate Resistance			1.2		Ω

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$, $I_D = 18.6\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$		18	32	ns
t_r	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			57	103	ns
t_f	Fall Time			11	20	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 20\text{ V}$, $I_D = 18.6\text{ A}$	103	144	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$		54	76	nC
Q_{gs}	Gate to Source Charge			16		nC
Q_{gd}	Gate to Drain "Miller" Charge			19		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 18.6\text{ A}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 18.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a.) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b.) 125°C/W when mounted on a minimum pad

- Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty cycle $< 2.0\%$.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- Starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 20\text{ A}$, $V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

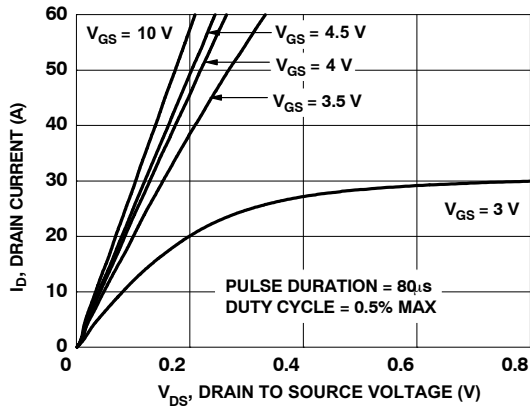


Figure 1. On-Region Characteristics

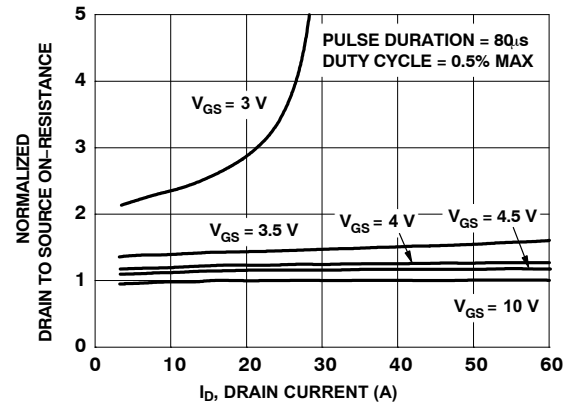


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

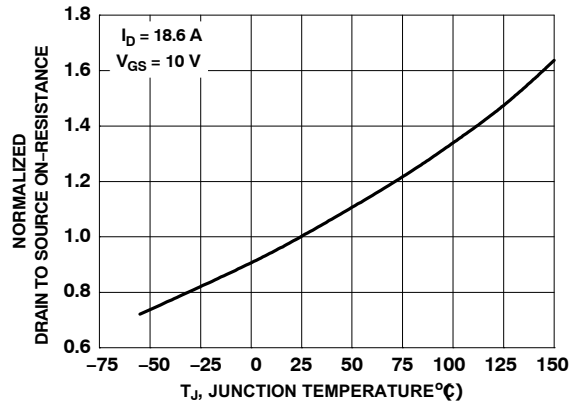


Figure 3. Normalized On-Resistance vs Junction Temperature

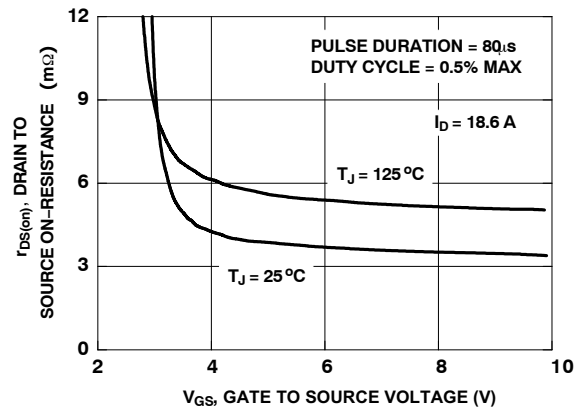


Figure 4. On-Resistance vs Gate to Source Voltage

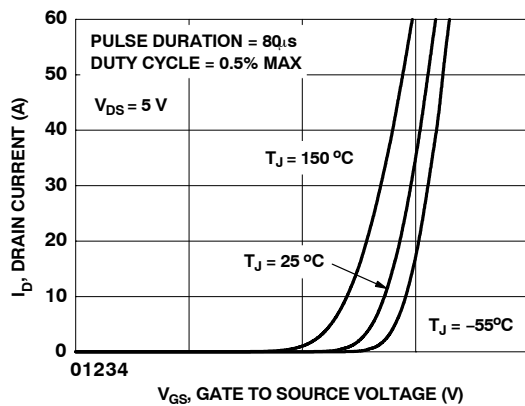


Figure 5. Transfer Characteristics

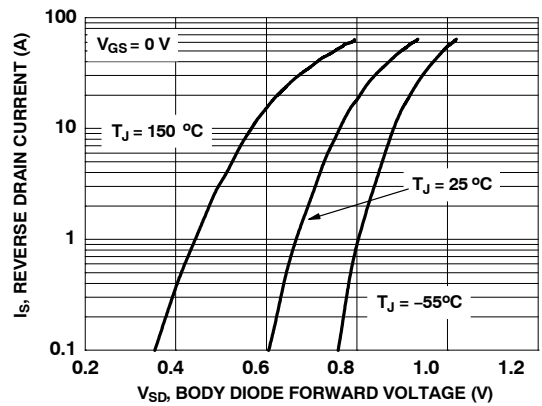


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

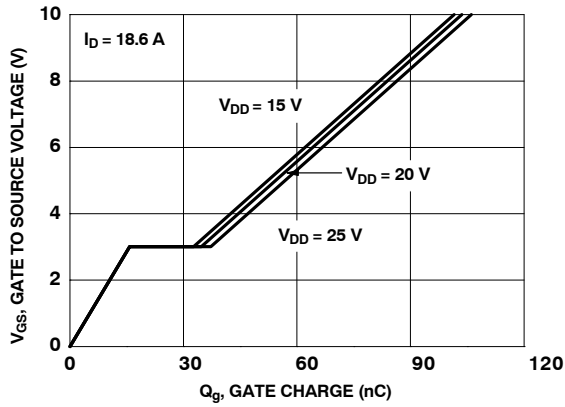


Figure 7. Gate Charge Characteristics

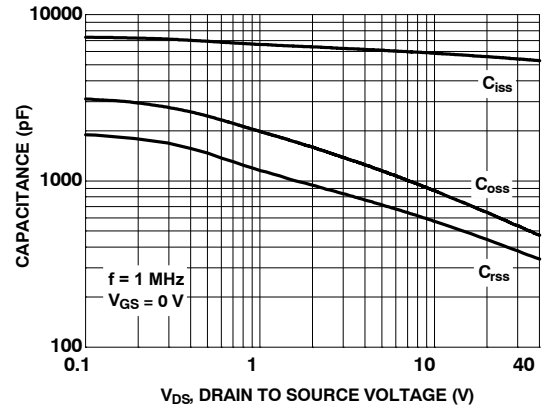


Figure 8. Capacitance vs Drain to Source Voltage

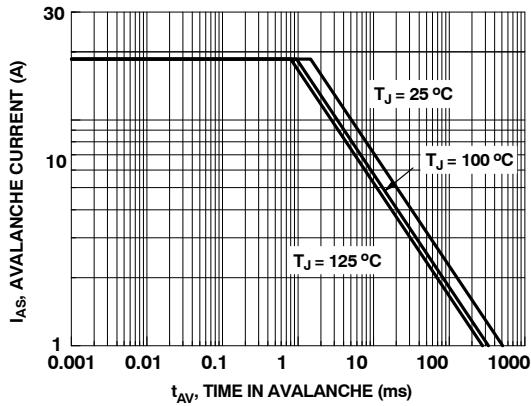


Figure 9. Unclamped Inductive Switching Capability

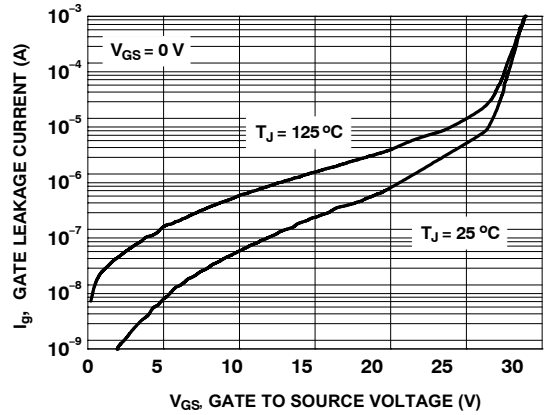


Figure 10. I_{GSS} vs V_{GS}

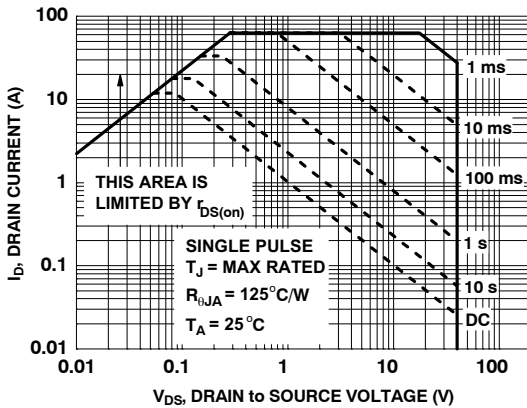


Figure 11. Forward Bias Safe Operating Area

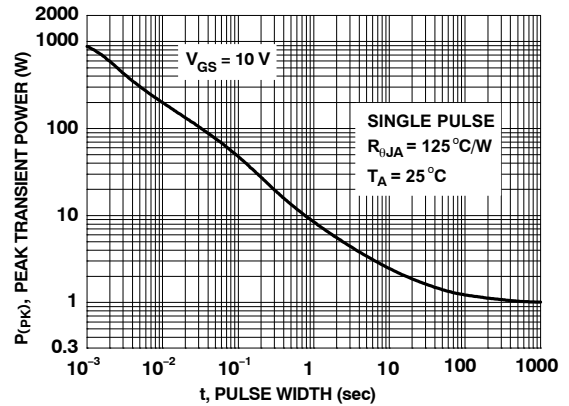


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

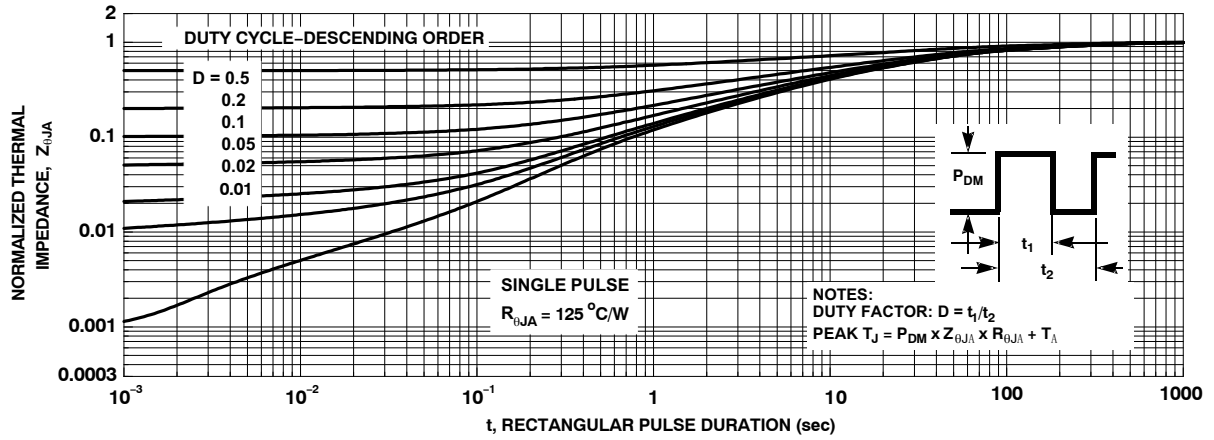
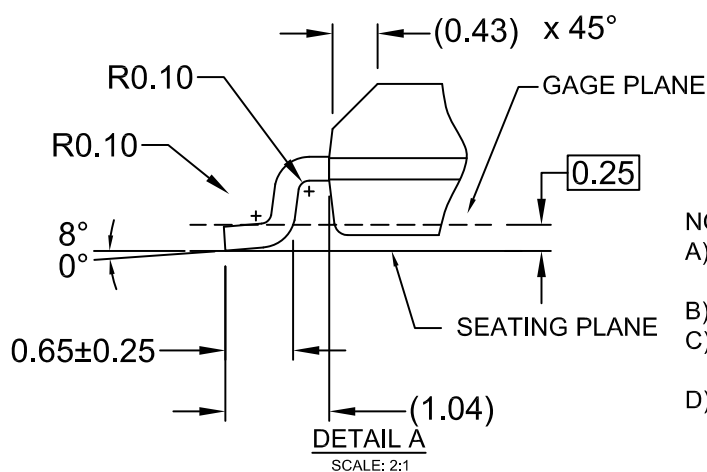
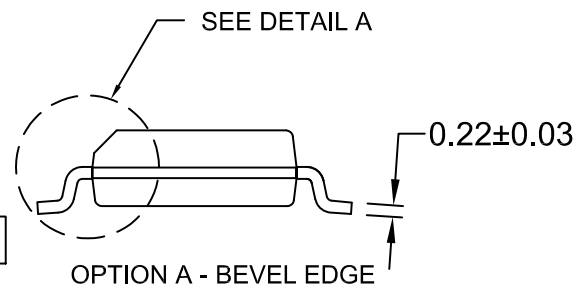
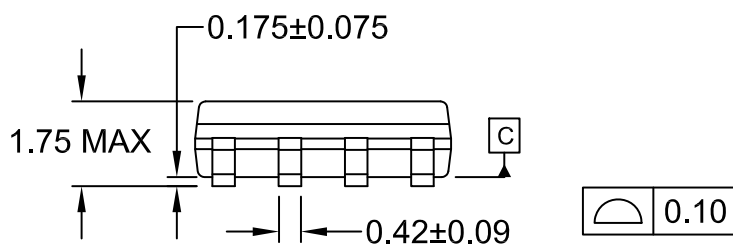
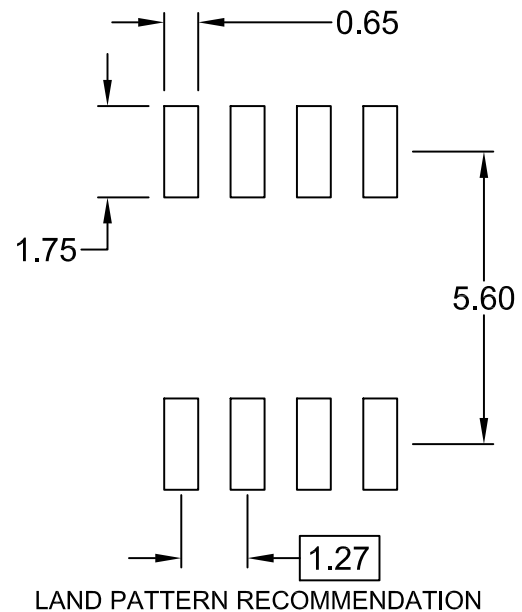
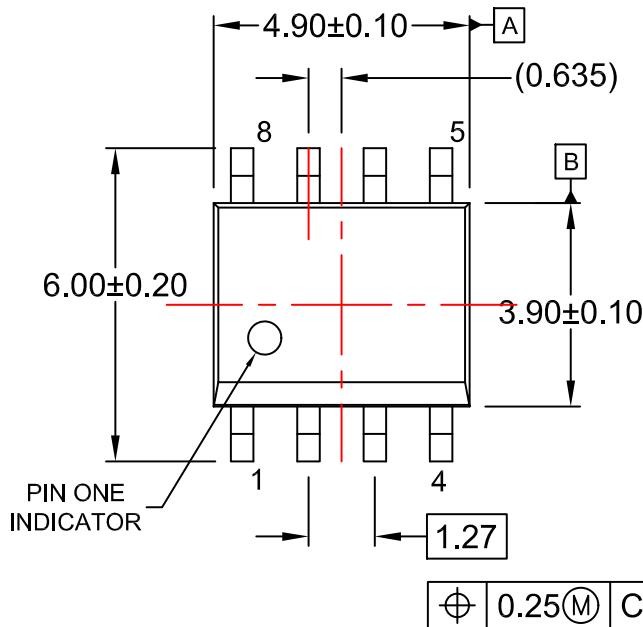
(T_J = 25°C unless otherwise noted)

Figure 13. Transient Thermal Response Curve

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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