

MOSFET

StrongIRFET™2 Power-Transistor, 40 V

Features

- Optimized for wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

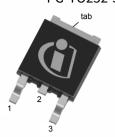
Product validation

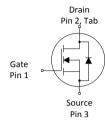
Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

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Parameter	Value	Unit				
$V_{ m DS}$	40	V				
$R_{\mathrm{DS(on),max}}$	2.3	mΩ				
I _D	143	А				
Q _{oss}	76	nC				
Q _G (0V10V)	68	nC				











Type/Ordering Code	Package	Marking	Related Links
IPD023N04NF2S	PG-TO252-3	023N04NS	-

Public

StrongIRFET™2 Power-Transistor, 40 V IPD023N04NF2S



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StronglRFET™2 Power-Transistor, 40 V IPD023N04NF2S



1 Maximum ratings

at T_{Δ} =25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	
raiailletei	Syllibot	Min.	Тур.	Мах.	Oilit	Note/ Test Condition	
Continuous drain current ¹⁾	I _D	-	-	143 110 27	А	$V_{\rm GS}$ =10 V, $T_{\rm C}$ =25 °C $V_{\rm GS}$ =10 V, $T_{\rm C}$ =100 °C $V_{\rm GS}$ =10 V, $T_{\rm A}$ =25°C, $R_{\rm THJA}$ =50°C/W ²⁾	
Pulsed drain current ³⁾	I _{D,pulse}	-	-	572	А	T _A =25 °C	
Avalanche energy, single pulse ⁴⁾	E _{AS}	-	-	167	mJ	$I_{\rm D}$ =70 A, $R_{\rm GS}$ =25 Ω	
Gate source voltage	V_{GS}	-20	-	20	V	-	
Power dissipation	P_{tot}	-	-	150 3.0	w	$T_{\rm C}$ =25 °C $T_{\rm A}$ =25 °C, $R_{\rm THJA}$ =50 °C/W ²⁾	
Operating and storage temperature	$T_{\rm j},T_{\rm stg}$	-55	-	175	°C	-	

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions

Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm 2 (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

StrongIRFET™2 Power-Transistor, 40 V IPD023N04NF2S



2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Nato/Test Condition	
raiailletei	Syllibol	Min.	Тур.	Мах.	Offic	Note/ Test Condition	
Thermal resistance, junction - case	R_{thJC}	-	-	1.0	°C/W	-	
Thermal resistance, junction - ambient, R_{thJA} 6 cm ² cooling area ⁵⁾		-	-	50	°C/W	-	
Thermal resistance, junction - ambient, minimal footprint	$R_{ m thJA}$	-	-	75	°C/W	-	

Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm 2 (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

StronglRFET™2 Power-Transistor, 40 V IPD023N04NF2S



3 Electrical characteristics

at T_i =25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	
Parameter	Symbol	Min.	Тур.	Мах.		Note/ Test Condition	
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{\rm GS}$ =0 V, $I_{\rm D}$ =1 mA	
Gate threshold voltage	$V_{\rm GS(th)}$	2.2	2.8	3.4	V	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 81 \mu \text{A}$	
Zero gate voltage drain current	I _{DSS}	-	0.1 10	1 100	μΑ	$V_{\rm DS}$ =40 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =25 °C $V_{\rm DS}$ =40 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =125 °C	
Gate-source leakage current	I _{GSS}	-	10	100	nA	$V_{\rm GS}$ =20 V, $V_{\rm DS}$ =0 V	
Drain-source on-state resistance	$R_{\mathrm{DS(on)}}$	-	1.9 2.2	2.3 3.1	mΩ	V_{GS} =10 V, I_{D} =70 A V_{GS} =6 V, I_{D} =35 A	
Gate resistance	R_{G}	-	3.0	-	Ω	-	
Transconductance ⁶⁾	g_{fs}	125	-	-	S	$ V_{\rm DS} \ge 2 I_{\rm D} R_{\rm DS(on)max}, I_{\rm D} = 70 \text{ A}$	

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol		Values			Nato/Tost Condition	
- Parameter	Syllibot	Min.	Тур.	Мах.	Unit	Note/ Test Condition	
Input capacitance	C _{iss}	-	4800	-	pF	V_{GS} =0 V, V_{DS} =20 V, f =1 MHz	
Output capacitance	Coss	-	1780	-	pF	V_{GS} =0 V, V_{DS} =20 V, f =1 MHz	
Reverse transfer capacitance	C _{rss}	-	98	-	pF	V_{GS} =0 V, V_{DS} =20 V, f =1 MHz	
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{\rm DD}$ =20 V, $V_{\rm GS}$ =10 V, $I_{\rm D}$ =70 A, $R_{\rm G,ext}$ =1.6 Ω	
Rise time	t _r	-	15	-	ns	$V_{\rm DD}$ =20 V, $V_{\rm GS}$ =10 V, $I_{\rm D}$ =70 A, $R_{\rm G,ext}$ =1.6 Ω	
Turn-off delay time	$t_{ m d(off)}$	-	35	-	ns	$V_{\rm DD}$ =20 V, $V_{\rm GS}$ =10 V, $I_{\rm D}$ =70 A, $R_{\rm G,ext}$ =1.6 Ω	
Fall time	$t_{\rm f}$	-	15	-	ns	$V_{\rm DD}$ =20 V, $V_{\rm GS}$ =10 V, $I_{\rm D}$ =70 A, $R_{\rm G,ext}$ =1.6 Ω	

Table 6 Gate charge characteristics 7)

Parameter	Symbol	Values			Unit	Note/ Test Condition
raiailietei	Syllibol	Min.	Тур.	Мах.	Oilit	Note/ Test Condition
Gate to source charge	$Q_{ m gs}$	-	21	-	nC	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V
Gate charge at threshold	$Q_{\mathrm{g(th)}}$	-	14	-	nC	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V
Gate to drain charge	$Q_{ m gd}$	-	13	-	nC	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V
Switching charge	Q_{sw}	-	20	-	nC	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V
Gate charge total ⁸⁾	Q_{g}	-	68	102	nC	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V

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Table 6 Gate charge characteristics 7)

Parameter	Symbol	Values			Unit	Note/ Test Condition	
raiailletei	Symbol	Min.	Тур.	Мах.	Oilit	Note/ Test Condition	
Gate plateau voltage	$V_{ m plateau}$	-	4.3	-	V	$V_{\rm DD}$ =20 V, $I_{\rm D}$ =70 A, $V_{\rm GS}$ =0 to 10 V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	61	-	nC	V _{DS} =0.1 V, V _{GS} =0 to 10 V	
Output charge	Q _{oss}	-	76	-	nC	V _{DS} =20 V, V _{GS} =0 V	

 $^{^{7)} \;\;}$ See "Gate charge waveforms" for parameter definition

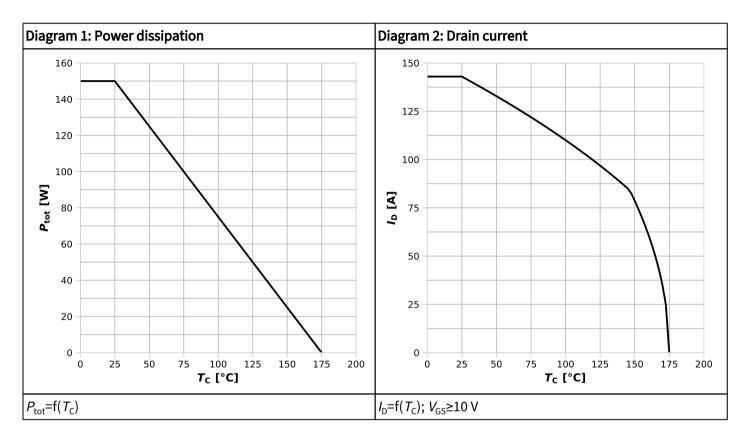
Table 7 Reverse diode

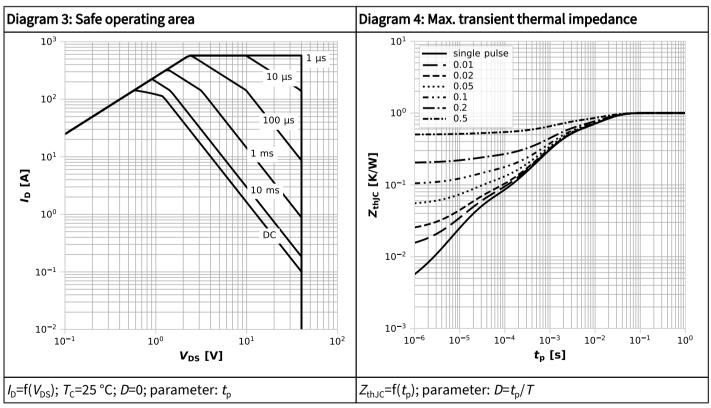
Parameter	Symbol	Values			Linit	Note / Test Condition	
raianietei	Symbol		Тур.	Max.	Unit	Note/ Test Condition	
Diode continuous forward current	I_{S}	-	-	106	А	<i>T</i> _c =25 °C	
Diode pulse current	I _{S,pulse}	-	-	572	А	<i>T</i> _c =25 °C	
Diode forward voltage	$V_{\rm SD}$	-	0.87	1.1	V	$V_{\rm GS}$ =0 V, $I_{\rm F}$ =70 A, $T_{\rm j}$ =25 °C	
Reverse recovery time	t_{rr}	-	44	-	ns	$V_{\rm R}$ =20 V, $I_{\rm F}$ =70 A, d $i_{\rm F}$ /d t =100 A/ μ s	
Reverse recovery charge	$Q_{\rm rr}$	-	45	-	nC	$V_{\rm R}$ =20 V, $I_{\rm F}$ =70 A, d $i_{\rm F}$ /d t =100 A/ μ s	
Reverse recovery time	t _{rr}	-	32	-	ns	$V_{\rm R}$ =20 V, $I_{\rm F}$ =70 A, d $i_{\rm F}$ /d t =500 A/ μ s	
Reverse recovery charge	$Q_{\rm rr}$	-	125	-	nC	$V_{\rm R}$ =20 V, $I_{\rm F}$ =70 A, d $i_{\rm F}$ /d t =500 A/ μ s	

⁸⁾ Defined by design. Not subject to production test.

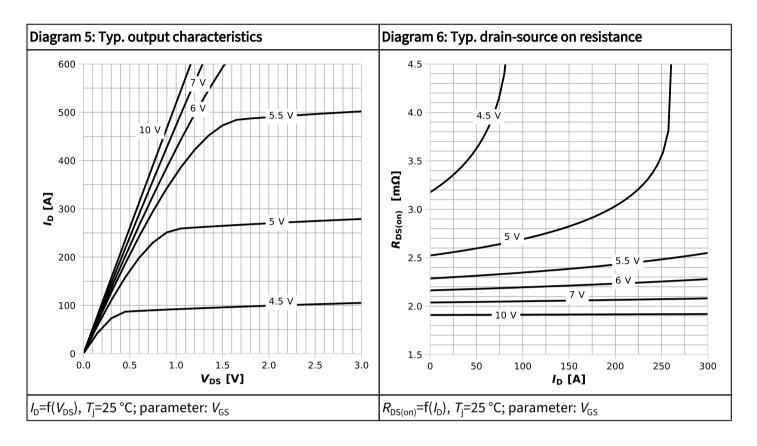


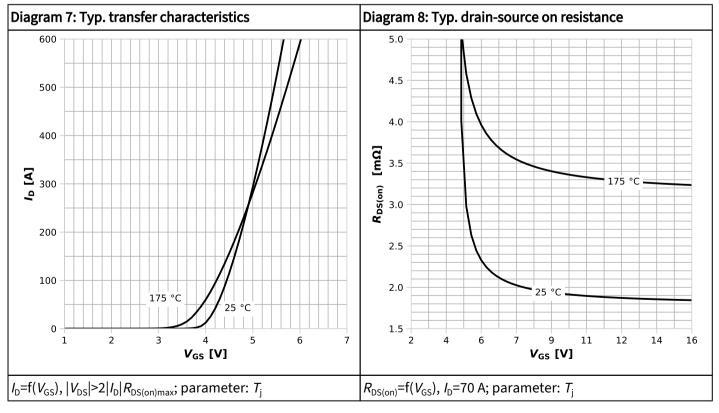
4 Electrical characteristics diagrams



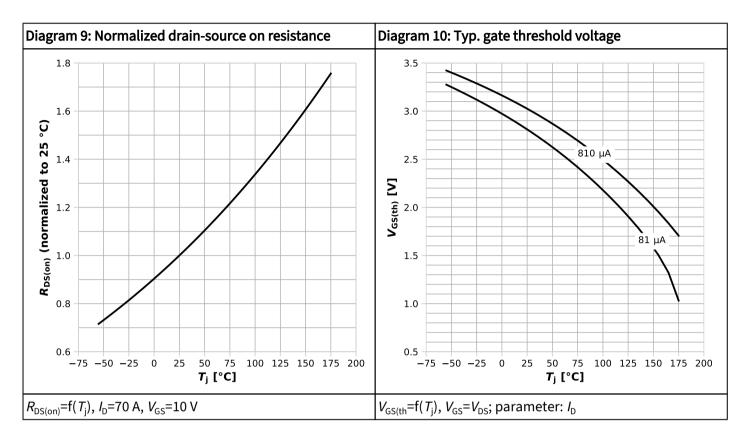


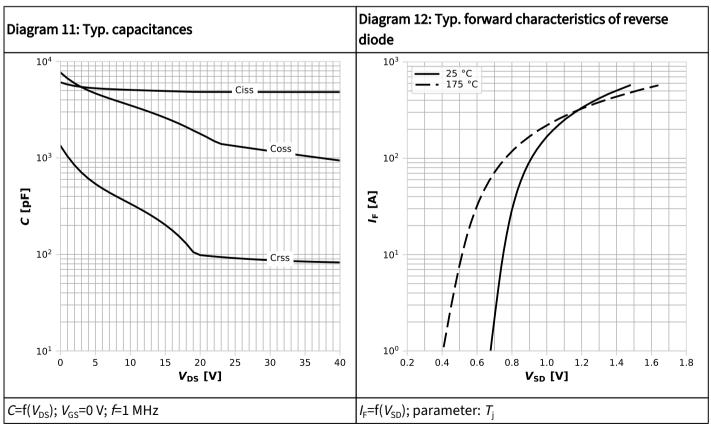




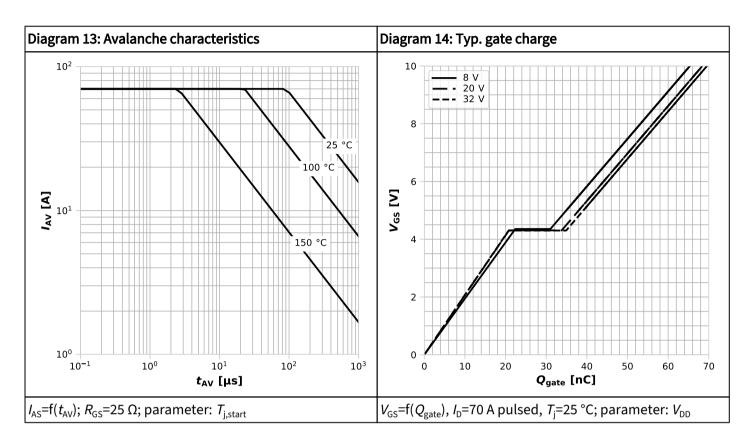


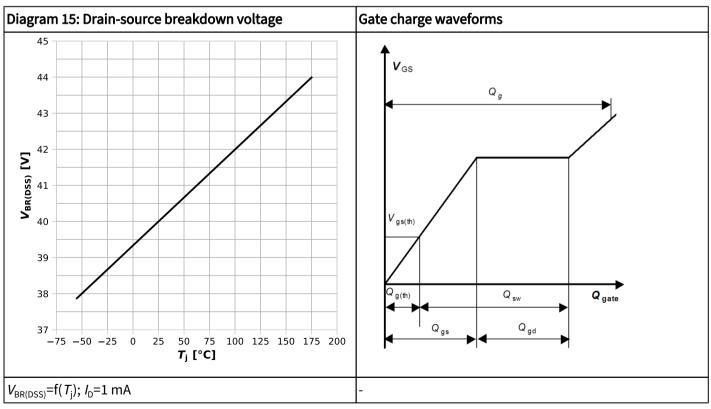






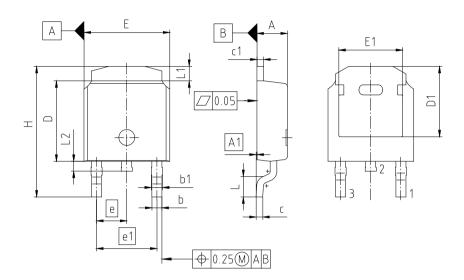








5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TO2	PG-TO252-3-U01					
DIMENSIONS	MILLIMETERS						
DIMENSIONS	MIN.	MAX.					
Α	2.18	2.39					
A1	0.00	0.13					
b	0.64	0.89					
b1	0.76	1.14					
С	0.46	0.61					
c1	0.40	0.89					
D	5.97	6.22					
D1	5.21						
E	6.35	6.73					
E1	4.32						
е	2.29						
e1	4.58						
N	:	3					
Н	9.40	10.41					
L	1.40	1.78					
L1	0.89	1.27					
L2	0.50	1.02					

Figure 1 Outline PG-TO252-3, dimensions in mm



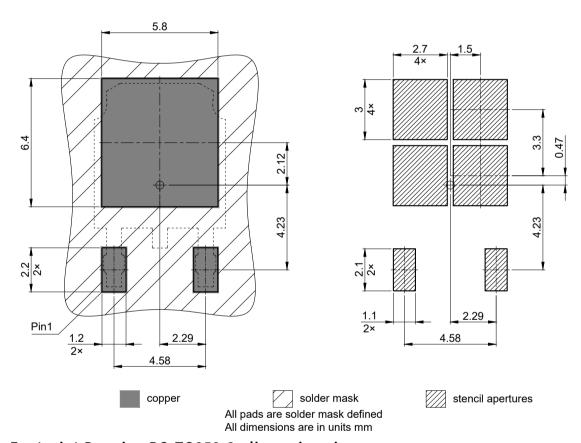


Figure 2 Footprint Drawing PG-TO252-3, dimensions in mm

StronglRFET™2 Power-Transistor, 40 V IPD023N04NF2S



Revision History

IPD023N04NF2S

Revision 2024-10-14, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-07-13	Release of final version
2.1	2022-09-20	updated Package outline drawing
2.2	2024-10-14	Added trr and Qrr at diF/dt=100 A/μs

Trademarks

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