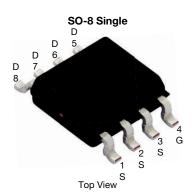
Vishay Siliconix

N-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	40					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0075					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0090					
Q _g typ. (nC)	21					
I _D (A) ^d	20.5					
Configuration	Single					

FEATURES

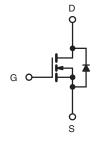
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN

FREE

APPLICATIONS

- Synchronous rectification
- DC/DC



N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free	Si4124DY-T1-E3			
Lead (Pb)-free and halogen-free	Si4124DY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	40	.,
Gate-source voltage		V _{GS}	±20	
	T _C = 25 °C		20.5	
0.01	T _C = 70 °C		16.4	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	13.6 ^{a, b}	┦ ,
	T _A = 70 °C		10.9 ^{a, b}	_ A
Pulsed drain current		I _{DM}	50	
Avalanche current	. 01	I _{AS}	33	
Avalanche energy	L = 0.1 mH	E _{AS}	54	mJ
Continuous source-drain diode current	T _C = 25 °C		4.7	_
	T _A = 25 °C	I _S	2.1 ^{a, b}	A
Maximum power dissipation	T _C = 25 °C		5.7	
	T _C = 70 °C	1 5	3.6	٠,,,
	T _A = 25 °C	P _D	2.5 ^{a, b}	W
	T _A = 70 °C	1	1.6 ^{a, b}	1
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient a, c	t ≤ 10 s	R_{thJA}	39	50	°C/W		
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	18	22]		

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. Maximum under steady state conditions is 85 °C/W
- d. Based on $T_C = 25$ °C



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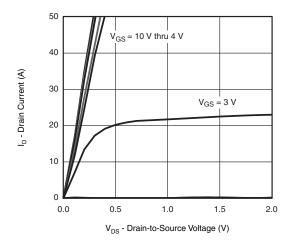
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•				
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	2/T		46	-	14/00	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$	-	-6.7	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	±100	nA	
Zana and a self-anni davida a senset	_	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μА	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5		
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50	-	-	Α	
		V _{GS} = 10 V, I _D = 14 A	-	0.0062	0.0075		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 12 \text{ A}$	-	0.0073	0.0090	Ω	
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 16 A	-	55	-	S	
Dynamic ^b		-					
Input capacitance	C _{iss}		-	3540	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		335	-		
Reverse transfer capacitance	C _{rss}		-	142	-		
Total gate charge	Qg	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 16 A -	51	77			
			-	21	32	nC	
Gate-source charge	Q _{qs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 16 \text{ A}$	-	10.7	-		
Gate-drain charge	Q _{ad}		-	3.0	-		
Gate resistance	R _a	f = 1 MHz	-	0.75	1.5	Ω	
Turn-on delay time	t _{d(on)}		-	30	45		
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$	-	14	21	1	
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		38	60		
Fall time	t _f		-	11	17		
Turn-on delay time	t _{d(on)}		-	14	21	ns	
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_1 = 2 \Omega$	-	10	15		
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	32	50		
Fall time	t _f		-	8	15		
Drain-Source Body Diode Characteristi	cs		•				
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	32		
Pulse diode forward current	I _{SM}		-	-	50	Α	
Body diode voltage	V _{SD}	$I_S = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	25	50	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	-	19	38	nC	
Reverse recovery fall time	t _a	$T_{J} = 25 ^{\circ}\text{C}$	-	13	-		
Reverse recovery rise time	t _b		_	12	-	ns	

Notes

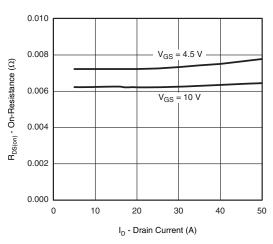
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

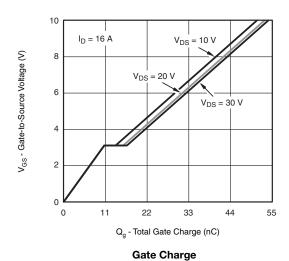


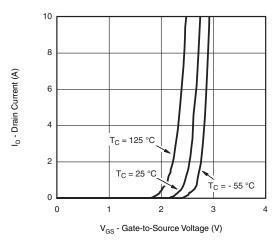


Output Characteristics

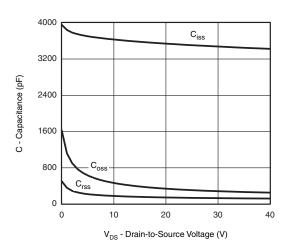


On-Resistance vs. Drain Current and Gate Voltage

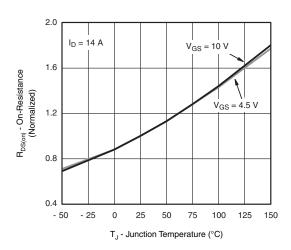




Transfer Characteristics

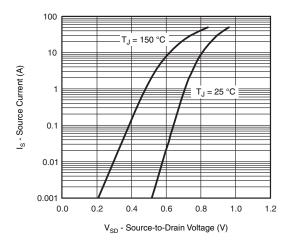


Capacitance

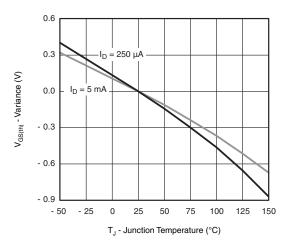


On-Resistance vs. Junction Temperature

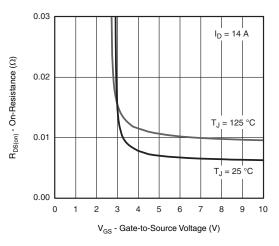




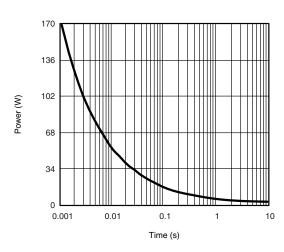
Source-Drain Diode Forward Voltage



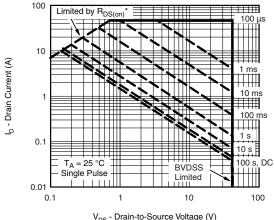
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



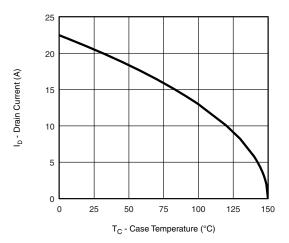
Single Pulse Power (Junction-to-Ambient)



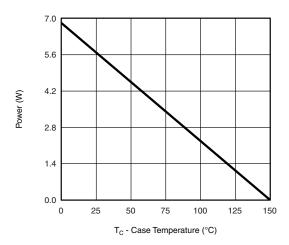
 $\rm V_{DS}$ - Drain-to-Source Voltage (V) * $\rm V_{DS}$ > minimum $\rm V_{GS}$ at which $\rm R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

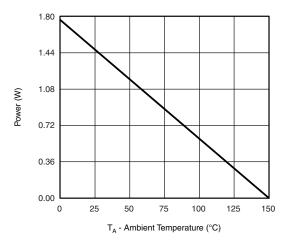




Current Derating a





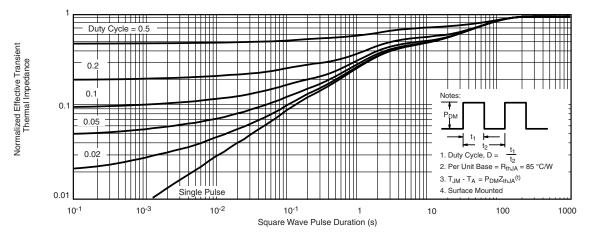


Power Derating, Junction-to-Ambient

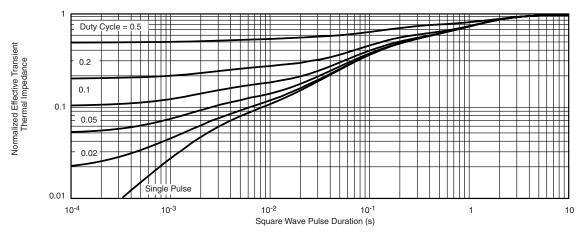
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68601.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

LON NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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