

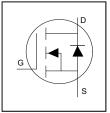
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

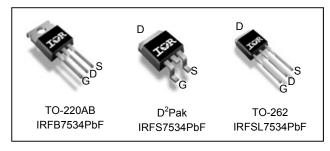
Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET



V _{DSS}	60V	
R _{DS(on)} typ.	$2.0 \text{m}\Omega$	
max	2.4mΩ	
D (Silicon Limited)	232A①	
I _{D (Package Limited)}	195A	



G	D	S	
Gate	Drain	Source	

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7534PbF	TO-220	Tube	50	IRFB7534PbF
IRFSL7534PbF	TO-262	Tube	50	IRFSL7534PbF
IDEC7534DbE	D ² -Pak	Tube	50	IRFS7534PbF
IRFS7534PbF	D-Pak	Tape and Reel Left	800	IRFS7534TRLPbF

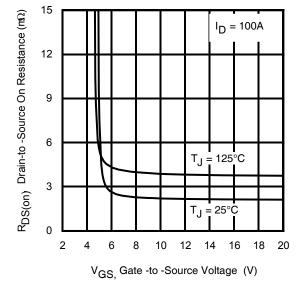


Fig 1. Typical On-Resistance vs. Gate Voltage

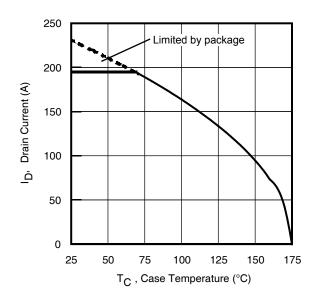


Fig 2. Maximum Drain Current vs. Case Temperature

2017-04-05



Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	232①	
$I_D @ T_C = 100^{\circ}C$ Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) $I_D @ T_C = 25^{\circ}C$ Continuous Drain Current, $V_{GS} @ 10V$ (Wire Bond Limited)		164	
		195	A
I _{DM}	Pulsed Drain Current ②	944*	
P _D @T _C = 25°C	Maximum Power Dissipation	294	W
	Linear Derating Factor	1.96	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

E _{AS (Thermally limited)}	Single Pulse Avalanche Energy ③	373	m l
E _{AS (Thermally limited)}	Single Pulse Avalanche Energy ®	775	mJ
I _{AR}	Avalanche Current ②	Coo Fig 15 16 220 22h	Α
E _{AR}	Repetitive Avalanche Energy ②	See Fig 15, 16, 23a, 23b	mJ

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ®		0.51	
$R_{ heta CS}$	Case-to-Sink, Flat Greased Surface	0.50		°C/\\
$R_{ heta JA}$	Junction-to-Ambient (TO-220)		62	°C/W
$R_{ heta JA}$	Junction-to-Ambient (PCB Mount) (D²-Pak)®		40	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		24		mV/°C	Reference to 25°C, I _D = 1mA ②
R _{DS(on)}	Static Drain-to-Source On-Resistance		2.0	2.4	m()	$V_{GS} = 10V, I_D = 100A$
			2.6		mΩ	$V_{GS} = 6.0V, I_D = 50A$
$V_{GS(th)}$	Gate Threshold Voltage	2.1		3.7	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
	Drain to Source Leakage Current			1.0		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
I _{DSS}	Drain-to-Source Leakage Current			150	μA	$V_{DS} = 60V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage			100	nΛ	$V_{GS} = 20V$
I _{GSS}	Gate-to-Source Reverse Leakage			-100	nA	$V_{GS} = -20V$
R_G	Gate Resistance		1.9		Ω	

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- \odot Limited by T_{Jmax}, starting T_J = 25°C, L = 75 μ H, R_G = 50 Ω , I_{AS} = 100A, V_{GS} =10V.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- $^{\circ}$ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- \odot C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- R_θ is measured at T_J approximately 90°C.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: http://www.irf.com/technical-info/appnotes/an-994.pdf
- ① Limited by T_{Jmax} , starting $T_J = 25$ °C, L = 1mH, $R_G = 50\Omega$, $I_{AS} = 39A$, $V_{GS} = 10V$.
- Pulse drain current is limited at 780A by source bonding technology.



Dynamic Electrical Characteristics @ $T_J = 25$ °C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
gfs	Forward Transconductance	498			S	$V_{DS} = 10V, I_{D} = 100A$
Q_g	Total Gate Charge		186	279		I _D = 100A
Q_{gs}	Gate-to-Source Charge		43		nC	$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain Charge		56		IIC	V _{GS} = 10V
Q _{sync}	Total Gate Charge Sync. (Qg- Qgd)		130			
$t_{d(on)}$	Turn-On Delay Time		20			$V_{DD} = 30V$
t _r	Rise Time		134			I _D = 100A
$t_{d(off)}$	Turn-Off Delay Time		118		ns	$R_G = 2.7\Omega$
t _f	Fall Time		93			V _{GS} = 10V⑤
C _{iss}	Input Capacitance		10034			V _{GS} = 0V
C _{oss}	Output Capacitance		921			V _{DS} = 25V
C_{rss}	Reverse Transfer Capacitance		594		pF	f = 1.0MHz, See Fig.7
Coss eff.(ER)	Effective Output Capacitance (Energy Related)		892] "	V _{GS} = 0V, VDS = 0V to 48V⑦
Coss eff.(TR)	Output Capacitance (Time Related)		1145			V _{GS} = 0V, VDS = 0V to 48V [©]

Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current (Body Diode)			232①		MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ②			944*		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 100A, V_{GS} = 0V $ §
dv/dt	Peak Diode Recovery dv/dt@		9.2		V/ns	$T_J = 175^{\circ}C, I_S = 100A, V_{DS} = 60V$
+	Boyona Booyany Timo		46		20	$T_J = 25^{\circ}C$ $V_{DD} = 51V$
t _{rr}	Reverse Recovery Time		49		ns	$T_J = 125^{\circ}C$ $I_F = 100A$,
0	Deverse Deservery Charge		71		20	<u>T_J = 25°C</u> di/dt = 100A/µs ⑤
Q_{rr}	Reverse Recovery Charge		83		nC	<u>T_J = 125°C</u>
I _{RRM}	Reverse Recovery Current		2.6		Α	T _J = 25°C



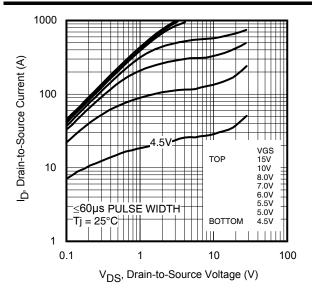


Fig 3. Typical Output Characteristics

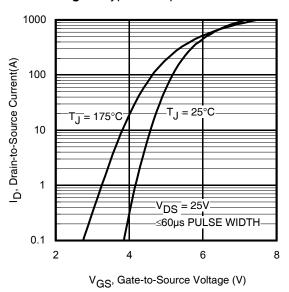


Fig 5. Typical Transfer Characteristics

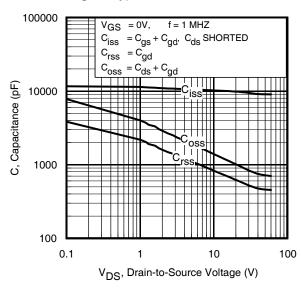


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

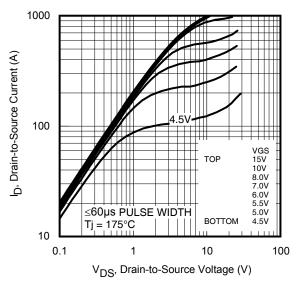


Fig 4. Typical Output Characteristics

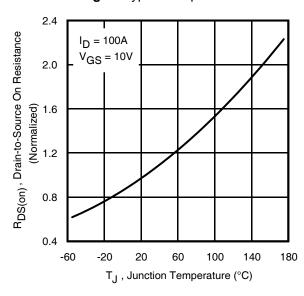


Fig 6. Normalized On-Resistance vs. Temperature

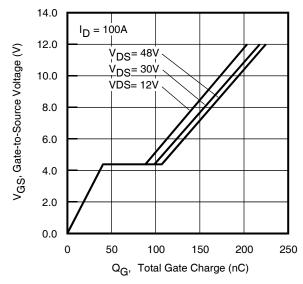


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage



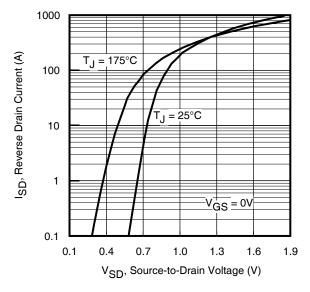


Fig 9. Typical Source-Drain Diode Forward Voltage

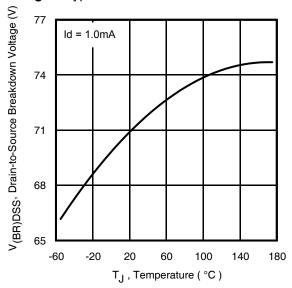


Fig 11. Drain-to-Source Breakdown Voltage

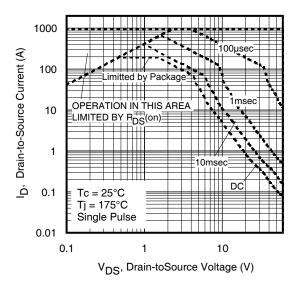


Fig 10. Maximum Safe Operating Area

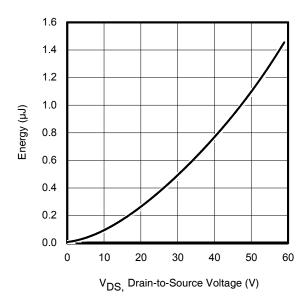


Fig 12. Typical Coss Stored Energy

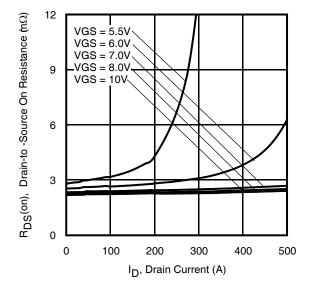


Fig 13. Typical On-Resistance vs. Drain Current



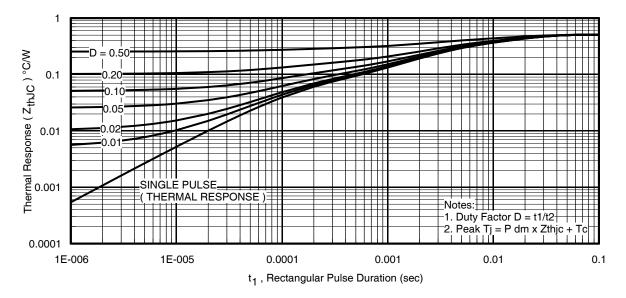


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

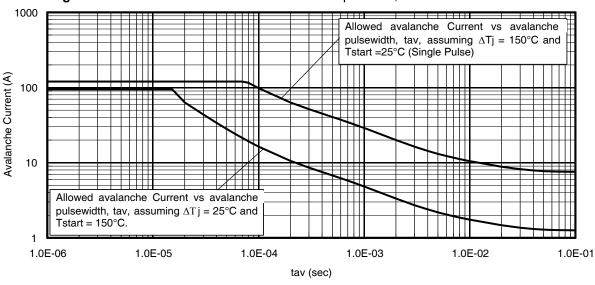


Fig 15. Avalanche Current vs. Pulse Width

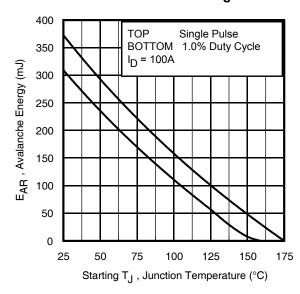


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:

Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.

- 2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
- 4. P_{D (ave)} = Average power dissipation per single avalanche pulse.
- 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I_{av} = Allowable avalanche current.
- ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

 t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14) PD (ave) = 1/2 (1.3·BV·I_{av}) = $\Delta T/Z_{thJC}$

 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

 $E_{AS (AR)} = P_{D (ave)} t_{av}$



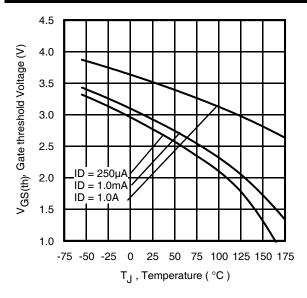


Fig 17. Threshold Voltage vs. Temperature

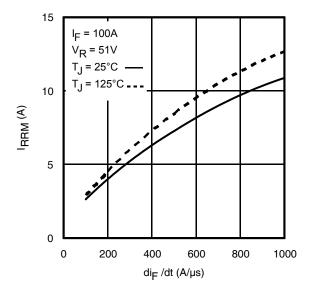


Fig 19. Typical Recovery Current vs. dif/dt

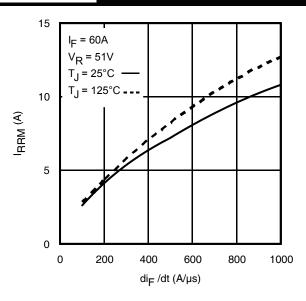


Fig 18. Typical Recovery Current vs. dif/dt

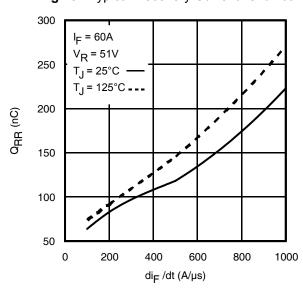


Fig 20. Typical Stored Charge vs. dif/dt

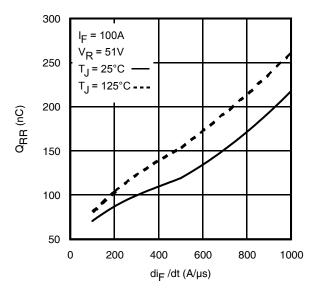


Fig 21. Typical Stored Charge vs. dif/dt



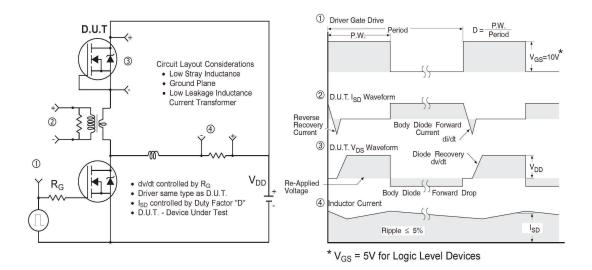


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

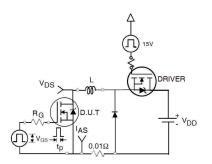


Fig 23a. Unclamped Inductive Test Circuit

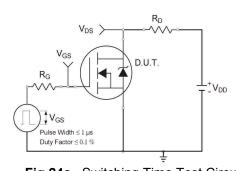


Fig 24a. Switching Time Test Circuit

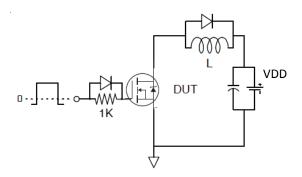


Fig 25a. Gate Charge Test Circuit

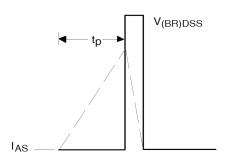


Fig 23b. Unclamped Inductive Waveforms

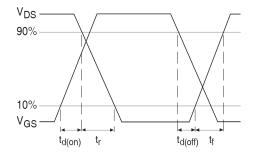


Fig 24b. Switching Time Waveforms

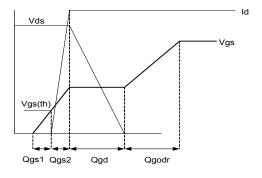
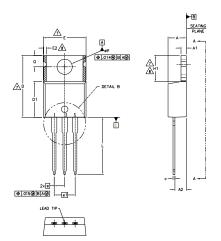


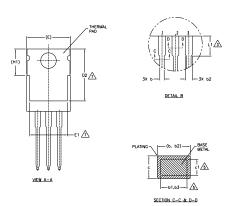
Fig 25b. Gate Charge Waveform

8



TO-220AB Package Outline (Dimensions are shown in millimeters (inches))





NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1
- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION 61, 63 & c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCHES.
- 7.-THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	MILLIM	ETERS	INC	HES	
	MIN.	MAX.	MIN.	MAX.	NOTES
Α	3.56	4.83	.140	.190	
A1	1,14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1,14	1.78	.045	.070	
b3	1,14	1.73	.045	.068	5
С	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
Ε	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	_	0.76	_	.030	8
e	2.54 BSC		.100	BSC	
e1	5.08	BSC	.200	BSC	
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØΡ	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

1.- GATE 2.- DRAIN 3.- SOURCE

IGBTs, CoPACK

1.- GATE 2.- COLLECTOR 3.- EMITTER

DIODES

1.- ANODE 2.- CATHODE 3.- ANODE

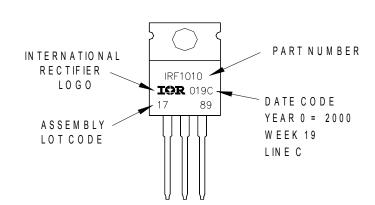
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010

LOT CODE 1789

ASSEMBLED ON WW 19,2000 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

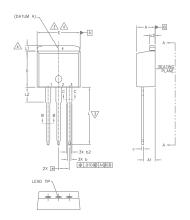


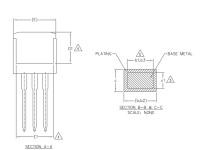
TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at http://www.irf.com/package/



TO-262 Package Outline (Dimensions are shown in millimeters (inches)





_							
	S		Ŋ				
	M B O	MILLIM	ETERS		INC	HES	O T E S
	O L	MIN.	MAX.	li	MIN.	MAX.	E S
İ	Α	4.06	4.83	li	.160	.190	
	A1	2.03	3.02		.080	.119	
	b	0.51	0.99		.020	.039	
	b1	0.51	0.89		.020	.035	5
	b2	1,14	1.78		.045	.070	
	ь3	1.14	1.73		.045	.068	5
ı	С	0.38	0.74		.015	.029	
ı	c1	0.38	0.58		.015	.023	5
ı	c2	1.14	1.65		.045	.065	
	D	8.38	9.65		.330	.380	3
	D1	6.86	-		.270	-	4
	Ε	9.65	10.67		.380	.420	3,4
	E1	6.22	-		.245		4
	е	2.54	BSC		.100 BSC		
	L	13.46	14.10		.530	.555	
	L1	-	1.65		-	.065	4
	L2	3.56	3.71		.140	.146	
				-			

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- 5. DIMENSION 61 AND c1 APPLY TO BASE METAL ONLY.
- 6. CONTROLLING DIMENSION: INCH.
- 7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(mox.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

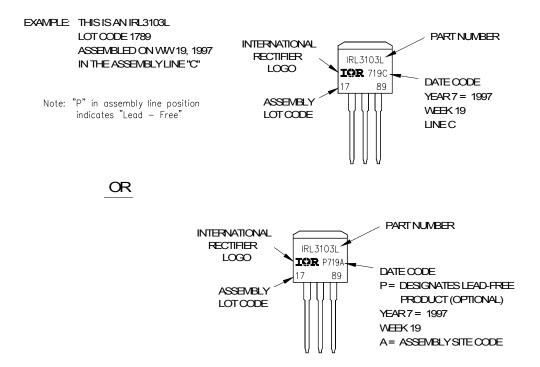
IGBTs, CoPACK

- 1.- GATE
 2.- COLLECTOR
 3 FMITTER
- 3.- EMITTER4.- COLLECTOR

HEXFET DIODES

- 1.- GATE 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- DRAIN 3.- SOURCE 2, 4.- CATHODE 3.- ANODE
- 4. DRAIN

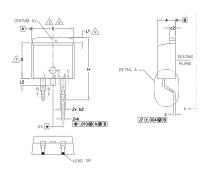
TO-262 Part Marking Information

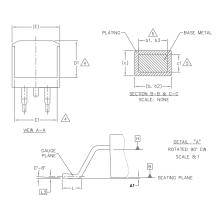


Note: For the most current drawing please refer to website at http://www.irf.com/package/



D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))





S Y M	DIMENSIONS					
В	MILLIM	MILLIMETERS INCHES				
O L	MIN.	MAX.	MIN.	MAX.	O T E S	
Α	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039		
ь1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1,14	1.73	.045	.068	5	
С	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1,14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	-	.270	_	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	-	.245	-	4	
е	2.54	BSC	.100 BSC			
Н	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
L1	_	1.68	-	.066	4	
L2	-	1.78	-	.070		
L3	0.25	5 BSC .010 BSC				

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION 61, 63 AND c1 APPLY TO BASE METAL ONLY.

- 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 7. CONTROLLING DIMENSION: INCH.
- 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

LEAD ASSIGNMENTS

1.- ANODE (TWO DIE) / OPEN (ONE DIE) 2, 4.- CATHODE

3.- ANODE

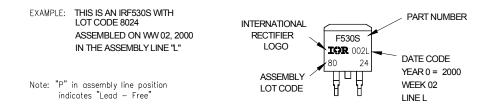
HEXFET

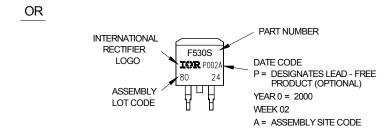
IGBTs, CoPACK

1.- GATE 2, 4.- DRAIN 3.- SOURCE

1.- GATE 2, 4.- COLLECTOR 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information



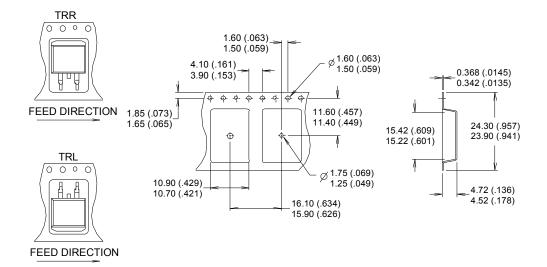


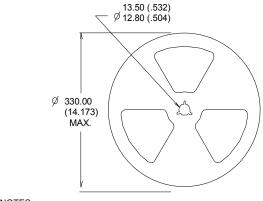
Note: For the most current drawing please refer to website at http://www.irf.com/package/

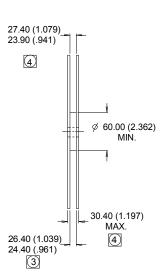
11 2017-04-05



D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))







- NOTES:
- COMFORMS TO EIA-418.
 CONTROLLING DIMENSION: MILLIMETER.
- (3) (4) DIMENSION MEASURED @ HUB.
 INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to website at http://www.irf.com/package/

12 2017-04-05



Qualification Information

Qualification Level	Industrial		
	(per JEDEC JESD47F) †		
Moisture Sensitivity Level	TO-220	N/A	
	D ² Pak	MSL1	
	TO-262	N/A	
RoHS Compliant		Yes	

[†] Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments	
11/5/2014	 Updated E_{AS (L =1mH)} = 775mJ on page 2 Updated note 10 "Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 39A, V_{GS} =10V". on page 2 Updated package outline on page 9,10,11. 	
04/05/2017	 Changed datasheet with Infineon logo - all pages. Added disclaimer on last page. Modify Fig 10 on page 5. 	

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