



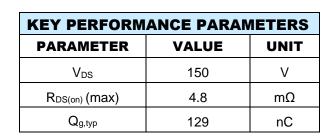
# **N-Channel Power MOSFET**

#### **FEATURES**

- Excellent FOM
- Reliability meets AEC-Q101 requirements
- 100% UIS & Rg tested
- Ultra low rdson
- RoHS compliant
- Halogen-free

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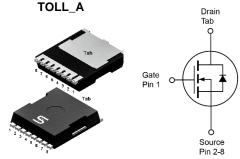
- Solenoid and motor drivers
- DC-DC converters
- Load Switch
- SMPS











Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	150	V	
Gate-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Drain Correct	$T_C = 25^{\circ}C$		224		
Continuous Drain Current	T <sub>C</sub> = 100°C	l <sub>D</sub>	158	A	
Pulsed Drain Current (Note 1)		I <sub>DM</sub>	896	А	
Total Dawer Dissipation	$T_C = 25^{\circ}C$	D	600	10/	
Total Power Dissipation	Tc = 100°C	P <sub>D</sub>	300	W	
Single Pulse Avalanche Energy (Note 2)		E <sub>AS</sub>	1164	mJ	
Single Pulse Avalanche Current (Note 2)		I <sub>AS</sub>	27.8	Α	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	- 55 to +175	°C	

THERMAL PERFORMANCE					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction to Case Thermal Resistance	Rejc	0.25	°C/W		
Junction to Ambient Thermal Resistance (Note 3)	RөJA	69	°C/W		

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#### Notes:

- 1. Pulse Width ≤ 100µs.
- 2. L = 3mH,  $R_G = 25\Omega$ , Starting  $T_J = 25$ °C.
- 3. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.



PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	150			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V <sub>GS(TH)</sub>	2.2	3.3	4.1	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>			1	μA
Drain-Source On-State Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	R <sub>DS(on)</sub>		3.7	4.8	mΩ
Dynamic (Note 5)						
Total Gate Charge		Qg		129		
Gate-Source Charge	$V_{DS} = 75V, I_D = 20A,$ $V_{GS} = 10V$	Qgs		45		nC
Gate-Drain Charge	VGS = 10V	Q <sub>gd</sub>		25		1
Input Capacitance	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V, f = 1.0MHz	Ciss		9924		
Output Capacitance		Coss		769		pF
Reverse Transfer Capacitance	7 I = 1.0IVID2	Crss		34		
Gate Resistance	f = 1.0MHz	Rg		2.8		Ω
Switching (Note 6)						
Turn-On Delay Time		t <sub>d(on)</sub>		28		
Turn-On Rise Time	$V_{DD} = 75V$ , $R_G = 3\Omega$ ,	tr		57		
Turn-Off Delay Time	$I_D = 20A, V_{GS} = 10V$	t <sub>d(off)</sub>		78		ns
Turn-Off Fall Time		t <sub>f</sub>		37		
Source-Drain Diode						
Forward Voltage (Note 4)	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	V <sub>SD</sub>			1.2	V
Reverse Recovery Time	Is = 20A	t <sub>rr</sub>		114		ns
Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs	Qrr		557		nC

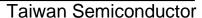
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#### Notes:

- 4. Pulse test: Pulse Width  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%.
- 5. Defined by design. Not subject to production test.
- 6. Switching time is essentially independent of operating temperature.

# **ORDERING INFORMATION**

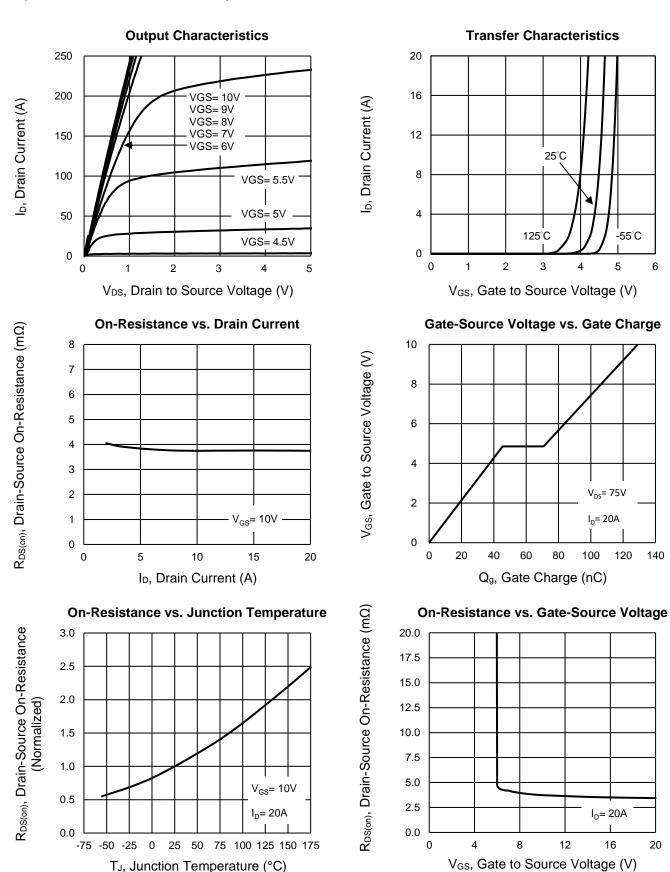
ORDERING CODE	PACKAGE	PACKING
TSM048NM15TL RAG	TOLL_A	2000pcs / 13" Reel





#### **CHARACTERISTICS CURVES**

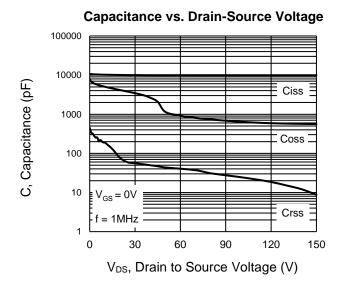
 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$ 

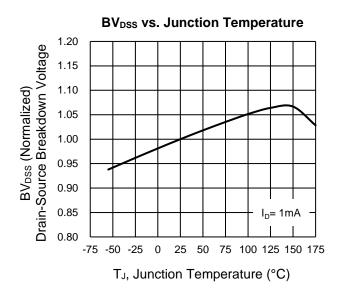




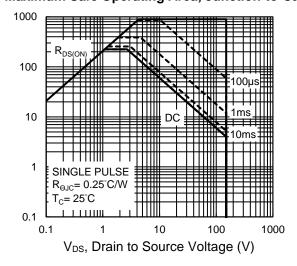
#### **CHARACTERISTICS CURVES**

(T<sub>A</sub> = 25°C unless otherwise noted)





# Maximum Safe Operating Area, Junction-to-Case

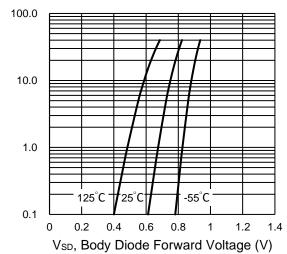


lp, Drain Current (A)

Normalized Effective Transient

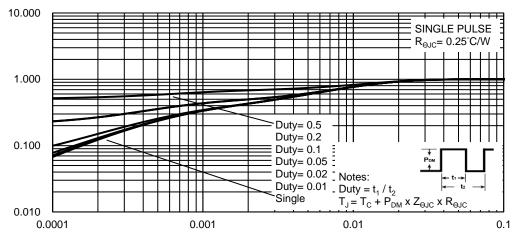
Thermal Impedance, Zeuc

#### Source-Drain Diode Forward Current vs. Voltage



# Normalized Thermal Transient Impedance, Junction-to-Case

Reverse Drain Current (A)



t, Square Wave Pulse Duration (sec)

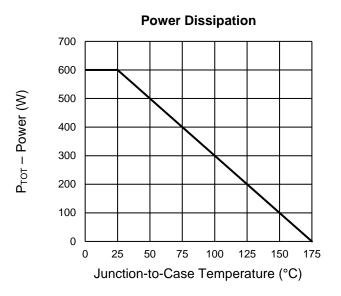
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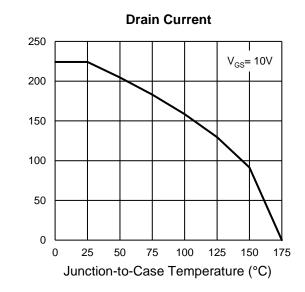




# **CHARACTERISTICS CURVES**

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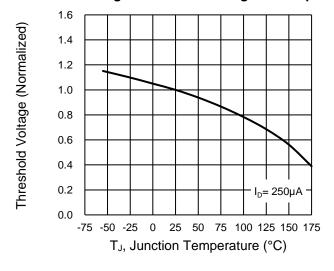




Ip-Drain Current (A)

5

## Normalized gate threshold voltage vs Temperature

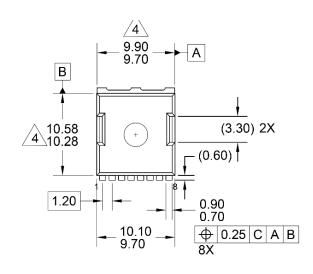


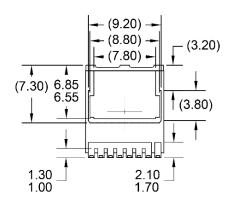


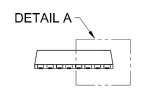


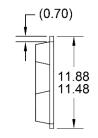
#### PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

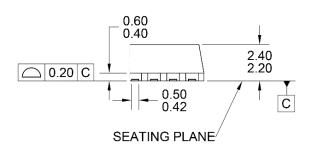
#### TOLL\_A







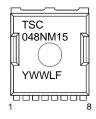




8.10 2.40 13.30 0.80 - 1.20

DETAIL A (SCALE 2:1)

SUGGESTED PAD LAYOUT



# MARKING DIAGRAM

048NM15 = Device marking

Y = Year Code

WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

#### NOTES: UNLESS OTHERWISE SPECIFIED

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. THE PACKAGE OUTLINE REFERENCE: JEDEC MO-299B, ISSUE B.
- MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
  - 5. DWG NO. REF: HQ2SD07-TOLL-141 REV A.



Taiwan Semiconductor

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