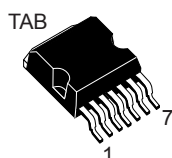
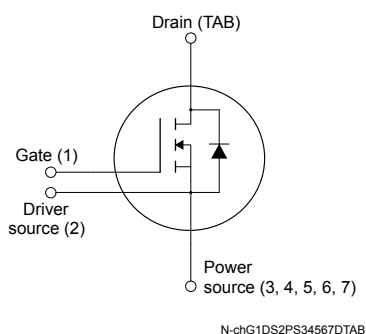


## Automotive-grade N-channel 650 V, 38 mΩ typ., 51 A MDmesh DM9 Power MOSFET in an H<sup>2</sup>PAK-7 package



H<sup>2</sup>PAK-7



### Product status link


[STH65N050DM9-7AG](#)

### Product summary

Order code	STH65N050DM9-7AG
Marking	65A050DM9
Package	H <sup>2</sup> PAK-7
Packing	Tape and reel

## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH65N050DM9-7AG	650 V	50 mΩ	51 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Very low FOM (R<sub>DS(on)</sub> · Q<sub>g</sub>)
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Excellent switching performance thanks to the extra driving source pin

## Applications

- DC/DC converter for EV/HEV
- On board charger (OBC)

## Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R<sub>DS(on)</sub> per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q<sub>rr</sub>), time (t<sub>rr</sub>) and R<sub>DS(on)</sub> makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	51	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	32	
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	266	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1000	A/ $\mu$ s
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	120	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 25.5\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
4.  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.47	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	760	mJ

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 4. On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$			5	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 25.5\text{ A}$		38	50	m $\Omega$

**Table 5. Dynamic characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$ , $V_{GS} = 0\text{ V}$	-	4680	-	pF
$C_{oss}$	Output capacitance		-	76	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$ , $V_{GS} = 0\text{ V}$	-	1070	-	pF
$R_g$	Intrinsic gate resistance	$f = 250\text{ kHz}$ , open drain	-	1	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}$ , $I_D = 25.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	100	-	nC
$Q_{gs}$	Gate-source charge		-	26	-	nC
$Q_{gd}$	Gate-drain charge		-	36	-	nC

1.  $C_{oss\text{ eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to stated value.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 25.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	29	-	ns
$t_r$	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	80	-	ns
$t_f$	Fall time		-	5	-	ns

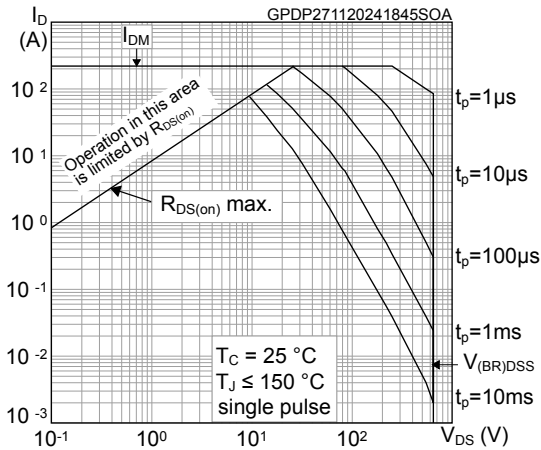
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		51	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 51\text{ A}$	-	1.1	1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 51\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 150\text{ V}$	-	170		ns
$Q_{rr}$	Reverse recovery charge		-	1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 51\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 150\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	225		ns
$Q_{rr}$	Reverse recovery charge		-	2.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A

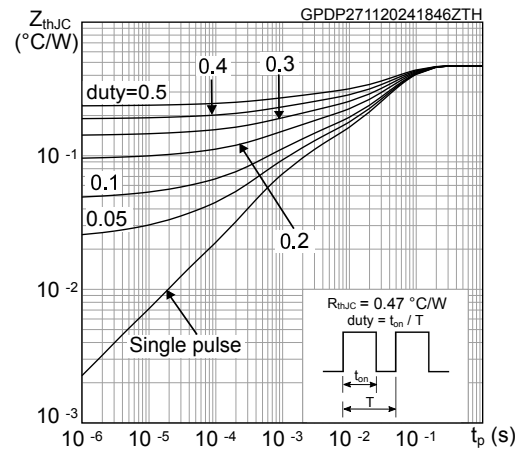
1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

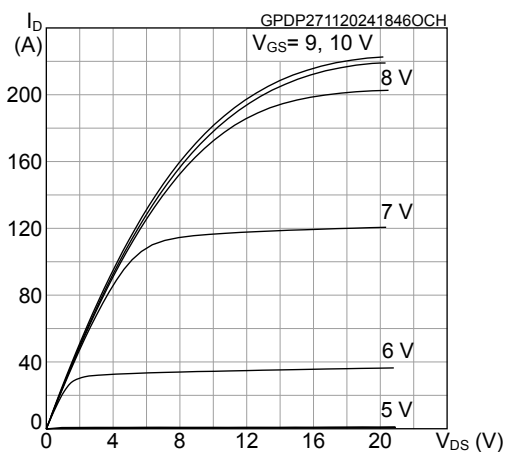
**Figure 1. Safe operating area**



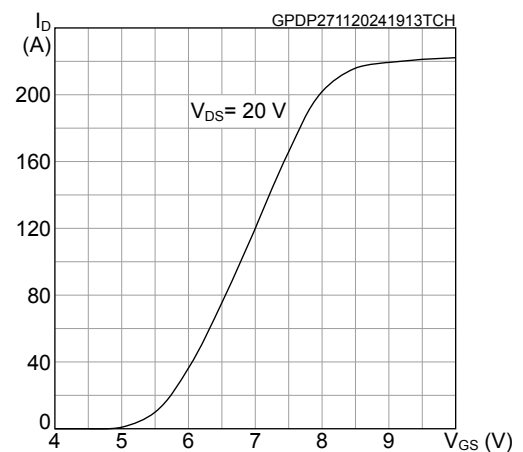
**Figure 2. Maximum transient thermal impedance**



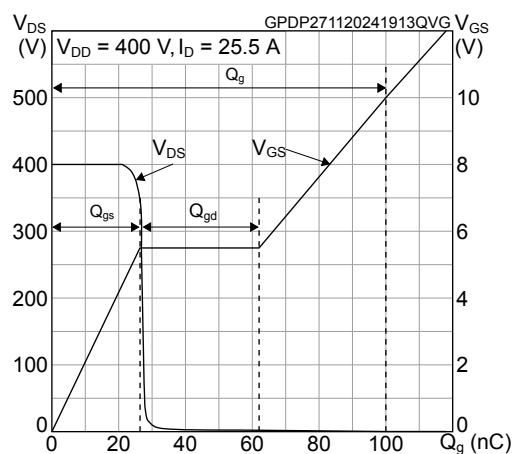
**Figure 3. Typical output characteristics**



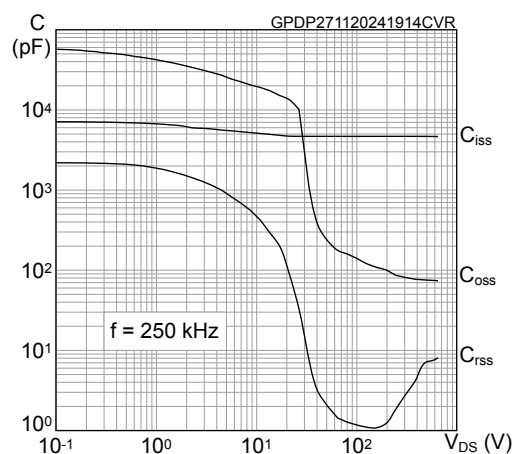
**Figure 4. Typical transfer characteristics**



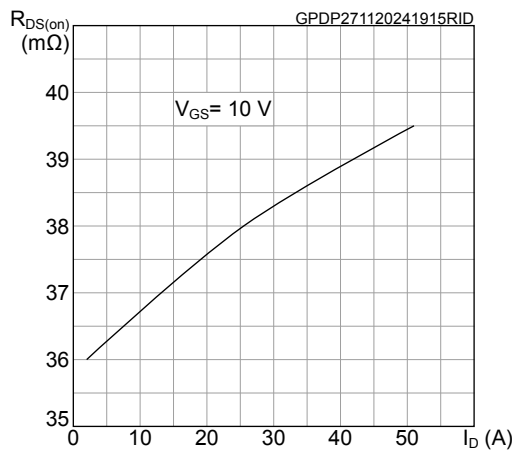
**Figure 5. Typical gate charge characteristics**



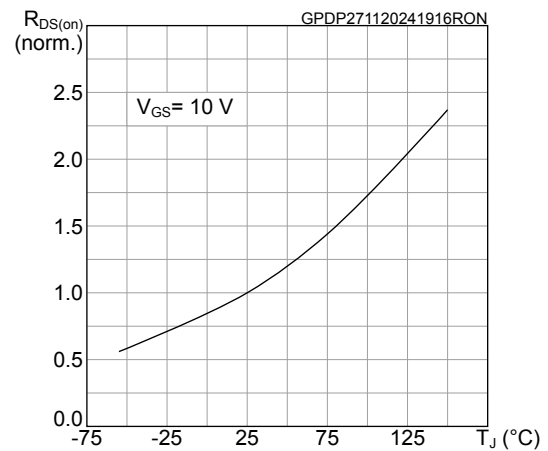
**Figure 6. Typical capacitance characteristics**



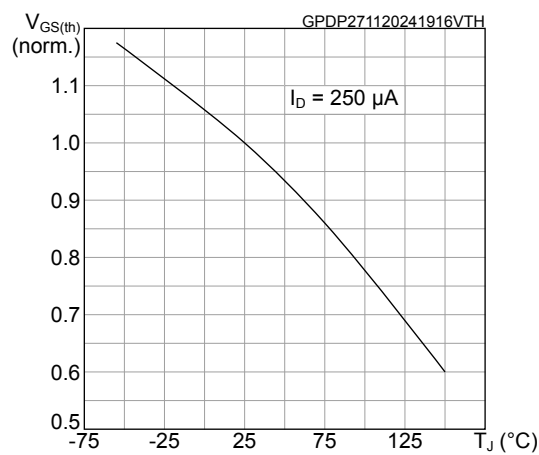
**Figure 7. Typical drain-source on-resistance**



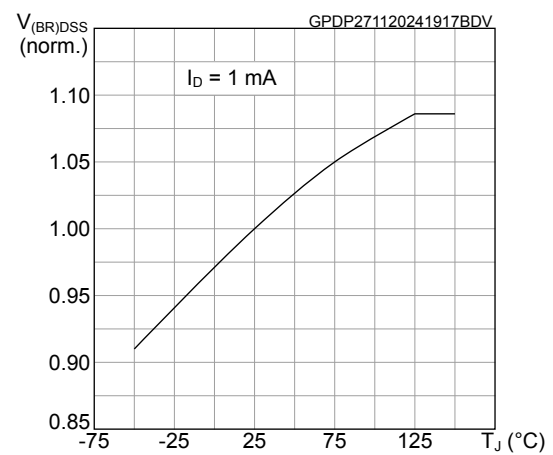
**Figure 8. Normalized on-resistance vs temperature**



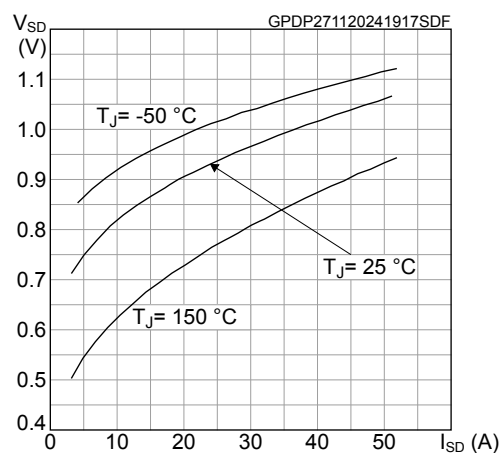
**Figure 9. Normalized gate threshold vs temperature**



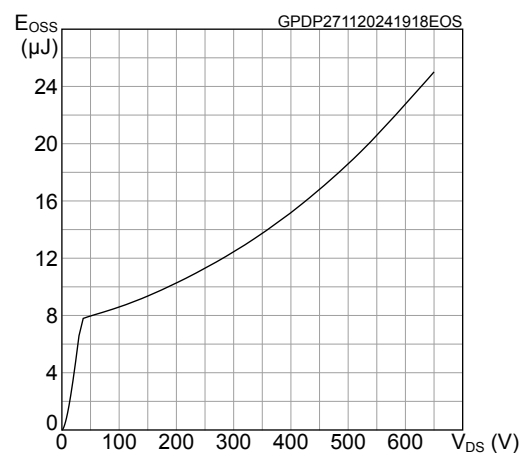
**Figure 10. Normalized breakdown voltage vs temperature**



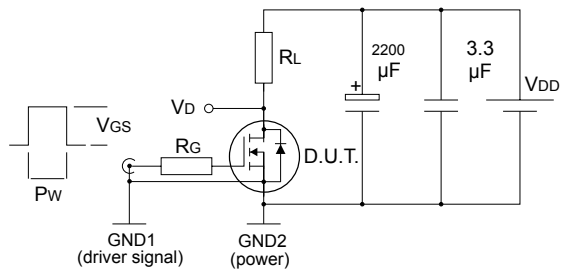
**Figure 11. Typical reverse diode forward characteristics**



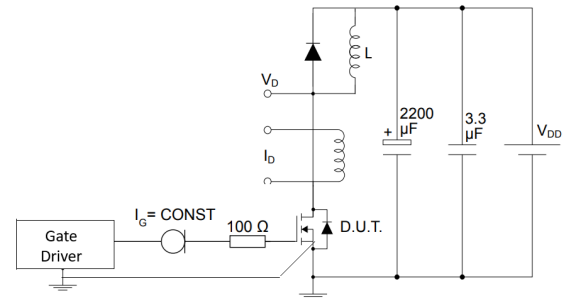
**Figure 12. Typical output capacitance stored energy**



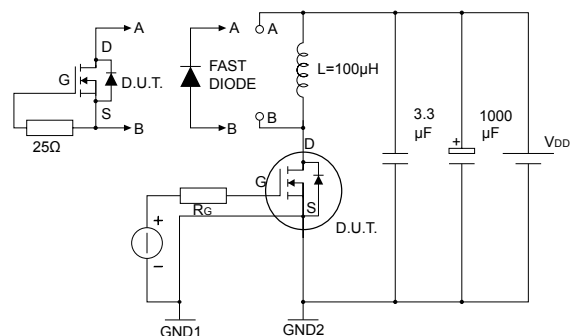
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


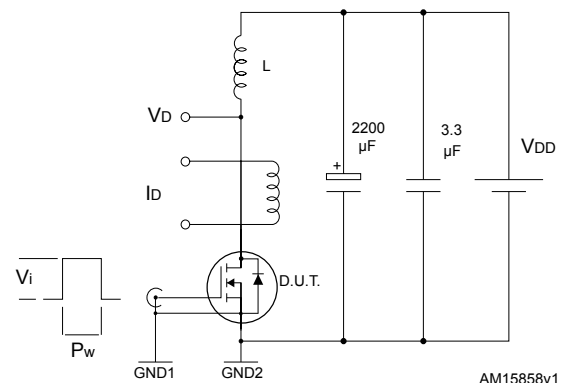
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


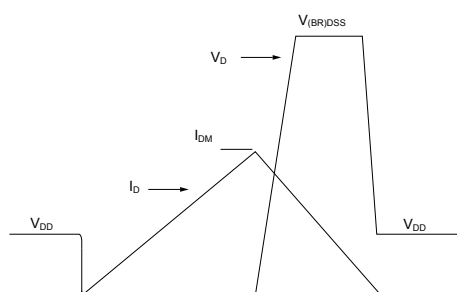
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


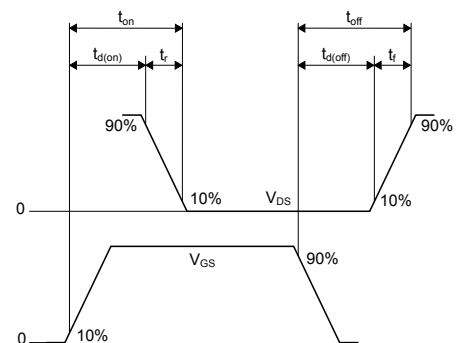
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


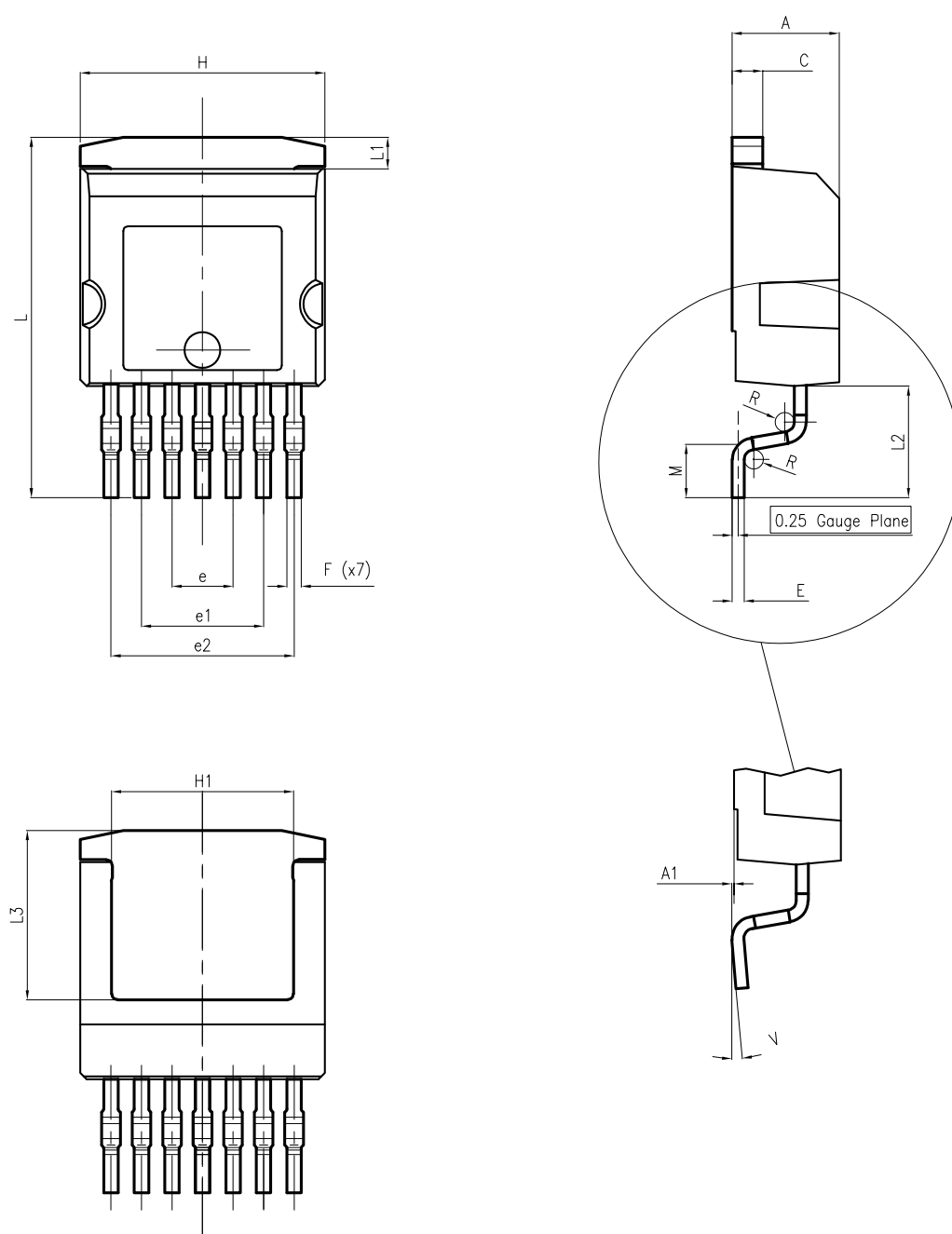
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 H<sup>2</sup>PAK-7 package information

Figure 19. H<sup>2</sup>PAK-7 package outline

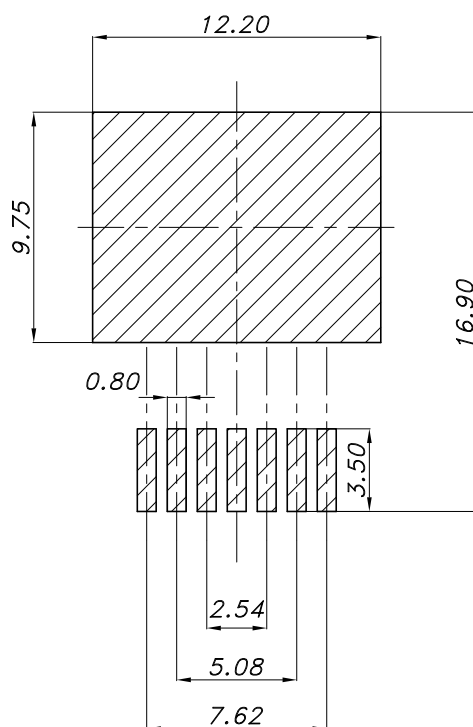


DM00249216\_6



**Table 8. H<sup>2</sup>PAK-7 package mechanical data**

Dim.	mm	
	Min.	Max.
A	4.30	4.80
A1	0.03	0.20
C	1.17	1.37
e	2.34	2.74
e1	4.88	5.28
e2	7.42	7.82
E	0.45	0.60
F	0.50	0.70
H	10.00	10.40
H1	7.40	8.00
L	14.75	15.25
L1	1.27	1.40
L2	4.35	4.95
L3	6.85	7.25
M	1.90	2.50
R	0.20	0.60
V	0°	8°

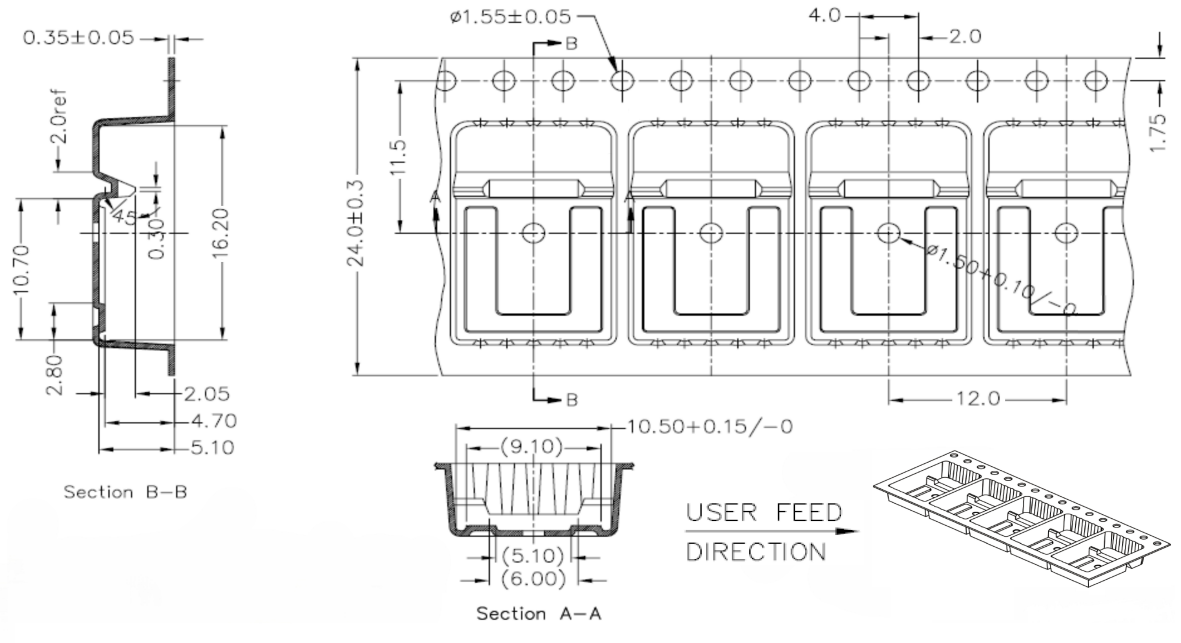
**Figure 20. H<sup>2</sup>PAK-7 recommended footprint**


footprint\_DM00249216\_6

**Note:** Dimensions are in mm.

## 4.2 H<sup>2</sup>PAK-7 packing information

Figure 21. H<sup>2</sup>PAK-7 tape drawing (dimensions are in mm)



DM01095771\_2

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Jun-2024	1	First release.
01-Oct-2024	2	Modified $R_{DS(on)}$ value in <i>Table 3. On/off-states</i> .
28-Nov-2024	3	Updated <i>Features</i> on cover page. Added <i>Table 3. Avalanche characteristics</i> . Updated <i>Table 5. Dynamic characteristics</i> , <i>Table 6. Switching times</i> and <i>Table 7. Source-drain diode</i> . Updated <i>Section 2.1: Electrical characteristics (curves)</i> . Updated <i>Section 3: Test circuits</i> . Minor text changes.
28-Jan-2025	4	Updated <i>Applications</i> . Updated <i>Figure 10. Normalized breakdown voltage vs temperature</i> .
19-Aug-2025	5	Updated <i>Section 4.2: H<sup>2</sup>PAK-7</i> packing information.

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