STL58N3LLH5



Automotive-grade N-channel 30 V, 0.0076 Ω typ., 56 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet — production data

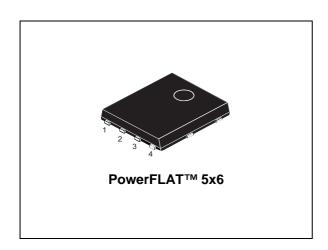
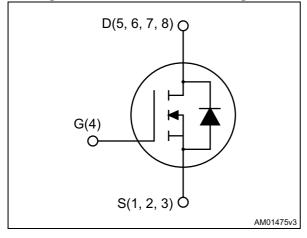


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	R _{DS(on)} max	I _D
STL58N3LLH5	30 V	0.009 Ω	56 A

- Designed for automotive applications and AEC-Q101 qualified
- Low on-resistance
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL58N3LLH5	58N3LH5	PowerFLAT™ 5x6	Tape and reel

Contents STL58N3LLH5

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STL58N3LLH5 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	30	V
V _{GS}	Gate-source voltage	+22 / -20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	64	А
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	45	А
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 25 °C	16	А
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} =100°C	11.5	А
I _{DM} ⁽¹⁾⁽³⁾	Drain current (pulsed)	224	А
I _{DM} ⁽²⁾⁽³⁾	Drain current (pulsed)	75	Α
P _{TOT} (1)	Total dissipation at T _C = 25°C	62.5	W
P _{TOT} (2)	Total dissipation at T _{pcb} = 25°C	4.8	W
E _{AS} ⁽⁴⁾	Single pulse avalanche energy	150	mJ
T _J	Operating junction temperature	-55 to 175	°C
T _{stg}	Storage temperature	00 10 170	

- 1. The value is rated according to R_{thj-c}
- 2. The value is rated according to $R_{\mbox{\scriptsize thj-pcb}}$
- 3. Pulse width limited by safe operating area
- 4. Starting $T_j = 25$ °C, $I_D = 56$ A, $V_{DD} = 50$ V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

Electrical characteristics STL58N3LLH5

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
	Zoro goto voltago drois	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V},$			1	μΑ
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0 V$ $V_{DS} = 30 V, T_{C} = 125 °C$			10	μΑ
I _{GSS}	Gate body leakage current	$V_{DS} = 0 \text{ V},$ $V_{GS} = +22 / -20 \text{ V}$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		2.5	V
Static drain-sou	Static drain-source	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$		0.0076	0.009	Ω
R _{DS(on)}	on- resistance	$V_{GS} = 4.5 \text{ V}, I_D = 7.5 \text{ A}$		0.0099	0.0112	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	950		pF
C _{oss}	Output capacitance	V _{DS} =2 5 V, f = 1 MHz,	-	193		pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0 V$	-	27		pF
Q_g	Total gate charge	V _{DD} = 15 V, I _D = 15 A,	-	6.5	10	nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V (see Figure 14)	-	3.3		nC
Q _{gd}	Gate-drain charge		-	2.4		nC
R_{g}	Gate input resistance	f = 1 MHz, gate DC Bias = 0, test signal level = 20 mV, I _D = 0 A	-	1.7	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time		-	10.8	-	ns
t _r	Rise time	$V_{DD} = 15 \text{ V}, I_{D} = 7.5 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	15.6	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13)	-	14.2	-	ns
t _f	Fall time		-	6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current		-		56	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		224	Α
V _{SD} ⁽²⁾	Forward on voltage $I_{SD} = 15 \text{ A}, V_{GS} = 0 \text{ V}$		-		1.1	V
t _{rr}	Reverse recovery time	I _{SD} = 15 A,	-	20	36	ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs, V _{DD} = 25 V,	-	10	18	nC
I _{RRM}	Reverse recovery current	T _J = 150 °C	-	1		Α

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration= $300 \mu s$, duty cycle 1.5%

Electrical characteristics STL58N3LLH5

Electrical characteristics (curves) 2.1

Figure 2. Safe operating area

Figure 3. Thermal impedance

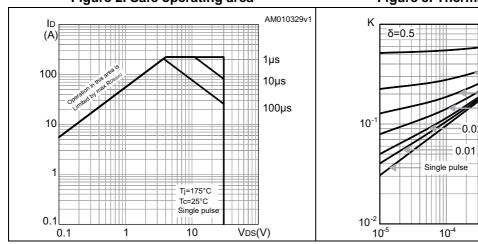


Figure 4. Output characteristics

Figure 5. Transfer characteristics

0.02

 $Z_{th} = k R_{thJ-c}$

 $\delta = t_{\rm p}/\tau$

10⁻³

GIPG230720141152S

tp(s)

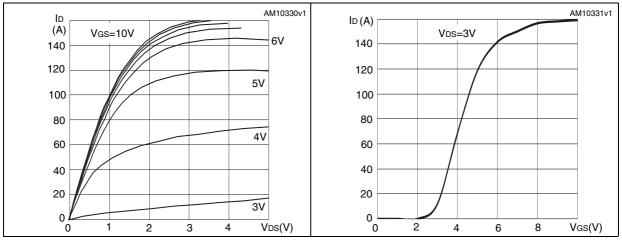
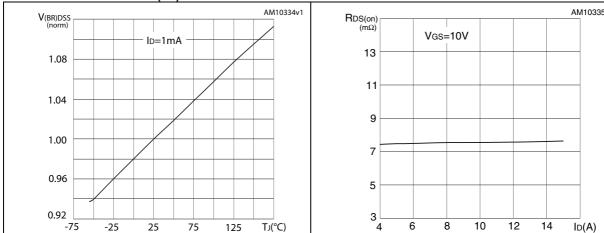


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance



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Figure 8. Gate charge vs gate-source voltage

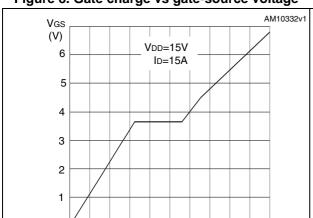


Figure 9. Capacitance variations

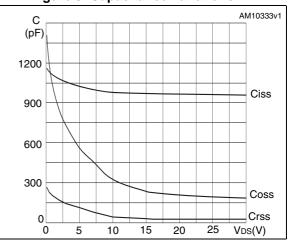


Figure 10. Normalized gate threshold voltage vs temperature

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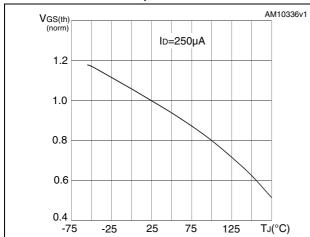
6

8

Q_g(nC)

2

Figure 11. Normalized on-resistance vs temperature



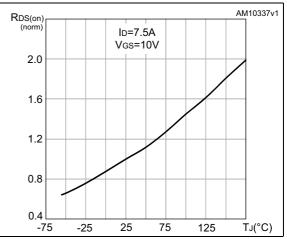
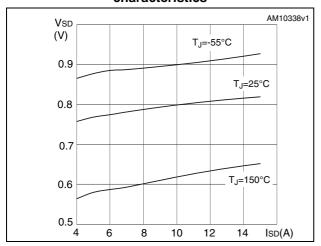


Figure 12. Source-drain diode forward characteristics



Test circuits STL58N3LLH5

3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

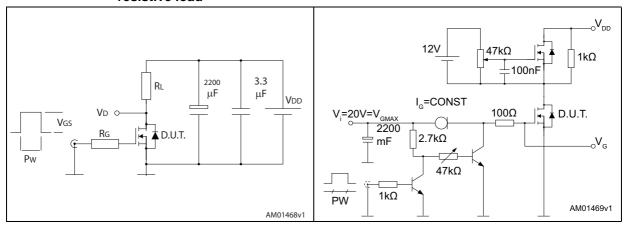


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

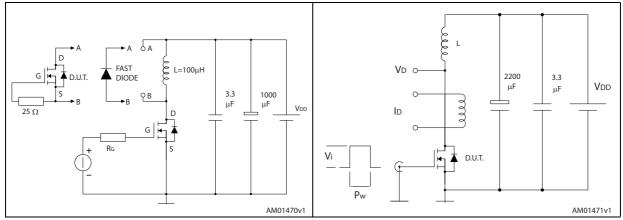
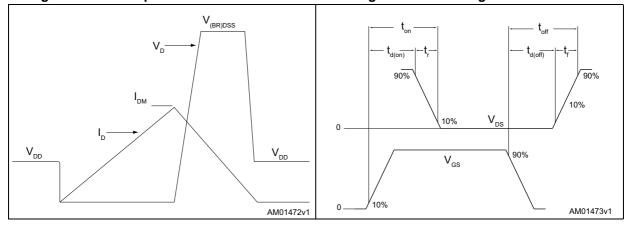


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



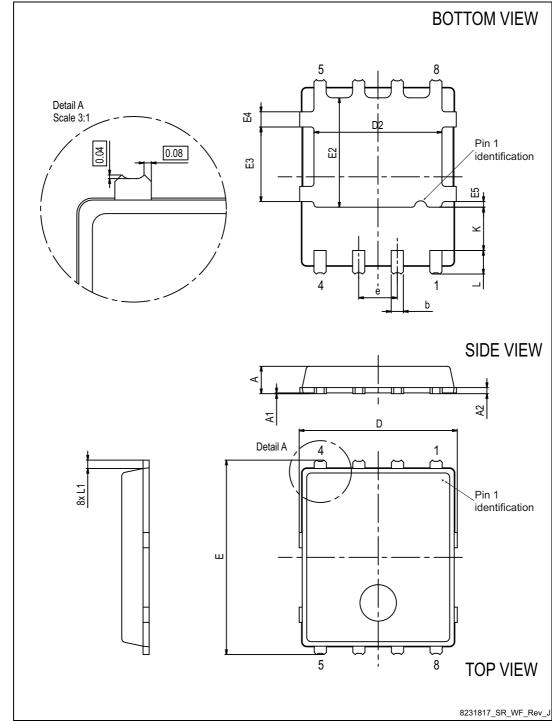


Figure 19. PowerFLAT™ 5x6 WF type S-R drawing



Table 8. PowerFLAT™ 5x6 WF type S-R mechanical data

Dim.		mm	
Diin.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
L	0.70		0.90
L1		0.275	
К	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28



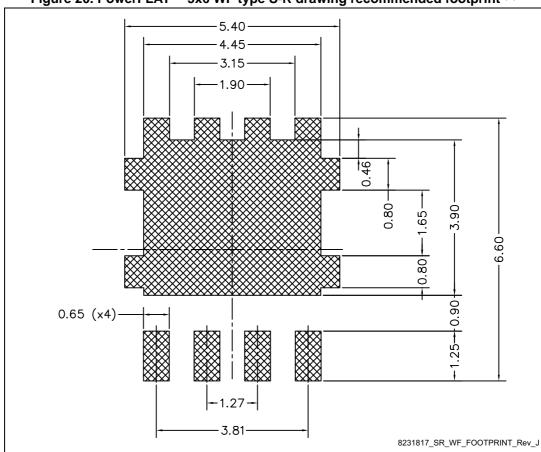


Figure 20. PowerFLAT™ 5x6 WF type S-R drawing recommended footprint ^(a)

a. All dimensions are in mm.

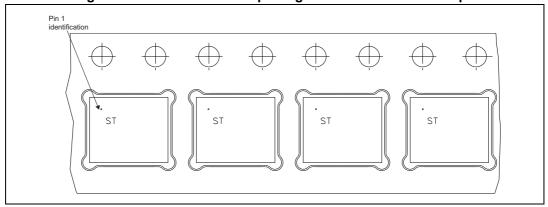
8234350_TapeWF_rev_C

5 Packaging mechanical data

P2 2.0±0.05(I) Po 4.0±0.1(II) Do E1 1.75±0.1 T 0.30±0.05 Ø 1.50 0.0 Ø1.50MIN Ao(6.70±0.1) Ko (1.20±0.1) P1(8.00±0.1) SECTION Y-Y (I) Measured from centreline of sprocket hole to centreline of pocket.
Cumulative tolerance of 10 sprocket (II) Base and bulk quantity 3000 pcs holes is ± 0.20 . Measured from centreline of sprocket hole to centreline of pocket.

Figure 21. PowerFLAT™ 5x6 type R-WF tape^(b)

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



b. All dimensions are in millimeters.



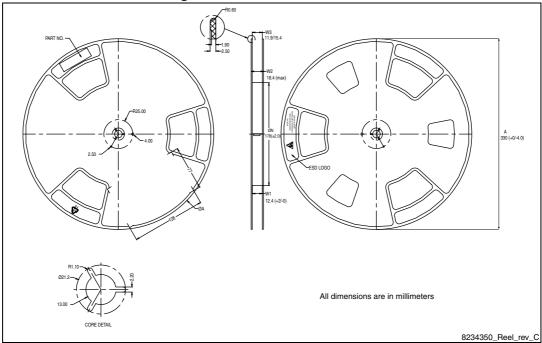


Figure 23. PowerFLAT™ 5x6 reel



STL58N3LLH5 Revision history

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
04-Aug-2014	1	First release.
15-Dec-2014	2	Text edits throughout document. On cover page: Updated title, features and description Updated Table 2: Absolute maximum ratings Updated Figure 19: PowerFLAT™ 5x6 WF type S-R drawing

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