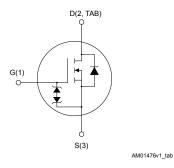




## Automotive-grade N-channel 600 V, 37 mΩ typ., 66 A MDmesh DM2 Power MOSFET in a TO-247 long leads package

TO-247 long leads



#### **Features**

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STWA72N60DM2AG	600 V	42 mΩ	66 A

- AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## **Applications**

Switching applications



This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.



#### Product status link

STWA72N60DM2AG

Product summary			
Order code STWA72N60DM2AG			
Marking	72N60DM2		
Package TO-247 long leads			
Packing	Tube		



# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
1-	Drain current (continuous) at T <sub>C</sub> = 25 °C	66	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	42	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	220	Α
P <sub>TOT</sub>	Total dissipation at T <sub>case</sub> = 25 °C	446	W
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	50	V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50	V/ns
T <sub>stg</sub>	Storage temperature range	-55 to 150	°C
T <sub>J</sub>	Operating junction temperature range	-55 (0 150	°C

- 1. Pulse width is limited by safe operating area.
- 2.  $I_{SD} \le 66$  A,  $V_{DS}$  (peak) <  $V_{(BR)DSS}$ , di/dt = 800 A/ $\mu$ s,  $V_{DD} = 480$  V.
- 3.  $V_{DS} \le 480 \text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thJC</sub>	Thermal resistance, junction-to-case	0.28	°C/W
R <sub>thJA</sub>	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>J</sub> max.)	8	Α
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 50$ V)	1500	mJ

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## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. Static** 

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			10	
I <sub>DSS</sub>	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_C = 125 ^{\circ}\text{C}^{(1)}$			100	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±5	μA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 33 A		37	42	mΩ

<sup>1.</sup> Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	5508	-	pF
C <sub>oss</sub>	Output capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	241	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	2.8	-	pF
C <sub>oss eq.</sub> (1)	Equivalent output capacitance	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0 V	-	470	-	pF
R <sub>g</sub>	Intrinsic gate resistance	f = 1 MHz open drain	-	2	-	Ω
Qg	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 66 A,	-	121	-	nC
$Q_{gs}$	Gate-source charge	V <sub>GS</sub> = 0 to 10 V	-	26	-	nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	61	-	nC

<sup>1.</sup>  $C_{\text{oss eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 33 A,	-	32	-	ns
t <sub>r</sub>	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$	-	67	-	ns
t <sub>d(off)</sub>	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	112	-	ns
t <sub>f</sub>	Fall time	resistive load switching times and Figure 18. Switching time waveform)	-	10.4	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		66	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		220	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 66 A	-		1.6	V
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 66 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	150		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 480 V	-	0.75		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.5		Α
t <sub>rr</sub>	Reverse recovery time	$I_{SD}$ = 66 A, di/dt = 100 A/ $\mu$ s,	-	250		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 480 V, T <sub>j</sub> = 150 °C	-	2.5		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.7		Α

<sup>1.</sup> Pulse width is limited by safe operating area.

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<sup>2.</sup> Pulse test: pulse duration =  $300 \mu s$ , duty cycle 1.5%.



### 2.1 Electrical characteristics (curves)

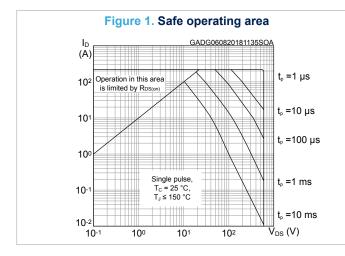


Figure 2. Normalized transient thermal impedance

K

AM09125v1

10<sup>-1</sup>

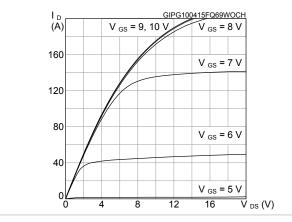
10<sup>-1</sup>

Single pulse

10<sup>-2</sup>

10<sup>-1</sup>

Figure 3. Tipical output characteristics



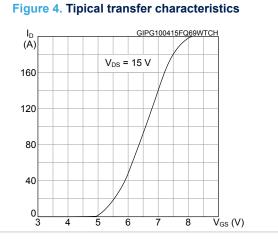
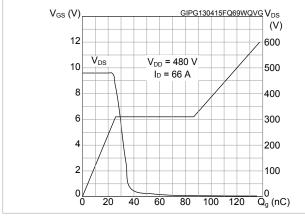
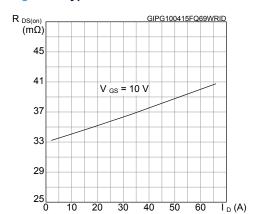


Figure 5. Typical gate charge characteristics







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Figure 7. Typical capacitance characteristics

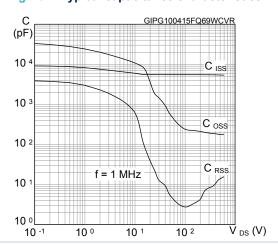


Figure 8. Normalized gate threshold vs temperature

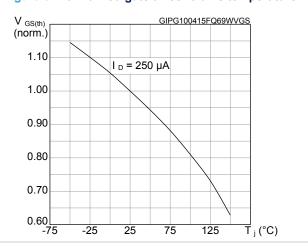


Figure 9. Normalized on-resistance vs temperature

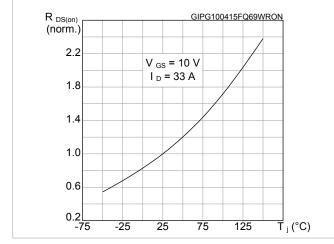


Figure 10. Normalized breakdown voltage vs temperature

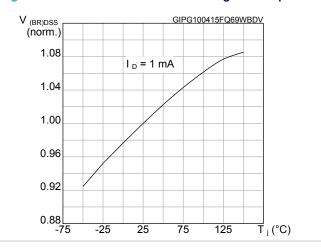


Figure 11. Typical output capacitance stored energy

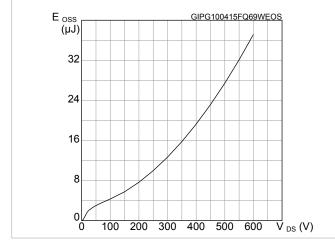
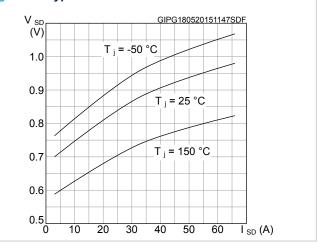


Figure 12. Typical reverse diode forward characteristics



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## 3 Test circuits

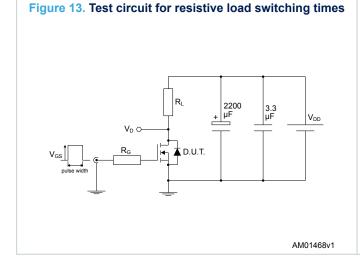
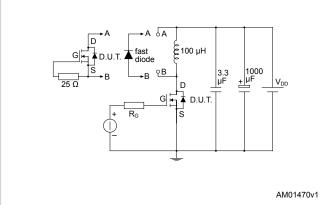


Figure 16. Unclamped inductive load test circuit

Figure 15. Test circuit for inductive load switching and diode recovery times



2200 3.3 V<sub>DD</sub>

| D.U.T. | D.U.T. | AM01471v1

Figure 17. Unclamped inductive waveform

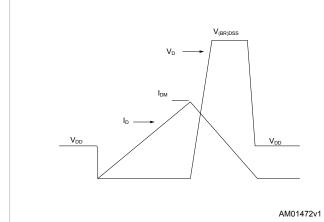
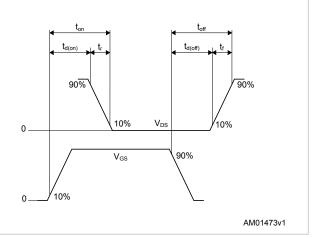


Figure 18. Switching time waveform



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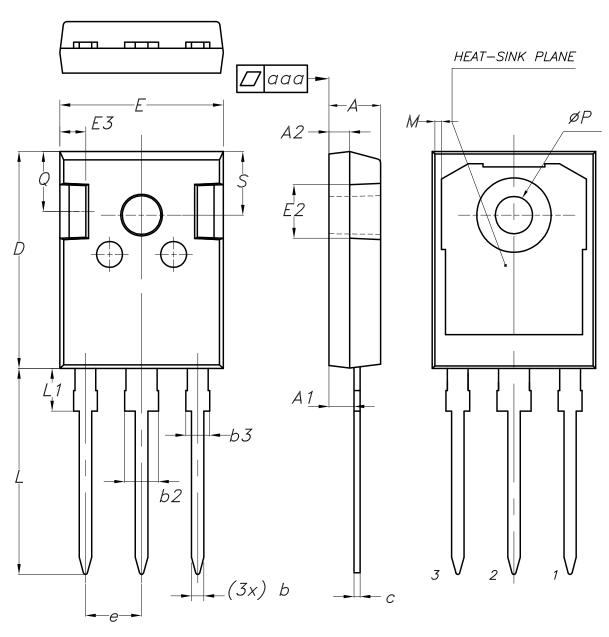


# 4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

### 4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline



BACK VIEW

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Table 8. TO-247 long leads package mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
Α	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
С	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
е	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
Р	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

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# **Revision history**

Table 9. Document revision history

Version	Changes
1	Initial release. The document status is production data.
2	Updated Section 4.1: TO-247 long leads package information.  Minor text changes.
	1

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