

### **Automotive MOSFET**

### OptiMOS™ 7 Power-Transistor







#### **Features**

- OptiMOS<sup>™</sup> power MOSFET for automotive applications
- N-channel Enhancement mode Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested



General automotive applications.



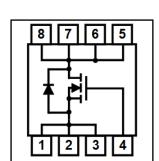
Qualified for automotive applications. Product validation according to AEC-Q101.

### **Product Summary**

$V_{\mathrm{DS}}$	80	V
R <sub>DS(on)</sub>	4.6	mΩ
I <sub>D</sub> (chip limited)	99	Α

Туре	Package	Marking
IAUZN08S7N046	PG-TSDSON-8-39	8A





2025-04-24

## IAUZN08S7N046



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# **Maximum Ratings**

at  $T_j = 25$ °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I <sub>D</sub>	$V_{\rm GS} = 10  \text{V}$ , Chip limitation <sup>1,2)</sup>	99	А
		V <sub>GS</sub> = 10 V, DC current	60	
		$T_a = 100$ °C, $V_{GS} = 10$ V, $R_{thJA}$ on $2s2p^{2,3)}$	14	
Pulsed drain current <sup>2)</sup>	I <sub>D,pulse</sub>	$T_{\rm C} = 25^{\circ}{\rm C}, t_{\rm p} = 100 \mu{\rm s}$	250	
Avalanche energy, single pulse <sup>2)</sup>	E <sub>AS</sub>	I <sub>D</sub> = 30 A	54	mJ
Avalanche current, single pulse	I <sub>AS</sub>	-	60	А
Gate source voltage	$V_{GS}$	-	±20	V
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> = 25°C	94	W
Operating temperature	T <sub>j</sub>	-	-55 +175	°C

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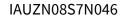
# Thermal Characteristics<sup>2)</sup>

Davamatav	Symbol Conditions -		Values			11:4:4
Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Thermal resistance, junction - case	$R_{thJC}$	-	_	_	1.6	K/W
Thermal resistance, junction - ambient <sup>3)</sup>	$R_{thJA}$	-	_	40.0	-	

## **Electrical Characteristics**

at T<sub>i</sub>=25 °C, unless otherwise specified

Parameter	Comple - I	Symbol Conditions -	Values			
	Symbol		min.	typ.	max.	Unit
Static Characteristics						
Drain-source breakdown voltage	V <sub>(Br)DSS</sub>	$V_{GS} = 0 \text{ V},$ $I_D = 1 \text{ mA}$	80	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 35 \mu\text{A}$	2.3	2.8	3.2	
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_j = 25^{\circ}\text{C}$	-	-	1	μΑ
Zero gate voltage drain current	7 <sub>DSS</sub>	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V},$ $T_j = 100^{\circ}\text{C}^{2}$	_	_	9	
Gate-source leakage current	I <sub>GSS</sub>	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	100	nA
		$V_{GS} = 7 \text{ V}, I_D = 15 \text{ A}$	-	4.7	5.5	mΩ
Drain-source on-state resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$	-	4.2	4.6	]
Gate resistance <sup>2)</sup>	R <sub>G</sub>	-	_	1.1	_	Ω





Parameter	Symbol Conditions -	Values			11:4:4	
		min.	typ.	max.	Unit	
Dynamic Characteristics <sup>2)</sup>						
Input capacitance	C iss		_	1742	2265	pF
Output capacitance	C oss	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}, f = 1 \text{ MHz}$	_	714	929	
Reverse transfer capacitance	C <sub>rss</sub>		-	13	20	
Turn-on delay time	t <sub>d(on)</sub>		-	6.4	-	ns
Rise time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, V_{GS} = 10 \text{ V},$ $I_{D} = 30 \text{ A}, R_{G} = 3.5 \Omega$	_	3.7	-	
Turn-off delay time	t <sub>d(off)</sub>		_	12.2	-	
Fall time	t <sub>f</sub>		_	7.0	-	

**Gate Charge Characteristics**2)

Gate to source charge	Q <sub>gs</sub>		ı	8.1	10.5	nC
Gate to drain charge	Q <sub>gd</sub>	$V_{DD} = 40 \text{ V}, I_D = 30 \text{ A},$	-	5.5	8.3	
Gate charge total	Qg	$V_{DD} = 40 \text{ V}, I_D = 30 \text{ A},$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	27.2	35.4	
Gate plateau voltage	V <sub>plateau</sub>		-	4.6	-	V

## **Reverse Diode**

Diode continuous forward current <sup>2)</sup>	Is	T <sub>C</sub> = 25°C	ı	ı	60	А
Diode pulse current <sup>2)</sup>	I <sub>S,pulse</sub>	$T_{\rm C} = 25^{\circ}{\rm C}, t_{\rm p} = 100 \mu{\rm s}$	ı	ı	250	
Diode forward voltage	V <sub>SD</sub>	$V_{GS} = 0 \text{ V}, I_F = 30 \text{ A}, T_j = 25^{\circ}\text{C}$	ı	0.9	1.0	V
Reverse recovery time <sup>2)</sup>	t <sub>rr</sub>	V <sub>R</sub> = 40 V, I <sub>F</sub> = 50 A	-	25	38	ns
Reverse recovery charge <sup>2)</sup>	Q <sub>rr</sub>	$di_F/dt = 100 A/\mu s$	-	11	22	nC

 $<sup>^{1)}</sup>$  Practically the current is limited by the overall system design including the customer-specific PCB.

<sup>&</sup>lt;sup>2)</sup> The parameter is not subject to production testing – specified by design.

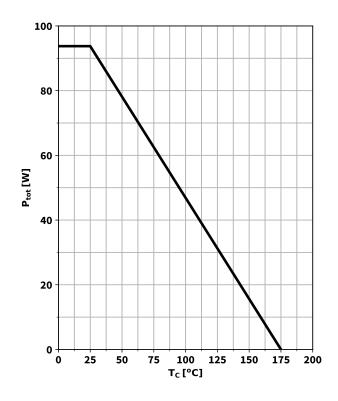
<sup>&</sup>lt;sup>3)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.



## **Electrical characteristics diagrams**

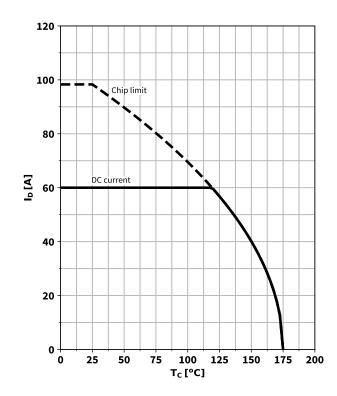
#### 1 Power dissipation

 $P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} \ge 6 \text{ V}$ 



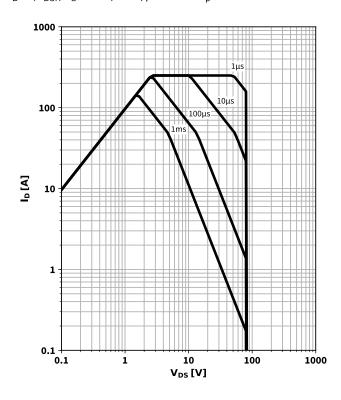
#### 2 Drain current

 $I_{\text{D}} = f(T_{\text{C}}); V_{\text{GS}} \ge 6 \text{ V}$ 



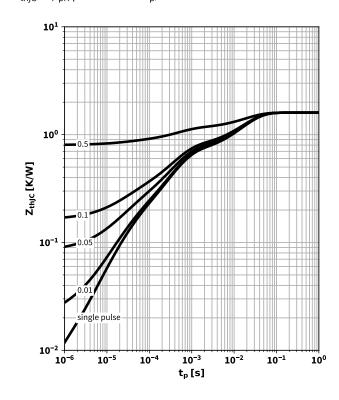
#### 3 Safe operating area

 $I_{\rm D}$  = f( $V_{\rm DS}$ );  $T_{\rm C}$  = 25 °C; D = 0; parameter:  $t_{\rm p}$ 



#### 4 Max. transient thermal impedance

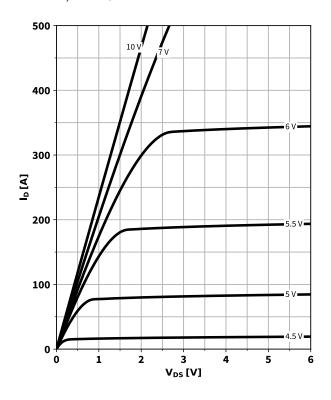
 $Z_{\text{thJC}} = f(t_p)$ ; parameter: D =  $t_p/T$ 





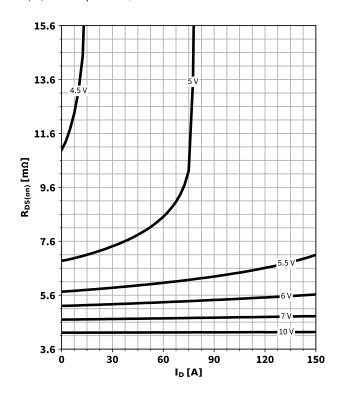
### 5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25 \,^{\circ}\text{C}; \text{ parameter: } V_{GS}$ 



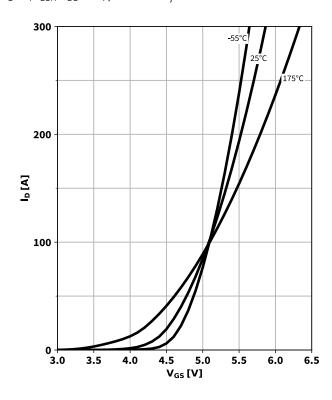
### 6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25 \text{ °C}; parameter: } V_{GS}$ 



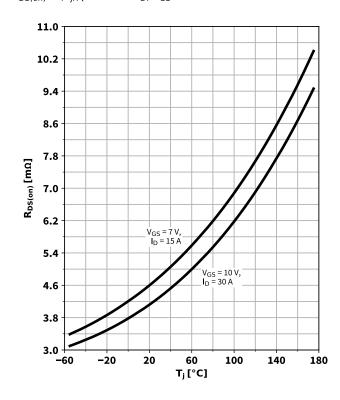
### 7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6 \text{ V}; \text{ parameter: } T_j$ 



#### 8 Typ. drain-source on-state resistance

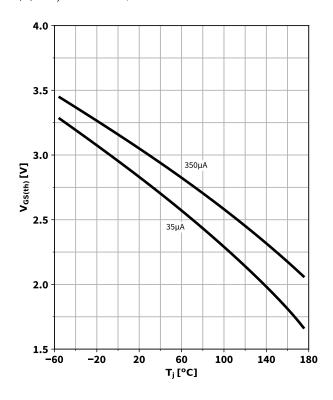
 $R_{DS(on)} = f(T_j)$ ; parameter:  $I_D$ ,  $V_{GS}$ 





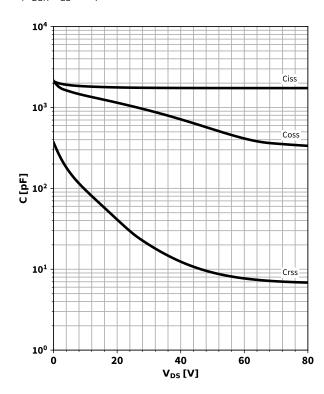
#### 9 Typ. gate threshold voltage

 $V_{\text{GS(th)}} = f(T_{\text{j}}); V_{\text{GS}} = V_{\text{DS}}; \text{ parameter: } I_{\text{D}}$ 



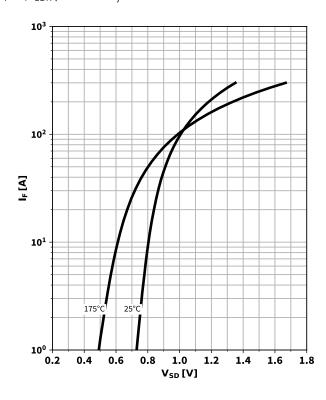
#### 10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$ 



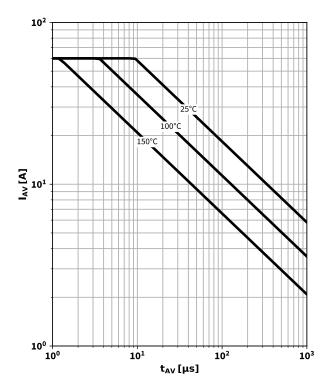
### 11 Typ. forward diode characteristics

 $I_F = f(V_{SD})$ ; parameter:  $T_j$ 



#### 12 Typ. avalanche characteristics

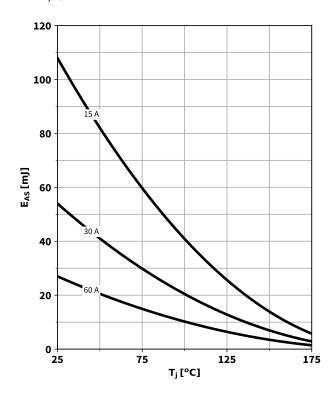
 $I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$ 





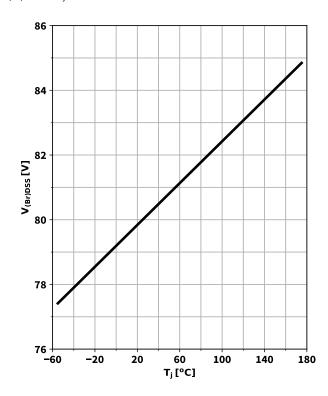
#### 13 Typical avalanche energy

 $E_{AS} = f(T_j)$ ; parameter:  $I_D$ 



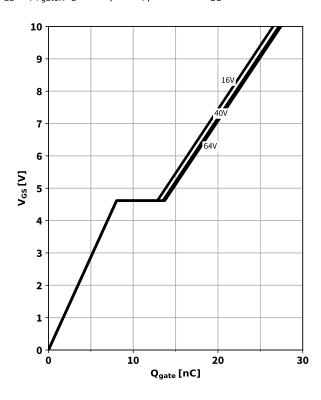
### 14 Drain-source breakdown voltage

 $V_{(Br)DSS} = f(T_j); I_D = 1 \text{ mA}$ 

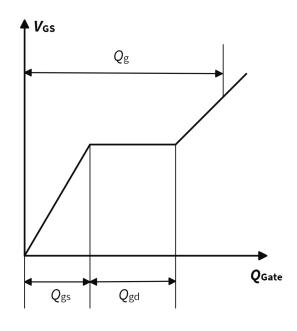


### 15 Typ. gate charge

 $V_{GS} = f(Q_{gate}); I_D = 30 \text{ A pulsed}; parameter: } V_{DD}$ 



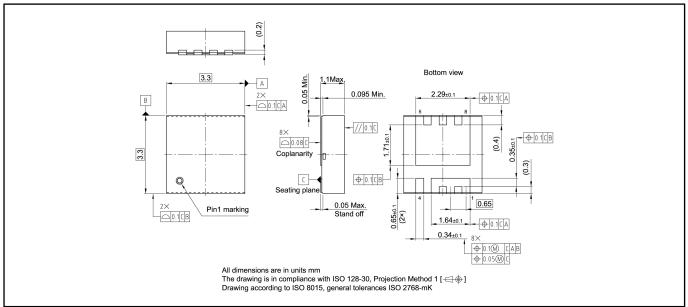
#### 16 Gate charge waveforms



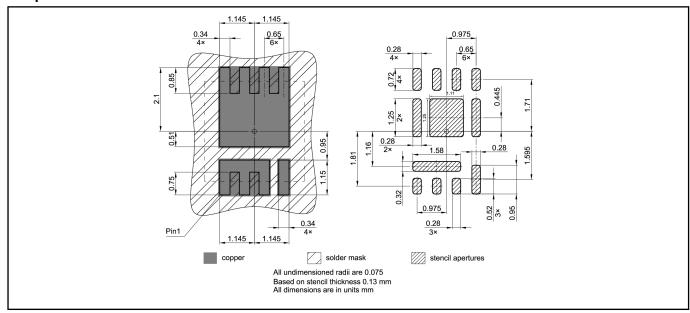
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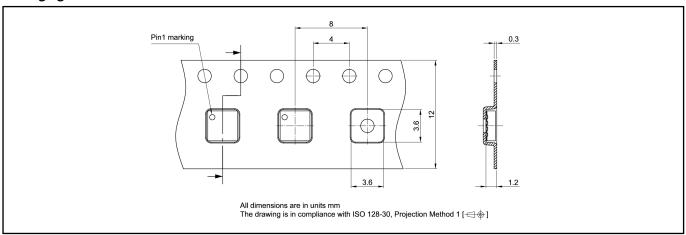
### **Package Outline**



#### **Footprint**



#### **Packaging**



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# **Revision History**

Revision	Date	Changes
Revision 1.0	2025-04-24	Final data sheet

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