Ι<sub>D</sub>

60A



### **SMPS MOSFET**

V<sub>DSS</sub>

150V

# IRFB61N15DPbF

R<sub>DS(on)</sub> max

 $\mathbf{0.032}\Omega$ 

HEXFET® Power MOSFET

### **Applications**

- High frequency DC-DC converters
- Motor Control
- Uninterrutible Power Supplies
- Lead-Free

#### **Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



### **Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	60	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	42	Α
I <sub>DM</sub>	Pulsed Drain Current ①	250	
P <sub>D</sub> @T <sub>A</sub> = 25°C	Power Dissipation	2.4	W
P <sub>D</sub> @T <sub>C</sub> = 25°C	Power Dissipation	330	
	Linear Derating Factor	2.2	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.7	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torqe, 6-32 or M3 screw®	10 lbf•in (1.1N•m)	

### **Thermal Resistance**

	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case		0.45	
R <sub>0CS</sub>	Case-to-Sink, Flat, Greased Surface	0.50		°C/W
$R_{\theta JA}$	Junction-to-Ambient		62	

Notes 1 through 5 are on page 8



## Static @ $T_J = 25^{\circ}C$ (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.18		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance			0.032	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 36A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0		5.5	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$
I <sub>DSS</sub>	Drain-to-Source Leakage Current			25	μА	$V_{DS} = 150V, V_{GS} = 0V$
אסטי	Brain to Course Ecanage Current			250	μΛ	$V_{DS} = 120V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 30V$
IGSS	Gate-to-Source Reverse Leakage			-100	IIA	V <sub>GS</sub> = -30V

### Dynamic @ $T_1 = 25^{\circ}C$ (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
<b>9</b> fs	Forward Transconductance	22			S	$V_{DS} = 50V, I_{D} = 37A$
Qg	Total Gate Charge		95	140		I <sub>D</sub> = 37A
Q <sub>gs</sub>	Gate-to-Source Charge		26	39	nC	V <sub>DS</sub> = 120V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge		45	68	Ī	$V_{GS} = 10V$ ,
t <sub>d(on)</sub>	Turn-On Delay Time		18			$V_{DD} = 75V$
t <sub>r</sub>	Rise Time		110		ns	$I_D = 37A$
t <sub>d(off)</sub>	Turn-Off Delay Time		28			$R_G = 1.8\Omega$
t <sub>f</sub>	Fall Time		51			V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance		3470			$V_{GS} = 0V$
Coss	Output Capacitance		690			$V_{DS} = 25V$
C <sub>rss</sub>	Reverse Transfer Capacitance		150		pF	f = 1.0MHz
Coss	Output Capacitance		4600			$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
Coss	Output Capacitance		310			$V_{GS} = 0V$ , $V_{DS} = 120V$ , $f = 1.0MHz$
Coss eff.	Effective Output Capacitance		580			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V ⑤

### **Avalanche Characteristics**

	Parameter	Тур.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>②</sup>		520	mJ
I <sub>AR</sub>	Avalanche Current①		37	Α
E <sub>AR</sub>	Repetitive Avalanche Energy①		33	mJ

### **Diode Characteristics**

	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current	60		60		MOSFET symbol
	(Body Diode)			60	A	showing the
I <sub>SM</sub>	Pulsed Source Current			250	' '	integral reverse
	(Body Diode) ①	4	250	0	p-n junction diode.	
$V_{SD}$	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C$ , $I_S = 37A$ , $V_{GS} = 0V$ ④
t <sub>rr</sub>	Reverse Recovery Time		180	270	ns	$T_J = 25^{\circ}C, I_F = 37A$
Q <sub>rr</sub>	Reverse RecoveryCharge		1340	2010	nC	di/dt = 100A/µs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

# International TOR Rectifier

## IRFB61N15DPbF

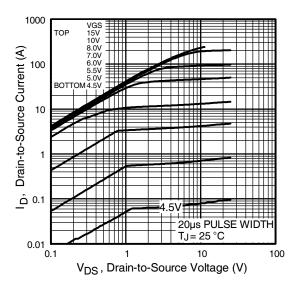


Fig 1. Typical Output Characteristics

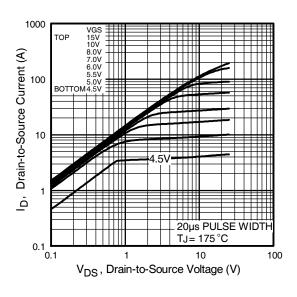


Fig 2. Typical Output Characteristics

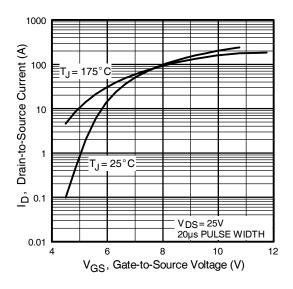
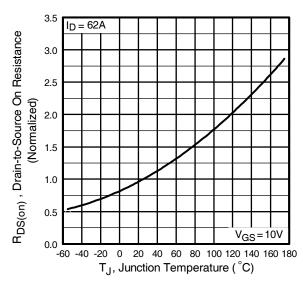
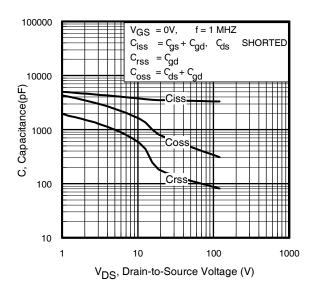


Fig 3. Typical Transfer Characteristics

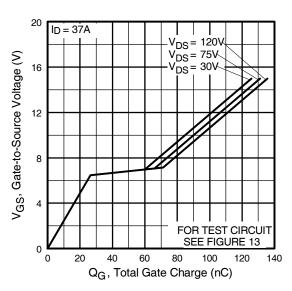


**Fig 4.** Normalized On-Resistance Vs. Temperature

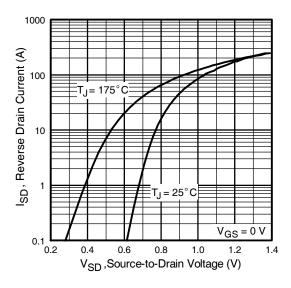
# International Rectifier



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage

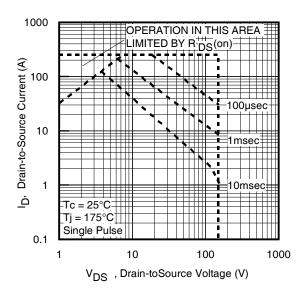
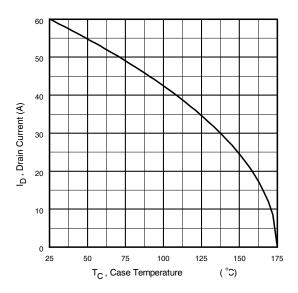


Fig 8. Maximum Safe Operating Area

# International TOR Rectifier

## IRFB61N15DPbF



**Fig 9.** Maximum Drain Current Vs. Case Temperature

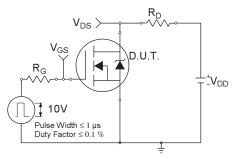


Fig 10a. Switching Time Test Circuit

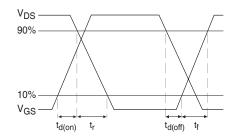


Fig 10b. Switching Time Waveforms

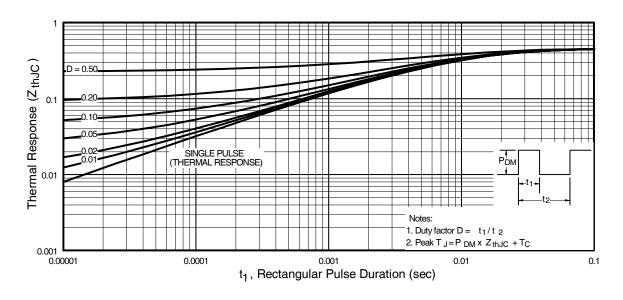


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

# International Rectifier

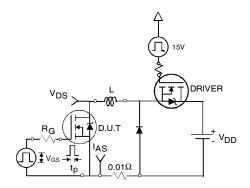


Fig 12a. Unclamped Inductive Test Circuit

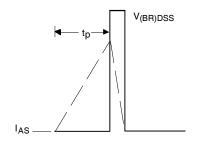
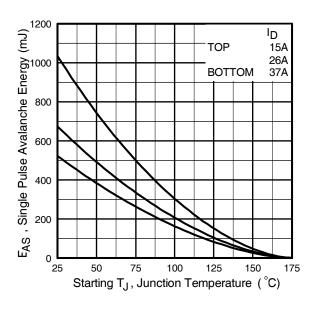


Fig 12b. Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

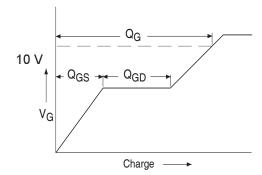


Fig 13a. Basic Gate Charge Waveform

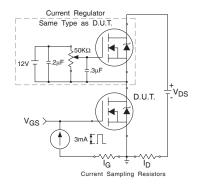
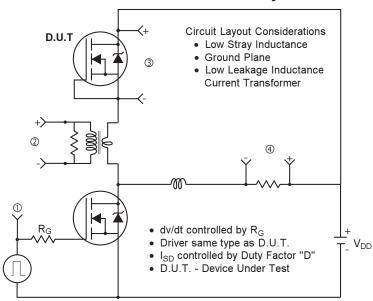
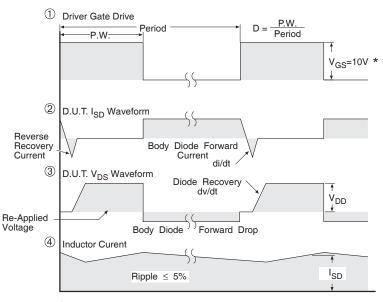


Fig 13b. Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit

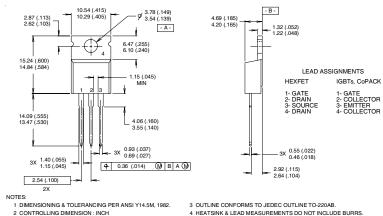




\* V<sub>GS</sub> = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

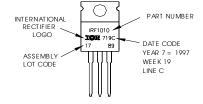
### TO-220AB Package Outline



### TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010 LOT CODE 1789 ASSEMBLED ON WW 19, 1997 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free



#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25$ °C, L = 0.98mH  $R_G = 25\Omega$ ,  $I_{AS} = 37A$ ,  $V_{GS} = 10V$
- T<sub>J</sub>≤ 175°C
- 4 Pulse width  $\leq$  400 $\mu$ s; duty cycle  $\leq$  2%.
- ⑤ Coss eff. is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 80% VDSS

Data and specifications subject to change without notice. This product has been designed and qualified for the Industrial market. Qualification Standards can be found on IR's Web site.



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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.08/04

Note: For the most current drawings please refer to the IR website at: <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>

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