MOSFET – Power, Single N-Channel 60 V, 4.0 m Ω , 100 A

NVMYS4D1N06CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage	Э		V_{GS}	±20	V
Continuous Drain	Steady State	T _C = 25°C	I _D	100	Α
Current R _{θJC} (Notes 1, 2, 3)	State	T _C = 100°C		71	
Power Dissipation		T _C = 25°C	P_{D}	79	W
R _{θJC} (Notes 1, 2)		T _C = 100°C		40	
Continuous Drain Current R _{0JA}	Steady State	T _A = 25°C	I _D	22	Α
(Notes 1, 2, 3)	State	T _A = 100°C		15	
Power Dissipation	T _A = 25°C		P_{D}	3.7	W
R _{θJA} (Notes 1, 2)		T _A = 100°C		1.8	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	820	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			I _S	100	Α
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25$ °C, $I_{L(pk)} = 5$ A)			E _{AS}	185	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{ heta JC}$	1.9	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	39	

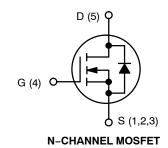
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX	
60 V	4.0 mΩ @ 10 V	100 A	
00 V	5.7 mΩ @ 4.5 V	100 A	





LFPAK4 CASE 760AB



4D1N06CL = Specific Device Code A = Assembly Location

WL =Wafer Lot Y = Year W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS					•			
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J				28		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	Voc = 0 V				10		
		$V_{GS} = 0 V$, $V_{DS} = 48 V$	T _J = 125°C			250	μΑ	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA	
ON CHARACTERISTICS (Note 4)					-			
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 80 μΑ	1.2		2.0	V	
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.4		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 50 A		3.3	4.0		
		V _{GS} = 4.5 V	I _D = 50 A		4.6	5.7	mΩ	
Forward Transconductance	9FS	V _{DS} = 15 V, I _D	= 50 A		105		S	
CHARGES, CAPACITANCES & GATE RESIS	STANCE				-			
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			2200			
Output Capacitance	C _{OSS}				900		pF	
Reverse Transfer Capacitance	C _{RSS}				17			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 30 V; I _D = 50 A			16			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 30 V; I _D = 50 A			34		1	
Threshold Gate Charge	Q _{G(TH)}				1.5		nC	
Gate-to-Source Charge	Q_{GS}		0)// 50 4		5.6		1 !	
Gate-to-Drain Charge	Q_{GD}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 30 \text{ V}; I_D = 50 \text{ A}$			5.1]	
Plateau Voltage	V_{GP}				2.8		V	
SWITCHING CHARACTERISTICS (Note 5)					-			
Turn-On Delay Time	t _{d(ON)}				10			
Rise Time	t _r	V _{GS} = 4.5 V, V _{DS}	s = 30 V,		15		1	
Turn-Off Delay Time	t _{d(OFF)}	$I_D = 50 \text{ A}, R_G =$	2.5 Ω		24		ns	
Fall Time	t _f				5.0		1	
DRAIN-SOURCE DIODE CHARACTERISTIC	s				-			
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V},$ $I_{S} = 50 \text{ A}$ $T_{J} = 25^{\circ}\text{C}$ $T_{J} = 125^{\circ}\text{C}$			0.88	1.2	'	
					0.78		V	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 50 \text{ A}$			41			
Charge Time	t _a				21		ns	
Discharge Time	t _b				20			
Reverse Recovery Charge	Q _{RR}				32		nC	
	•				•			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

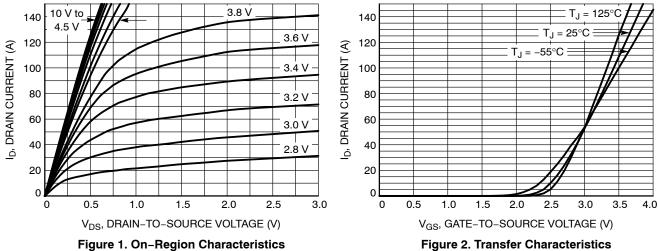


Figure 1. On-Region Characteristics

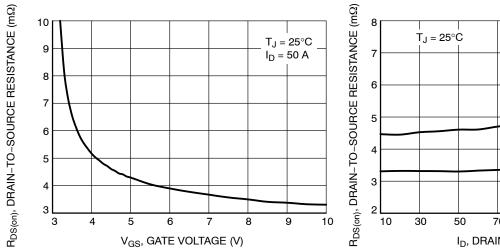


Figure 3. On-Resistance vs. Gate-to-Source Voltage

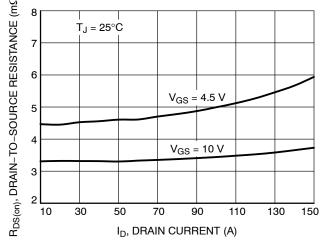


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**

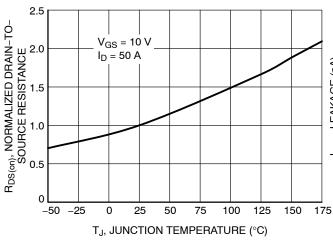


Figure 5. On-Resistance Variation with **Temperature**

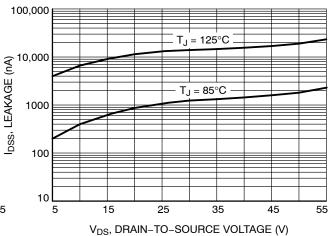
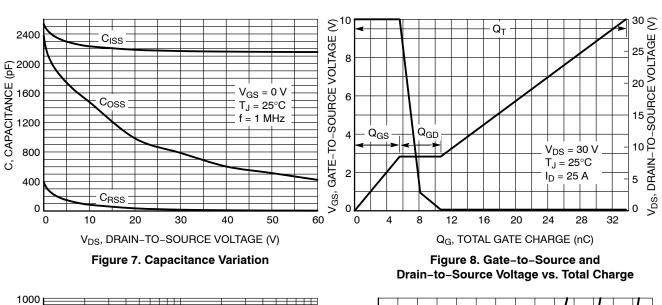


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS



 $V_{GS} = 4.5 V$ V_{DD} = 30 V $I_D = 25 A$ 100 t, TIME (ns) $t_{d(on)}$ 10 10 100 R_G , GATE RESISTANCE (Ω)



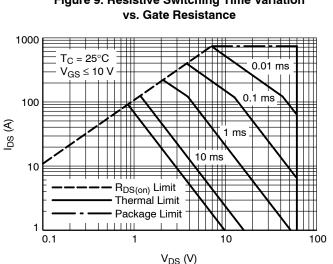


Figure 11. Safe Operating Area

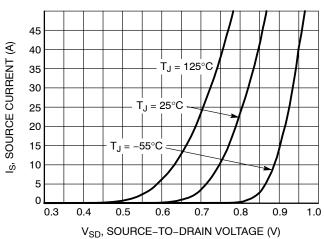


Figure 10. Diode Forward Voltage vs. Current

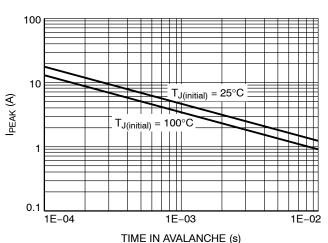


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

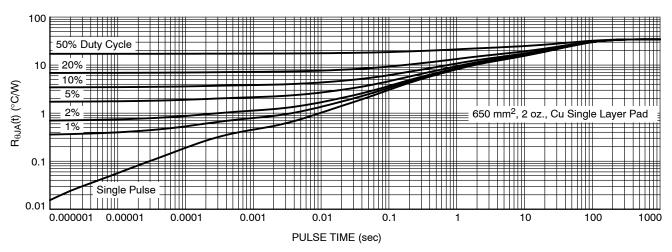


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMYS4D1N06CLTWG	4D1N06CL	LFPAK4 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





DATE 22 MAY 2024





NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
- 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.



0.70		- 1.27 -	
RECOM	IMENDI	ED LAND	PATTERN

1.30

1.06

0.60

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

BOTTOM VIEW

(D8)

XXXXXX XXXXXX AWLYW XXXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot Y = Year W = Work Week

MILLIMETER						
DIM	MIN	NOM	MAX			
Α	1.10	1.20	1.30			
A1	0.00	0.08	0.15			
A2	1.10	1.15	1.20			
А3	C).25 BSC)			
b	0.40	0.45	0.50			
b2	3.80	4.10	4.40			
b4	0.45	0.55	0.65 0.25			
C	0.19	0.22	0.25			
c2	0.19	0.22	0.25			
D	4	4.15 BS0				
D1	3.80	4.00	4.20			
D2	3.00	3.10	3.20			
D3	0.30	0.40	0.50			
D4	0.90	1.00	1.10			
D5	0.70	0.80	0.90			
D6	0.55	0.65	0.75			
D7		0.31 REI				
D8	(0.40 REF				
Е	4	4.90 BS	2			
E1	4.85	4.95	5.05			
E2	3.10	3.20	3.30			
E3	0.00	0.10	0.20			
E4	2.00	2.10	2.20			
е	1.27 BSC					
e/2		0.635 BSC				
e1	0.40 REF					
Н	6.00	6.15	6.30			
L	0.50	0.70	0.90			
L1	0.80	0.90	1.00			
L2	1.10 REF					
θ	0°	4°	8°			

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