International Rectifier

- Ultra Low On-Resistance
- Surface Mount (IRFR3910)
- Straight Lead (IRFU3910)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

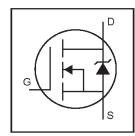
Description

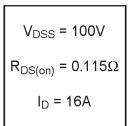
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

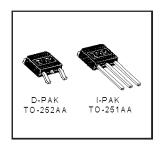
The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for throughhole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

IRFR3910PbFIRFU3910PbF

HEXFET® Power MOSFET







Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	16	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	12	A
I _{DM}	Pulsed Drain Current ①⑥	60	
P _D @T _C = 25°C	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy②⑤	150	mJ
I _{AR}	Avalanche Current①⑥	9.0	Α
E _{AR}	Repetitive Avalanche Energy®	7.9	mJ
d∨/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
TJ	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Тур.	Max.	Units
Rejc	Junction-to-Case		1.9	
Reja	Junction-to-Ambient (PCB mount) **		50	°C/W
Ra. IA	Junction-to-Ambient		110	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Мах.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_{D} = 250\mu A$
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient		0.12		V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.115		V _{GS} = 10V, I _D = 10A ⊕
V _{GS(th)}	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g fs	Forward Transconductance	6.4			S	V _{DS} = 50V, I _D = 9.0A6
	Paris to Course Looks as Courset			25		V _{DS} = 100V, V _{GS} = 0V
l _{DSS}	Drain-to-Source Leakage Current			250	μΑ	$V_{DS} = 80V$, $V_{GS} = 0V$, $T_{J} = 150$ °C
ı	Gate-to-Source Forward Leakage			100	- A	V _{GS} = 20V
I _{GSS}	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -20V
Qq	Total Gate Charge			44		I _D = 9.0A
Qgs	Gate-to-Source Charge			6.2	nC	V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	_		21		V _{GS} = 10V, See Fig. 6 and 13 ⊕ €
t _{d(on)}	Turn-On Delay Time		6.4			V _{DD} = 50V
tr	Rise Time	_	27		ns	I _D = 9.0A
t _{d(off)}	Turn-Off Delay Time		37		115	$R_{G} = 12\Omega$
tf	Fall Time		25			R _D = 5.5Ω, See Fig. 10 ⊕⑥
	Internal Dusin Industrues		4.5			Between lead,
L _D	Internal Drain Inductance	_	4.5		nΗ	6mm (0.25in.)
	Internal Source Inductance		7.5			from package
L _S	Internal Source Inductance		7.5			and center of die contact® s
C _{iss}	Input Capacitance		640			V _{GS} = 0V
Coss	Output Capacitance		160		pF	V _{DS} = 25V
Crss	Reverse Transfer Capacitance		88		†	f = 1.0MHz, See Fig. 5®

Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions		
Is	Continuous Source Current			16		MOSFET symbol		
	(Body Diode)		16		A	showing the		
I _{SM}	Pulsed Source Current				^	integral reverse		
	(Body Diode) ①⑥			60		p-n junction diode.		
V _{SD}	Diode Forward Voltage			1.3	V	T _J = 25°C, I _S = 9.0A, V _{GS} = 0V ⊕		
trr	Reverse Recovery Time		130	190	ns	T _J = 25°C, I _F = 9.0A		
Qn	Reverse RecoveryCharge		650	970	nC	di/dt = 100A/µs ⊕ ⊚		
ton	Forward Turn-On Time	Intr	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)					

Notes

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- \mathbb{Q} V_{DD} = 25V, starting T_J = 25°C, L = 3.1mH R_G = 25 Ω , I_{AS} = 9.0A. (See Figure 12)
- 4 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$
- ⑤ This is applied for I-PAK, Ls of D-PAK is measured between lead and center of die contact
- \$ $I_{SD}\!\le\!9.0A,$ di/dt $\le\!520A/\mu s,$ $V_{DD}\!\le\!V_{(BR)DSS},$ \$ Uses IRF530N data and test conditions $T_{J}\!\le\!175^{\circ}C$
- ** When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994

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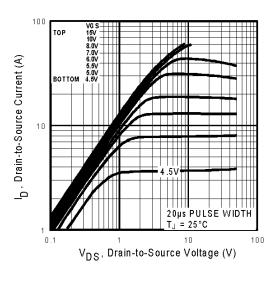
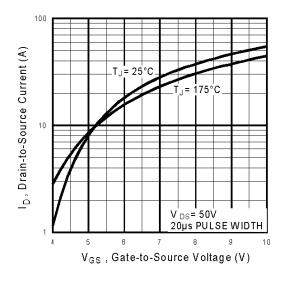


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics



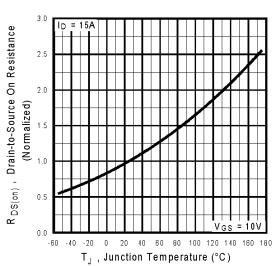


Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature

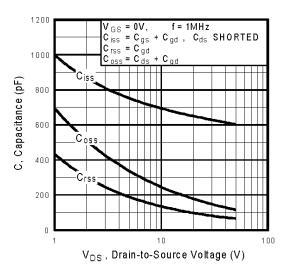


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

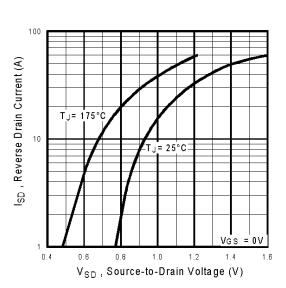


Fig 7. Typical Source-Drain Diode Forward Voltage

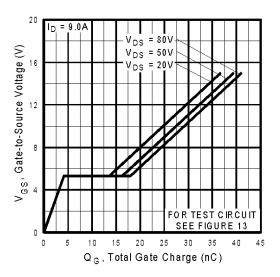


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

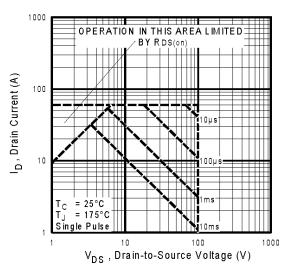


Fig 8. Maximum Safe Operating Area

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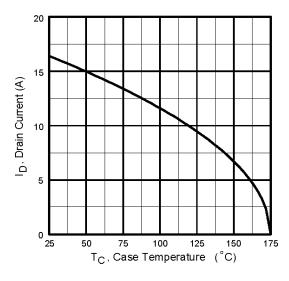


Fig 9. Maximum Drain Current Vs. Case Temperature

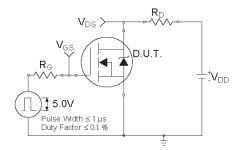


Fig 10a. Switching Time Test Circuit

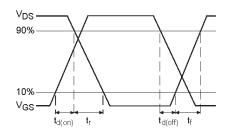
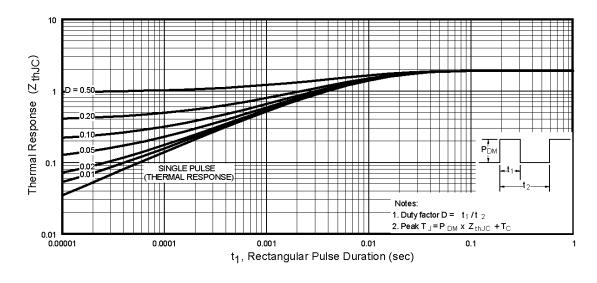


Fig 10b. Switching Time Waveforms



 $\textbf{Fig 11.} \ \ \textbf{Maximum Effective Transient Thermal Impedance, Junction-to-Case}$

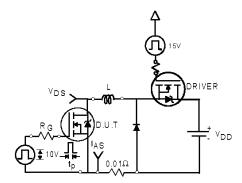


Fig 12a. Unclamped Inductive Test Circuit

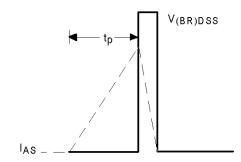


Fig 12b. Unclamped Inductive Waveforms

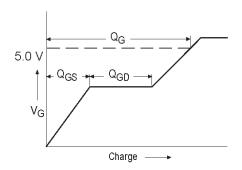


Fig 13a. Basic Gate Charge Waveform

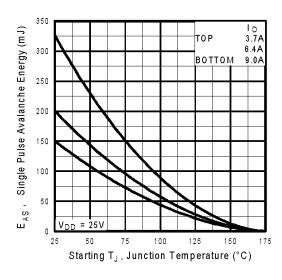


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

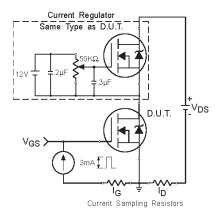
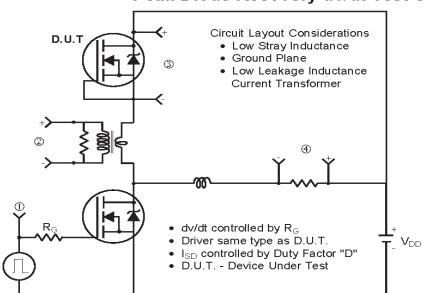


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



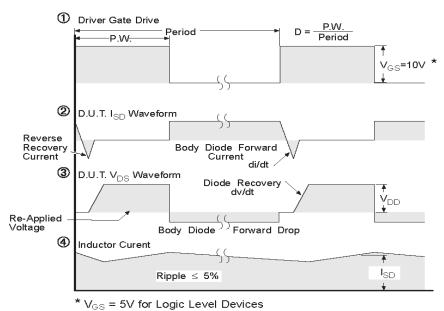


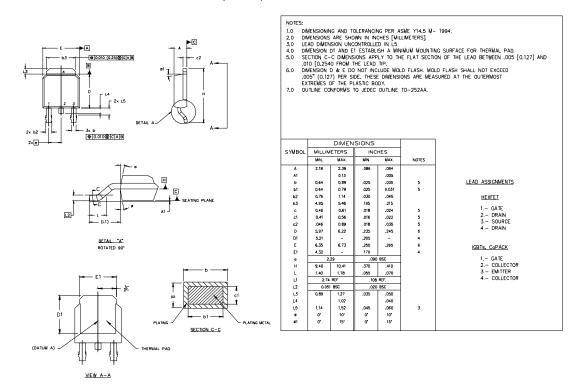
Fig 14. For N-Channel HEXFETS

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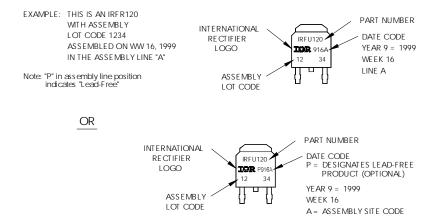


D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



D-Pak (TO-252AA) Part Marking Information

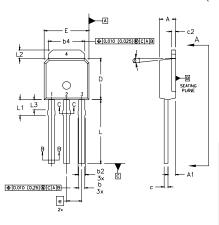


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I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



TES:					

- DIMENSIONING AND TOLERANCING PER ASME Y14,5 M- 1994.
- DMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

 DMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

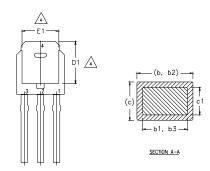
 DMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.005 (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

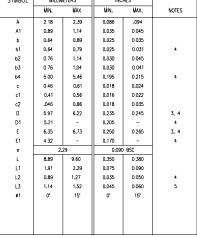
 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION 64, L2, E1 & D1.
- LEAD DIMENSION UNCONTROLLED IN L3.
- DIMENSION 61, 63 APPLY TO BASE METAL ONLY. OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- CONTROLLING DIMENSION: INCHES.

LEAD ASSIGNMENTS

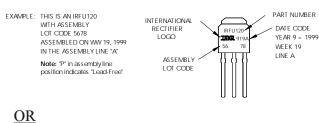
HEXFET

- 1,- GATE 2,- DRAIN 3,- SOURCE 4,- DRAIN
- DIMENSIONS SYMBOL MILLIMETERS INCHES

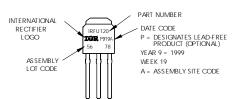




I-Pak (TO-251AA) Part Marking Information

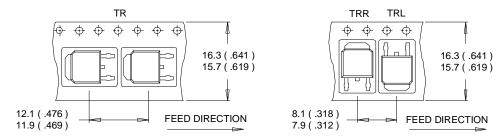






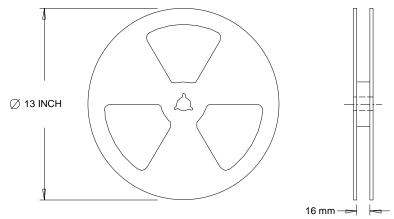
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.



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Note: For the most current drawings please refer to the IR website at: http://www.irf.com/package/

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