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NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE0110K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

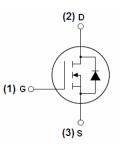
- V_{DS} =100V,I_D =9.6A
 - $R_{DS(ON)} < 140 \text{m}\Omega$ @ $V_{GS} = 10 \text{V}$ (Typ:108m Ω)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

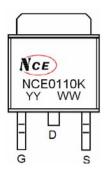
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

-						
	Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
	NCE0110K	NCE0110K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	9.6	Α
Drain Current-Continuous(T _C =100°C)	I _D (100°C)	6.5	Α
Pulsed Drain Current	I _{DM}	38.4	Α
Maximum Power Dissipation	P _D	30	W
Derating factor		0.2	W/°C
Single pulse avalanche energy (Note 5)	E _{AS}	20	mJ
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 175	$^{\circ}$ C



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NCE0110K

Thermal Characteristic

Electrical Characteristics (T_C=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current	ro Gate Voltage Drain Current I _{DSS} V _{DS} =		-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =6A	-	108	140	mΩ
Forward Transconductance	g FS	V _{DS} =25V,I _D =6A	3.5	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{lss}	.,	-	690	-	PF
Output Capacitance	Coss	$V_{DS}=25V,V_{GS}=0V,$	-	120	-	PF
Reverse Transfer Capacitance	C_{rss}	F=1.0MHz	-	90	-	PF
Switching Characteristics (Note 4)			•			•
Turn-on Delay Time	t _{d(on)}		-	11	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, I_{D} =2A, R_{L} =15 Ω	-	7.4	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10V, R_{G} =2.5 Ω	-	35	-	nS
Turn-Off Fall Time	t _f		-	9.1	-	nS
Total Gate Charge	Qg	\/ -20\/ -24	-	15.5		nC
Gate-Source Charge	Q _{gs}	V_{DS} =30V, I_{D} =3A, V_{GS} =10V	-	3.2	-	nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V	-	4.7	-	nC
Drain-Source Diode Characteristics			•			•
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =9.6A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	9.6	Α
Reverse Recovery Time	Recovery Time t_{rr} TJ = 25°C, IF =9.6A		-	21		nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	97		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

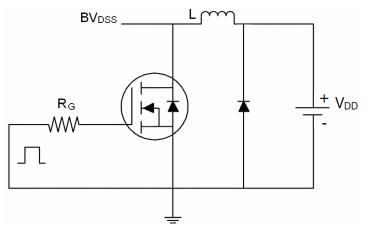
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board, $t \leq 10$ sec.
- **3.** Pulse Test: Pulse Width $\leq 300 \,\mu\,\mathrm{s}$, Duty Cycle $\leq 2\%$.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition : Tj=25 $^{\circ}$ C,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25 Ω

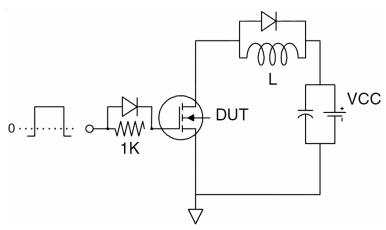


Test Circuit

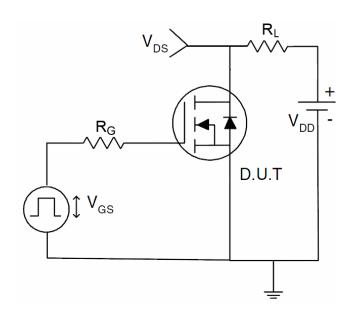
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



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Typical Electrical and Thermal Characteristics (Curves)

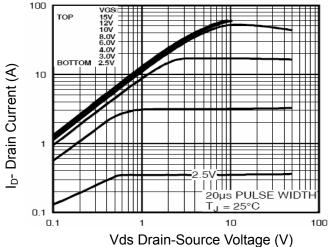


Figure 1 Output Characteristics

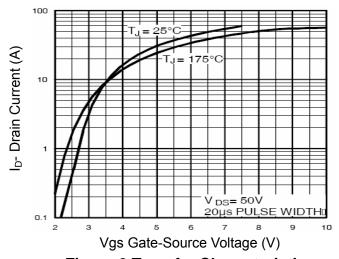


Figure 2 Transfer Characteristics

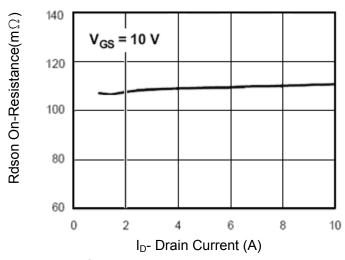


Figure 3 Rdson- Drain Current

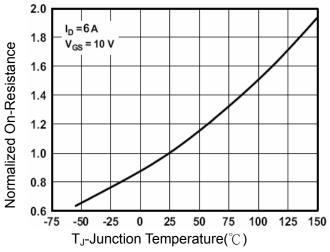


Figure 4 Rdson-JunctionTemperature

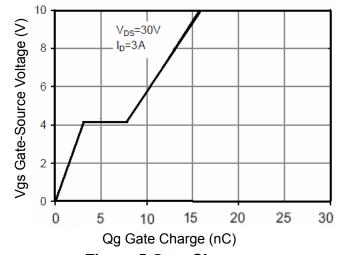


Figure 5 Gate Charge

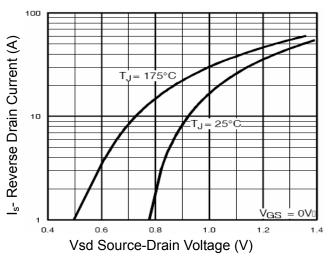


Figure 6 Source- Drain Diode Forward

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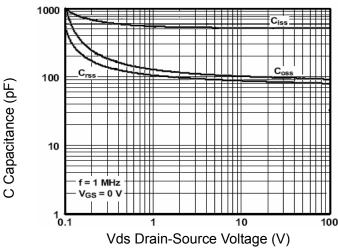


Figure 7 Capacitance vs Vds

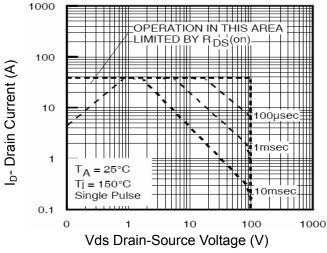


Figure 8 Safe Operation Area

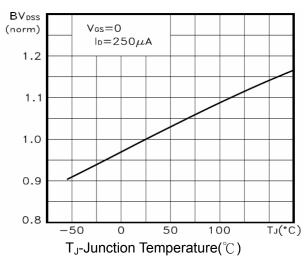


Figure 9 BV_{DSS} vs Junction Temperature

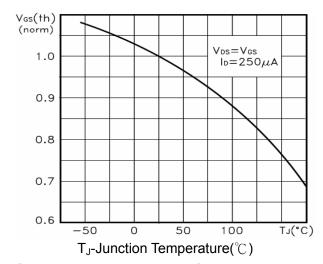


Figure 10 V_{GS(th)} vs Junction Temperature

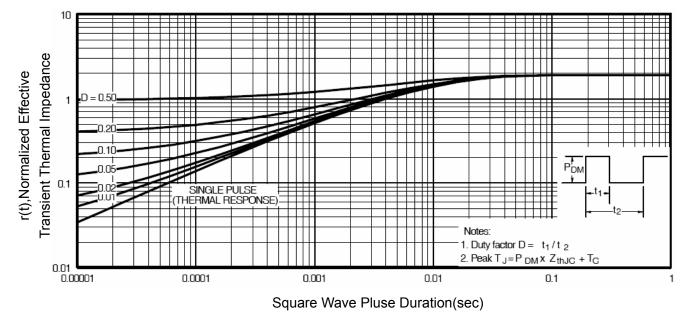


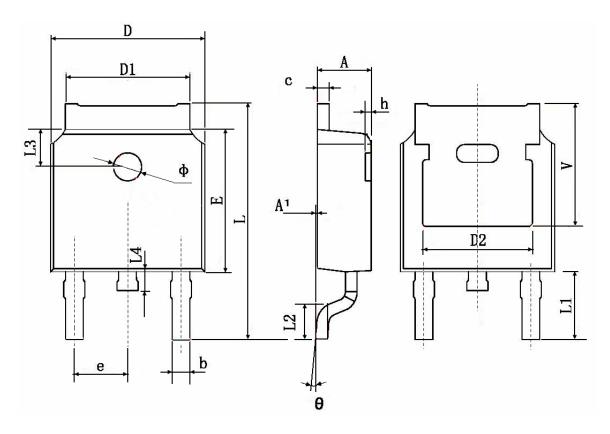
Figure 11 Normalized Maximum Transient Thermal Impedance

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TO-252 Package Information



O-mak al	Dimensions In Millimeters		Dimensions In Inches			
Symbol	Min.	Max.	Min.	Max.		
А	2.200	2.400	0.087	0.094		
A1	0.000	0.127	0.000	0.005		
b	0.660	0.860	0.026	0.034		
С	0.460	0.580	0.018	0.023		
D	6.500	6.700	0.256	0.264		
D1	5.100	5.460	0.201	0.215		
D2	4.830 TYP.		0.190 TYP.			
Е	6.000	6.200	0.236	0.244		
е	2.186	2.386	0.086	0.094		
L	9.800	10.400	0.386	0.409		
L1	2.900 TYP.		0.114 TYP.			
L2	1.400	1.700	0.055	0.067		
L3	1.600	1.600 TYP.		0.063 TYP.		
L4	0.600	1.000	0.024	0.039		
Ф	1.100	1.300	0.043	0.051		
θ	0°	8°	0°	8°		
h	0.000	0.300	0.000	0.012		
V	5.350	5.350 TYP. 0.211 TY				



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