N-Channel Power MOSFET

FEATURES

- Excellent FOM
- Ultra low rdson
- 100% UIS & Rg tested
- RoHS compliant
- Halogen-free

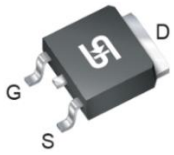
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	100	V
$R_{DS(on)}$ (max)	9.8	mΩ
$Q_{g,typ}$	26	nC

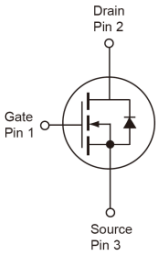
APPLICATIONS

- Solenoid and motor drivers
- DC-DC converters
- Load Switch
- SMPS

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-252_A





Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	49	A
	T_C = 100°C		31	
Pulsed Drain Current (Note 1)		I_{DM}	196	A
Total Power Dissipation	T_C = 25°C	P_D	46	W
	T_C = 100°C		19	
Single Pulse Avalanche Energy (Note 2)		E_{AS}	145	mJ
Single Pulse Avalanche Current (Note 2)		I_{AS}	9.8	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.7	°C/W
Junction to Ambient Thermal Resistance (Note 3)	$R_{\Theta JA}$	45	°C/W

Notes:

1. Pulse Width ≤ 100μs.
2. L = 3mH, R_G = 25Ω, Starting T_J = 25°C.
3. Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	100	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2	3	3.8	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 20A	$R_{DS(on)}$	--	7.5	9.8	mΩ
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 50V, I_D = 20A, V_{GS} = 10V	Q_g	--	26	--	nC
Gate-Source Charge		Q_{gs}	--	6.9	--	
Gate-Drain Charge		Q_{gd}	--	8	--	
Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1535	--	pF
Output Capacitance		C_{oss}	--	606	--	
Reverse Transfer Capacitance		C_{rss}	--	43	--	
Gate Resistance	f = 1.0MHz	R_g	--	1.5	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 50V, R_G = 3Ω, I_D = 20A, V_{GS} = 10V	$t_{d(on)}$	--	11	--	ns
Turn-On Rise Time		t_r	--	46	--	
Turn-Off Delay Time		$t_{d(off)}$	--	23	--	
Turn-Off Fall Time		t_f	--	34	--	
Source-Drain Diode						
Forward Voltage (Note 4)	I_S = 20A, V_{GS} = 0V	V_{SD}	--	--	1.2	V
Reverse Recovery Time	I_S = 20A, dI_F/dt = 100A/μs	t_{rr}	--	45	--	ns
Reverse Recovery Charge		Q_{rr}	--	61	--	nC

Notes:

4. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
5. Defined by design. Not subject to production test.
6. Switching time is essentially independent of operating temperature.

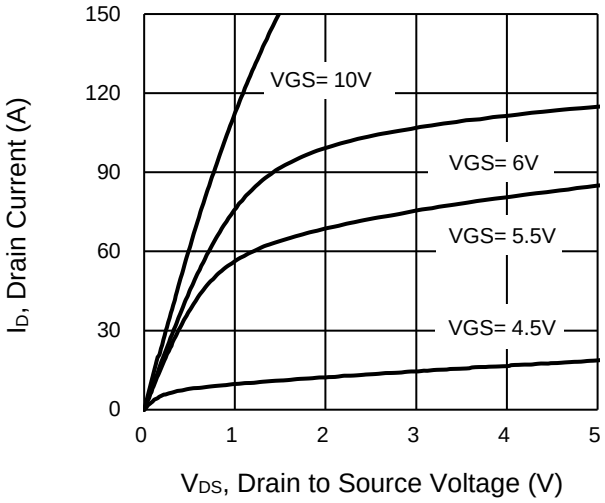
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM098NM10CP ROG	TO-252_A	2,500pcs / 13” Reel

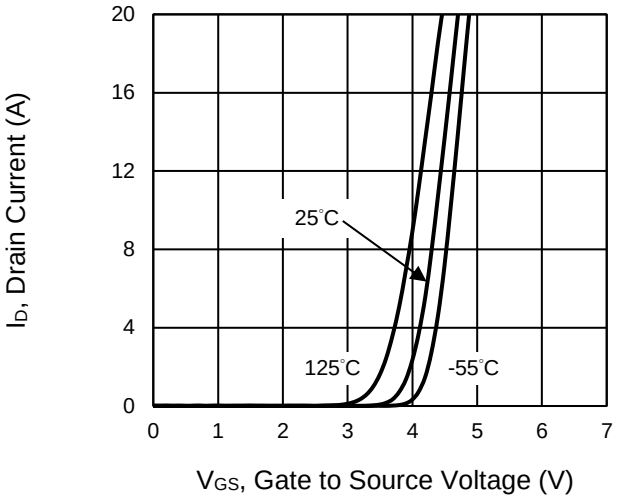
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

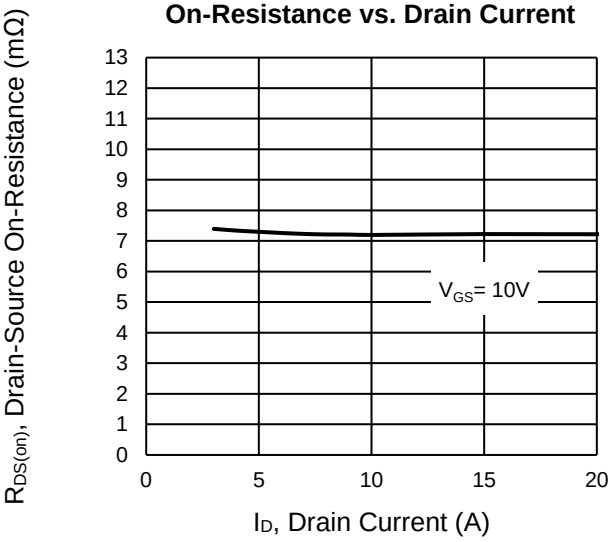
Output Characteristics



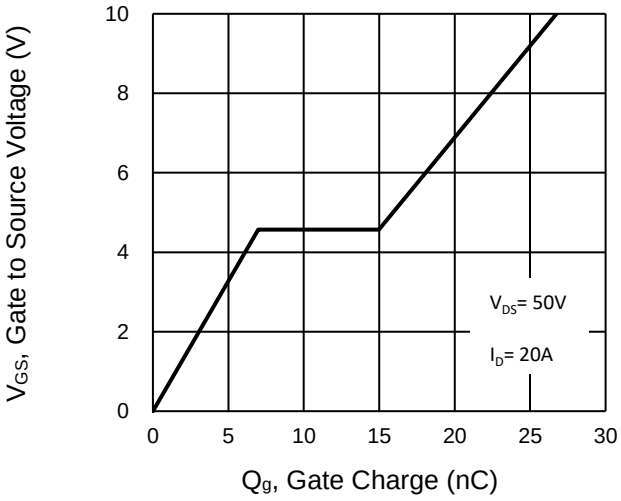
Transfer Characteristics



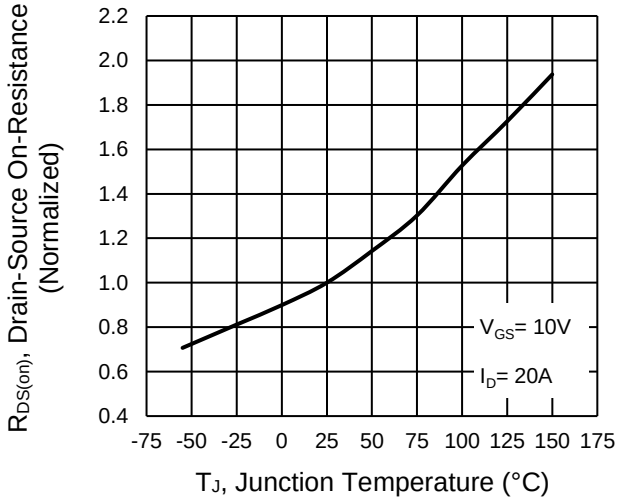
On-Resistance vs. Drain Current



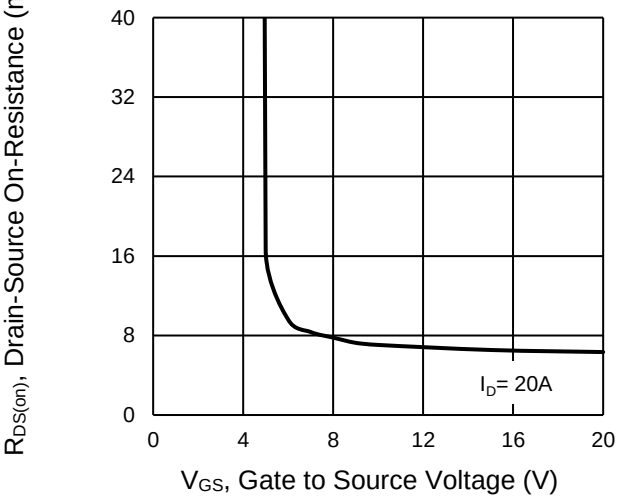
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



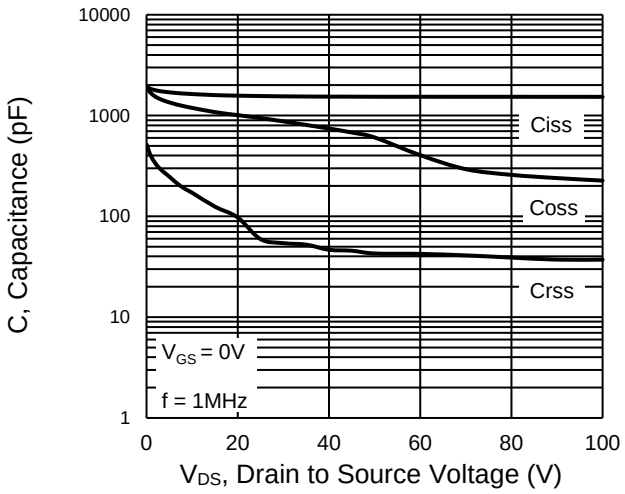
On-Resistance vs. Gate-Source Voltage



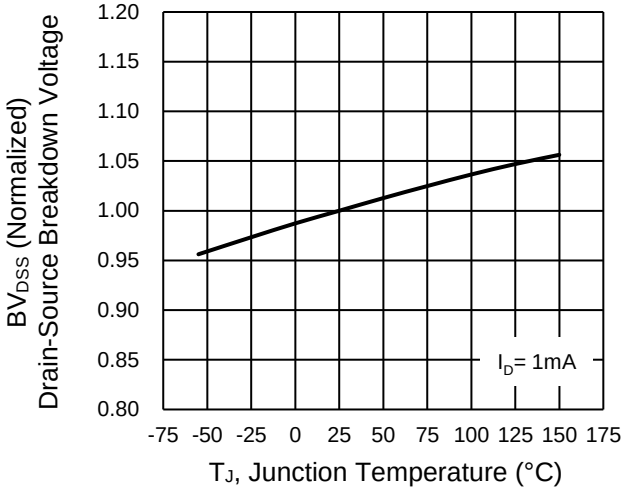
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

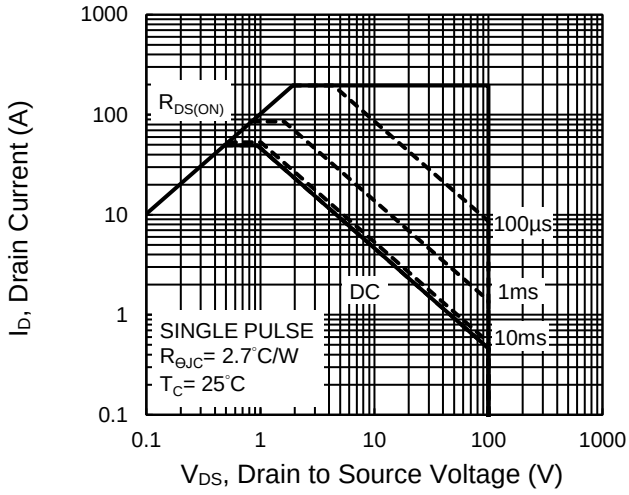
Capacitance vs. Drain-Source Voltage



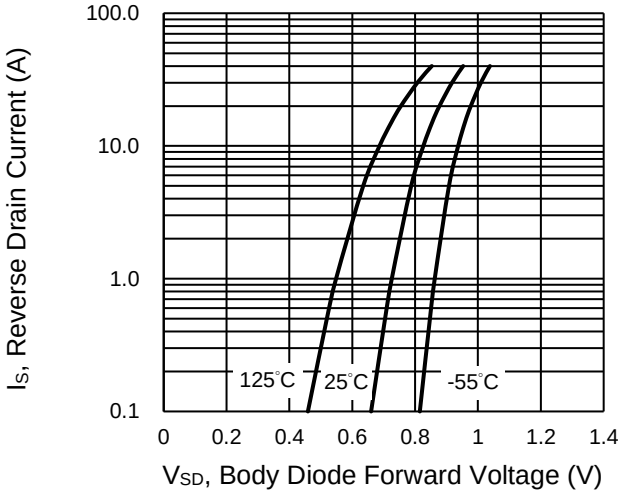
BV_{DSS} vs. Junction Temperature



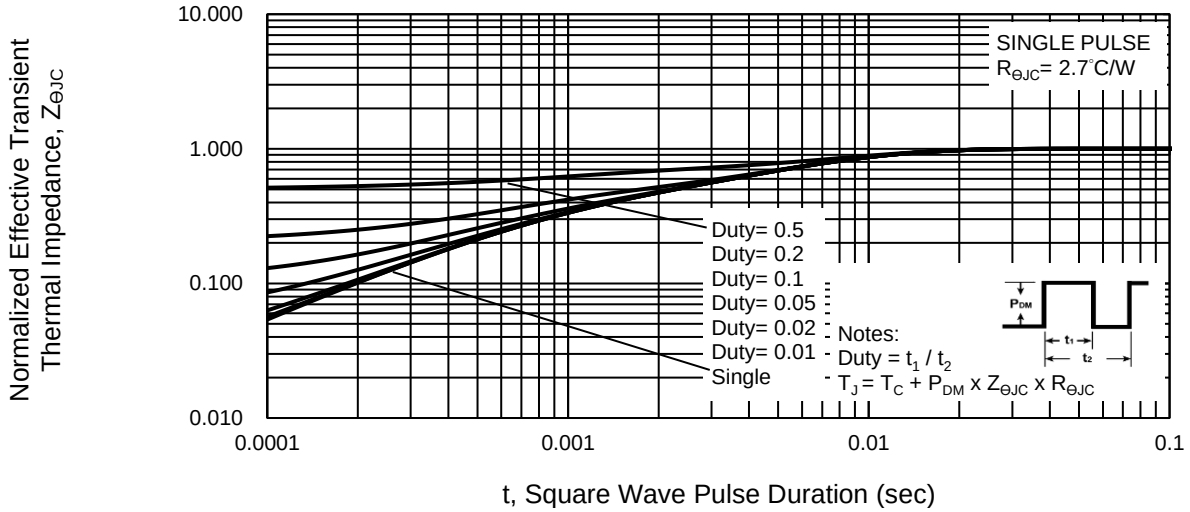
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



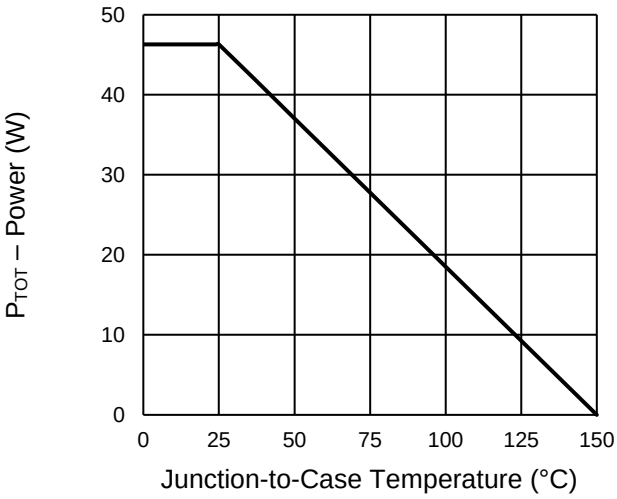
Normalized Thermal Transient Impedance, Junction-to-Case



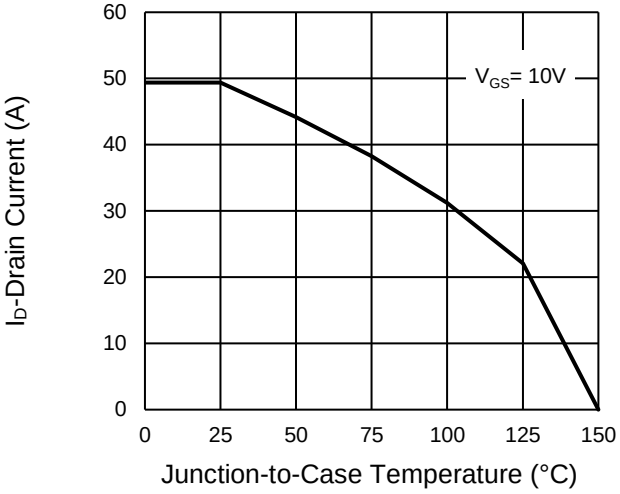
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

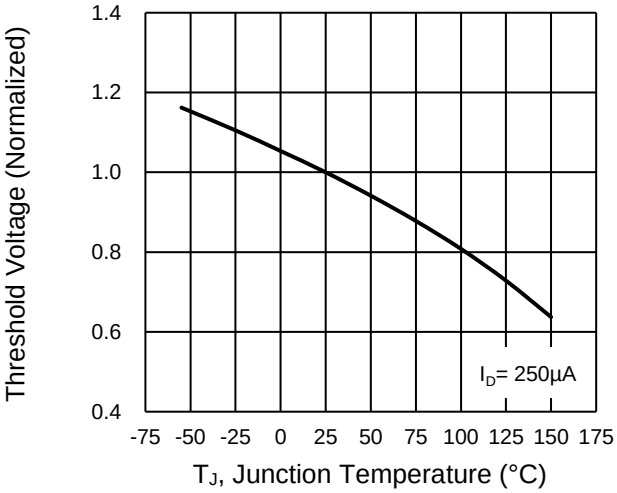
Power Dissipation



Drain Current

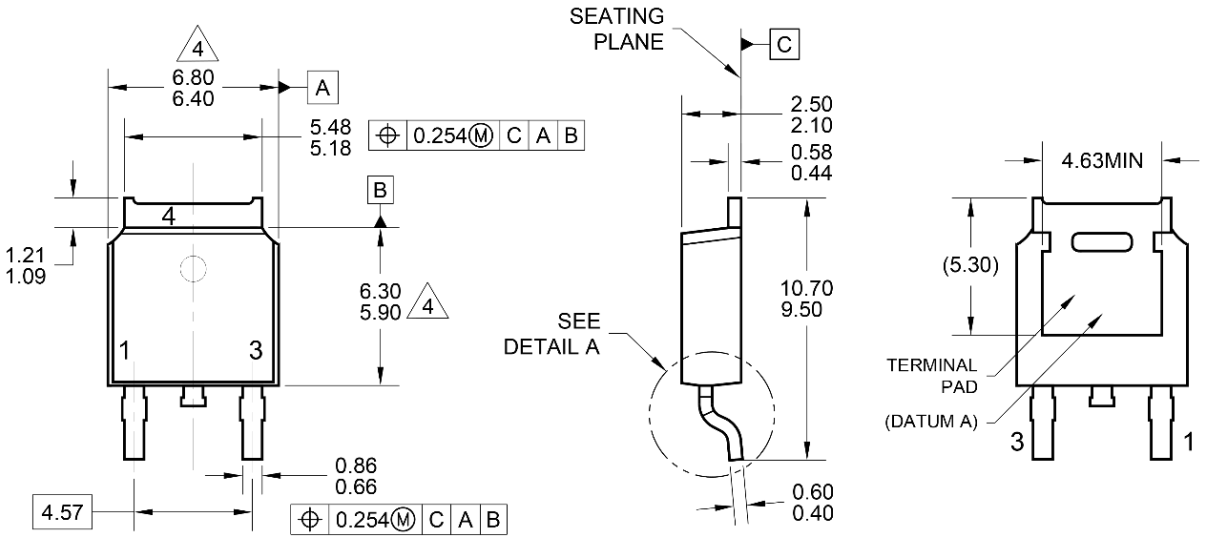


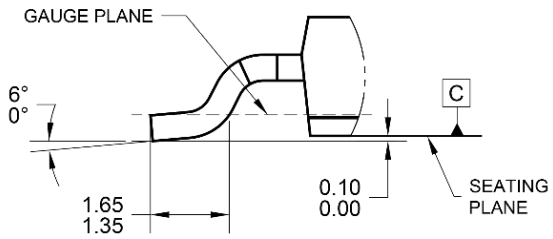
Normalized gate threshold voltage vs Temperature



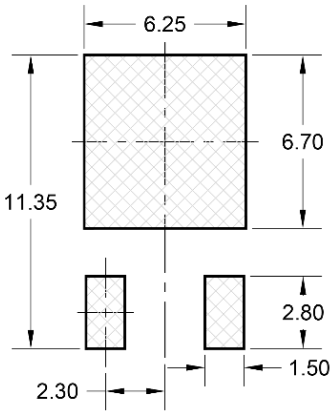
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252_A

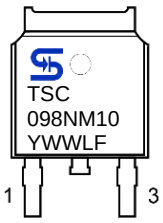




DETAIL A, ROTATED -90°
(SCALE 2:1)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM

098NM10	= Device marking
Y	= Year Code
WW	= Week Code (01~52)
L	= Lot Code (1~9,A~Z)
F	= Factory Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-TO252_A-144 REV A.

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