

MOSFET - Power, Single

N-Channel, μ 8FL

30 V, 7.4 m Ω , 47 A

NVTFS4C10N

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C10NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	30	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	$T_A = 25^\circ\text{C}$	I_D	15.3
			10.8
	$T_A = 100^\circ\text{C}$	P_D	3.0
			1.5
Power Dissipation $R_{\theta JA}$ (Notes 1, 2, 4)	$T_A = 25^\circ\text{C}$	I_D	47
			33
	$T_C = 25^\circ\text{C}$	P_D	28
			14
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3, 4)	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	196
	T_J, T_{stg}		-55 to +175
			$^\circ\text{C}$
Operating Junction and Storage Temperature Range			
Source Current (Body Diode)	I_S	53	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_L = 10.2 \text{ A}, L = 0.5 \text{ mH}$)	E_{AS}	26	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

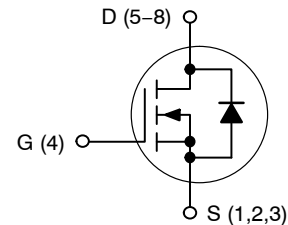
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Notes 1, 3)	$R_{\theta JC}$	5.4	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	50	

1. The entire application environment impacts the thermal resistance values shown; they are not constants and are valid for the specific conditions noted.
2. Surface-mounted on FR4 board using 650 mm², 2 oz. Cu Pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	7.4 m Ω @ 10 V	47 A
	11 m Ω @ 4.5 V	

N-Channel MOSFET

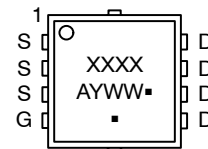


WDFN8
(μ 8FL)
CASE 511AB



WDFNW8
(μ 8FL WF)
CASE 515AN

MARKING DIAGRAM



4C10 = Specific Device Code for NVTFS4C10N

WF10 = Specific Device Code of NVTFS4C10NWF

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NVTFS4C10N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			14.5		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.3		2.2	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-4.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A		5.9	7.4	mΩ
		V _{GS} = 4.5 V, I _D = 15 A		8.8	11	
Forward Transconductance	g _{FS}	V _{DS} = 1.5 V, I _D = 15 A		43		S
Gate Resistance	R _G	T _A = 25°C		1.0		Ω

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V		993		pF
Output Capacitance	C _{OSS}			574		
Reverse Transfer Capacitance	C _{RSS}			163		
Capacitance Ratio	C _{RSS} /C _{ISS}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		0.164		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A		10.1		nC
Threshold Gate Charge	Q _{G(TH)}			1.8		
Gate-to-Source Charge	Q _{GS}			2.6		
Gate-to-Drain Charge	Q _{GD}			6.1		
Gate Plateau Voltage	V _{GP}			3.2		V
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V; I _D = 30 A		19.3		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		9.0		ns
Rise Time	t _r			30		
Turn-Off Delay Time	t _{d(OFF)}			14		
Fall Time	t _f			7.0		
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		6.0		ns
Rise Time	t _r			25		
Turn-Off Delay Time	t _{d(OFF)}			18		
Fall Time	t _f			4.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.80	1.1	V
			T _J = 125°C		0.67		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		23.3			ns
Charge Time	t _a			12.7			
Discharge Time	t _b			10.6			
Reverse Recovery Charge	Q _{RR}			8.3			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

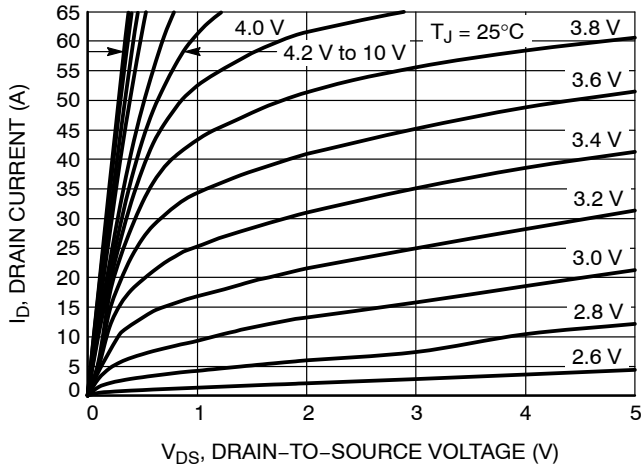


Figure 1. On-Region Characteristics

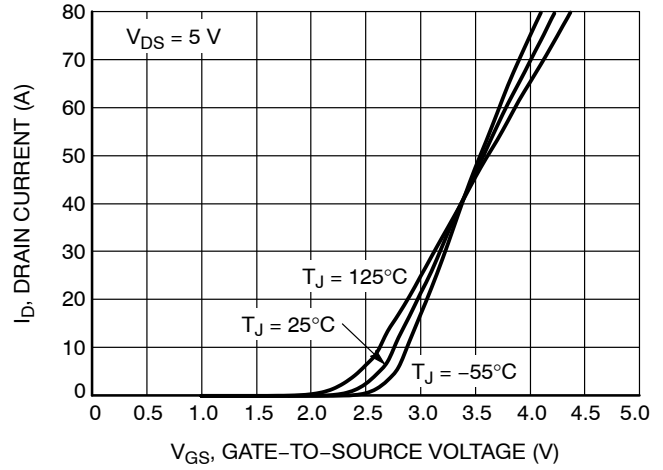


Figure 2. Transfer Characteristics

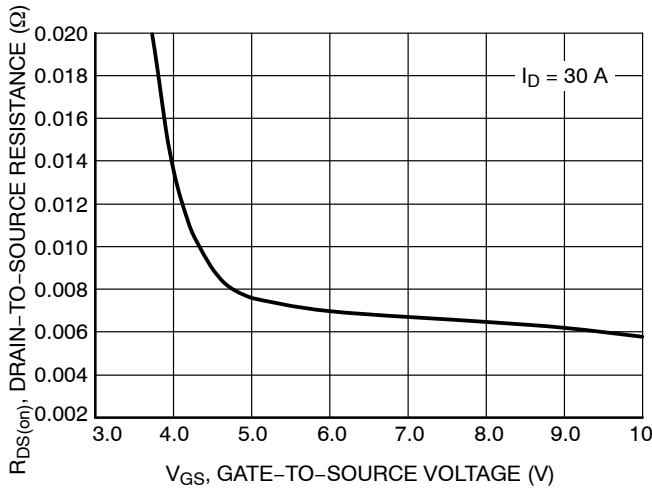


Figure 3. On-Resistance vs. V_{GS}

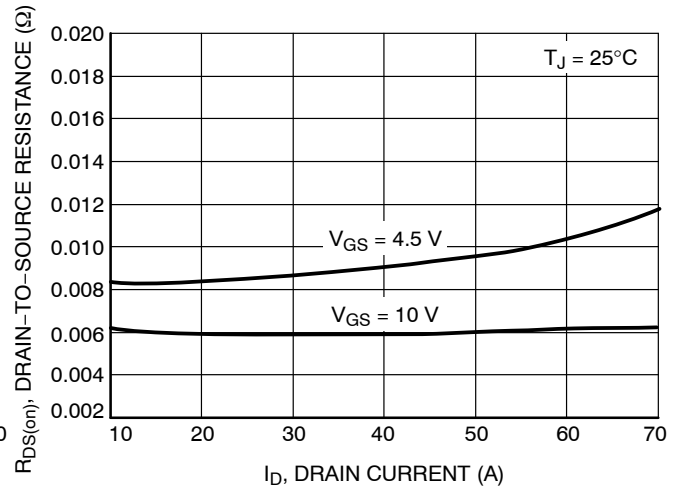


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

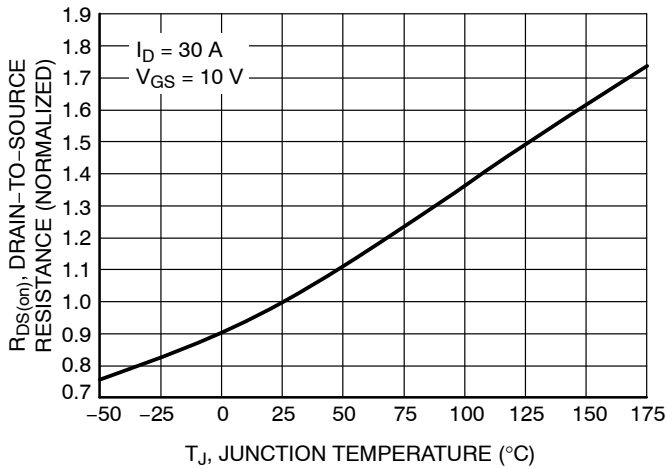


Figure 5. On-Resistance Variation with Temperature

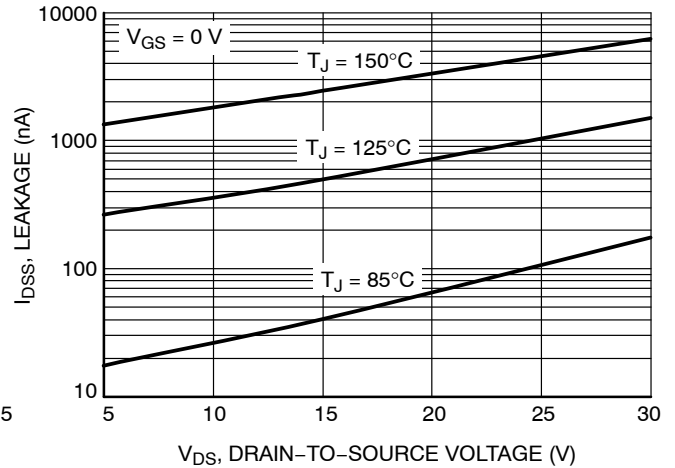


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTFS4C10N

TYPICAL CHARACTERISTICS

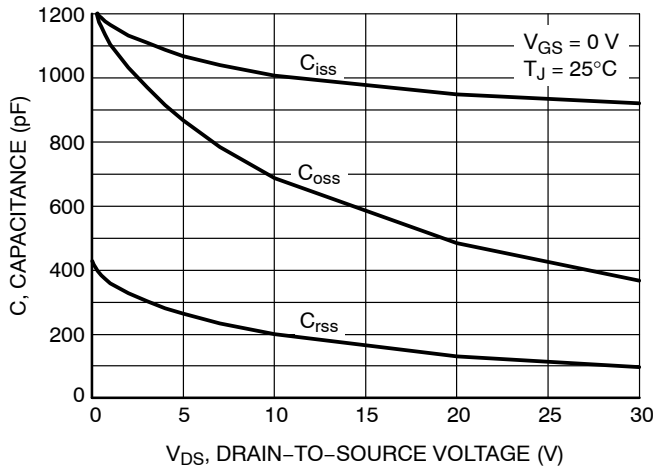


Figure 7. Capacitance Variation

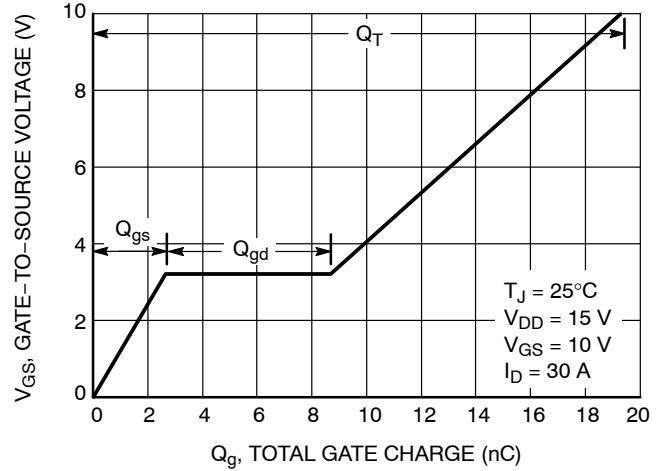


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

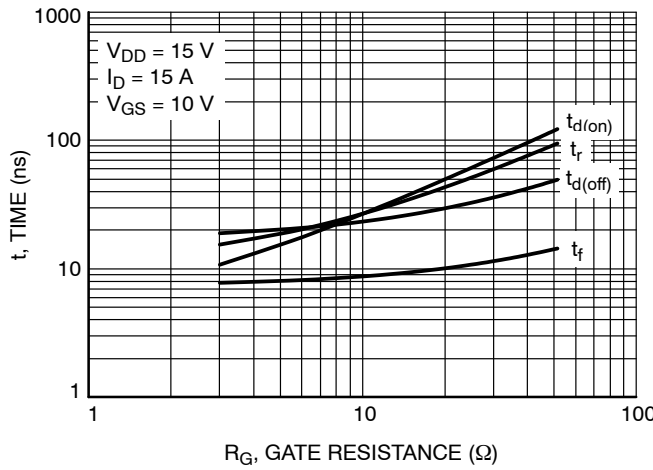


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

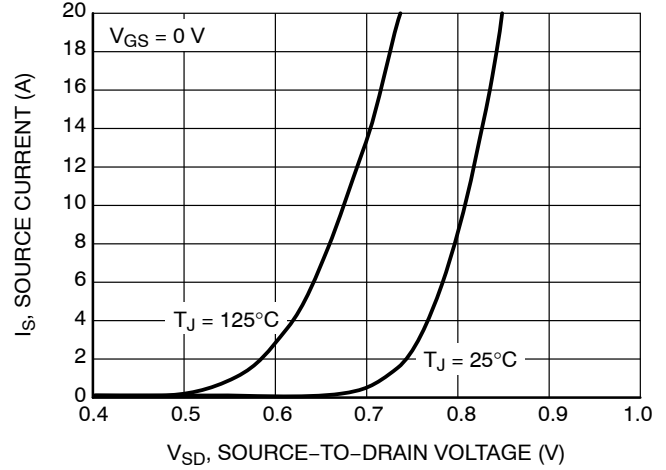


Figure 10. Diode Forward Voltage vs. Current

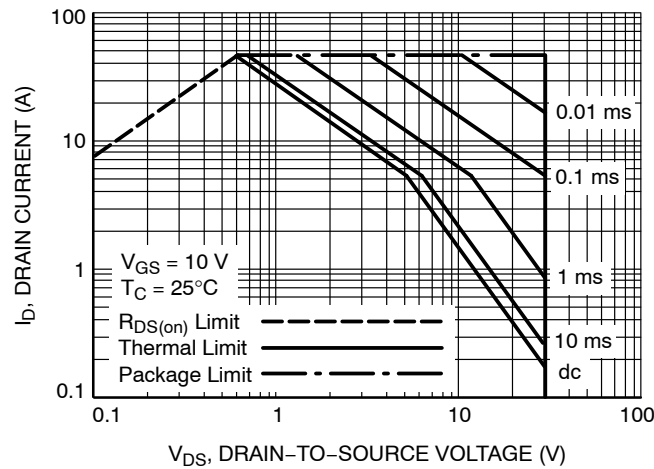


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NVTFS4C10N

TYPICAL CHARACTERISTICS

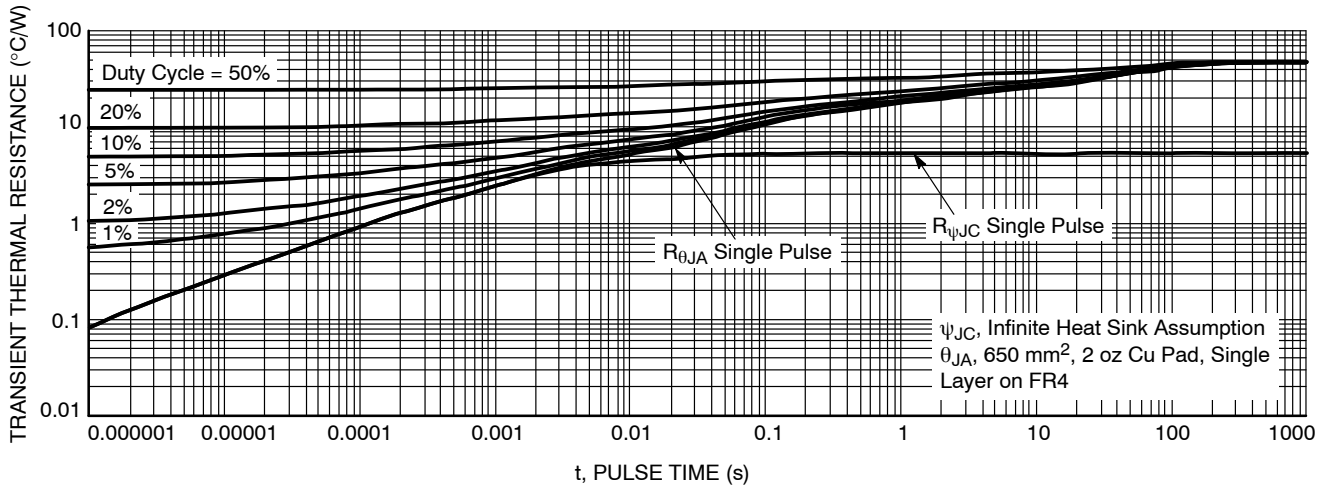


Figure 12. Thermal Response

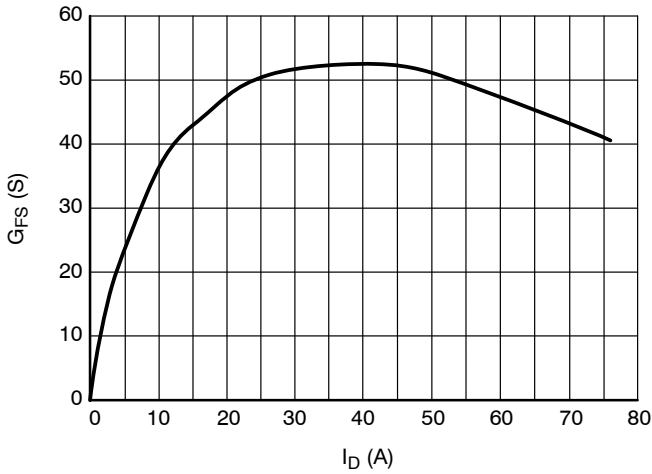


Figure 13. G_{FS} vs. I_D

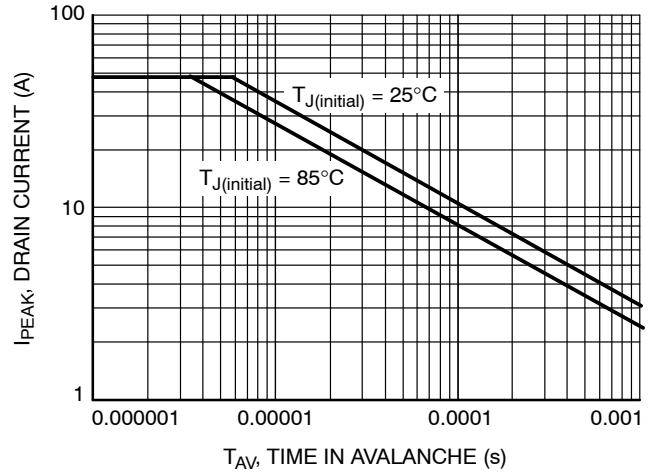


Figure 14. Avalanche Characteristics

ORDERING INFORMATION

Device	Package	Shipping [†]
NVTFS4C10NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C10NWFTAG	WDFNW8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

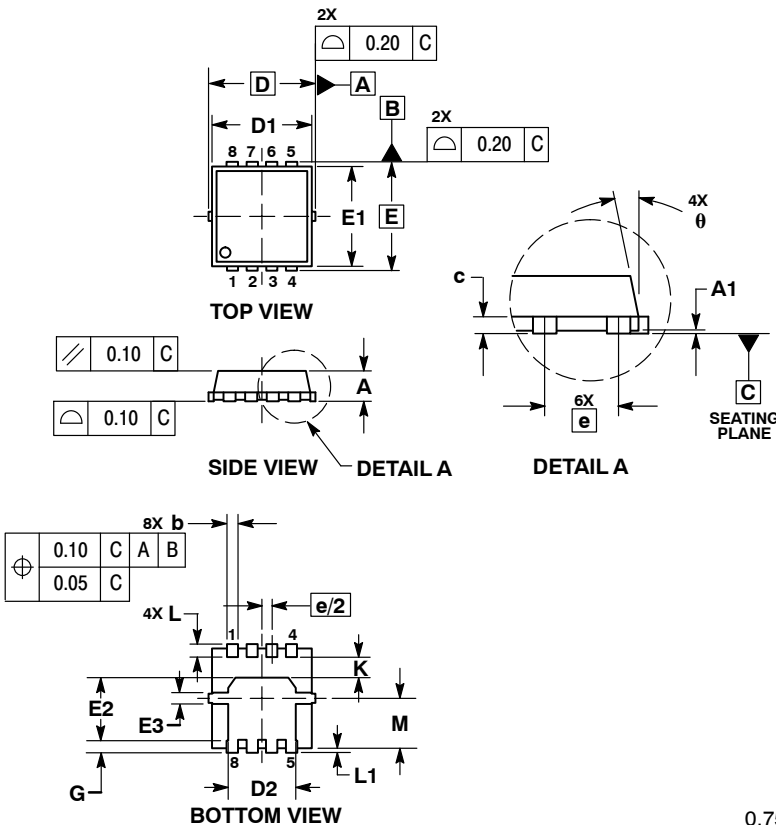
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

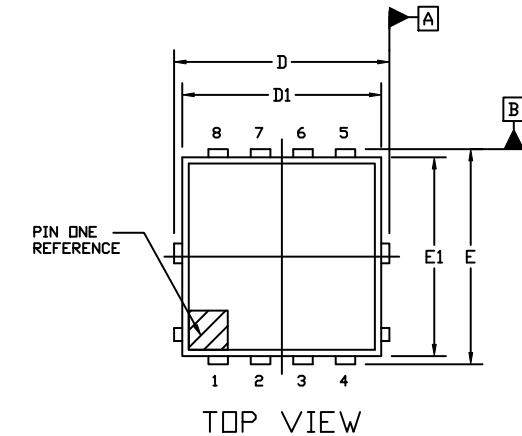
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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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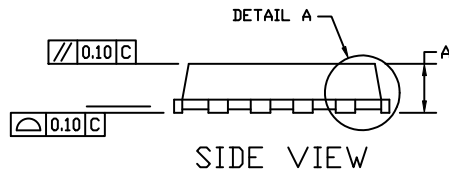


WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)
CASE 515AN
ISSUE O

DATE 25 AUG 2020



TOP VIEW



SIDE VIEW



DETAIL A

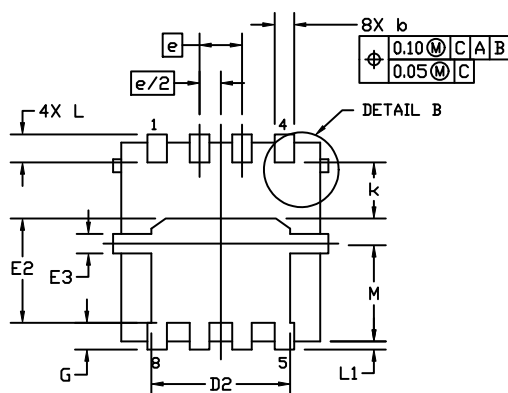


DETAIL B

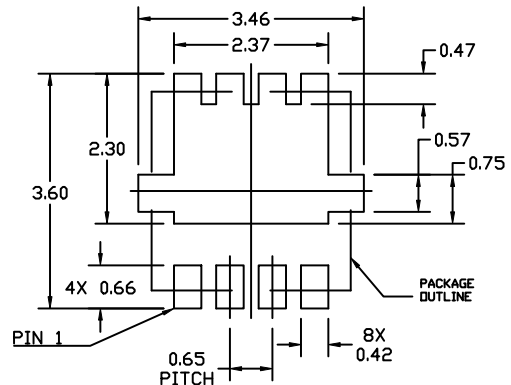
NOTES:

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3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



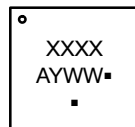
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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