



PXN040-100QS

N-channel 100 V, 40 mOhm, standard level Trench MOSFET in MLPAK33

5 November 2024

Product data sheet

1. General description

General purpose MOSFET for standard applications, 17 A, standard level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Standard level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

4. Quick reference data

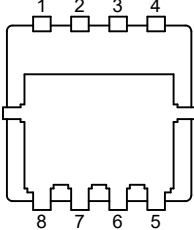
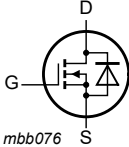
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	17	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	21	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9	-	36	40	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 11 ; Fig. 12	-	1.5	-	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 5\text{ A}$; $dI_S/dt = -100\text{ A/μs}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15	[1]	19	-	nC

[1] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN040-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN040-100QS	7AS

8. Limiting values

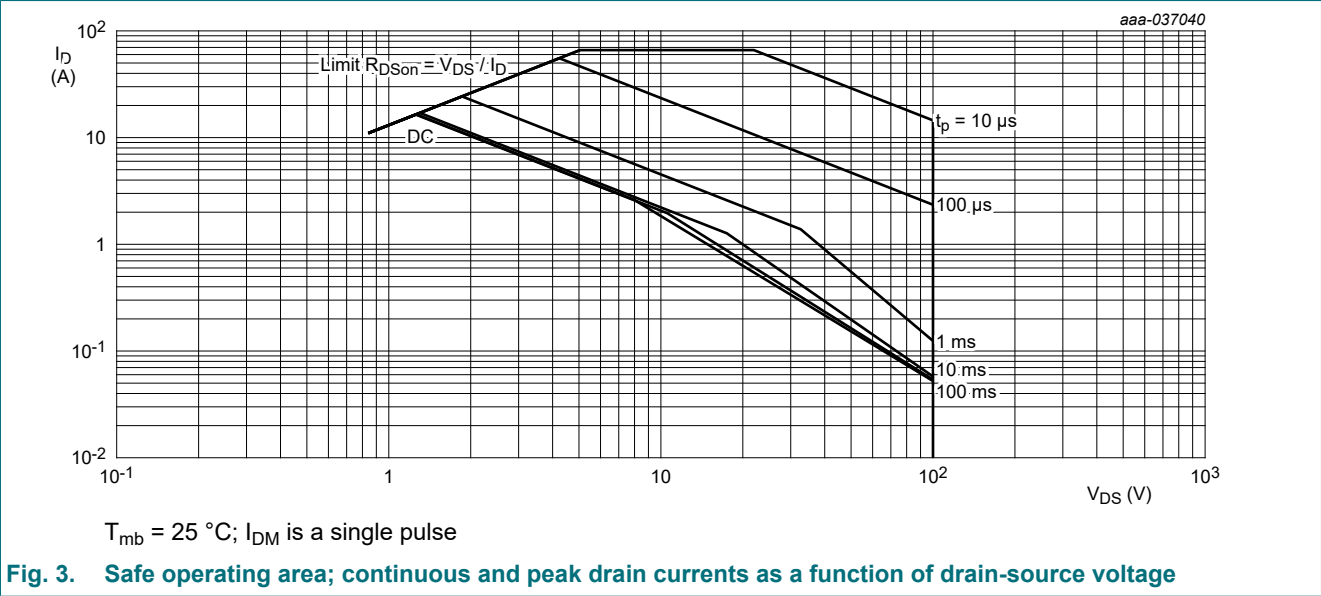
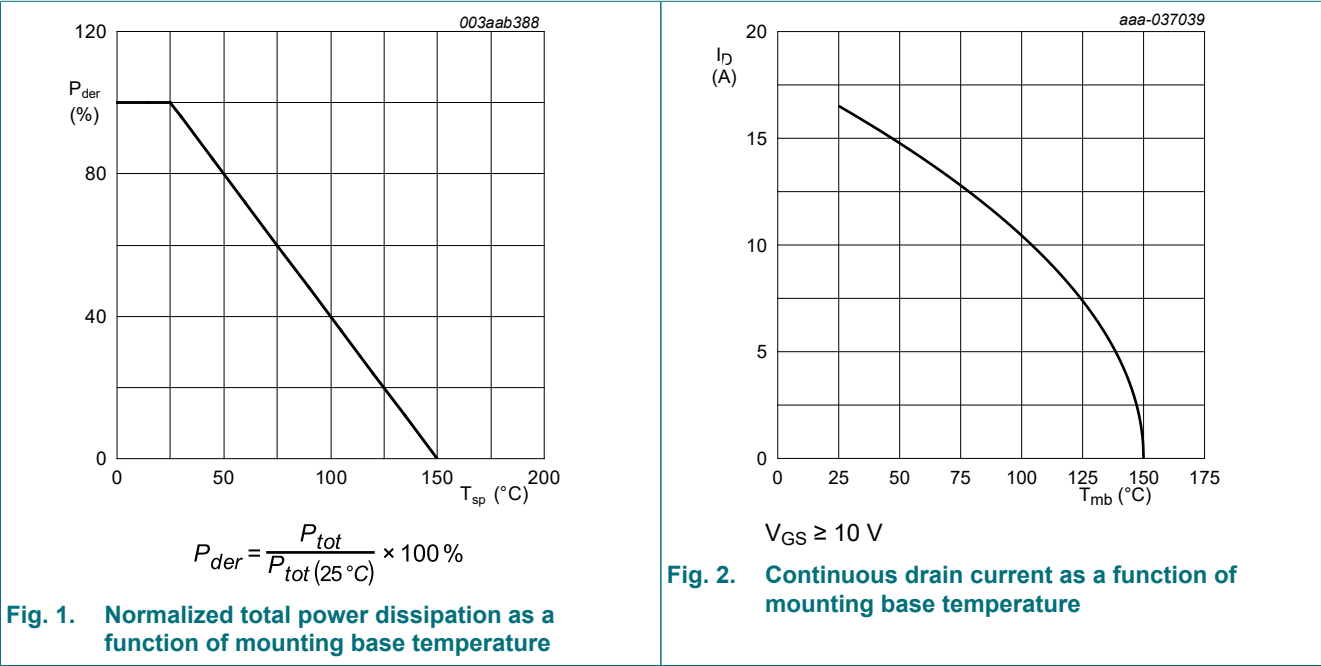
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	21	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	17	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	10	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	66	A
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	17	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	66	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 9.5\text{ A}$; $V_{sup} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped	[1]	-	9	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$	[1]	-	9.5	A

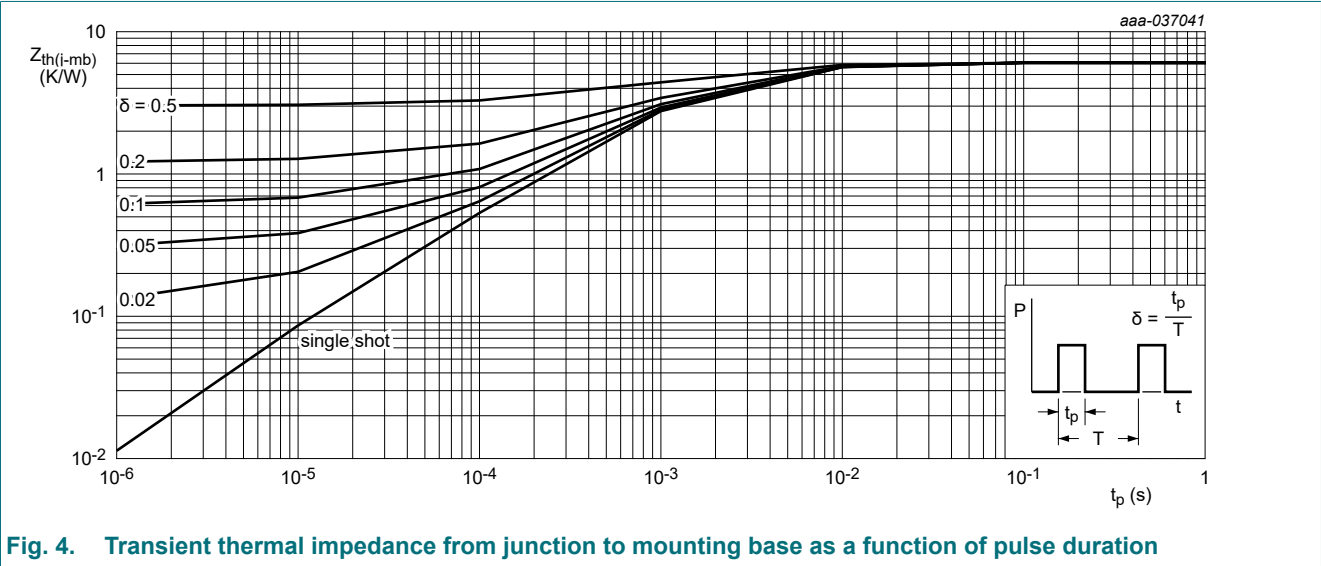
[1] Protected by 100% test



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	5	6	K/W



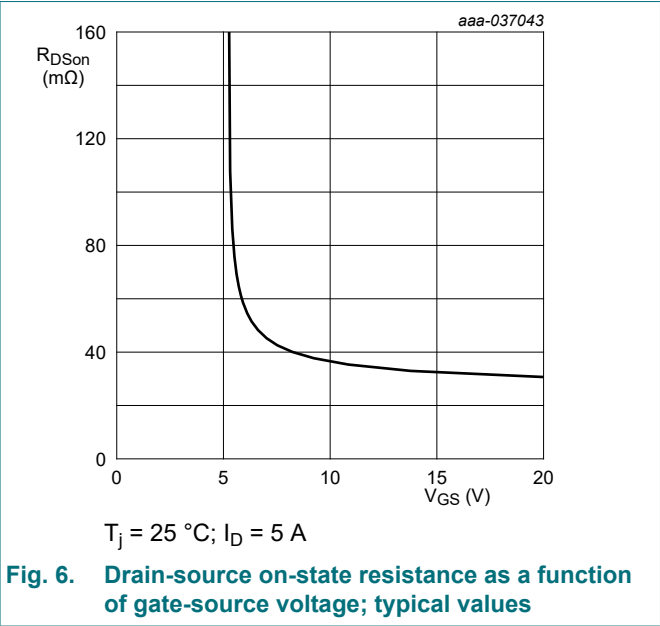
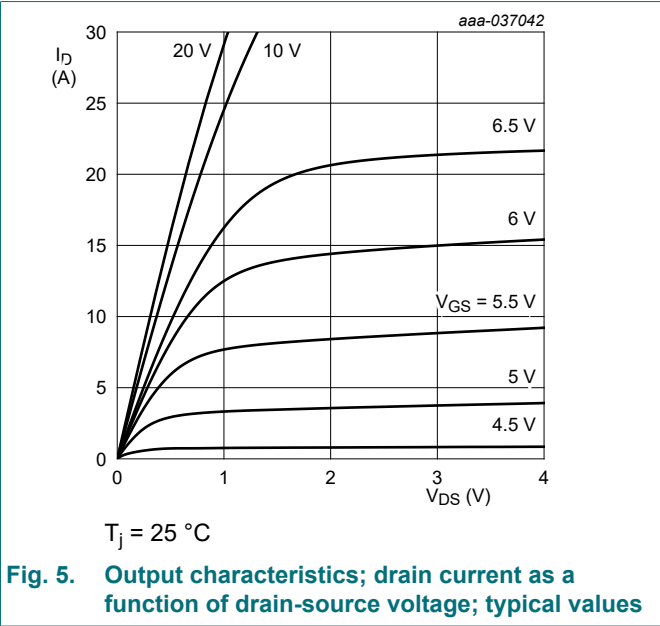
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 8}$	2	3	4	V
		$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 150 \text{ }^\circ C$	-	1.9	-	V
		$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.5	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-8.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	3	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}$	-	36	40	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ C; \text{ Fig. 10}$	-	-	76	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	0.6	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11; Fig. 12		-	6.6	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	5.5	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11; Fig. 12		-	2.3	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	1.3	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	1	-	nC
Q _{GD}	gate-drain charge			-	1.5	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 11; Fig. 12		-	5.2	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 13		-	351	-	pF
C _{oss}	output capacitance			-	114	-	pF
C _{rss}	reverse transfer capacitance			-	6	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 10 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	3.3	-	ns
t _r	rise time			-	2.1	-	ns
t _{d(off)}	turn-off delay time			-	5.6	-	ns
t _f	fall time			-	4.4	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz; T _j = 25 °C		-	8.8	-	nC
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 14		-	0.86	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 15		-	28	-	ns
Q _r	recovered charge		[1]	-	19	-	nC

[1] includes capacitive recovery



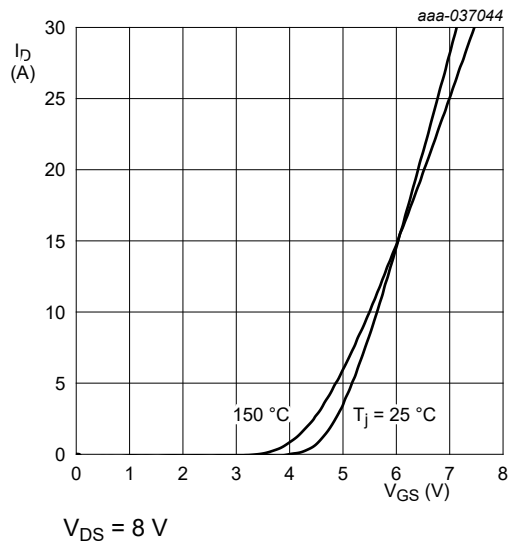


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

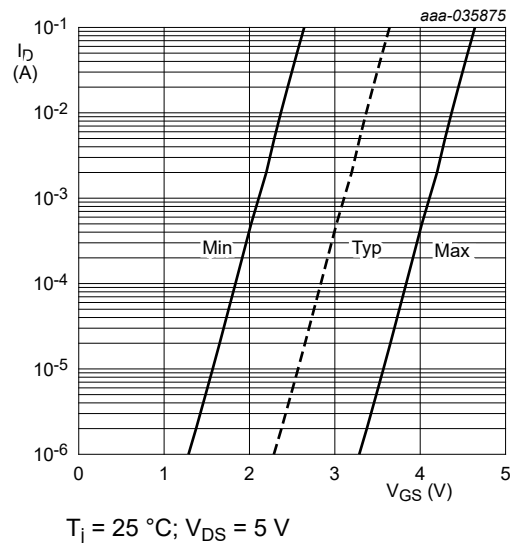


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

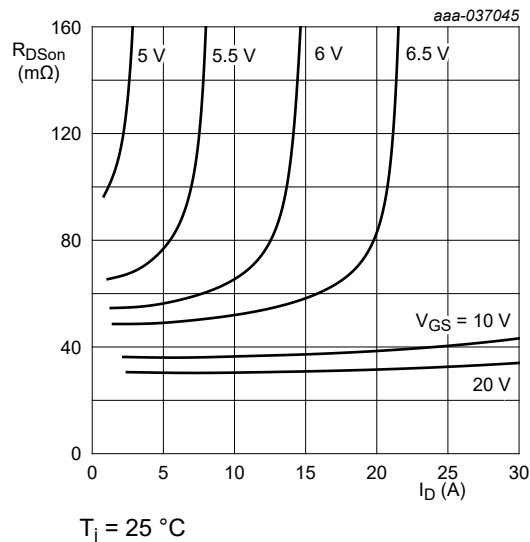


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

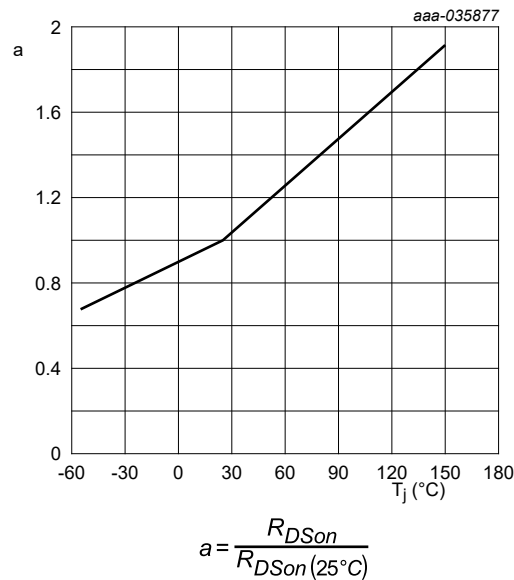


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

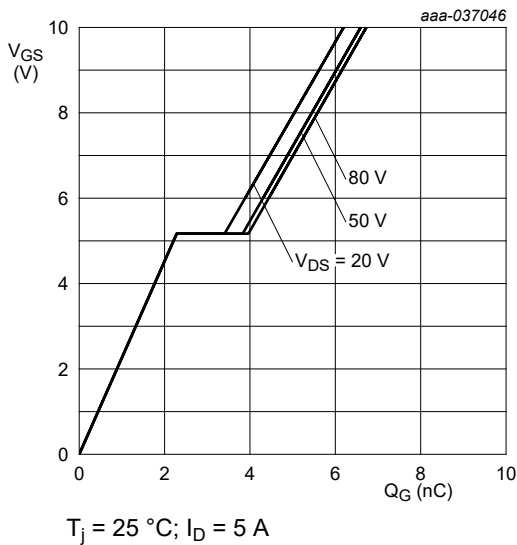


Fig. 11. Gate-source voltage as a function of gate charge; typical values

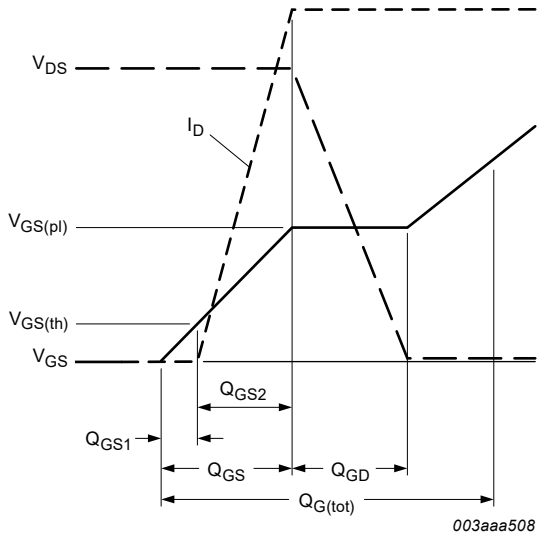


Fig. 12. Gate charge waveform definitions

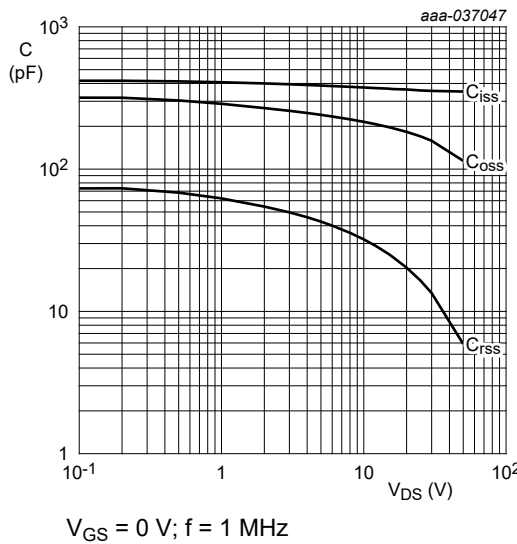


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

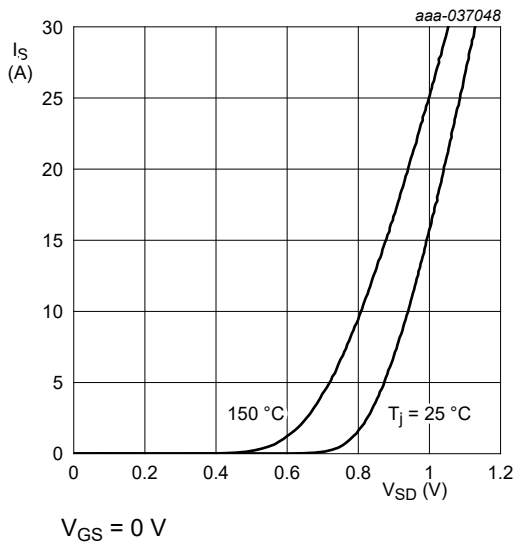


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

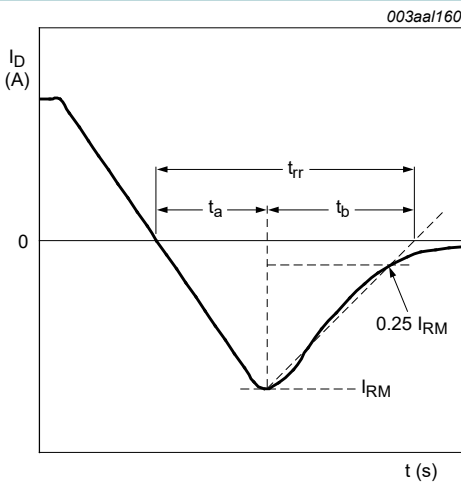


Fig. 15. Reverse recovery timing definition

11. Package outline

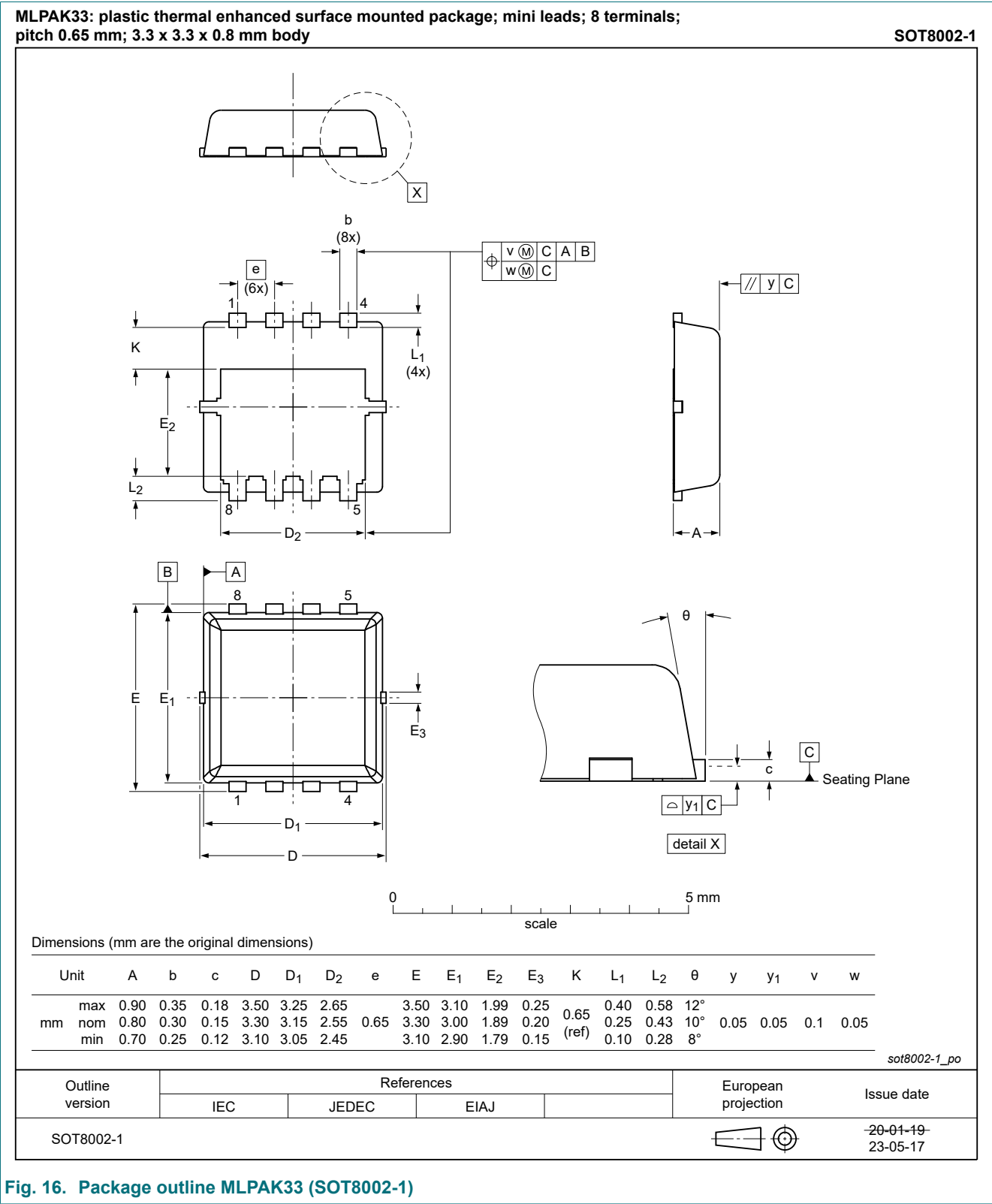


Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

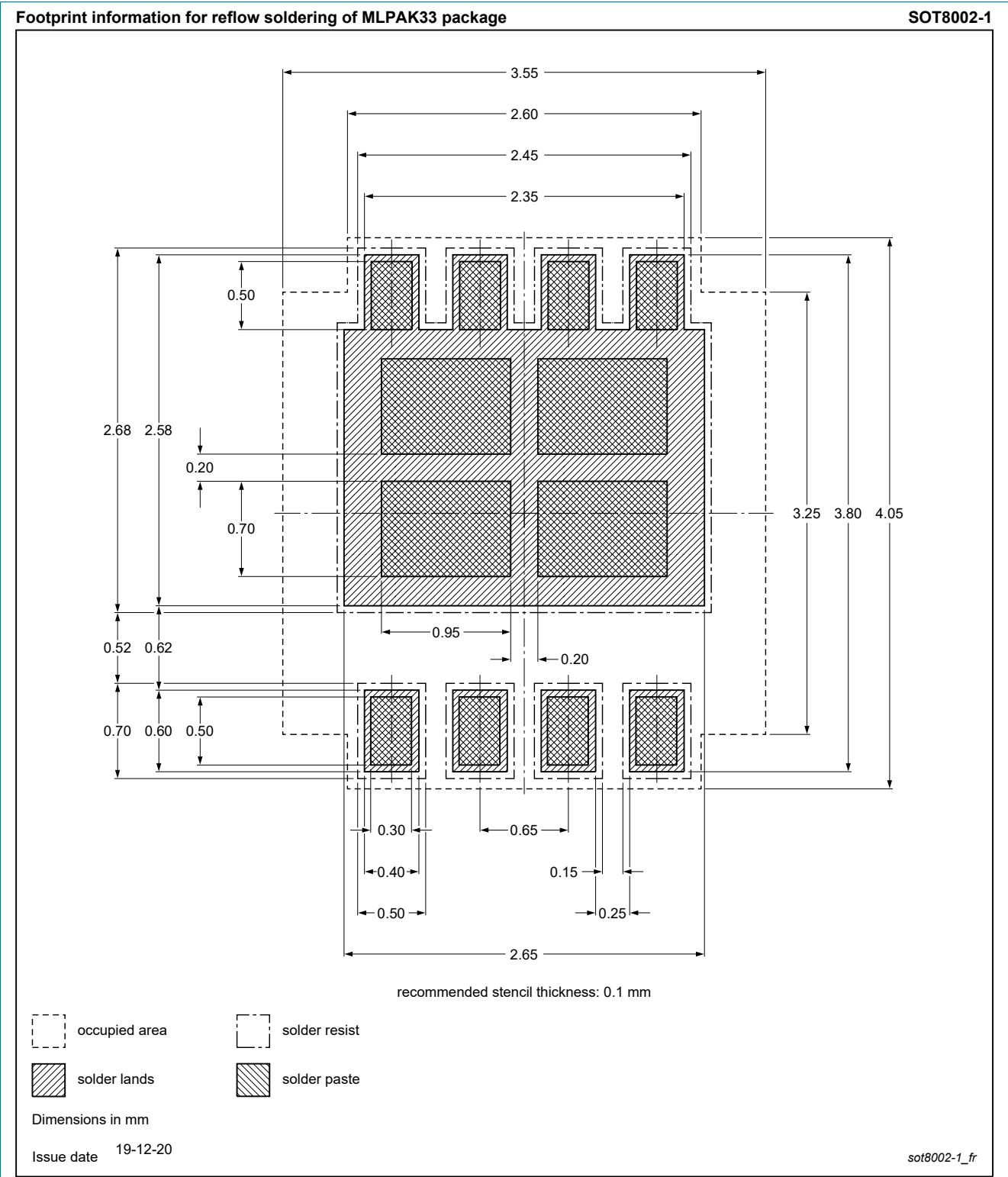


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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