

# MOSFET – N-Channel, Logic Level, POWER trench<sup>®</sup>

60 V, 80 A, 6 mΩ

## FDP5800

### Description

This N-Channel MOSFET is produced using onsemi's advanced POWER trench process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

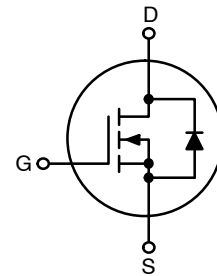
### Features

- $R_{DS(on)} = 4.6 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- Low Gate Charge
- High Power and Current Handling Capability
- RoHS Compliant

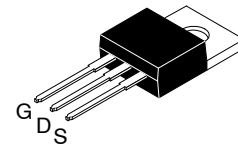
### Applications

- Power Tools
- Motor Drives and Uninterruptible Power Supplies
- Synchronous Rectification
- Battery Protection Circuit

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
60 V	6 mΩ @ 10 V	80 A

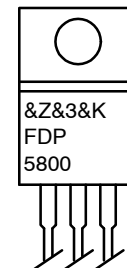


N-Channel



TO-220-3LD  
CASE 340AT

### MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digit Date Code
&K	= 2-Digits Lot Run Code
FDP5800	= Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
FDP5800	TO-220-3LD	800 Units / Tube

# FDP5800

## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		FDP5800	Unit
$V_{DS}$	Drain–Source Voltage		60	V
$V_{GS}$	Gate–Source Voltage		$\pm 20$	V
$I_D$	Drain Current	– Continuous ( $T_C = 25^\circ\text{C}$ )	80	A
		– Continuous ( $T_C = 100^\circ\text{C}$ )	80*	
		– Continuous ( $T_A = 25^\circ\text{C}$ )	14	
$I_{DM}$	Drain Current	– Pulsed	320	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 1)		652	mJ
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	242	W
		–Derate above $25^\circ\text{C}$	1.61	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		–55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

\*Drain current limited by package.

1.  $L = 1\text{ mH}$ ,  $I_{AS} = 36\text{ A}$ ,  $V_{DD} = 54\text{ V}$ ,  $V_{GS} = 10\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Parameter	FDP5800	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.62	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

# FDP5800

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	I <sub>D</sub> = 250 $\mu$ A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C	60	–	–	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V	–	–	1	$\mu$ A
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150°C	–	–	500	
I <sub>GSS</sub>	Gate–Body Leakage Current, Forward	V <sub>GS</sub> = $\pm$ 20 V, V <sub>DS</sub> = 0 V	–	–	$\pm$ 100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 $\mu$ A	1.0	–	2.5	V
R <sub>DS(on)</sub>	Static Drain–Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A	–	4.6	6.0	m $\Omega$
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 80 A	–	5.9	7.2	
		V <sub>GS</sub> = 5 V, I <sub>D</sub> = 80 A	–	5.6	7.0	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A, T <sub>J</sub> = 175°C	–	10.4	12.6	

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	6890	9160	pF
C <sub>oss</sub>	Output Capacitance		–	750	1000	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	295	445	pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 0.5 V, f = 1 MHz	–	1.2	–	$\Omega$
Q <sub>g(TOT)</sub>	Total Gate Charge at 10 V	V <sub>GS</sub> = 0 V to 10 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 80 A, I <sub>g</sub> = 1 mA	–	112	145	nC
Q <sub>g(TH)</sub>	Total Gate Charge at 5 V	V <sub>GS</sub> = 0 V to 5 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 80 A, I <sub>g</sub> = 1 mA	–	58	–	nC
Q <sub>g(TH)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 V to 1 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 80 A, I <sub>g</sub> = 1 mA	–	7.0	–	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 80 A, I <sub>g</sub> = 1 mA	–	23	–	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau		–	13	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	18	–	nC

### SWITCHING CHARACTERISTICS (V<sub>GS</sub> = 10 V)

t <sub>ON</sub>	Turn–On Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 1.5 $\Omega$	–	37	85	ns
t <sub>d(on)</sub>	Turn–On Delay Time		–	18	46	ns
t <sub>r</sub>	Turn–On Rise Time		–	19	47	ns
t <sub>d(off)</sub>	Turn–Off Delay Time		–	55	120	ns
t <sub>f</sub>	Turn–Off Fall Time		–	9	28	ns
t <sub>OFF</sub>	Turn–Off Time		–	64	138	ns

### DRAIN–SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 80 A	–	–	1.25	V
		V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 40 A	–	–	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 60 A, dI <sub>F</sub> /dt = 100 A/ $\mu$ s	–	58	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	106	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

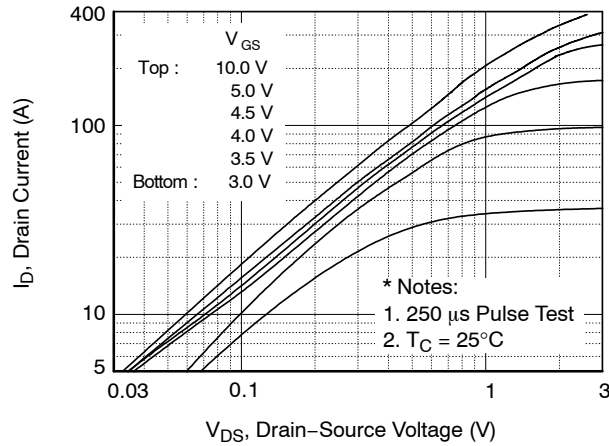


Figure 1. On-Region Characteristics

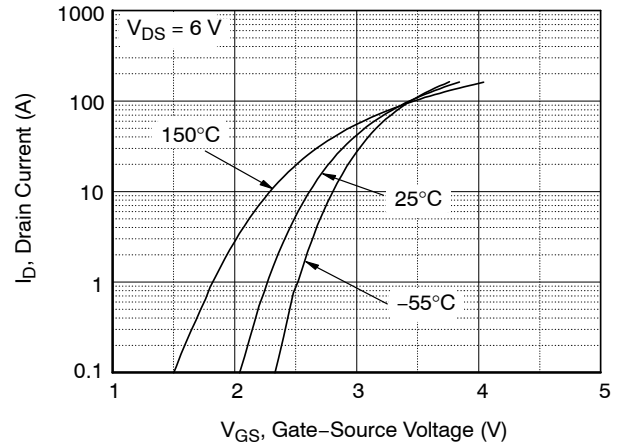


Figure 2. Transfer Characteristics

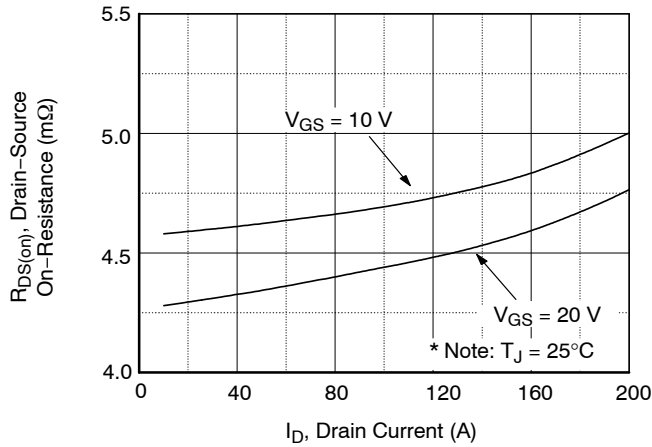


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

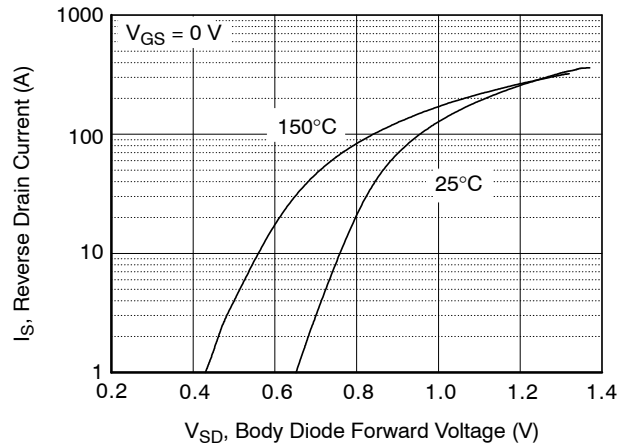


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

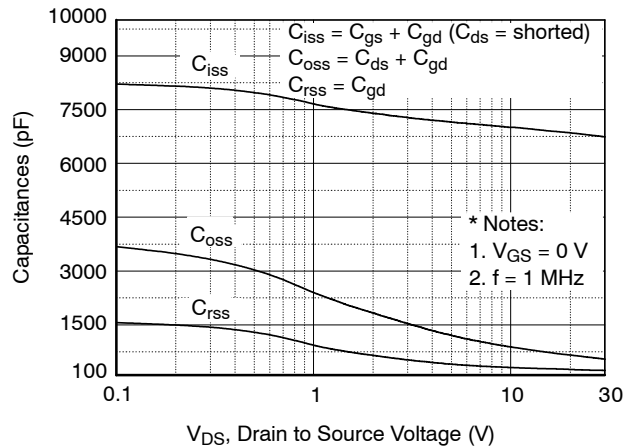


Figure 5. Capacitance Characteristics

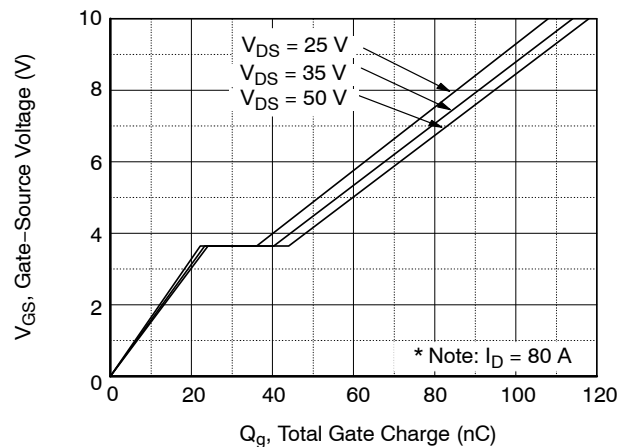


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

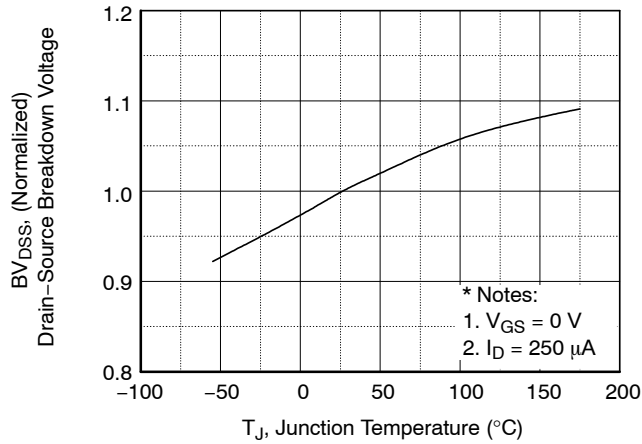


Figure 7. Breakdown Voltage Variation vs. Temperature

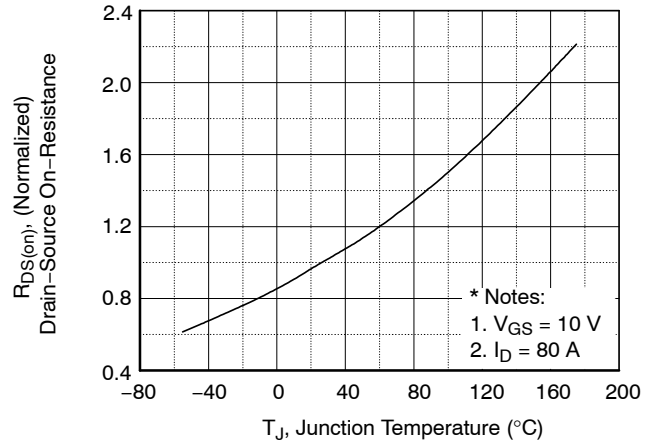


Figure 8. On-Resistance Variation vs. Temperature

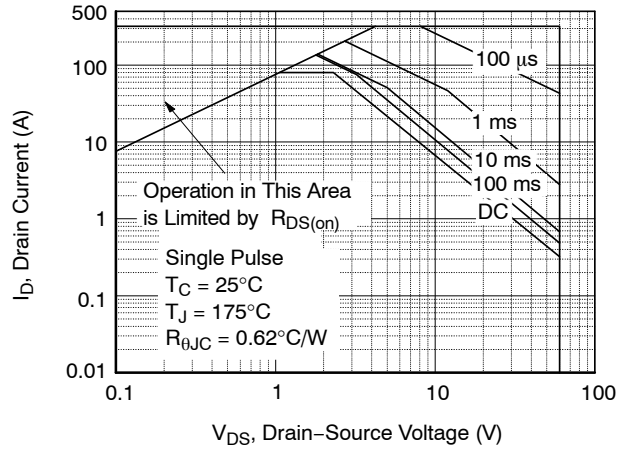


Figure 9. Maximum Safe Operating Area

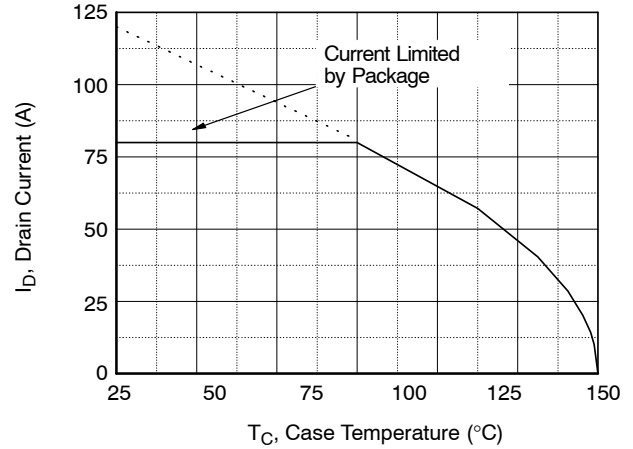


Figure 10. Maximum Drain Current vs. Case Temperature

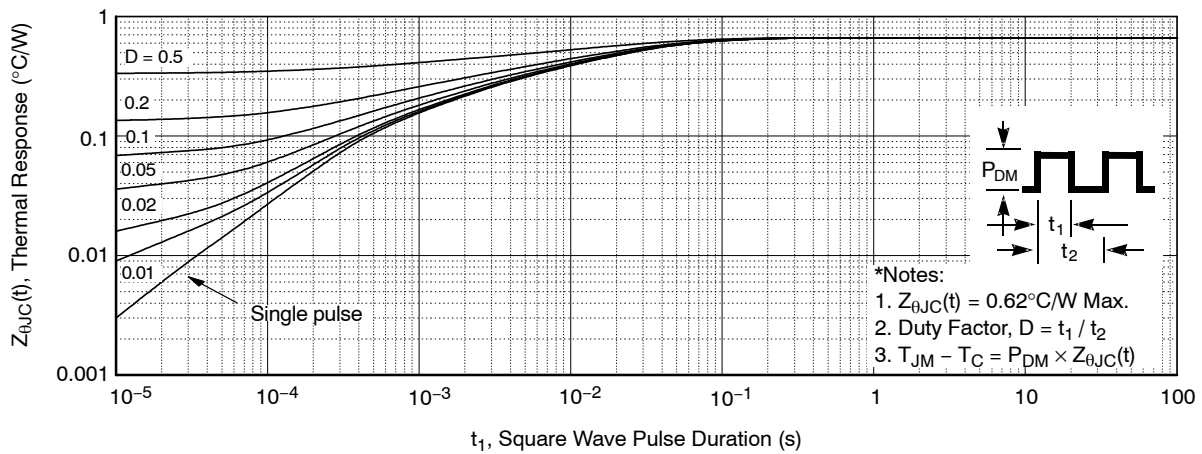


Figure 11. Transient Thermal Response Curve

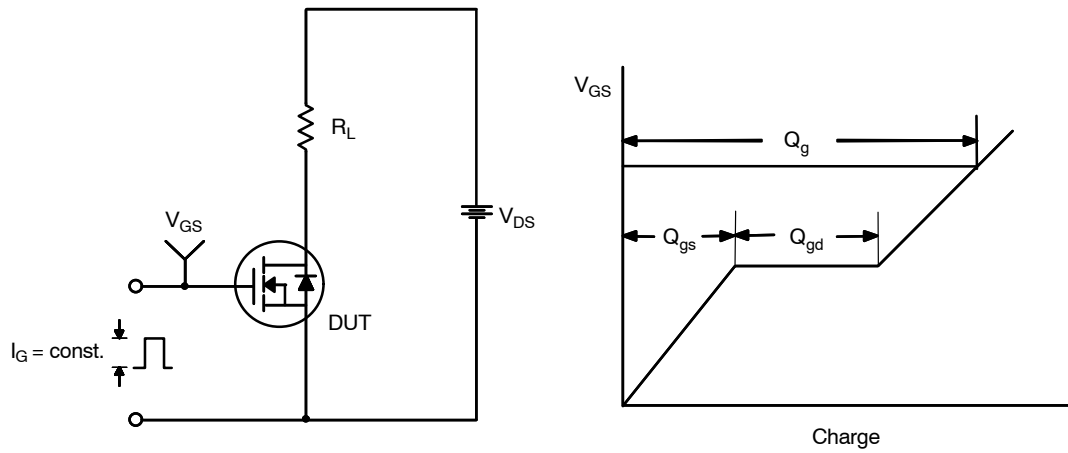


Figure 12. Gate Charge Test Circuit & Waveform

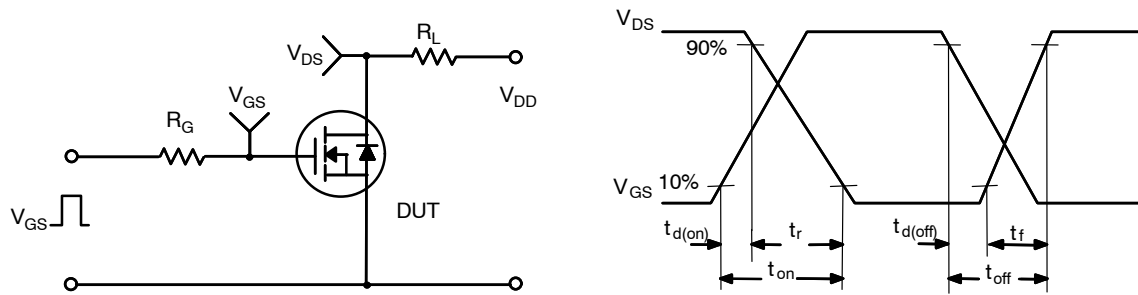


Figure 13. Resistive Switching Test Circuit & Waveforms

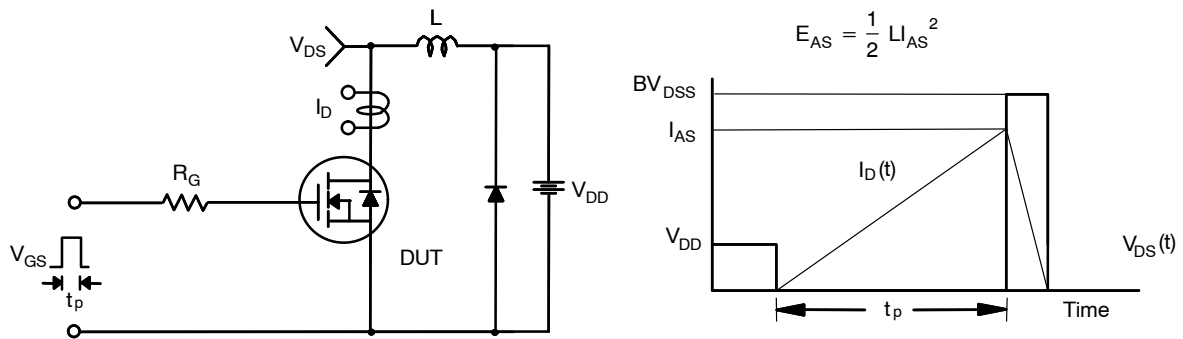
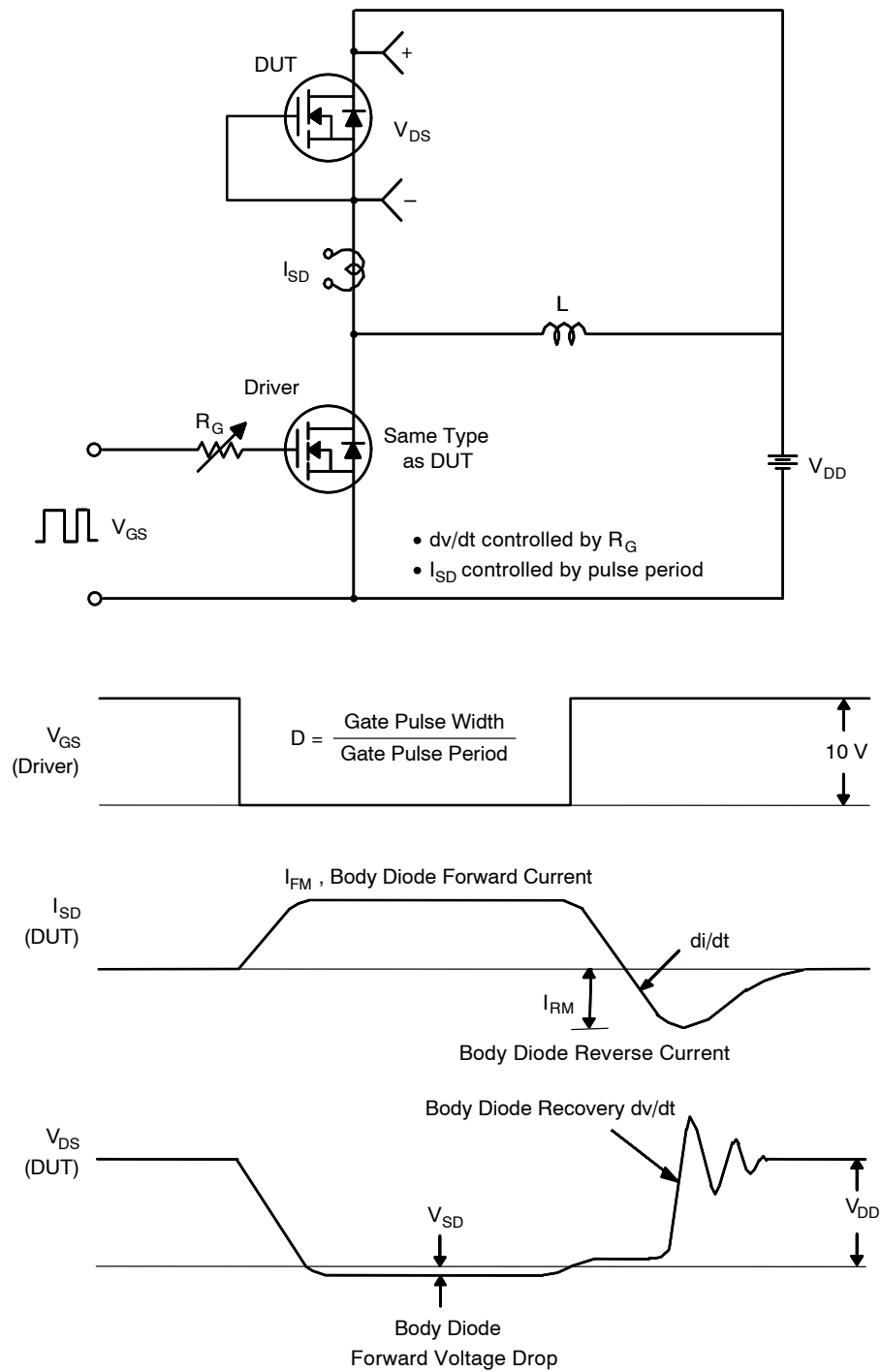
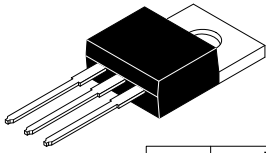


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**



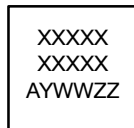
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CASE 340AT  
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

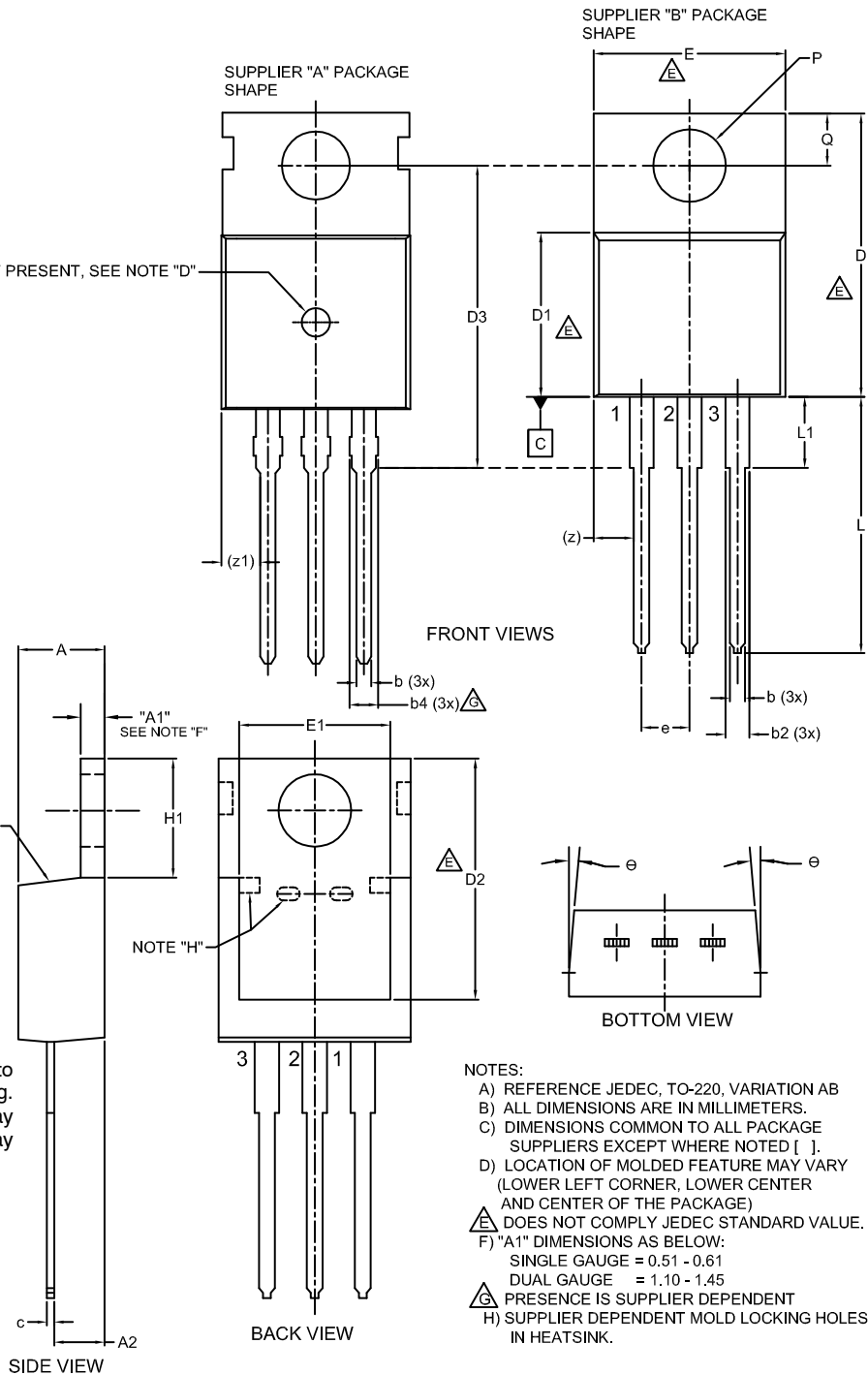
IF PRESENT, SEE NOTE "D"

GENERIC  
MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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