

# N-Channel Enhancement Mode Field Effect Transistor

## 2N7002T

### Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- This Device is Pb-Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	60	V
Drain-Gate Voltage $R_{GS} \leq 1.0 \text{ M}\Omega$	$V_{DGR}$	60	V
Gate-Source Voltage Continuous Pulsed	$V_{GSS}$	$\pm 20$ $\pm 40$	V
Gate-Source Voltage Continuous Continuous at $100^\circ\text{C}$ Pulsed	$I_D$	115 73 800	mA
Junction Temperature Range	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 to +150	$^\circ\text{C}$

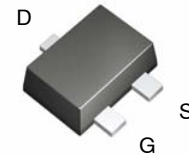
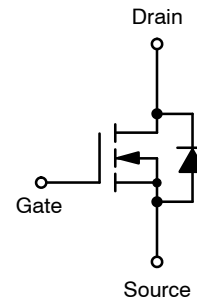
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Max	Unit
Total Device Dissipation Derating above $T_A = 25^\circ\text{C}$	$P_D$	200 1.6	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	625	$^\circ\text{C/W}$

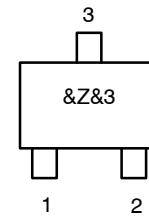
1. Device mounted on FR-4 PCB, 1 inch  $\times$  0.85 inch  $\times$  0.062 inch. Minimum land pad size.

### SIMPLIFIED SCHEMATIC



SOT-523FL  
CASE 419BG

### MARKING DIAGRAM



&Z = Assembly location  
&3 = Data code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
2N7002T	SOT-523FL (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

## 2N7002T

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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#### OFF CHARACTERISTICS (Note 2)

Drain–Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	60	78	–	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 60\text{ V}, V_{GS} = 0\text{ V}$	–	0.001	1.0	$\mu\text{A}$
		$V_{GS} = 60\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125^\circ\text{C}$	–	7	500	$\mu\text{A}$
Gate–Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	–	0.2	$\pm 10$	nA

#### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.76	2.0	V
Static Drain–Source On–Resistance	$R_{DS(on)}$	$V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$	–	1.6	7.5	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$	–	–	2.0	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A},$ $T_J = 125^\circ\text{C}$	–	2.53	13.5	$\Omega$
On–State Drain Current	$I_{D(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	0.5	1.43	–	A
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ A}$	80	356.5	–	mS

#### DYNAMIC CHARACTERISTICS

Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	–	37.8	50	pF
Output Capacitance	$C_{OSS}$		–	12.4	25	
Reverse Transfer Capacitance	$C_{RSS}$		–	6.5	7.0	

#### SWITCHING CHARACTERISTICS

Turn–On Delay Time	$t_{D(on)}$	$V_{DD} = 30\text{ V}, I_D = 0.2\text{ A},$ $V_{GEN} = 10\text{ V}, R_L = 150\text{ }\Omega,$ $R_{GEN} = 25\text{ }\Omega$	–	5.85	20	ns
Turn–Off Delay Time	$t_{D(off)}$		–	12.5	20	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self–heating effect.

## TYPICAL PERFORMANCE CHARACTERISTICS

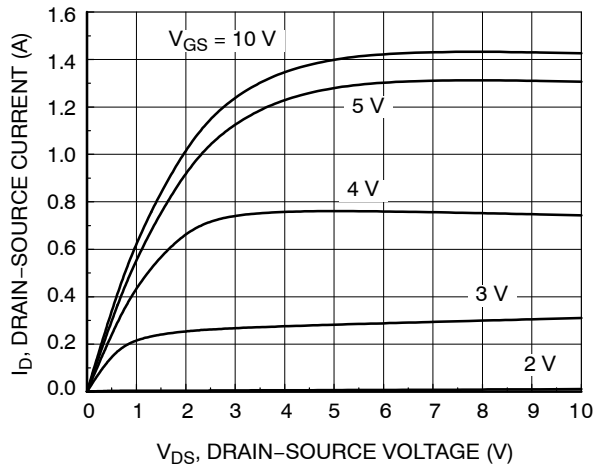


Figure 1. On-Region Characteristics

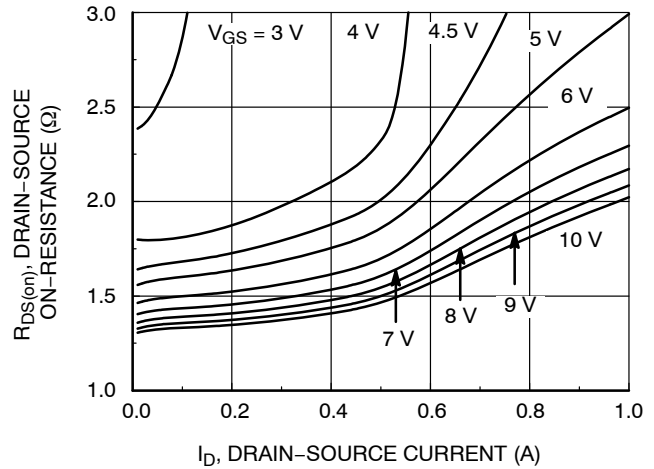


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

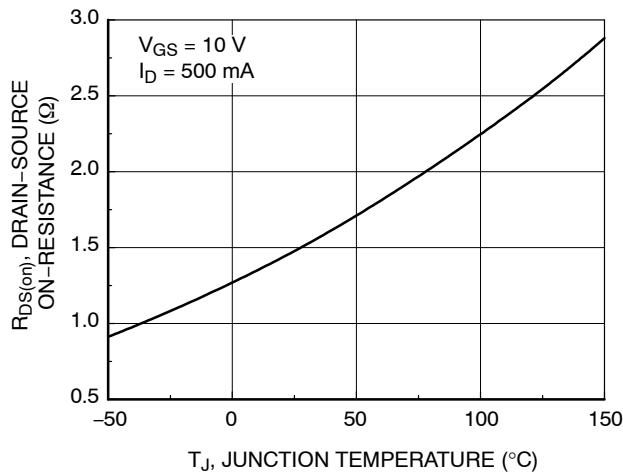


Figure 3. On-Resistance Variation with Temperature

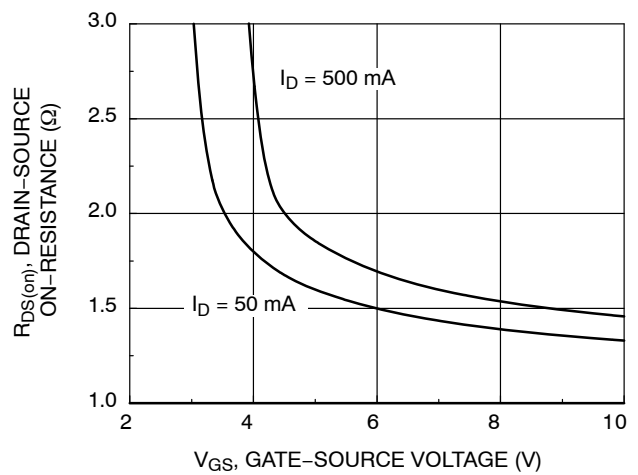


Figure 4. On-Resistance Variation with Gate-Source Voltage

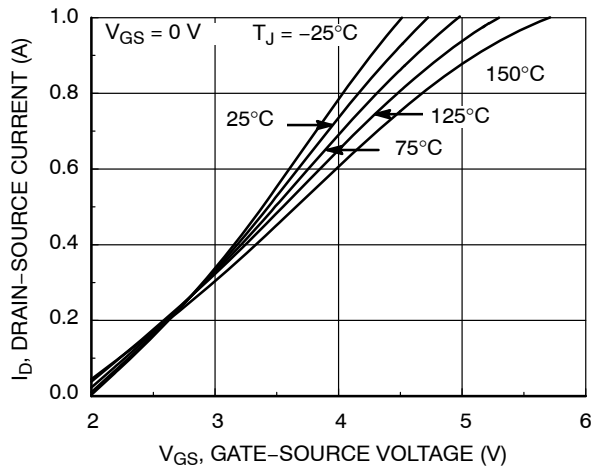


Figure 5. Transfer Characteristics

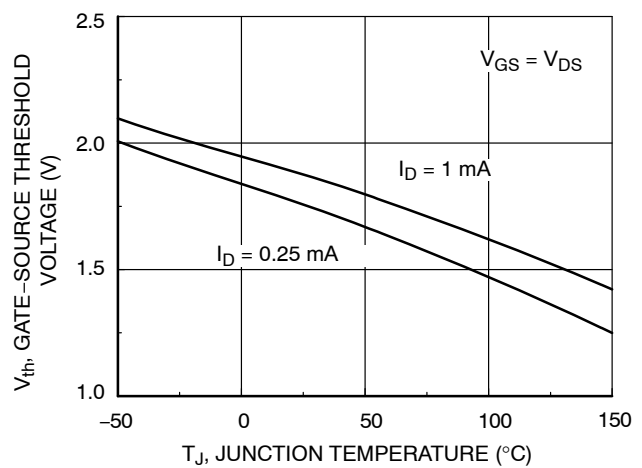
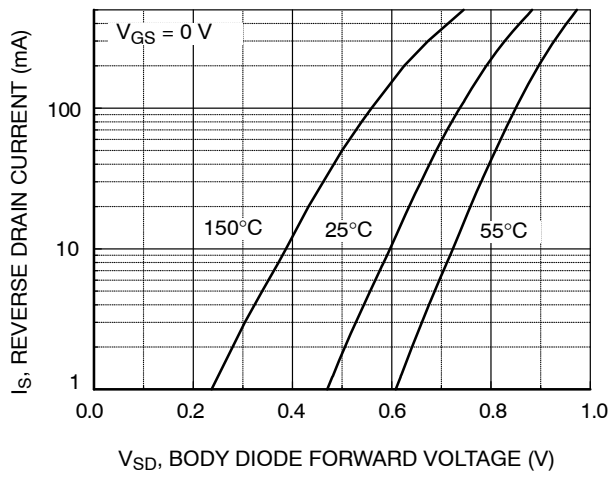
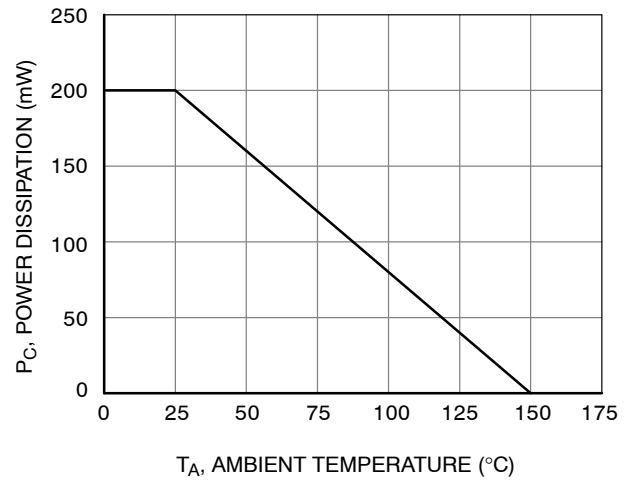


Figure 6. Gate Threshold Variation with Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



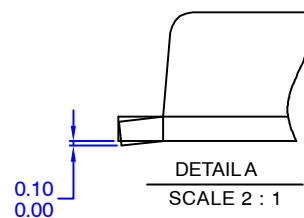
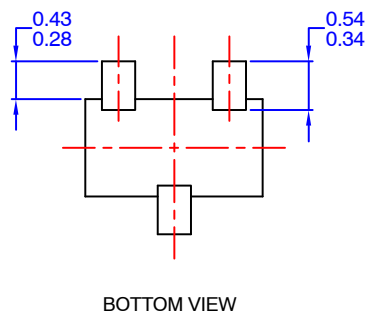
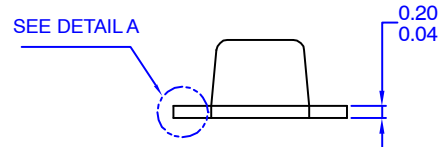
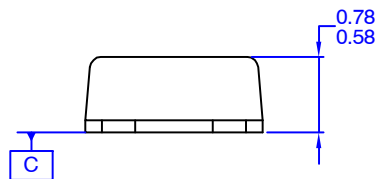
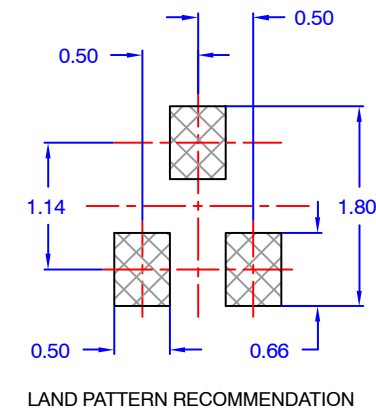
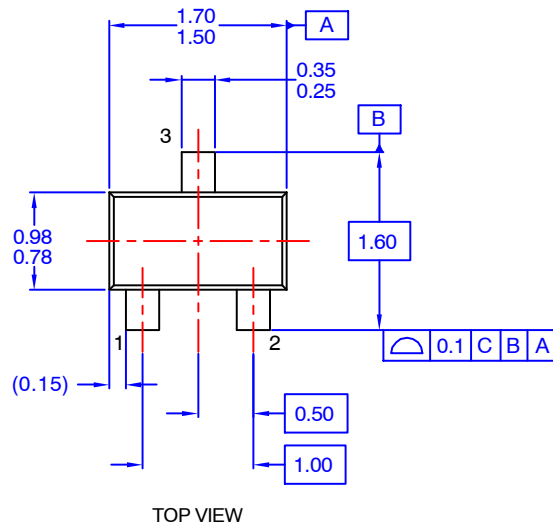
**Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature**



**Figure 8. Power Derating**

**SOT-523FL**  
**CASE 419BG**  
**ISSUE A**

DATE 29 SEP 2017



**NOTES:**

- A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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