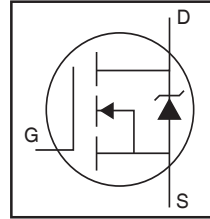


# AUIRFR4615 AUIRFU4615

HEXFET® Power MOSFET

## Features

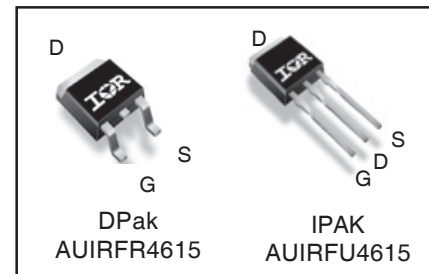
- Advanced Process Technology
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



$V_{DSS}$		<b>150V</b>
$R_{DS(on)}$	typ.	<b>34mΩ</b>
	max.	<b>42mΩ</b>
$I_D$		<b>33A</b>

## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	33	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	24	
$I_{DM}$	Pulsed Drain Current ①	140	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	109	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ
$dv/dt$	Peak Diode Recovery ③	38	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	1.045	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

**Static Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	34	42	mΩ	$V_{GS} = 10V, I_D = 21A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$g_{fs}$	Forward Transconductance	35	—	—	S	$V_{DS} = 50V, I_D = 21A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_{G(int)}$	Internal Gate Resistance	—	2.7	—	Ω	

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	26	—	nC	$I_D = 21A$
$Q_{gs}$	Gate-to-Source Charge	—	8.6	—		$V_{DS} = 75V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	9.0	—		$V_{GS} = 10V$ ④
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	17	—		$I_D = 21A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 98V$
$t_r$	Rise Time	—	35	—		$I_D = 21A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 7.3\Omega$
$t_f$	Fall Time	—	20	—		$V_{GS} = 10V$ ④
$C_{iss}$	Input Capacitance	—	1750	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	155	—		$V_{DS} = 50V$
$C_{rss}$	Reverse Transfer Capacitance	—	40	—		$f = 1.0MHz$ (See Fig.5)
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	179	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑥ (See Fig.11)
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	382	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	140		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 21A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	70	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 100V,$
		—	83	—		$T_J = 125^\circ\text{C}$ $I_F = 21A$
$Q_{rr}$	Reverse Recovery Charge	—	177	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④
		—	247	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	4.9	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.51mH$   
 $R_G = 25\Omega$ ,  $I_{AS} = 21A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 21A$ ,  $di/dt \leq 549A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

- ⑤  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$

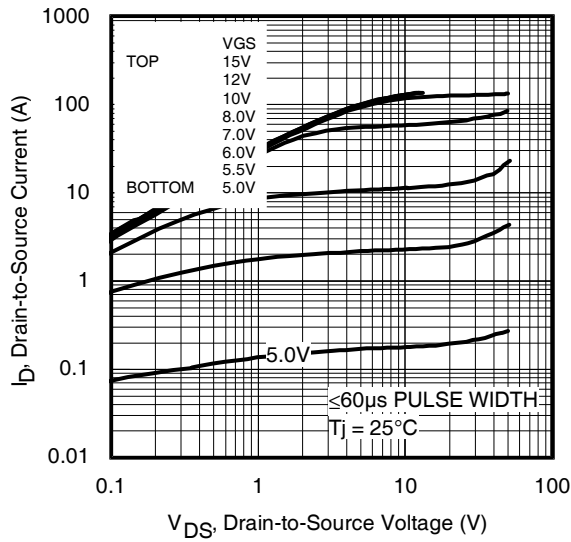
# Qualification Information<sup>†</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q101) <sup>††</sup>	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D PAK	MSL1
		I-PAK	N/A
<b>ESD</b>	Machine Model	Class M3(+/- 400V ) <sup>†††</sup> AEC-Q101-002	
	Human Body Model	Class H1B(+/- 1000V ) <sup>†††</sup> AEC-Q101-001	
	Charged Device Model	Class C5(+/- 2000V ) <sup>†††</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

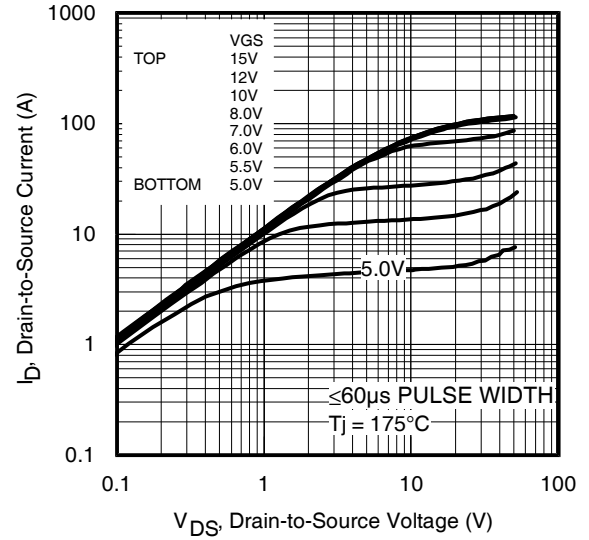
† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

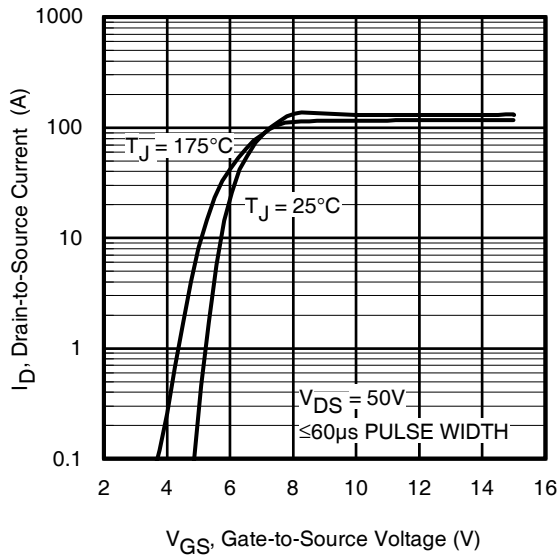
††† Highest passing voltage



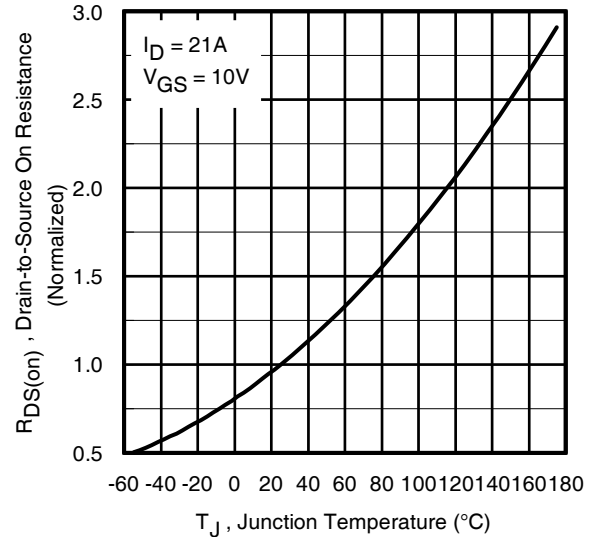
**Fig 1.** Typical Output Characteristics



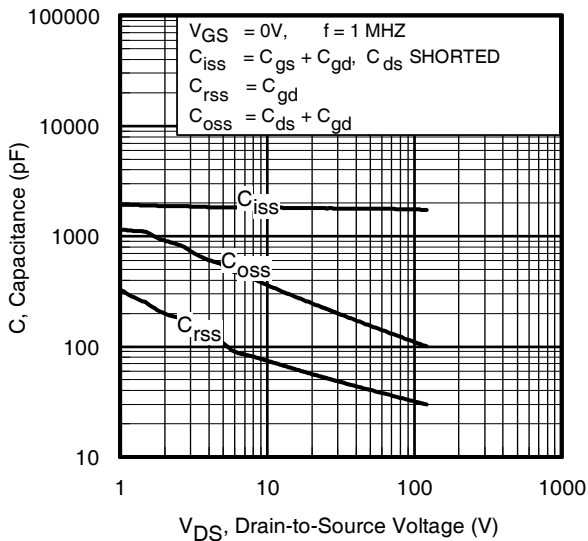
**Fig 2.** Typical Output Characteristics



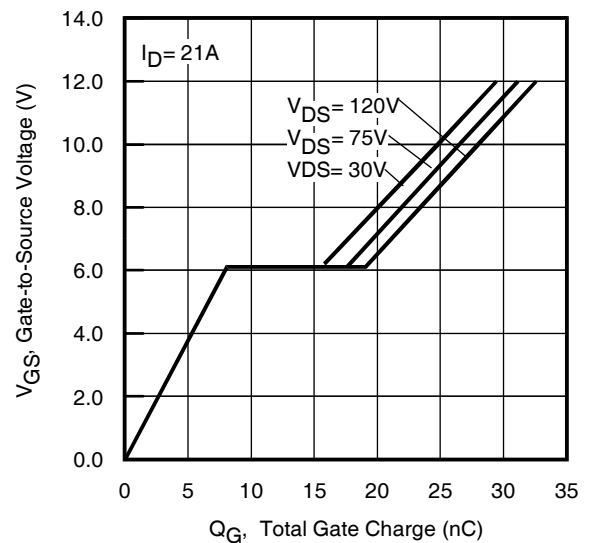
**Fig 3.** Typical Transfer Characteristics



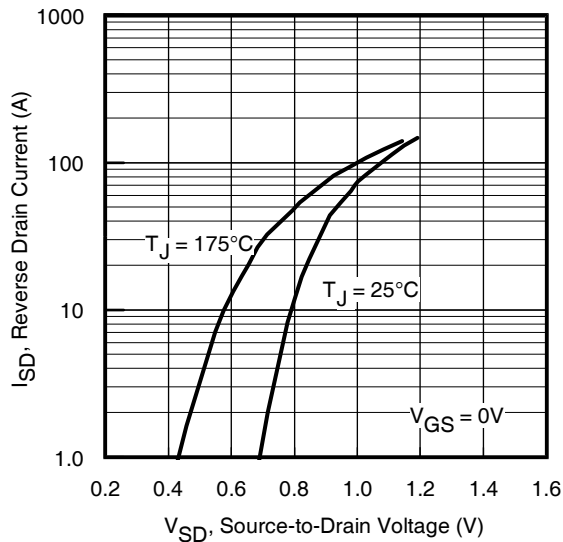
**Fig 4.** Normalized On-Resistance vs. Temperature



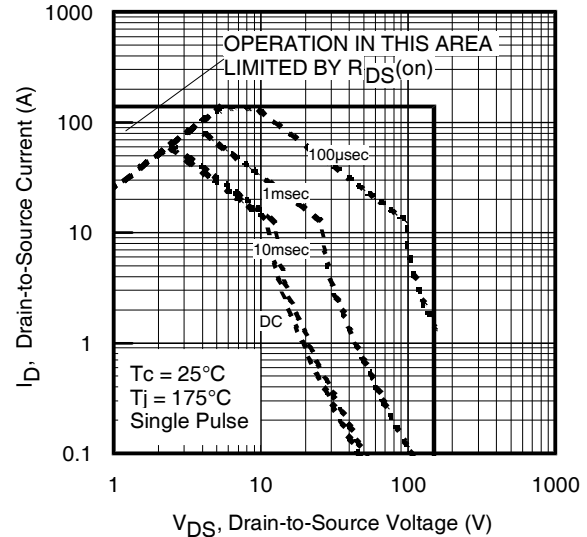
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



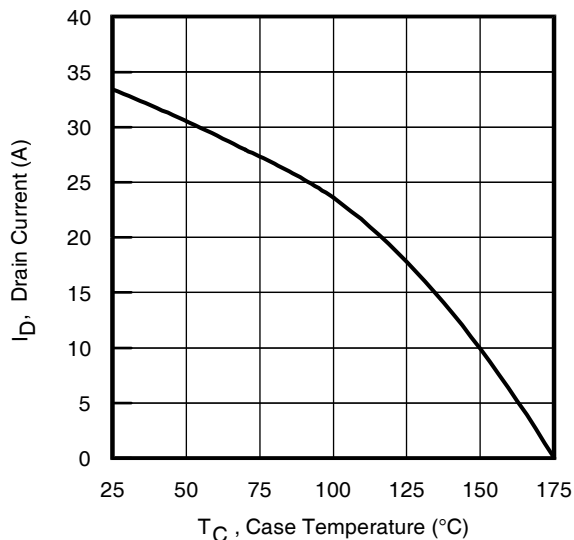
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



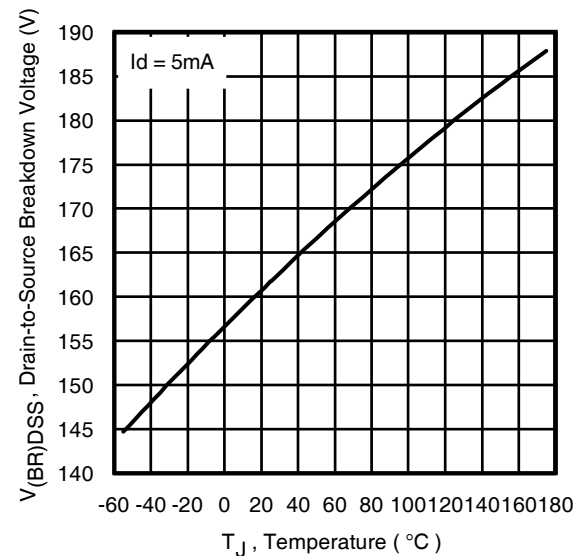
**Fig 7.** Typical Source-Drain Diode Forward Voltage



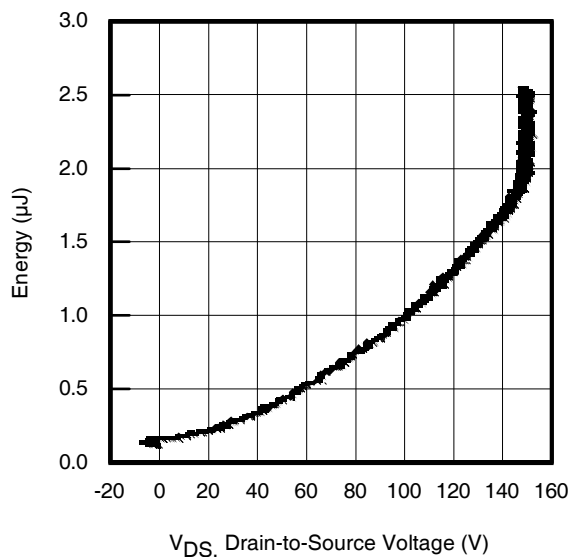
**Fig 8.** Maximum Safe Operating Area



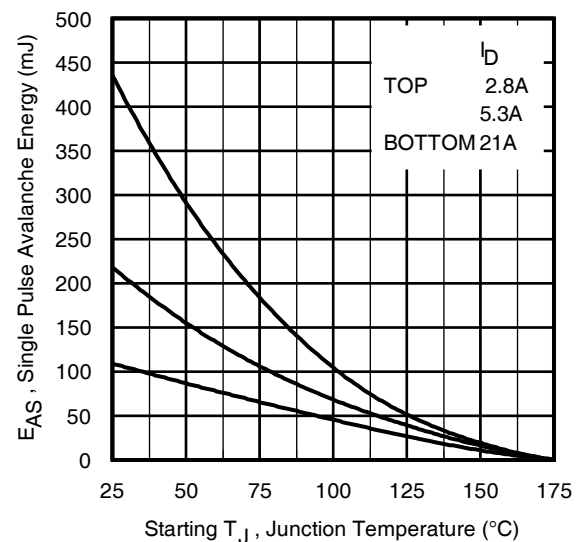
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

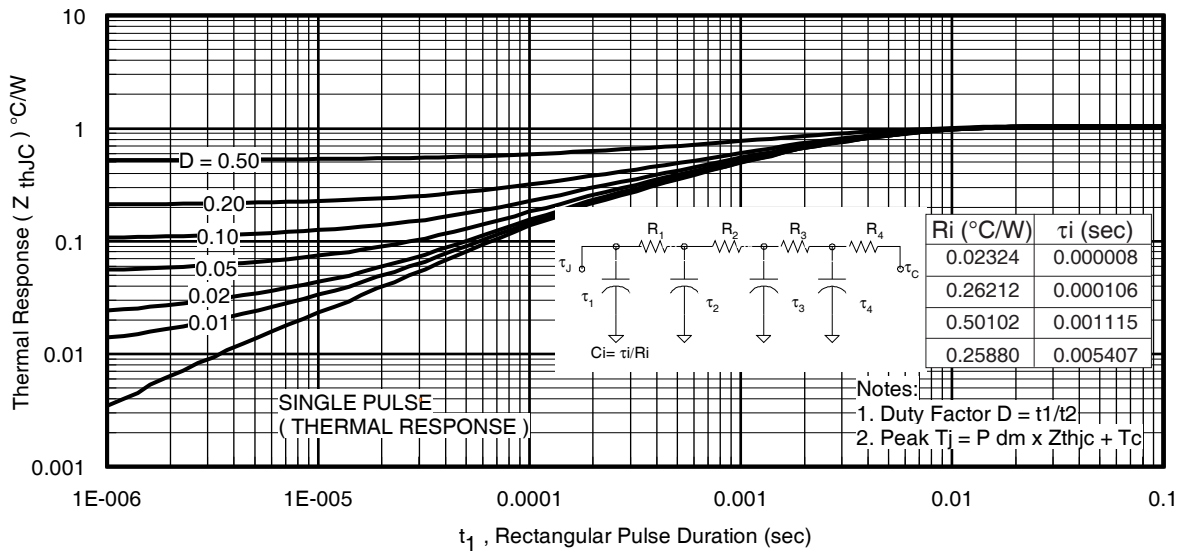


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

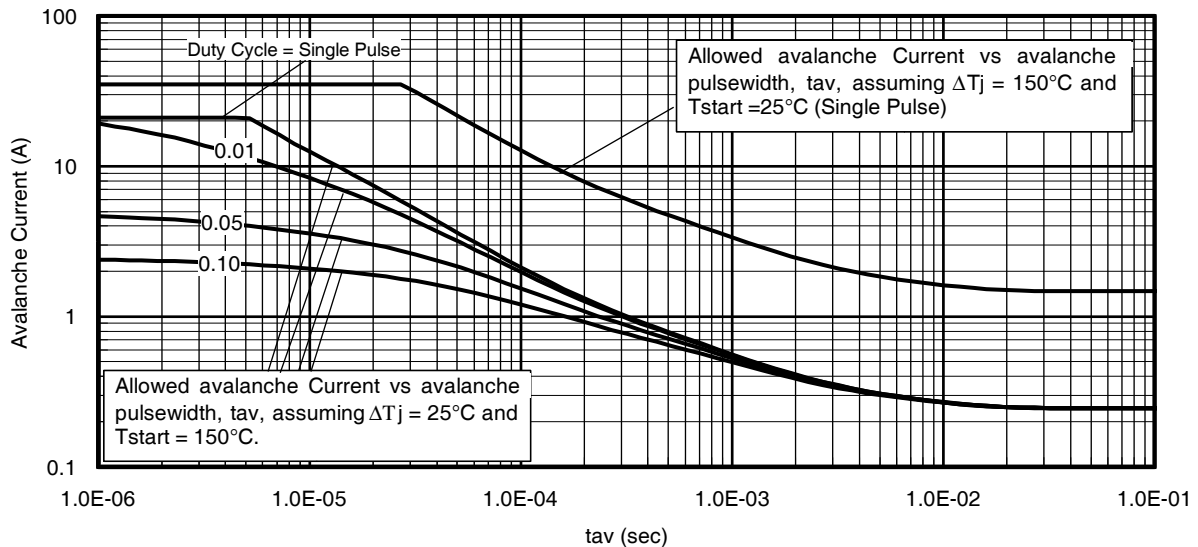


Fig 14. Typical Avalanche Current vs. Pulsewidth

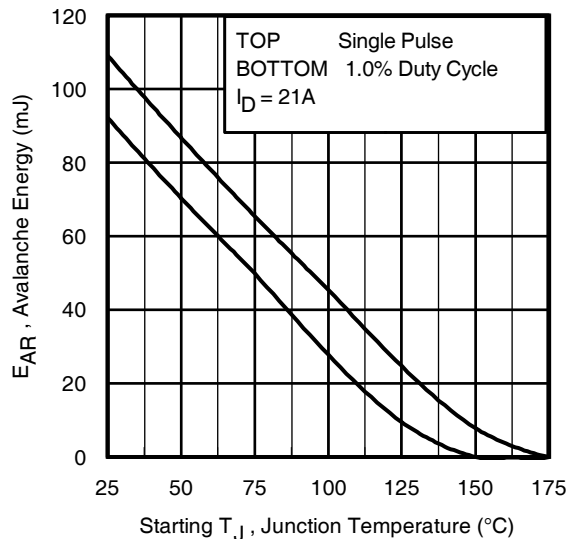


Fig 15. Maximum Avalanche Energy vs. Temperature

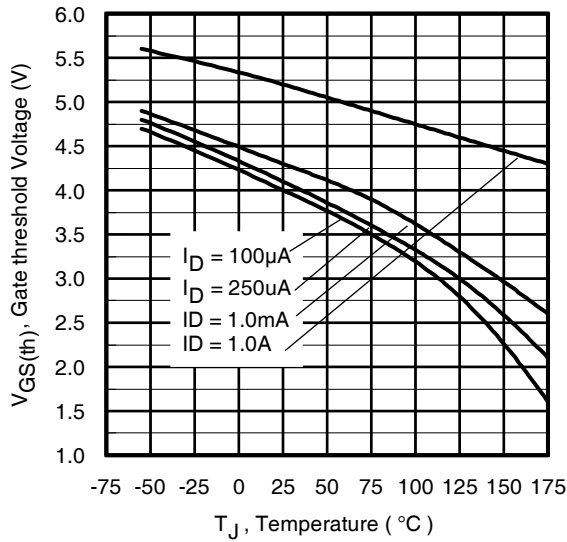
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

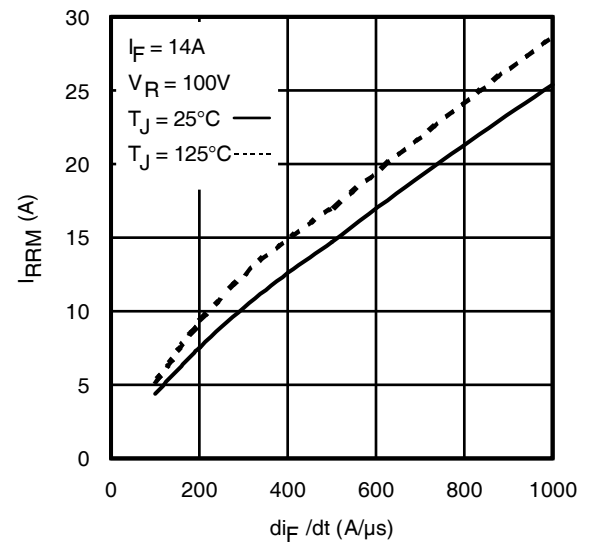
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

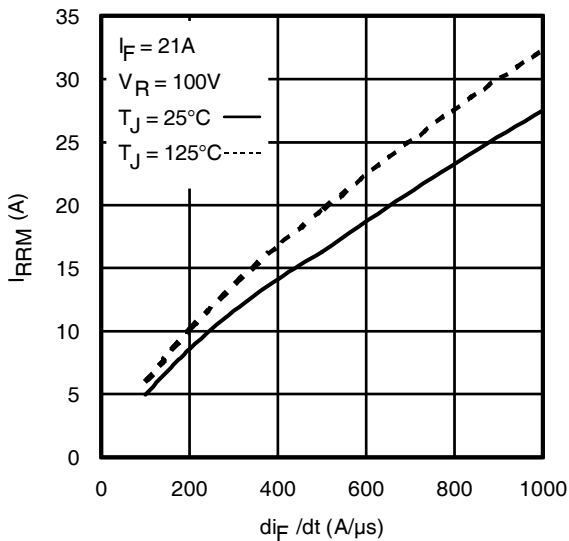
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



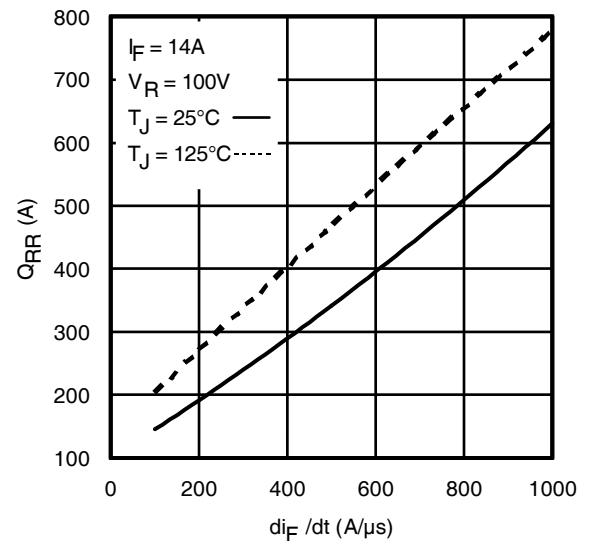
**Fig 16.** Threshold Voltage vs. Temperature



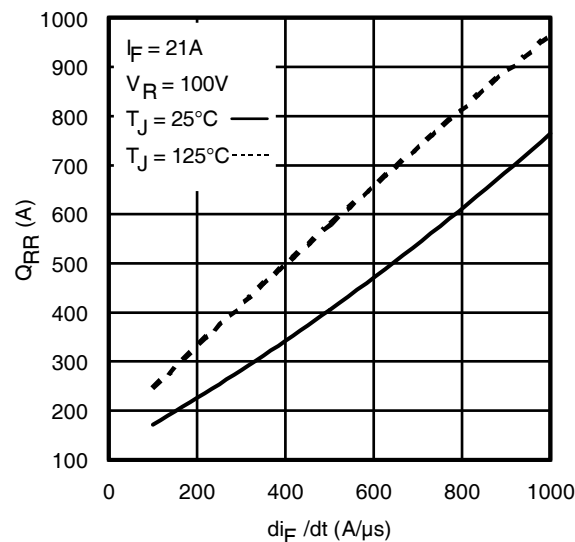
**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$



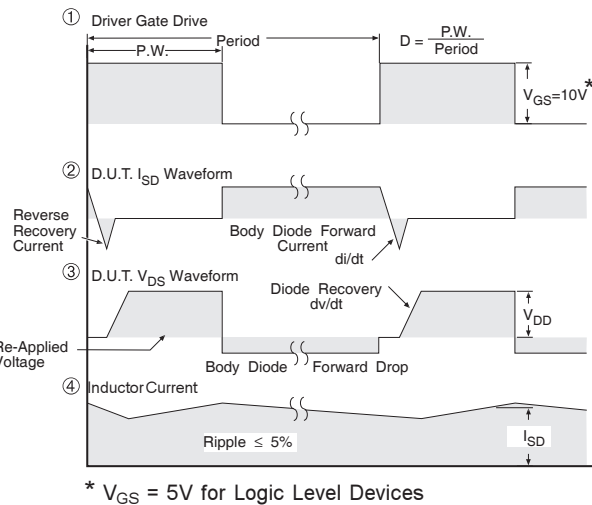
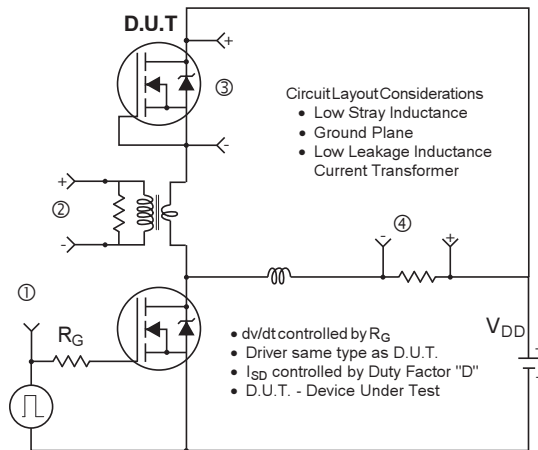
**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$



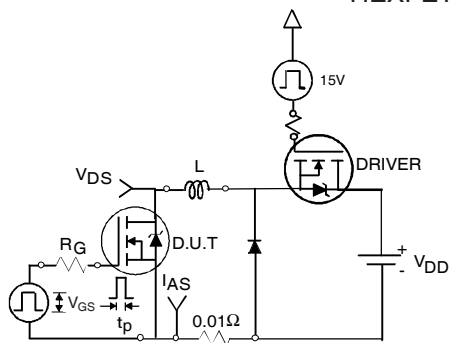
**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$



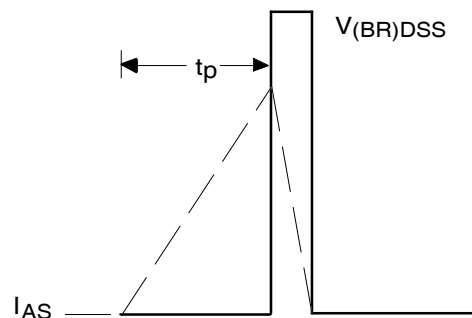
**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$



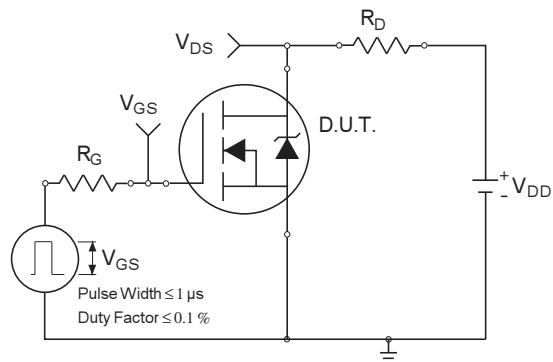
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



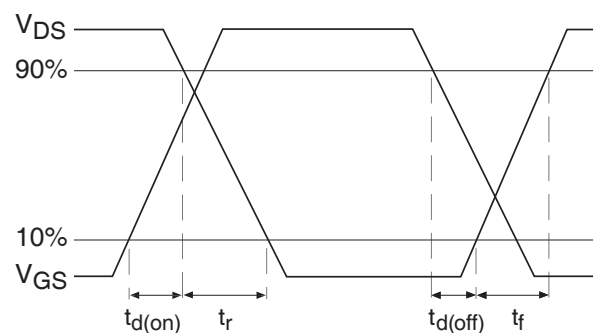
**Fig 22a.** Unclamped Inductive Test Circuit



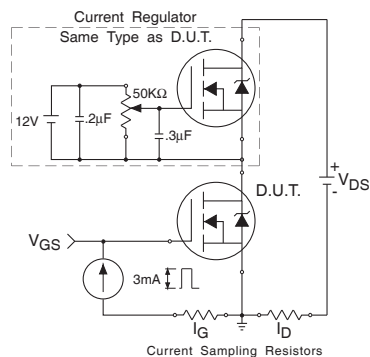
### Fig 22b. Unclamped Inductive Waveforms



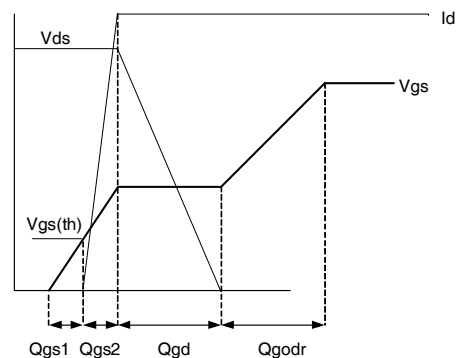
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**

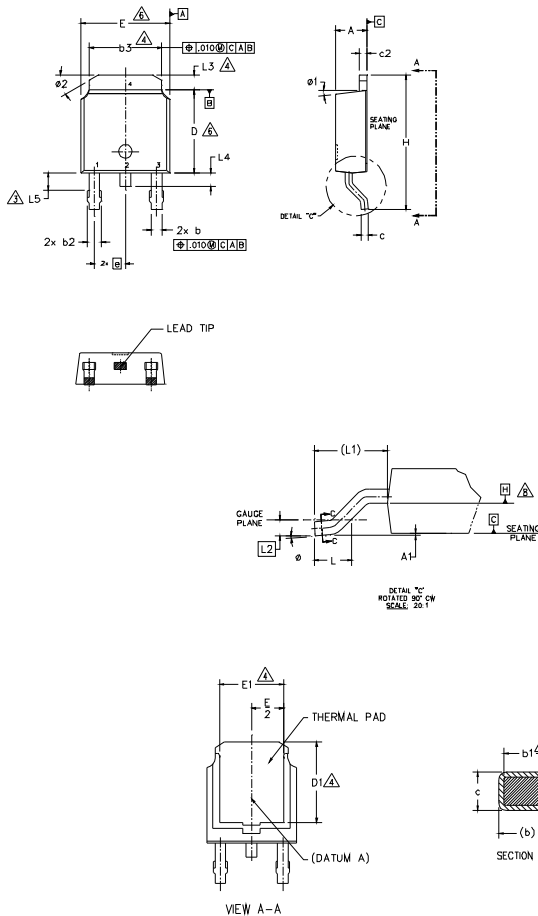


**Fig 24b. Gate Charge Waveform**



## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	—	0.13	—	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	—	.205	—	4
E	6.35	6.73	.250	.265	6
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	—	1.02	—	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

### LEAD ASSIGNMENTS

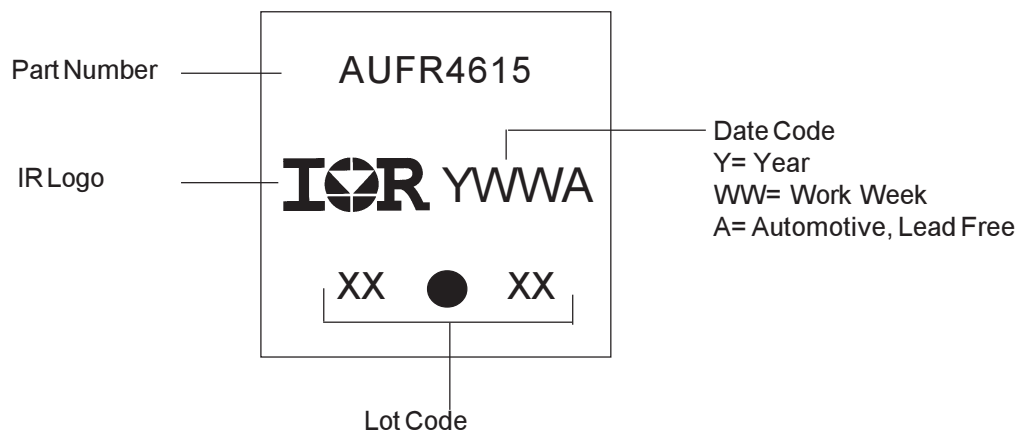
### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

### IGBT & CoPAK

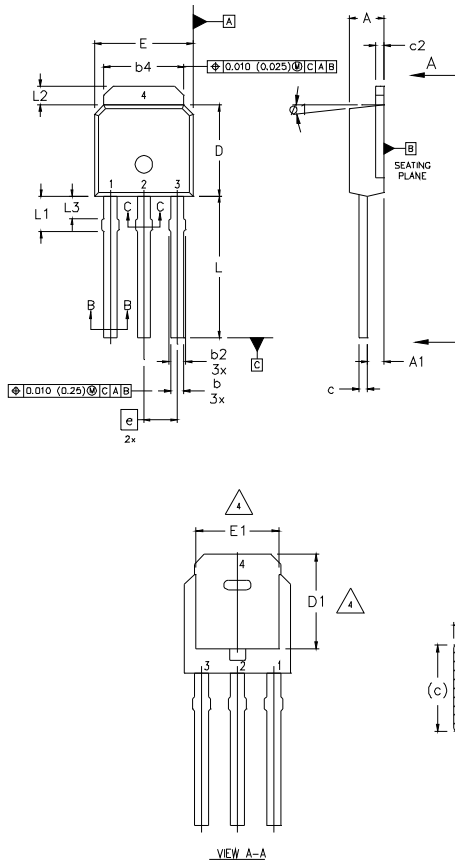
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# I-Pak (TO-251AA) Package Outline ( Dimensions are shown in millimeters (inches) )



## NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

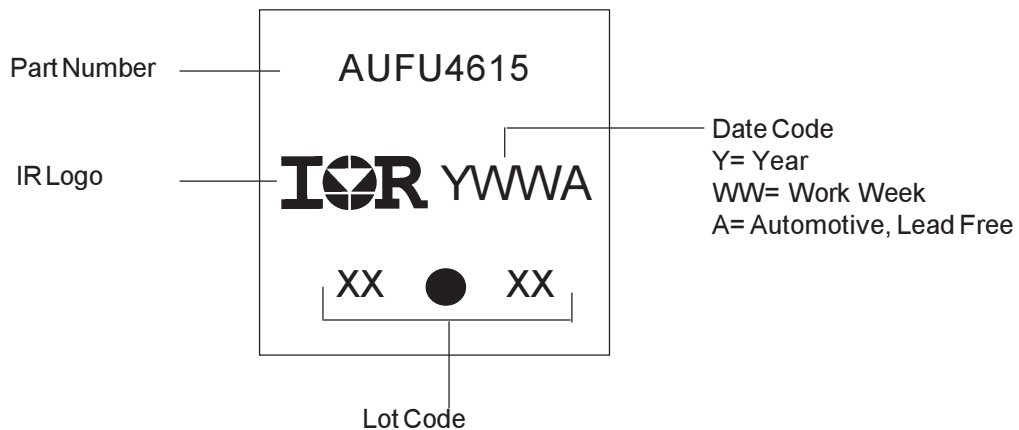
## LEAD ASSIGNMENTS

### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	—	0.205	—	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	—	0.170	—	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15°	Ø	15°	

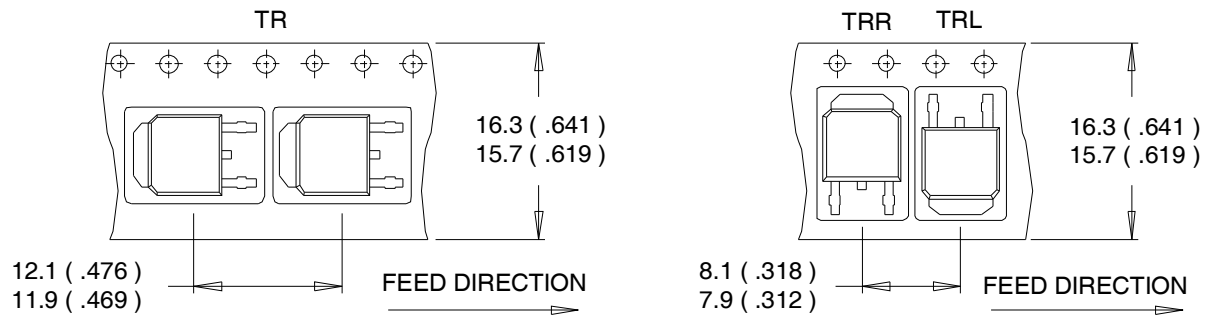
# I-Pak (TO-251AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

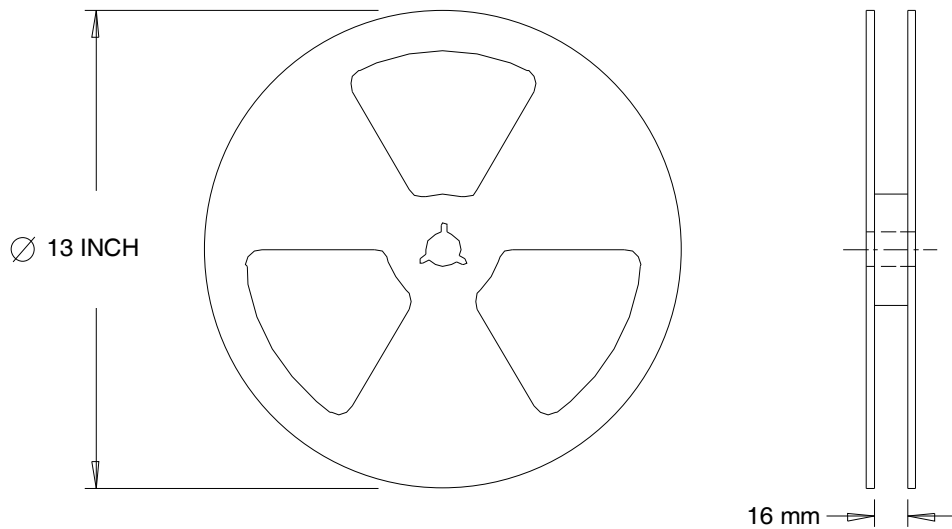
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES :

1. OUTLINE CONFORMS TO EIA-481.

## Ordering Information

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFR4615	DPak	Tube	75	AUIRFR4615
		Tape and Reel	2000	AUIRFR4615TR
		Tape and Reel Left	3000	AUIRFR4615TRL
		Tape and Reel Right	3000	AUIRFR4615TRR
AUIRFU4615	IPak	Tube	75	AUIRFU4615

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<http://www.irf.com/technical-info/>

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