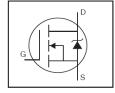
HEXFET® Power MOSFET



- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

$V_{ t DSS}$	55V
R _{DS(on)}	0.008Ω
I _D	64A



	Т	O-220 Full-Pak	
G		D	S
Gate		Drain	Source

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Book Bort Number	Dookogo Typo	Standar	Orderable Bort Number		
Base Part Number	Package Type	Form	Quantity	Orderable Part Number	
IRFI3205PbF	TO-220 Full-Pak	Tube	50	IRFI3205PbF	

Absolute Maximum Ratings					
Symbol	Parameter	Max.	Units		
_D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	64			
_D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	45	Α		
DM	Pulsed Drain Current ①⑥	390			
P _D @T _C = 25°C	Maximum Power Dissipation	63	W		
	Linear Derating Factor	0.42	W/°C		
V_{GS}	Gate-to-Source Voltage	± 20	V		
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②⑥	480	mJ		
AR	Avalanche Current ①⑥	59	А		
= AR	Repetitive Avalanche Energy ①	6.3	mJ		
dv/dt	Peak Diode Recovery dv/dt36	5.0	V/ns		
Γ _J	Operating Junction and	-55 to + 175			
$\Gamma_{ m STG}$	Storage Temperature Range		°C		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)			

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case		2.4	°C/W
$R_{ heta JA}$	Junction-to-Ambient		65	C/VV

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_{D} = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.057		V/°C	Reference to 25°C, I _D = 1mA ®
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.008	Ω	$V_{GS} = 10V, I_{D} = 34A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
gfs	Forward Trans conductance	42			S	V _{DS} = 25V, I _D = 59A [®]
ı	Drain to Source Leakage Current			25	μA	$V_{DS} = 55V$, $V_{GS} = 0V$
I _{DSS}	Drain-to-Source Leakage Current			250	μΑ	$V_{DS} = 44V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
1	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
I _{GSS}	Gate-to-Source Reverse Leakage			-100	IIA.	$V_{GS} = -20V$
Q_g	Total Gate Charge			170		I _D = 59A
Q_{gs}	Gate-to-Source Charge			32	nC	V _{DS} = 44V
Q_{qd}	Gate-to-Drain Charge			74		V _{GS} = 10V , See Fig. 6 and 13⊕⊚
$t_{d(on)}$	Turn-On Delay Time		14			$V_{DD} = 28V$
t _r	Rise Time		100		ns	I _D = 59A
$t_{d(off)}$	Turn-Off Delay Time		43		115	$R_G = 2.5\Omega$
t _f	Fall Time		70			R _D = 0.39Ω, See Fig. 10⊕⊚
L_D	Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
L _S	Internal Source Inductance		7.5			from package and center of die contact
C _{iss}	Input Capacitance		4000			V _{GS} = 0V
C _{oss}	Output Capacitance		1300			V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance		480		pF	f = 1.0MHz, See Fig. 5®
С	Drain to Sink Capacitance		12			f = 1.0MHz

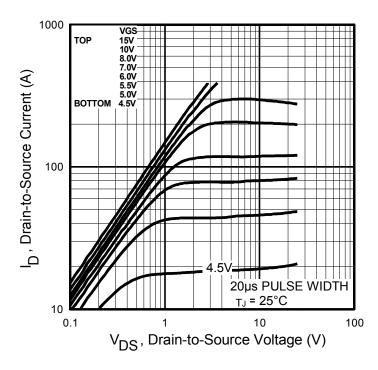
Source-Drain Ratings and Characteristics

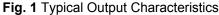
	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current (Body Diode)			64		MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ① ©			390		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 34A, V_{GS} = 0V $ ④
t _{rr}	Reverse Recovery Time		110	170	ns	$T_J = 25^{\circ}C, I_F = 59A$
Q _{rr}	Reverse Recovery Charge		450	680	nC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsio	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 190 μ H, R_G = 25 Ω , I_{AS} = 59A (See fig. 12)
- $\label{eq:local_spin_spin} \text{ } I_{SD} \leq 59\text{A}, \text{ } di/dt \leq 290\text{A}/\mu\text{s}, \text{ } V_{DD} \leq V_{(BR)DSS}, \text{ } T_J \leq 175^{\circ}\text{C}.$
- 4 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.
- ⑤ t=60s, *f*=60Hz
- © Uses IRF3205 data and test conditions.







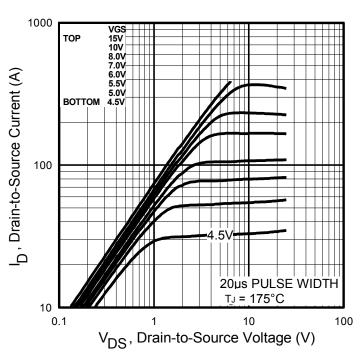


Fig. 2 Typical Output Characteristics

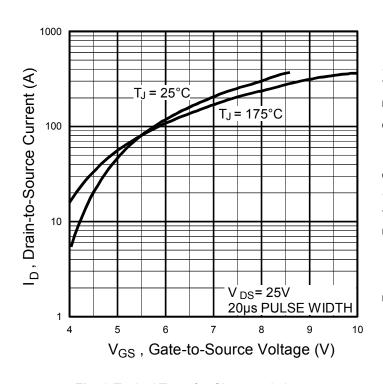


Fig. 3 Typical Transfer Characteristics

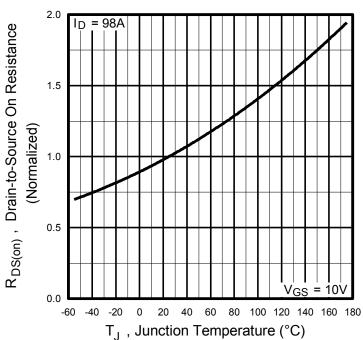


Fig. 4 Normalized On-Resistance vs. Temperature



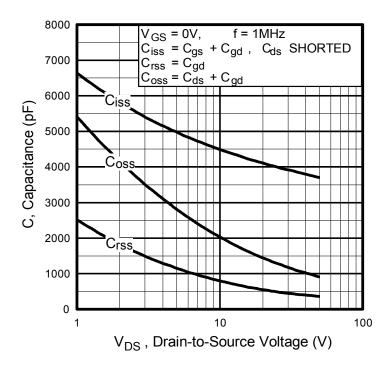


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

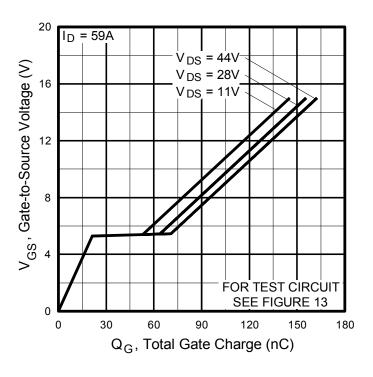


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

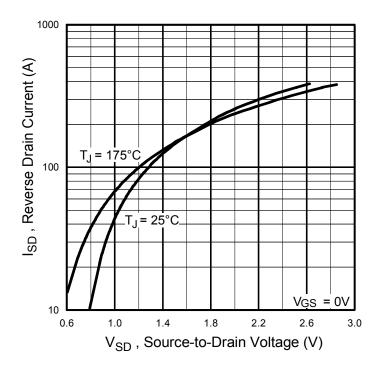


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

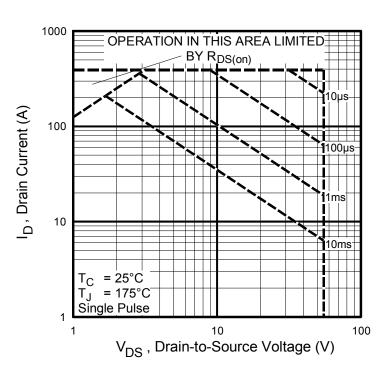


Fig 8. Maximum Safe Operating Area

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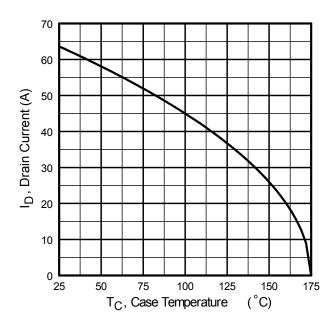


Fig 9. Maximum Drain Current vs. Case Temperature

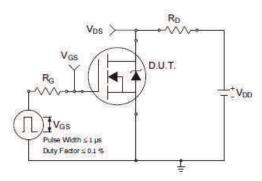


Fig 10a. Switching Time Test Circuit

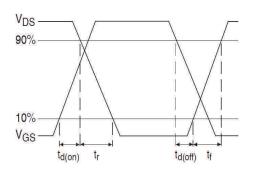


Fig 10b. Switching Time Waveforms

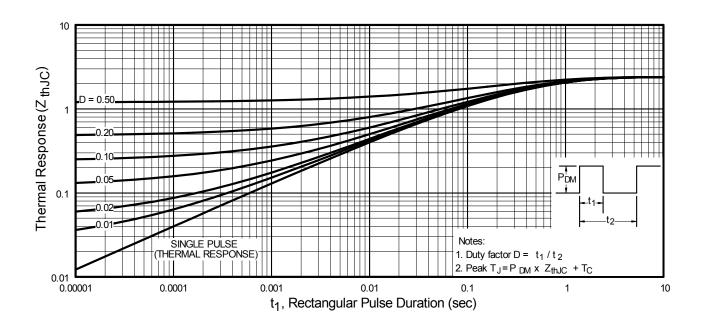


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



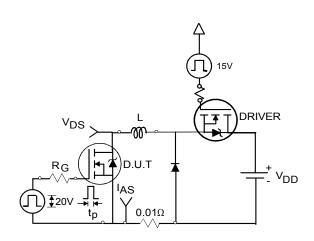


Fig 12a. Unclamped Inductive Test Circuit

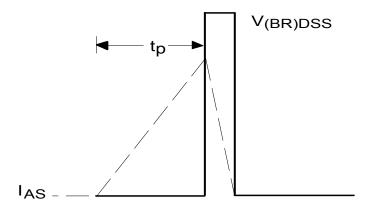


Fig 12b. Unclamped Inductive Waveforms

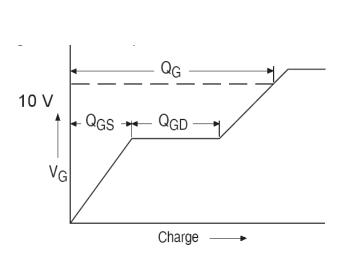


Fig 13a. Gate Charge Waveform

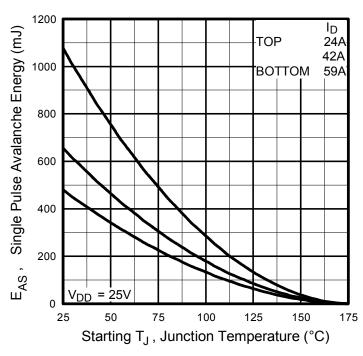


Fig 12c. Maximum Avalanche Energy vs. Drain Current

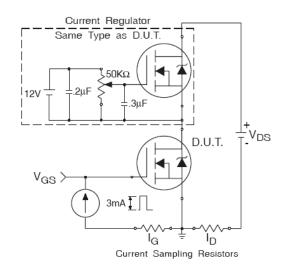
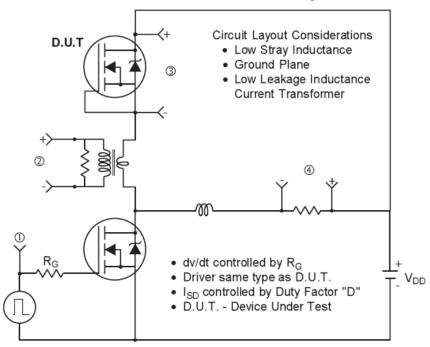


Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit



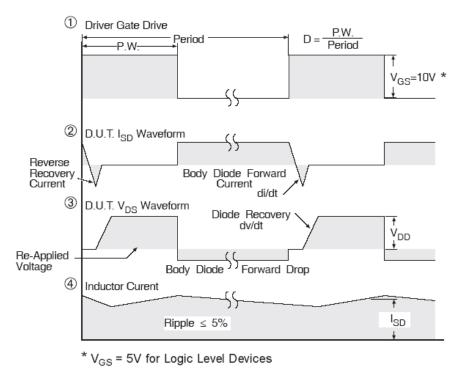
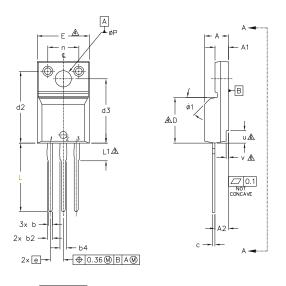
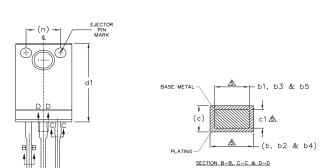


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))





NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2,0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 2.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.

DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.

DIMENSION 61, 63, 65 & c1 APPLY TO BASE METAL ONLY.

6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.

7.0 CONTROLLING DIMENSION: INCHES.

S Y M	DIMENSIONS			N		
В	MILLIM	ETERS	INC	INCHES		
0 L	MIN.	MAX.	MIN.	MAX.	NOTES	
А	4.57	4.83	.180	.190		
Α1	2.57	2.82	.101	.111		
Α2	2.51	2.92	.099	.115		
Ь	0.61	0.94	.024	.037		
ь1	0.61	0.89	.024	.035	5	
b2	0.76	1.27	.030	.050		
Ь3	0.76	1.22	.030	.048	5	
b4	1.02	1.52	.040	.060		
b5	1.02	1.47	.040	.058	5	
С	0.33	0.63	.013	.025		
c1	0.33	0.58	.013	.023	5	
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635		
d2	13.97	14.22	.550	.560		
d3	12.29	12.93	.484	.509		
Ε	9.63	10.74	.379	.423	4	
е		BSC	.100	BSC		
L	13.21	13.72	.520	.540		
L1	3.10	3.68	.122	.145	3	
n	6.05	6.60	.238	.260		
ØΡ	3.05	3.45	.120	.136		
u	2.39	2.49	.094	.098	6	
٧	0.41	0.51	.016	.020	6	
Ø1		45°	_	45°		

LEAD ASSIGNMENTS

<u>HEXFET</u>

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

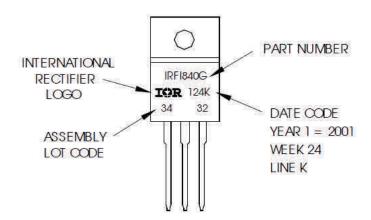
TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G

WITH ASSEMBLY LOT CODE 3432

ASSEMBLED ON WW 24, 2001 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at http://www.irf.com/package/



Qualification Information

Qualification information					
Qualification Level	Industrial (per JEDEC JESD47F) [†]				
Moisture Sensitivity Level	TO-220 Full-Pak	N/A			
RoHS Compliant	Yes				

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
04/27/2017	 Changed datasheet with Infineon logo - all pages. Corrected Package Outline on page 8.
04/21/2011	Added disclaimer on last page.

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