

# **MOSFET** - Power, Single N-Channel, SO8-FL 40 V, 0.42 mΩ, 509 A

# NTMFS0D4N04XM

#### **Features**

- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5x6 mm) with Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- Motor Drive
- Battery Protection
- ORing

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	40	V	
Gate-to-Source Voltage	DC	$V_{GS}$	±20	V
Continuous Drain Current T <sub>C</sub> = 25°C		I <sub>D</sub>	509	Α
	T <sub>C</sub> = 100°C		360	
Power Dissipation	T <sub>C</sub> = 25°C	$P_{D}$	197	W
Pulsed Drain Current	$T_{C} = 25^{\circ}C,$ $t_{p} = 10 \ \mu s$	I <sub>DM</sub>	4044	Α
Operating Junction and Storag Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +175	ç	
Source Current (Body Diode)		Is	202	Α
Single Pulse Avalanche Energy	I <sub>PK</sub> = 38.6 A	E <sub>AS</sub>	2396	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C

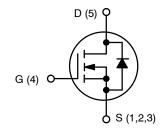
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.76	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{ heta JA}$	38.2	

- 1. Surface-mounted on FR4 board using 650 mm<sup>2</sup>, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
40 V	0.42 m $\Omega$ @ 10 V	509 A



**N-CHANNEL MOSFET** 



DFN5 (SO8-FL) CASE 506FA

#### **MARKING DIAGRAM**

0D4N4 AYWZZ

0D4N4 = Specific Device Code A = Assembly Location Y = Year W = Work Week

ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 2 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 25^{\circ}\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/ \Delta T_J$	I <sub>D</sub> = 250 μA, Referenced to 25°C		14.9		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 25°C			10	μΑ
		V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125°C			100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R <sub>DS(ON)</sub>	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}, T_J = 25^{\circ}\text{C}$		0.33	0.42	$m\Omega$
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 330 \mu A, T_J = 25^{\circ}C$	2.5	3	3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/ \Delta T_J$	$V_{GS} = V_{DS}$ , $I_D = 330 \mu A$		-7.21		mV/°C
Forward Trans-conductance	9FS	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 A		286		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE			•	•	
Input Capacitance	C <sub>ISS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		8577		pF
Output Capacitance	Coss			6090		1
Reverse Transfer Capacitance	C <sub>RSS</sub>			120		
Output Charge	Q <sub>OSS</sub>	$V_{DD} = 20 \text{ V}, I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$		183		nC
Total Gate Charge	Q <sub>G(TOT)</sub>			133		
Threshold Gate Charge	Q <sub>G(TH)</sub>			25.2		1
Gate-to-Source Charge	Q <sub>GS</sub>			37.2		1
Gate-to-Drain Charge	Q <sub>GD</sub>			24.2		1
Gate Resistance	R <sub>G</sub>	f = 1 MHz		0.42		Ω
SWITCHING CHARACTERISTICS			-			-
Turn-On Delay Time	t <sub>d(ON)</sub>	Resistive Load, V <sub>GS</sub> = 0/10 V,		34.5		ns
Rise Time	t <sub>r</sub>	$V_{DD} = 20 \text{ V}, I_D = 50 \text{ A}, R_G = 0 \Omega$		11.1		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>			49.4		1
Fall Time	t <sub>f</sub>			13		
SOURCE-TO-DRAIN DIODE CHARACTE	RISTICS			•	•	
Forward Diode Voltage	V <sub>SD</sub>	$I_S = 50 \text{ A}, V_{GS} = 0 \text{ V}, T_J = 25^{\circ}\text{C}$		0.79	1.2	V
		I <sub>S</sub> = 50 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C		0.63		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V}, I_{S} = 50 \text{ A},$		94.4		ns
Charge Time	ta	dl/dt = 100 A/μs, V <sub>DD</sub> = 20 V		55.3		1
Discharge Time	t <sub>b</sub>			39.1		1
Reverse Recovery Charge	Q <sub>RR</sub>			316		nC

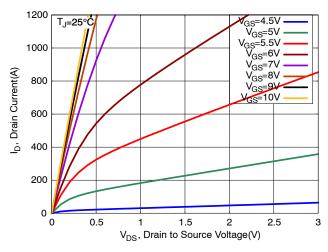
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTMFS0D4N04XMT1G	0D4N4	DFN5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **TYPICAL CHARACTERISTICS**



1200 V<sub>DS</sub>=5V

1000

(V)
1000

600

200

T<sub>J</sub>=-55°C

T<sub>J</sub>=25°C

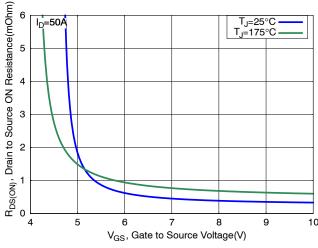
T<sub>J</sub>=175°C

0
1
2
3
4
5
6
7

V<sub>GS</sub>, Gate to Source Voltage(V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



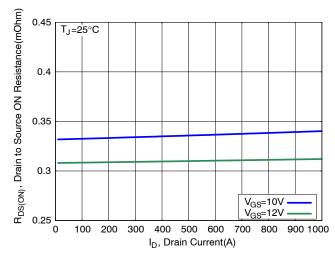
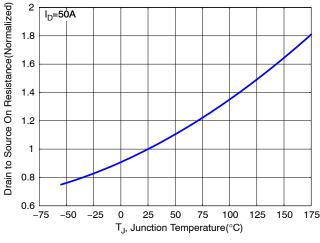


Figure 3. On-Resistance vs. Gate Voltage

Figure 4. On-Resistance vs. Drain Current



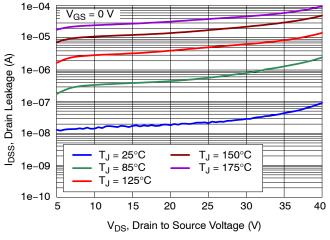


Figure 5. Normalized ON Resistance vs. Junction Temperature

Figure 6. Drain to Source Voltage vs Drain Leakage

#### TYPICAL CHARACTERISTICS (CONTINUED)

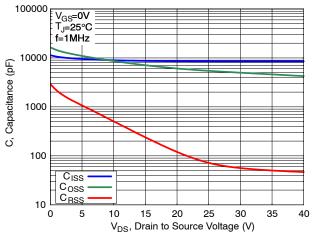
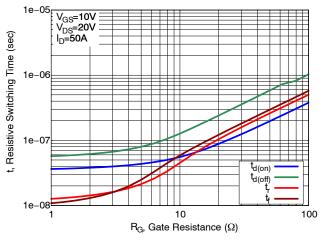


Figure 7. Capacitance Characteristics

Figure 8. Gate Charge Characteristics



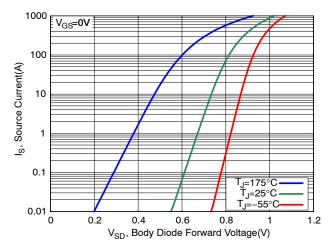
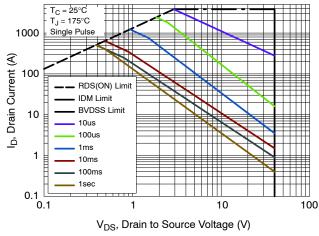


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Characteristics



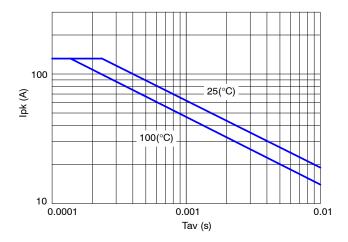


Figure 11. Safe Operating Area (SOA)

Figure 12. Avalanche Current vs. Pulse Time (UIS)

# TYPICAL CHARACTERISTICS (CONTINUED)

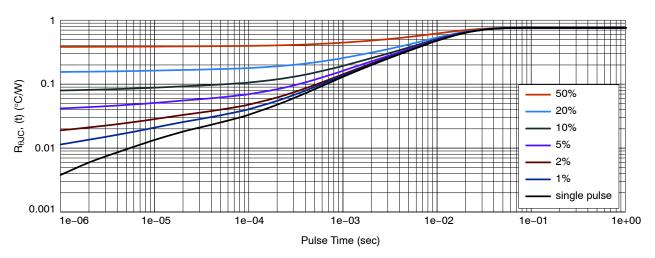


Figure 13. Thermal Response





**IDENTIFIER** 

// 0.10 C

△ 0.10 C

⊕ 0.10 C A B 0.05 C

#### DFN5 5.00x5.90x1.00, 1.27P CASE 506FA **ISSUE A**

**DATE 03 OCT 2024** 

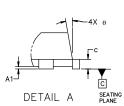
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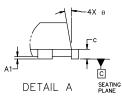
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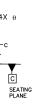
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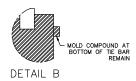
SEATING PLANE

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

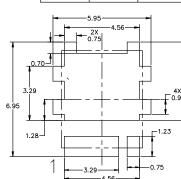


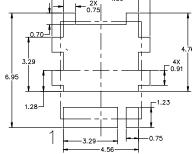






MILLIMETERS					
DIM	MIN	NOM	MAX		
Α	0.90	1.00	1.10		
A1	0.00		0.05		
b	0.33	0.41	0.51		
С	0.23	0.28	0.33		
D	5.00	5.15	5.30		
D1	4.80	5.00	5.20		
D2	3.90	4.10	4.30		
E	6.00	6.15	6.30		
E1	5.70	5.90	6.10		
E2	3.55	3.75	3.95		
е	1	.27 BS0			
G	0.50	0.55	0.70		
G1	0.26	0.36	0.46		
k	1.10	1.25	1.40		
L	0.50	0.60	0.70		
L1	0.150 REF				
М	3.00	3.40	3.80		
Θ	0.		12°		





#### RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# DETAIL B G1-(EXPOSED PAD)

BOTTOM VIEW

TOP VIEW

SIDE VIEW

DETAIL A

## **GENERIC MARKING DIAGRAM\***

XXXXXX **AYWZZ** 

XXXX = Specific Device Code

= Assembly Location

Υ = Year W = Work Week

ZΖ = Assembly Lot Code \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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