

CoolSiC™ 440V CoolSiC™ G2 MOSFET with extended V_{DS}

Features

- Ideal for high frequency switching and synchronous rectification
- Commutation robust fast body diode with low Often
- Low R_{DS(on)} dependency on temperature
 Benchmark gate threshold voltage, V_{GS(th)} = 4.5 V
- Recommended gate driving voltage 0 V to 18 V
- .XT interconnection technology for best-in-class thermal performance
- 100% avalanche tested
- Fully tested in production to guarantee extended $V_{(BR)DSS}$

Potential applications

- Application specific MOSFET designed to power AI
- · High Power SMPS for server, datacenter and telecom rectifiers

Product validation

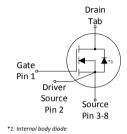
Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Key performance parameters Table 1

Parameter	Value	Unit
V_{DS}	440	V
$V_{\mathrm{DS,tr}}$	455	V
$R_{\mathrm{DS(on),typ}}$	25.4	mΩ
I_{D}	68	A
$Q_{ m oss}$	59	nC
E _{oss}	4.2	μJ
Q_{G}	36	nC











Part number	Package	Marking	Related links
IMT44R025M2H	PG-HSOF-8	44R025M2	-

Public

440V CoolSiC[™] G2 MOSFET with extended V_{DS} IMT44R025M2H



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1 Maximum ratings

at T_A =25 °C, unless otherwise specified

Table 2 Maximum ratings

Daramatar	Cymphol		Values			Note / Took on white a	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test condition	
				68		V _{GS} =18 V, T _C =25 °C	
Continuous drain current 1)	I_{D}	-	-	48	Α	V _{GS} =18 V, T _C =100 °C	
				9		$V_{\rm GS}$ =18 V, $T_{\rm A}$ =25 °C, $R_{\rm THJA}$ =40 °C/W ²⁾	
Pulsed drain current ³⁾	I _{D,pulse}	-	-	204	А	<i>T</i> _c =25 °C	
Avalanche energy, single pulse ⁴⁾	E _{AS}			93	ml	$I_{\rm D}$ =15.7 A, $R_{\rm GS}$ =25 Ω	
Avalanche energy, repetitive	E_{AR}	1	-	0.47	11113	1D-13.1 /1, NGS-23 12	
Gate source voltage (static)	$V_{\rm GS,DC}$	-7	-	23	V	-	
Gate source voltage (transient)	$V_{\rm GS,AC}$	-10	-	25	V	t _{pulse} ≤500 ns, duty cycle≤1%	
Power dissipation P_{tot}			-	214	147	<i>T</i> _C =25 °C	
	P_{tot}	-		3.8	W	$T_{\rm A}$ =25 °C, $R_{\rm THJA}$ =40 °C/W ²⁾	
Storage temperature	$T_{\rm stg}$	-55		150	°C		
Operating junction temperature	T _j	-55	-	175			

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm 2 (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 19 for more detailed information.



2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			1155	Nieto / Test sou dition
	Syllibol	Min.	Тур.	Max.	Onit	Note / Test condition
Thermal resistance, junction - case	R_{thJC}			0.7		
Thermal resistance, junction -		_	_		°C/W	_
ambient,	R_{thJA}			40	0, 11	
6 cm ² cooling area ⁵⁾						

Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm 2 (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

3 Operating range

Table 4 Operating range

Parameter	Symbol		Values		Linit	Note / Test condition	
rarameter	Syllibot	Min.	Тур.	Max.	Onic	Note / Test condition	
Recommended turn-on voltage	$V_{GS(on)}$		18		\/		
Recommended turn-off voltage	$V_{GS(off)}$]	0	-	l v		



4 Electrical characteristics

at T_i =25 °C, unless otherwise specified

Table 5 Static characteristics

Davamatar	Cymphal	Values			115.4	Note / Took on white
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test condition
Drain-source breakdown voltage	V _{(BR)DSS}	440	-	-	V	$V_{\rm GS}$ =0 V, $I_{\rm D}$ =0.56 mA
Transient drain-source breakdown voltage ⁶⁾	$V_{(BR)DSS,tr}$	455	-	-	V	$V_{\rm GS}$ =0 V, $I_{\rm D}$ =5.6 mA, $t_{\rm pulse}$ ≤10 ms, duty cycle≤50%
Gate threshold voltage ⁷⁾	$V_{\rm GS(th)}$	3.5	4.5	5.6	٧	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 5.6 \rm mA$
	I _{DSS}	-	1	75		V _{DS} =400 V, V _{GS} =0 V, T _j =25 °C
Zero gate voltage drain current			2	-	μΑ	$V_{\rm DS}$ =400 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =25 °C $V_{\rm DS}$ =400 V, $V_{\rm GS}$ =0 V, $T_{\rm j}$ =175 °C
Gate-source leakage current	I _{GSS}	-	1	100	nA	V _{GS} =20 V, V _{DS} =0 V
			25.4	32.1		$V_{\rm GS}$ =18 V, $I_{\rm D}$ =15.7 A, $T_{\rm j}$ =25 °C
Drain-source on-state resistance	$R_{\mathrm{DS(on)}}$	-	36.5	-	mΩ	$V_{\rm GS}$ =18 V, $I_{\rm D}$ =15.7 A, $T_{\rm j}$ =175 °C
			31.1	-]	$V_{\rm GS}$ =15 V, $I_{\rm D}$ =15.7 A, $T_{\rm j}$ =25 °C
Gate resistance	R_{G}	-	3.3	5.0	Ω	-

⁶⁾ Guaranteed by design, rated for transient startup overvoltages to comply with IPC-9592B derating guidelines.

Table 6 Dynamic characteristics

Davamakar	Crossbal		Values		115:4	Nata / Tast as a dition	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test condition	
Input capacitance	C _{iss}		1200	1690			
Output capacitance	C _{oss}]-	180	-	pF	V _{GS} =0 V, V _{DS} =200 V, <i>f</i> =1 MHz	
Reverse transfer capacitance	C _{rss}		14	-			
Effective output capacitance, energy related ⁸⁾	$C_{\rm o(er)}$	-	211	-	рF	V _{GS} =0 V, V _{DS} =0200 V	
Effective output capacitance, time related ⁹⁾	$C_{\rm o(tr)}$	-	290	-	рF	$I_{\rm D}$ =constant, $V_{\rm GS}$ =0 V, $V_{\rm DS}$ =0200 V	
Turn-on delay time	$t_{\rm d(on)}$		12.5		ns	$V_{\rm DD}$ =200 V, $V_{\rm GS}$ =018 V, $I_{\rm D}$ =15.7 A,	
Rise time	t _r	-	11.9]-	115	$R_{\rm G,ext}$ =1.8 Ω	
Turn-off delay time	$t_{ m d(off)}$		19.9		nc	$V_{\rm DD}$ =200 V, $V_{\rm GS}$ =180 V, $I_{\rm D}$ =15.7 A,	
Fall time	$t_{\rm f}$]-	7.9]_	ns	$R_{\rm G,ext}$ =1.8 Ω	

⁸⁾ $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 200 V.

⁷⁾ Tested after 1ms pulse at V_{GS} = +20V.

⁹⁾ $C_{\rm o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{\rm oss}$ while $V_{\rm DS}$ is rising from 0 to 200 V.



Table 7 Gate Charge Characteristics 10)

Parameter	Symbol	Values			Linit	Note / Test condition
	Symbol	Min.	Тур.	Max.	Oilit	Note / Test condition
Gate to source charge	Q_{gs}		9.8			
Gate to drain charge	Q_{gd}]-	7.5	-	- nC	$V_{\rm DD}$ =200 V, $I_{\rm D}$ =15.7 A, $V_{\rm GS}$ =0 to 18 V
Gate charge total	Q_{g}		36			
Gate charge total, sync. FET	$Q_{\rm g(sync)}$	-	34	-	nC	V _{DS} =0.1 V, V _{GS} =0 to 18 V
Output charge	Q _{oss}		59		nC	1/ -200 //
Output Energy	E _{oss}	-	4.2		μJ	$V_{\rm DS}$ =200 V, $V_{\rm GS}$ =0 V

 $^{^{10)}}$ As per JEP192, Guidelines for Gate Charge ($Q_{
m G}$) Test Method for SiC MOSFET.

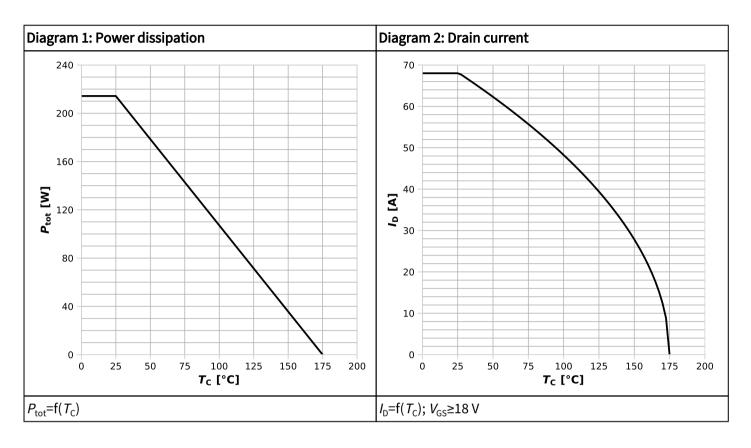
Table 8 Reverse diode characteristics

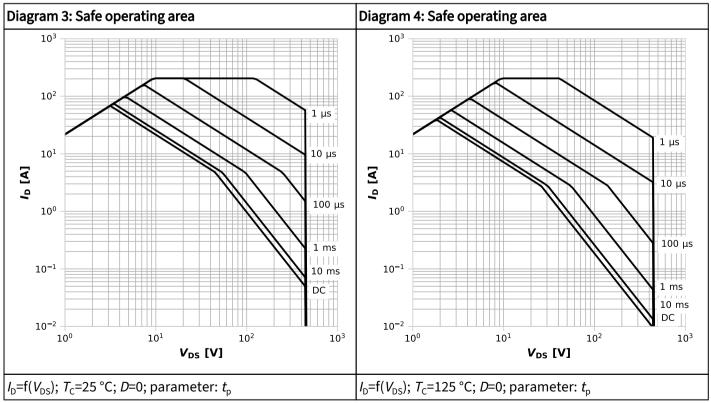
Devemakev	Comphal	Values			11	Note / Test condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test condition
Diode continuous forward current	I _S	-	-	32	Α	<i>T</i> _C =25 °C
Diode pulse current	I _{S,pulse}	-	-	204	Α	$T_{\rm C}$ =25 °C, $t_{\rm pulse}$ ≤250 ns
Diode forward voltage	$V_{\rm SD}$	-	3.5	4.3	V	$V_{\rm GS}$ =0 V, $I_{\rm S}$ =15.7 A, $T_{\rm j}$ =25 °C
MOSFET forward recovery time	t _{fr}	-	13.6			$V_{\rm R}$ =200 V, $I_{\rm S}$ =15.7 A, d $i_{\rm S}$ /d t =1000 A/ μ s
			8.9		ns	$V_{\rm R}$ =200 V, $I_{\rm S}$ =15.7 A, d $i_{\rm S}$ /d t =4000 A/ μ s
MOSFET forward recovery charge ¹¹⁾	Q_{fr}	-	55	-	nC	$V_{\rm R}$ =200 V, $I_{\rm S}$ =15.7 A, d $i_{\rm S}$ /d t =1000 A/ μ s
			116		IIC	$V_{\rm R}$ =200 V, $I_{\rm S}$ =15.7 A, d $i_{\rm S}$ /d t =4000 A/ μ s

 $^{^{11)}~~}Q_{\rm fr}$ includes $Q_{\rm oss}.$ Refer to Table 10 for test setup.

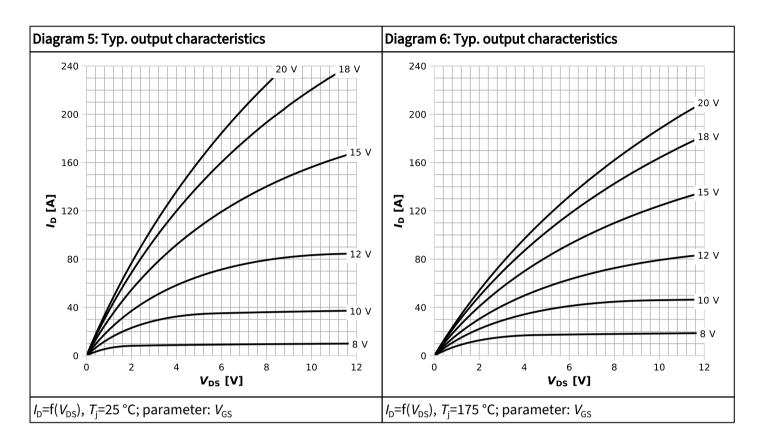


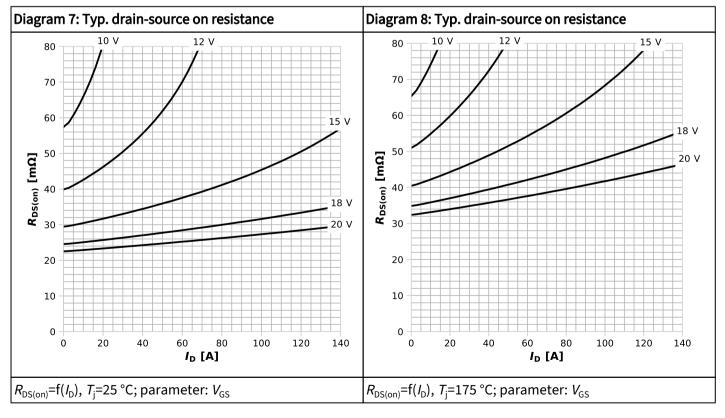
5 Electrical characteristics diagrams



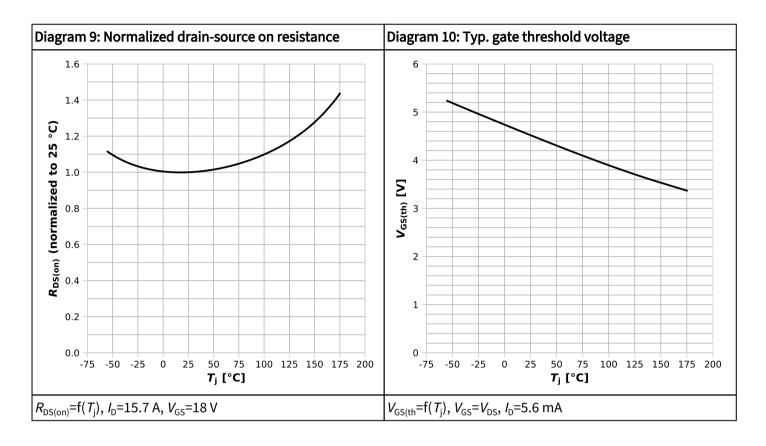


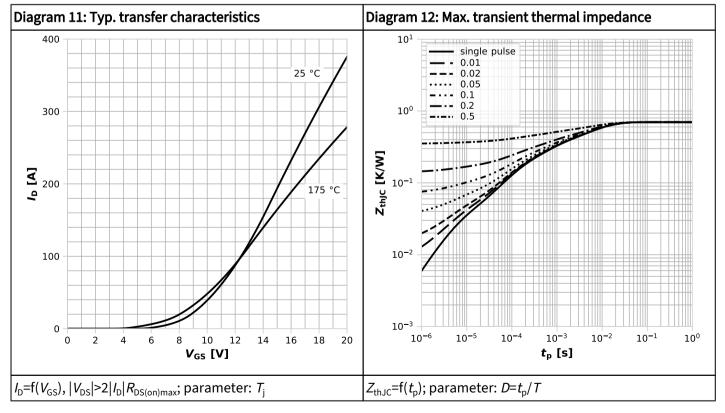




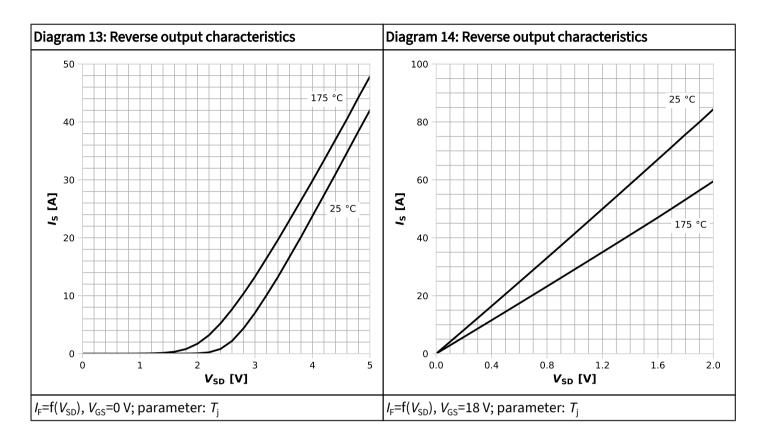


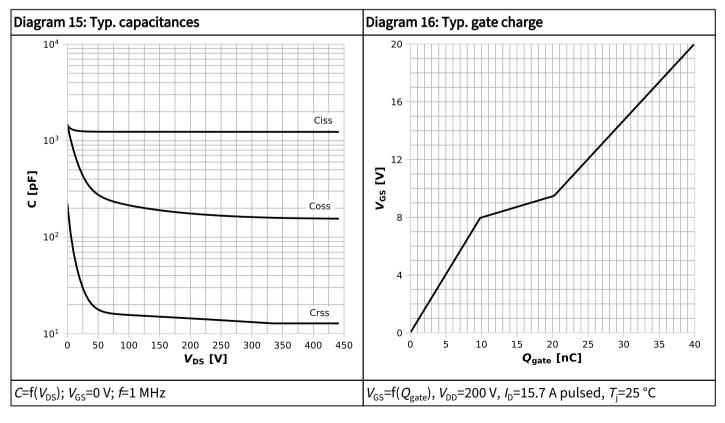




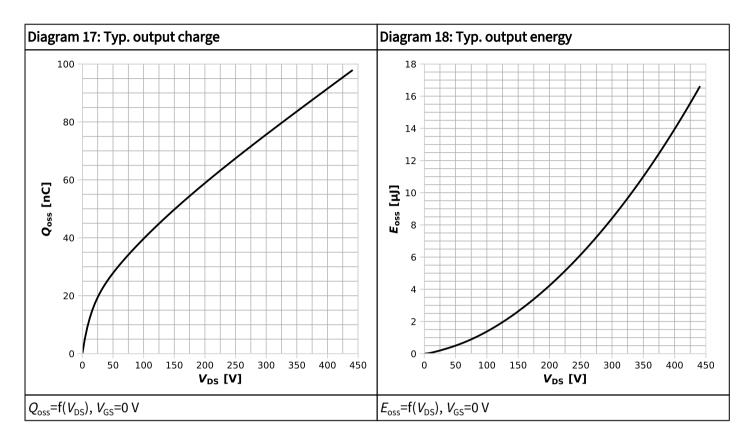


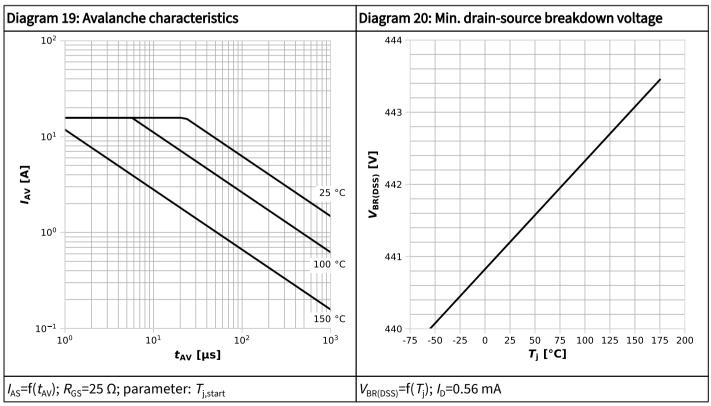




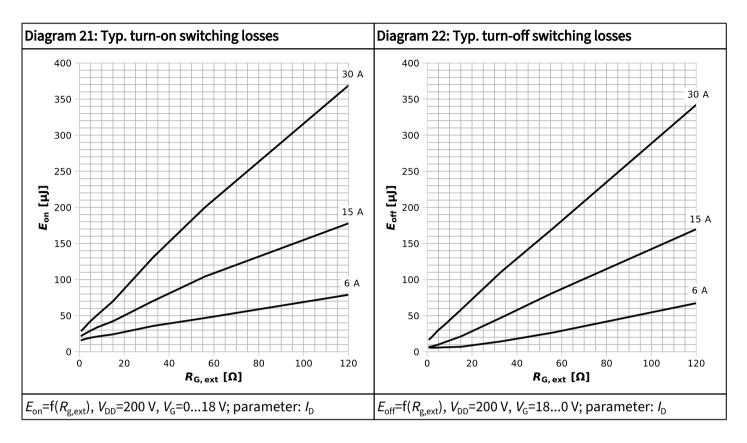


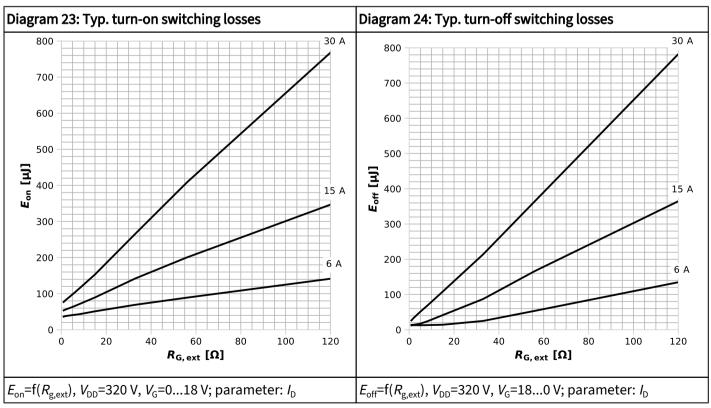














6 Test circuits

Table 9 Switching times

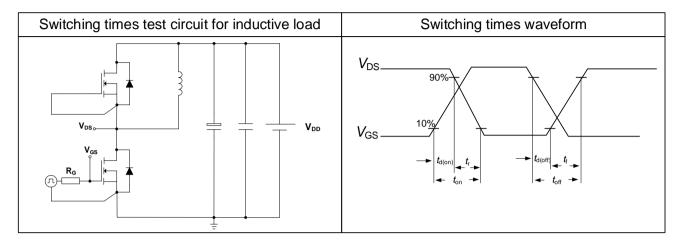
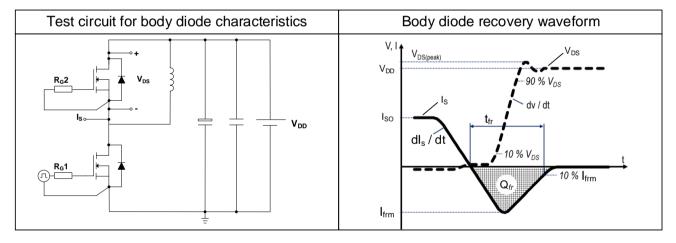
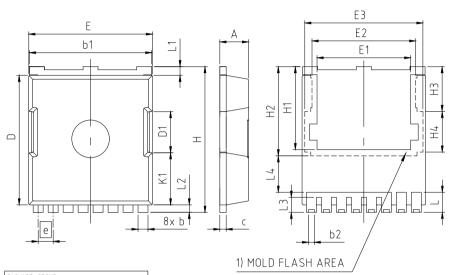


Table 10 Body diode characteristics





7 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U						
DIMENSIONS	MILLIMETERS						
DIMENSIONS	MIN.	MAX.					
Α	2.20	2.40					
b	0.70	0.90					
b1	9.70	9.90					
b2	0.42	0.50					
С	0.40	0.60					
D	10.28	10.58					
D1	3.	30					
E	9.70	10.10					
E1	7.50						
E2	8.50						
E3	9.46						
е	1.20 (BSC)						
Н	11.48 11.88						
H1	6.55	6.95					
H2	7.15						
Н3	3.	59					
H4	3.26						
N	8						
K1	4.18						
L	1.40 1.80						
L1	0.50	0.90					
L2	0.50	0.70					
L3	1.00	1.30					
L4	2.62	2.81					

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm



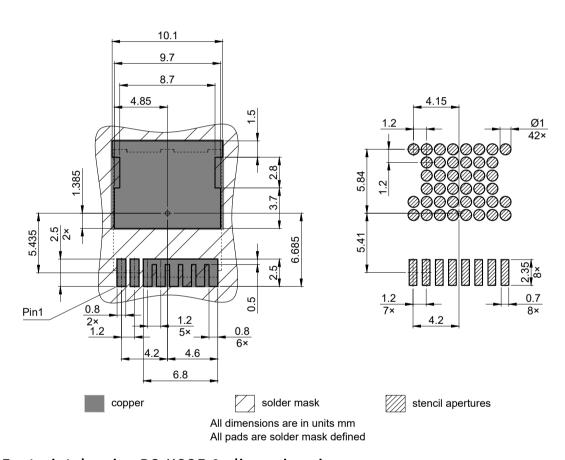


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



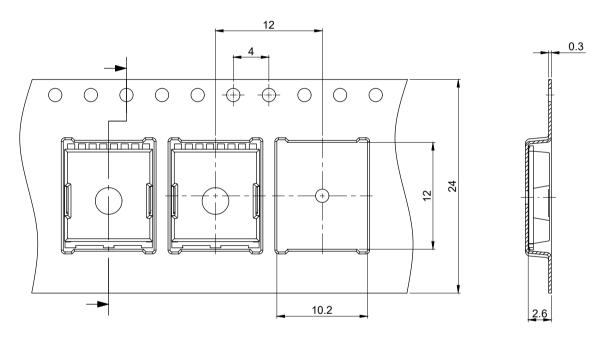


Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

Public

440V CoolSiC[™] G2 MOSFET with extended V_{DS} IMT44R025M2H



Revision history

IMT44R025M2H

Revision 2025-05-27, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-05-27	Release of final datasheet

Public

440V CoolSiC™ G2 MOSFET with extended V_{DS} IMT44R025M2H



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