

### **General Description**

The BSC109N10NS3G use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

#### **General Features**

V<sub>DS</sub> =100V I<sub>D</sub> =75A

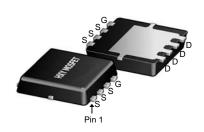
 $R_{DS(ON)}$  < 9.2m $\Omega$ @  $V_{GS}$ =10V

### **Applications**

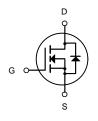
Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



DFN5X6-8L



N-Channel MOSFET

## **Package Marking and Ordering Information**

Product ID	Pack	Marking	Qty(PCS)
BSC109N10NS3G	DFN5X6-8L	109N10NS XXXX	5000

# Absolute Maximum Ratings at T<sub>j</sub>=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	100	V
Gate source voltage	VGS	±20	V
Continuous drain current <sup>1)</sup>	ID	75	Α
Pulsed drain current <sup>2)</sup>	ID, pulse	300	Α
Power dissipation <sup>3)</sup>	P <sub>D</sub>	97	W
Single pulsed avalanche energy <sup>5)</sup>	EAS	90	mJ
Operation and storage temperature	Tstg, Tj	-55 to 150	°C
Thermal resistance, junction-case	RθJC	1.3	°C/W

### N-SGT Enhancement Mode MOSFET

# **Electrical Characteristics** (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100	-	- V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V		-	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	1.0	1.6	2.5	V
D	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	7.3	9.2	mΩ
R <sub>DS(on)</sub>	note3	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	-	9	13.5	mΩ
C <sub>iss</sub>	Input Capacitance	\/ -F0\/\/ -0\/	-	2046	-	pF
Coss	Output Capacitance	$V_{DS}$ =50V, $V_{GS}$ =0V, $f$ =1.0MHz	-	865	-	pF
Crss	Reverse Transfer Capacitance	T I = I.UIVIDZ	-	25	-	pF
Qg	Total Gate Charge	V 50V L 20A	-	39.4	-	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =30A,	-	5.2	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge	V <sub>GS</sub> =10V	-	9.8	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time		-	20	-	ns
t <sub>r</sub>	Turn-on Rise Time	V <sub>DD</sub> =50V, I <sub>D</sub> =25A,	-	5.2	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	$R_G=6\Omega$ , $V_{GS}=10V$	-	49	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	12	-	ns
Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	75	А
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	300	Α
\/	Drain to Source Diode Forward	\/=0\/ L=20A	-	-	1	V
V <sub>SD</sub>	Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A				
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T -25°C	-	49	-	ns
Qrr	Body Diode Reverse Recovery Charge	T <sub>J</sub> =25℃, I <sub>F</sub> =12A,dI/dt=100A/μs	_	85	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

- 2. EAS condition:  $T_J$ =25  $^{\circ}$ C,  $V_{DD}$ =50V,  $V_G$ =10V,  $R_G$ =25 $\Omega$ , L=0.5mH,  $I_{AS}$ =19A
- 3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



# **Typical Performance Characteristics**

Figure1: Output Characteristics

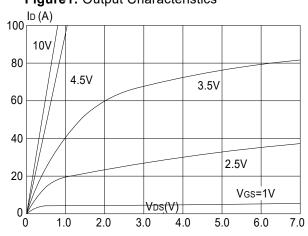


Figure 2: Typical Transfer Characteristics

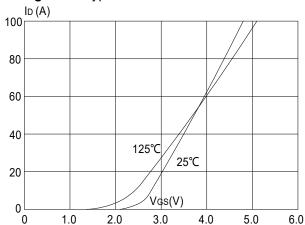


Figure 3:On-resistance vs. Drain Current

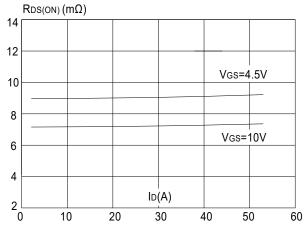


Figure 4: Body Diode Characteristics

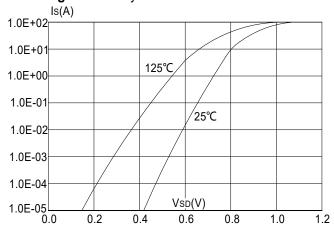


Figure 5: Gate Charge Characteristics

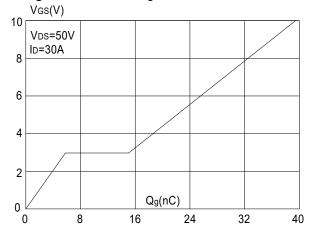
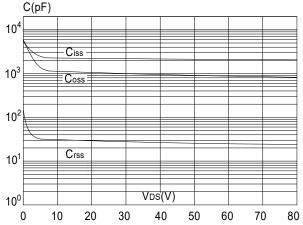
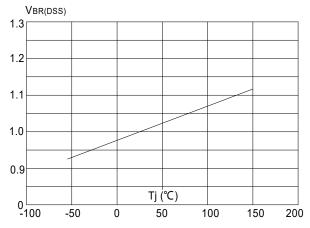


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



**Figure 8:** Normalized on Resistance vs. Junction Temperature

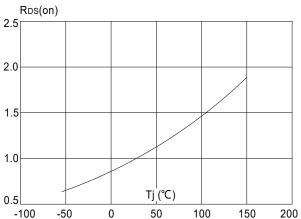
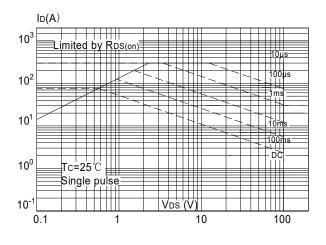
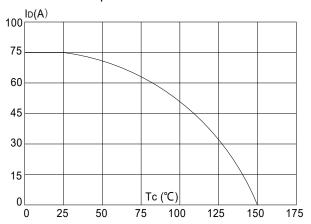


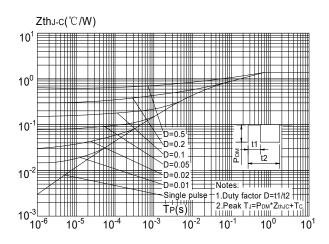
Figure 9: Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## **Test Circuit**

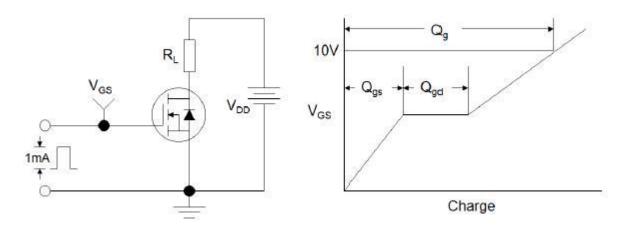


Figure1:Gate Charge Test Circuit & Waveform

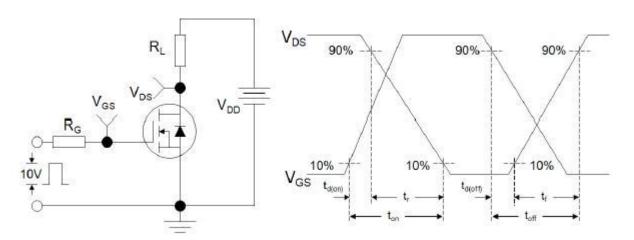


Figure 2: Resistive Switching Test Circuit & Waveforms

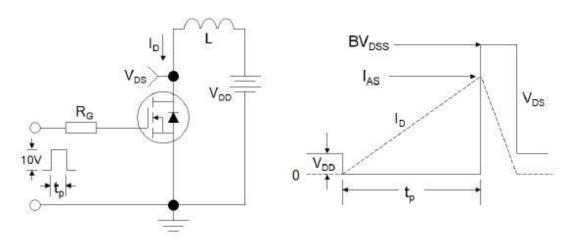
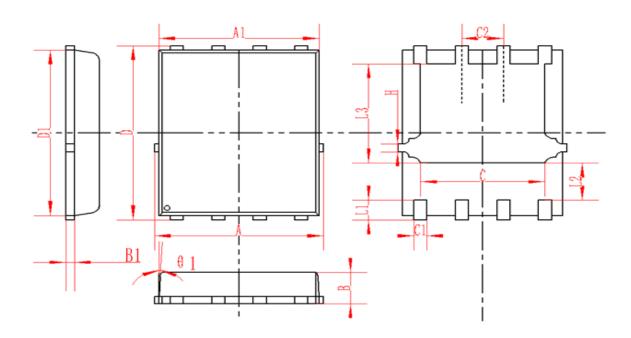


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



# **DFN5X6-8L Package Information**



SYMBOL		MM		INCH		
STIVIDOL	MIN	NOM	MAX	MIN	NOM	MAX
Α	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
В	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF		0.010REF			
С	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2		1.27TYP			0.5TYP	
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
Η	0.24	0.25	0.26	0.009	0.010	0.010



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