

MOSFET

CoolSiC™ MOSFET 650 V G2

Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC[™] MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

Features

- · Ultra-low switching losses
- Benchmark gate threshold voltage, V_{GS(th)} = 4.5 V
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance

Benefits

- · Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

Potential applications

- SMPS
- · Solar PV inverters
- · Energy storage and battery formation
- UPS
- · EV charging infrastructure
- · Motor drives

Product validation

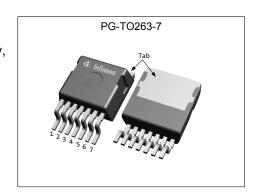
Fully qualified according to JEDEC for Industrial Applications

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.



Parameter	Value	Unit			
$V_{\rm DSS}$ over full $T_{\rm j,range}$	650	V			
R _{DS(on),typ}	14.5	mΩ	mΩ		
R _{DS(on),max}	18	mΩ			
$Q_{G,typ}$	79	nC			
$I_{ m D,pulse}$	398	A			
Q _{oss} @ 400 V	148	nC			
E _{oss} @ 400 V	20.1	μJ			

Type / Ordering Code	Package	Marking	Related Links
IMBG65R015M2H	PG-TO263-7	65R015M2	see Appendix A



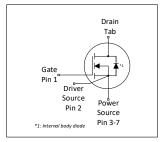










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1 Maximum ratings at $T_j = 25$ °C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Damamatan	Symbol		Value	s		Note / Took Condition
Parameter		Min.	Тур.	Max.	Unit	Note / Test Condition
Continuous DC drain current ¹⁾	$I_{ m DDC}$	-	-	115 84	А	T _C = 25 °C T _C = 100 °C
Peak drain current ²⁾	I _{DM}	-	-	398	Α	T _C = 25 °C, V _{GS} = 18 V
Avalanche energy, single pulse	E _{AS}	-	-	372	mJ	$I_{\rm D}$ = 13.9 A, $V_{\rm DD}$ = 50 V; see table 11
Avalanche energy, repetitive	E AR	-	-	1.86	mJ	I_D = 13.9 A, V_{DD} = 50 V; see table 11
Avalanche current, single pulse	I _{AS}	-	-	13.9	Α	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	V _{DS} = 0400 V
Gate source voltage (static) ³⁾	V _{GS}	-7	-	23	V	-
Gate source voltage (transient)	V _{GS}	-10	-	25	V	$t_p \le 500$ ns, duty cycle ≤ 1 %
Power dissipation	P _{tot}	-	-	416	W	T _C = 25 °C
Storage temperature	$T_{ m stg}$	-55	-	150	°C	-
Operating junction temperature	T _j	-55	-	175	°C	-
Mounting torque	-	-	-	-	Ncm	-
Continuous reverse drain current ¹⁾	I _{SDC}	-	-	115 77	А	V _{GS} = 18 V, T _C = 25 °C V _{GS} = 0 V, T _C = 25 °C
Peak reverse drain current ²⁾	I _{SM}	-	-	398 121	А	$T_{\rm C}$ = 25 °C, $t_{\rm p}$ ≤ 250 ns $T_{\rm C}$ = 25 °C
Insulation withstand voltage	V _{ISO}	-	-	n.a.	V	$V_{\rm rms}$, $T_{\rm C}$ = 25 °C, t = 1 min

¹⁾ Limited by $T_{\rm J,max}$ ²⁾ Pulse width $t_{\rm pulse}$ limited by $T_{\rm j,max}$.
³⁾ The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.



2 Thermal characteristics

Table 3 Thermal characteristics

Devenuetor	Complete	Values			11:4	Nata / Tank Open Hilliam	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Thermal resistance, junction - case	R _{th(j-c)}	-	-	0.36	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.	
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1	

3 Operating range

Table 4 Operating range

Davamatav	Cumbal	Values			l lmi4	Note / Toet Condition
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Recommended turn-on voltage	V _{GS(on)}	-	18	-	V	-
Recommended turn-off voltage	V _{GS(off)}	-	0	-	V	-



4 Electrical characteristics at $T_j = 25$ °C, unless otherwise specified

Table 5 **Static characteristics**

D	0	Values			Ī., .,	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition
Drain-source voltage	V _{DSS}	650	-	-	V	$V_{GS} = 0 \text{ V}, I_D = 1.30 \text{ mA}$
Gate threshold voltage ¹⁾	V _{GS(th)}	3.5	4.5	5.6	V	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 13.0 \text{ mA}$
Zero gate voltage drain current	I _{DSS}	-	1 3	75 -	μΑ	$V_{\rm DS} = 650 \text{ V}, \ V_{\rm GS} = 0 \text{ V}, \ T_{\rm j} = 25 \text{ °C} $ $V_{\rm DS} = 650 \text{ V}, \ V_{\rm GS} = 0 \text{ V}, \ T_{\rm j} = 175 \text{ °C} $
Gate-source leakage current	I _{GSS}	-	-	100	nA	V _{GS} = 20 V, V _{DS} = 0 V
Drain-source on-state resistance	R _{DS(on)}	- - - -	18.9 14.5 13.2 23.7	- 18 - -	mΩ	$V_{\rm GS} = 15 \text{ V}, I_{\rm D} = 64.2 \text{ A}, T_{\rm j} = 25 ^{\circ}\text{C}$ $V_{\rm GS} = 18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, T_{\rm j} = 25 ^{\circ}\text{C}$ $V_{\rm GS} = 20 \text{ V}, I_{\rm D} = 64.2 \text{ A}, T_{\rm j} = 25 ^{\circ}\text{C}$ $V_{\rm GS} = 18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, T_{\rm j} = 175 ^{\circ}\text{C}$
Internal gate resistance	$R_{G,int}$	-	2.1	-	Ω	f = 1 MHz

 $^{^{1)}}$ Tested after 1 ms pulse at V_{GS} = +20 V. "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.



Table 6 **Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly. Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Davometer	Cumbal		Value	s	l lmit		
Parameter	Symbol	Min.	. Typ. Max.		Unit	Note / Test Condition	
Input capacitance	C _{iss}	-	2792	-	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 400 \text{ V}, f = 250 \text{ kHz}$	
Reverse transfer capacitance	C _{rss}	-	16	-	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 400 \text{ V}, f = 250 \text{ kHz}$	
Output capacitance ¹⁾	Coss	-	207	269	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 400 \text{ V}, f = 250 \text{ kHz}$	
Output charge ¹⁾	Qoss	-	148	193	nC	calculation based on Coss	
Effective output capacitance, energy related ²⁾	C _{o(er)}	-	251	-	pF	$V_{GS} = 0 \text{ V},$ $V_{DS} = 0400 \text{ V}$	
Effective output capacitance, time related ³⁾	C _{o(tr)}	-	371	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0400 V	
Turn-on delay time	$t_{\sf d(on)}$	-	11.6	-	ns	$V_{\rm DD} = 400 \text{ V}, \ V_{\rm GS} = 0/18 \text{ V}, \ I_{\rm D} = 64.2 \text{ A}, \ R_{\rm G,ext} = 1.8 \ \Omega;$ see table 10	
Rise time	t _r	-	14.7	-	ns	$V_{\rm DD} = 400 \text{ V}, \ V_{\rm GS} = 0/18 \text{ V}, \ I_{\rm D} = 64.2 \text{ A}, \ R_{\rm G,ext} = 1.8 \ \Omega;$ see table 10	
Turn-off delay time	$t_{\sf d(off)}$	-	22	-	ns	$V_{\rm DD} = 400 \text{ V}, \ V_{\rm GS} = 0/18 \text{ V}, \ I_{\rm D} = 64.2 \text{ A}, \ R_{\rm G,ext} = 1.8 \ \Omega;$ see table 10	
Fall time	t _f	-	6.4	-	ns	$V_{\rm DD} = 400 \text{ V}, V_{\rm GS} = 0/18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, R_{\rm G,ext} = 1.8 \Omega;$ see table 10	
Turn-ON switching losses ⁴⁾	Eon	-	84	-	μJ	$V_{\rm DD} = 400 \text{ V}, V_{\rm GS} = 0/18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, R_{\rm G,ext} = 1.8 \Omega$	
Turn-OFF switching losses ⁴⁾	E _{off}	-	138	-	μJ	$V_{\rm DD} = 400 \text{ V}, V_{\rm GS} = 0/18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, R_{\rm G,ext} = 1.8 \Omega$	
Total switching losses ⁴⁾	E _{tot}	-	222	-	μJ	$V_{\rm DD} = 400 \text{ V}, V_{\rm GS} = 0/18 \text{ V}, I_{\rm D} = 64.2 \text{ A}, R_{\rm G,ext} = 1.8 \Omega$	

Table 7 **Gate charge characteristics**

Doromotor	Cumbal	Values			I Incid	Nata / Tant Candition	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Plateau gate to source charge	$Q_{GS(pl)}$	-	20	-	nC	$V_{\text{DD}} = 400 \text{ V}, I_{\text{D}} = 64.2 \text{ A}, V_{\text{GS}} = 0 \text{ to } 18 \text{ V}$	
Gate to drain charge	Q_{GD}	-	15	-	nC	V_{DD} = 400 V, I_{D} = 64.2 A, V_{GS} = 0 to 18 V	
Total gate charge	Q_G	-	79	-	nC	$V_{\rm DD}$ = 400 V, $I_{\rm D}$ = 64.2 A, $V_{\rm GS}$ = 0 to 18 V	

 $^{^{1)}}$ Maximum specification is defined by calculated six sigma upper confidence bound $^{2)}$ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{\rm oss}$ while $V_{\rm DS}$ is rising from 0 to 400 V. $^{3)}$ $C_{\rm o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{\rm oss}$ while $V_{\rm DS}$ is rising from 0 to 400 V. $^{4)}$ MOSFET used in half-bridge configuration without external diode

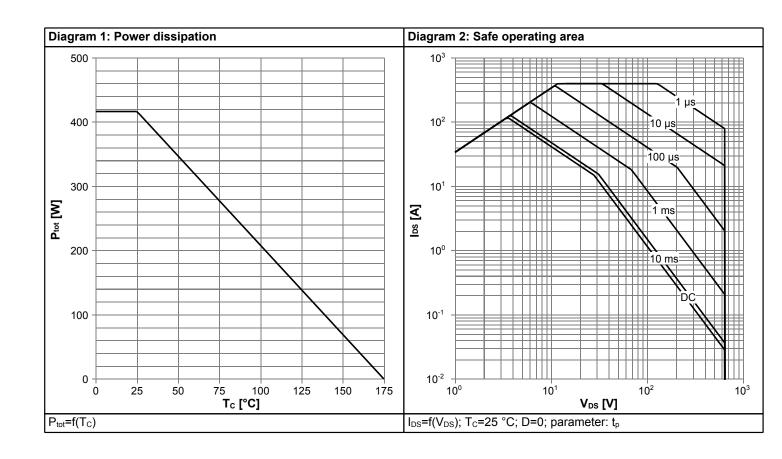


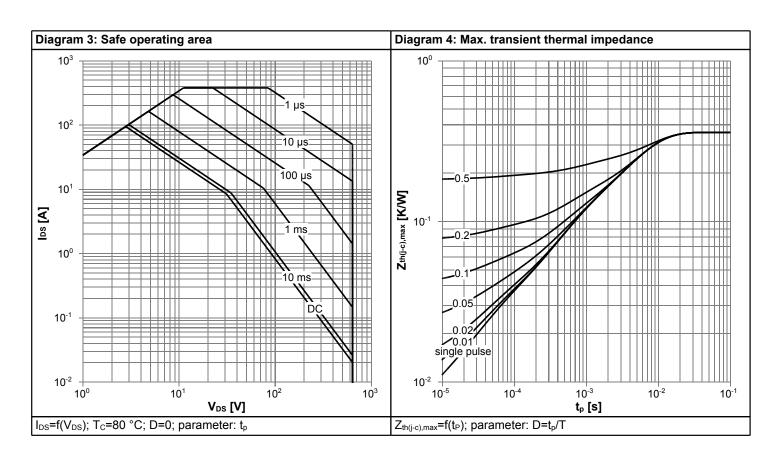
Table 8 Reverse diode characteristics

Damanastan	0	Values				Note / Took Condition	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note / Test Condition	
Drain-source reverse voltage	V _{SD}	-	4.3	-	V	$V_{GS} = 0 \text{ V}, I_S = 64.2 \text{ A}, T_j = 25 \text{ °C}$	
MOSFET forward recovery time	t fr	-	21.5 16.0	-	ns	$V_{\rm DD} = 400 \text{ V}, I_{\rm S} = 64.2 \text{ A},$ $di_{\rm S}/dt = 1000 \text{ A/}\mu\text{s}; \text{ see table 9}$ $V_{\rm DD} = 400 \text{ V}, I_{\rm S} = 64.2 \text{ A},$ $di_{\rm S}/dt = 4000 \text{ A/}\mu\text{s}; \text{ see table 9}$	
MOSFET forward recovery charge ¹⁾	Qfr	-	154 258	-	nC	$V_{\rm DD} = 400 \text{ V}, I_{\rm S} = 64.2 \text{ A},$ $di_{\rm S}/dt = 1000 \text{ A/}\mu\text{s}; \text{ see table 9}$ $V_{\rm DD} = 400 \text{ V}, I_{\rm S} = 64.2 \text{ A},$ $di_{\rm S}/dt = 4000 \text{ A/}\mu\text{s}; \text{ see table 9}$	
MOSFET peak forward recovery current	I frm	-	14.3 32.3	-	A	$V_{\rm DD}$ = 400 V, $I_{\rm S}$ = 64.2 A, $di_{\rm S}/dt$ = 1000 A/ μ s; see table 9 $V_{\rm DD}$ = 400 V, $I_{\rm S}$ = 64.2 A, $di_{\rm S}/dt$ = 4000 A/ μ s; see table 9	

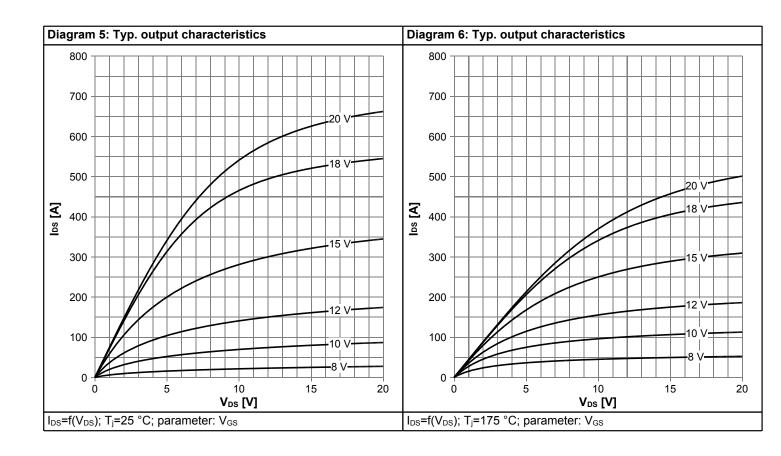


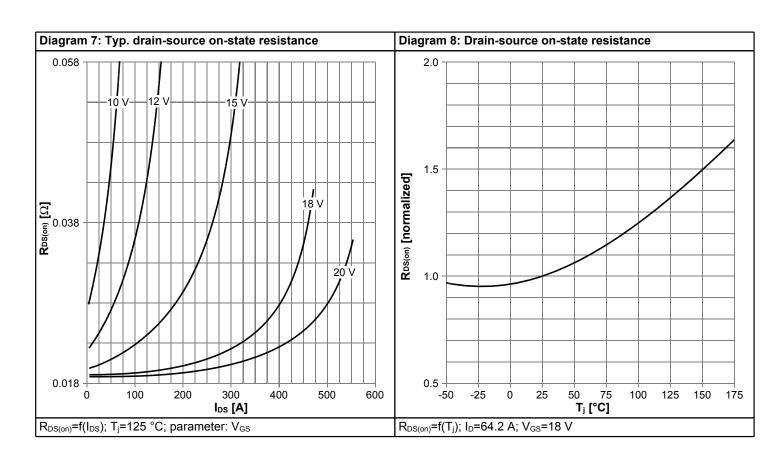
5 Electrical characteristics diagrams



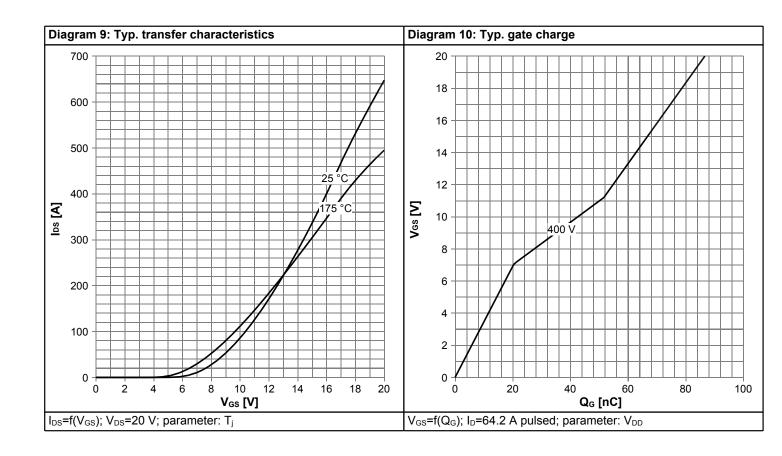


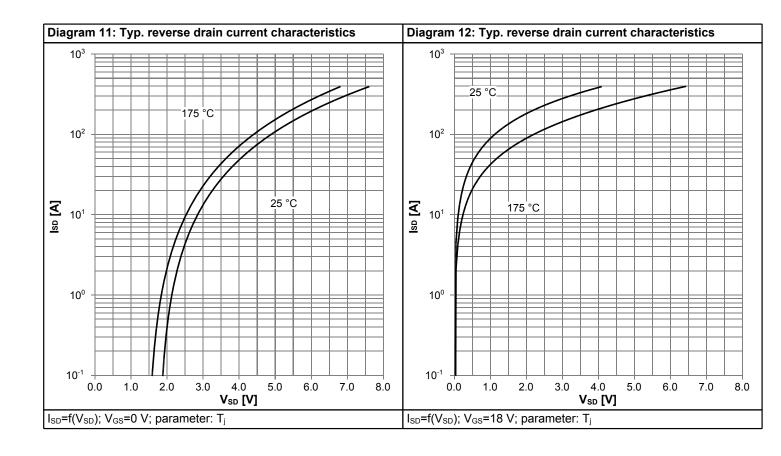




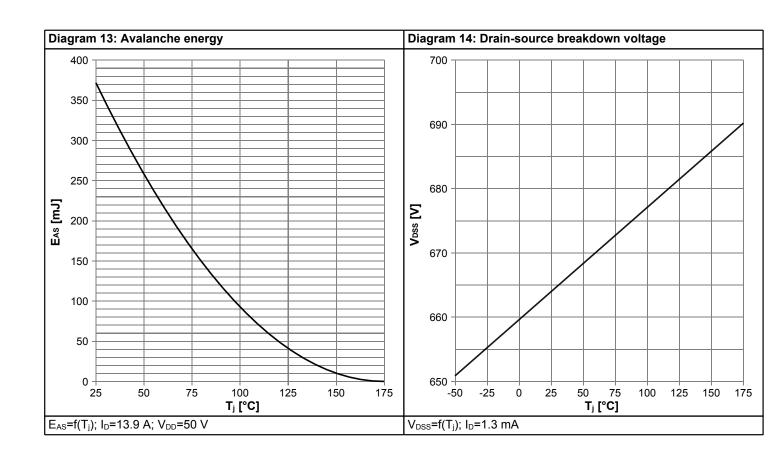


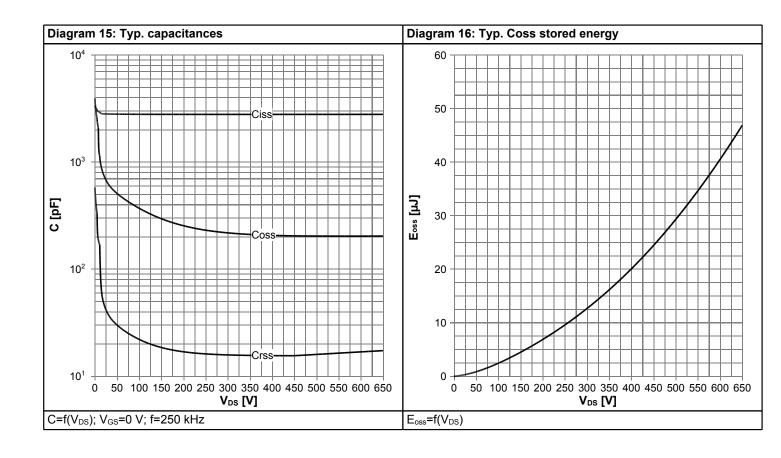




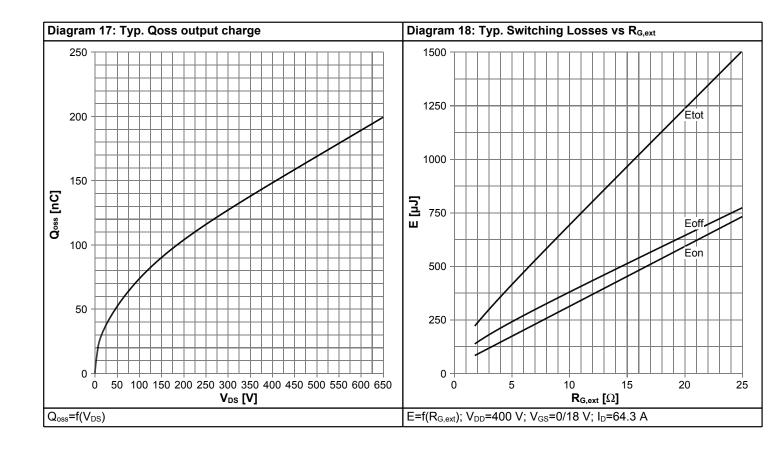


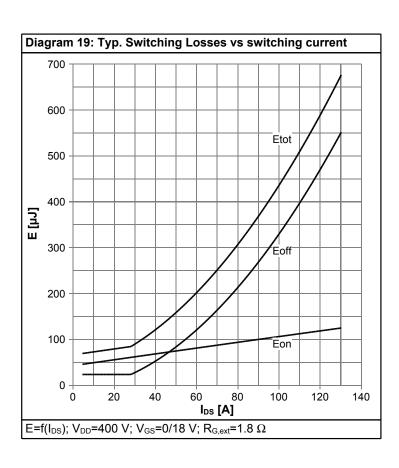














6 Test Circuits

Table 9 Body diode characteristics

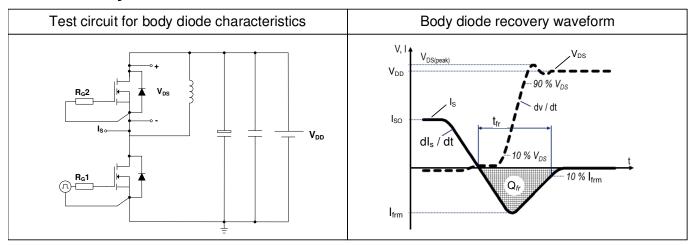


Table 10 Switching times

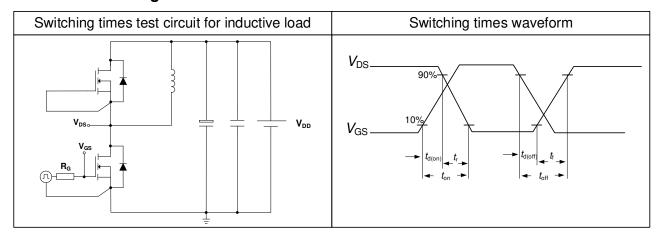
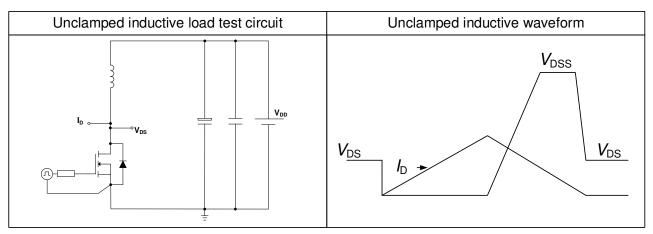


Table 11 Unclamped inductive load





7 Package Outlines

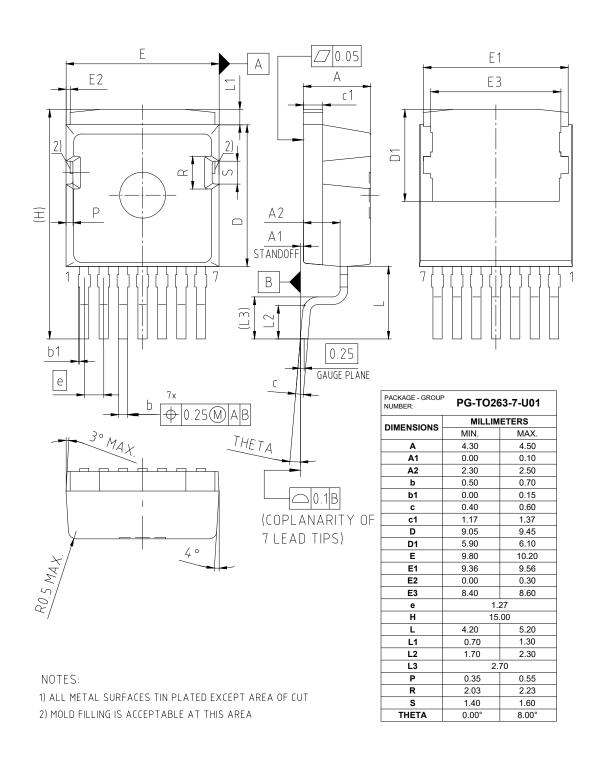


Figure 1 Outline PG-TO263-7, dimensions in mm



8 Appendix A

Table 12 Related Links

- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage: www.infineon.com
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 application note: www.infineon.com
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com



Revision History

IMBG65R015M2H

Revision: 2024-03-05, Rev. 2.2

Previous Revision

	1 10 VIOUS IX	CVIOIOII		
	Revision	Date	Subjects (major changes since last revision)	
2.0 2023-09-26 Release of final version				
	2.1	2024-02-29	updated simulation model; included Eon and Eoff data and diagrams	
	2.2	2024-03-05	minor layout changes	

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