

# MOSFET - Power, Single N-Channel

40 V, 9.5 mΩ, 43 A

NVTYS010N04CL

## Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	40	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Notes 1, 2, 3, 4)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	43	A
		T <sub>C</sub> = 100°C		30	
Power Dissipation R <sub>θJC</sub> (Notes 1, 2, 3)	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub>	32	W
		T <sub>C</sub> = 100°C		16	
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 3, 4)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	13	A
		T <sub>A</sub> = 100°C		9.4	
Power Dissipation R <sub>θJA</sub> (Notes 1, 3)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	3.0	W
		T <sub>A</sub> = 100°C		1.5	
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	162	A
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	26	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 2.2 A)			E <sub>AS</sub>	57	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

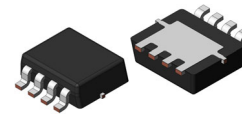
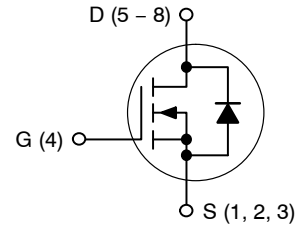
## THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	$R_{\theta JC}$	4.8	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	49.3	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

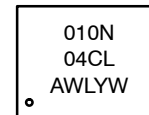
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	9.5 mΩ @ 10 V	43 A
	15.5 mΩ @ 4.5 V	

## N-Channel



LPAK8  
3.3x3.3  
CASE 760AD

## MARKING DIAGRAM



010N04CL = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVTYS010N04CL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V, T <sub>J</sub> = 25°C			10	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 20 μA	1.2		2.2	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		7.9	9.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		12.4	15.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		43		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		710		pF
Output Capacitance	C <sub>oss</sub>			261		
Reverse Transfer Capacitance	C <sub>rss</sub>			12		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 20 A		5.5		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.2		
Gate-to-Source Charge	Q <sub>GS</sub>			2.1		
Gate-to-Drain Charge	Q <sub>GD</sub>			2		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 20 A		12		nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 20 A, R <sub>G</sub> = 1.0 Ω		9.0		ns
Rise Time	t <sub>r</sub>			4		
Turn-Off Delay Time	t <sub>d(off)</sub>			12		
Fall Time	t <sub>f</sub>			4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A, T <sub>J</sub> = 25°C		0.8	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A, T <sub>J</sub> = 125°C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 20 A		21		ns
Charge Time	t <sub>a</sub>			10		
Discharge Time	t <sub>b</sub>			11		
Reverse Recovery Charge	Q <sub>RR</sub>			6		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

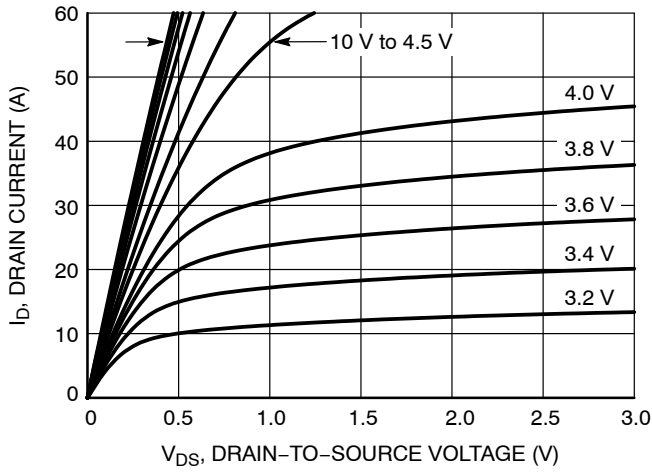


Figure 1. On-Region Characteristics

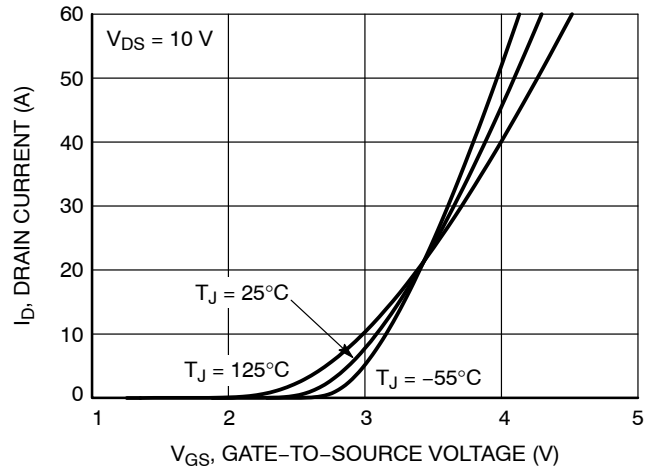


Figure 2. Transfer Characteristics

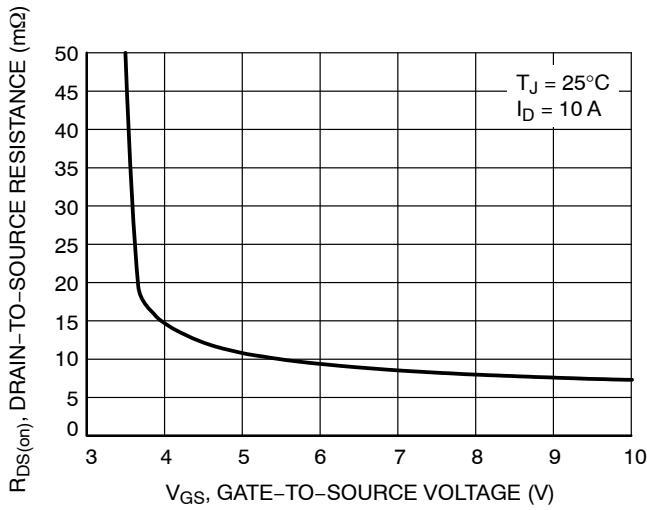


Figure 3. On-Resistance vs. Gate-to-Source Voltage

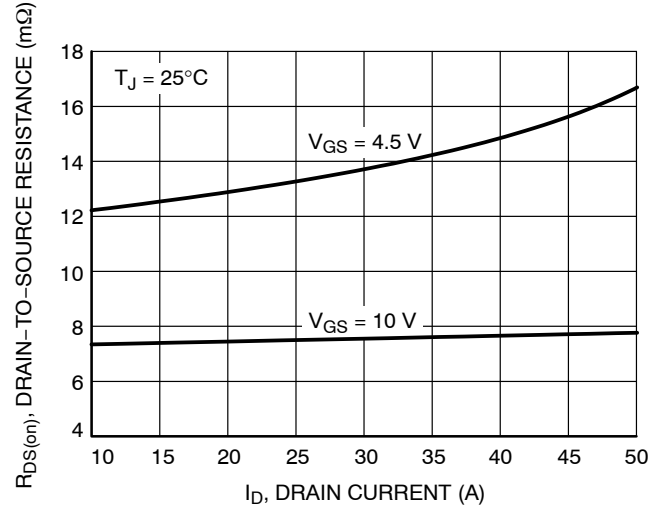


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

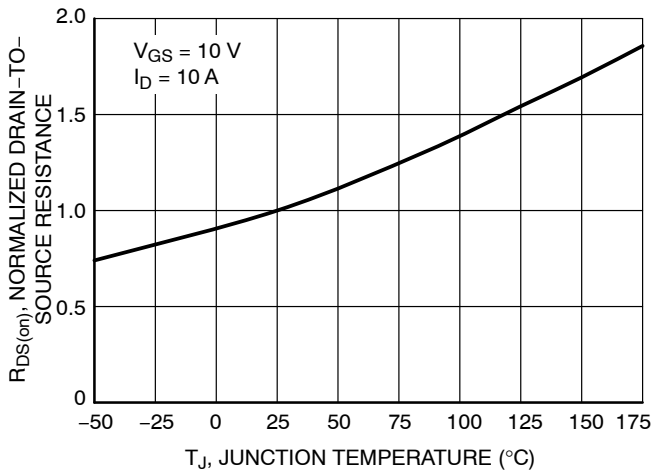


Figure 5. On-Resistance Variation with Temperature

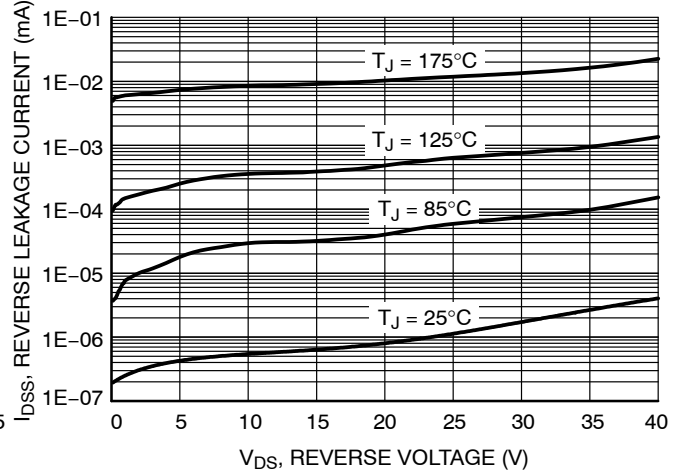


Figure 6. Reverse Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

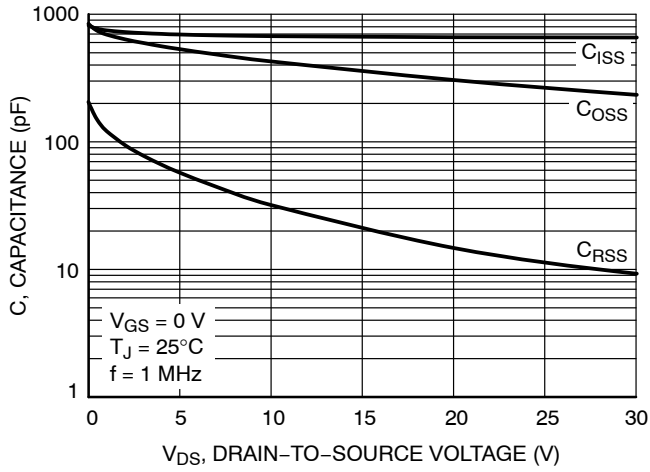


Figure 7. Capacitance Variation

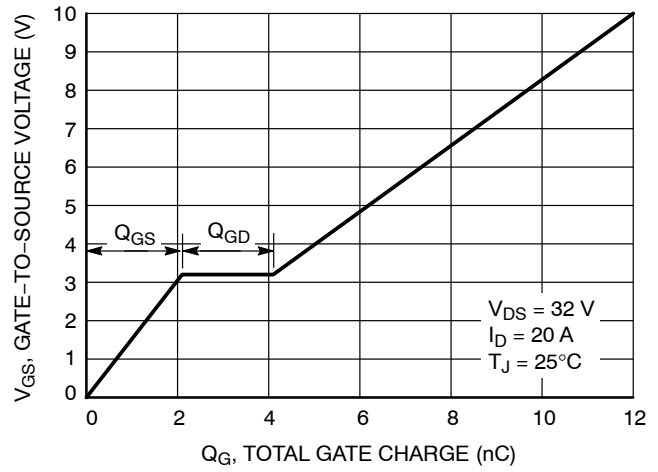


Figure 8. Gate-to-Source Voltage vs. Total Charge

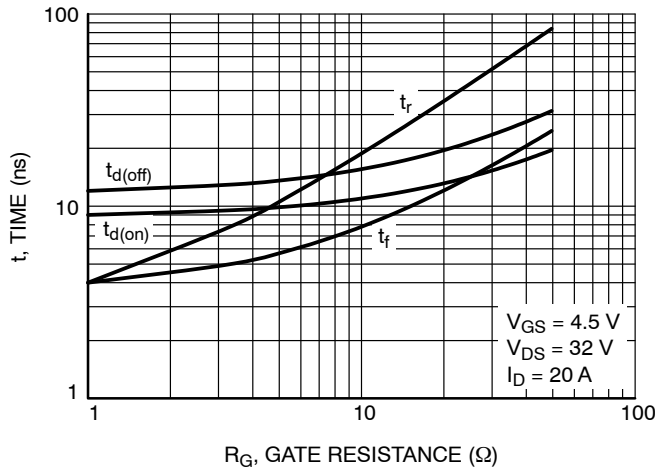


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

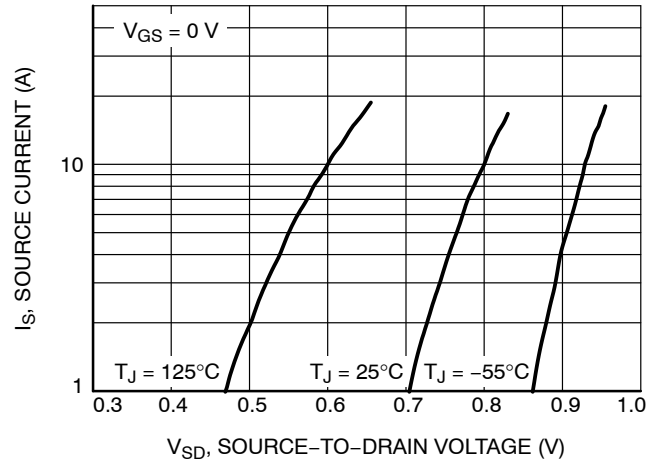


Figure 10. Diode Forward Voltage vs. Current

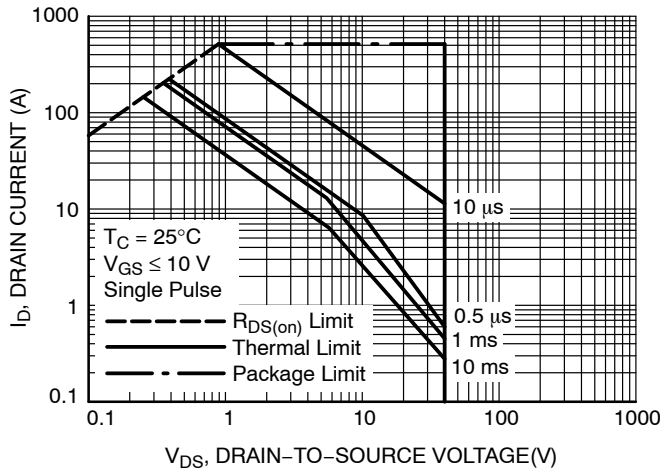


Figure 11. Maximum Rated Forward Biased Safe Operating Area

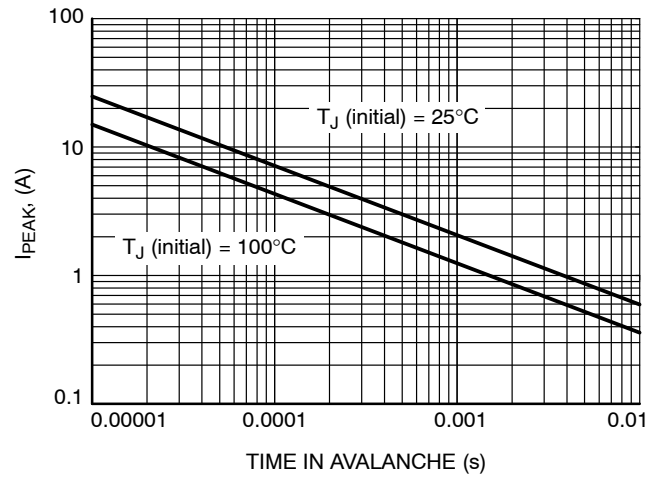


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVTYS010N04CL

## TYPICAL CHARACTERISTICS

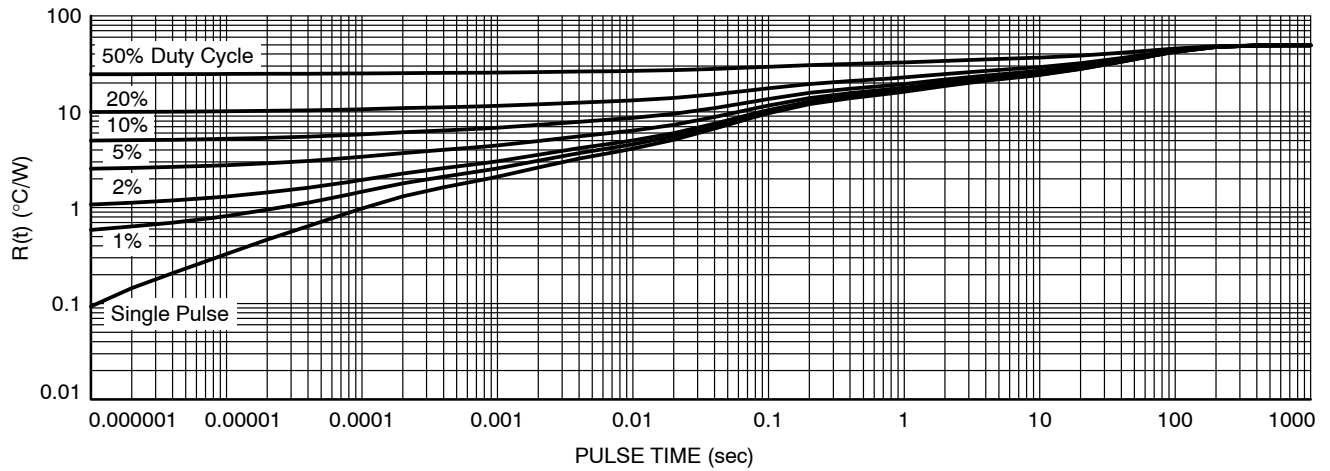
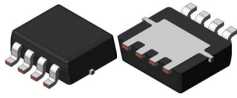


Figure 13. Thermal Characteristics

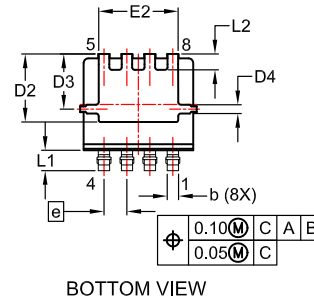
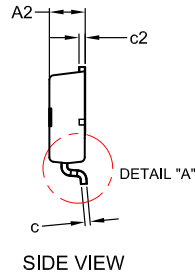
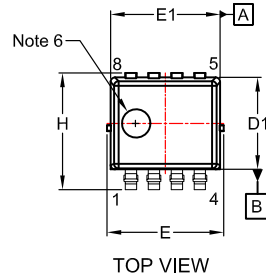
### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVTYS010N04CLTWG	010N 04CL	LFPAK33	3000 / Tape & Reel

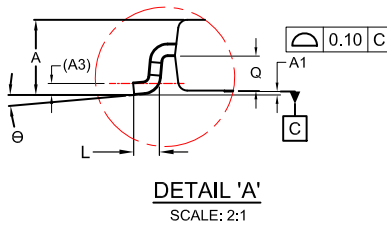
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


**LPAK8 3.3x3.3, 0.65P**  
**CASE 760AD**  
**ISSUE E**

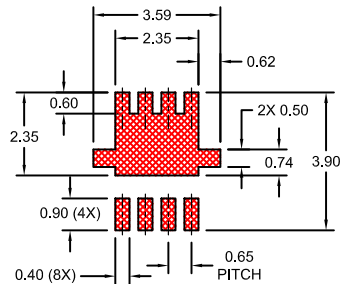
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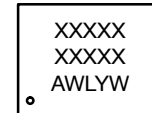
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
Θ	0°	4°	8°


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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