

N-Channel MOSFET

Applications:

- •Power switch circuit of adaptor and charger;
- LED backlight driver;
- Synchronous rectification

Lead Free Package and Finish

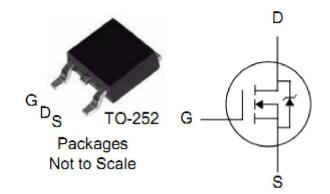
V_{DSS}	$R_{DS(ON)}(Typ.)$	I _D
60V	$23 m\Omega$	25A

Features:

- Fast Switching
- Low ON Resistance
- Low Gate Charge
- Low Reverse transfer capacitances
- •100% Single Pulse avalanche energy Test

Ordering Information

PART NUMBER	PACKAGE	BRAND	
FTD36N06NA	TO-252	IPS	



Absolute Maximum Ratings T_J =25 $^{\circ}$ C unless otherwise specified

Symbol	Parameter	FTD36N06NA	Units
V _{DSS}	Drain-to-Source Voltage	60	V
1	Continuous Drain Current T _C = 25 °C	25	Α
I _D	Continuous Drain Current T _C =100℃	17.5	Α
I _{DM}	Pulsed Drain Current T _C = 25 °C (NOTE *1)	100	Α
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy(NOTE *2)	56.2	mJ
P _D	Power Dissipation T _C = 25 °C	36.2	W
T_{J} and T_{STG}	Operating Junction and Storage Temperature Range	150, -55 to150	$^{\circ}$ C

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
В	Junction-to-Case	3.45		Water cooled heatsink, P _D adjusted for a
$R_{\theta JC}$	Junction-to-Case	3.45	$^{\circ}$ C/W	peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	111.5		1 cubic foot chamber, free air.



OFF Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60			V	V _{GS} =0V, I _D =250μA
I _{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS} =60V, V_{GS} =0V T_{J} =25°C
				100		V _{DS} =48V, V _{GS} =0V T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage			+100	nΛ	V _{GS} =+20V
	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -20V

ON Characteristics $T_J=25^{\circ}\mathbb{C}$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
R _{DS(ON)}	StaticDrain-to-Source On-Resistance		23	29	mΩ	V_{GS} =10V, I_D =19A	
			30	38	mΩ	V_{GS} =4.5V, I_D =19A	
$V_{GS(TH)}$	Gate Threshold Voltage	1	1.5	2	V	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	
Pulse width	Pulse width ≤300µs; duty cycle≤ 2%						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
R _g	Gate resistance		1.9		Ω	f =1.0MHz
C _{iss}	Input Capacitance		939		pF	V_{GS} = 0V, V_{DS} = 30V f = 1.0MHz
C _{oss}	Output Capacitance		73.5			
C _{rss}	Reverse Transfer Capacitance		52.7			
Q _g	Total Gate Charge		21.2			1 -204 \/ -20\/
Q_{gs}	Gate-to-Source Charge		3.6		nC	$I_D = 20A, V_{DD} = 30V$ $V_{GS} = 10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge		5.5			

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
t _{d(ON)}	Turn-on Delay Time		8.4		- ns	V_{DD} =30V, I_{D} =20A, V_{GS} =10V R_{G} =3 Ω
t _{rise}	Rise Time		8.5			
t _{d(OFF)}	Turn-Off Delay Time		35.4			
t _{fall}	Fall Time		4.8			



Source-Drain Diode Characteristics

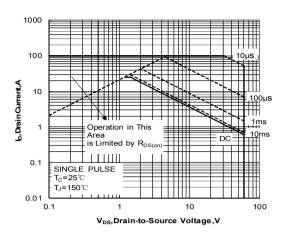
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
I _S	Continuous Source Current			25	А	- T _C =25℃
	(Body Diode)					
I _{SM}	Maximum Pulsed Current			100	А	
	(Body Diode)					
V _{SD}	Diode Forward Voltage			1.2	V	I _{SD} =20A, V _{GS} =0V
t _{rr}	Reverse Recovery Time		18.8		ns	di/dt=100A/us
Q _{rr}	Reverse Recovery Charge		13.4		nC	IF=20A
Pulse width ≤300µs; duty cycle ≤ 2%						

Notes:

- *1. Repetitive rating; pulse width limited by maximum junction temperature.
- *2. L=0.5mH, V_{DD} =30V,Ias=15A Start T_J =25 $^{\circ}$ C
- *3. Recommend soldering temperature defined by IPC/JEDEC J-STD 020



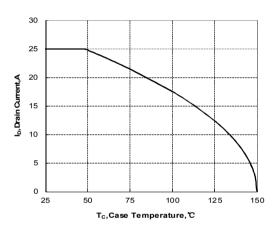
Characteristics Curve:



T_c, Case Temperature, °C

Figure 1 . Maximum Safe Operating Area

Figure 2. Maximum Power Dissipation vs Case Temperature



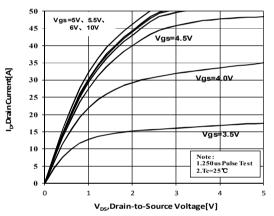


Figure 3. Maximum Continuous Drain Current vs Case Temperature

Figure 4. Typical output Characteristics

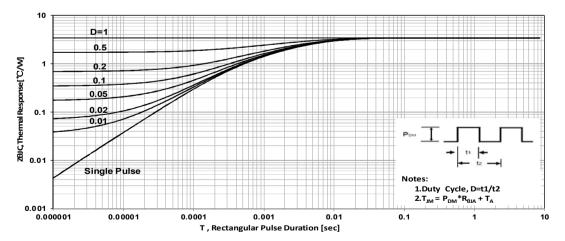


Figure 5 Maximum Effective Thermal Impedance, Junction to Case



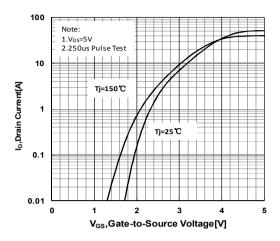
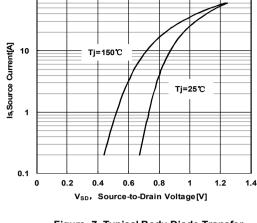


Figure 6 Typical Transfer Characteristics



100

Figure 7 Typical Body Diode Transfer Characteristics

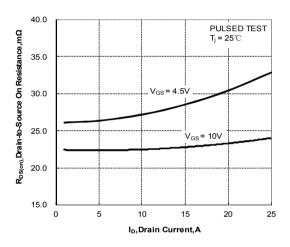


Figure 8. Drain-to-Source On Resistance vs Drain Current

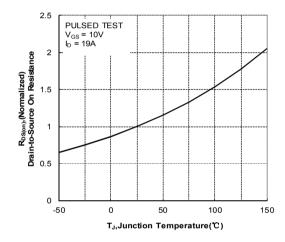


Figure 9. Normalized On Resistance vs Junction Temperature

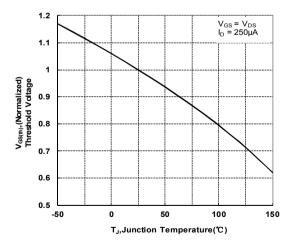


Figure 10. Normalized Threshold Voltage vs Junction Temperature

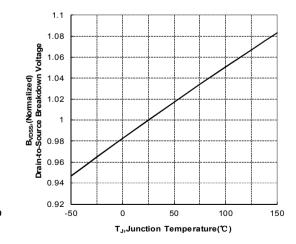


Figure 11. Normalized Breakdown Voltage vs Junction Temperature





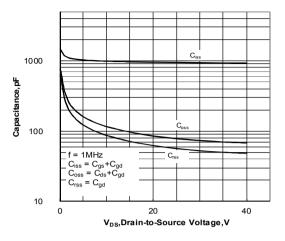


Figure 12. Capacitance Characteristics

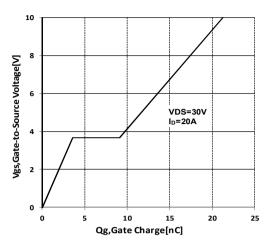


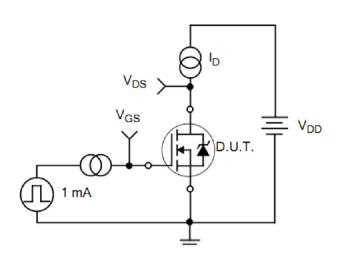
Figure 13 Typical Gate Charge vs Gate to Source Voltage

Figure 15. Gate Charge Waveforms



Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit



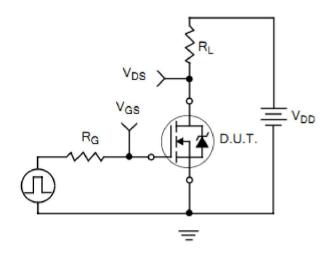
V_{DS}

Miller
Region

V_{GS(TH)}

Figure 16. Resistive Switching Test Circuit

Figure 17. Resistive Switching Waveforms



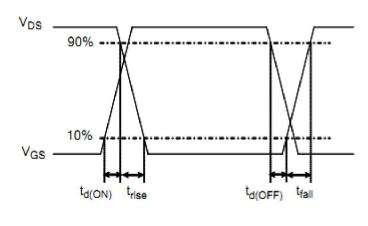






Figure 18. Diode Reverse Recovery Test Circuit

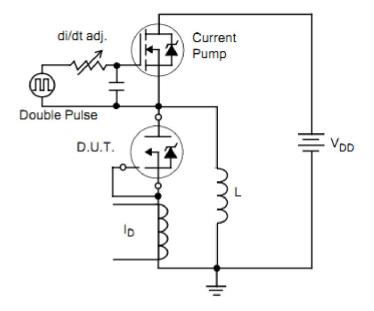


Figure 19. Diode Reverse Recovery Waveform

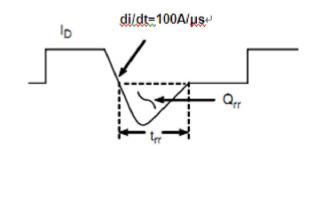
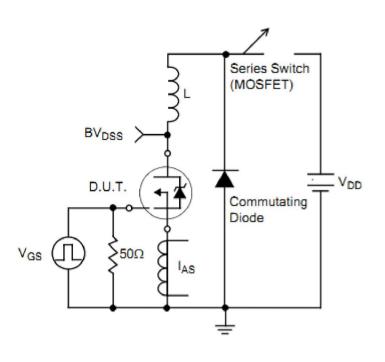
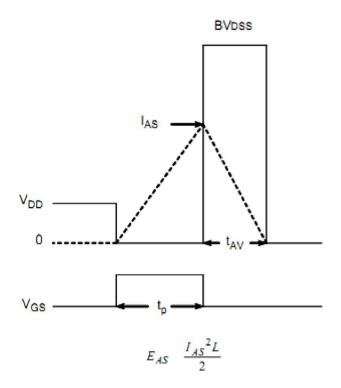


Figure 20. Unclamped Inductive Switching Test Circuit

Figure 21. Unclamped Inductive Switching Waveform







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