

N-Channel Power MOSFET

FEATURES

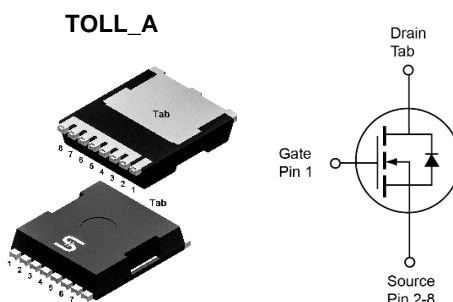
- Excellent FOM
- Ultra low $r_{DS(on)}$
- 100% UIS & R_g tested
- RoHS compliant
- Halogen-free

APPLICATIONS

- Solenoid and motor drivers
- DC-DC converters
- Load Switch
- SMPS

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	80	V
$R_{DS(on)}$ (max)	1.8	mΩ
$Q_{g,typ}$	179	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$ I_D	334	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$ I_D	300	A
	$T_C = 100^\circ\text{C}$ I_D	211	
Pulsed Drain Current (Note 2)	I_{DM}	1336	A
Total Power Dissipation	$T_C = 25^\circ\text{C}$ P_D	357	W
	$T_C = 100^\circ\text{C}$ P_D	143	
Single Pulse Avalanche Energy (Note 3)	E_{AS}	1387	mJ
Single Pulse Avalanche Current (Note 3)	I_{AS}	30.4	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.35	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance (Note 4)	$R_{\theta JA}$	35	$^\circ\text{C/W}$

Notes:

1. Package current limit.
2. Pulse Width $\leq 100\mu\text{s}$.
3. $L = 3\text{mH}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
4. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 5)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	80	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.0	2.8	4.1	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 64V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 20A	R _{DS(on)}	--	1.4	1.8	mΩ
Dynamic (Note 6)						
Total Gate Charge	V _{DS} = 40V, I _D = 20A, V _{GS} = 10V	Q _g	--	179	--	nC
Gate-Source Charge		Q _{gs}	--	57	--	
Gate-Drain Charge		Q _{gd}	--	33	--	
Input Capacitance	V _{DS} = 40V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	12182	--	pF
Output Capacitance		C _{oss}	--	2269	--	
Reverse Transfer Capacitance		C _{rss}	--	45	--	
Gate Resistance	f = 1.0MHz	R _g	--	0.4	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V _{DD} = 40V, R _G = 3Ω, I _D = 20A, V _{GS} = 10V	t _{d(on)}	--	40	--	ns
Turn-On Rise Time		t _r	--	47	--	
Turn-Off Delay Time		t _{d(off)}	--	78	--	
Turn-Off Fall Time		t _f	--	34	--	
Source-Drain Diode						
Forward Voltage (Note 5)	I _S = 20A, V _{GS} = 0V	V _{SD}	--	--	1.2	V
Reverse Recovery Time	I _S = 20A	t _{rr}	--	103	--	ns
Reverse Recovery Charge	dI _F /dt = 100A/μs	Q _{rr}	--	324	--	nC

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

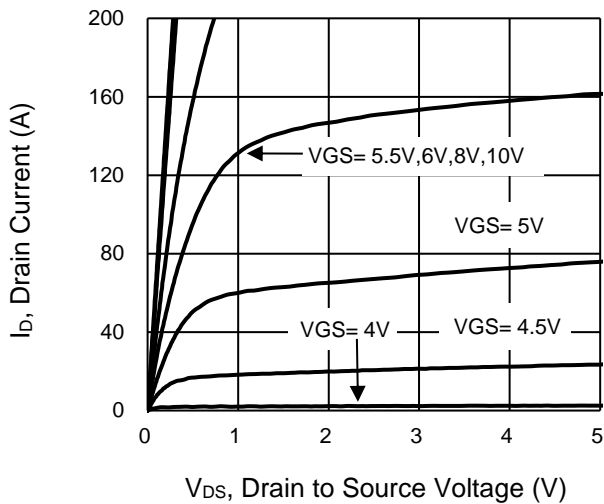
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM018NM08TL RAG	TOLL_A	2000pcs / 13" Reel

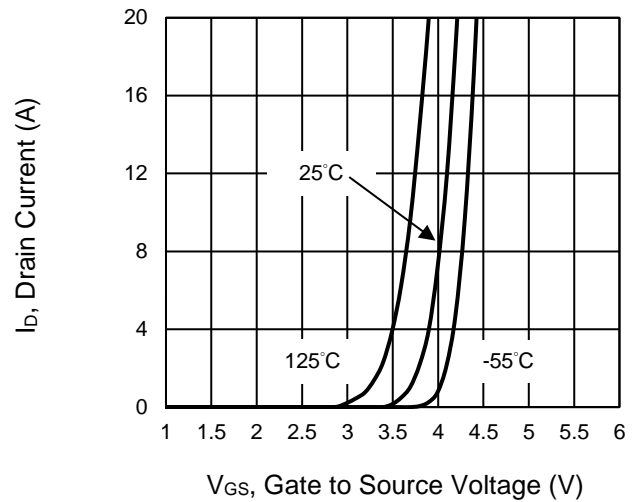
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

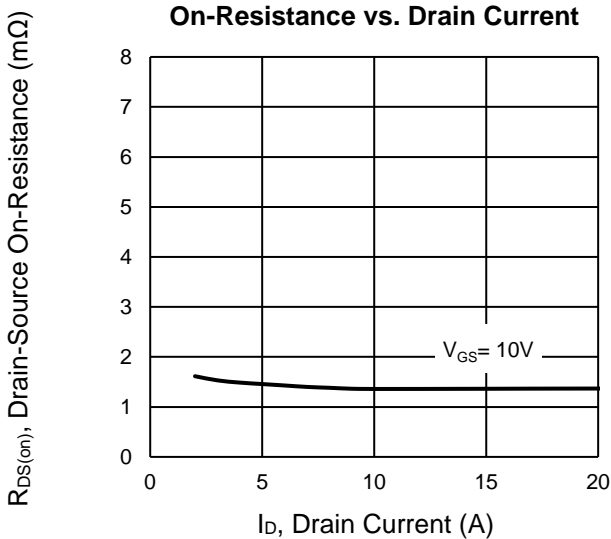
Output Characteristics



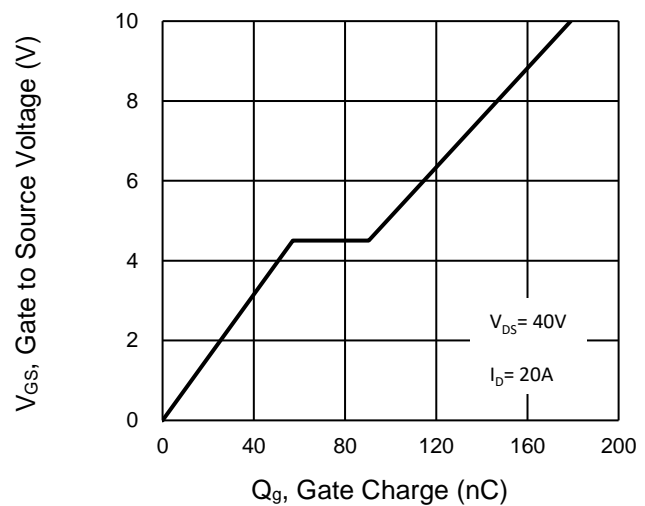
Transfer Characteristics



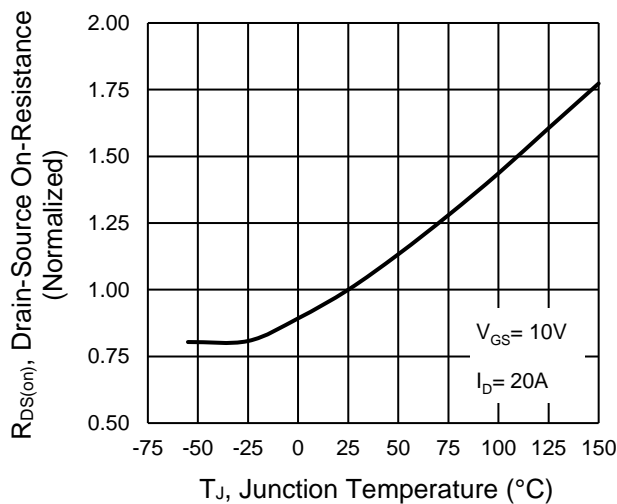
On-Resistance vs. Drain Current



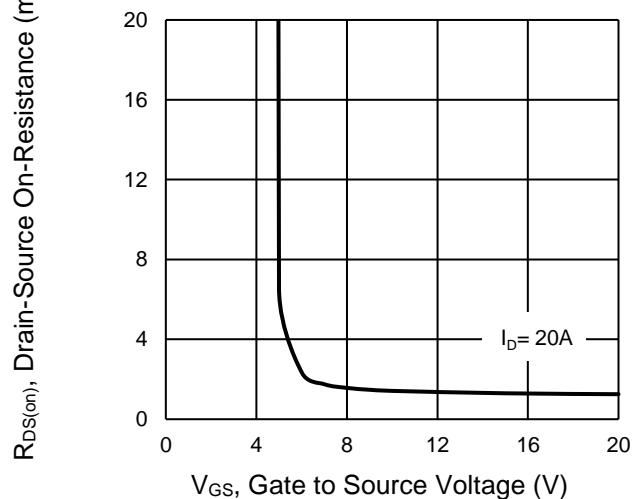
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

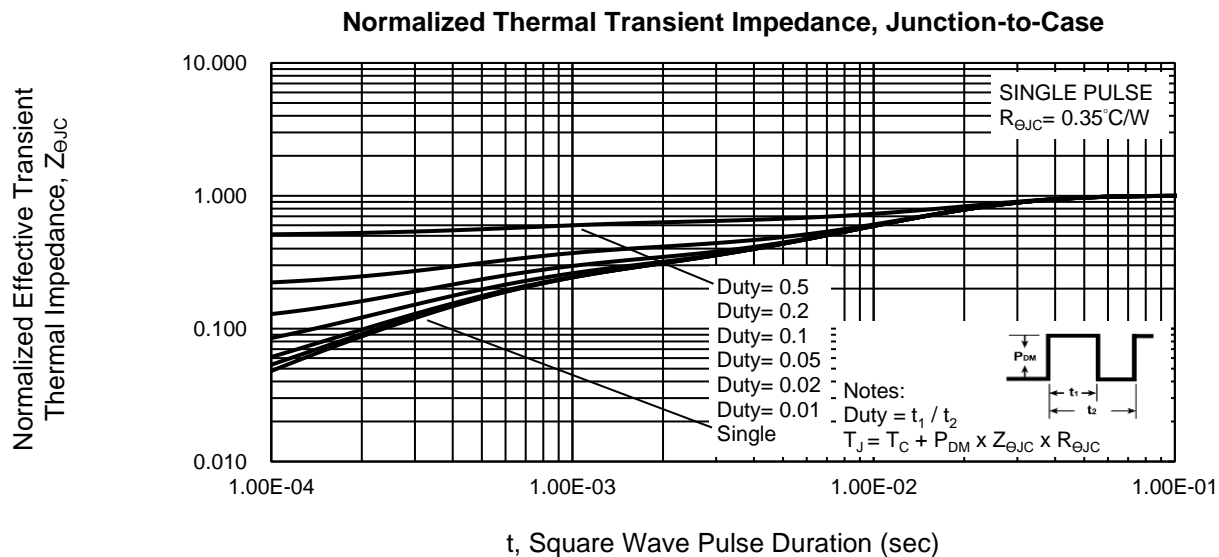
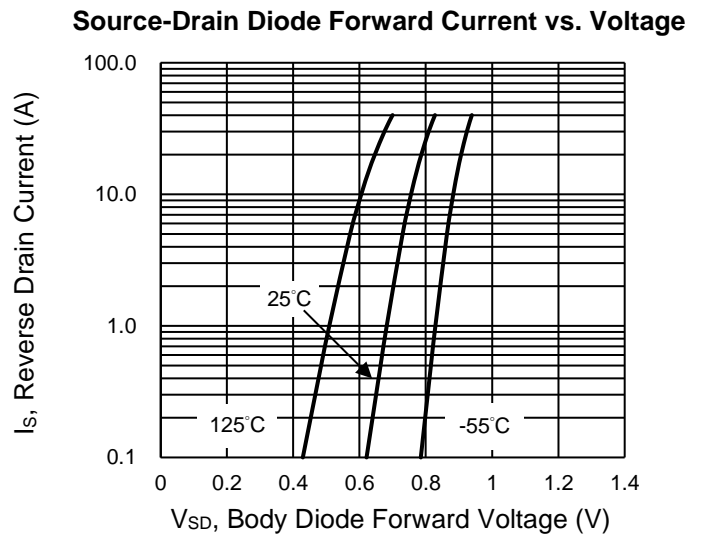
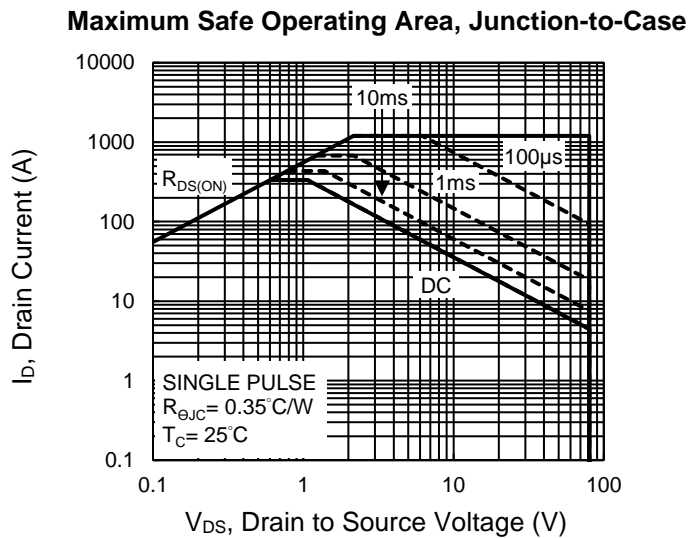
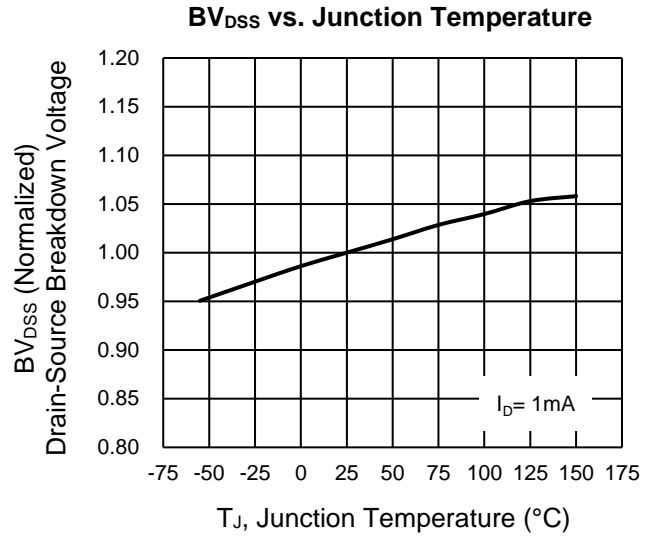
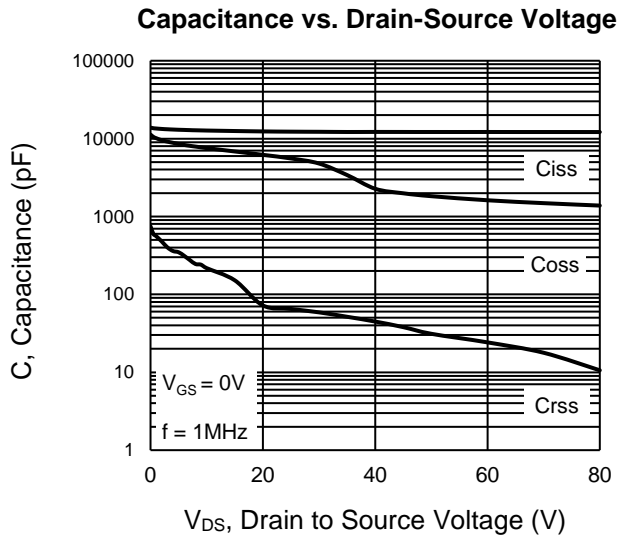


On-Resistance vs. Gate-Source Voltage



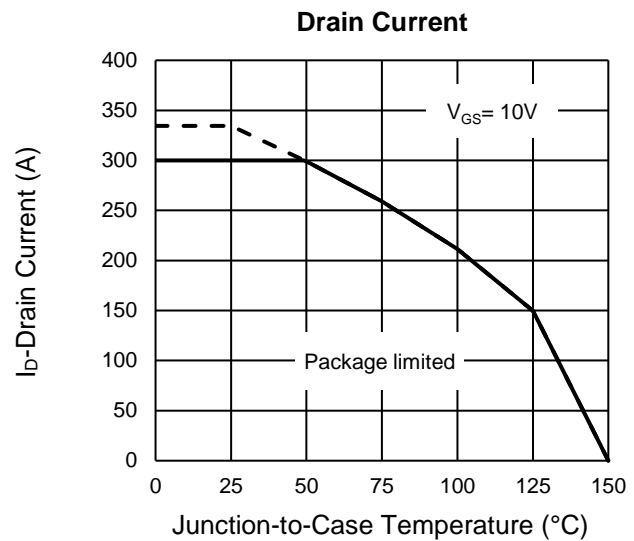
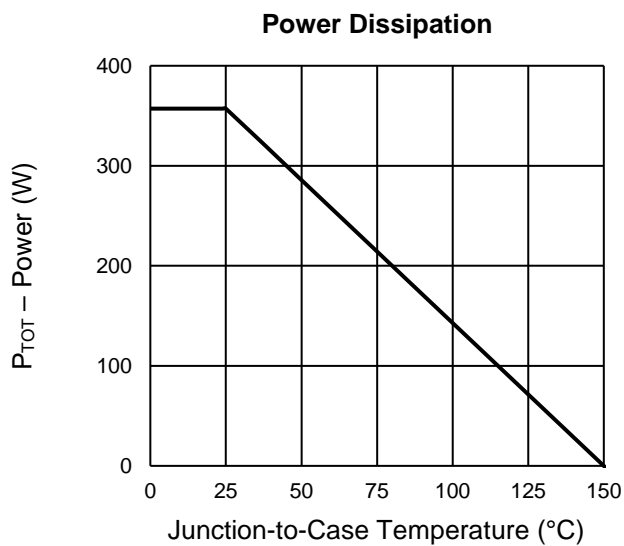
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

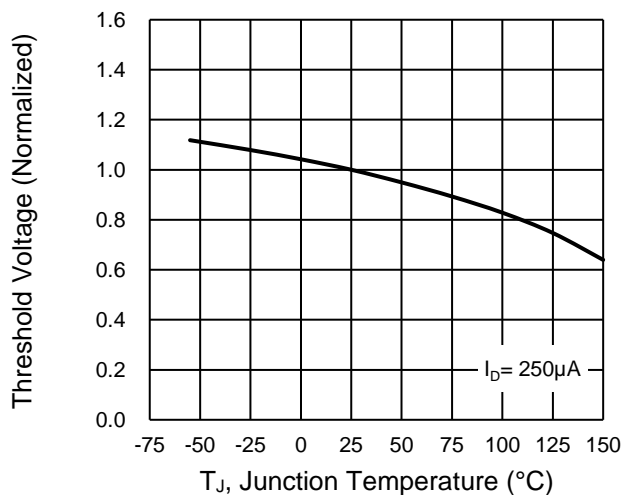


CHARACTERISTICS CURVES

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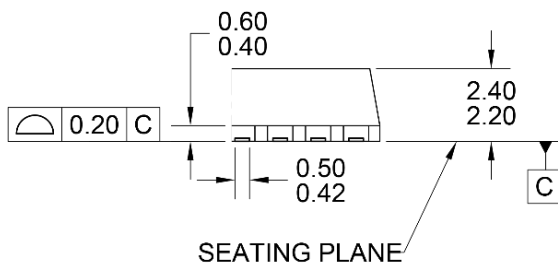
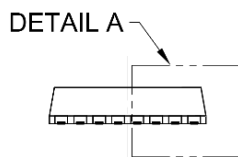
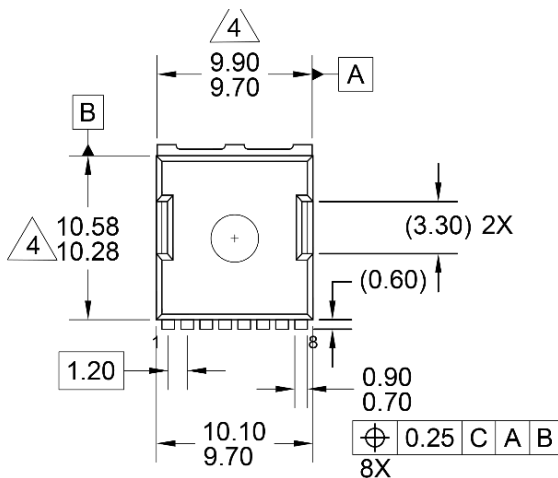


Normalized gate threshold voltage vs Temperature

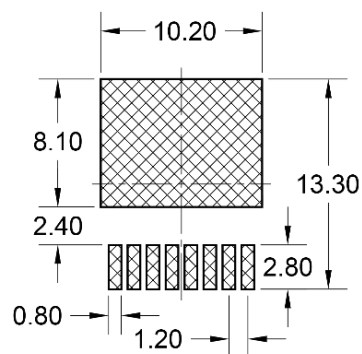
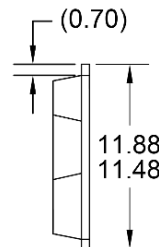
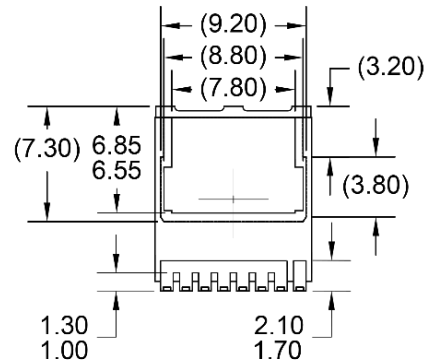


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

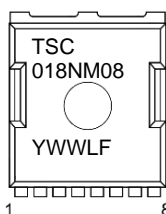
TOLL_A



DETAIL A
(SCALE 2:1)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM

018NM08 = Device marking
Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE PACKAGE OUTLINE REFERENCE: JEDEC MO-299B, ISSUE B.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DWG NO. REF: HQ2SD07-TOLL-141 REV A.

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