

MOSFET

650V CoolMOS™ CM8 Power Transistor

The CoolMOS™ 8th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 650V CoolMOS™ CM8 series is the successor to the 650V CoolMOS™ 7 Family and is enhancing Infineon's WBG offering. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g low ringing tendency, implemented fast body diode (CFD) for all products with outstanding robustness against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses of CM8, make switching applications even more efficient.

Features

- Best in class 650V SJ MOSFET performance
- Suitable for hard and soft switching topologies thanks to an outstanding commutation ruggedness
- Integrated fast body diode and ESD protection
- .XT interconnection technology for best in class thermal performance

Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to our advanced die attach technique
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due state of the art ESD protection
- Suitable for a wide variety of applications and power ranges

Potential applications

- Power supplies and converters
- PFC stages & LLC resonant converters
- High efficiency switching applications
- e.g. Datacenter, AI Server, Telecom Power Supply

Product validation

Fully qualified according to JEDEC for Industrial Applications

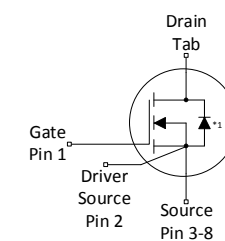
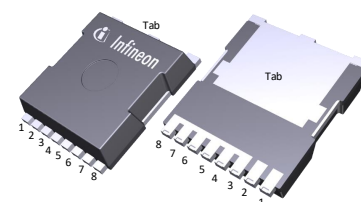
Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

| Parameter | Value | Unit |
|----------------------|-------|------|
| $V_{DS} @ T_{j,max}$ | 700 | V |
| $R_{DS(on),max}$ | 18 | mΩ |
| $Q_{g,typ}$ | 173 | nC |
| $I_{D,pulse}$ | 505 | A |
| $E_{oss} @ 400V$ | 19.6 | μJ |
| Body diode di_F/dt | 1300 | A/μs |
| ESD class (HBM) | 2 | |

| Type / Ordering code | Package | Marking | Related links |
|----------------------|-----------|----------|----------------|
| IPT65R018CM8 | PG-HSOF-8 | 65R018C8 | see Appendix A |

TOLL



*1: Internal body diode

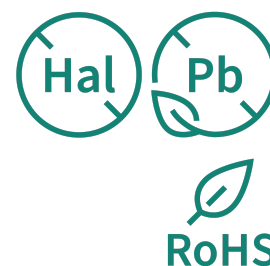




Table of contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Test circuits 11

Package outlines 12

Appendix A 15

Revision history 16

Trademarks 16

Disclaimer 16

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---------------|--------|------|-----------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 134 84 | A | $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 505 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 297 | mJ | $I_D=6.7\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche energy, repetitive | E_{AR} | - | - | 1.48 | mJ | |
| Avalanche current, single pulse | I_{AS} | - | - | 6.7 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 120 | V/ns | $V_{DS}=0\ldots 400\text{V}$ |
| Gate source voltage (static) | V_{GS} | -20 | - | 20 | V | static; |
| Gate source voltage (dynamic) | V_{GS} | -30 | - | 30 | V | AC ($f>1\text{ Hz}$) |
| Power dissipation | P_{tot} | - | - | 694 | W | $T_C=25^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | - |
| Operating junction temperature | T_j | -55 | - | 150 | $^\circ\text{C}$ | |
| Extended operating junction temperature | T_j | 150 | - | 175 | $^\circ\text{C}$ | $\leq 50\text{ h}$ in the application lifetime |
| Mounting torque | - | - | - | - | Ncm | - |
| Continuous diode forward current | I_S | - | - | 134 | A | $T_C=25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 505 | A | |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 70 | V/ns | $V_{DS}=0\ldots 400\text{V}$, $I_{SD}\leq 134\text{A}$, $T_j=25^\circ\text{C}$ see table 8 |
| Maximum diode commutation speed | di_F/dt | - | - | 1300 | A/ μs | |
| Insulation withstand voltage | V_{ISO} | - | - | n.a. | V | V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$ |

1) Limited by $T_{j,max}$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 0.18 | K/W | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | K/W | device on PCB, minimal footprint |
| Thermal resistance, junction - ambient for SMD version | R_{thJA} | - | 35 | 45 | K/W | Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70μm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling. |
| Soldering temperature, wave- & reflow soldering allowed | T_{sold} | - | - | 260 | °C | reflow MSL1 |

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|----------------------------------|---------------|--------|----------------|------------|----------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 650 | - | - | V | $V_{GS}=0V$, $I_D=1mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 3.7 | 4.2 | 4.7 | V | $V_{DS}=V_{GS}$, $I_D=1.48mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - 244 | 2 - | μA | $V_{DS}=650V$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650V$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$ |
| Gate-source leakage current | I_{GSS} | - | - | 0.1 | μA | $V_{GS}=20V$, $V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.015 0.033 | 0.018 - | Ω | $V_{GS}=10V$, $I_D=55.6A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=55.6A$, $T_j=150^\circ\text{C}$ |
| Gate resistance | R_G | - | 1 | - | Ω | $f=1MHz$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 8290 | - | pF | $V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$ |
| Output capacitance | C_{oss} | - | 91 | - | pF | |
| Effective output capacitance, energy related ⁴⁾ | $C_{o(er)}$ | - | 245 | - | pF | $V_{GS}=0V$, $V_{DS}=0...400V$ |
| Effective output capacitance, time related ⁵⁾ | $C_{o(tr)}$ | - | 2702 | - | pF | $I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 33.5 | - | ns | $V_{DD}=400V$, $V_{GS}=13V$, $I_D=29.7A$, $R_G=1.8\Omega$; see table 9 |
| Rise time | t_r | - | 10.5 | - | ns | |
| Turn-off delay time | $t_{d(off)}$ | - | 145 | - | ns | |
| Fall time | t_f | - | 5.1 | - | ns | |

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|-----------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 48 | - | nC | $V_{DD}=400V$, $I_D=29.7A$, $V_{GS}=0$ to $10V$ |
| Gate to drain charge | Q_{gd} | - | 54 | - | nC | |
| Gate charge total | Q_g | - | 173 | - | nC | |
| Gate plateau voltage | $V_{plateau}$ | - | 5.8 | - | V | |

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|-------------------------------|-----------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0V$, $I_F=29.7A$, $T_j=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 180 | 225 | ns | $V_R=400V$, $I_F=29.7A$, $di_F/dt=100A/\mu s$; see table 8 |
| Reverse recovery charge | Q_{rr} | - | 1.54 | 2.31 | μC | |
| Peak reverse recovery current | I_{rrm} | - | 16.4 | - | A | |

4 Electrical characteristics diagrams

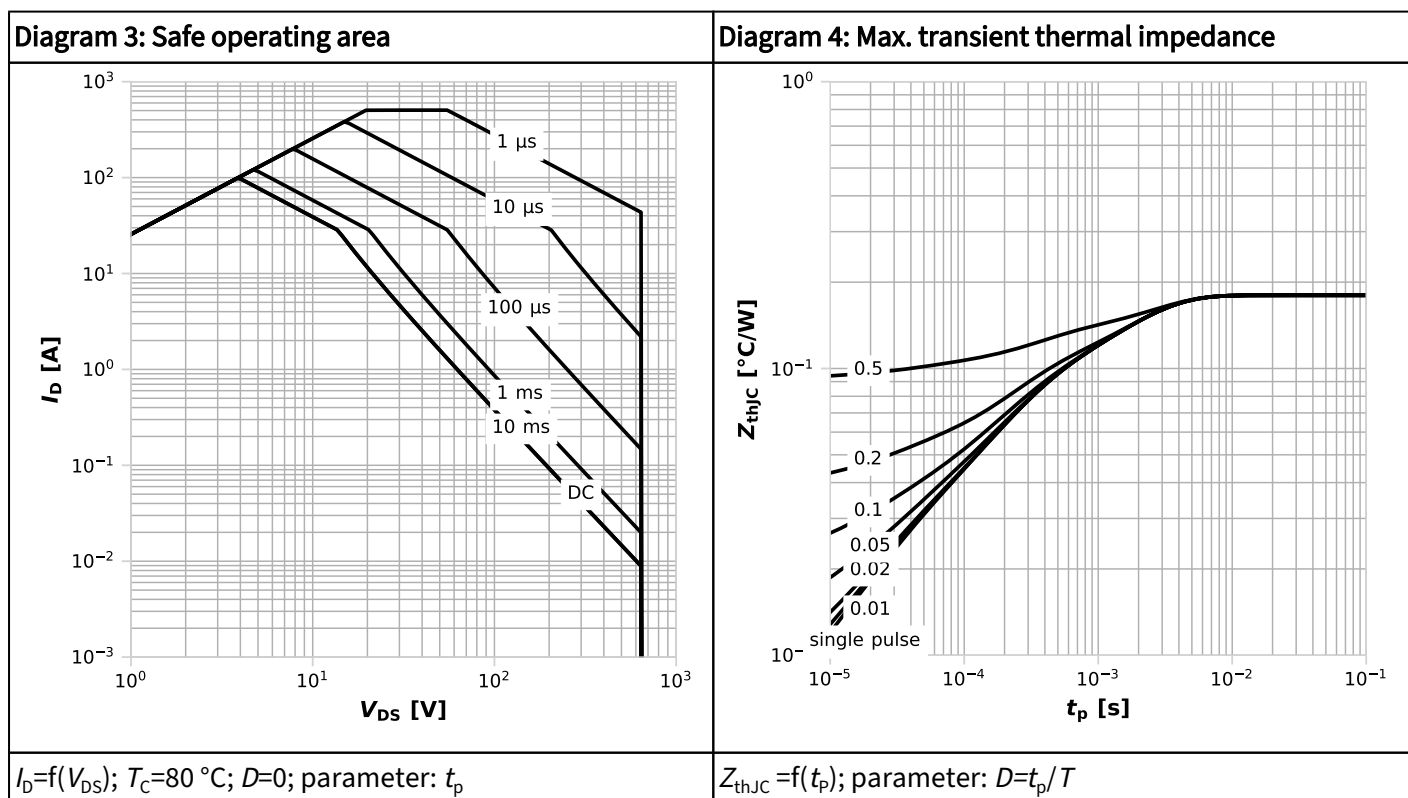
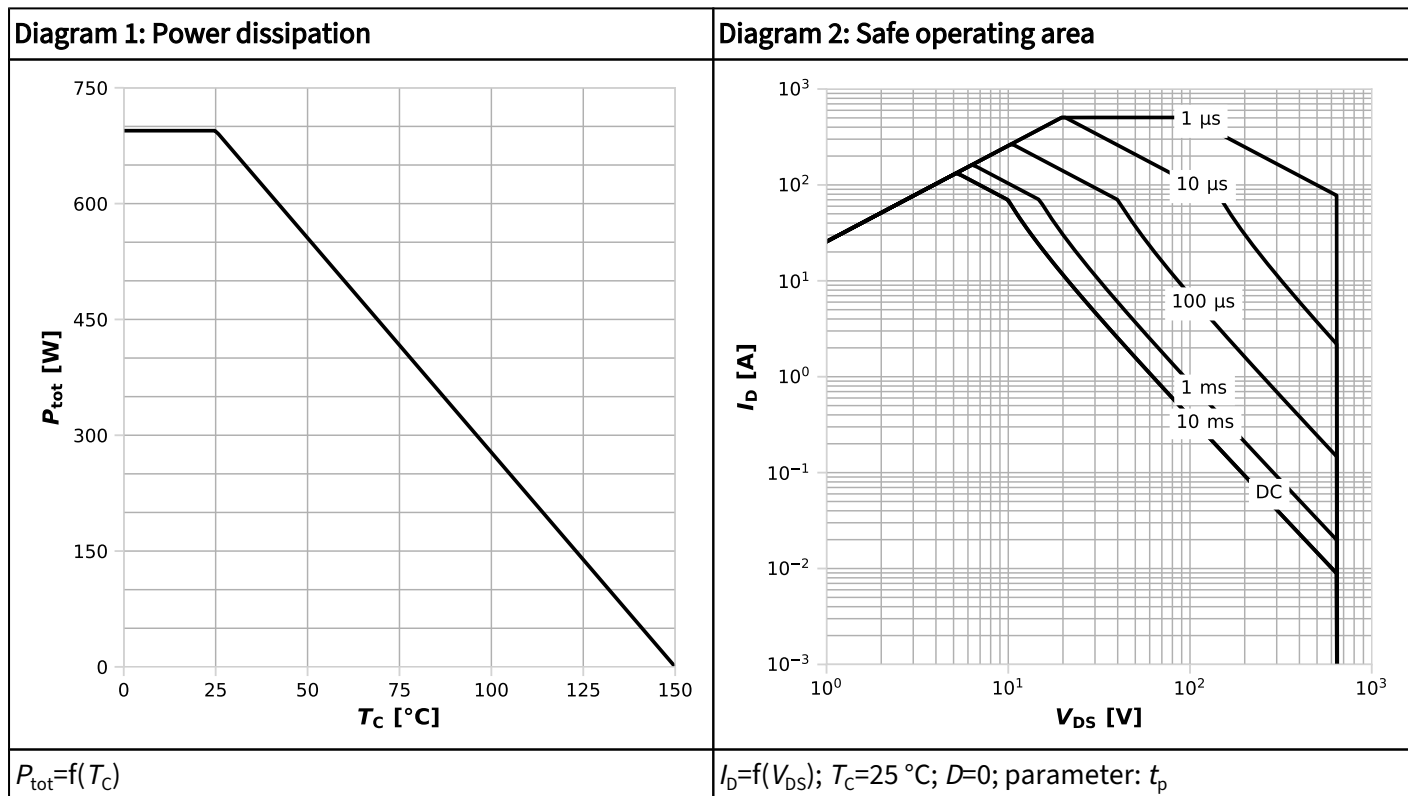
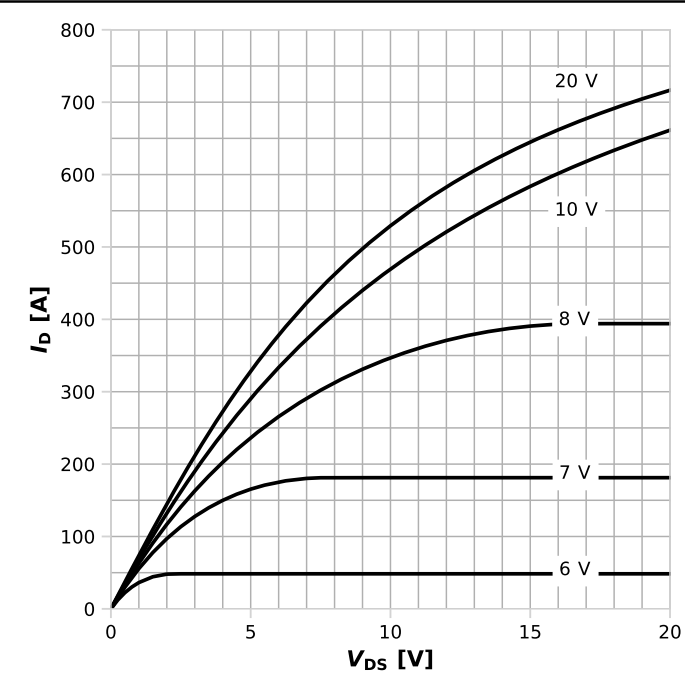
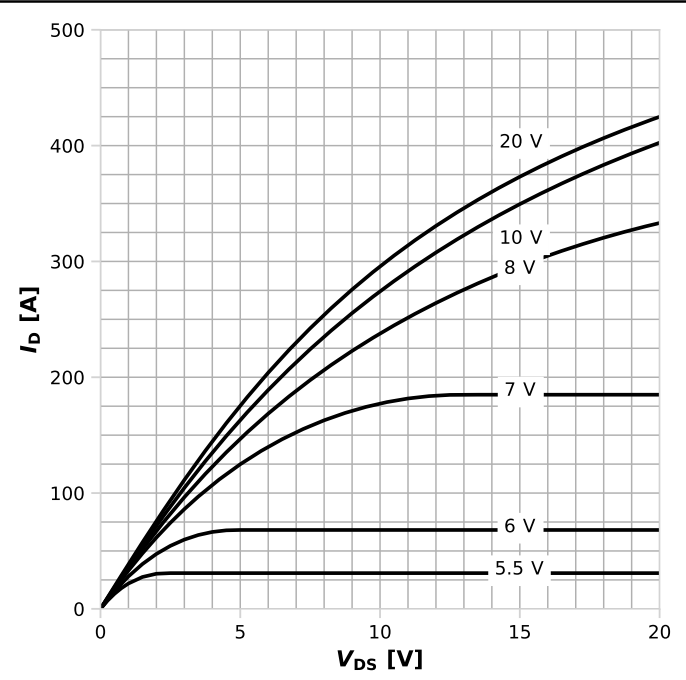


Diagram 5: Typ. output characteristics



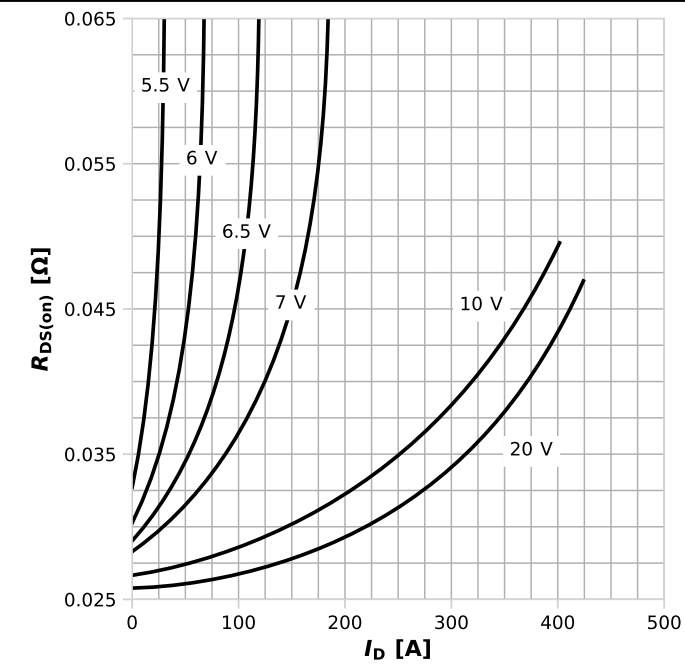
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



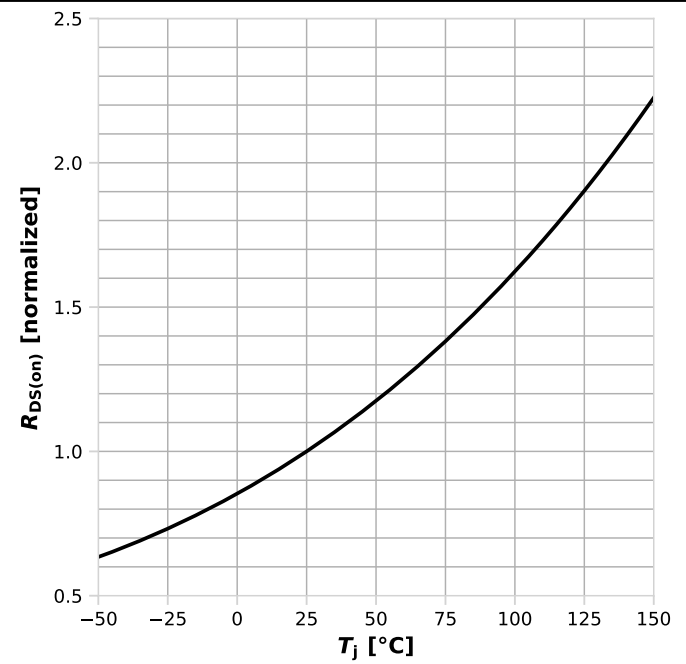
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



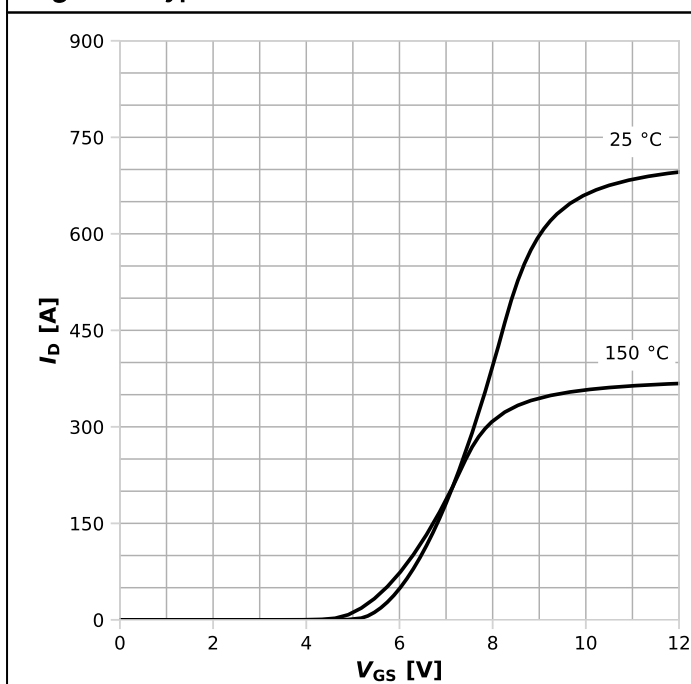
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



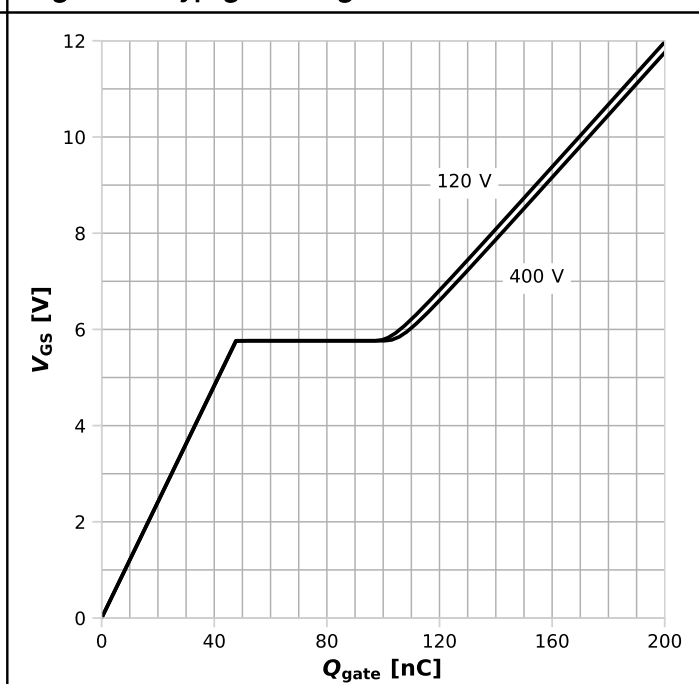
$R_{DS(on)} = f(T_j)$; $I_D = 55.6\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



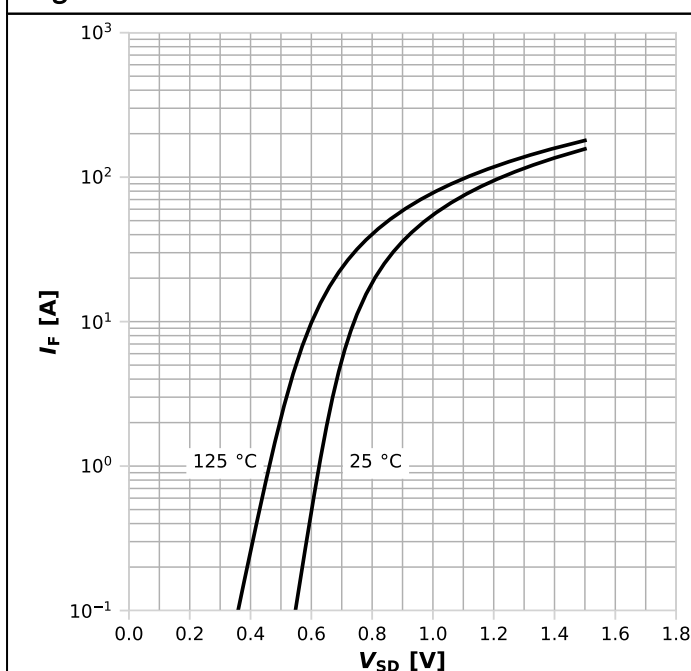
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



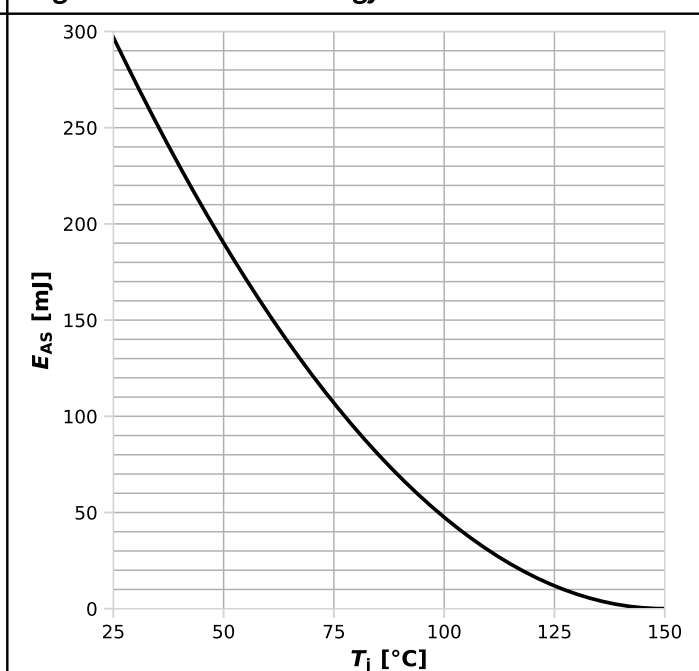
$V_{GS} = f(Q_{gate})$; $I_D = 29.7$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



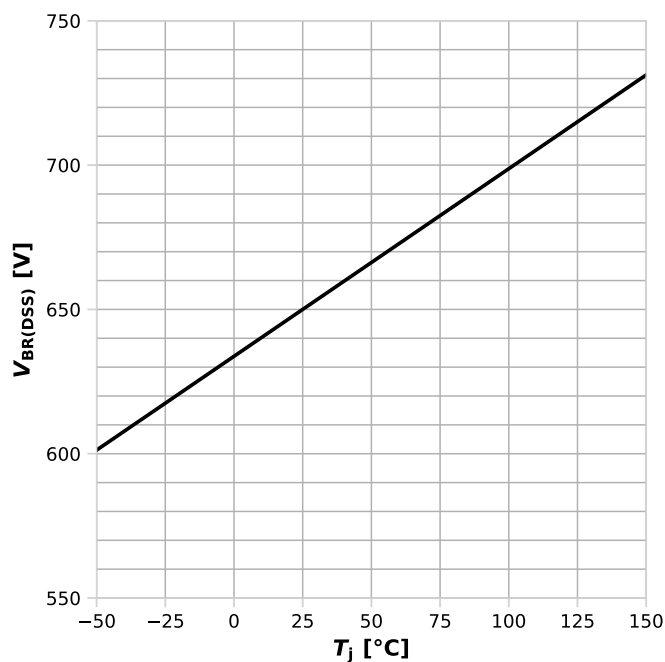
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



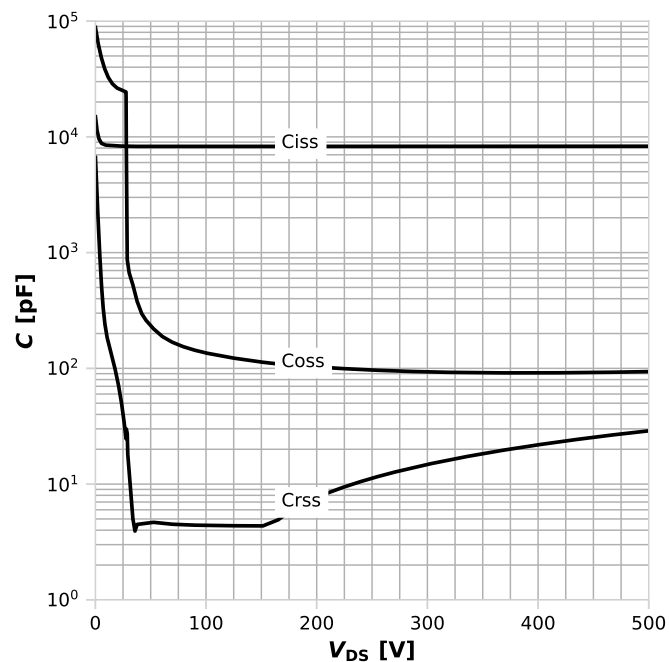
$E_{AS} = f(T_j)$; $I_D = 6.7$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



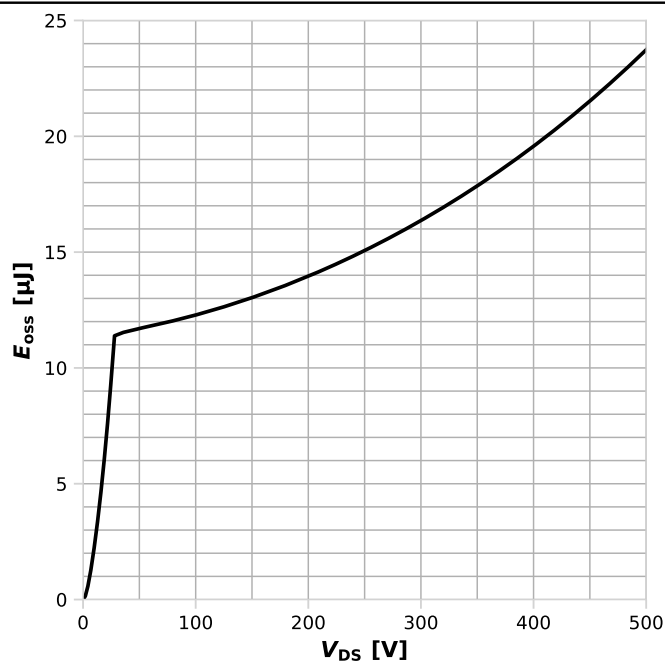
$$V_{BR(DSS)} = f(T_j); I_D = 10 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

5 Test circuits

Table 8 Diode characteristics

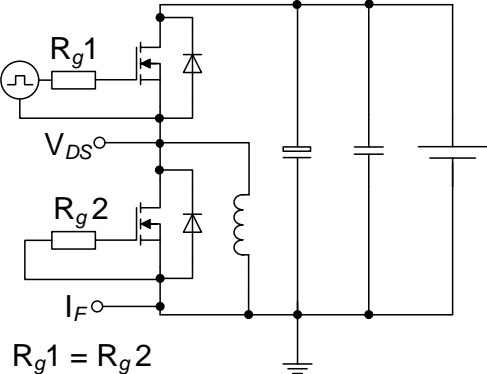
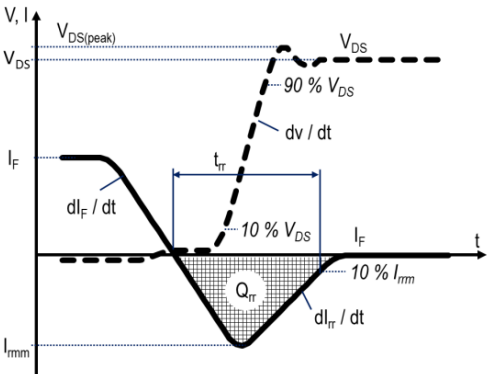
| Test circuit for diode characteristics | Diode recovery waveform |
|---|--|
|  <p>$R_{g1} = R_{g2}$</p> |  |

Table 9 Switching times (ss)

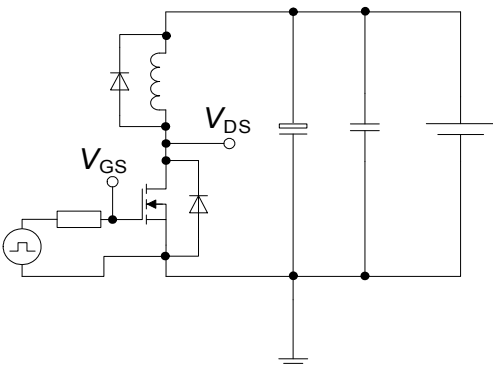
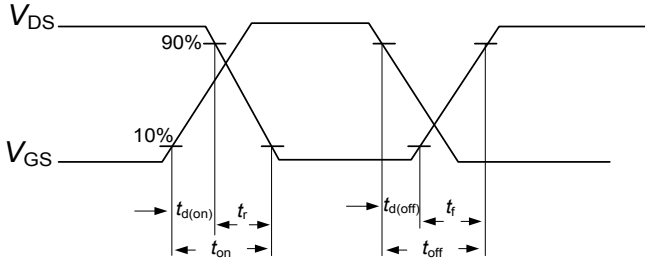
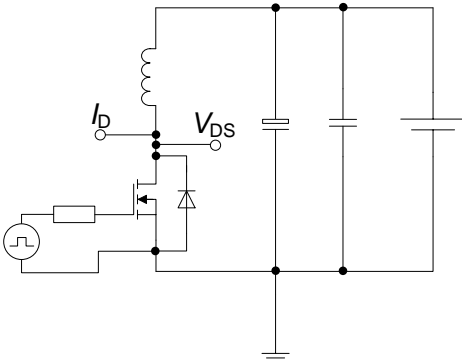
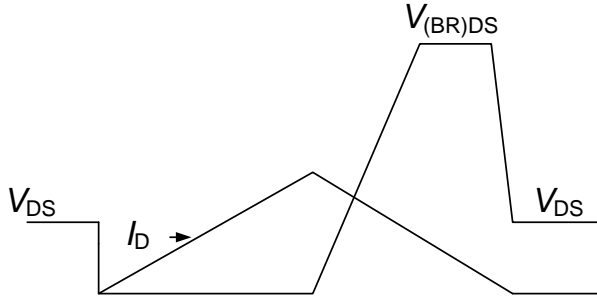
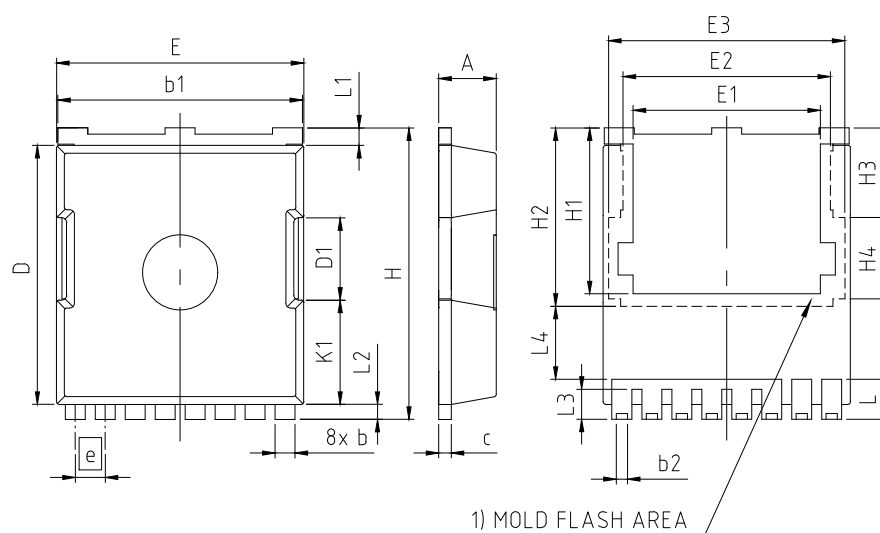
| Switching times test circuit for inductive load | Switching times waveform |
|---|--|
|  |  |

Table 10 Unclamped inductive load (ss)

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|--|
|  |  |

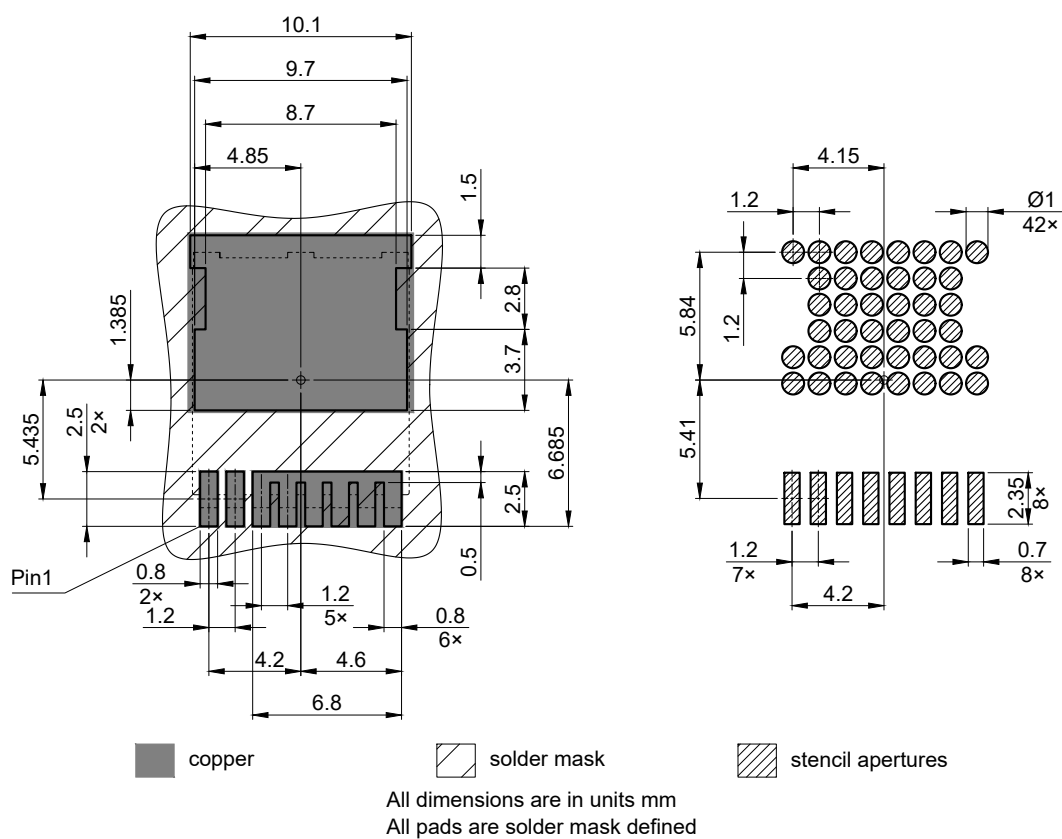
6 Package outlines

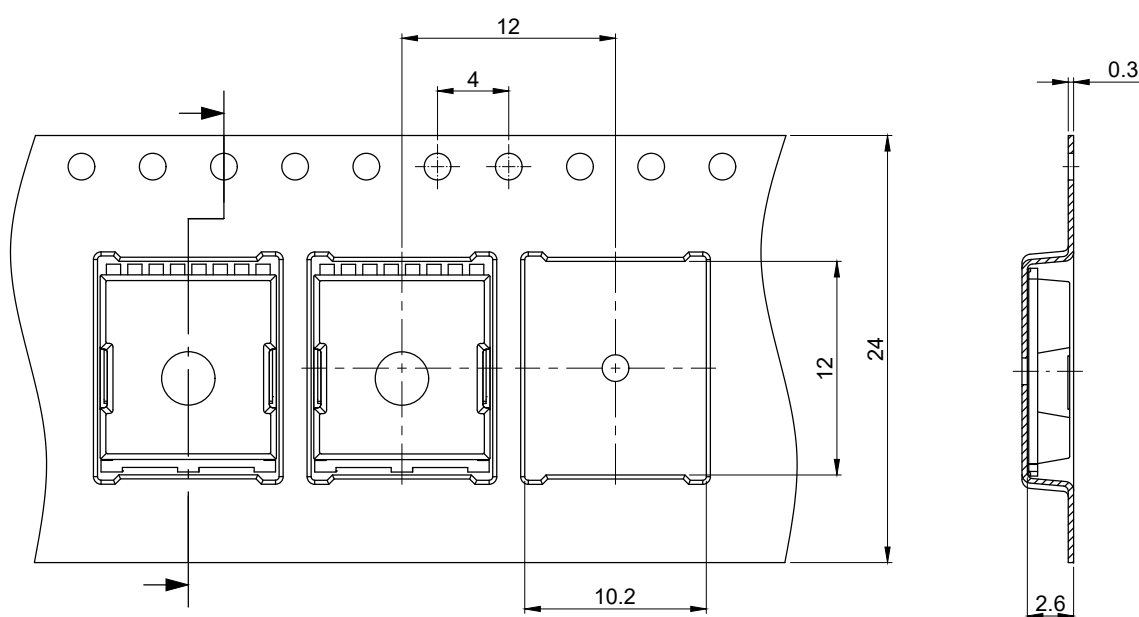


| PACKAGE - GROUP NUMBER: PG-HSOF-8-U02 | | |
|--|-------------|-------|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.20 | 2.40 |
| b | 0.70 | 0.90 |
| b1 | 9.70 | 9.90 |
| b2 | 0.42 | 0.50 |
| c | 0.40 | 0.60 |
| D | 10.28 | 10.58 |
| D1 | 3.30 | |
| E | 9.70 | 10.10 |
| E1 | 7.50 | |
| E2 | 8.50 | |
| E3 | 9.46 | |
| e | 1.20 (BSC) | |
| H | 11.48 | 11.88 |
| H1 | 6.55 | 6.95 |
| H2 | 7.15 | |
| H3 | 3.59 | |
| H4 | 3.26 | |
| N | 8 | |
| K1 | 4.18 | |
| L | 1.40 | 1.80 |
| L1 | 0.50 | 0.90 |
| L2 | 0.50 | 0.70 |
| L3 | 1.00 | 1.30 |
| L4 | 2.62 | 2.81 |

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm


The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 **Related links**

- [IFX CoolMOS CM8 Webpage](#)
- [IFX CoolMOS CM8 application note](#)
- [IFX CoolMOS CM8 simulation model](#)
- [IFX Design tools](#)

Revision history

IPT65R018CM8

Revision 2024-12-19, Rev. 2.0

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2024-12-19 | Release of final version |

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