

MOSFET – N-Channel, POWERTRENCH®

80 V, 8.9 A, 16 mΩ

FDS3572

Features

- $R_{DS(ON)} = 14 \Omega$ (Typ.), $V_{GS} = 10 \text{ V}$, $I_D = 8.9 \text{ A}$
- $Q_{g(tot)} = 31 \text{ nC}$ (Typ.), $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- This Device is Pb-Free and Halide Free

Applications

- Primary Switch for Isolated DC-DC Converters
- Distributed Power and Intermediate Bus Architectures
- High Voltage Synchronous Rectifier for DC Bus Converters

ABSOLUTE MAXIMUM RATINGS

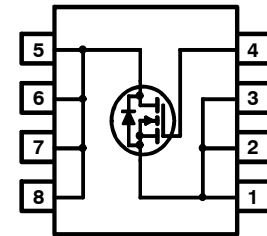
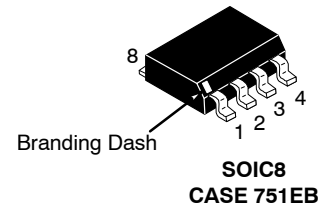
($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($T_A = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 50^\circ\text{C/W}$) ($T_A = 100^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 50^\circ\text{C/W}$) Pulsed Fig. 4	8.9 5.6	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	515	mJ
P_D	Power Dissipation	2.5	W
	Derate above 25°C	20	mW/ $^\circ\text{C}$
T_J , T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$

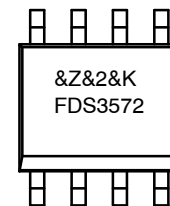
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient at 10 seconds (Note 3)	50	$^\circ\text{C/W}$
	Thermal Resistance, Junction-to-Ambient at 1000 seconds (Note 3)	85	$^\circ\text{C/W}$



MARKING DIAGRAM



&Z = Assembly Plant Code
 &2 = Date Code (Year & Week)
 &K = Lot Traceability Code
 FDS3572 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDS3572	SOIC8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDS3572

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 60 V, V _{GS} = 0 V V _{DS} = 60 V, V _{GS} = 0 V, T _A = 150 °C	– –	– –	1 250	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS (Note 3)

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	–	4	V
R _{DS(on)}	Drain to Source On-Resistance	I _D = 8.9 A, V _{GS} = 10 V I _D = 5.6 A, V _{GS} = 6 V I _D = 8.9 A, V _{GS} = 10 V, T _A = 150°C	– – –	0.014 0.019 0.027	0.016 0.029 0.032	Ω

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	1990	–	pF
C _{oss}	Output Capacitance		–	320	–	pF
C _{rss}	Reverse Transfer Capacitance		–	85	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 40 V, I _D = 8.9 A, I _g = 1.0 mA	–	31	41	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V, V _{DD} = 40 V, I _D = 8.9 A, I _g = 1.0 mA	–	4	5.2	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 40 V, I _D = 8.9 A, I _g = 1.0 mA	–	9	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	5	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	7.5	–	nC

SWITCHING CHARACTERISTICS (V_{GS} = 10 V)

t _{ON}	Turn On Time	V _{DD} = 40 V, I _D = 8.9 A, V _{GS} = 10 V, R _{GS} = 10 Ω	–	–	40	ns
t _{d(on)}	Turn-On Delay Time		–	13	–	ns
t _r	Rise Time		–	14	–	ns
t _{d(off)}	Turn-Off Delay Time		–	31	–	ns
t _f	Fall Time		–	13	–	ns
t _{OFF}	Total Off Time		–	–	67	ns

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 8.9 A I _{SD} = 4.3 A	– –	– –	1.25 1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 8.9 A, dI _{SD} /dt = 100 A/μs	–	–	50	ns
Q _{rr}	Reverse Recovery Charge	I _{SD} = 8.9 A, dI _{SD} /dt = 100 A/μs	–	–	70	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- Starting T_J = 25°C, L = 21mH, I_{AS} = 7 A.
- R_{θJA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.
- R_{θJA} is measured with 1.0 in² copper on FR-4 board.

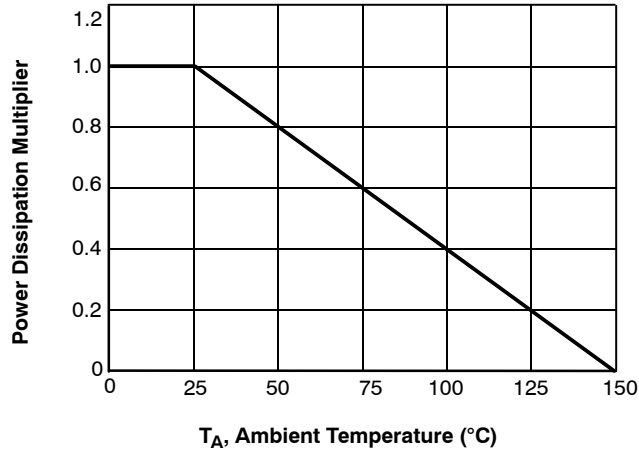
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Figure 1. Normalized Power Dissipation vs. Ambient Temperature

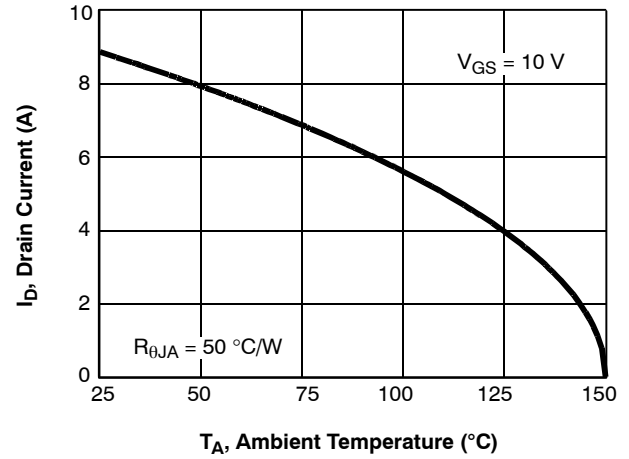


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

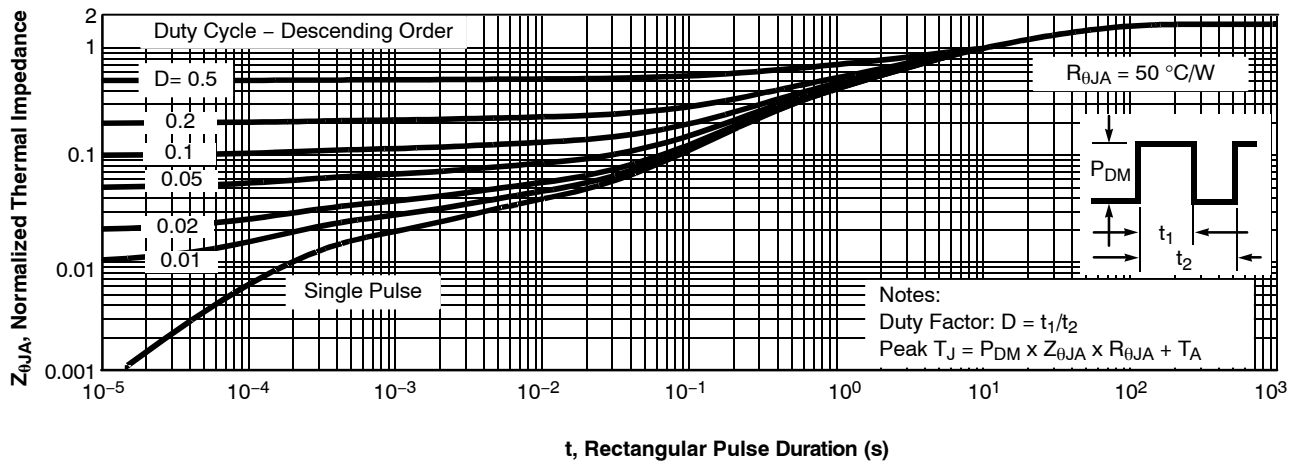


Figure 3. Normalized Maximum Transient Thermal Impedance

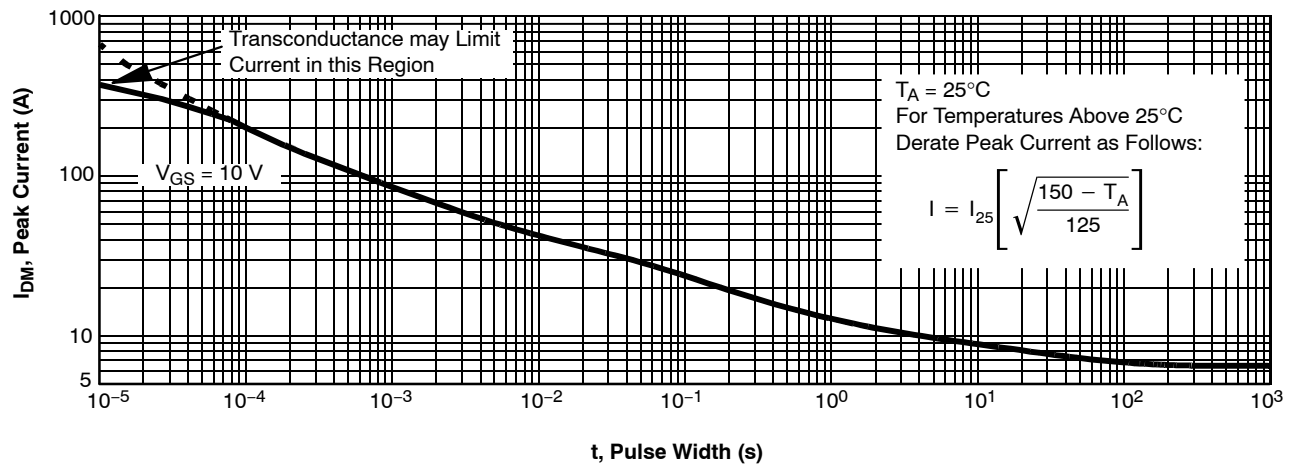
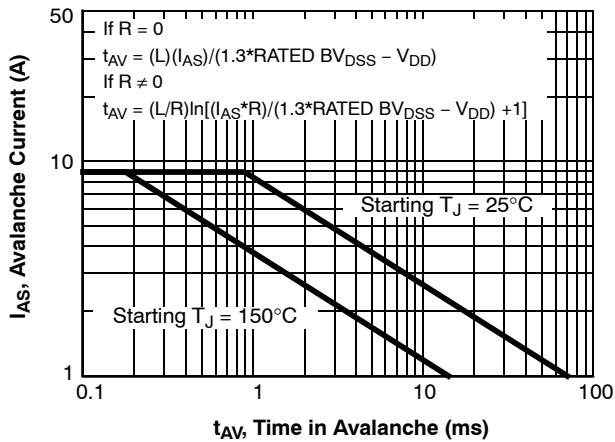


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

NOTES: Refer to Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching Capability

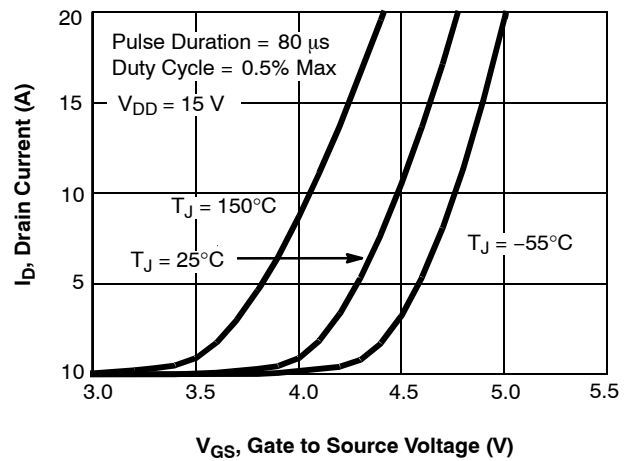


Figure 6. Transfer Characteristics

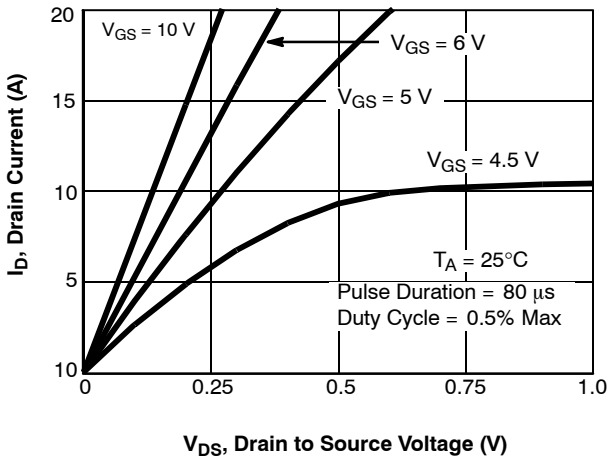


Figure 7. Saturation Characteristics

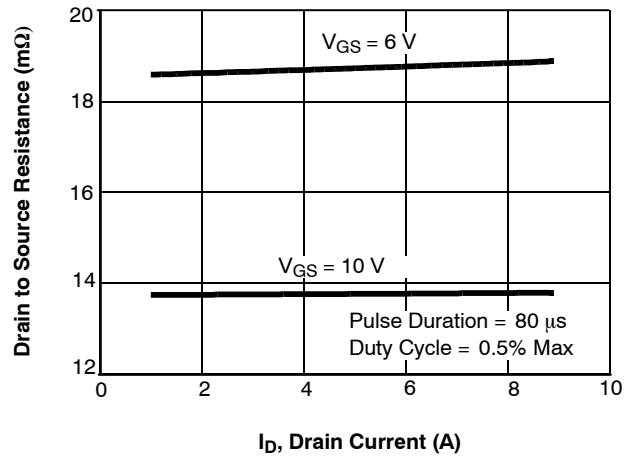


Figure 8. Drain to Source On Resistance vs Drain Current

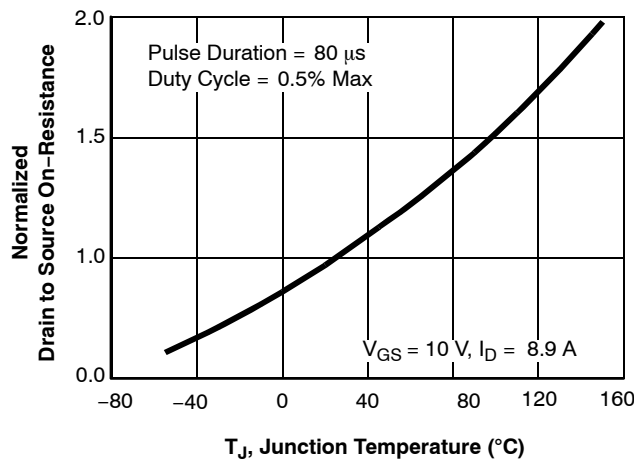


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

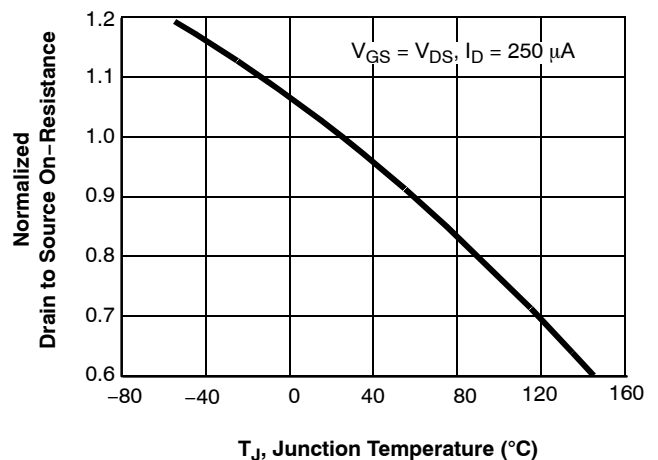


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

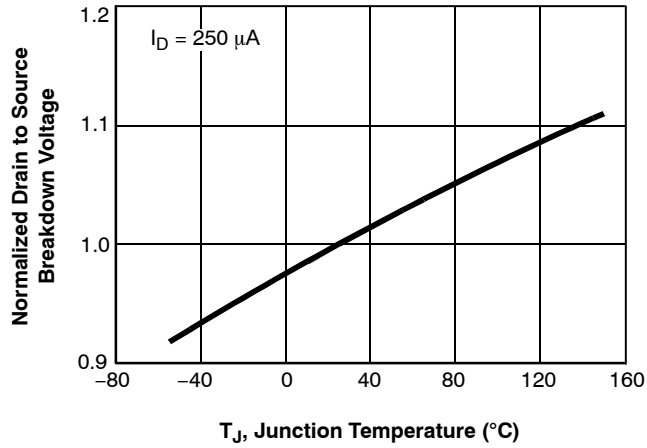


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

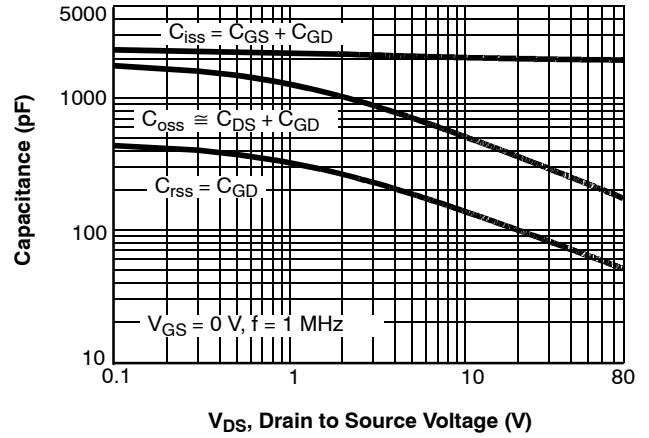


Figure 12. Capacitance vs Drain to Source Voltage

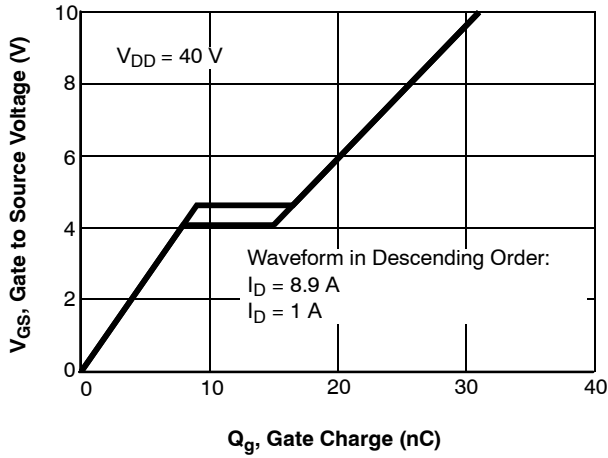


Figure 13. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

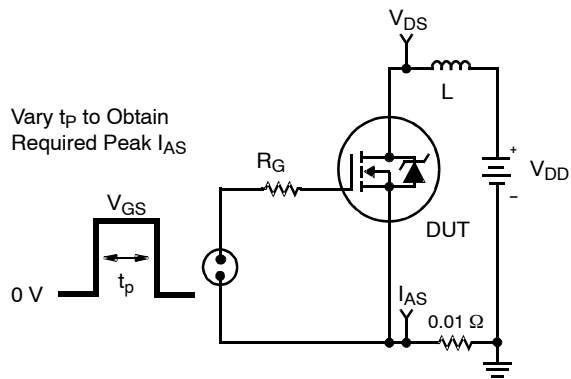


Figure 14. Unclamped Energy Test Circuit

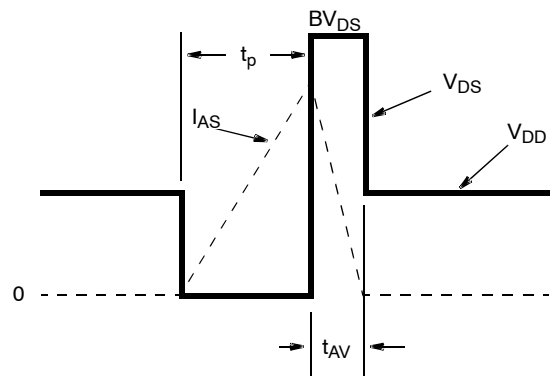


Figure 15. Unclamped Energy Waveforms

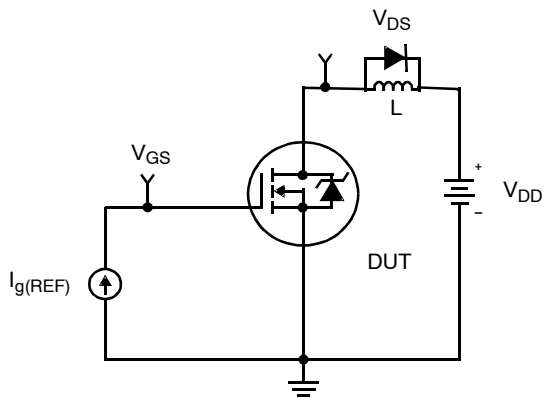


Figure 16. Gate Charge Test Circuit

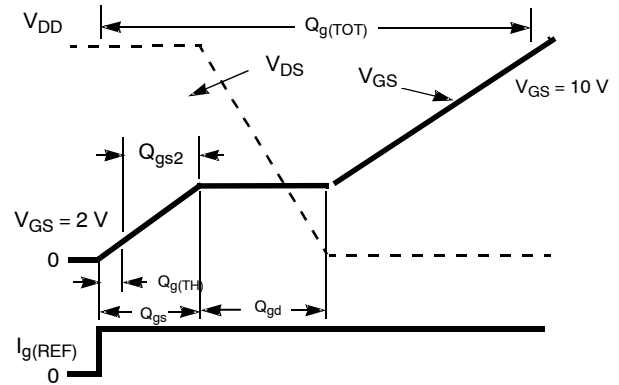


Figure 17. Gate Charge Waveforms

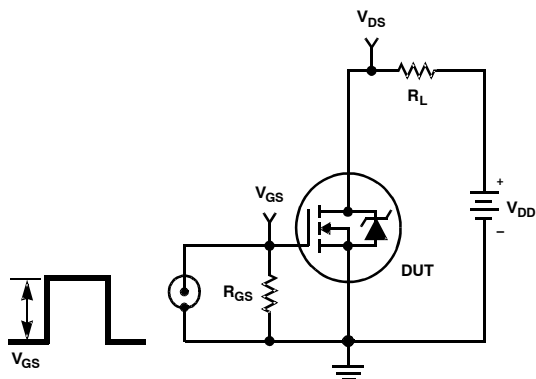


Figure 18. Switching Time Test Circuit

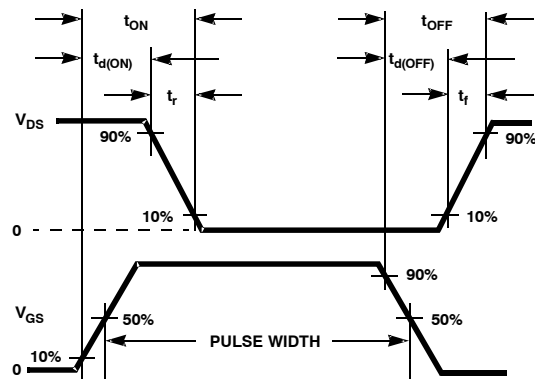


Figure 19. Switching Time Waveforms

THERMAL RESISTANCE VS. MOUNTING PAD AREA

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C}/\text{W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{eq. 2})$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

onsemi provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1 oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the **onsemi** device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 20 or by calculation using Equation 3. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{(0.23 + \text{Area})} \quad (\text{eq. 3})$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 21 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100 ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, C THERM1 through C THERM5 and R THERM1 through R THERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

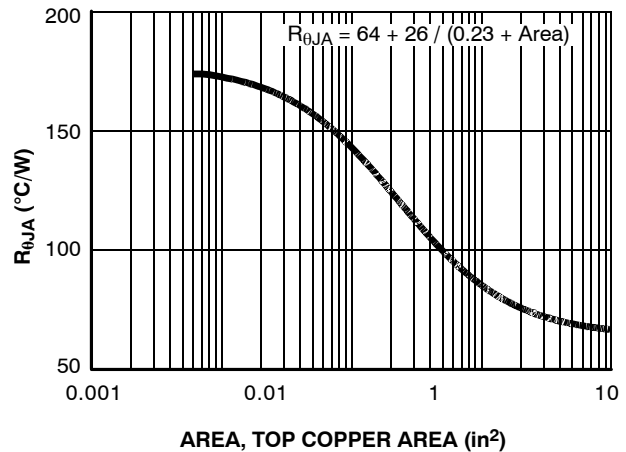


Figure 20. Thermal Resistance vs. Mounting Pad Area

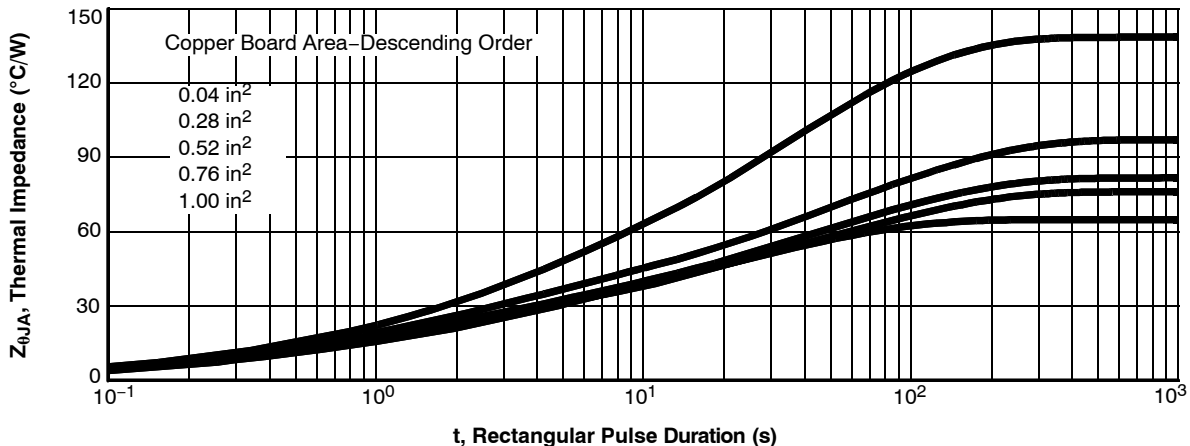


Figure 21. Thermal Impedance vs Mounting Pad Area

PSPICE ELECTRICAL MODEL

.SUBCKT FDS3572 2 1 3 ; rev November 2003
Ca 12 8 7e-10
Cb 15 14 7e-10
Cin 6 8 1.9e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 86.6
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 1e-9
Ldrain 2 5 1e-9
Lsource 3 7 0.1e-9

```
RLgate 1 9 10
RLdrain 2 5 10
RLsource 3 7 1
```

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
MweakMOD 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 5.5e-3
Rgate 9 20 1.3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 5.5e-3
Rvthres 22 8 Rvthresmod 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={V(5,51)/ABS(V(5,51))}*(PWR(V(5,51)/(1e-6*250),2.5))}

```
.MODEL DbodyMOD D (IS=4.5E-12 RS=4.7e-3 TRS1=1.5e-3 TRS2=2e-5 XTI=3 CJO=1.4e-9 TT=3e-08 M=0.55)
.MODEL DbreakMOD D (RS=2.5 TRS1=1e-4 TRS2=1e-6)
.MODEL DplcapMOD D (CJO=4.6e-10 IS=1e-30 N=10 M=0.5)
```

```
.MODEL MmedMOD NMOS (VTO=3.35 KP=3 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.3 T_ABS=25)
.MODEL MstroMOD NMOS (VTO=3.9 KP=60 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)
.MODEL MweakMOD NMOS (VTO=2.88 kp=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=13 RS=0.1 T_ABS=25)
```

```
.MODEL RbreakMOD RES (TC1=1e-3 TC2=-7.5e-7)
.MODEL RdrainMOD RES (TC1=4.8e-3 TC2=3e-5)
.MODEL RSLCMOD RES (TC1=2.4e-2 TC2=1e-7)
.MODEL RSourceMOD RES (TC1=1e-2 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-4.4e-3 TC2=-1.4e-5)
.MODEL RvtempMOD RES (TC1=-4e-3 TC2=2e-7)
```

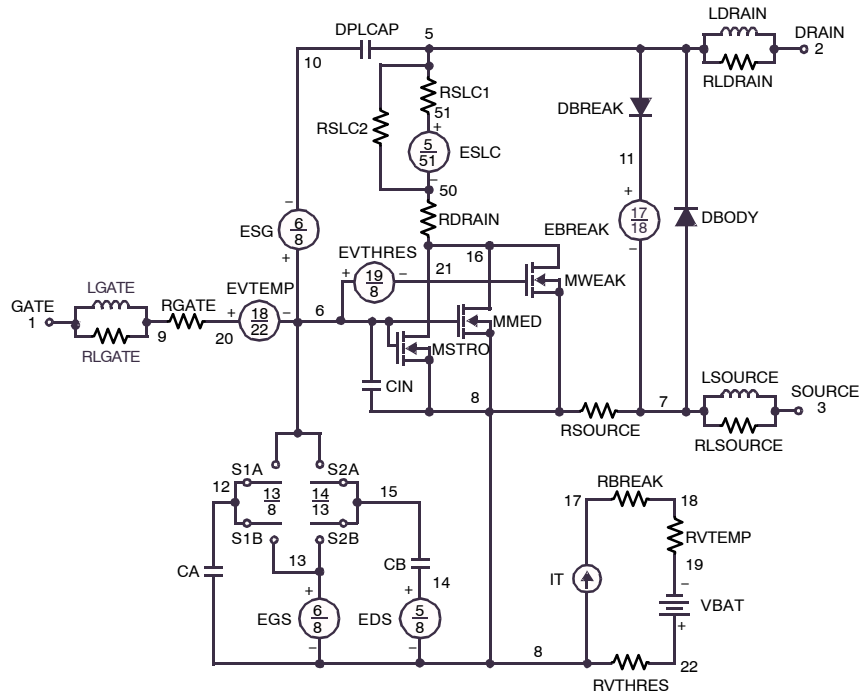


Figure 22.

FDS3572

```
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=-2.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-4.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0 VOFF=-0.5)
```

.ENDS

For further discussion of the PSPICE model, consult *A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options*; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SPICE THERMAL MODEL

REV November 2003
FDS3572

Copper Area = 1.0 in²
CTHERM1 TH 8 2.0e-3
CTHERM2 8 7 5.0e-3
CTHERM3 7 6 1.0e-2
CTHERM4 6 5 4.0e-2
CTHERM5 5 4 9.0e-2
CTHERM6 4 3 2e-1
CTHERM7 3 2 1
CTHERM8 2 TL 3

R THERM1 TH 8 1e-1
R THERM2 8 7 5e-1
R THERM3 7 6 1
R THERM4 6 5 5
R THERM5 5 4 8
R THERM6 4 3 12
R THERM7 3 2 18
R THERM8 2 TL 25

SABER THERMAL MODEL

Copper Area = 1.0 in²
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 =2.0e-3
ctherm.ctherm2 8 7 =5.0e-3
ctherm.ctherm3 7 6 =1.0e-2
ctherm.ctherm4 6 5 =4.0e-2
ctherm.ctherm5 5 4 =9.0e-2
ctherm.ctherm6 4 3 =2e-1
ctherm.ctherm7 3 2 1
ctherm.ctherm8 2 tl 3

rtherm.rtherm1 th 8 =1e-1
rtherm.rtherm2 8 7 =5e-1
rtherm.rtherm3 7 6 =1
rtherm.rtherm4 6 5 =5
rtherm.rtherm5 5 4 =8
rtherm.rtherm6 4 3 =12
rtherm.rtherm7 3 2 =18
rtherm.rtherm8 2 tl =25
}

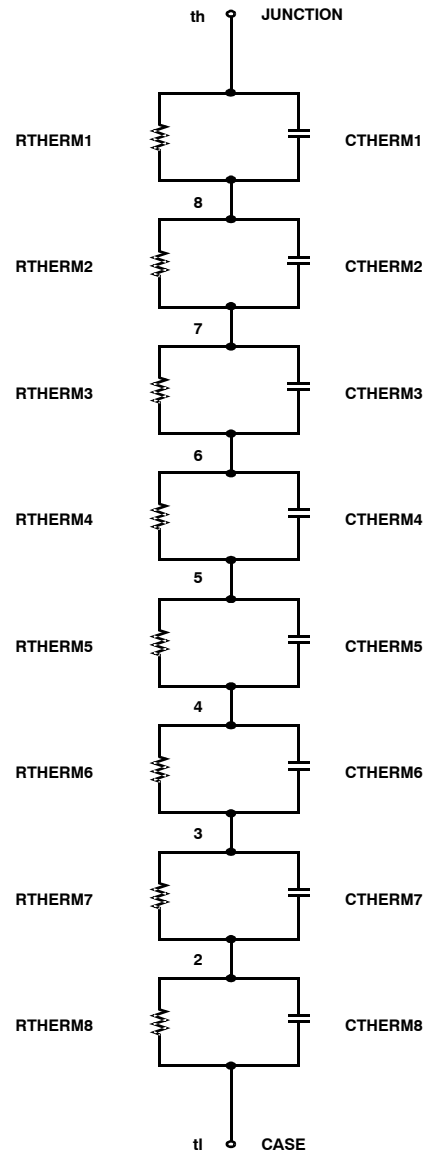


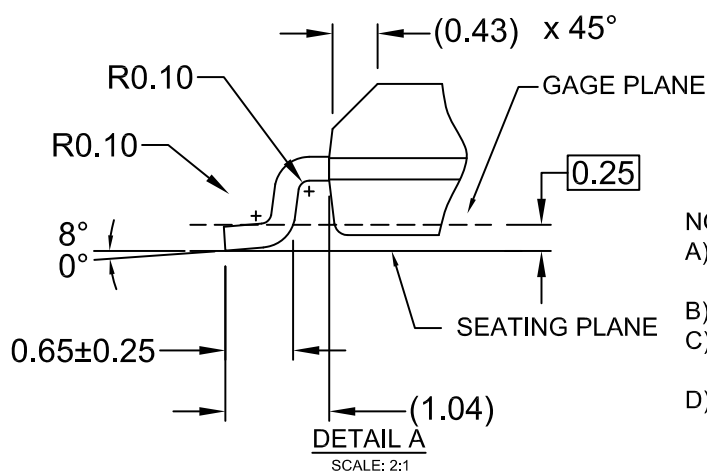
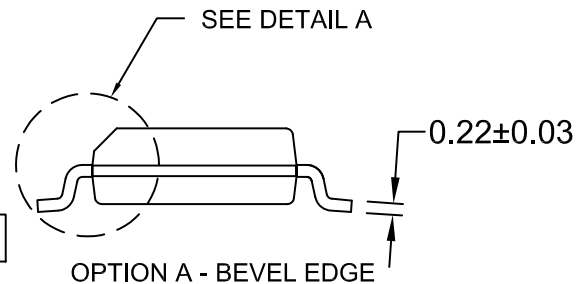
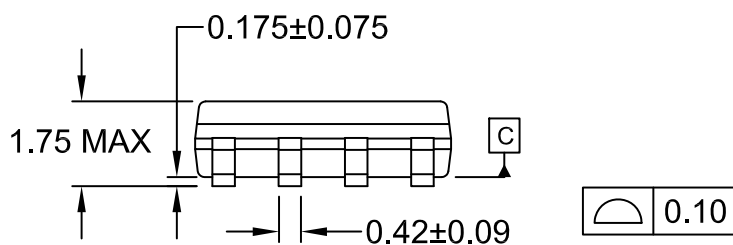
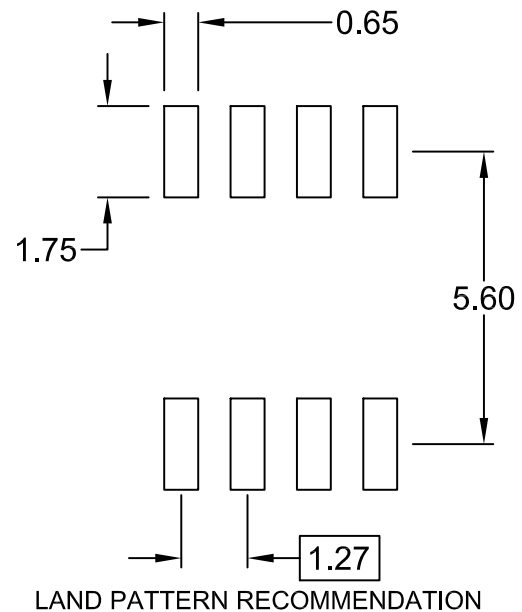
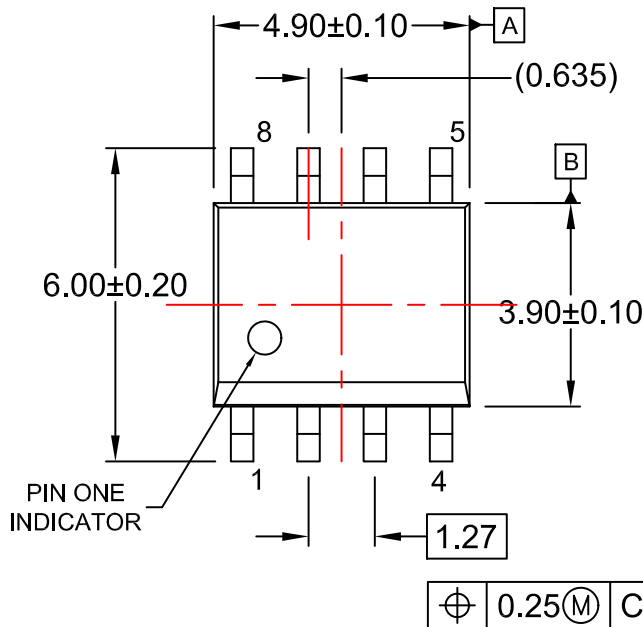
Figure 24.

Table 1. Thermal Models

Component	0.04 in ²	0.28 in ²	0.52 in ²	0.76 in ²	1.0 in ²
CTHERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
R THERM6	26	20	15	13	12
R THERM7	39	24	21	19	18
R THERM78	55	38.7	31.3	29.7	25

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

DOCUMENT NUMBER:	98AON13735G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC8	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales