

MOSFET

StrongIRFET™ 2 Power-Transistor, 30 V

Features

- Optimized for a wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

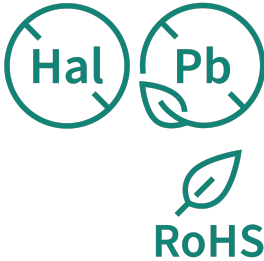
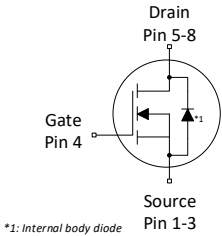
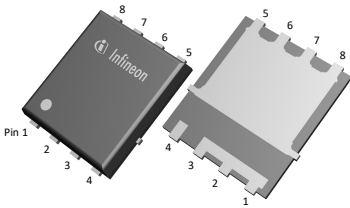
Product validation

Qualified according to JEDEC Standard

Table 1 Key performance parameters

| Parameter | Value | Unit |
|------------------|-------|------|
| V_{DS} | 30 | V |
| $R_{DS(on),max}$ | 2.3 | mΩ |
| I_D | 150 | A |
| Q_{oss} | 26 | nC |
| $Q_g (0V..4.5V)$ | 16 | nC |

PG-TDSON-8



| Type / Ordering code | Package | Marking | Related links |
|----------------------|------------|----------|---------------|
| ISC023N03LF2S | PG-TDSON-8 | 023N03F2 | - |



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|----------------|--------|------|------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 150 106 27 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}$ ²⁾ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 600 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 109 218 | mJ | $I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$ $I_D=25\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 94 3.0 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}$ ²⁾ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 175 | °C | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | R_{thJC} | - | - | 1.6 | °C/W | - |
| Thermal resistance, junction - case, top | R_{thJC} | - | - | 20 | °C/W | |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾ | R_{thJA} | - | - | 50 | °C/W | |

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|----------------------------------|---------------|--------|--------------|------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 30 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=2\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 1.35 | 1.85 | 2.35 | V | $V_{DS}=V_{GS}$, $I_D=40\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 1.96 2.58 | 2.3 3.9 | m Ω | $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$ |
| Gate resistance | R_G | - | 2.2 | - | Ω | - |
| Transconductance ⁶⁾ | g_{fs} | 60 | - | - | S | $ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$ |

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|------------------------------|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 2300 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance | C_{oss} | - | 450 | - | pF | |
| Reverse transfer capacitance | C_{rss} | - | 120 | - | pF | |
| Turn-on delay time | $t_{d(on)}$ | - | 14 | - | ns | $V_{DD}=15\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 9.0 | - | ns | |
| Turn-off delay time | $t_{d(off)}$ | - | 15 | - | ns | |
| Fall time | t_f | - | 8.4 | - | ns | |

Table 6 Gate charge characteristics ⁷⁾

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 7.6 | - | nC | $V_{DD}=15\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 4.2 | - | nC | |
| Gate to drain charge | Q_{gd} | - | 5.0 | - | nC | |
| Switching charge | Q_{sw} | - | 8.5 | - | nC | |
| Gate charge total ⁸⁾ | Q_g | - | 16 | 24 | nC | |
| Gate plateau voltage | $V_{plateau}$ | - | 3.4 | - | V | $V_{DD}=15\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ⁸⁾ | Q_g | - | 33 | 50 | nC | |

Table 6 Gate charge characteristics ⁷⁾

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate charge total, sync. FET ⁸⁾ | $Q_{g(sync)}$ | - | 14 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Output charge ⁸⁾ | Q_{oss} | - | 26 | - | nC | $V_{DS}=15\text{ V}$, $V_{GS}=0\text{ V}$ |

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|----------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 88 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 600 | A | |
| Diode forward voltage | V_{SD} | - | 0.82 | 1.0 | V | $V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$ |
| Reverse recovery time | t_{rr} | - | 18 | - | ns | $V_R=15\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$ |
| Reverse recovery charge | Q_{rr} | - | 46 | - | nC | |

4 Electrical characteristics diagrams

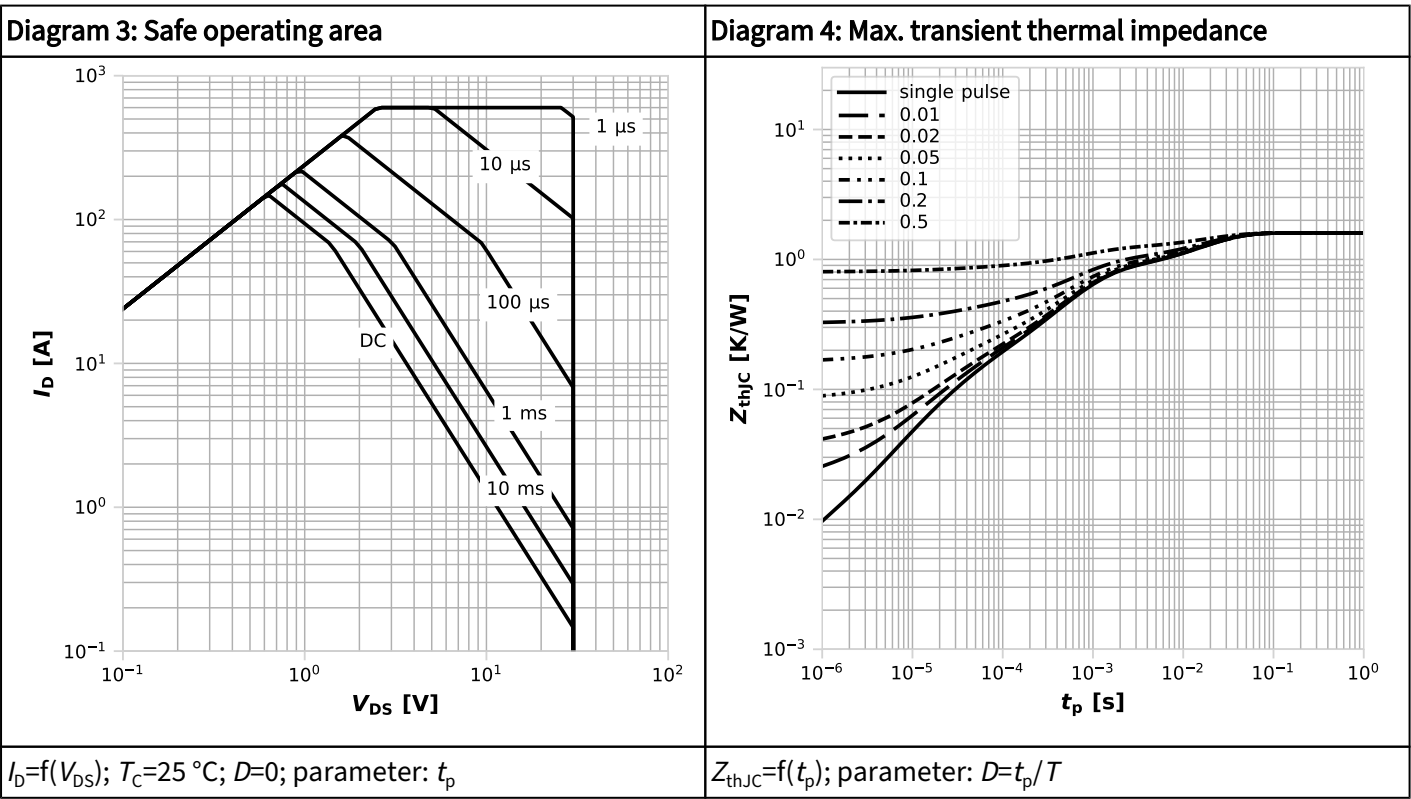
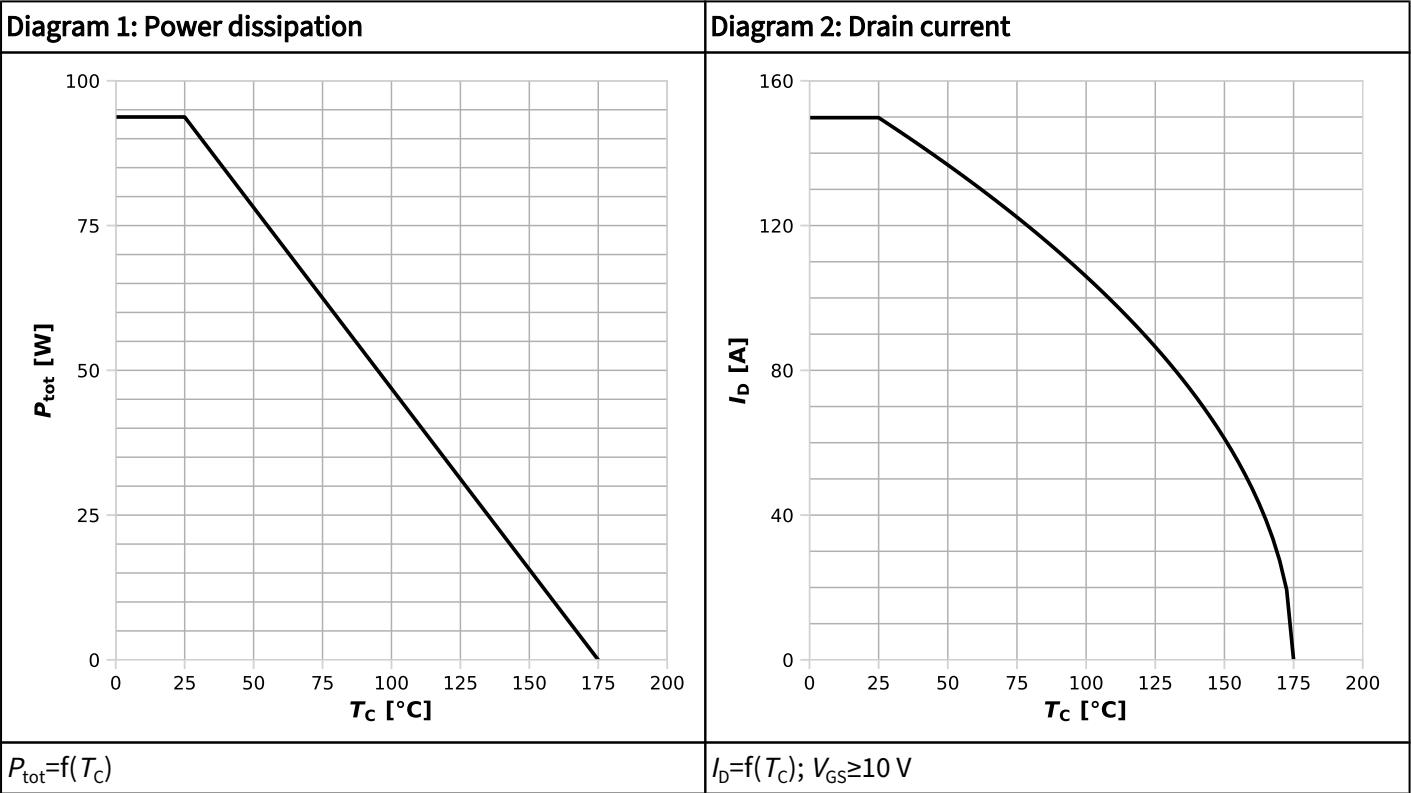
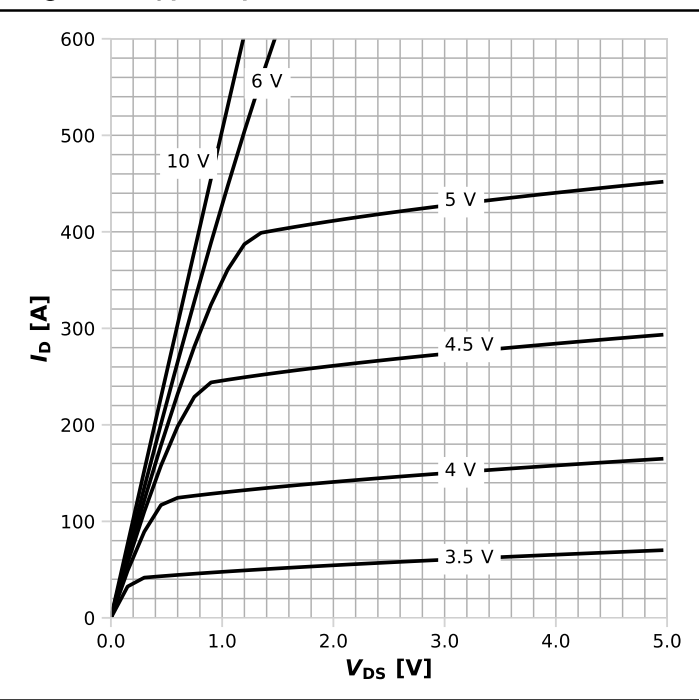
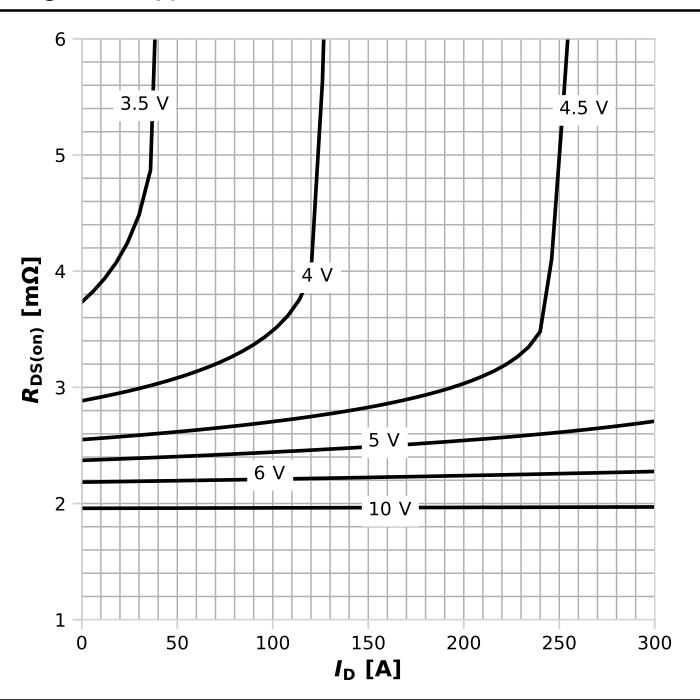


Diagram 5: Typ. output characteristics



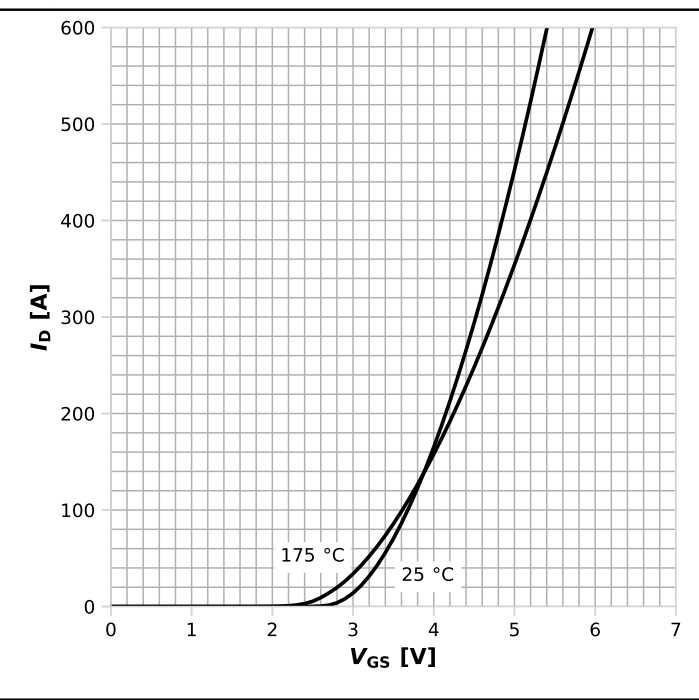
$I_D=f(V_{DS})$, $T_j=25\text{ }^{\circ}\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



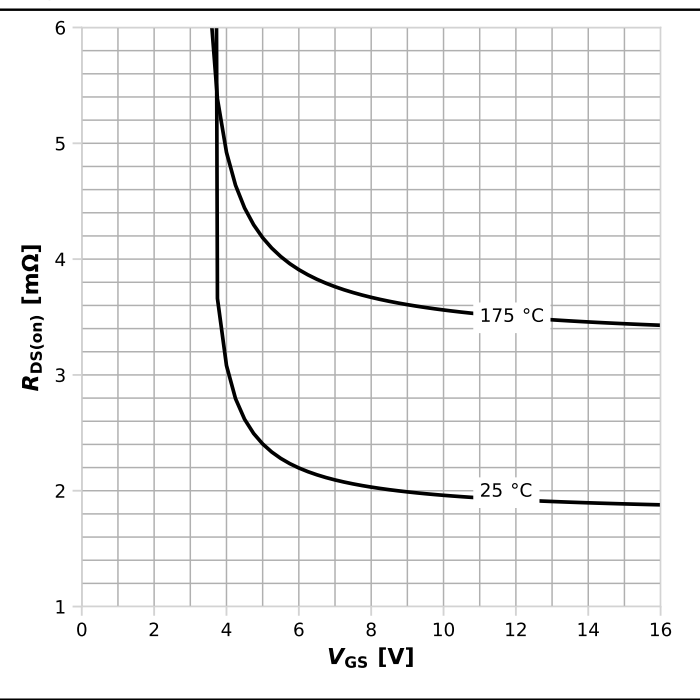
$R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^{\circ}\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



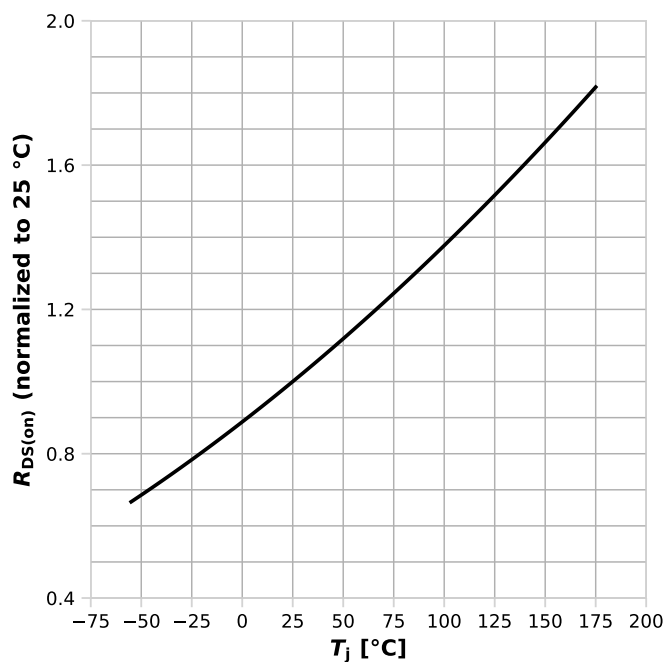
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



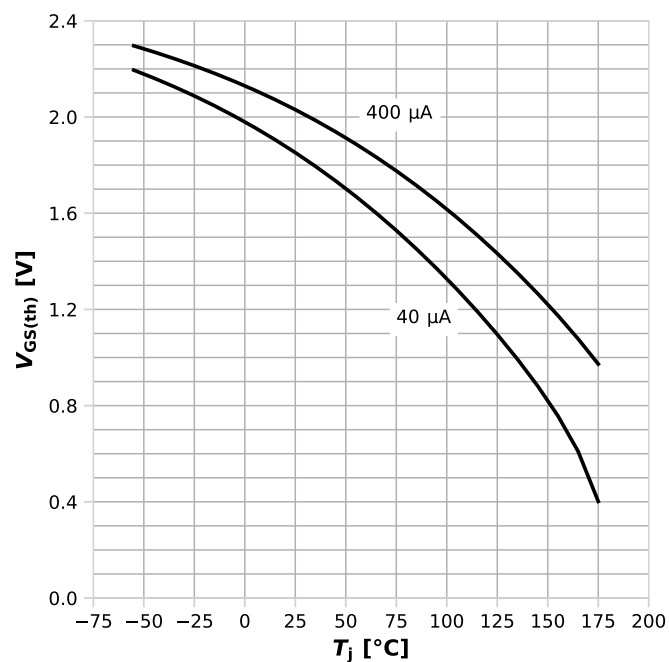
$R_{DS(on)}=f(V_{GS})$, $I_D=50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



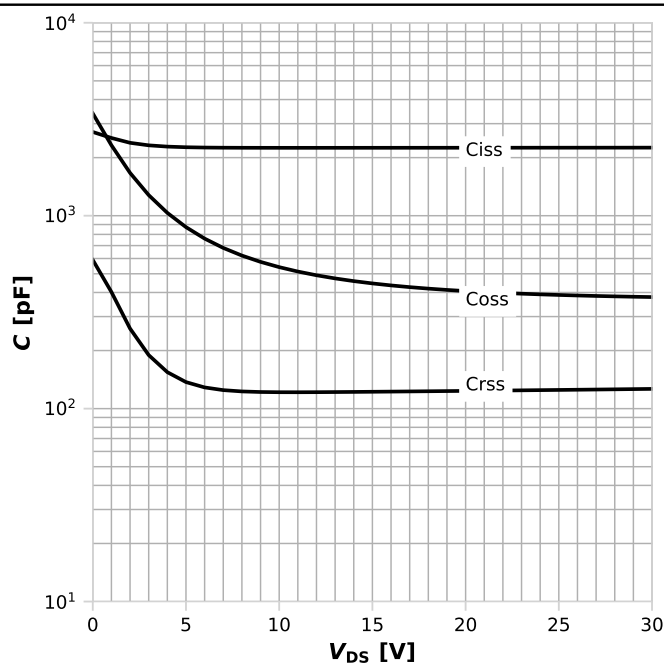
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



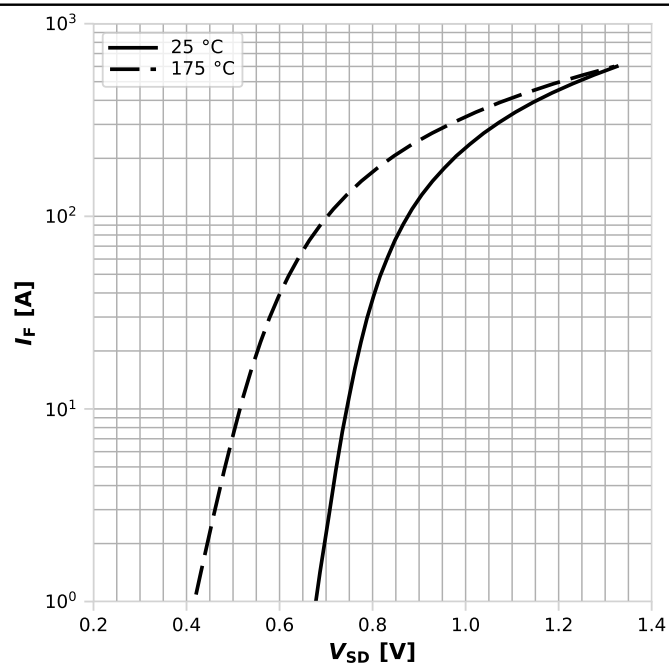
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



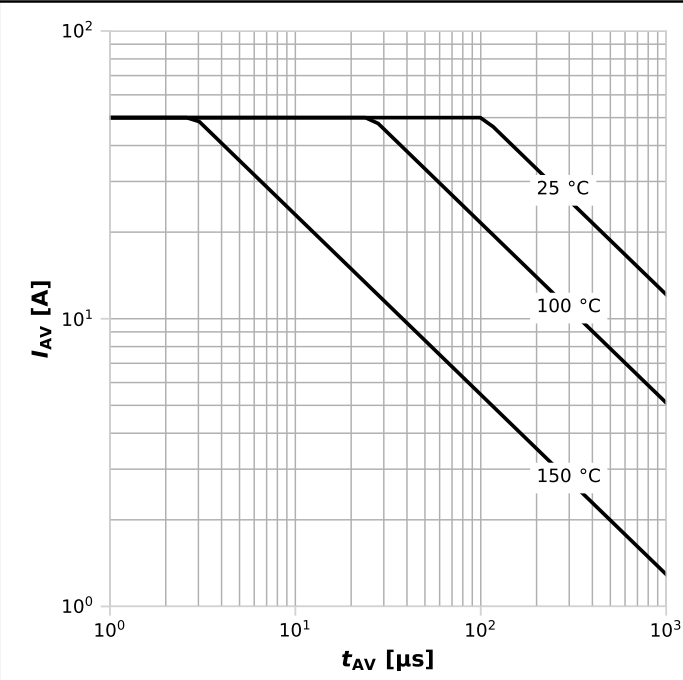
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



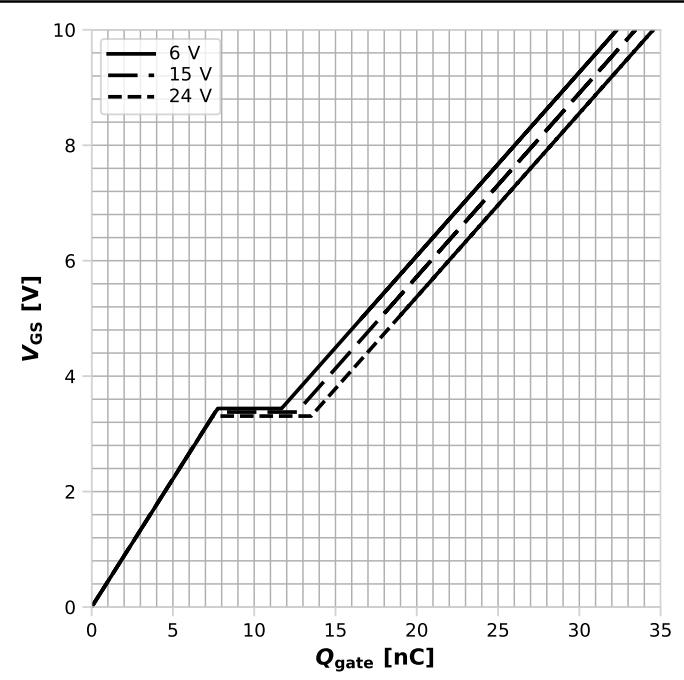
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



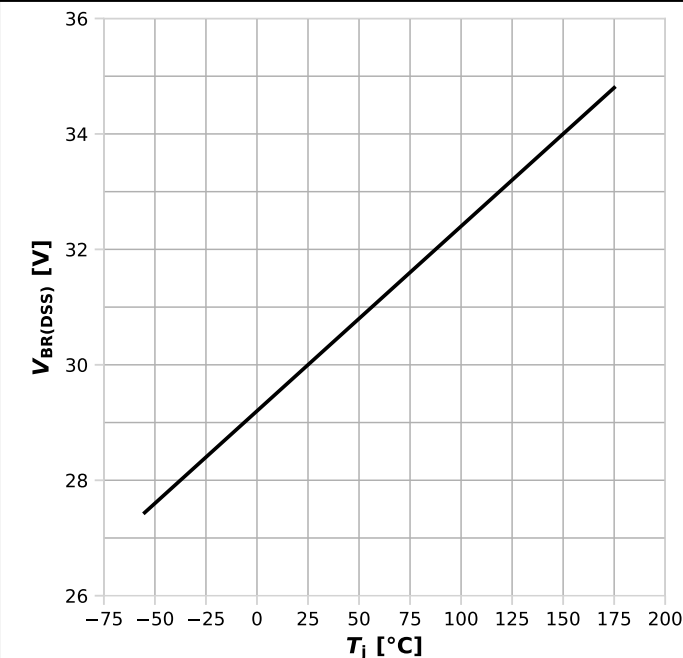
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



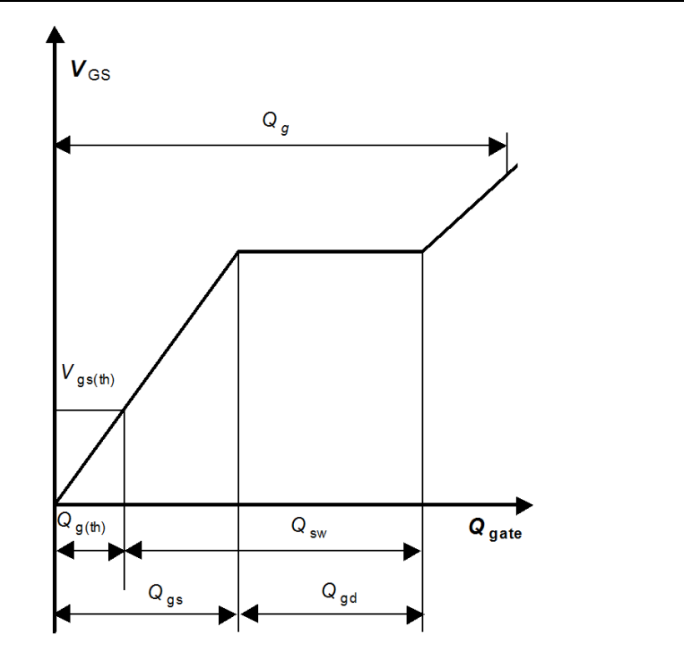
$V_{GS}=f(Q_{gate})$, $I_D=50\text{ A}$ pulsed, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=2\text{ mA}$

Gate charge waveforms



5 Package outlines

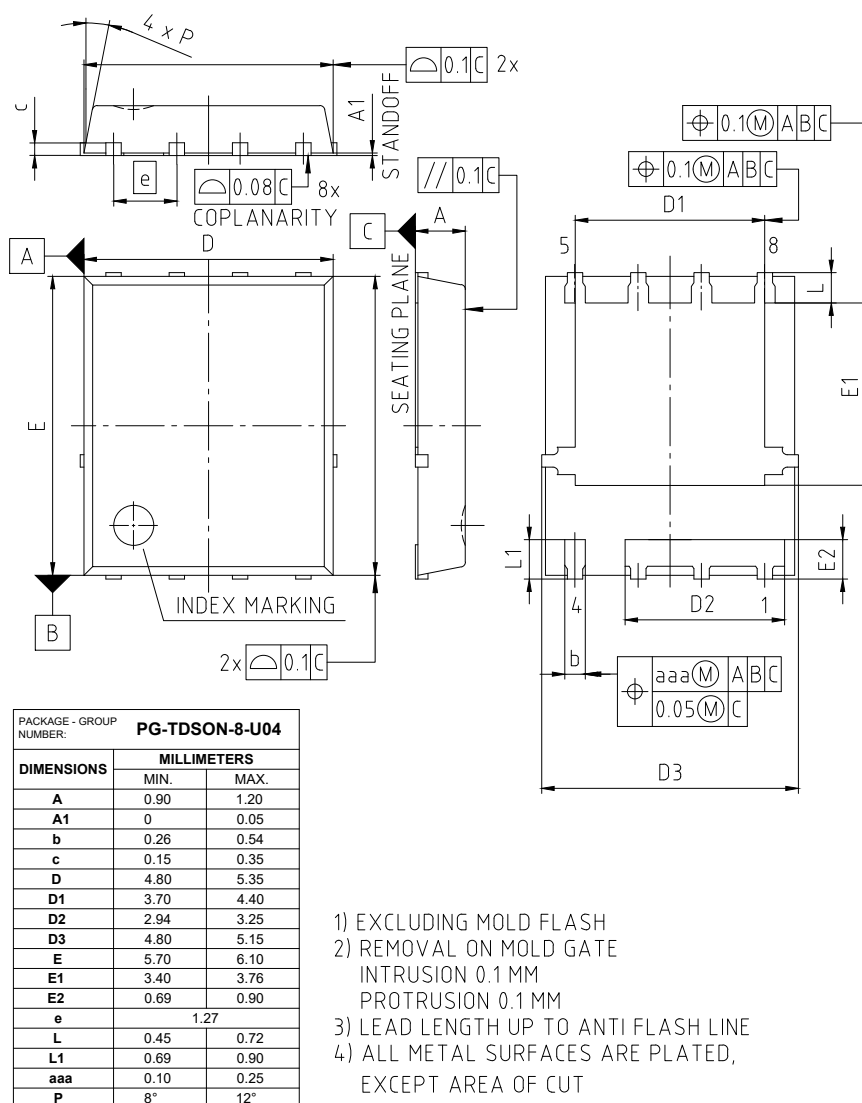


Figure 1 Outline PG-TDSON-8, dimensions in mm

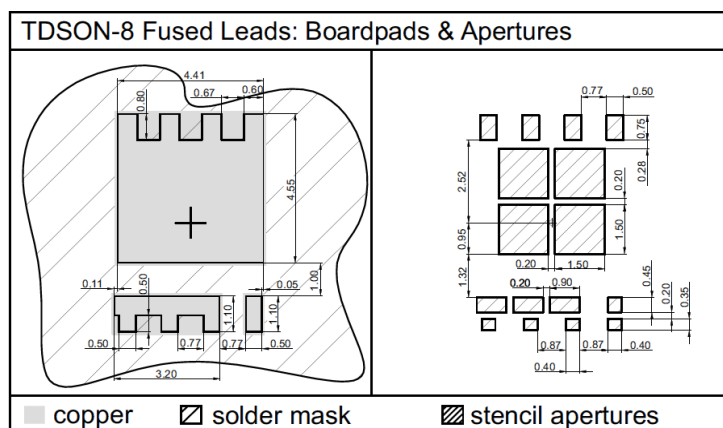


Figure 2 Footprint drawing PG-TDSO-8, dimensions in mm

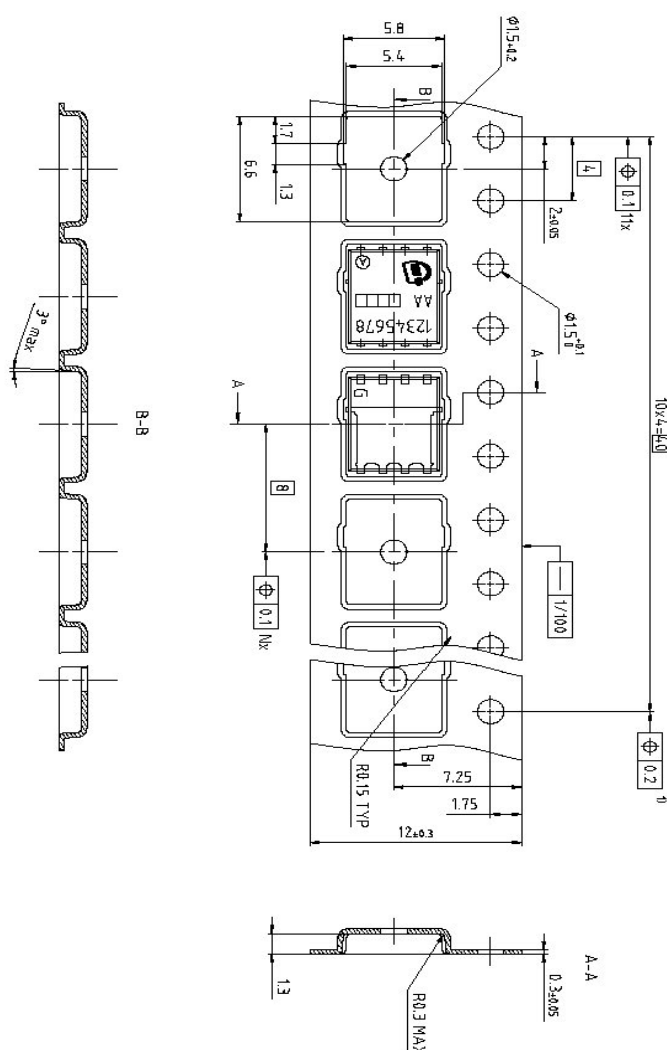


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

ISC023N03LF2S

Revision 2024-11-25, Rev. 1.1

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 1.0 | 2024-11-13 | Release of final |
| 1.1 | 2024-11-25 | updated Package outline |

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