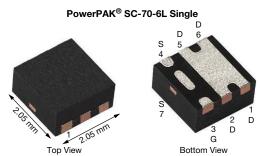


Vishay Siliconix

N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY								
V _{DS} (V)	60							
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0185							
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5 \text{ V}$	0.0225							
Q _g typ. (nC)	6.9							
I _D (A)	12 ^{a, g}							
Configuration	Single							

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} Q_g Figure-of-Merit (FOM)
- Tuned for the lowest R_{DS} Q_{oss}
- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

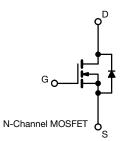


RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Primary side switch
- Synchronous rectification
- DC/DC converters
- · Motor drive switch
- Boost converter
- · LED backlighting



ORDERING INFORMATION							
Package	PowerPAK SC-70						
Lead (Pb)-free and halogen-free	SiA106DJ-T1-GE3						
ADCOLUTE MAYIMUM DATINGS /T	OF OC unless otherwise metadly						

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
PARAMETER		SYMBOL	LIMIT	UNIT			
Drain-source voltage		V_{DS}	60	V			
Gate-source voltage		V_{GS}	± 20	v			
	T _C = 25 °C		12 ^a				
Continuous drain ourrent (T = 150 °C)	T _C = 70 °C	1	12 ^a				
Continuous drain current (T _J = 150 °C)	T _A =25 °C	I _D	10 b, c				
	T _A = 70 °C	†	8.1 ^{b, c}	_			
Pulsed drain current (t = 100 μs)		I _{DM}	40	Α			
Continuous source drain diade surrent	T _C = 25 °C	,	12 ^a				
Continuous source-drain diode current	T _A = 70 °C	- I _S	2.9 b, c	\neg			
Single pulse avalanche current	L = 0.1 mH	I _{AS}	12				
Single pulse avalanche energy	L = 0.1 MH	E _{AS}	7.2	mJ			
	T _C = 25 °C		19				
Manian and a sure aliania ation	T _C = 70 °C		12	14/			
Maximum power dissipation	T _A = 25 °C	P _D	3.5 ^{b, c}	W			
	T _A = 70 °C		2.2 ^{b, c}				
Operating junction and storage temperature	range	T _J , T _{stg}	-55 to +150	°C			
Soldering recommendations (peak tempera	ture) ^{d, e}		260				

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient b, f	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum junction-to-case (drain)	Steady state	R _{thJC}	5.3	6.5	C/VV				

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 80 °C/W
- g. $T_C = 25$ °C



Vishay Siliconix

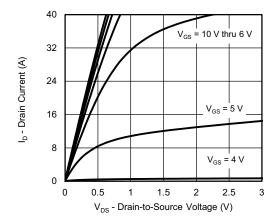
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					l .	
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	35	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu\text{A}$	-	-7.1	-	mV/°
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2	-	4	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA
7		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	_
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 70 °C	-	=	10	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	10	-	-	Α
.	_	V _{GS} = 10 V, I _D = 4 A	-	0.0142	0.0185	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 4 \text{ A}$	-	0.0166	0.0225	Ω
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	-	25	-	S
Dynamic ^b					L	
Input capacitance	C _{iss}		-	540	-	pF
Output capacitance	C _{oss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	150	-	
Reverse transfer capacitance	C _{rss}		-	11	-	
		V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4 A	-	8.9	13.5	nC
Total gate charge	Q_g		-	6.9	10.5	
Gate-source charge	Q _{qs}	$V_{DS} = 30 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 4 \text{ A}$	-	2.5	-	
Gate-drain charge	Q _{qd}		-	1.8	-	
Output charge	Q _{oss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	9	-	
Gate resistance	Ra	f = 1 MHz	0.3	1.3	2.6	Ω
Turn-on delay time	t _{d(on)}		-	10	20	
Rise time	t _r	$V_{DD} = 30 \text{ V}, \text{ R}_L = 7.5 \Omega, \text{ I}_D \cong 4 \text{ A},$	-	5	10	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	14	30	
Fall time	t _f		-	5	10	
Turn-on delay time	t _{d(on)}		-	10	20	ns
Rise time	t _r	$V_{DD} = 30 \text{ V}, R_1 = 7.5 \Omega, I_D \cong 4 \text{ A},$	-	5	10	= = =
Turn-off delay time	t _{d(off)}	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	12	25	
Fall time	t _f		-	5	10	
Drain-Source Body Diode Characteristi	cs		1			
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	12	
Pulse diode forward current	I _{SM}		-	-	40	A
Body diode voltage	V _{SD}	I _S = 4 A, V _{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t _{rr}		-	38	75	ns
Body diode reverse recovery charge	Q _{rr}		-	23	45	nC
Reverse recovery fall time	ta	$I_F = 4 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	17	-	
Reverse recovery rise time	t _b		-	21	-	ns

Notes

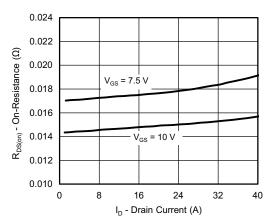
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

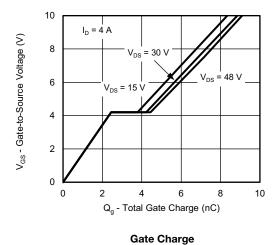


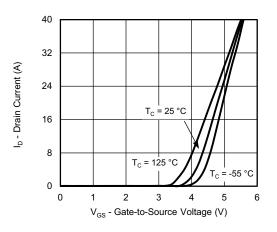


Output Characteristics

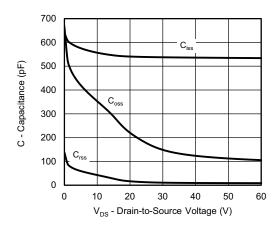


On-Resistance vs. Drain Current and Gate Voltage

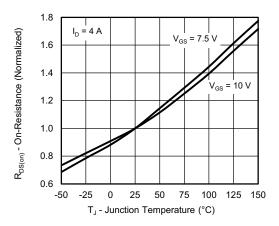




Transfer Characteristics

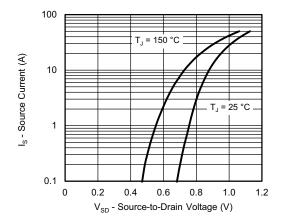


Capacitance

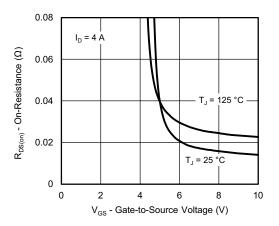


On-Resistance vs. Junction Temperature

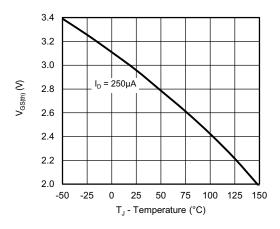




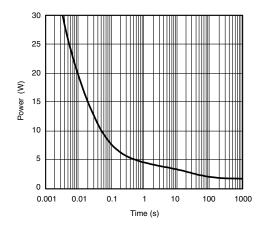
Source-Drain Diode Forward Voltage



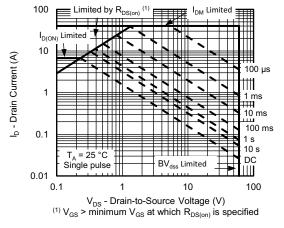
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

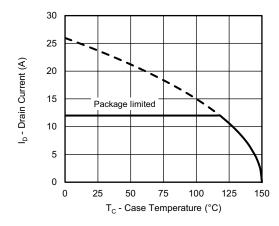


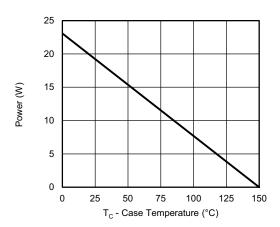
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient







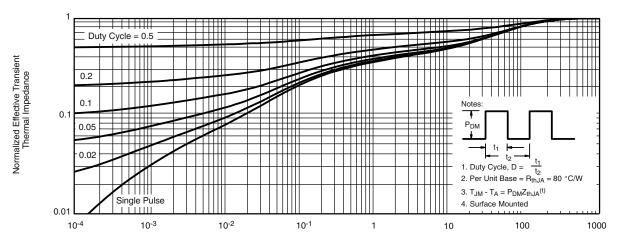
Current Derating a

Power, Junction-to-Case

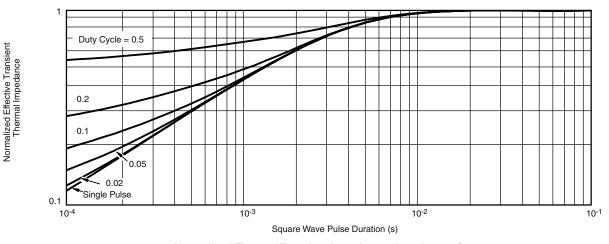
Note

a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76280.





Vishay Siliconix

PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

			SINGL	E PAD			DUAL PAD						
DIM	M	ILLIMETER	RS		INCHES		M	ILLIMETER	RS		INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	,	0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP		0.275 TYP			0.011 TYP			
K1		0.400 TYP	1		0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP	1	0.009 TYP			0.252 TYP			0.010 TYP			
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP	1		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
ECNI- C C	7404 D	. 0 00 1	. 07										

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

Document Number: 73001 06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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