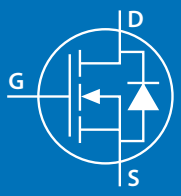
EPC2066 – Enhancement Mode Power Transistor

V_{DS} , 40 V
$R_{DS(on)}$, 1.1 mΩ max
I_D , 90 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised April 17, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

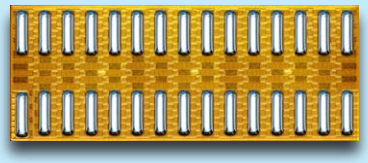
Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous (T_A = 25°C)	90	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	639	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.0	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	51	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90122 EVB)	29	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 1.2 mA	40			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 32 V		0.006	1.0	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.006	4.0	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.2	9.0	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.007	0.3	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 28 mA	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 50 A		0.8	1.1	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.



Die size: 6.05 x 2.3 mm

EPC2066 eGaN® FETs are supplied in passivated die form with solder bumps.

Applications
- High density DC-DC conversion
- Motor drive
- Industrial automation
- Synchronous rectification
- Inrush protection
- Point-of-Load (POL) converters

Benefits
- Ultra high efficiency
- Higher switching frequency
- Very low $R_{DS(on)}$, Q_G, Q_{GD}, Q_{OSS} and 0 Q_{RR}
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2066

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 20 V , V_{GS} = 0 V		3539	4523	pF
C_{RSS}	Reverse Transfer Capacitance			30		
C_{OSS}	Output Capacitance			1670	1919	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 20 V, V_{GS} = 0 V		2431		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			2970		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 50 A		25	33	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 20 V, I_D = 50 A		8.9		
Q_{GD}	Gate to Drain Charge			3.2		
$Q_{G(TH)}$	Gate Charge at Threshold			6.7		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 20 V		59	78	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

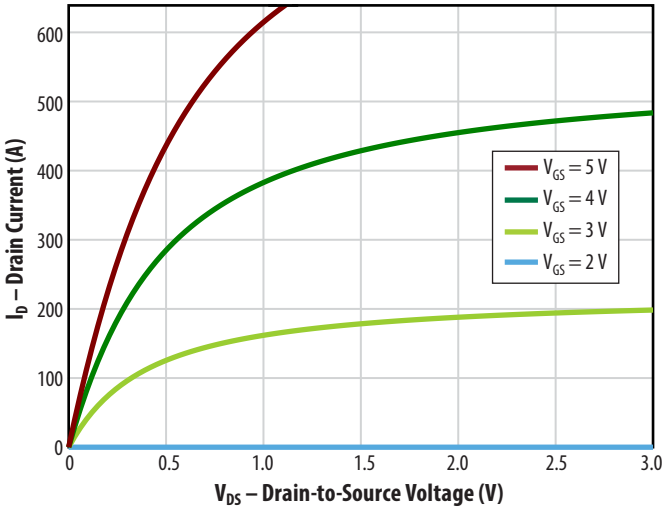


Figure 2: Typical Transfer Characteristics

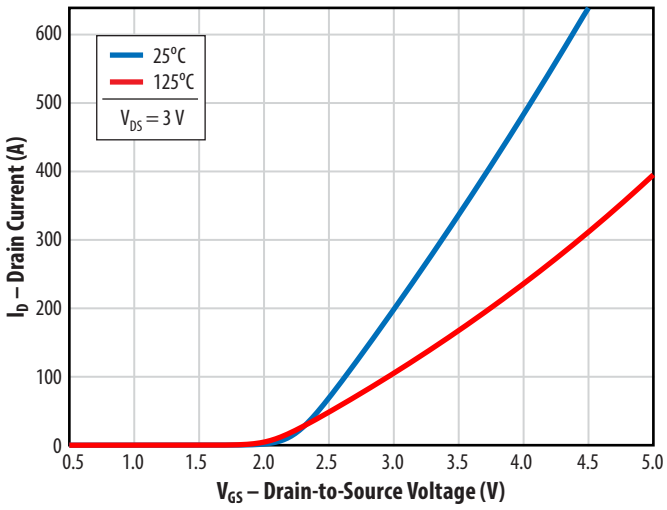


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Currents

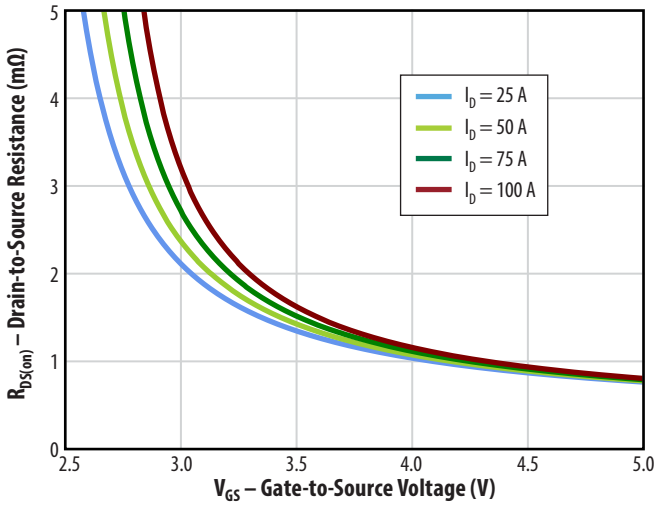


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

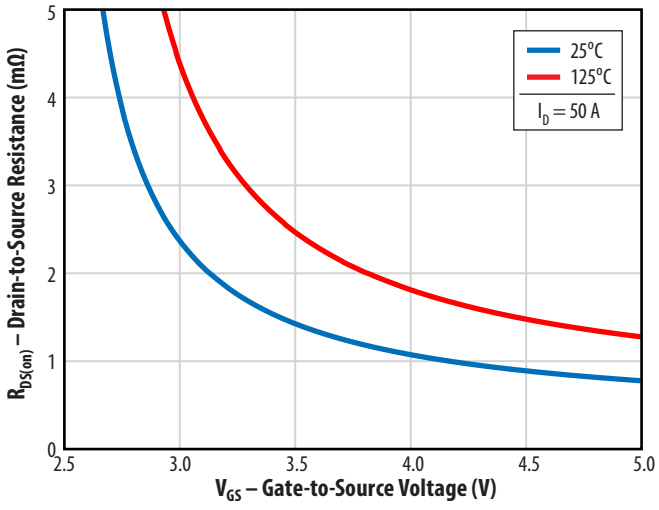


Figure 5a: Typical Capacitance (Linear Scale)

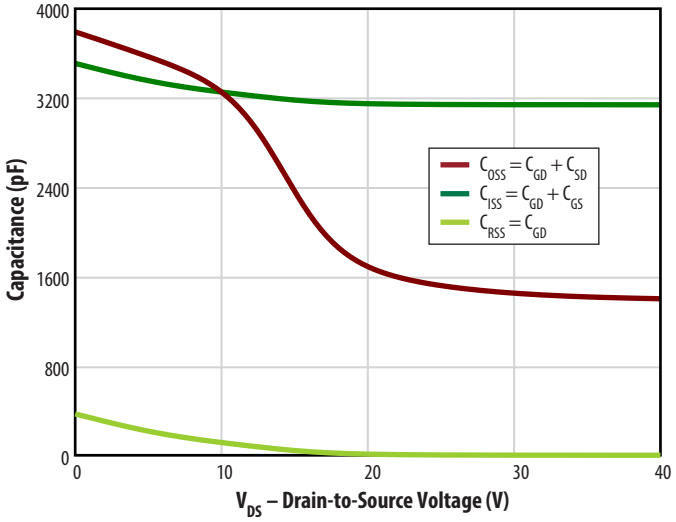


Figure 5b: Typical Capacitance (Log Scale)

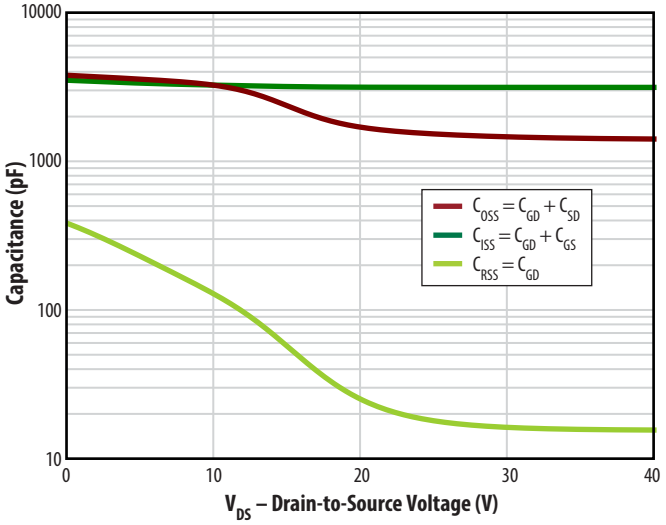


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

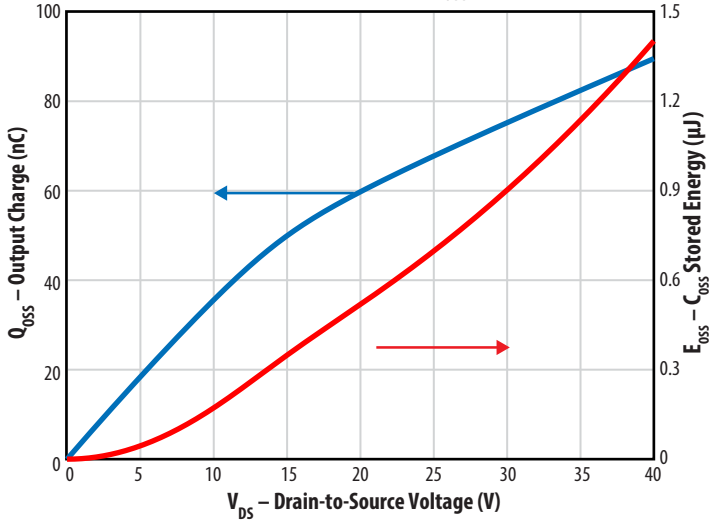


Figure 7: Typical Gate Charge

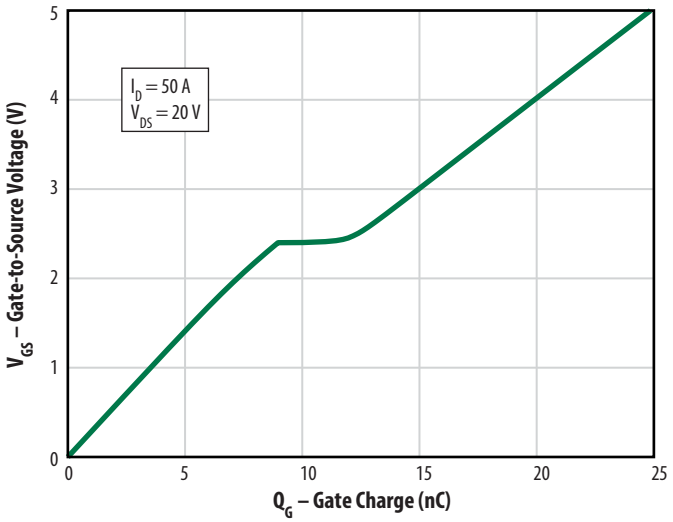


Figure 8: Typical Reverse Drain-Source Characteristics

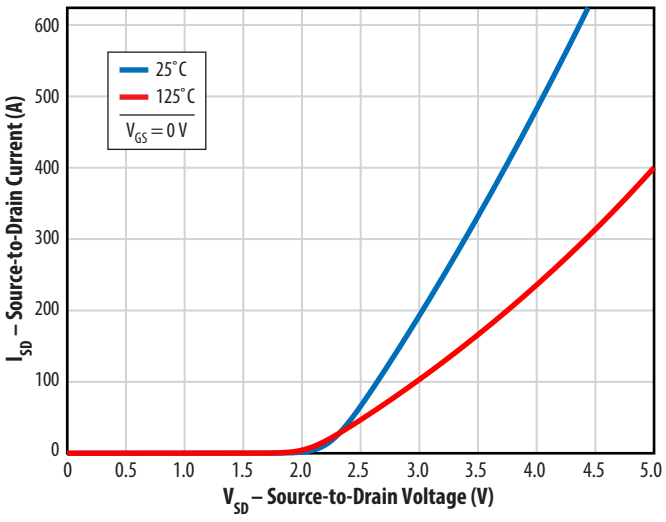
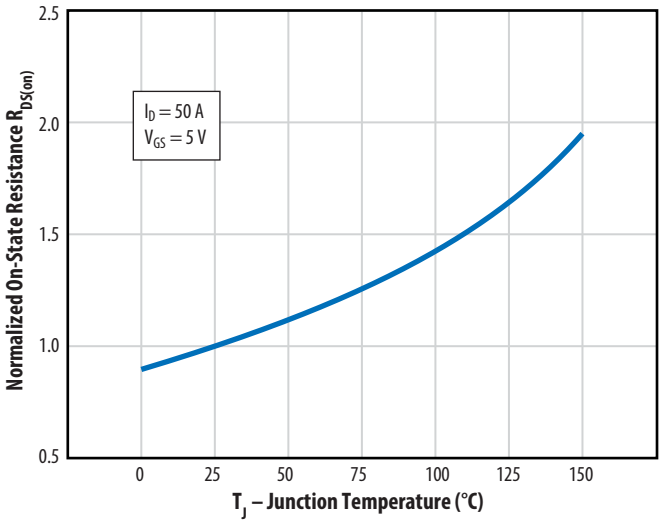


Figure 9: Typical Normalized On-State Resistance vs. Temperatu



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

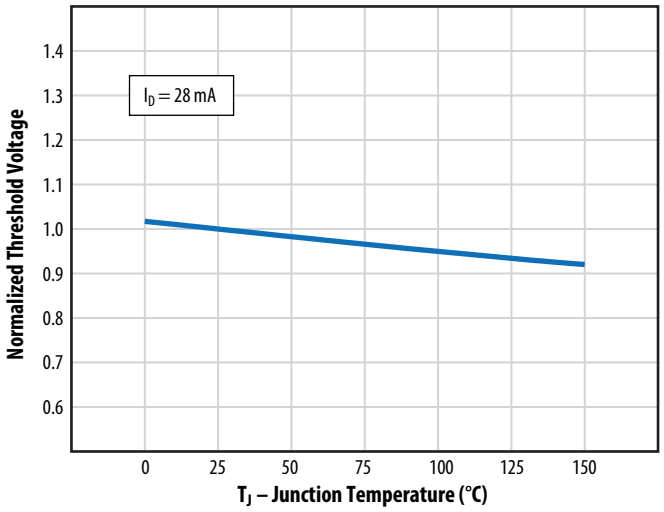
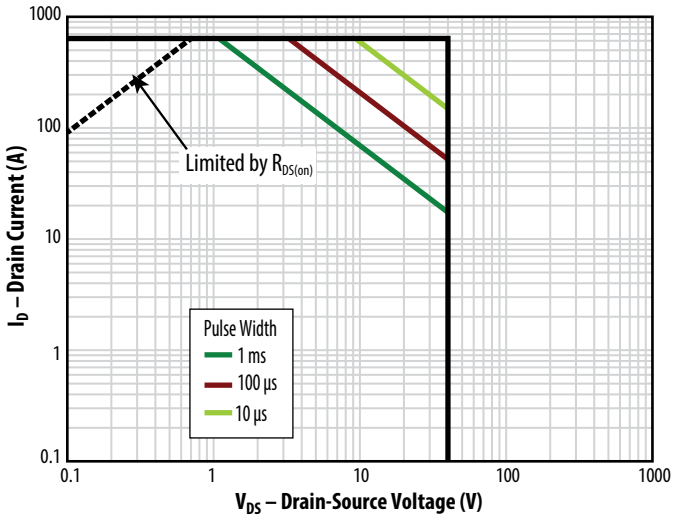


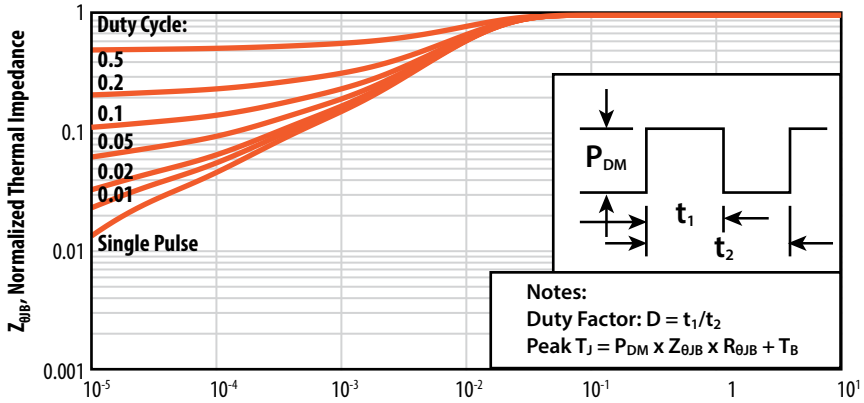
Figure 11: Safe Operating Area



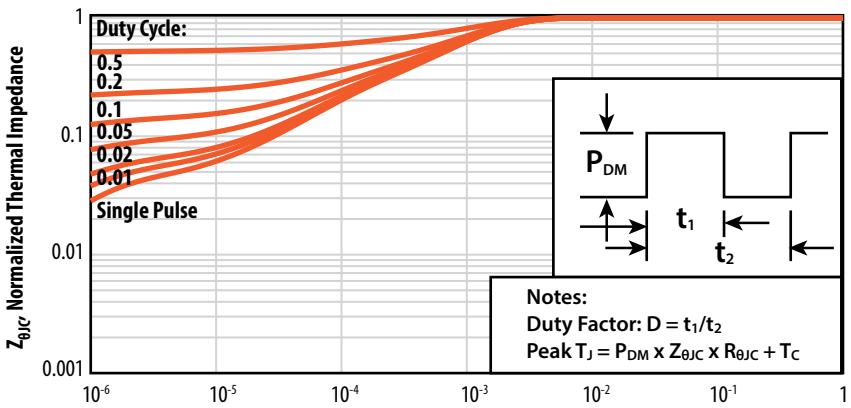
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board

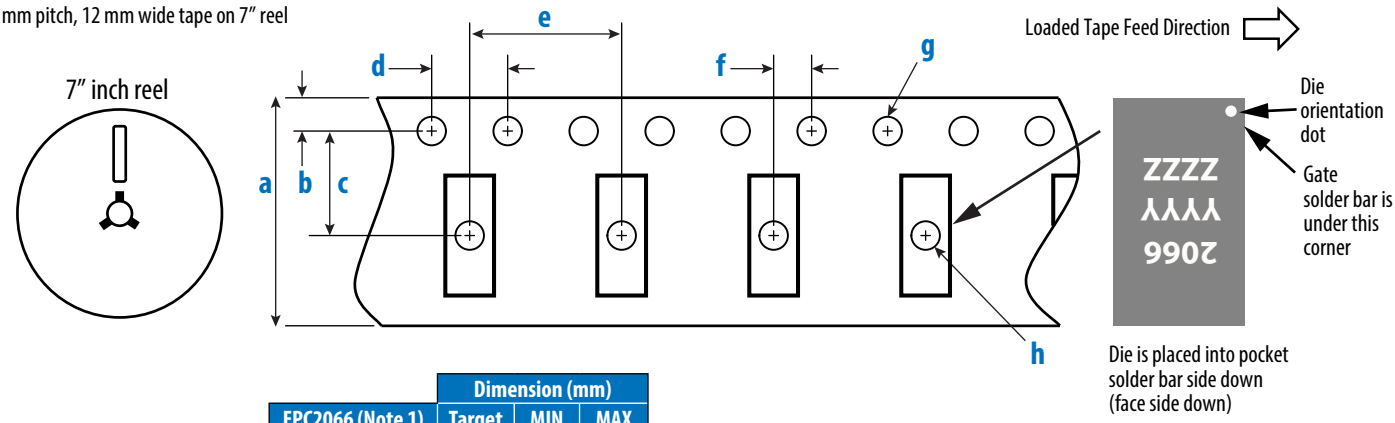


Junction-to-Case



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

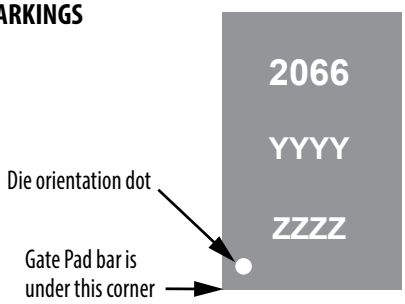


EPC2066 (Note 1)	Dimension (mm) Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

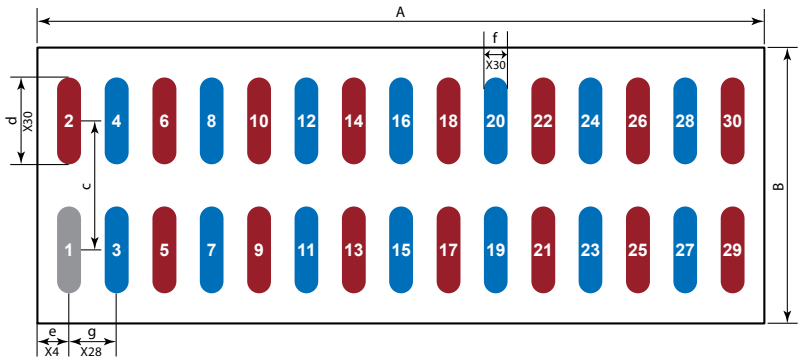
DIE MARKINGS



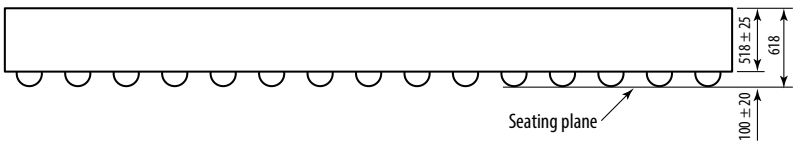
Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2066	2066	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



Side View



DIM	Micrometers MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c		1330	
d		720	
e		225	
f		200	
g		400	

Pad 1 is Gate;

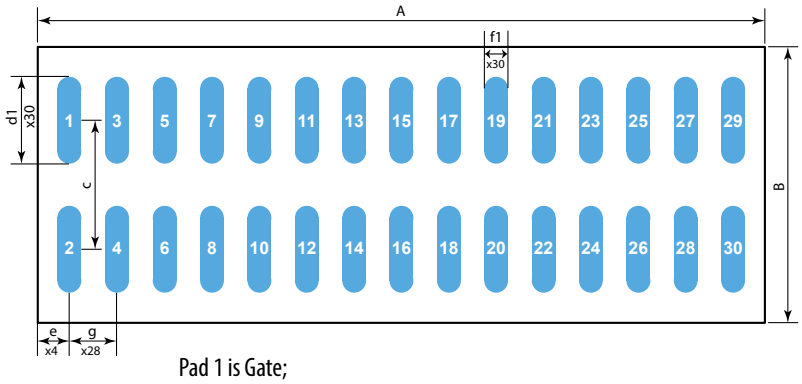
Pads 2 ,5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30 are Source;

Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain

Note: Substrate (top side) connected to source

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined.

DIM	Micrometers
A	6050
B	2300
c	1330
d1	700
e	225
f1	180
g	400

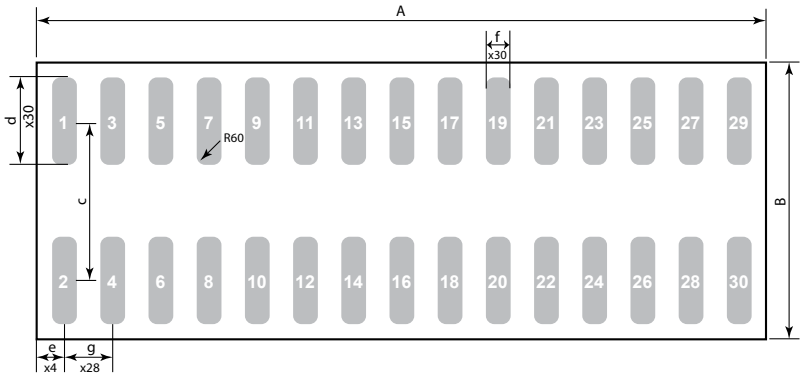
Pad 1 is Gate;

Pads 2, 5, 6, 9,10,13,14, 17, 18, 21, 22, 25, 26, 29. 30 are Source;

Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

DIM	Micrometers
A	6050
B	2300
c	1330
d	700
e	225
f	180
g	400

Additional Resources Available

- Assembly resources available at: https://epc-co.com/epc/design-support
- Library of Altium footprints for production FETs and ICs: https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)