

Automotive MOSFET

OptiMOS™ 5 Power-Transistor







Features

- OptiMOS[™] power MOSFET for automotive applications
- N-channel enhancement mode normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested
- Very low reverse recovery charge (Q_{rr})



General automotive applications.

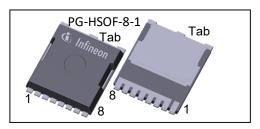
Product validation

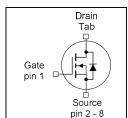
Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	120	V
R _{DS(on)}	1.7	mΩ
I _D (chip limited)	314	А

Туре	Package	Marking
IAUTN12S5N017	PG-HSOF-8-1	5N12N017





IAUTN12S5N017



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Maximum ratings

at T_i=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I D	V _{GS} =10 V, Chip limitation ^{1,2)}	314	A
		V _{GS} =10V, DC current ³⁾	300	
		T_a =100 °C, V_{GS} =10 V, R_{thJA} on 2s2p ^{2,4)}	37	
Pulsed drain current ²⁾	/ _{D,pulse}	T _C =25 °C, t _p = 100 μs	1170	7
Avalanche energy, single pulse ²⁾	E AS	/ _D =150 A	510	mJ
Avalanche current, single pulse	I _{AS}	-	300	А
Gate source voltage	V _{GS}	-	±20	V
Power dissipation	P tot	Т _С =25 °С	358	W
Operating and storage temperature	$T_{\rm j}, T_{\rm stg}$	-	-55 +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

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Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values		Unit	
			min.	typ.	max.	
Thermal resistance, junction - case	R thJC	-	-	-	0.42	K/W
Thermal resistance, junction - ambient ⁴⁾	R thJA	-	-	14.8	-	

Electrical characteristics

at T_i=25 °C, unless otherwise specified

Parameter	Symbol	Symbol Conditions		Values		
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0 V, I _D =1 mA	120	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =270 μA	2.6	3.1	3.6	
Zero gate voltage drain current	I _{DSS}	V _{DS} =120 V, V _{GS} =0 V, T _j =25 °C	-	0.3	3	μΑ
		V_{DS} =120 V, V_{GS} =0 V, T_{j} =100 °C ²⁾	-	10	100	
Gate-source leakage current	I _{GSS}	V _{GS} =20 V, V _{DS} =0 V	-	-	100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =7 V, I _D =50 A	-	2.0	2.8	mΩ
		V _{GS} =10 V, I _D =100 A	-	1.5	1.7	
Gate resistance ²⁾	R _G	-	-	1.1	-	Ω



Parameter	Symbol	Symbol Conditions		Values	Unit	
			min.	typ.	max.	
Dynamic characteristics ²⁾	-					
Input capacitance	C iss		-	8260	10740	pF
Output capacitance	C oss	V_{GS} =0 V, V_{DS} =60 V, f =1 MHz	-	2369	3080	
Reverse transfer capacitance	C _{rss}	1	-	45	68	
Turn-on delay time	t d(on)		-	27	-	ns
Rise time	t _r	$V_{\rm DD}$ =60 V, $V_{\rm GS}$ =10 V,	-	47	-	
Turn-off delay time	t d(off)	$I_{\rm D}$ =100 A, $R_{\rm G}$ =3.5 Ω	-	43	-	
Fall time	t _f]	-	47	-	
Gate Charge Characteristics ²⁾				1 42		L.c
Gate to source charge	Q gs		_	43	55	nC
Gate to drain charge	Q _{gd}	V_{DD} =60 V, I_{D} =100 A,	-	23	35	
Gate charge total	Q _g	V _{GS} =0 to 10 V	_	111	145	
Gate plateau voltage	$V_{ m plateau}$		-	5.2	-	V
Reverse Diode						
Diode continous forward current ²⁾	I _s	Т _С =25 °С	-	-	314	А
Diode pulse current ²⁾	I _{S,pulse}	T _C =25 °C, t _p = 100 μs	-	-	1170	
Diode forward voltage	V _{SD}	V_{GS} =0 V, I_F =100 A, T_j =25 °C	-	0.85	0.95	V
Reverse recovery time ²⁾	t rr	V _R =60 V, I _F =50A,	-	45	67	ns
Reverse recovery charge ²⁾	Q rr	$di_F/dt = 100 \text{ A/}\mu\text{s}$	-	34	68	nC

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¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production testing – specified by design.

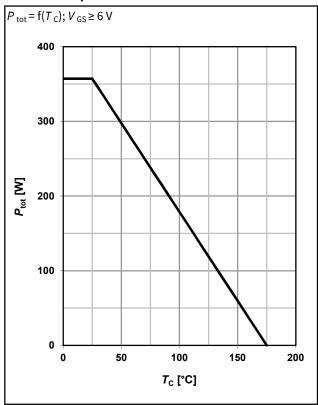
³⁾ Current is limited by package.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

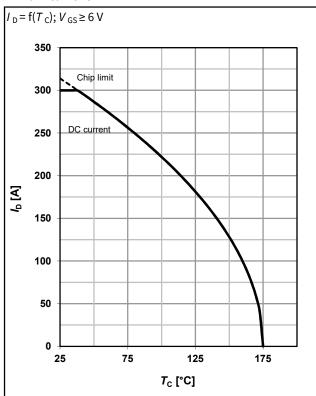


Electrical characteristics diagrams

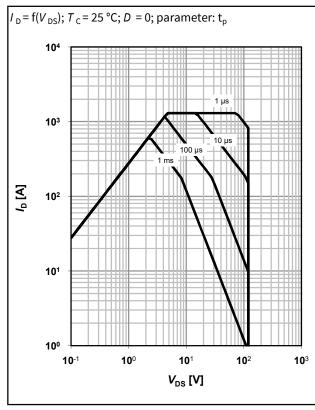
1 Power dissipation



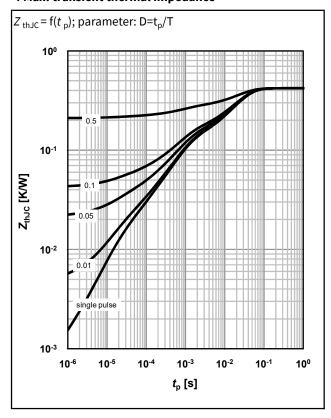
2 Drain current



3 Safe operating area

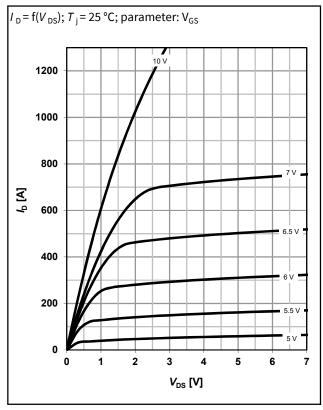


4 Max. transient thermal impedance

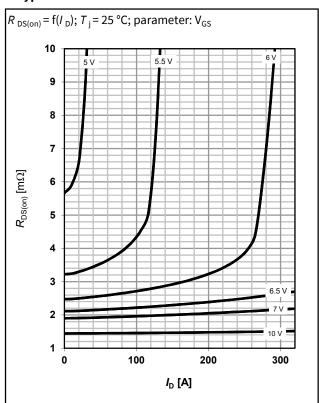




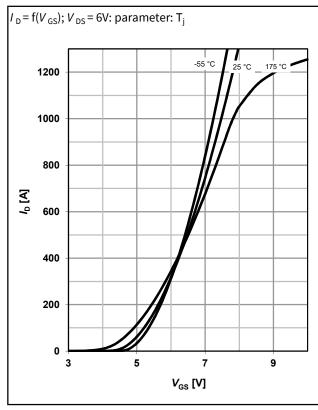
5 Typ. output characteristics



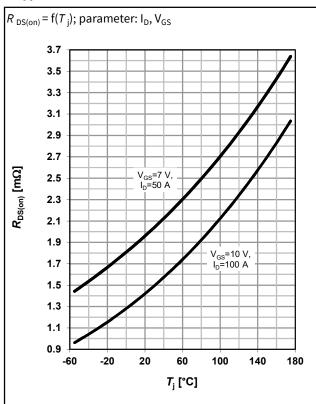
6 Typ. drain-source on-state resistance



7 Typ. transfer characteristics

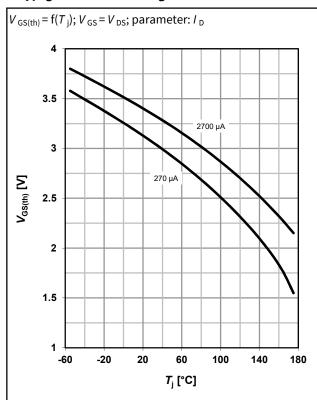


8 Typ. drain-source on-state resistance

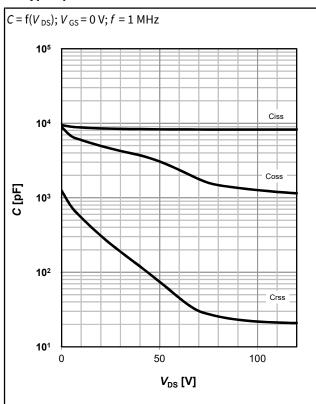


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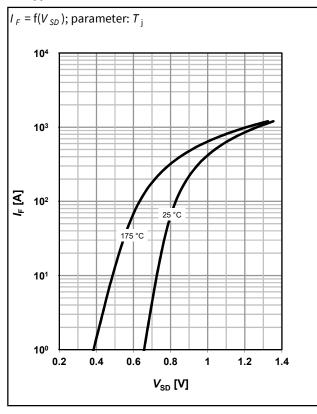
9 Typ. gate threshold voltage



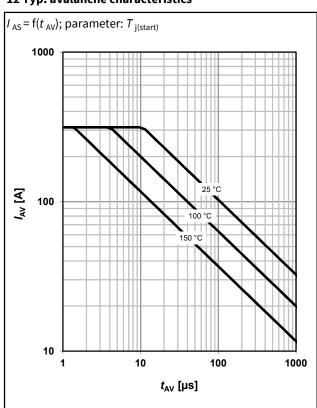
10 Typ. capacitances



11 Typical forward diode characteristics

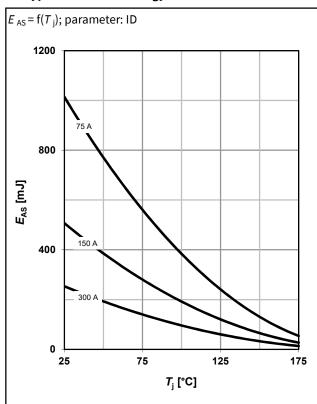


12 Typ. avalanche characteristics

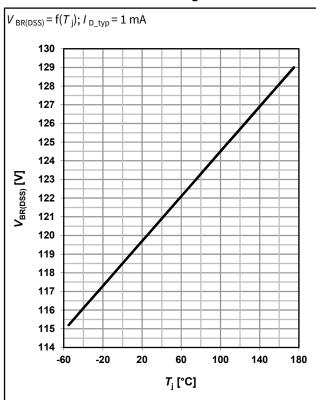


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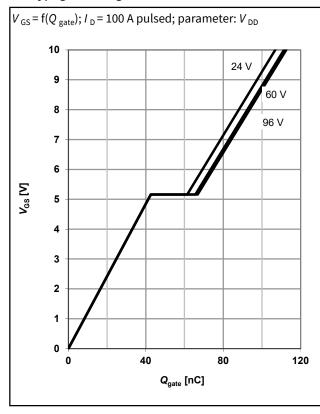
13 Typical avalanche energy



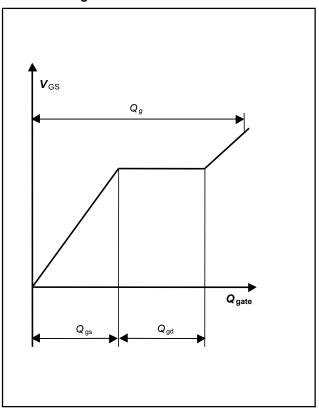
14 Drain-source breakdown voltage



15 Typ. gate charge



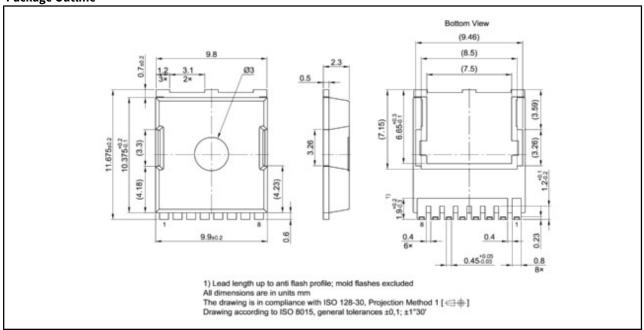
16 Gate charge waveforms



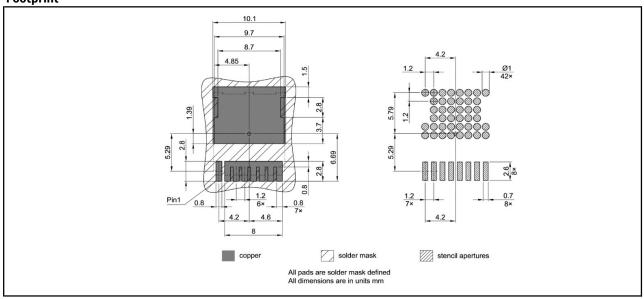
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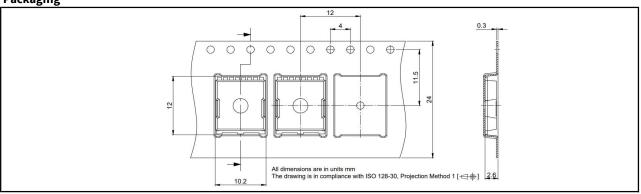
Package Outline



Footprint



Packaging



IAUTN12S5N017



Revision History

Revision	Date	Changes
Revision 1.0	2022-12-15	Final data sheet

Trademarks

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