

## OptiMOS™-T2 Power-Transistor



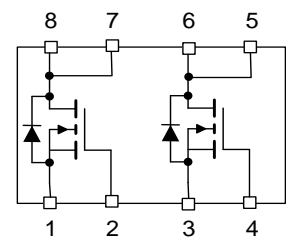
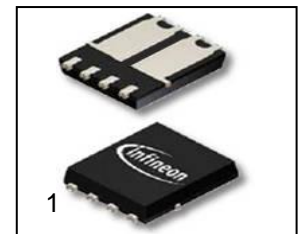
### Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Automatic optical inspection (AOI) capable

### Product Summary

$V_{DS}$	40	V
$R_{DS(on),max}^{4)}$	18	mΩ
$I_D^{2)}$	20	A

PG-TDSON-8



Type	Package	Marking
IPG20N04S4L-18A	PG-TDSON-8	4N04L18

**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}^{1,2)}$	20	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{2)}$	20	
Pulsed drain current <sup>2)</sup> one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse <sup>2, 4)</sup>	$E_{AS}$	$I_D=10\text{ A}$	25	mJ
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	15	A
Gate source voltage	$V_{GS}$	-	±16	V
Power dissipation one channel active	$P_{tot}$	$T_C=25\text{ °C}$	26	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55...+175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Thermal characteristics<sup>2)</sup>

Thermal resistance, junction - case	$R_{thJC}$	-	-	-	5.6	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	100	-	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	60	-	

### Electrical characteristics, at $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=8\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current <sup>4)</sup>	$I_{DSS}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS}=18\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=85\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current <sup>4)</sup>	$I_{GSS}$	$V_{GS}=16\text{ V}$ , $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance <sup>4)</sup>	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$ , $I_D=17\text{ A}$ ,	-	21.4	26.0	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=17\text{ A}$	-	15.2	18.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Dynamic characteristics<sup>2)</sup>

Input capacitance <sup>4)</sup>	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	824	1071	pF
Output capacitance <sup>4)</sup>	$C_{oss}$		-	178	231	
Reverse transfer capacitance <sup>4)</sup>	$C_{rss}$		-	7	16	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=20\text{ A}, R_G=11\text{ }\Omega$	-	2.4	-	ns
Rise time	$t_r$		-	0.4	-	
Turn-off delay time	$t_{d(off)}$		-	12.7	-	
Fall time	$t_f$		-	5.0	-	

### Gate Charge Characteristics<sup>2, 4)</sup>

Gate to source charge	$Q_{gs}$	$V_{DD}=32\text{ V}, I_D=20\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	2.7	5.0	nC
Gate to drain charge	$Q_{gd}$		-	1.2	3.0	
Gate charge total	$Q_g$		-	10.5	15.0	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V

### Reverse Diode

Diode continuous forward current <sup>2)</sup> one channel active	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	20	A
Diode pulse current <sup>2)</sup> one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=17\text{ A}, T_J=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=20\text{ V}, I_F=I_S, di_F/dt=100\text{ A}/\mu\text{s}$	-	25	-	ns
Reverse recovery charge <sup>2, 4)</sup>	$Q_{rr}$		-	15	-	nC

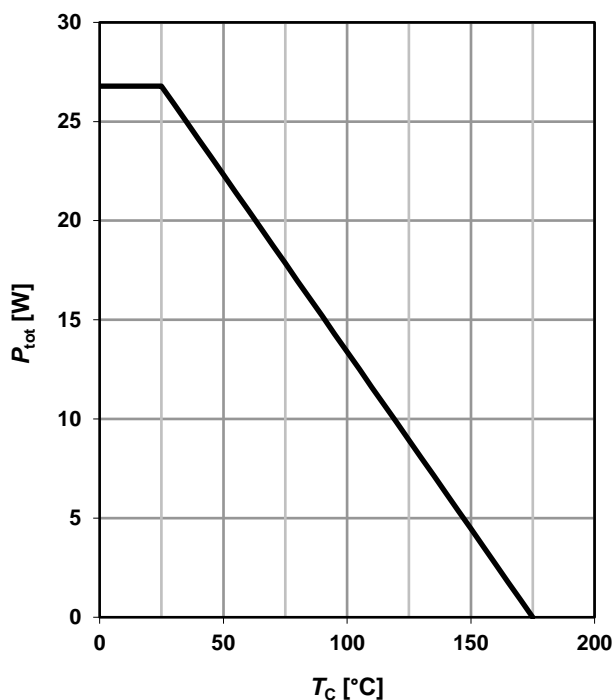
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC}=5.6\text{ K/W}$  the chip is able to carry 30 A at 25°C.

<sup>2)</sup> Specified by design. Not subject to production test.

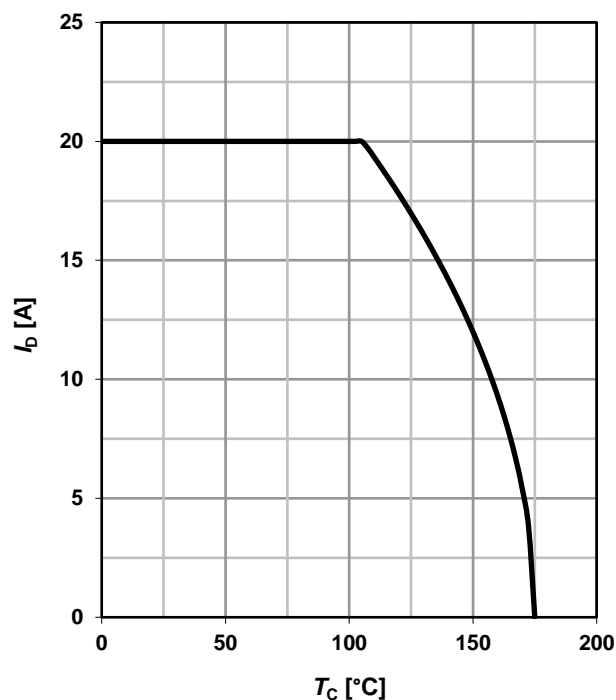
<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup> Per channel

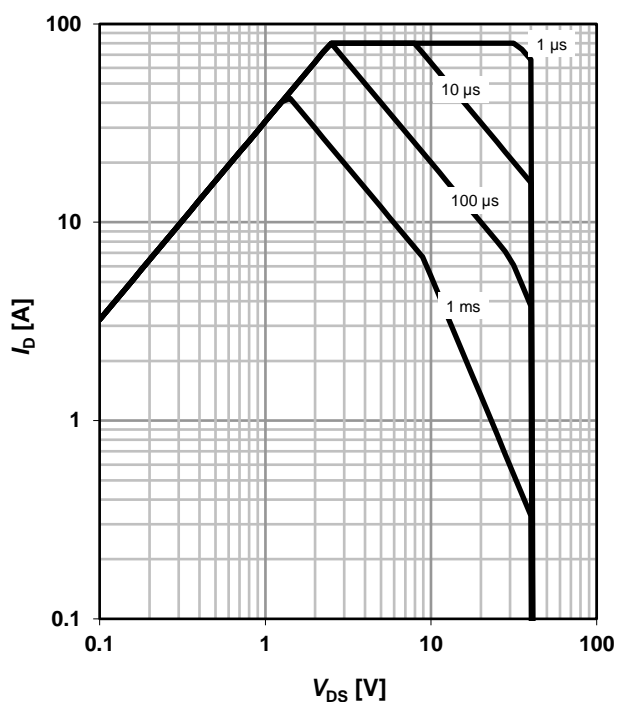
### 1 Power dissipation

 $P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$ 


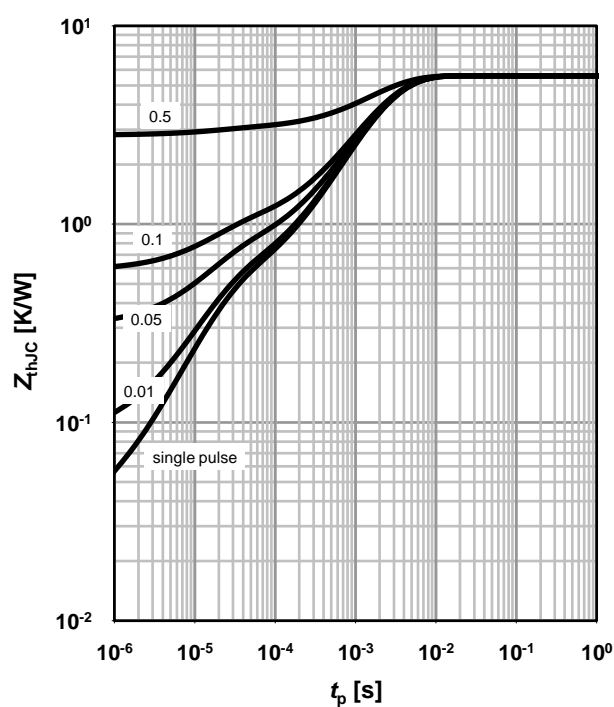
### 2 Drain current

 $I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$ 


### 3 Safe operating area

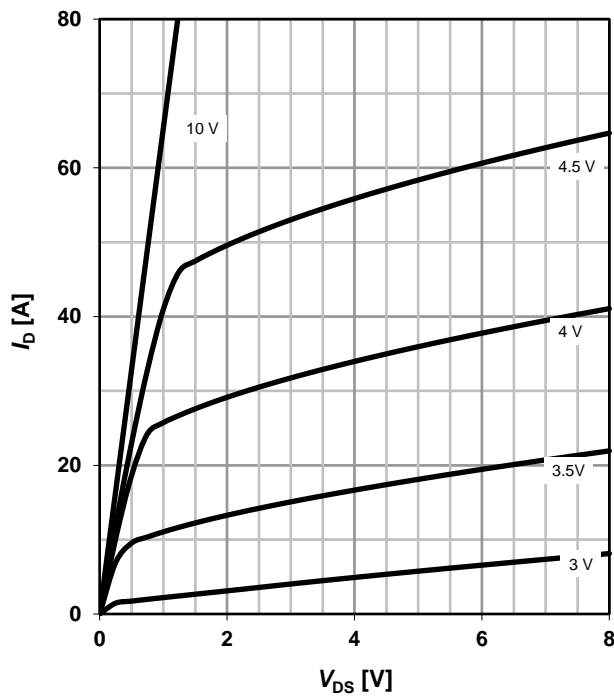
 $I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0; \text{ one channel active}$   
 parameter:  $t_p$ 


### 4 Max. transient thermal impedance

 $Z_{\text{thJC}} = f(t_p)$   
 parameter:  $D = t_p / T$ 


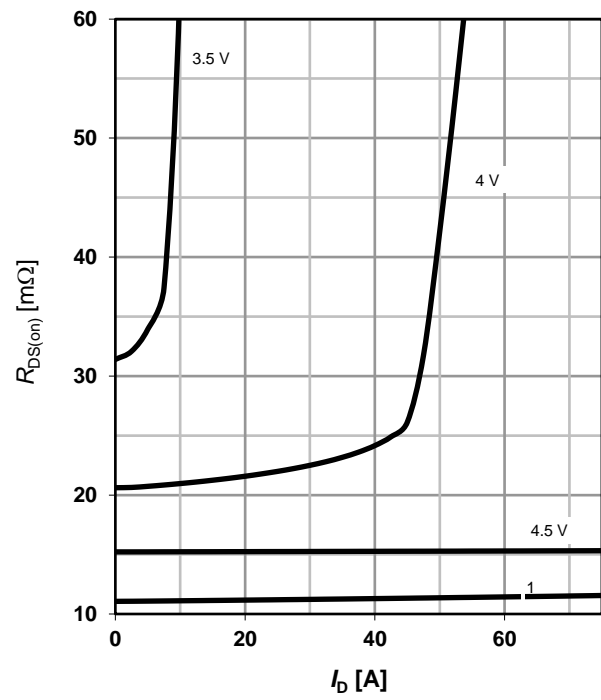
#### 5 Typ. output characteristics<sup>4)</sup>

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$ 

parameter:  $V_{GS}$ 


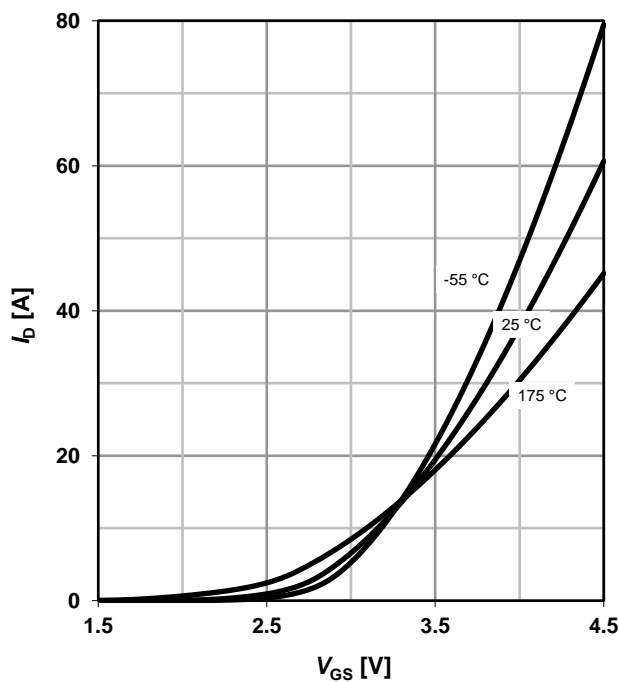
#### 6 Typ. drain-source on-state resistance<sup>4)</sup>

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$ 

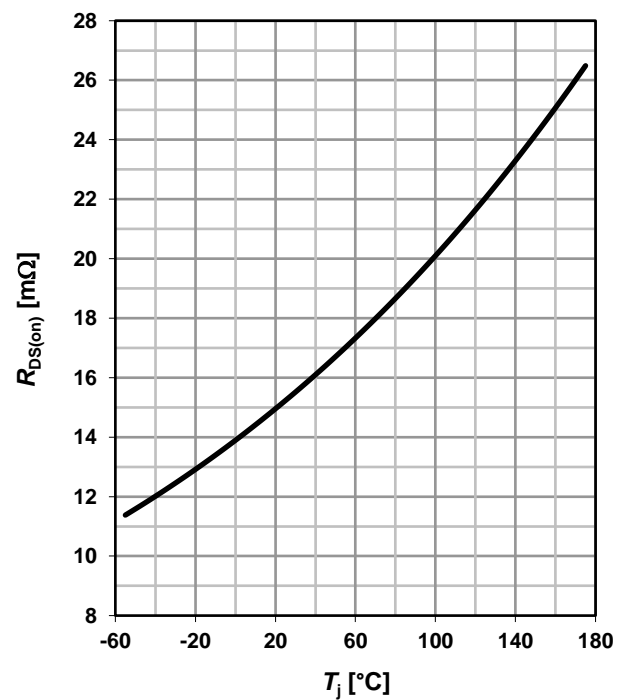
parameter:  $V_{GS}$ 


#### 7 Typ. transfer characteristics<sup>4)</sup>

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$ 

parameter:  $T_j$ 


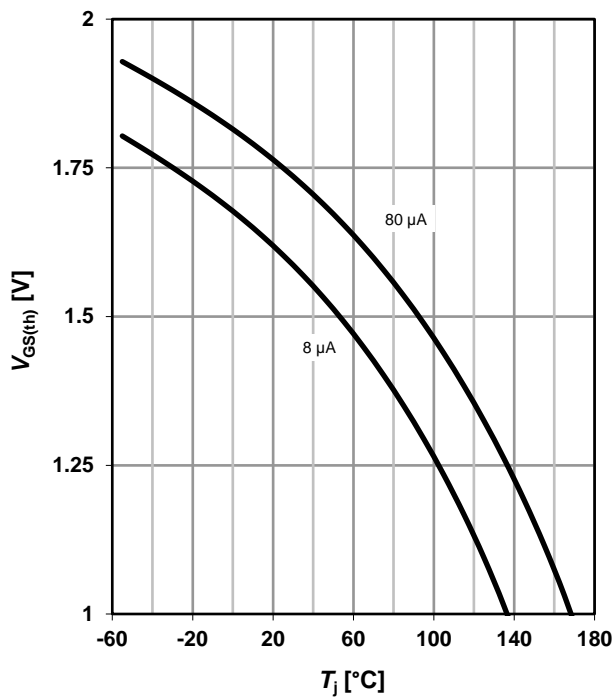
#### 8 Typ. drain-source on-state resistance<sup>4)</sup>

 $R_{DS(on)} = f(T_j); I_D = 17\text{ A}; V_{GS} = 10\text{ V}$ 


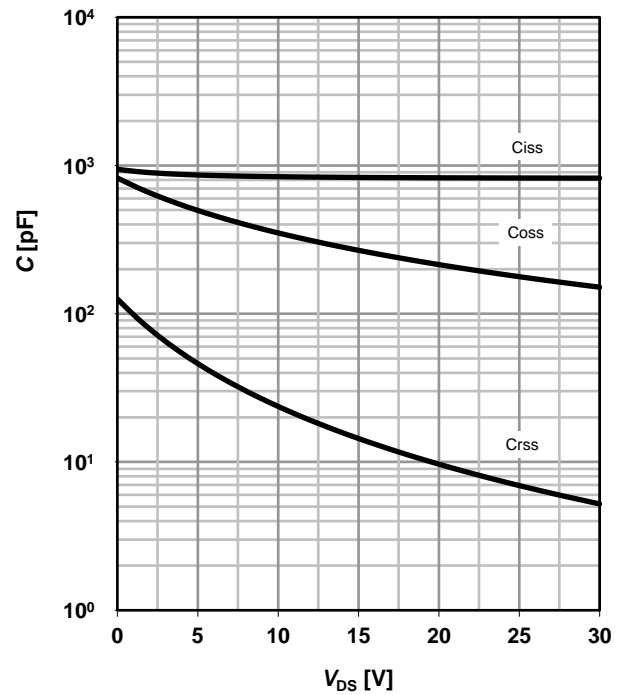
**9 Typ. gate threshold voltage**

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$

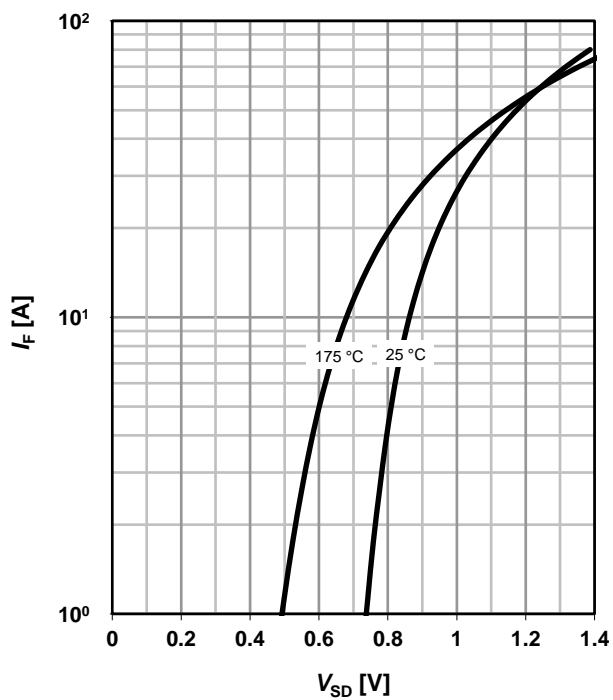

**10 Typ. Capacitances<sup>4)</sup>**

$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$


**11 Typical forward diode characteristics<sup>4)</sup>**

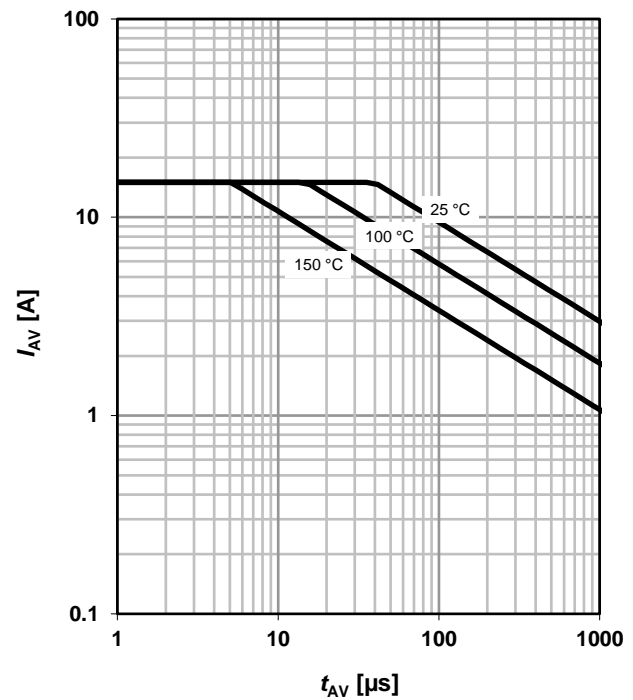
$$I_F = f(V_{SD})$$

parameter:  $T_j$


**12 Avalanche characteristics<sup>4)</sup>**

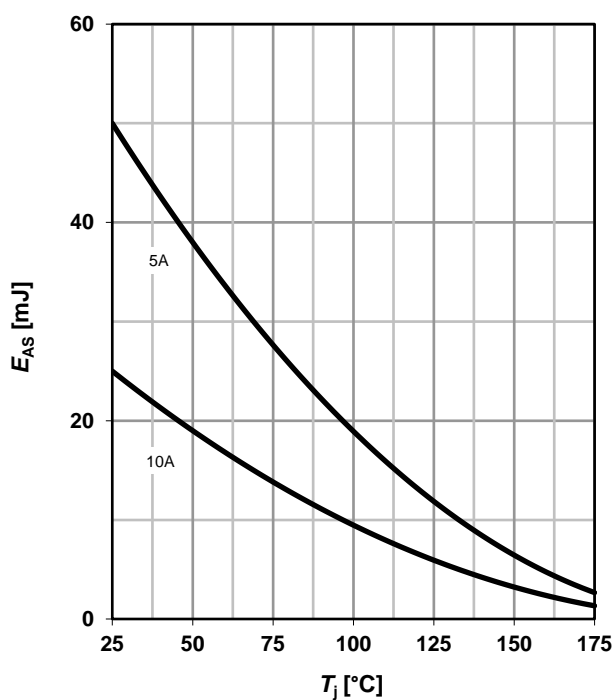
$$I_{AS} = f(t_{AV})$$

parameter:  $T_{j(start)}$



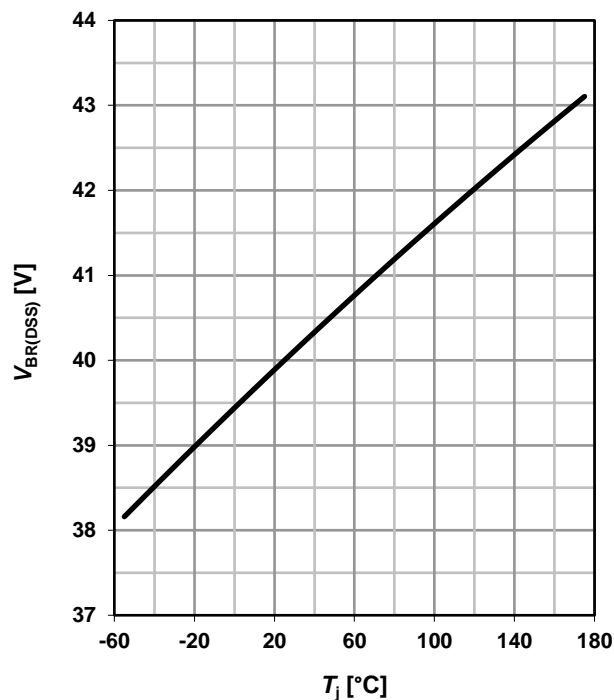
### 13 Avalanche energy<sup>4)</sup>

$$E_{AS} = f(T_j); I_D = 10A$$



### 14 Drain-source breakdown voltage

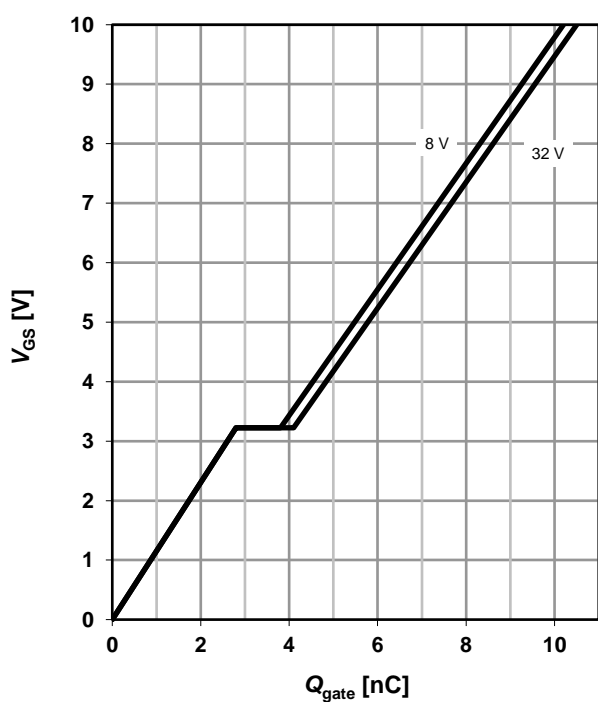
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



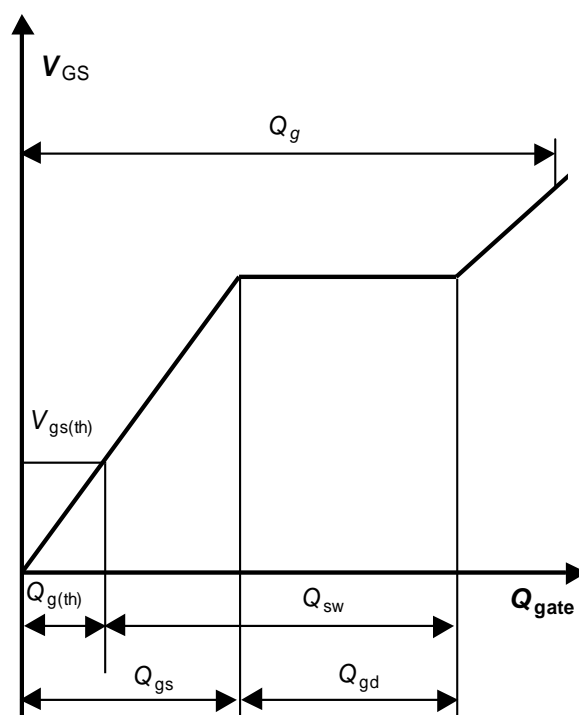
### 15 Typ. gate charge<sup>4)</sup>

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

parameter:  $V_{DD}$



### 16 Gate charge waveforms



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Revision History

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Version	Date	Changes
Revision 1.0	27.05.2019	Final Data Sheet
Revision 1.01	22.08.2024	Package naming updated
Revision 1.02	11.09.2024	Typo correction