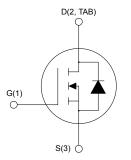


N-channel 650 V, 39 mΩ typ., 54 A MDmesh M9 Power MOSFET in a TO-247 long leads package



TO-247 long leads



AM01475v1_noZe



Product status link

STWA65N045M9

Product summary			
Order code STWA65N045M9			
Marking	65N045M9		
Package	TO-247 long leads		
Packing	Tube		

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STWA65N045M9	650 V	45 mΩ	54 A

- Worldwide best FOM R_{DS(on)}*Q_g among silicon-based devices
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_	Drain current (continuous) at T _C = 25 °C	54	A
I _D	Drain current (continuous) at T _C = 100 °C	34	_ A
I _{DM} ⁽¹⁾	Drain current (pulsed)	170	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	312	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	50	V/ns
di/dt ⁽²⁾	Peak diode recovery current slope	900	A/µs
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	120	V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 150	°C

- 1. Pulse width is limited by safe operating area.
- 2. $I_{SD} \le 28 \, A$, $V_{DS} \, (peak) < V_{(BR)DSS}$, $V_{DD} = 400 \, V$.
- 3. V_{DS} (peak) $< V_{(BR)DSS}$, $V_{DD} = 400 \text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	0.40	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max.)	6	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	775	mJ

DS14231 - Rev 3 page 2/12



2 Electrical characteristics

 T_{C} = 25 °C unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 650 V			1	
I _{DSS}		V _{GS} = 0 V, V _{DS} = 650 V, T _C = 125 °C ⁽¹⁾			200	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.2	3.7	4.2	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 28 A		39	45	mΩ

^{1.} Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 400 V, f = 1 MHz, V _{GS} = 0 V	-	4610	-	pF
C _{oss}	Output capacitance	V _{DS} = 400 V, I = 1 MH12, V _{GS} = 0 V	-	76	-	pF
Coss eq. (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V f = 1 MHz, open drain		885	-	pF
R _G	Intrinsic gate resistance			1	-	Ω
Qg	Total gate charge	V _{DD} = 400 V, I _D = 28 A, V _{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	80	-	nC
Q _{gs}	Gate-source charge		-	26.5	-	nC
Q _{gd}	Gate-drain charge		-	23.5	-	nC

C_{OSS eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 28 A,	-	25	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	-	26	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times	-	77	-	ns
t _f	Fall time	and Figure 18. Switching time waveform)	-	4	-	ns

DS14231 - Rev 3 page 3/12



Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		54	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		170	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 55 A, V _{GS} = 0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 55 A, di/dt = 100 A/µs,	-	288		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 100 V	-	4		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	26		Α
t _{rr}	Reverse recovery time	I _{SD} = 55 A, di/dt = 100 A/μs,	-	400		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 100 V, T _J = 150 °C	-	7.5		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	34		Α

^{1.} Pulse width is limited by safe operating area.

DS14231 - Rev 3 page 4/12

^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.



2.1 Electrical characteristics (curves)

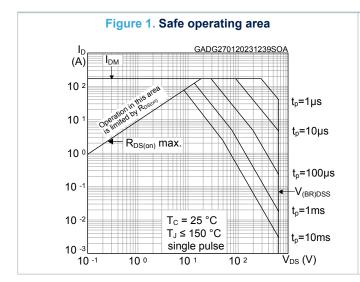
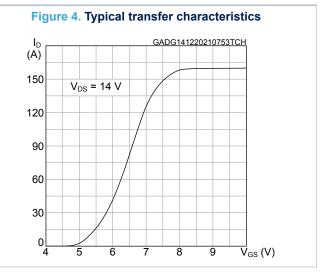
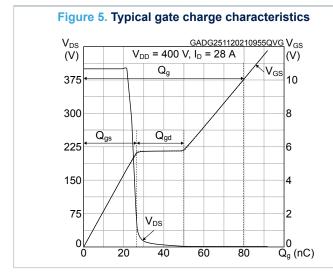
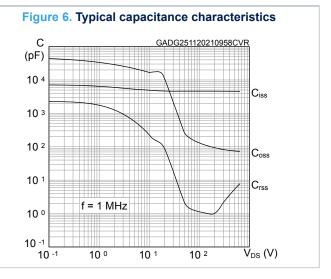


Figure 2. Maximum transient thermal impedance Z_{thJC} (°C/W) GADG270120231130ZTH duty=0.5 10 -1 0.2 0.1 0.05 10 -2 R_{thJC} = 0.40 °C/W $duty = t_{on} / T$ Single pulse 10 -5 10 -4 10 -3 10 -1 $t_p(s)$







DS14231 - Rev 3 page 5/12



Figure 7. Typical drain-source on-resistance

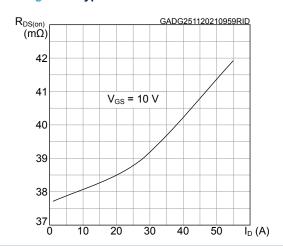


Figure 8. Normalized on-resistance vs temperature

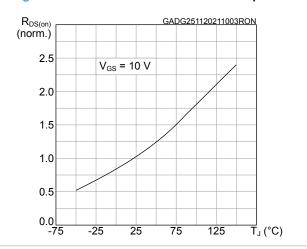


Figure 9. Normalized gate threshold vs temperature

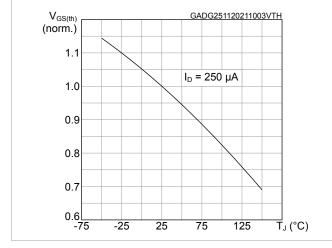


Figure 10. Normalized breakdown voltage vs temperature

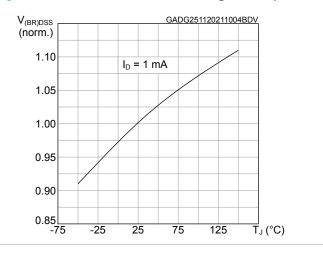


Figure 11. Typical reverse diode forward characteristics

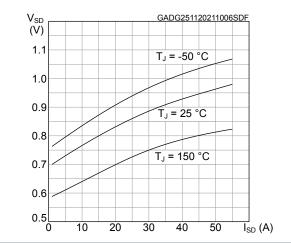
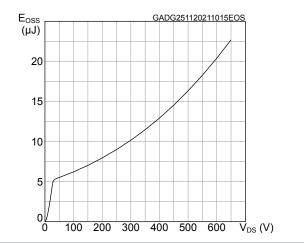


Figure 12. Typical output capacitance stored energy



DS14231 - Rev 3 page 6/12



3 Test circuits

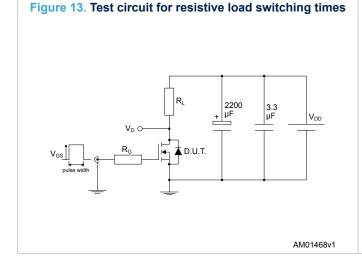


Figure 14. Test circuit for gate charge behavior

V_{GS}

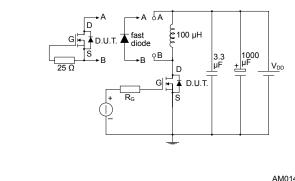
Pulse width

2200

47 kΩ

AM01469v10

Figure 15. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 16. Unclamped inductive load test circuit

Figure 17. Unclamped inductive waveform

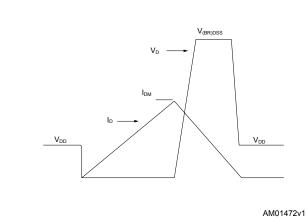
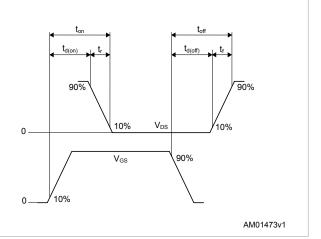


Figure 18. Switching time waveform

AM01471v1



DS14231 - Rev 3 page 7/12

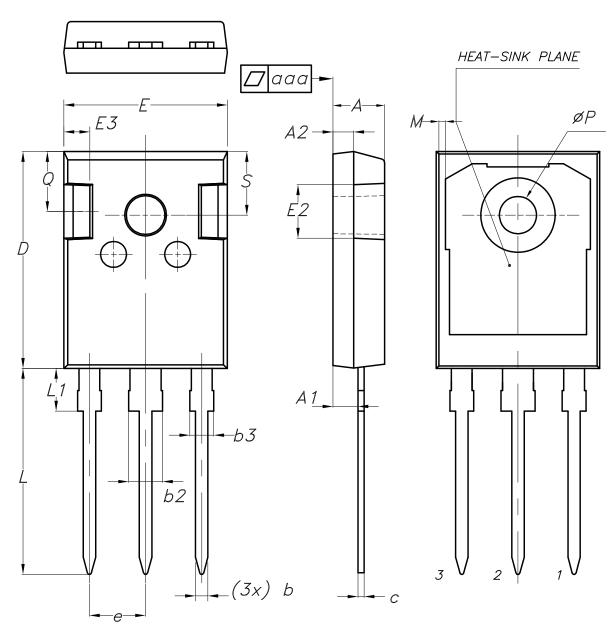


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline



BACK VIEW

8463846_5

DS14231 - Rev 3 page 8/12



Table 8. TO-247 long leads package mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
С	0.59		0.66
D	20.90	21.00	21.10
Е	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
е	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
Р	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

DS14231 - Rev 3 page 9/12



Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Feb-2023	1	First release.
16-Jun-2023	2	Updated Table 6. Switching times. Updated Section 3 Test circuits. Minor text changes.
19-Jul-2024	3	Updated Figure 8. Normalized on-resistance vs temperature and Figure 10. Normalized breakdown voltage vs temperature. Updated Section 4.1: TO-247 long leads package information.

DS14231 - Rev 3 page 10/12





Contents

1	Elec	trical ratings	2
2	Elec	ctrical characteristics	3
	2.1	Electrical characteristics (curves)	5
3	Test	circuits	7
4	Pac	kage information	8
	4.1	TO-247 long leads package information	8
Rev	vision	history	10



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DS14231 - Rev 3 page 12/12