

# MOSFET – N-Channel, POWERTRENCH® 60 V, 22 A, 7.9 mΩ

## FDMC86520L

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Features

- Max  $r_{DS(on)}$  = 7.9 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 13.5 A
- Max  $r_{DS(on)}$  = 11.7 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 11.5 A
- Low Profile – 1 mm Max in Power 33
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant

### Applications

- Primary Switch in Isolated DC-DC
- Synchronous Rectifier
- Load Switch

### MOSFET MAXIMUM RATINGS ( $T_A$ = 25°C unless otherwise noted)

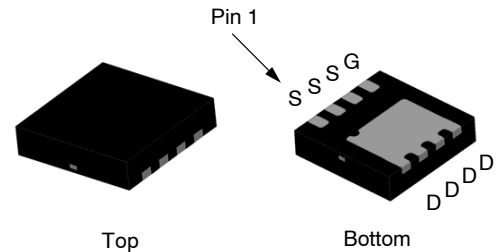
Symbol	Parameter			Rating	Unit
$V_{DS}$	Drain to Source Voltage			60	V
$V_{GS}$	Gate to Source Voltage			±20	V
$I_D$	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	22	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	13.5	
		Pulsed		60	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)			79	mJ
$P_D$	Power Dissipation		$T_C = 25^\circ\text{C}$	40	W
	Power Dissipation (Note 1a)		$T_A = 25^\circ\text{C}$	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range			–55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

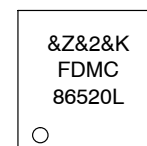
Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
60 V	7.9 mΩ @ 10 V	22 A
	11.7 mΩ @ 4.5 V	



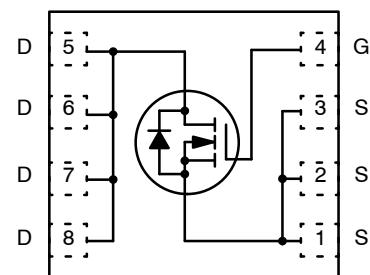
WDFN8 3.3x3.3, 0.65P  
CASE 511DH

### MARKING DIAGRAM



&Z = Assembly Plant Code  
&2 = 2-Digit Date Code (Year and Week)  
&K = 2-Digit Lot Run Code  
FDMC86520L = Specific Device Code

### PIN ASSIGNMENT



P-Channel MOSFET

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDMC86520L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	29	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–7	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.5 A	–	6.5	7.9	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 11.5 A	–	9.1	11.7	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.5 A, T <sub>J</sub> = 125°C	–	9	11	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 13.5 A	–	49	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	3420	4550	pF
C <sub>oss</sub>	Output Capacitance		–	638	850	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	25	40	pF
R <sub>g</sub>	Gate Resistance		–	0.5	–	Ω

### SWITCHING CHARACTERISTICS

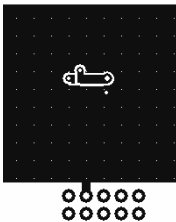
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 13.5 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	15	30	ns
t <sub>r</sub>	Rise Time		–	5.2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	32	55	ns
t <sub>f</sub>	Fall Time		–	3.4	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 30 V, I <sub>D</sub> = 13.5 A	–	45	64	nC
		V <sub>GS</sub> = 0 V to 4.5 V, V <sub>DD</sub> = 30 V, I <sub>D</sub> = 13.5 A	–	21	30	
Q <sub>gs</sub>	Total Gate Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 13.5 A	–	9.6	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	4.9	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

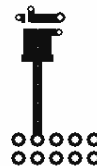
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13.5 A (Note 2)	–	0.82	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A (Note 2)	–	0.71	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 13.5 A, di/dt = 100 A/μs	–	38	62	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 53°C/W when mounted on  
a 1 in<sup>2</sup> pad of 2 oz copper



b. 125°C/W when mounted on  
a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T<sub>J</sub> = 25°C; N-ch: L = 0.3 mH, I<sub>AS</sub> = 23 A, V<sub>DD</sub> = 54 V, V<sub>GS</sub> = 10 V.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

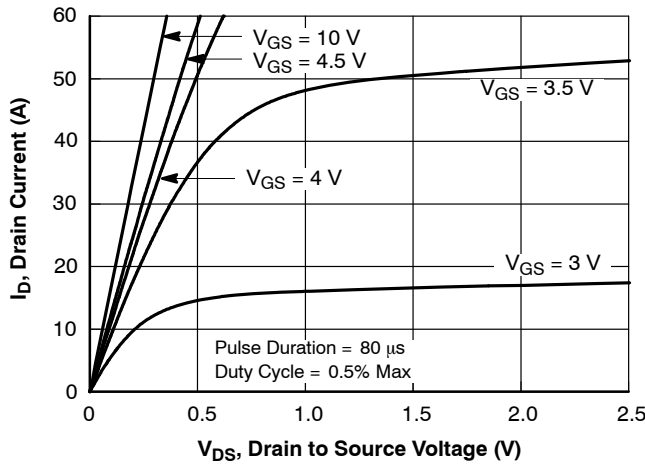


Figure 1. On Region Characteristics

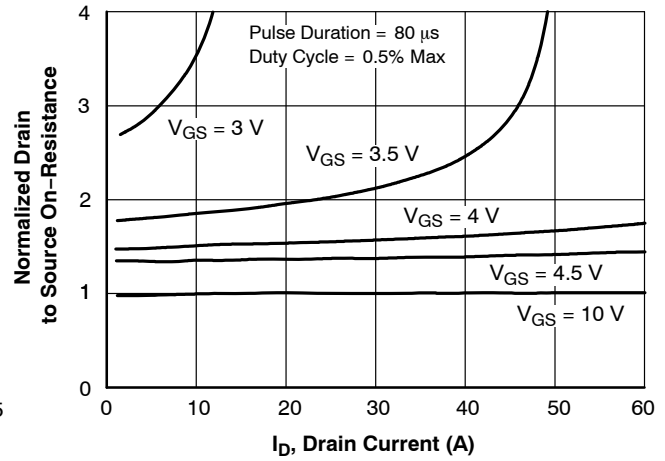


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

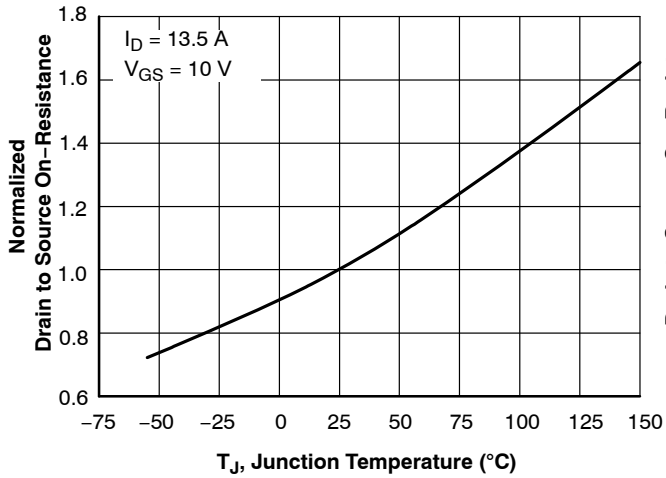


Figure 3. Normalized On Resistance vs. Junction Temperature

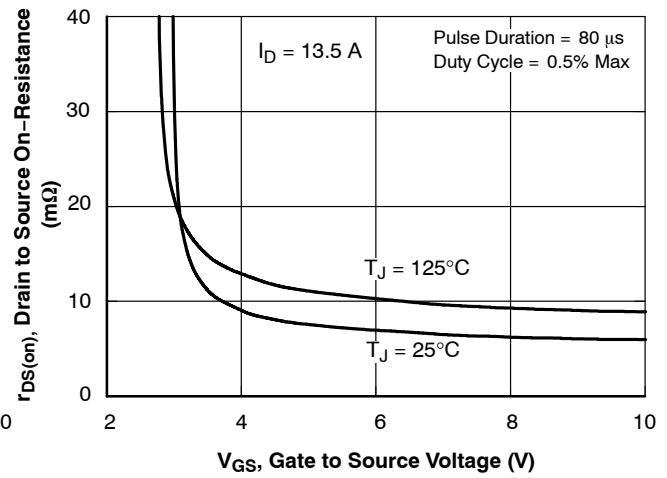


Figure 4. On-Resistance vs. Gate to Source Voltage

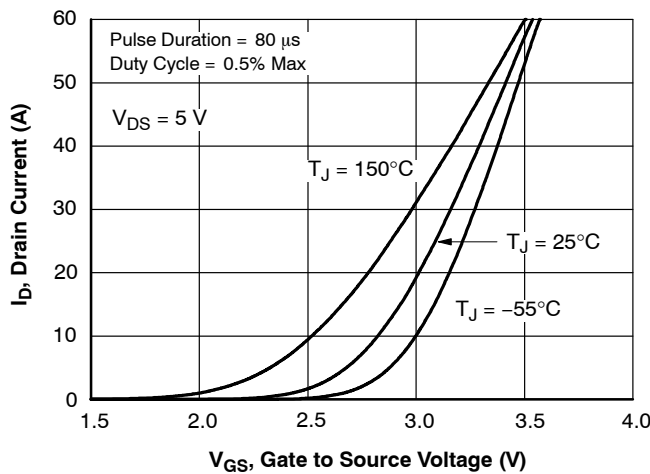


Figure 5. Transfer Characteristics

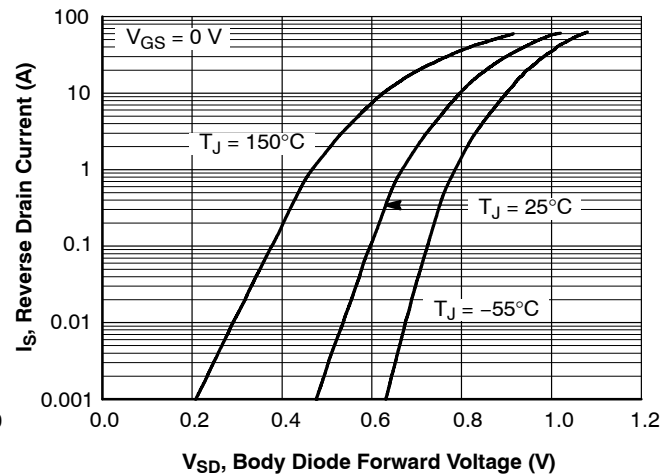


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

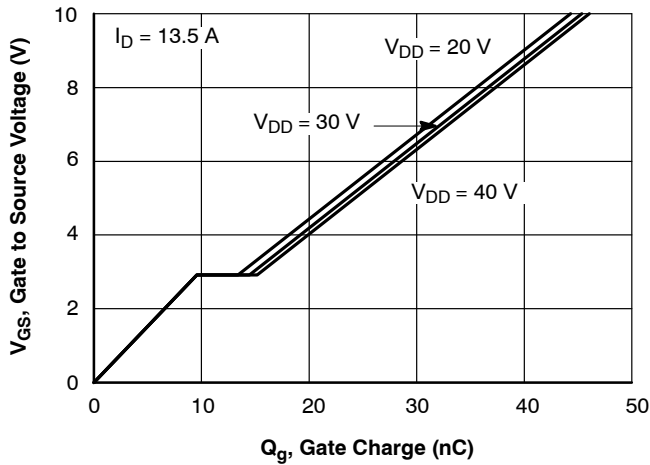


Figure 7. Gate Charge Characteristics

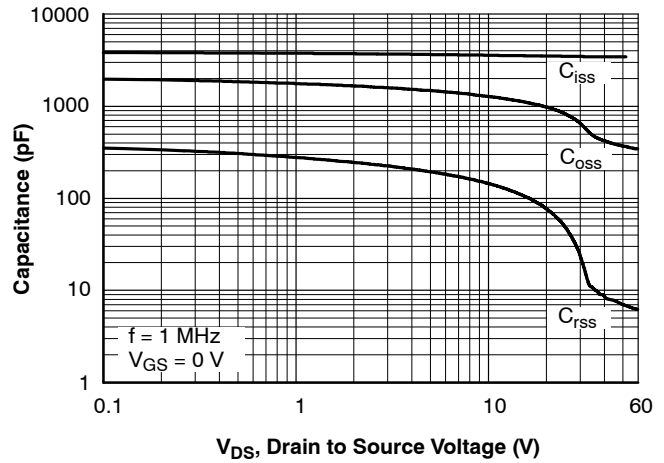


Figure 8. Capacitance vs. Drain to Source Voltage

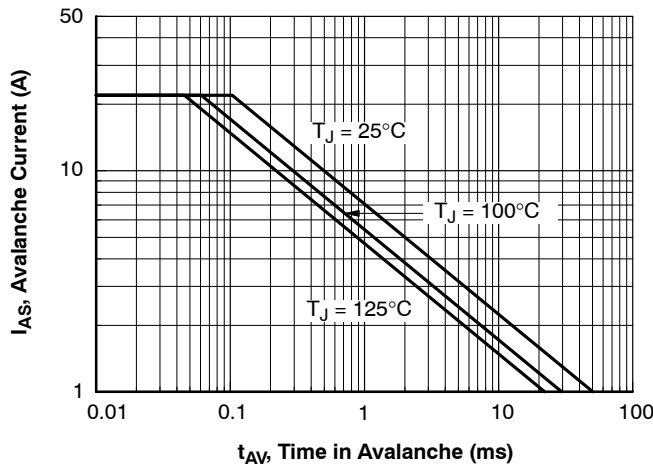


Figure 9. Unclamped Inductive Switching Capability

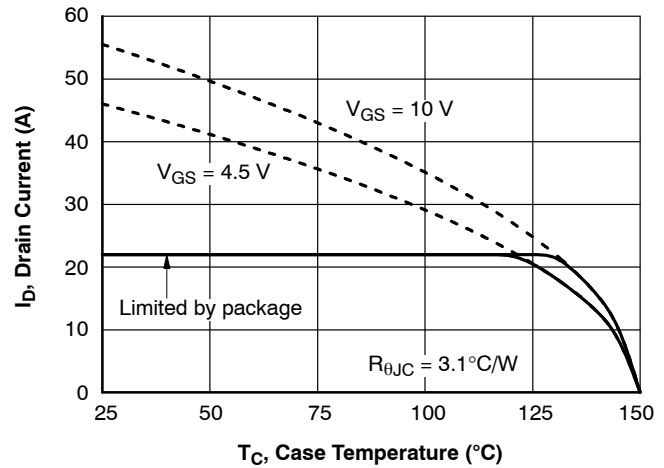


Figure 10. Maximum Continuous Drain Current vs Case Temperature

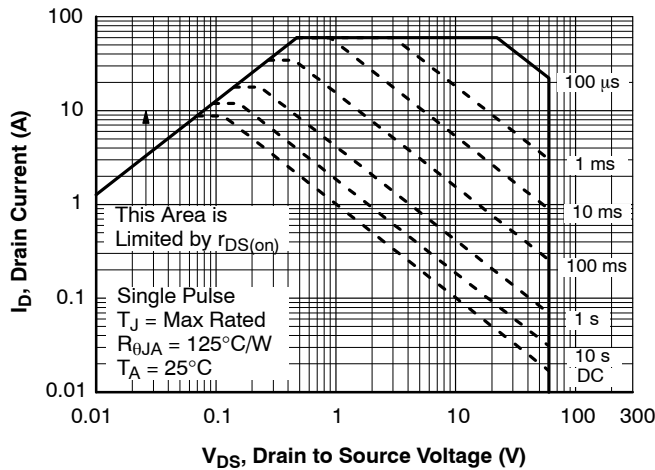


Figure 11. Forward Bias Safe Operating Area

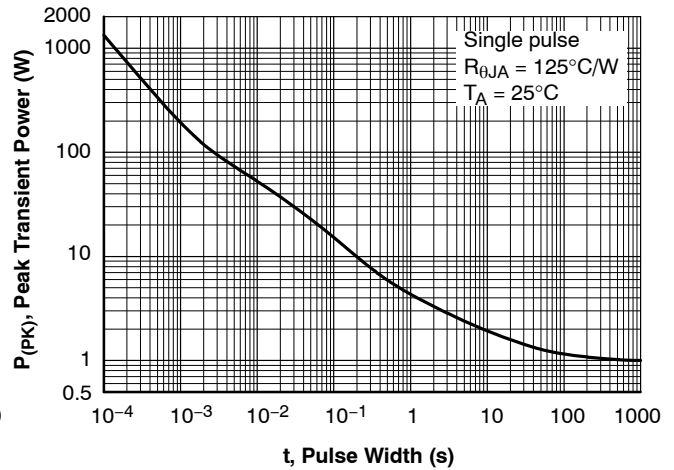


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

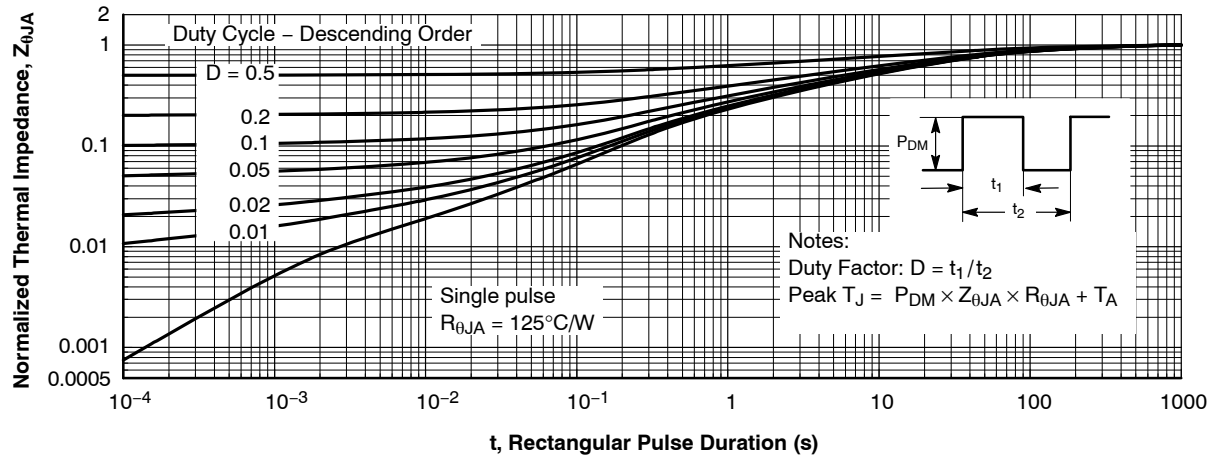


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

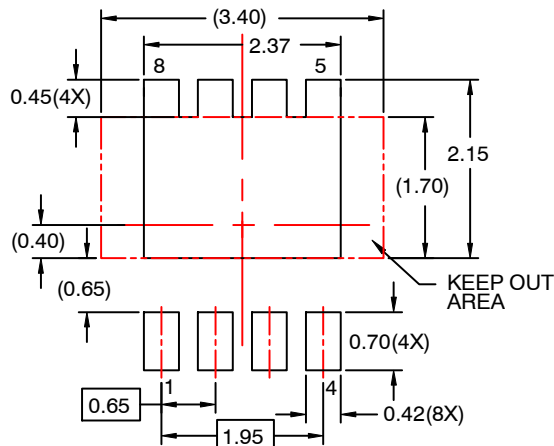
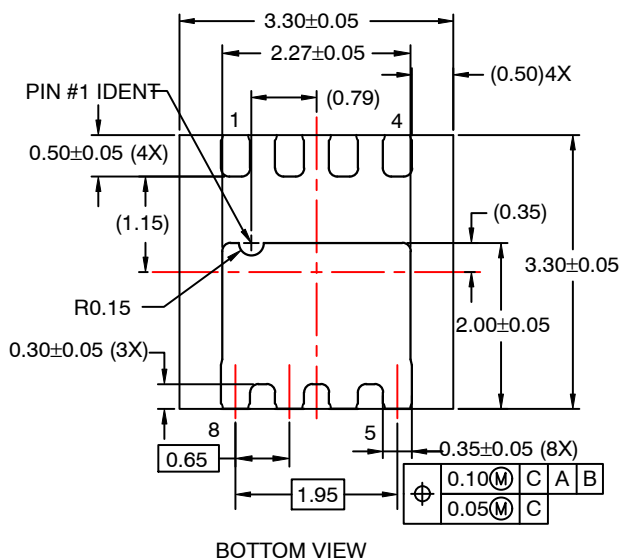
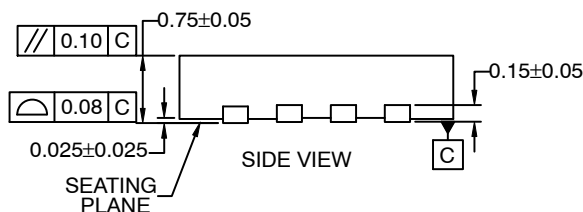
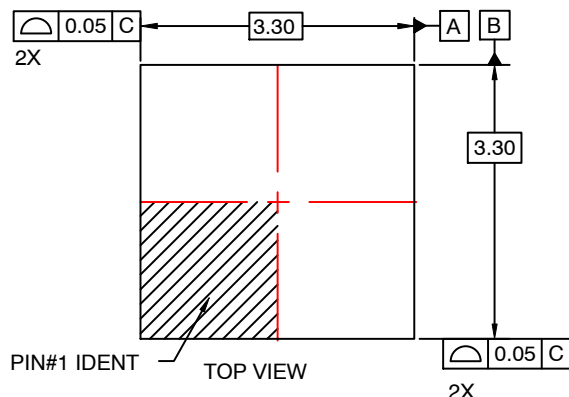
ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMC86520L	FDMC86520L	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**WDFN8 3.3x3.3, 0.65P**  
**CASE 511DH**  
**ISSUE O**

DATE 31 JUL 2016



**RECOMMENDED LAND PATTERN**

**NOTES:**

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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