# OptiMOS™ 5 Power MOS Transistor Chip

## IPC331N15NM5R

| Type | $V_{(BR)DSS}$ | $R_{DS(on)}$ | Die size | Die-thickness |
|---|---|---|---|---|
| IPC331N15NM5R | 150 V | 2.9 mΩ | 7.05 x 4.7 mm$^2$ | 193 µm |

## Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPP051N15N5[1)]
- Electrostatic Discharge Sensitive Device according to JEDEC
- Die bond: soft solder recommended
- Wire bond: Al wedge recommended
- Backside metallization: NiAg system
- Frontside metallization: AlCu system
- Passivation: imide

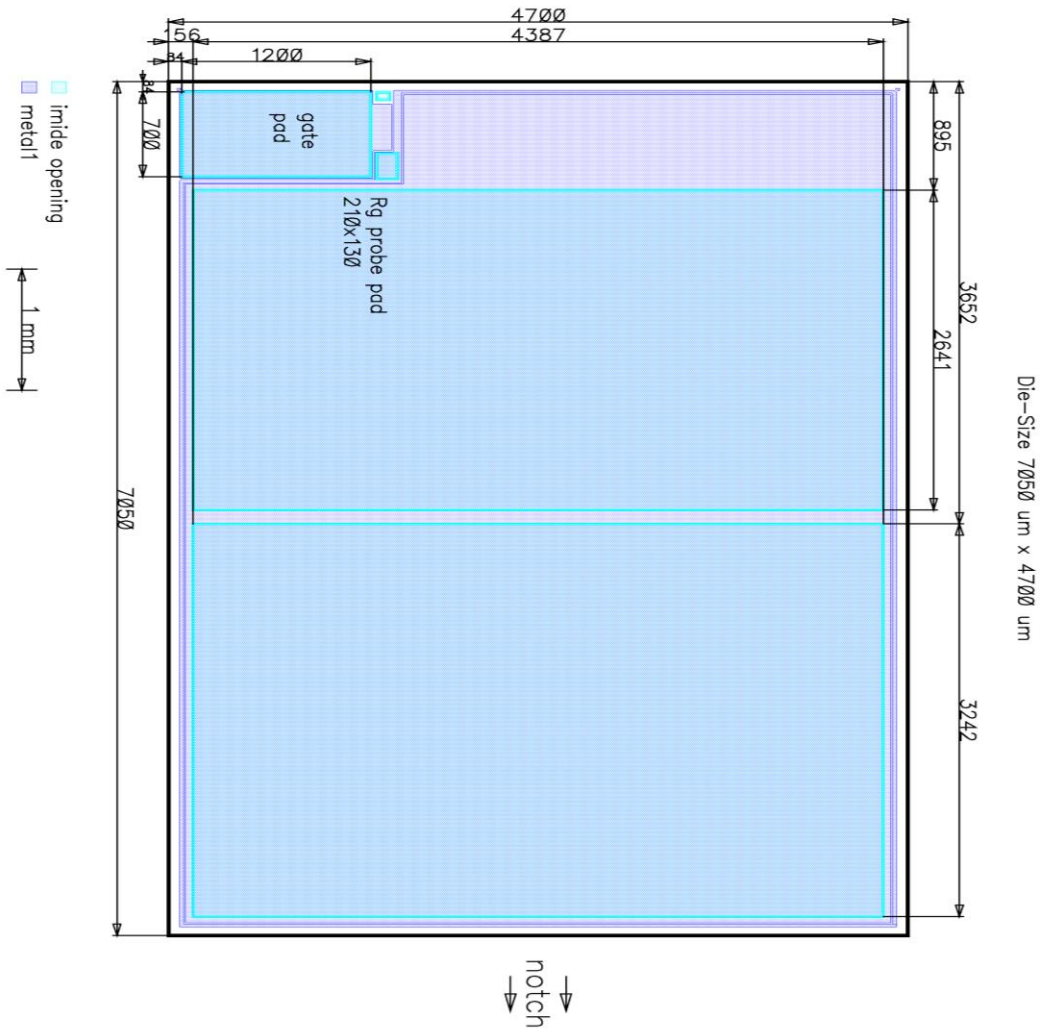
## 1 Electrical Characteristics on Wafer Level

at $T_j$ = 25 °C, unless otherwise specified.

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 150 | - | - | V | $V_{GS}$ = 0 V<br>$I_D$ = 1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 3.0 | 3.8 | 4.6 | V | $V_{DS}$ = $V_{GS}$<br>$I_D$ = 290 µA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 0.1 | 1 | µA | $V_{GS}$ = 0 V<br>$V_{DS}$ = 120 V |
| Gate-source leakage current | $I_{GSS}$ | - | 1 | 100 | nA | $V_{GS}$ = 20 V<br>$V_{DS}$ = 0 V |
| Drain-source on-resistance | $R_{DS(on)}$ | - | 2.9[2)] | 100[3)] | mΩ | $V_{GS}$ = 10 V<br>$I_D$ = 2 A |
| Gate resistance | $R_G$ | 5.5 | 14 | 22.5 | Ω | - |
| Reverse diode forward on-voltage | $V_{SD}$ | - | 0.65 | 0.9 | V | $V_{GS}$ = 0 V<br>$I_F$ = 1 A |
| Avalanche energy, single pulse | $E_{AS}$ | - | 70[4)] | - | mJ | $I_D$ = 38 A, $R_{GS}$ = 25 Ω |

[1)] IPP051N15N5 dynamic characterization does not include the internal added $R_G$
[2)] typical bare die $R_{DS(on)}$; $V_{GS}$ = 10 V
[3)] limited by wafer test-equipment
[4)] Wafer tested.

# 2 Chip Layout



# Revision History

## Major changes since the last revision

| Page or Reference | Description of change |
|---|---|
| 2.0 | Update from preliminary to final version |
| 2.1 | Update in description. Die bond: soft solder recommended |
| 2.2 | Update die thickness |
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