

CoolMOS™ CFD7A

650V CoolMOS™ CFD7A SJ Power Device

650V CoolMOS™ CFD7A is Infineon's latest generation of market leading automotive qualified high voltage CoolMOS™ MOSFETs. In addition to the well-known attributes of high quality and reliability required by the automotive industry, the new CoolMOS™ CFD7A series provides for an integrated fast body diode and can be used for PFC and resonant switching topologies like the ZVS phase-shift full-bridge and LLC.

Features

- Latest 650V automotive qualified technology with integrated fast body diode on the market featuring ultra low Q_{rr}
- Lowest FOM $R_{DS(on)} \cdot Q_g$ and $R_{DS(on)} \cdot E_{oss}$
- 100% avalanche tested
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Optimized for higher battery voltages up to 475 V thanks to further improved robustness
- Lower switching losses enabling higher switching frequencies
- High quality and reliability
- Increased efficiency in light load and full load conditions

Potential applications

Suitable for PFC and DC-DC stages for:

- Unidirectional and bidirectional DC-DC converters,
- On-Board battery Chargers

Product validation

Qualified according to AEC Q101

Please note: For production part approval process (PPAP) release we propose to share application related information during an early design phase to avoid delays in PPAP release. Please contact Infineon sales office. The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.

PG-TO247-4

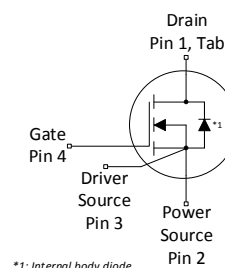
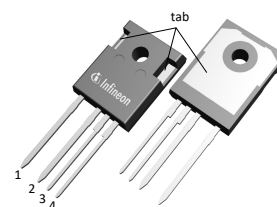


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
$R_{DS(on),max}$	35	mΩ
$Q_{g,typ}$	145	nC
$I_{D,pulse}$	304	A
$E_{oss} @ 400V$	18.4	μJ
Body diode di_F/dt	1300	A/μs

Type/Ordering Code	Package	Marking	Related Links
IPZA65R035CFD7A	PG-TO247-4	65A035F7	see Appendix A



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	63	A	$T_C = 25^\circ\text{C}$
Continuous drain current	I_D	-	-	40	A	$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	304	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	358	mJ	$I_D = 7.3\text{A}$; $V_{DD} = 50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	7.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS,pulse}$	-30	-	30	V	$f_{repetition} \leq 100\text{kHz}$, $t_{pulse} \leq 2\text{ns}$
Power dissipation	P_{tot}	-	-	305	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	63	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	304	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 35.8\text{A}$, $T_j = 25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 35.8\text{A}$, $T_j = 25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.41	°C/W	-
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage ⁴⁾	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage ⁵⁾	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=1.79mA$
Zero gate voltage drain current	I_{DSS}	-	- 160	1 -	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=650V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	0.1	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.029 0.064	0.035 -	Ω	$V_{GS}=10V, I_D=35.8A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=35.8A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	3.8	-	Ω	$f=250kHz$, open drain

⁴⁾ For applications with applied blocking voltage > 475 V of the specified blocking voltage, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support by Infineon.

⁵⁾ We do not recommend using the CoolMOS mentioned in this datasheet to operate in "linear mode". For assessment of potential "linear mode", please contact Infineon sales office.

Table 5 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	7149	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	C_{oss}	-	95	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related ⁶⁾	$C_{o(er)}$	-	230	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ⁷⁾	$C_{o(tr)}$	-	2430	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	30	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega$; see table 9
Rise time	t_r	-	9.2	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	131	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega$; see table 9
Fall time	t_f	-	2.7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega$; see table 9

6) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

7) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	41	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	44	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	145	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.1	-	V	$V_{GS}=0V, I_F=35.8A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	208	-	ns	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	1.60	-	μC	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	13.1	-	A	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

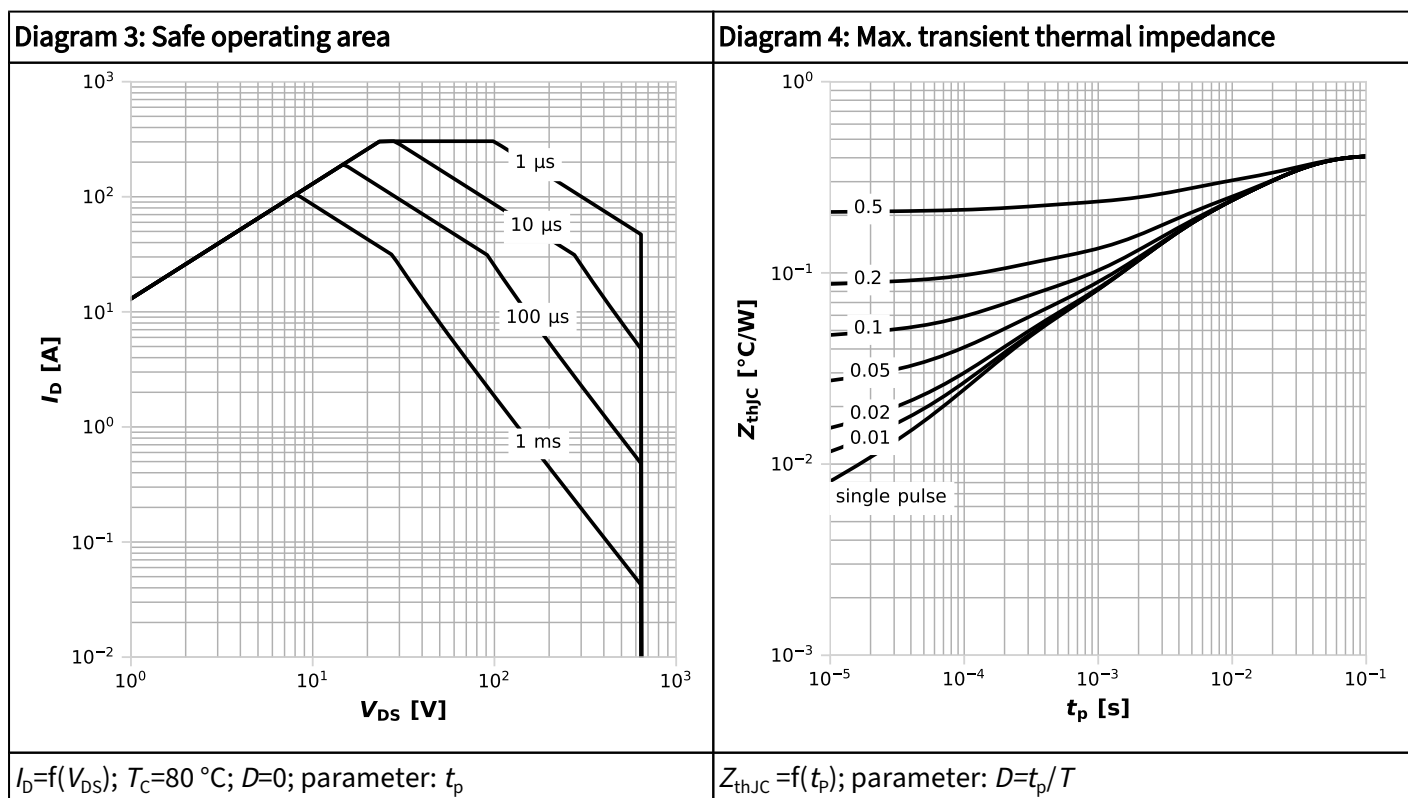
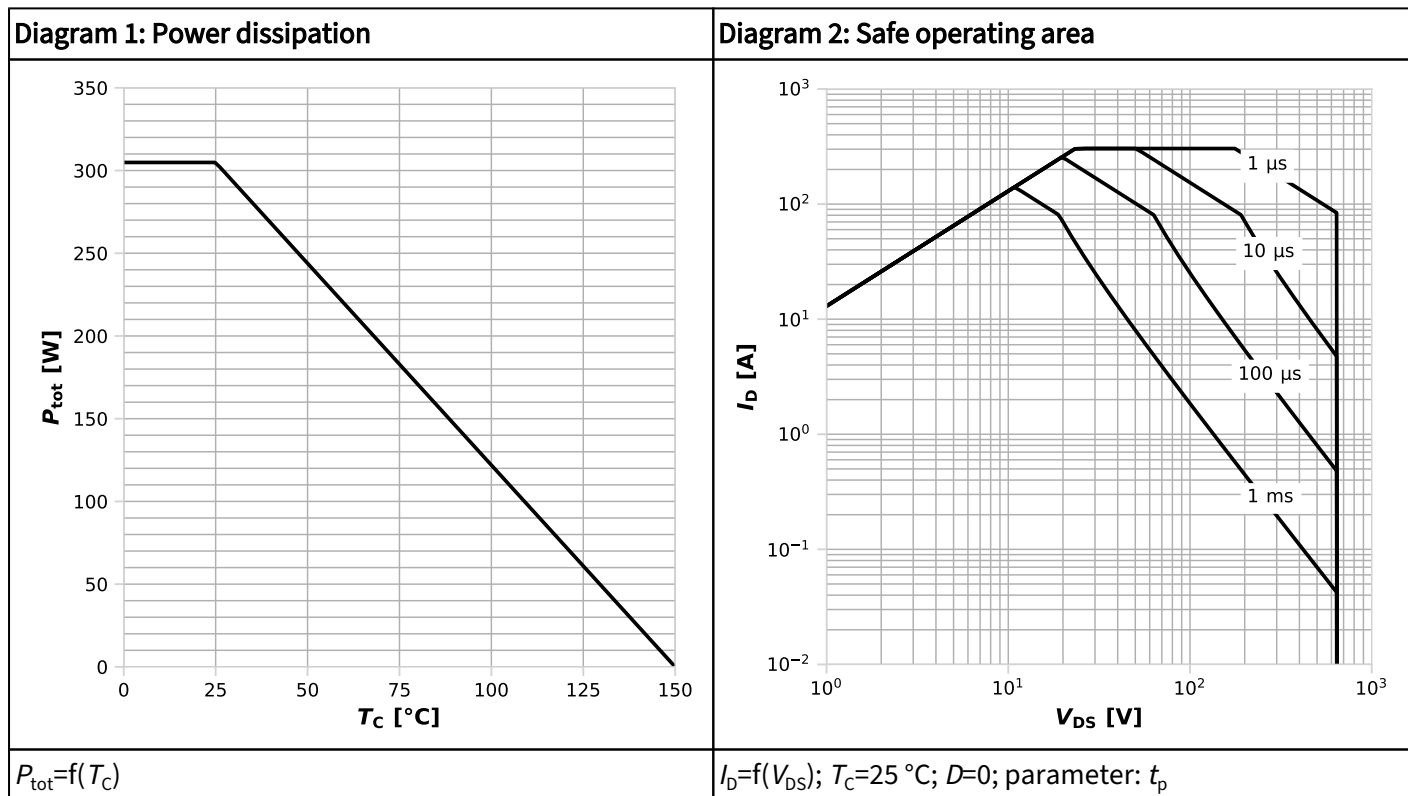
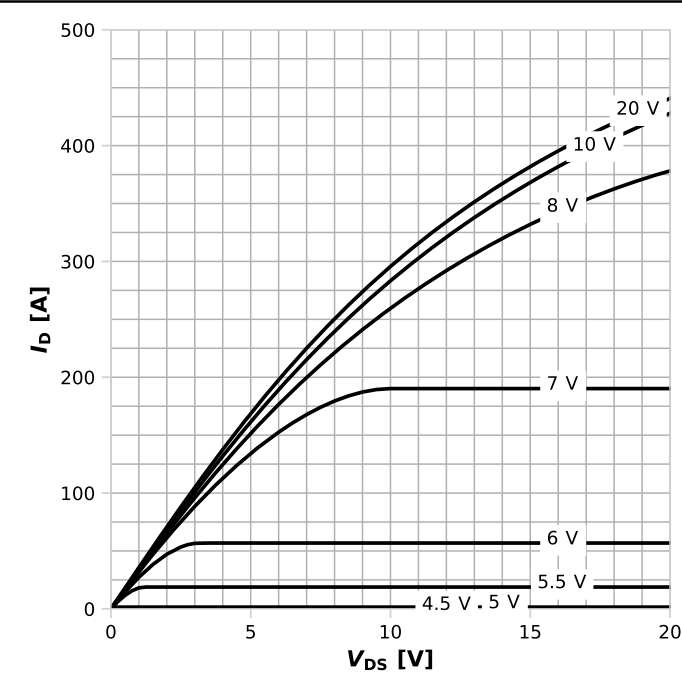
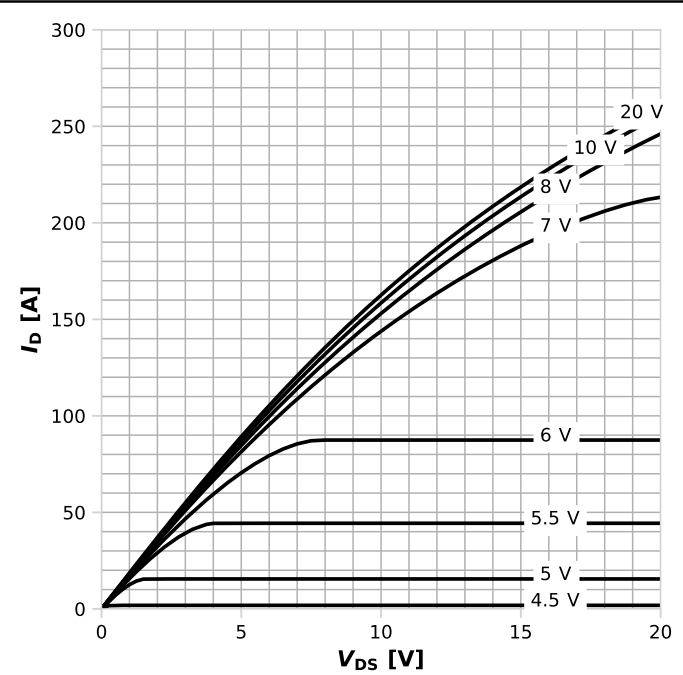


Diagram 5: Typ. output characteristics



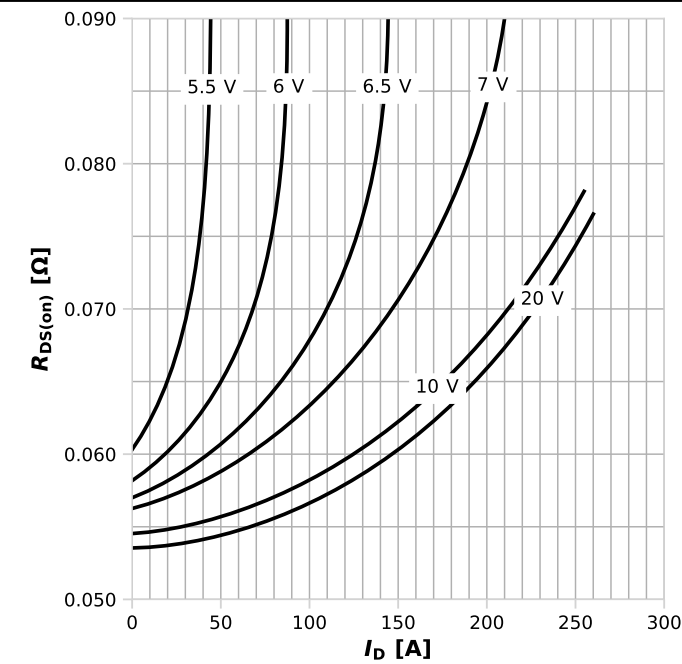
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



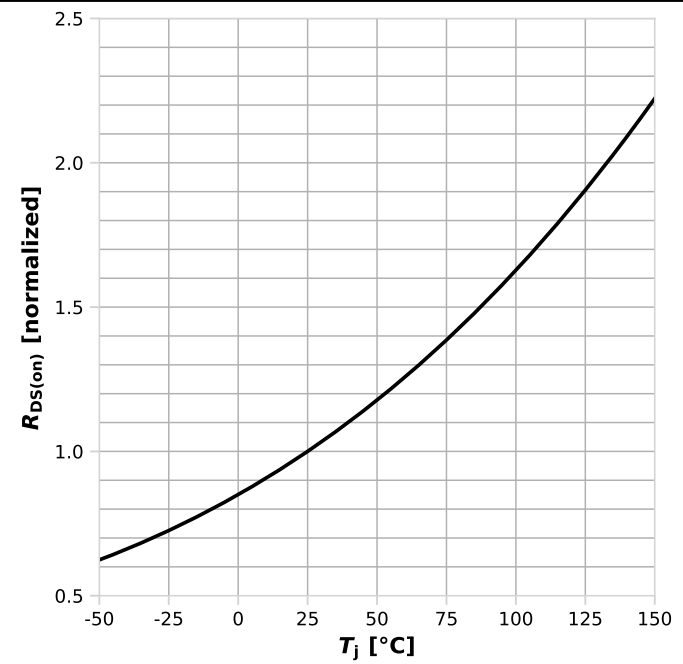
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)} = f(T_j)$; $I_D = 35.8\text{ A}$; $V_{GS} = 10\text{ V}$

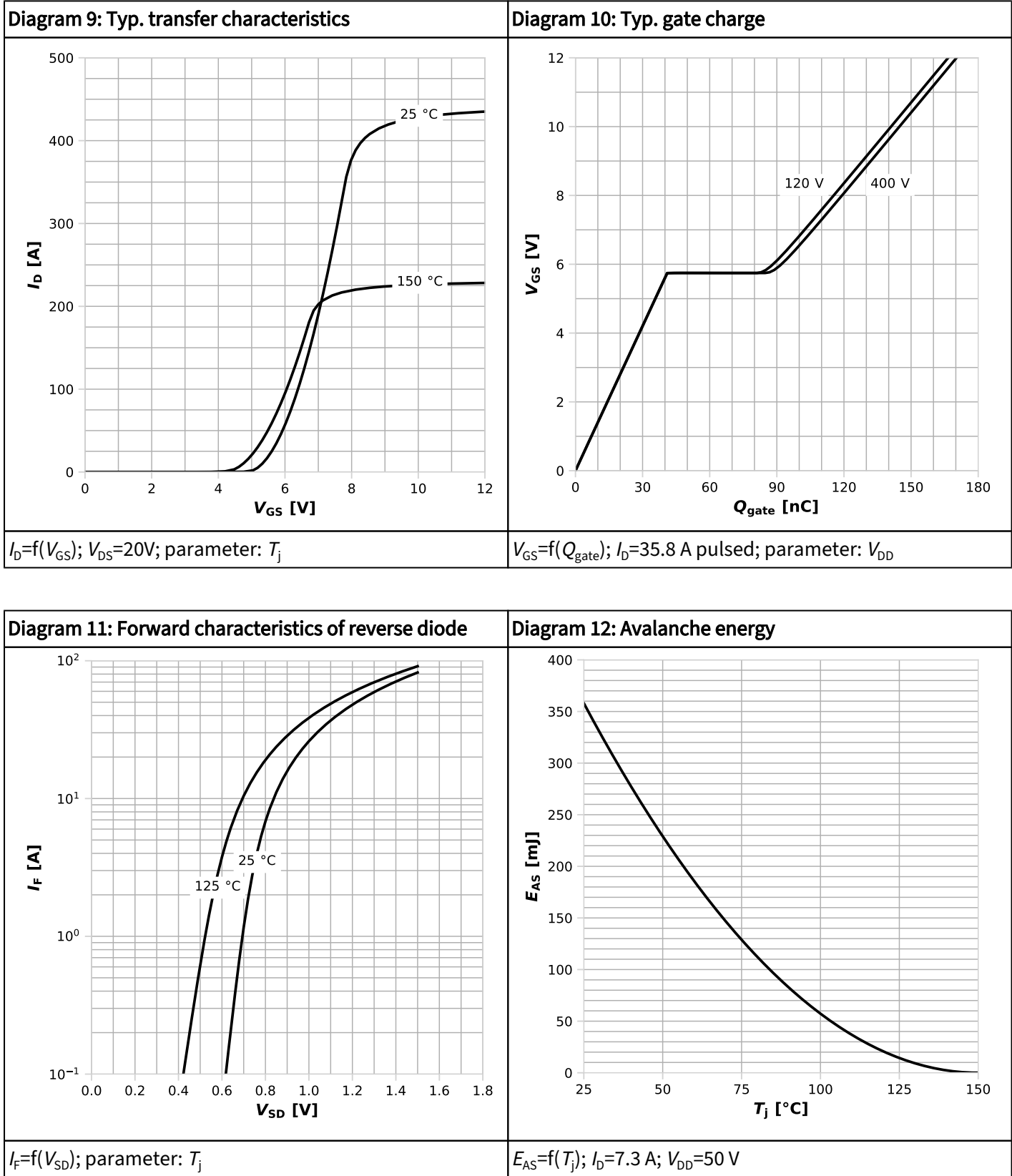
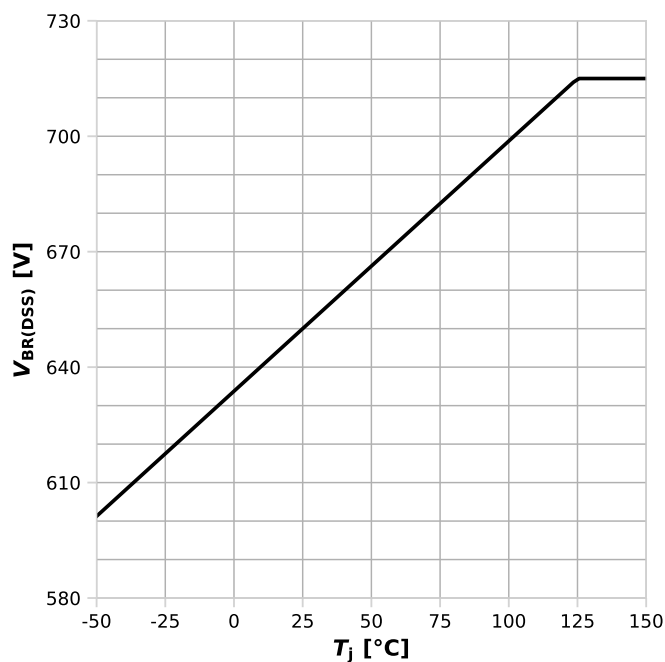
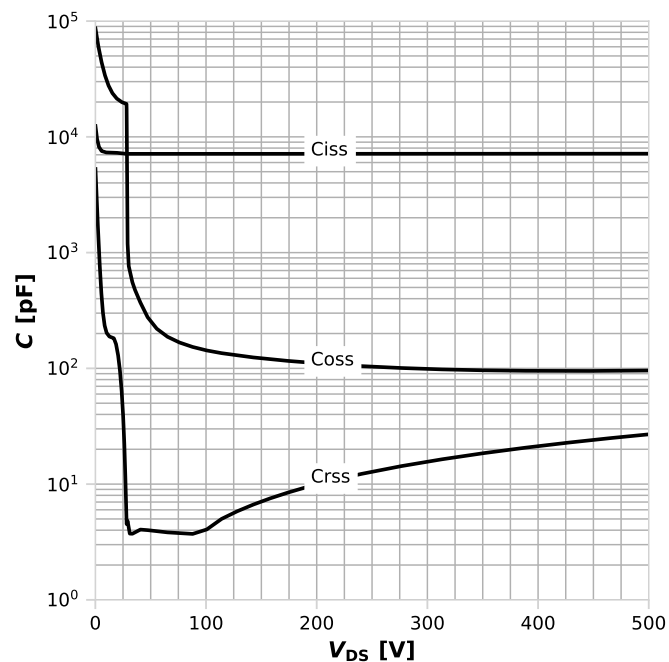


Diagram 13: Drain-source breakdown voltage



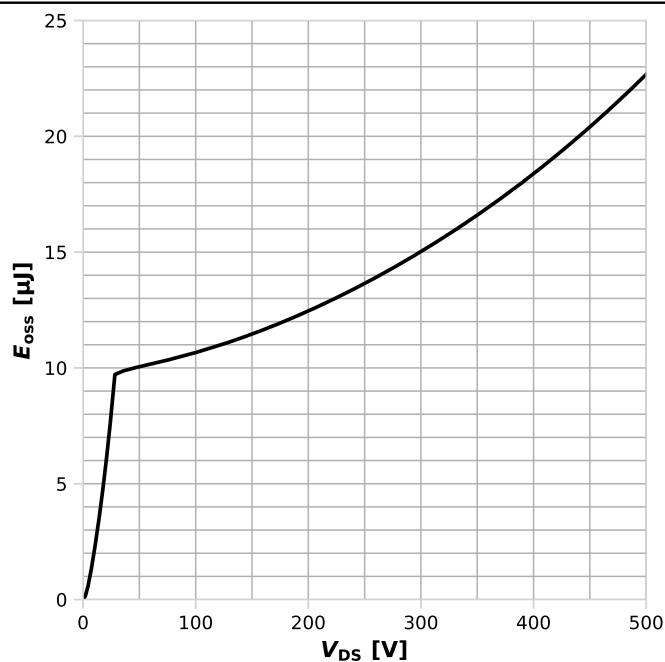
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



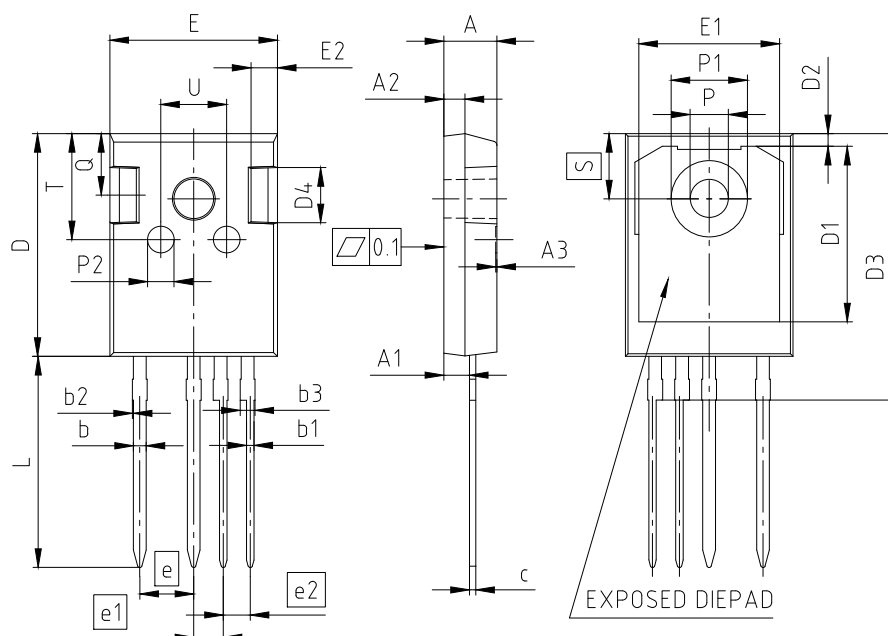
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Package Outlines


NOTES:

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER: PG-T0247-4-U02					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	E	15.70	15.90
A1	2.31	2.51	E1	13.10	13.50
A2	1.90	2.10	E2	2.40	2.60
A3	0.05	0.25	e	5.08	
b	1.10	1.30	e1	2.79	
b1	0.65	0.79	e2	2.54	
b2	---	0.20	N	4	
b3	1.34	1.44	L	19.80	20.10
c	0.58	0.66	øP	3.50	3.70
D	20.90	21.10	øP1	7.00	7.40
D1	16.25	16.85	øP2	2.40	2.60
D2	1.05	1.35	Q	5.60	6.00
D3	24.97	25.27	S	6.15	
D4	4.90	5.10	T	9.80	10.20
			U	6.00	6.40

Figure 1 Outline PG-T0247-4, dimensions in mm

7 Appendix A

Table 11 **Related Links**

- [IFX CoolMOS CFD7A Webpage](#)
- [IFX CoolMOS CFD7A application note](#)
- [IFX CoolMOS CFD7A simulation model](#)
- [IFX Design tools](#)

Revision History

IPZA65R035CFD7A

Revision 2024-04-29, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-04-29	Release of final

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