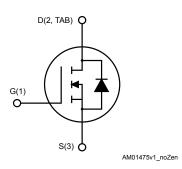


N-channel 100 V, 30 mΩ typ., 25 A, STripFET™ II Power MOSFET in a DPAK package

Features





Туре	V _{DS}	R _{DS(on)} max.	l _D
STD25NF10LT4	100 V	35 mΩ	25 A

- Exceptional dv/dt capability
- 100% avalanche tested
- · Low gate charge

Applications

· Switching applications

Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link			
STD25NF10LT4			
Product	summary		
Order code	STD25NF10LT4		
Marking D25NF10L			

Package Packing DPAK

Tape and reel



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{DGR}	Gate-source voltage (R _{GS} = 20 k Ω)	100	V
V _{GS}	Gate-source voltage	±16	V
1_	Drain current (continuous) at T _C = 25 °C	25	А
I _D	Drain current (continuous) at T _C = 100 °C	21	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	100	Α
P _{TOT}	Total dissipation at T _C = 25 °C	100	W
E _{AS} ⁽²⁾	Single-pulse avalanche energy	450	mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	20	V/ns
T _{stg}	Storage temperature range	55 to 175	°C
T _j	Operating junction temperature range	-55 to 175	

- 1. Pulse width limited by safe operating area.
- 2. Starting T_J = 25 °C, I_D = 12.5 A, V_{DD} = 50 V
- 3. $I_{SD} \le 25~A,~di/dt \le 300~A/\mu s,~V_{DS} \le V_{(BR)DSS},~T_J \le T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	1.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50	°C/W

1. When mounted on an FR-4 board of 1 inch², 2 oz Cu.

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2 Electrical characteristics

 T_{CASE} = 25 °C unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
		V _{GS} = 0 V, V _{DS} = 100 V			1	μA
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 100 \text{ V},$ $T_{C} = 125 ^{\circ}\text{C}^{(1)}$			10	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±16 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DD} = V_{GS}, I_D = 250 \mu A$	1		2.5	V
Proc	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 12.5 A		30	35	mΩ
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 4.5 V, I _D = 12.5 A		35	40	mΩ

^{1.} Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz,	-	1710		pF
C _{oss}	Output capacitance	$V_{DS} = 25 \text{ V}, 1 - 1 \text{ Wiriz},$ $V_{CS} = 0 \text{ V}$	-	250		pF
C _{rss}	Reverse transfer capacitance	VGS 0 V	-	110		pF
Qg	Total gate charge	$V_{DD} = 80 \text{ V}, I_D = 25 \text{ A},$	-	38	52	nC
Q_{gs}	Gate-source charge	V _{GS} = 0 to 5 V	-	8.5		nC
Q _{gd}	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	21		nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 12.5 A,	-	20	-	ns
t _r	Rise time	$R_G = 4.7 \Omega, V_{GS} = 5 V$	-	40	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and	-	58	-	ns
t _f	Fall time	Figure 17. Switching time waveform)	-	20	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		25	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		100	Α

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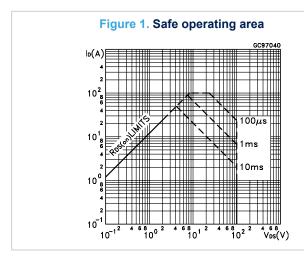
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 25 A, V _{GS} = 0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 25 A, di/dt = 100 A/μs,	-	88		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 50 V, T _J = 150 °C	-	317		nC
I _{RRM}	Reverse recovery current	(see Figure 17. Switching time waveform)	-	7.2		Α

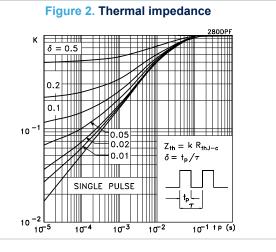
- 1. Pulse width limited by safe operating area
- 2. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

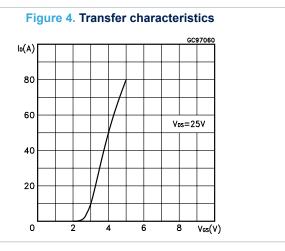
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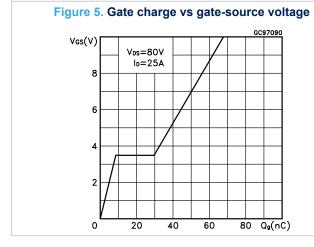


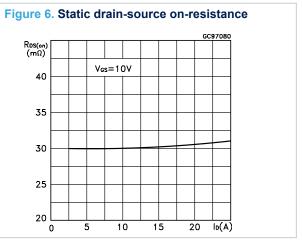
2.1 Electrical characteristics (curves)











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Figure 7. Capacitance variations

C(pF)

Ciss

Coss

C

Ves(th)
(norm)

1.3

Vos=Ves
ID=250µA

1.1

0.9

0.7

0.5

-50

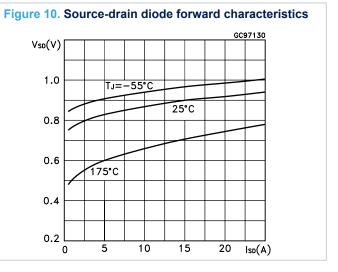
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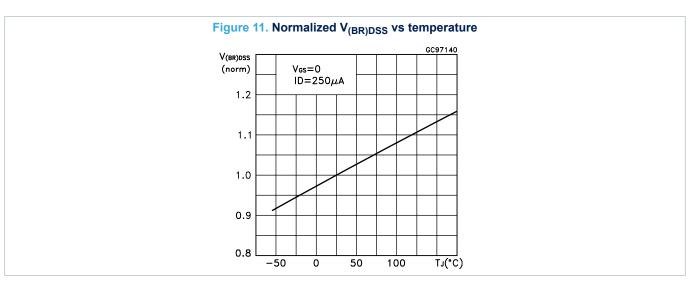
50

100

TJ(*C)

Figure 9. Normalized on-resistance vs temperature GC97120 Ros(on) Vgs=10V (norm) lo=12.5A 2.0 1.5 1.0 0.5 0.0 -50 0 50 100 TJ(°C)





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3 Test circuits

Figure 12. Test circuit for resistive load switching times

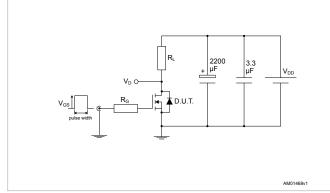


Figure 13. Test circuit for gate charge behavior

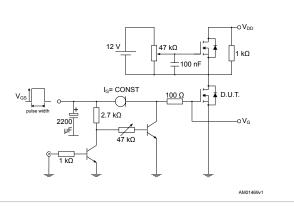


Figure 14. Test circuit for inductive load switching and diode recovery times

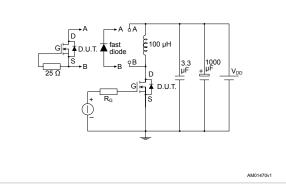


Figure 15. Unclamped inductive load test circuit

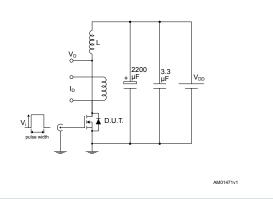


Figure 16. Unclamped inductive waveform

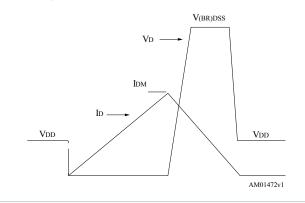
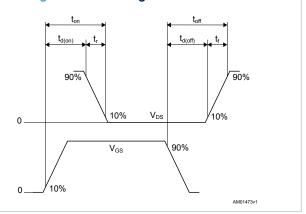


Figure 17. Switching time waveform



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4 Package information

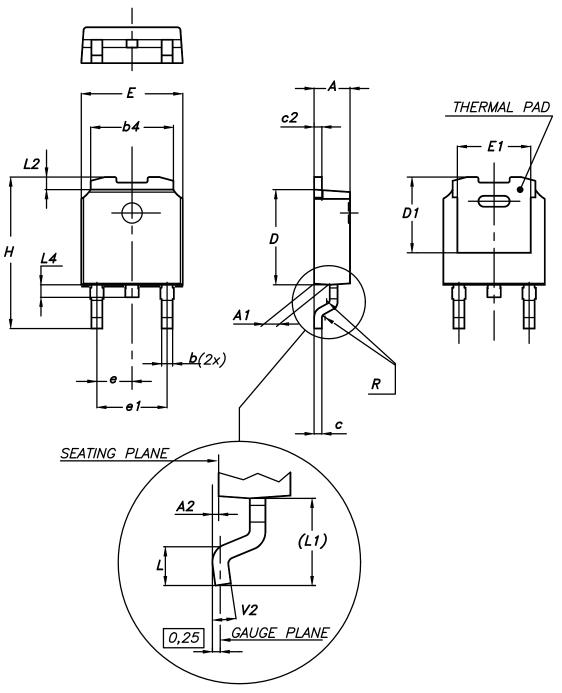
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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4.1 DPAK (TO-252) type A package information

Figure 18. DPAK (TO-252) type A package outline



0068772_A_25

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Table 7. DPAK (TO-252) type A mechanical data

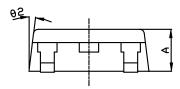
Dim.		mm	
Dilli.	Min.	Тур.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

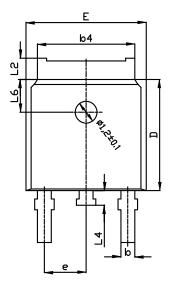
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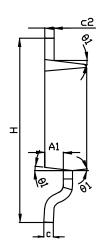


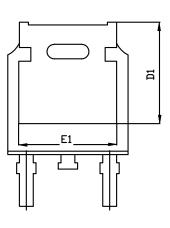
4.2 DPAK (TO-252) type C2 package information

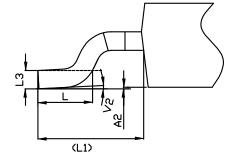
Figure 19. DPAK (TO-252) type C2 package outline











0068772_C2_25

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Table 8. DPAK (TO-252) type C2 mechanical data

Dim.		mm	
Dim.	Min.	Тур.	Max.
Α	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
С	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
Е	6.50	6.60	6.70
E1	5.20		5.50
е	2.186	2.286	2.386
Н	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

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6.3 = = = = 11.2

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)

1.5

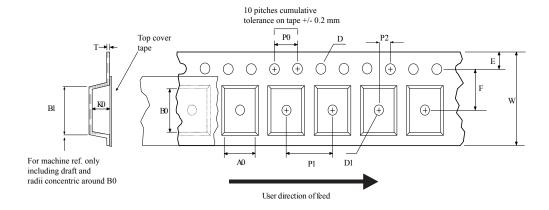
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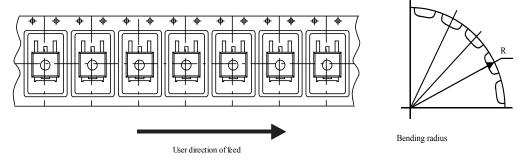
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4.3 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



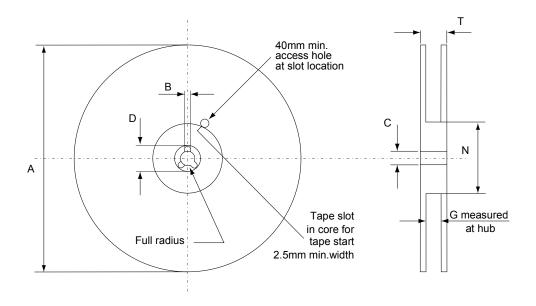


AM08852v1

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Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	n	nm	Dim.	,	nm
Dilli.	Min.	Max.	Diiii.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	e qty.	2500
P1	7.9	8.1	Bul	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

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Revision history

Table 10. Document revision history

Date	Version	Changes
21-Jun-2004	3	Preliminary version
03-Jun-2006	4	New template, no content change
		Updated information on cover page.
09-Aug-2018	5	Updated Section 4 Package information.
		Minor text changes

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