MOSFET

OptiMOS™ 5 Power-Transistor, 80 V

PG-TSDSON-8 FL

Features

• Ideal for high frequency switching and sync. rec.
• Optimized technology for DC/DC converters
• Excellent gate charge x $R_{DS(on)}$ product (FOM)
• Very low on-resistance $R_{DS(on)}$
• N-channel, normal level
• 100% avalanche tested
• Pb-free plating; RoHS compliant
• Qualified according to JEDEC[1) for target applications
• Halogen-free according to IEC61249-2-21
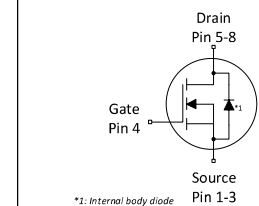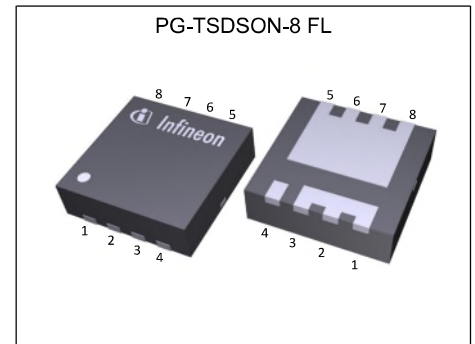• Higher solder joint reliability with enlarged source interconnection

Drain
Pin 5-8

Gate
Pin 4

Source
Pin 1-3

*1: Internal body diode

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	8.4	mΩ
I_D	64	A
Q_{oss}	25	nC
$Q_G(0V..10V)$	20	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ084N08NS5	PG-TSDSON-8 FL	084N08N	-

[1) J-STD20 and JESD22

Table of Contents

1　Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2　Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	64 41	A	T_C=25 °C T_C=100 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	256	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	76	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	63	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2　Thermal characteristics

Table 3　Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.2	2	K/W	-
Device on PCB, 6 cm² cooling area[4]	R_{thJA}	-	-	60	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=31 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.1 9.9	8.4 11.9	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=6 V, I_D=5 A
Gate resistance	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	20	39	-	S	$|V_{DS}|$>2$|I_D|R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	1400	1820	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	240	312	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	13	22.8	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	5	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	5	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6.5	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	4.4	7	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	7.1	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	20	25	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	17	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	25	33	nC	V_{DD}=40 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See ″Gate charge waveforms″ for parameter definition.

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	46	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	256	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.86	1.2	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	38	76	ns	V_R=40 V, I_F=20 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	44	88	nC	V_R=40 V, I_F=20 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot} [W] vs T_C [°C]

$P_{tot}=f(T_C)$

Diagram 2: Drain current

I_D [A] vs T_C [°C]

$I_D=f(T_C)$; $V_{GS} \geq 10$ V

Diagram 3: Safe operating area

I_D [A] vs V_{DS} [V]

1 µs
10 µs
100 µs
DC
1 ms
10 ms

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance

Z_{thJC} [K/W] vs t_P [s]

0.5
0.2
0.1
0.05
0.02
0.01
single pulse

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$
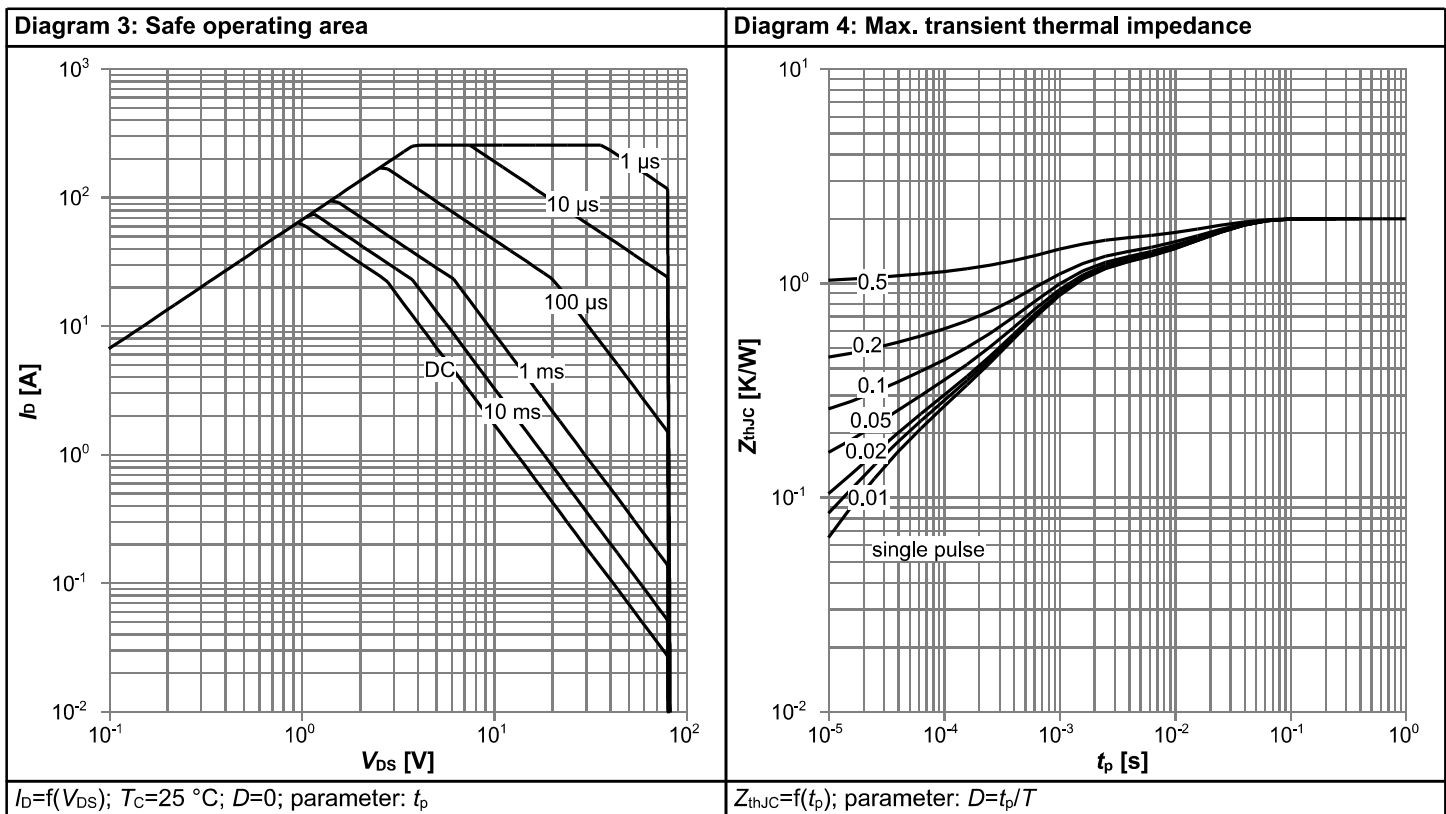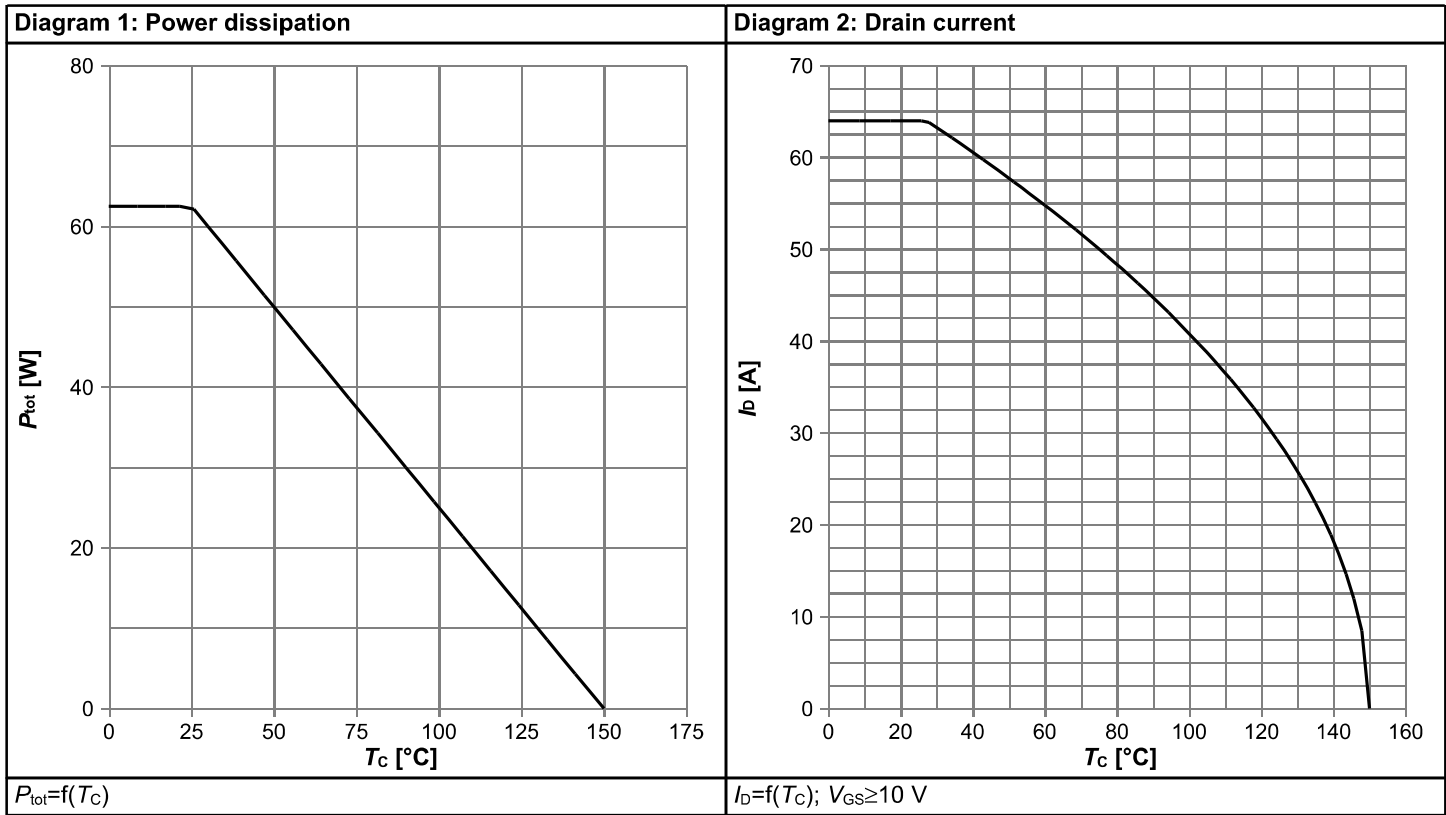
Diagram 5: Typ. output characteristics
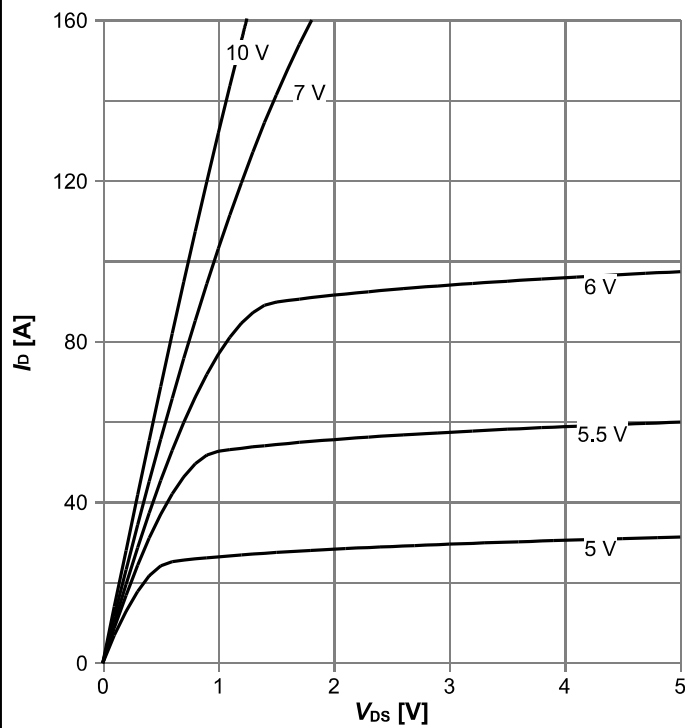
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
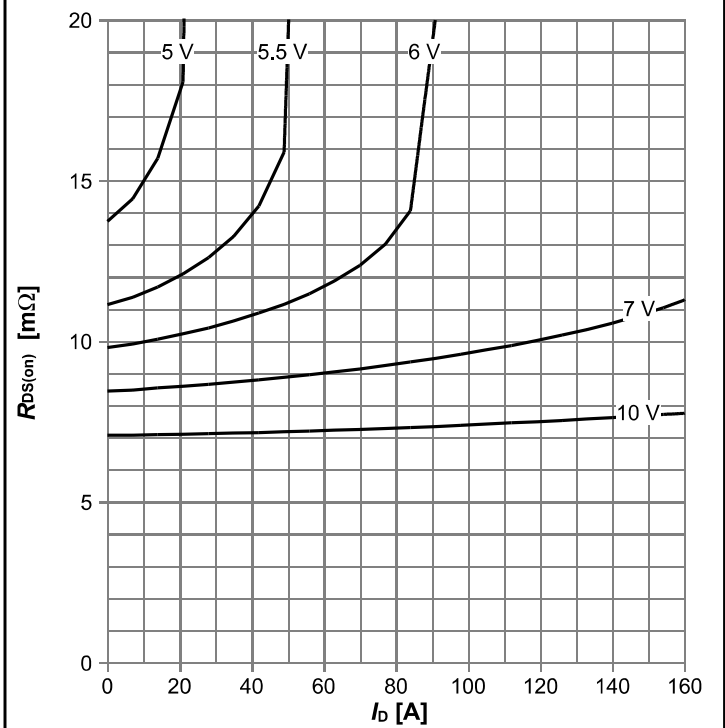
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
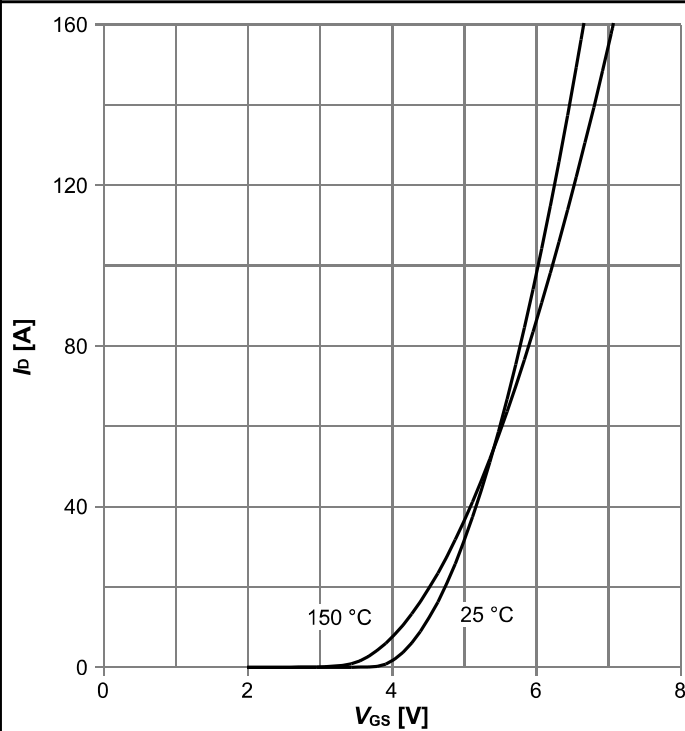
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance
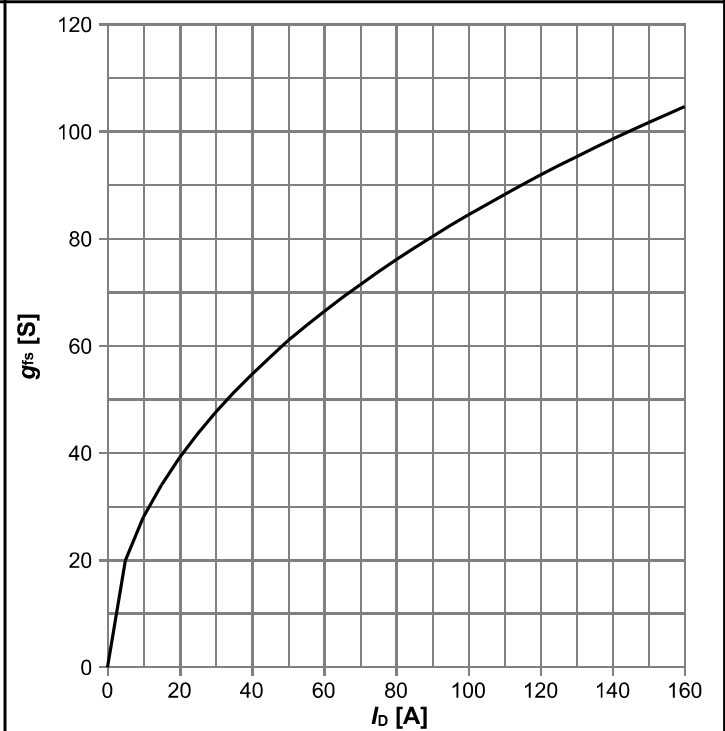
g_{fs}=f(I_D); T_j=25 °C
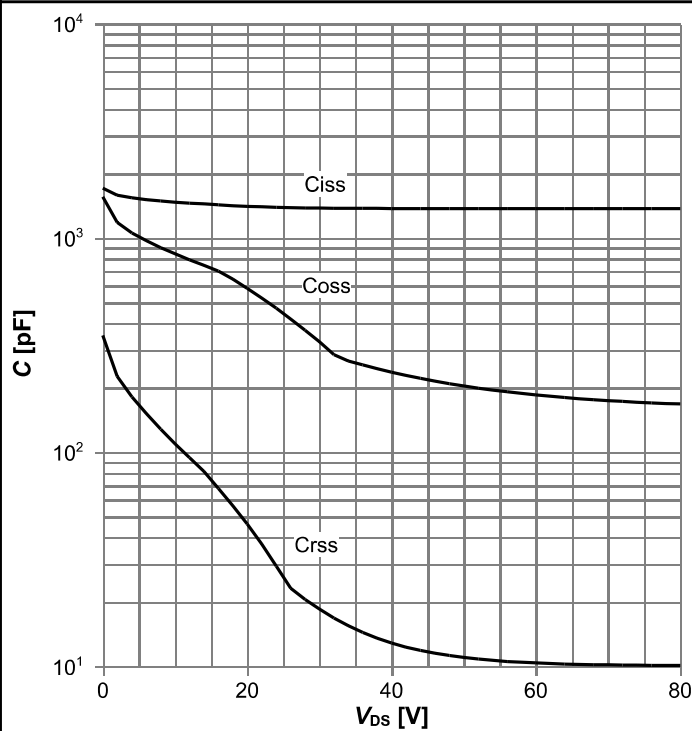
Diagram 9: Drain-source on-state resistance
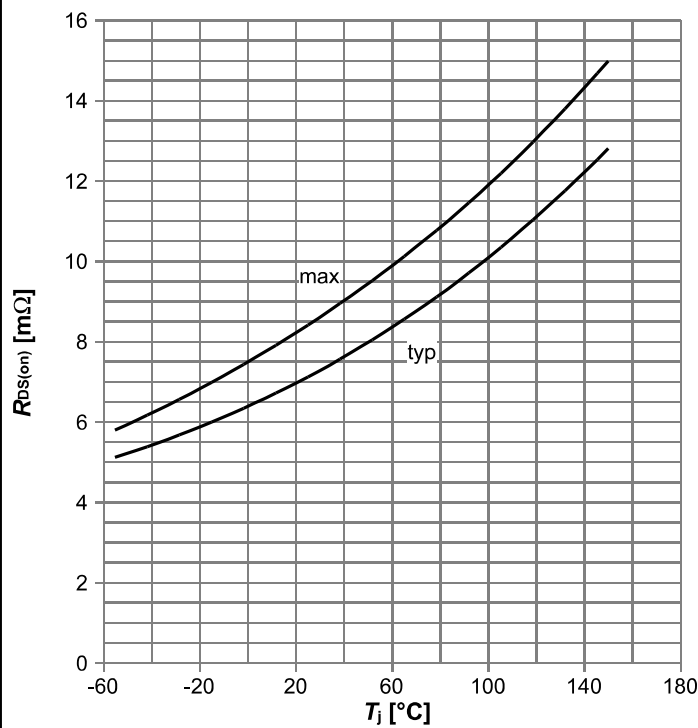
$R_{DS(on)}=f(T_j)$; $I_D=20$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage
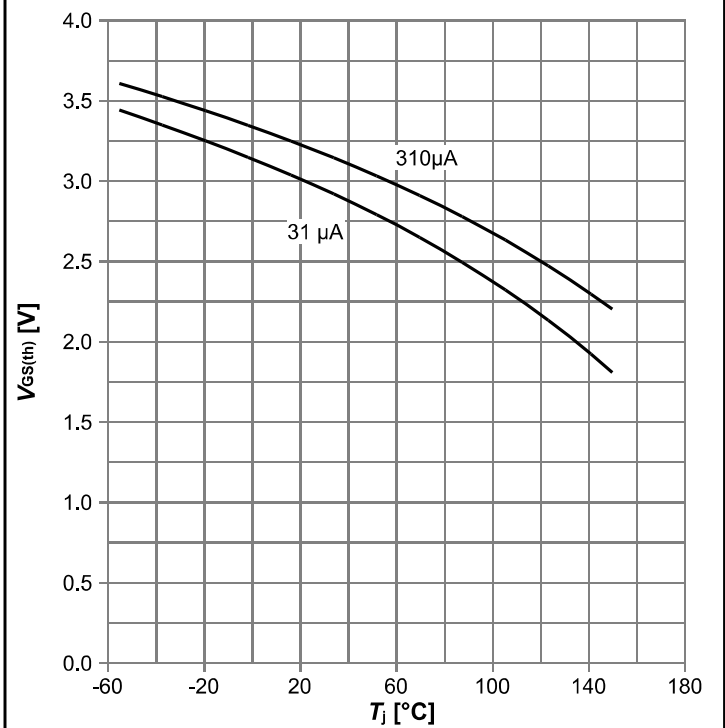
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances

$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

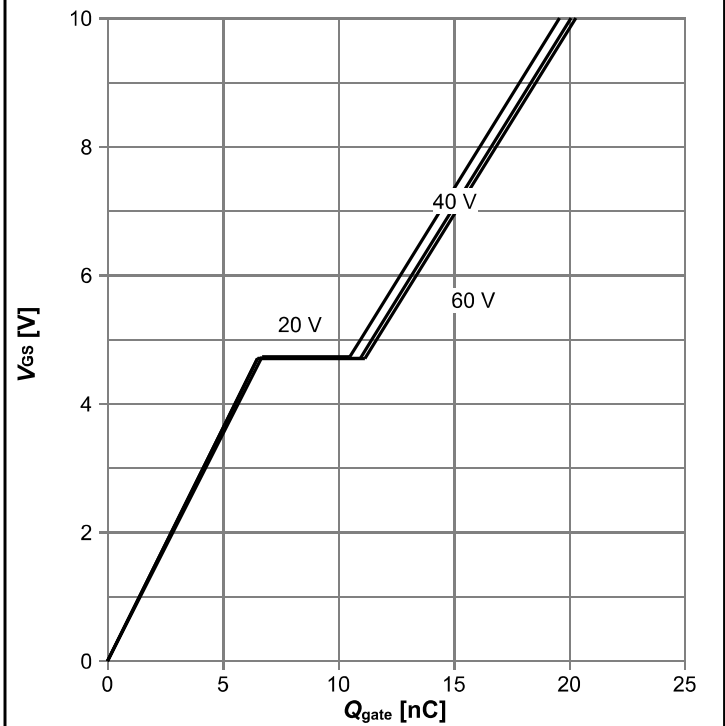**Diagram 12: Forward characteristics of reverse diode**
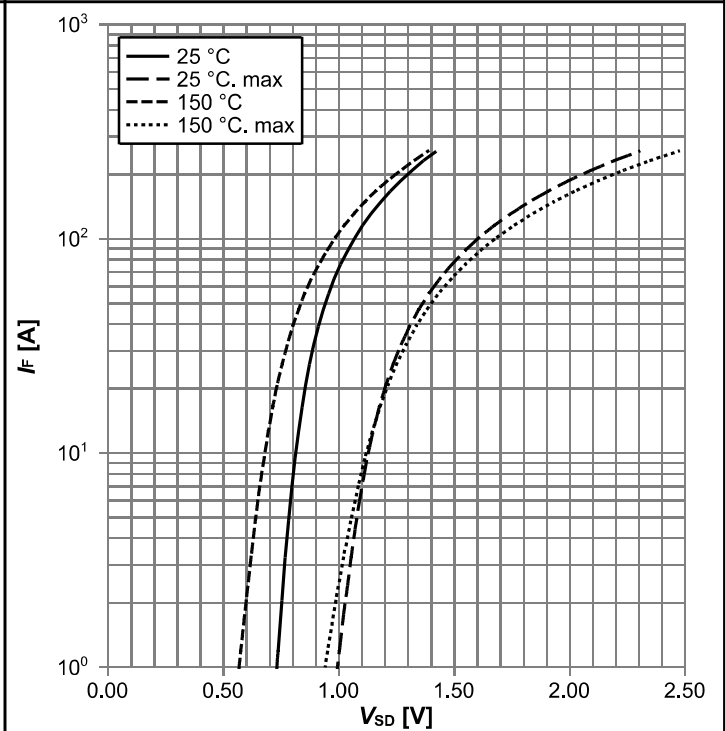
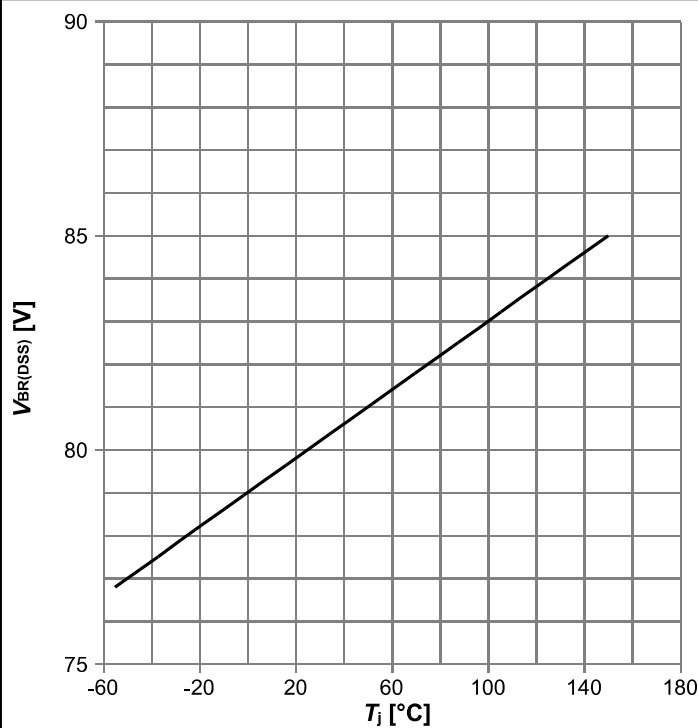$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics
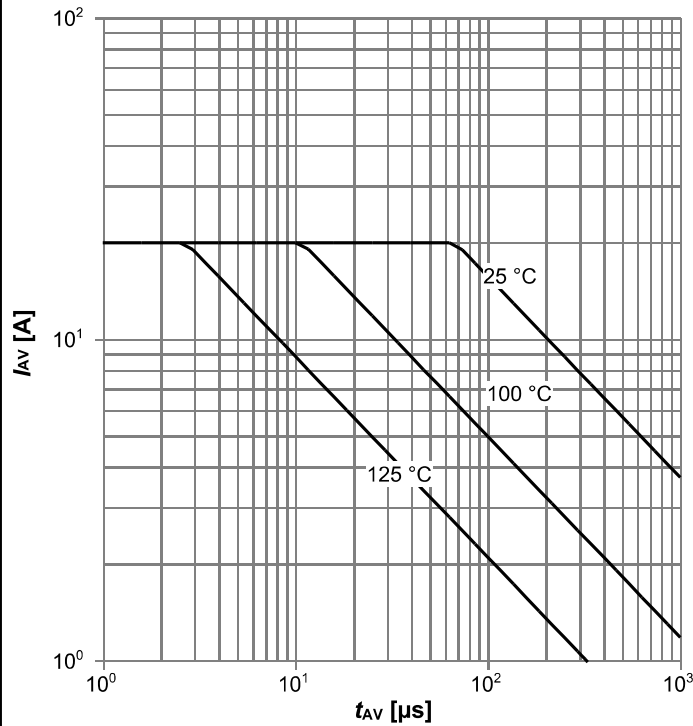
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=20 A pulsed; parameter: V_{DD}
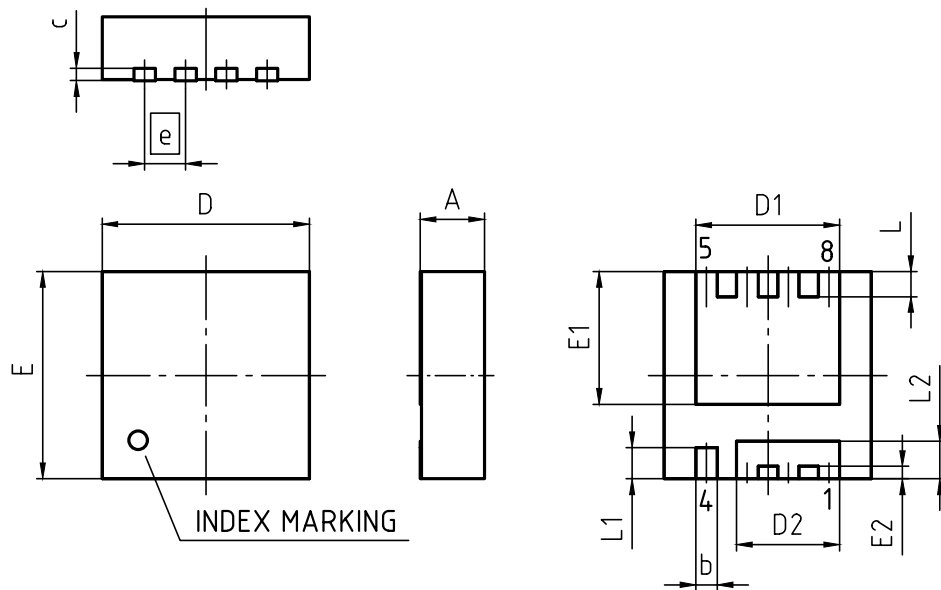
Diagram 15: Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms

5   Package Outlines

DIMENSIONS	MILLIMETERS	
PACKAGE - GROUP NUMBER: **PG-TSDSON-8-U03**		
REVISION: 03	DATE: 20.10.2020	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1   Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

BSZ084N08NS5

Revision: 2021-06-23, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version
2.1	2020-11-09	Update package drawing, footnotes and Diagram 13
2.2	2021-06-23	Update Id max current rating

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