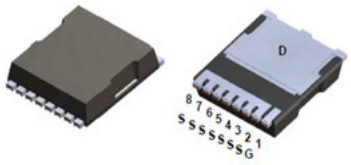
MOSFET – Power, Single N-Channel, TOLL

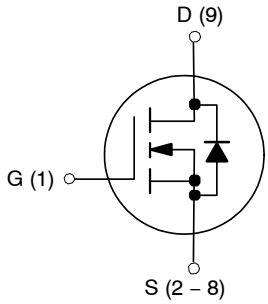
40 V, 300 A, 0.57 mΩ

NVBLS0D5N04C

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.57 mΩ @ 10 V	300 A



H–PSOF8L
CASE 100CU



N–CHANNEL MOSFET

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC–Q101 Qualified and PPAP Capable
- Small Footprint (TOLL) for Compact Design
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain–to–Source Voltage			40	V
V_{GS}	Gate–to–Source Voltage			+20/–16	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	300	A
			T_C = 100°C	300	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	198.4	W
			T_C = 100°C	97.4	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	65	A
			T_A = 100°C	46	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	4.3	W
			T_A = 100°C	2.1	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		4700	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			–55 to +175	°C
I_S	Source Current (Body Diode)			170	A
E_{AS}	Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 55 A, L = 1 mH)			1512	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction–to–Case – Steady State	0.77	°C/W
$R_{\theta JA}$	Junction–to–Ambient – Steady State (Note 2)	35	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface–mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ORDERING INFORMATION

Device	Package	Shipping†
NVBLS0D5N04CTXG	H–PSOF8L (Pb–Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		40			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				21.3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V	T_J = 25°C			1	μA
			T_J = 175°C			1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = +20/−16 V				±100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 475 μA		2	2.8	4	V
$V_{GS(th)}/T_J$	Threshold Temperature Coefficient				−7.4		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 50 A			0.5	0.57	mΩ
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			12600		pF
C_{oss}	Output Capacitance				6705		pF
C_{rss}	Reverse Transfer Capacitance				227		pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz			1.8		Ω
$Q_{G(tot)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A			185		nC
$Q_{G(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V			22		nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 32 V, I_D = 50 A			48		nC
Q_{gd}	Gate−to−Drain “Miller” Charge				38		nC
V_{GP}	Plateau Voltage				4.2		V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(on)}$	Turn−On Delay Time	V_{GS} = 10 V, V_{DD} = 20 V, I_D = 50 A, R_{GEN} = 6 Ω			40		ns
t_r	Turn−On Rise Time				84		ns
$t_{d(off)}$	Turn−Off Delay Time				164		ns
t_f	Turn−Off Fall Time				81		ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 50 A, V_{GS} = 0 V			0.76	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/d_t = 100 A/μs, I_S = 50 A			108		ns
t_a	Charge Time				62		ns
t_b	Discharge Time				46		ns
Q_{rr}	Reverse Recovery Charge				288		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

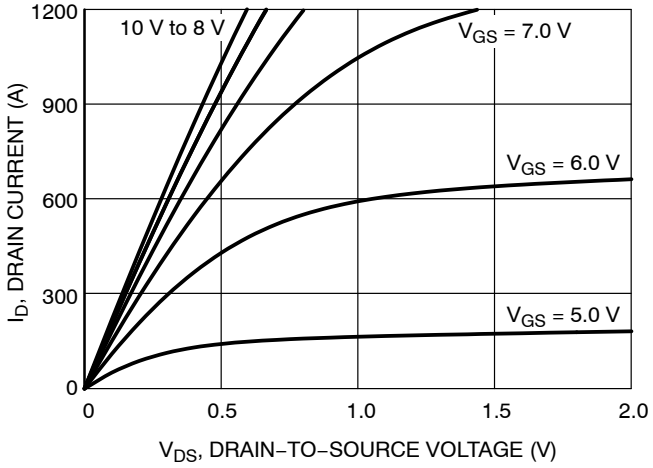


Figure 1. On−Region Characteristics

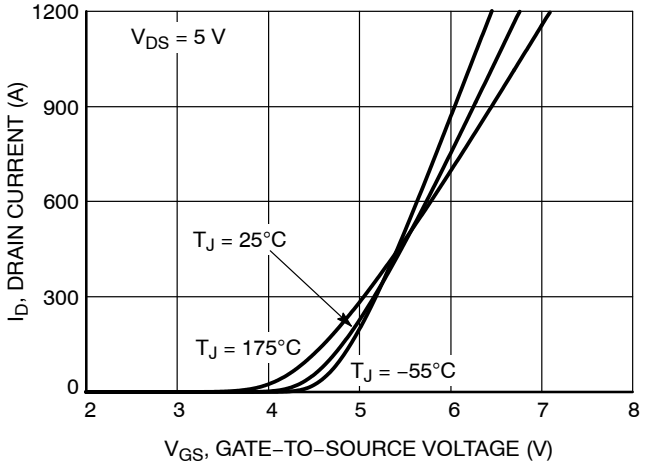


Figure 2. Transfer Characteristics

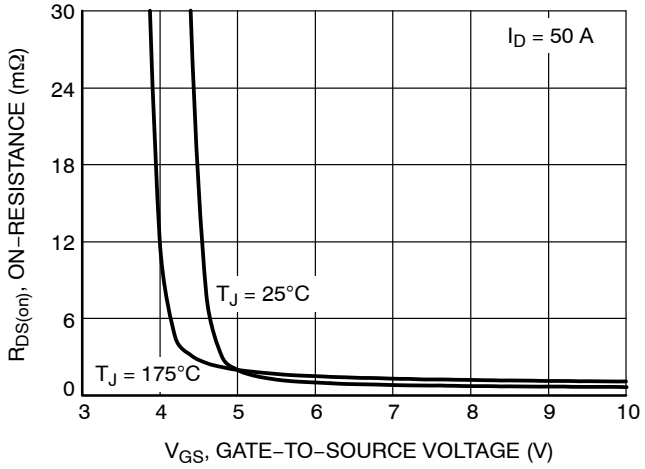


Figure 3. On−Resistance vs. Gate−to−Source Voltage

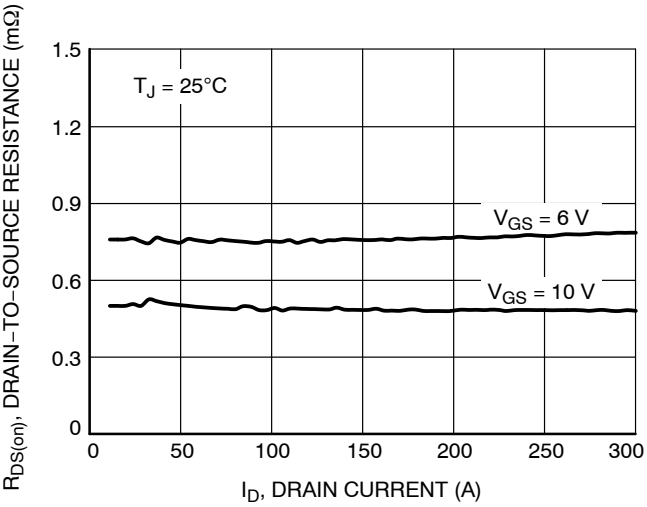


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

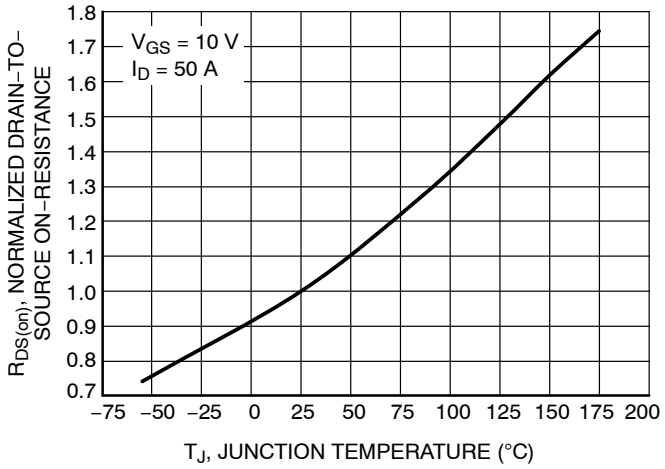


Figure 5. On−Resistance Variation with Temperature

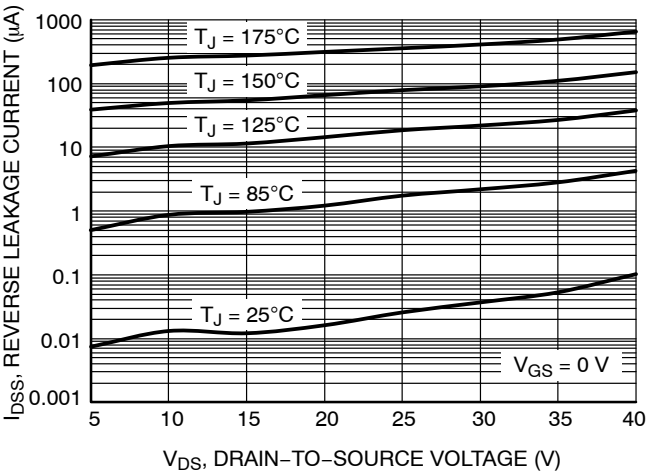


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

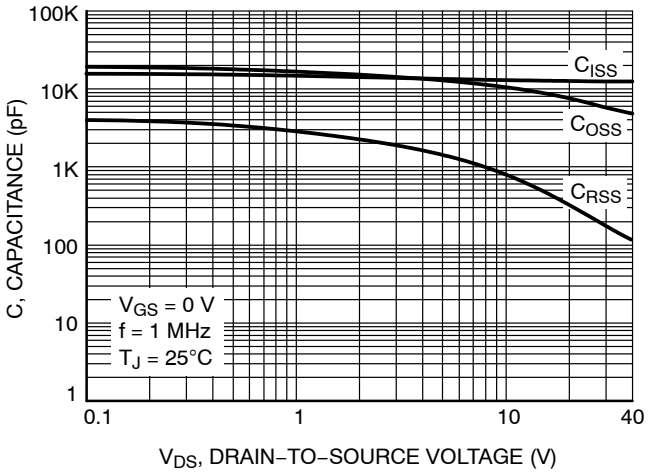


Figure 7. Capacitance Variation

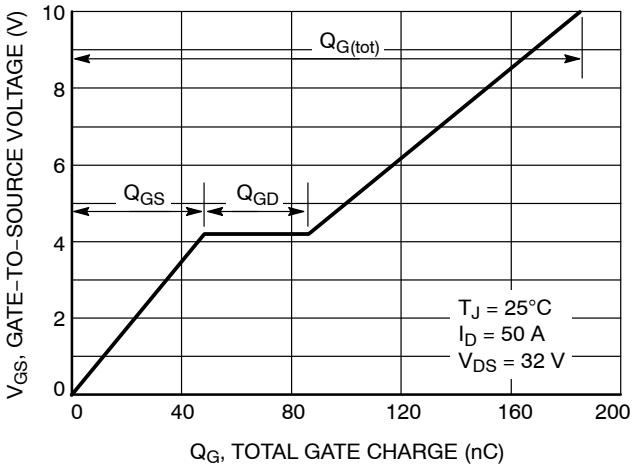


Figure 8. Gate−to−Source Voltage vs. Total Charge

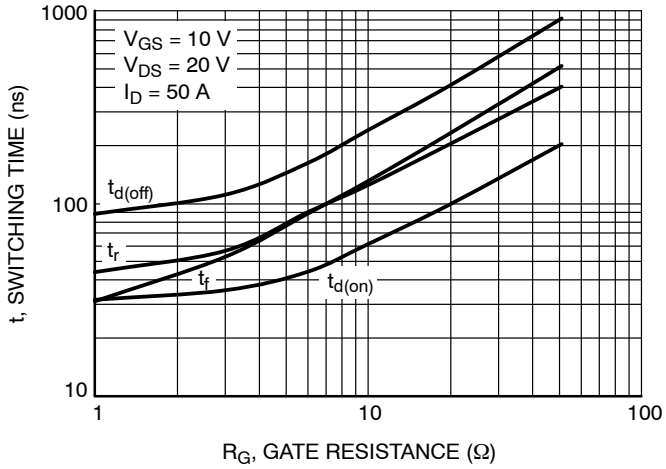


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

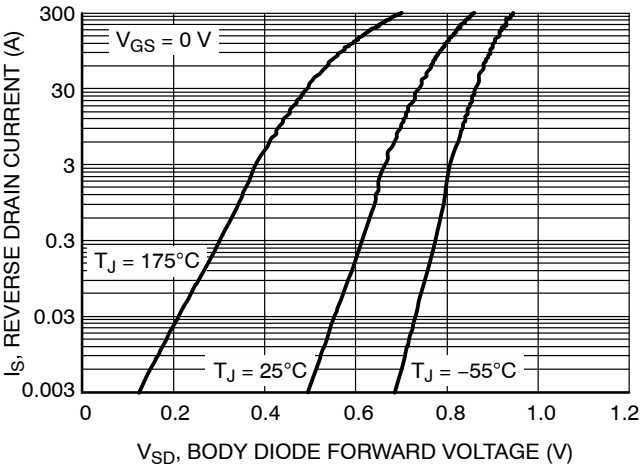


Figure 10. Diode Forward Voltage vs. Current

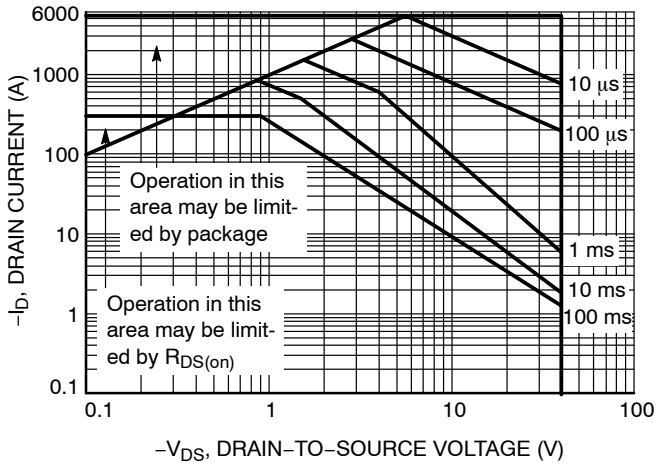


Figure 11. Forward Biased Safe Operating Area

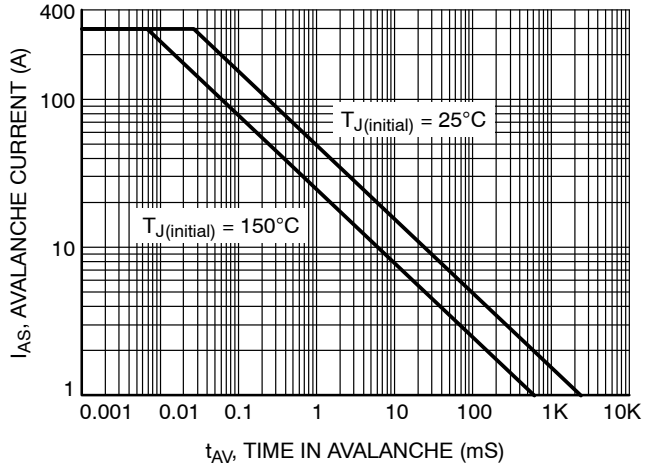


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

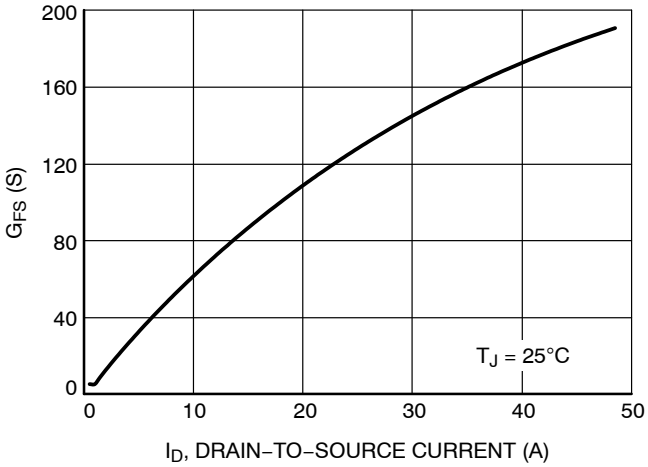


Figure 13. G_{FS} vs. I_D

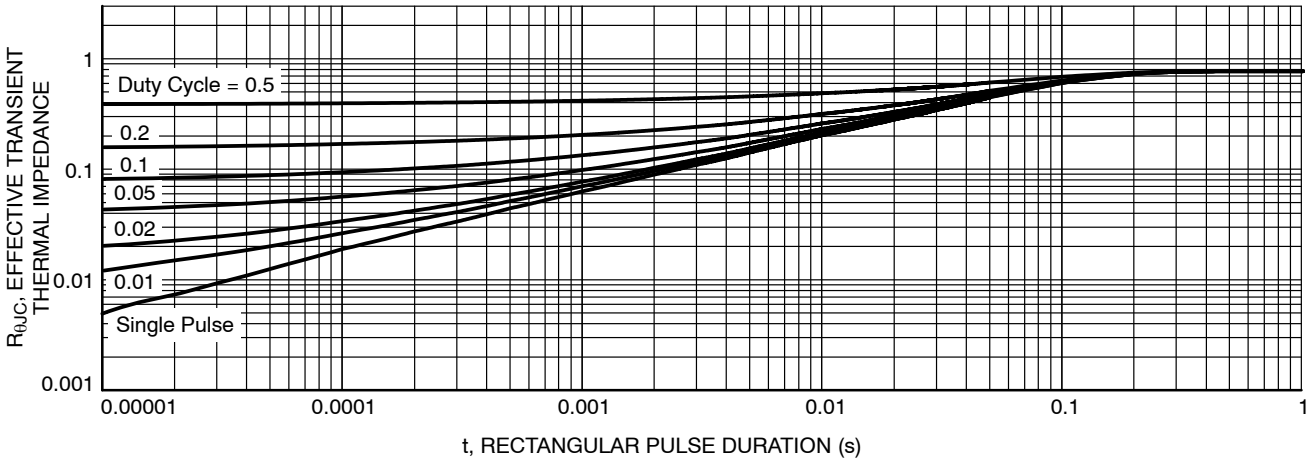
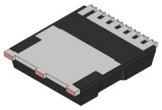
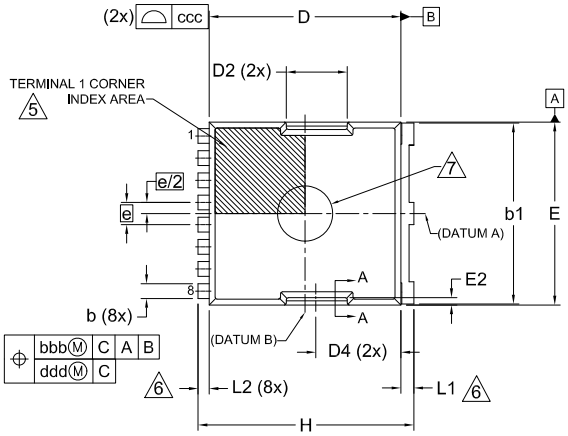


Figure 14. Transient Thermal Impedance

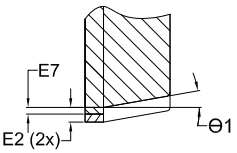


H−PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

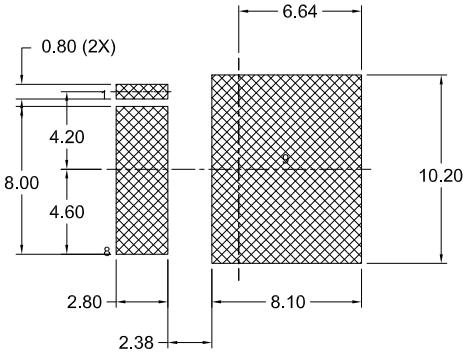
DATE 30 JUL 2024



TOP VIEW

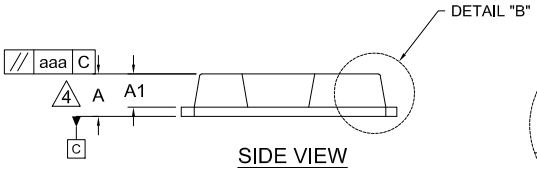


SECTION "A-A"
SCALE: 2X

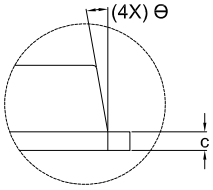


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



SIDE VIEW



DETAIL "B"
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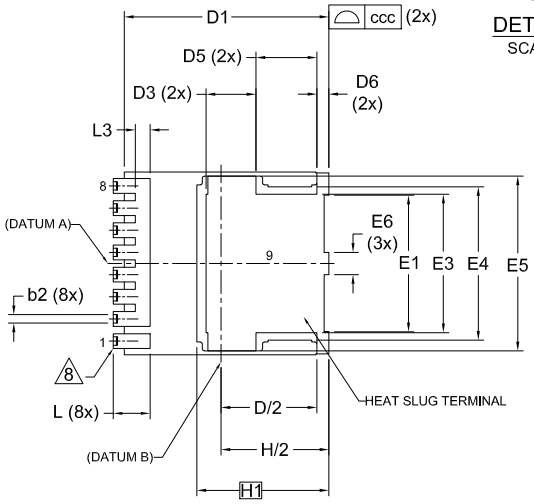


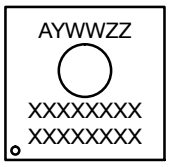
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80x2.30, 1.20P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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