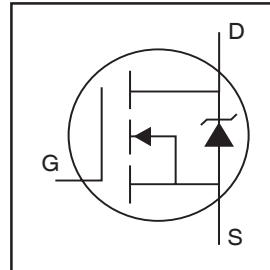


# IRFPS3810PbF

HEXFET® Power MOSFET

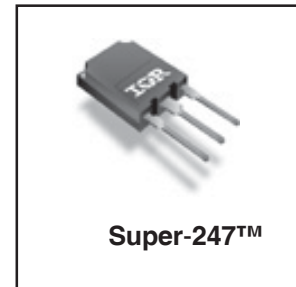
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



$V_{DSS} = 100V$
$R_{DS(on)} = 0.009\Omega$
$I_D = 170A\text{⑥}$

## Description

The HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



## Absolute Maximum Ratings

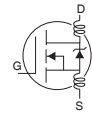
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	170⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	120⑥	
$I_{DM}$	Pulsed Drain Current ①	670	
$P_D @ T_C = 25^\circ C$	Power Dissipation	580	W
	Linear Derating Factor	3.8	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy②	1350	mJ
$I_{AR}$	Avalanche Current①	100	A
$E_{AR}$	Repetitive Avalanche Energy①	58	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.3	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.26	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.009	$\Omega$	$V_{GS} = 10V, I_D = 100A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	52	—	—	S	$V_{DS} = 50V, I_D = 100A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$
$Q_g$	Total Gate Charge	—	260	390	nC	$I_D = 100A$
$Q_{gs}$	Gate-to-Source Charge	—	49	74		$V_{DS} = 80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	160	250		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 50V$
$t_r$	Rise Time	—	270	—		$I_D = 100A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 1.03\Omega$
$t_f$	Fall Time	—	140	—		$V_{GS} = 10V$ ④
$L_D$	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	13	—		
$C_{iss}$	Input Capacitance	—	6790	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	2470	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	990	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	10740	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	1180	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	2210	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$



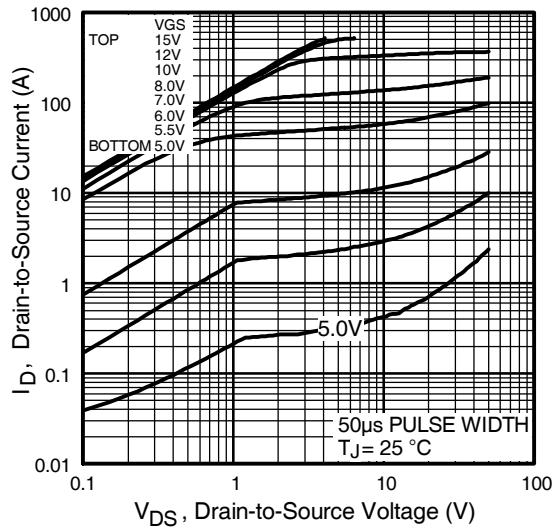
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	170	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	670		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 100A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	220	330	ns	$T_J = 25^\circ\text{C}, I_F = 100A$
$Q_{rr}$	Reverse Recovery Charge	—	1640	2460	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

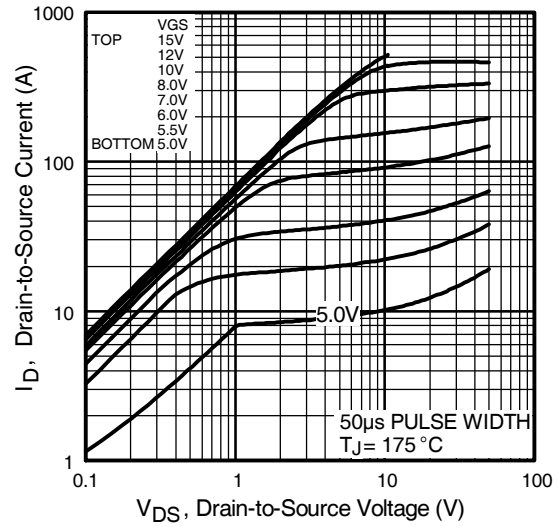
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.27mH$   
 $R_G = 25\Omega$ ,  $I_{AS} = 100A$ . (See Figure 12)
- ③  $I_{SD} \leq 100A$ ,  $di/dt \leq 350A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$

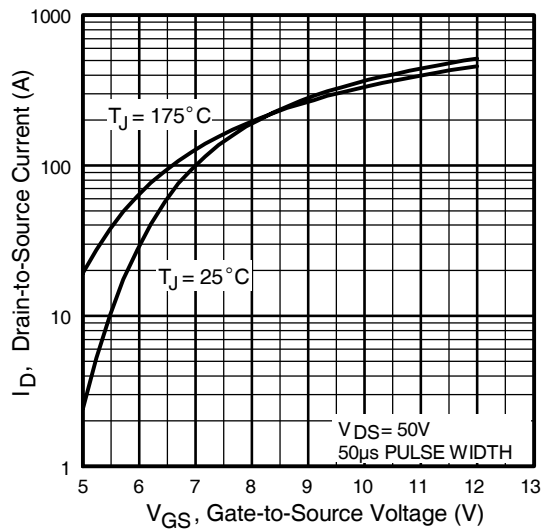
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 105A.



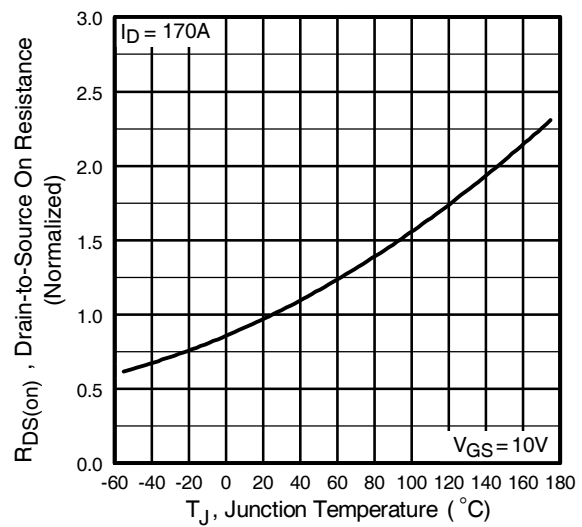
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



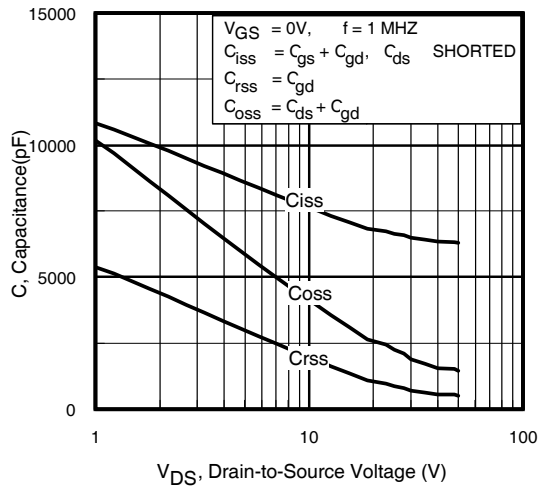
**Fig 3.** Typical Transfer Characteristics



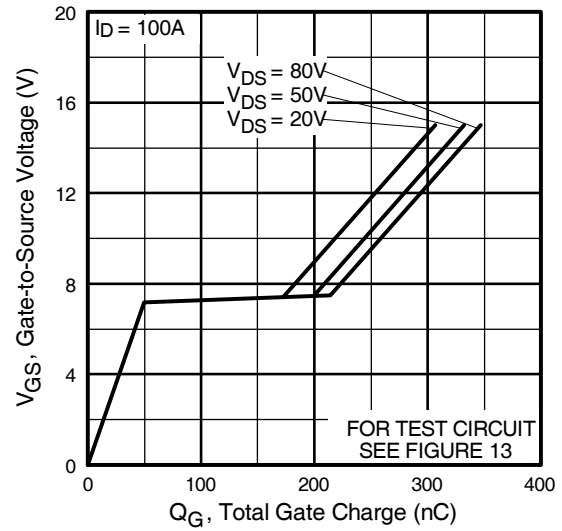
**Fig 4.** Normalized On-Resistance Vs. Temperature

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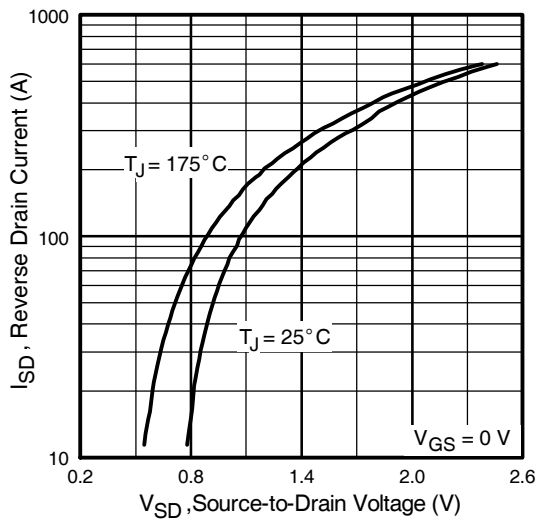
International  
**IR** Rectifier



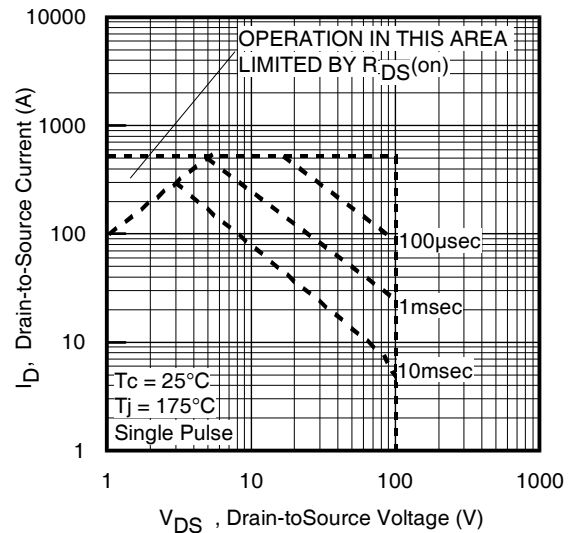
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



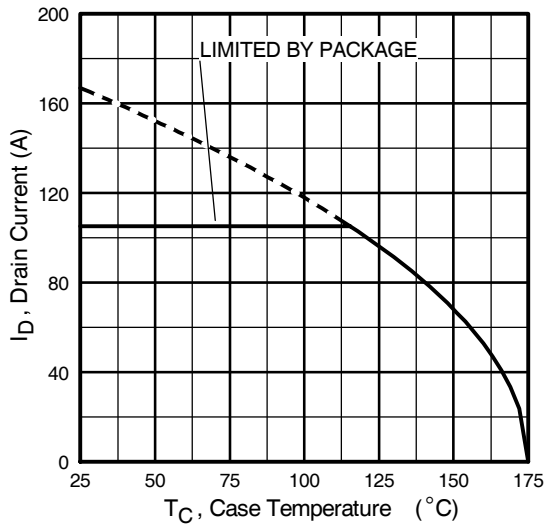
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



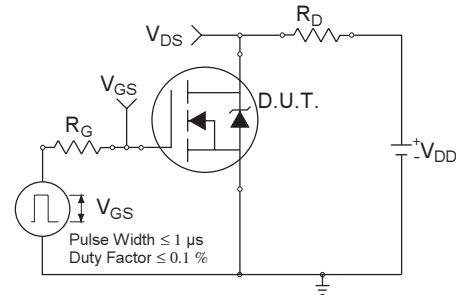
**Fig 7.** Typical Source-Drain Diode Forward Voltage



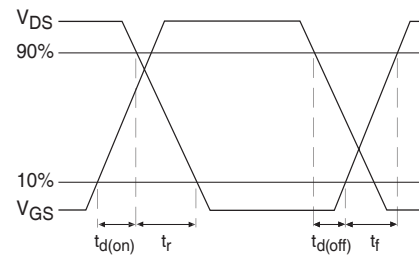
**Fig 8.** Maximum Safe Operating Area



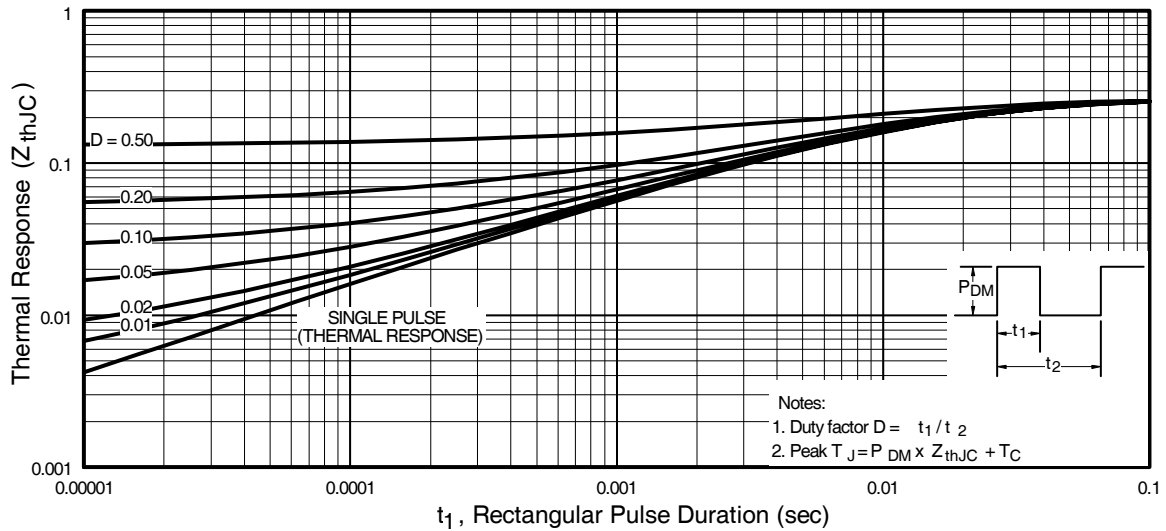
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



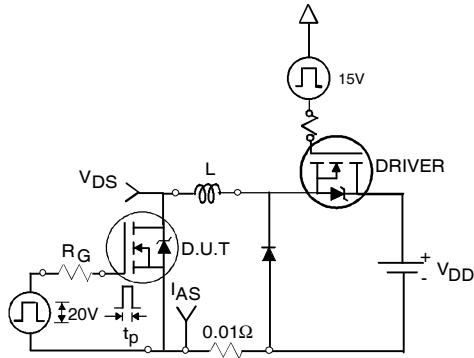
**Fig 10b.** Switching Time Waveforms



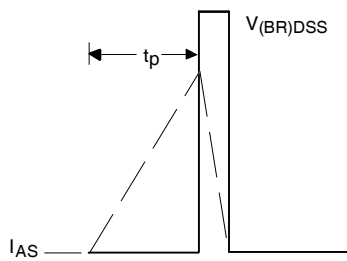
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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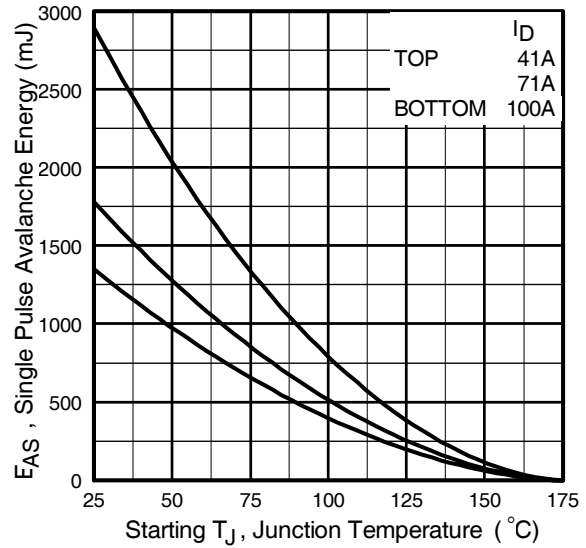
International  
**IR** Rectifier



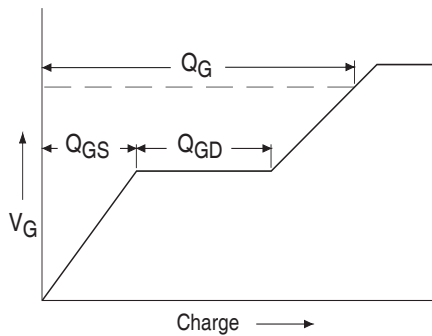
**Fig 12a.** Unclamped Inductive Test Circuit



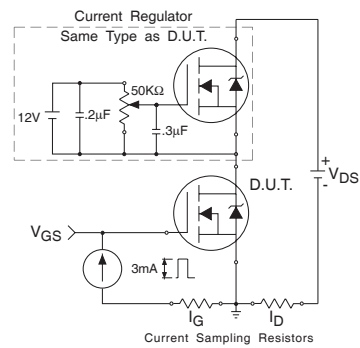
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy  
Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

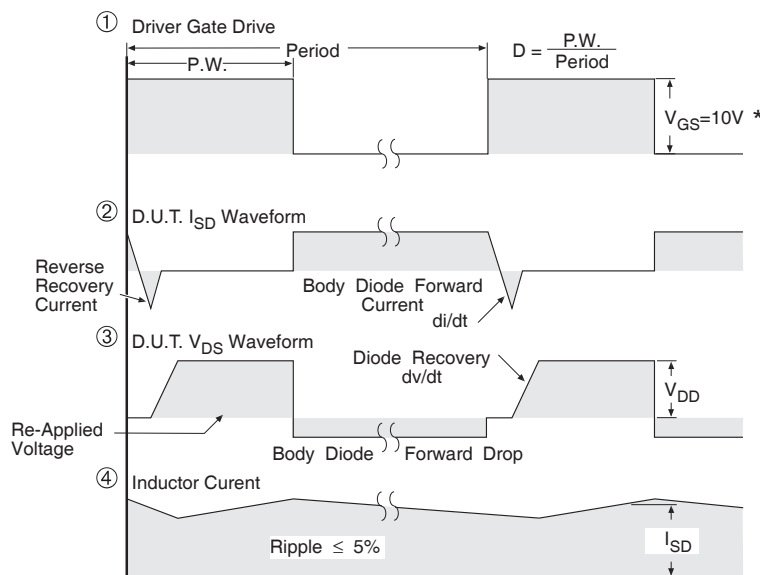
The diagram shows a Class D amplifier circuit. A square-wave voltage source (1) is connected to a gate resistor  $R_G$  and the gate of a MOSFET (D.U.T.). The MOSFET's source is grounded. Its drain is connected to a transformer (2) and a series combination of an inductor (3) and a load resistor (4). The other end of the load resistor is connected to a DC supply  $V_{DD}$ . The transformer's secondary is also connected to ground. A second MOSFET (D.U.T.) is shown in a similar configuration, but its gate is connected to the drain of the first MOSFET. The transformer's primary is connected to the gate of this second MOSFET. The circuit is designed for low stray inductance, a ground plane, and low leakage inductance.

**Circuit Layout Considerations**

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance

**Current Transformer**

- $dv/dt$  controlled by  $R_G$
- Driver same type as D.U.T.
- $I_{SD}$  controlled by Duty Factor "D"
- D.U.T. - Device Under Test

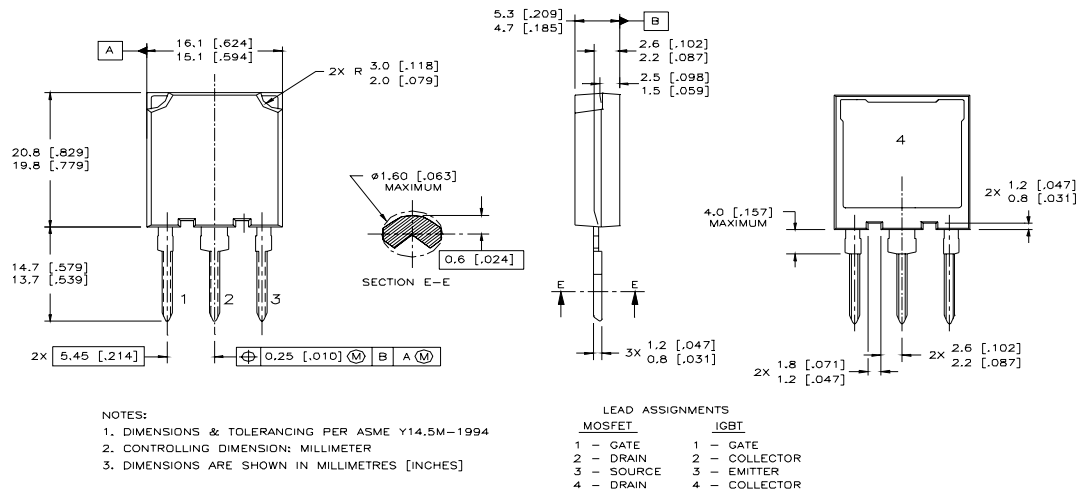


**Fig 14.** For N-Channel HEXFET<sup>®</sup> Power MOSFETs

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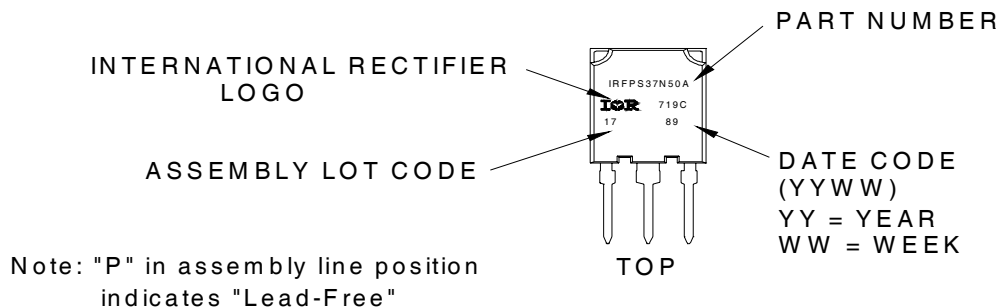
International  
**IR** Rectifier

## Case Outline and Dimensions — Super-247



## Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH  
ASSEMBLY LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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