

# **MOSFET** – Power, Single N-Channel

**60 V, 26 A, 24 m** $\Omega$ 

# **NVMFS5826NL**

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- NVMFS5826NLWF Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices and RoHS Compliant

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parar	Value	Unit		
V <sub>DSS</sub>	Drain-to-Source Voltage			60	V
$V_{GS}$	Gate-to-Source Voltage			±20	V
I <sub>D</sub>	Continuous Drain Cur-		T <sub>mb</sub> = 25°C	26	Α
	(1000000000000000000000000000000000000	, , ,		19	
$P_{D}$	Power Dissipation			39	W
	R <sub>ΨJ-mb</sub> (Notes 1, 2, 3)		T <sub>mb</sub> = 100°C	19	
I <sub>D</sub>	Continuous Drain Current R <sub>0.IA</sub> (Notes 1, 3,		T <sub>A</sub> = 25°C	8.0	Α
	4) Steady	T <sub>A</sub> = 100°C	6.0		
P <sub>D</sub>	Power Dissipation R <sub>0</sub> JA (Notes 1 & 3)	State	T <sub>A</sub> = 25°C	3.6	W
			T <sub>A</sub> = 100°C	1.8	
$I_{DM}$	Pulsed Drain Current	130	Α		
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction and Storage Temperature			–55 to + 175	ç
IS	Source Current (Body Diode)			32	Α
E <sub>AS</sub>	Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, V <sub>DD</sub> = 24 V, V <sub>GS</sub> = 10 V, $I_{L(pk)}$ = 20 A, L = 0.1 mH, $R_G$ = 25 $\Omega$ )			20	mJ
TL	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

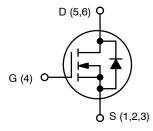
Symbol	Parameter	Value	Unit
$R_{\Psi J-mb}$	Junction-to-Mounting Board (top) - Steady State (Notes 2, 3)	3.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 3)	42	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi  $(\Psi)$  is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub> R <sub>DS(ON)</sub> MA		I <sub>D</sub> MAX
60 V	24 mΩ @ 10 V	00.4
	32 mΩ @ 4.5 V	26 A

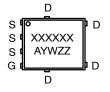


DFN5 (SO-8FL) CASE 488AA STYLE 1



**N-CHANNEL MOSFET** 

#### MARKING DIAGRAM



A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

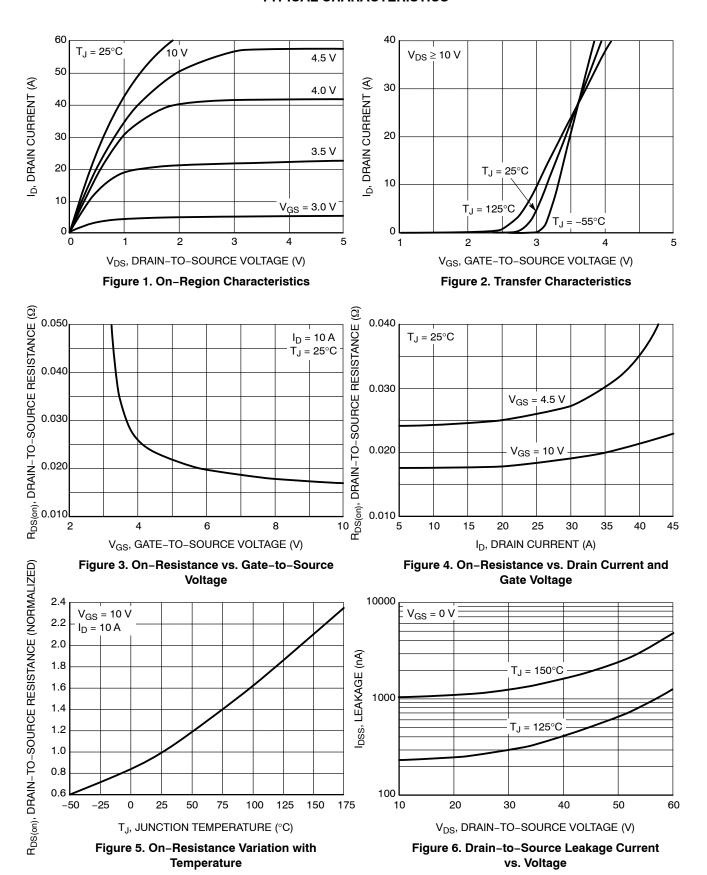
NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Тур	Max	Unit
OFF CHARAC	CTERISTICS	•	•		-	-	-
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
I <sub>DSS</sub>			T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{GS} = 0 V$ , $V_{DS} = 60 V$	T <sub>J</sub> = 125°C			10	1
I <sub>GSS</sub>	Gate-to-Source Leakage Current	$V_{DS} = 0 \text{ V}, V_{G}$	<sub>S</sub> = ± 20 V			±100	nA
ON CHARAC	TERISTICS (Note 5)						
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub>	, = 250 μΑ	1.5		2.5	V
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V,	I <sub>D</sub> = 10 A		18	24	mΩ
		V <sub>GS</sub> = 4.5 V,	I <sub>D</sub> = 10 A		24	32	1
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V,	I <sub>D</sub> = 5 A		8.0		S
CHARGES AN	ND CAPACITANCES						
C <sub>iss</sub>	Input Capacitance	$V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 25 V			850		pF
C <sub>oss</sub>	Output Capacitance				85		1
C <sub>rss</sub>	Reverse Transfer Capacitance	1			50		1
Q <sub>G(TOT)</sub>	Total Gate Charge				9.1		nC
Q <sub>G(TH)</sub>	Threshold Gate Charge				1.0		
$Q_{GS}$	Gate-to-Source Charge	$V_{GS} = 4.5 \text{ V}, V_{DS} =$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 48 \text{ V}, I_D = 10 \text{ A}$		3.0		
$Q_{GD}$	Gate-to-Drain Charge	1			4.0		1
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 10 V, V <sub>DS</sub> =	48 V, I <sub>D</sub> = 10 A		17		nC
SWITCHING	CHARACTERISTICS (Note 6)						
t <sub>d(ON)</sub>	Turn-On Delay Time				9.0		
t <sub>r</sub>	Rise Time	V <sub>GS</sub> = 4.5 V, V	<sub>'DS</sub> = 48 V,		32		ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time	$I_{\rm D} = 10  \rm A,  R_{\rm C}$	$_{\rm G}$ = 2.5 $\Omega$		15		
t <sub>f</sub>	Fall Time	1	-		24		
DRAIN-SOUF	RCE DIODE CHARACTERISTICS						
$V_{SD}$	Forward Diode Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.7		1
t <sub>RR</sub>	Reverse Recovery Time		1		15		
t <sub>a</sub>	Charge Time	$V_{GS}$ = 0 V, dls/dt = 100 A/ $\mu$ s, $I_S$ = 10 A			11		ns
t <sub>b</sub>	Discharge Time				4.0		1
Q <sub>RR</sub>	Reverse Recovery Charge				11		nC

<sup>5.</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



### TYPICAL CHARACTERISTICS (continued)

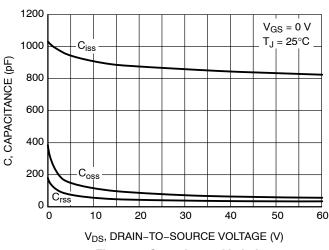


Figure 7. Capacitance Variation

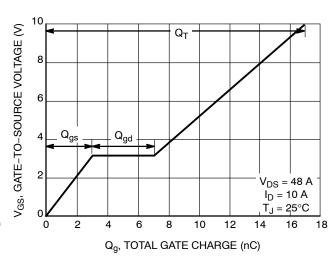


Figure 8. Gate-to-Source Voltage vs. Total Charge

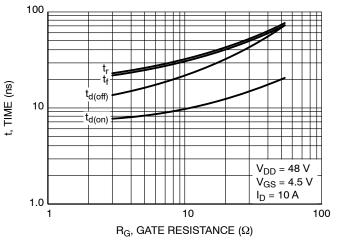


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

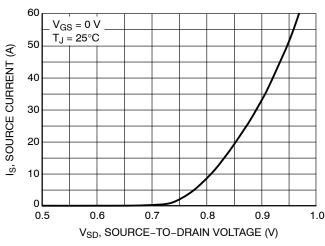


Figure 10. Diode Forward Voltage vs. Current

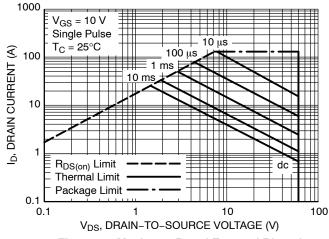


Figure 11. Maximum Rated Forward Biased Safe Operating Area

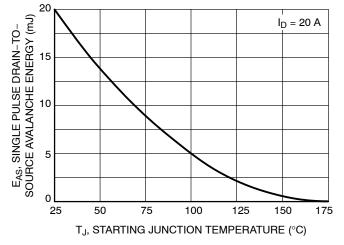


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

### TYPICAL CHARACTERISTICS (continued)

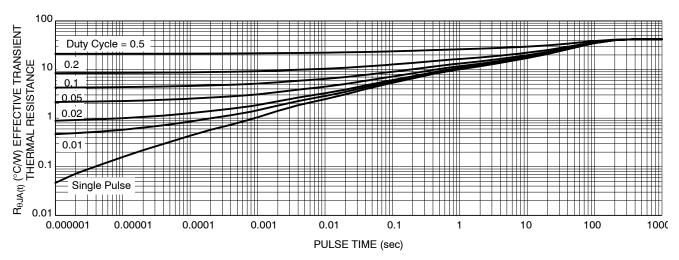


Figure 13. Thermal Response

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5826NLWFT1G	5826LW	DFN5 (Pb-Free)	1500 / Tape & Reel

#### **DISCONTINUED** (Note 7)

NVMFS5826NLT1G	V5826L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5826NLT3G	V5826L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5826NLWFT3G	5826LW	DFN5 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <a href="https://example.com/BRD8011/D">BRD8011/D</a>.

<sup>7.</sup> **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on <a href="https://www.onsemi.com">www.onsemi.com</a>.





DFN5 5x6, 1.27P (SO-8FL) CASE 488AA **ISSUE N** 

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#### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE
- MOLD FLASH PROTRUSIONS OR GATE BURRS

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
М	3.00	3.40	3.80	
θ	0 °		12 °	

#### **GENERIC MARKING DIAGRAM\***



XXXXXX = Specific Device Code

= Assembly Location Α

= Lot Traceability

Υ = Year W = Work Week

ZZ

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





**DETAIL** A

SIDE VIEW

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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