

# N-channel 30 V 4.65 m $\Omega$ logic level MOSFET in LFPAK33 using NextPower Technology

Rev. 3 — 15 June 2012

Product data sheet

### 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

### 1.3 Applications

- DC-to-DC converters
- Load switching

Synchronous buck regulator

#### 1.4 Quick reference data

Table 1. Quick reference data

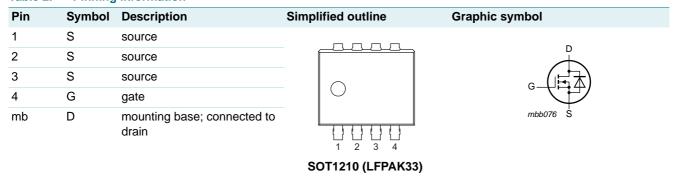
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 ^{\circ}\text{C}$	-	-	30	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	<u>[1]</u> _	-	70	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	69	W
Tj	junction temperature		-55	-	175	°C
Static characte	eristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	5.2	6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	4.05	4.65	mΩ
Dynamic chara	acteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	2.9	-	nC
Q <sub>G(tot)</sub>	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	10.6	-	nC

<sup>[1]</sup> Continuous current is limited by package.



# 2. Pinning information

Table 2. Pinning information



# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R4-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210

### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 ^{\circ}\text{C}$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <u>Figure 1</u>	<u>[1]</u> _	70	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <u>Figure 1</u>	-	64	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 ^{\circ}C$ ; see Figure 4	-	363	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	69	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C
$V_{ESD}$	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	240	-	V
Source-drain	diode				
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	63	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$	-	363	Α
Avalanche rug	ggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 70 A; $V_{sup} \le$ 30 V; $R_{GS}$ = 50 Ω; unclamped; see Figure 3	-	28.6	mJ

<sup>[1]</sup> Continuous current is limited by package.

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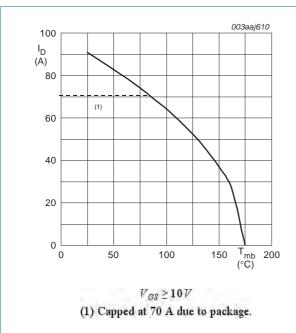


Fig 1. Continuous drain current as a function of mounting base temperature

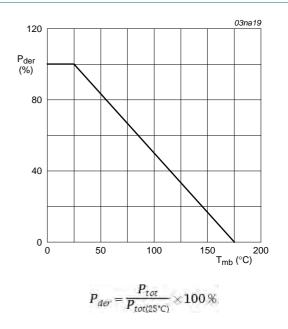


Fig 2. Normalized total power dissipation as a function of mounting base temperature

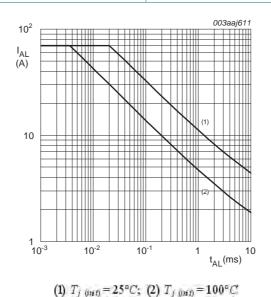
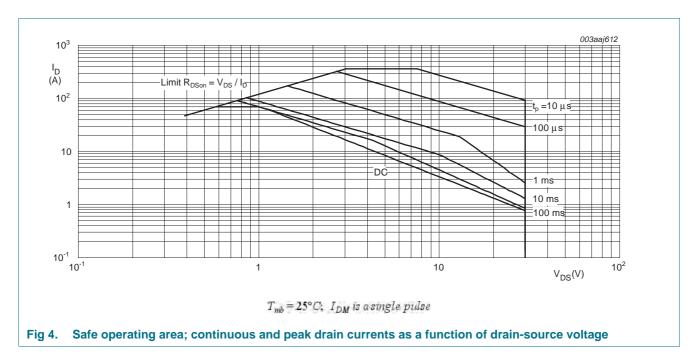


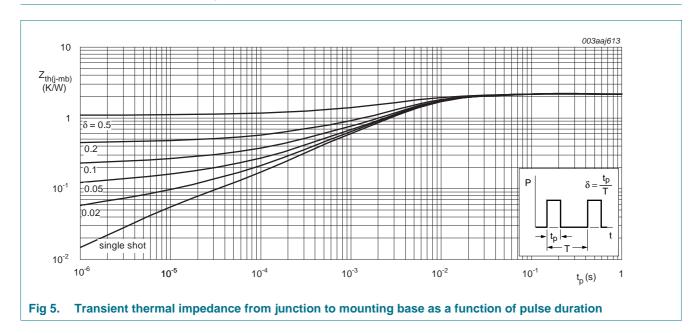
Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	1.95	2.18	K/W



## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac				<i>-</i> 1		-
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 25 °C	30	-	-	V
(511)500	breakdown voltage	$I_D = 250 \mu\text{A};  V_{GS} = 0  \text{V};  T_i = -55 ^{\circ}\text{C}$	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.45	1.8	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-4.1	-	mV/K
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 10	-	5.2	6	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ °C};$ see Figure 10; see Figure 11	-	-	10.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	4.05	4.65	mΩ
		$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 150 \text{ °C}$ ; see <u>Figure 10</u> ; see <u>Figure 11</u>	-	-	7.9	mΩ
$R_G$	gate resistance	f = 1 MHz	0.9	1.8	3.6	Ω
Dynamic cha	aracteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$ ; $V_{DS} = 15 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; see Figure 12; see Figure 13	-	23	-	nC
		$I_D = 25 \text{ A}$ ; $V_{DS} = 15 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; see Figure 12; see Figure 13	-	10.6	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	22.9	-	nC
Q <sub>GS</sub>	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	4.3	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge	see <u>Figure 12</u> ; see <u>Figure 13</u>	-	3.9	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	0.4	-	nC
$Q_{GD}$	gate-drain charge		-	2.9	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	2.88	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	1515	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	333	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	122	-	pF

 Table 6.
 Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 15 V; $R_L$ = 0.6 $\Omega$ ; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 $\Omega$	-	12.6	-	ns
t <sub>r</sub>	rise time		-	23.2	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	16	-	ns
t <sub>f</sub>	fall time		-	11.2	-	ns
Q <sub>oss</sub>	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	9.8	-	nC
Source-drai	in diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 15</u>	-	0.82	1.1	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	18.3	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 15 V	-	11	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V; } I_S = 25 \text{ A; } dI_S/dt = -100 \text{ A/}\mu\text{s;}$ $V_{DS} = 15 \text{ V; see } \frac{\text{Figure 16}}{\text{Figure 16}}$	-	11.3	-	ns
t <sub>b</sub>	reverse recovery fall time		-	7	-	ns

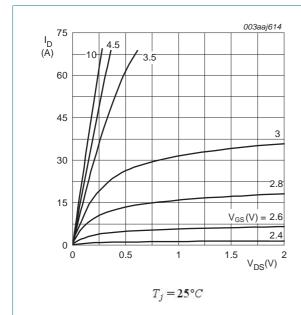


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

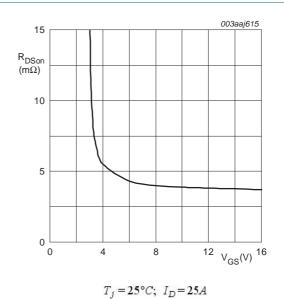


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

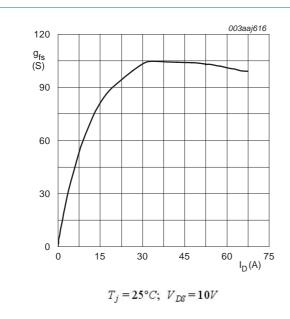


Fig 8. Forward transconductance as a function of drain current; typical values

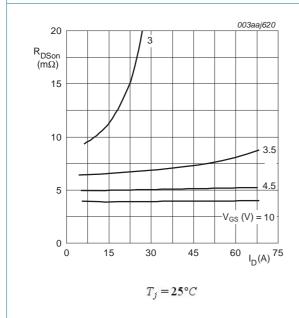


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

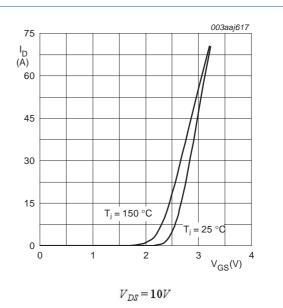


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

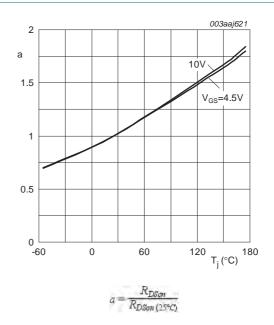


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

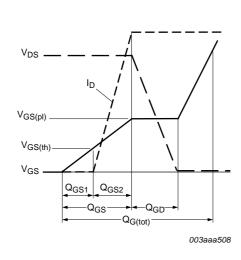


Fig 12. Gate charge waveform definitions

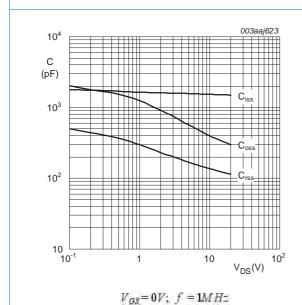


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

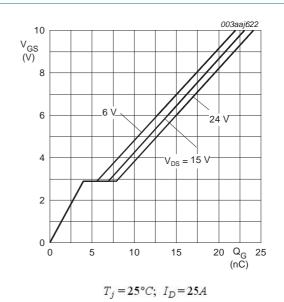


Fig 13. Gate-source voltage as a function of gate charge; typical values

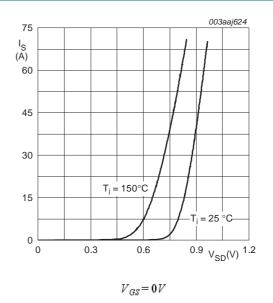
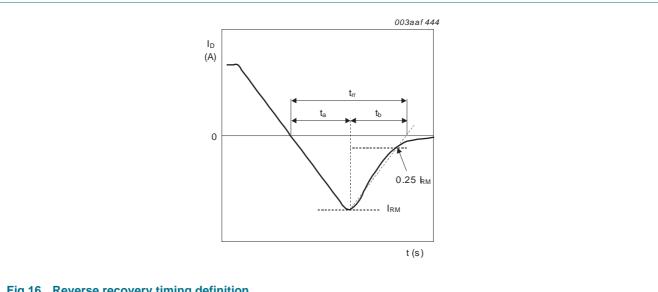


Fig 15. Source current as a function of source-drain voltage; typical values



## 7. Package outline

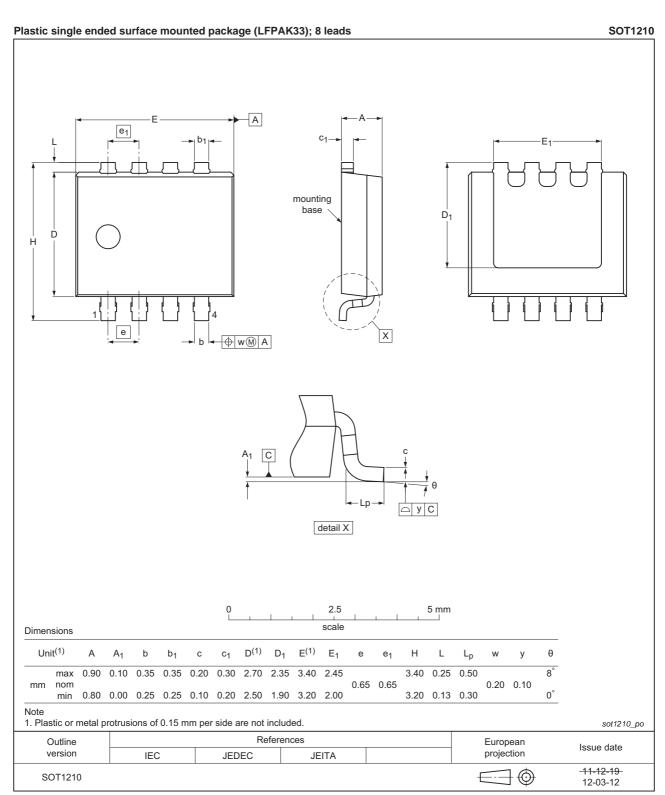


Fig 17. Package outline SOT1210 (LFPAK33)

PSMN4R4-30MLC

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N-channel 30 V 4.65 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

# 8. Revision history

### Table 7. Revision history

Document ID	ocument ID Release date Data she		Change notice	Supersedes
PSMN4R4-30MLC v.3	20120615	Product data sheet	-	PSMN4R4-30MLC v.2
Modifications:	<ul> <li>Various changes to</li> </ul>	content.		
PSMN4R4-30MLC v.2	20120606	Product data sheet	-	PSMN4R4-30MLC v.1

### N-channel 30 V 4.65 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

### 9. Legal information

#### 9.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions".
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