MOSFET – Power, Single **N-Channel** 40 V, 4.6 mΩ, 73 A

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Cur-		T _C = 25°C	I _D	73	Α
rent R _{θJC} (Notes 1 & 3)	Steady	T _C = 100°C		52	
Power Dissipation R _{θJC}	State	T _C = 25°C	P_{D}	47	W
(Note 1)		T _C = 100°C		23	
Continuous Drain	Steady State	T _A = 25°C	I _D	18	Α
Current R _{θJA} (Notes 1, 2 & 3)		T _A = 100°C		13	
Power Dissipation R _{θJA}		T _A = 25°C	P _D	3.0	W
(Notes 1 & 2)		T _A = 100°C		1.5	
Pulsed Drain Current	T _A = 25°	C, t _p = 10 μs	I _{DM}	395	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	39	Α
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _{L(pk)} = 6.5 A)			E _{AS}	147	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	3.2	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	49	

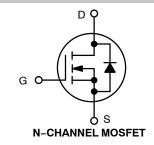
- 1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
 Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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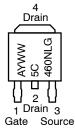
V _{(BR)DSS}	R _{DS(on)}	I _D	
40 V	4.6 mΩ @ 10 V	73 A	
	$6.5~\mathrm{m}\Omega$ @ $4.5~\mathrm{V}$	75 K	





DPAK CASE 369C STYLE 2

MARKING DIAGRAM **& PIN ASSIGNMENT**



= Assembly Location

= Year WW = Work Week 5C460NL = Device Code = Pb-Free Package

ORDERING INFORMATION

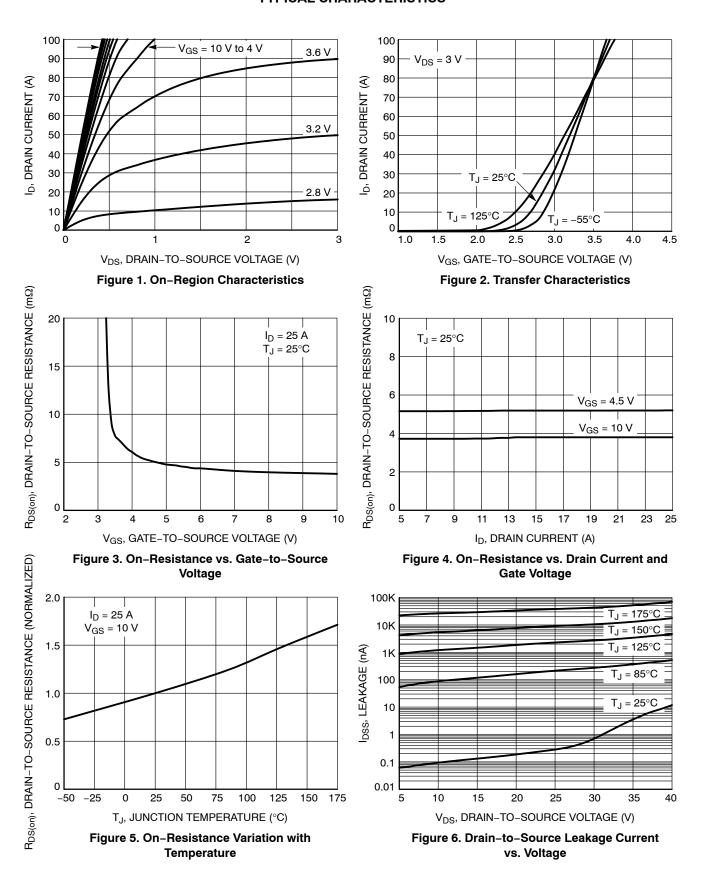
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condi	ition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u> </u>						•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			10	μΑ
		$V_{DS} = 40 \text{ V}$	T _J = 125°C			250	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	_S = 20 V			100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D}$	= 60 μΑ	1.2		2.2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _E	₎ = 25 A		5.2	6.5	mΩ
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D	= 25 A		3.8	4.6	mΩ
Forward Transconductance	9FS	$V_{DS} = 3 \text{ V}, I_{D}$	= 25 A		76		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCES						
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 25 \text{ V}$			2100		pF
Output Capacitance	C _{oss}				800		1
Reverse Transfer Capacitance	C _{rss}				36		1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 32 \text{ V},$ $I_D = 25 \text{ A}$			17		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 25 A			36		nC
Threshold Gate Charge	Q _{G(TH)}				3.7		
Gate-to-Source Charge	Q_{GS}				6.5		1
Gate-to-Drain Charge	Q_{GD}				5.7		
Plateau Voltage	V _{GP}				3.1		V
SWITCHING CHARACTERISTICS (Note 5)			•		•		
Turn-On Delay Time	t _{d(on)}				9.0		ns
Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DS}$	c = 32 V.		26		-
Turn-Off Delay Time	t _{d(off)}	$I_D = 25 \text{ A}, R_G$	= 2.5 Ω		29		
Fall Time	t _f	•			6.0		1
DRAIN-SOURCE DIODE CHARACTERISTIC	S						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.85	1.2	V
		$I_{S} = 25 \text{ A}$	T _J = 125°C		0.73		1
Reverse Recovery Time	t _{RR}		1		37		ns
Charge Time	ta	V _{GS} = 0 V, dls/dt = 100 A/μs, l _S = 25 A			18		1
Discharge Time	tb				19		1
Reverse Recovery Charge	Q _{RR}				30		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

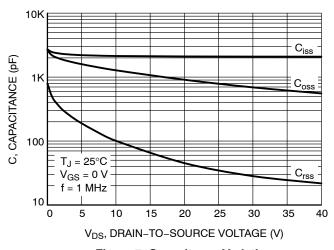


Figure 7. Capacitance Variation

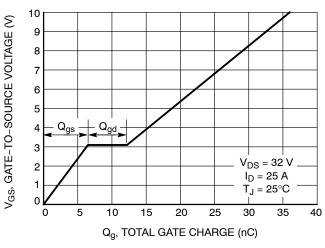


Figure 8. Gate-to-Source Voltage vs. Total Charge

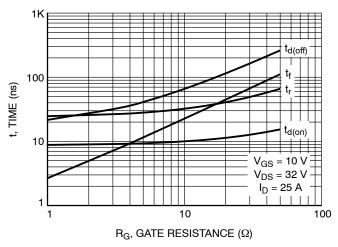


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

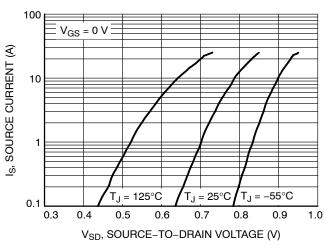


Figure 10. Diode Forward Voltage vs. Current

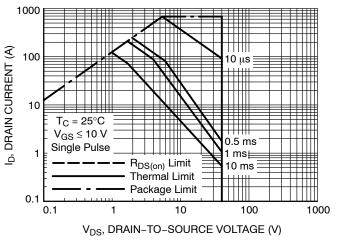


Figure 11. Maximum Rated Forward Biased Safe Operating Area

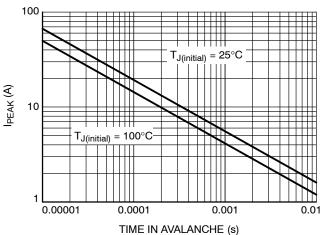


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

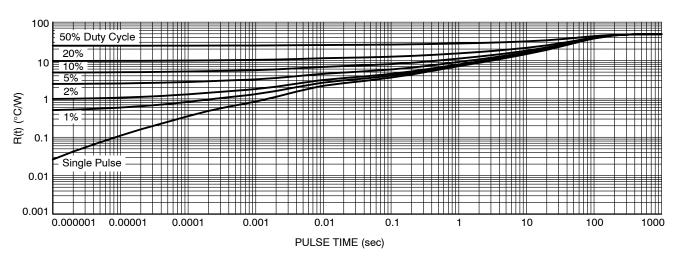


Figure 13. Thermal Response

ORDERING INFORMATION

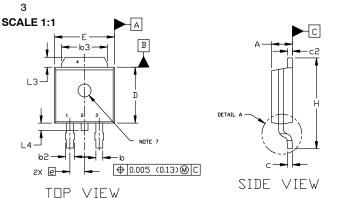
Order Number	Package	Shipping [†]
NVD5C460NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DPAK (SINGLE GAUGE)

CASE 369C ISSUE G

DATE 31 MAY 2023

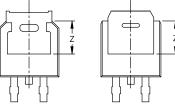


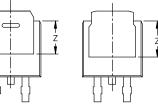


- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
 GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE DUTERMOST EXTREMES OF THE PLASTIC BODY.

 DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS		
MIM	MIN.	MAX.	MIN.	MAX.	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
ھ	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b 3	0.180	0.215	4.57	5.46	
Ū	0.018	0.024	0.46	0.61	
-2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29 BSC		
Η	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114	REF	2.90 REF		
L2	0.020	BSC	0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040	-	1.01	
Z	0.155		3.93		

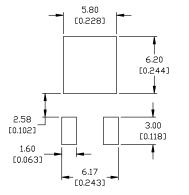




BOTTOM VIEW

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS





CW ROTATED 90°

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
Α	= Assembly Location
L	= Wafer Lot
Υ	= Year
WW	= Work Week
G	= Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT* *FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

S

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:
PIN 1. BASE	PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE	PIN 1. GATE
2. COLLECTOR	2. DRAIN	CATHODE	2. ANODE	ANODE
EMITTER	SOURCE	ANODE	3. GATE	CATHODE
COLLECTOR	4. DRAIN	CATHODE	ANODE	ANODE

STYLE 7: PIN 1. GATE 2. COLLECTOR STYLE 6: STYLE 8: STYLE 9: STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE PIN 1. MT1 2. MT2 PIN 1. N/C 2. CATHODE 3. ANODE PIN 1. ANODE 2. CATHODE 3 FMITTER 3 RESISTOR ADJUST 3 GATE 4. COLLECTOR 4. CATHODE 4. ANODE 4. CATHODE

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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