

Automotive MOSFET

OptiMOS™ 7 Power-Transistor



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential Applications

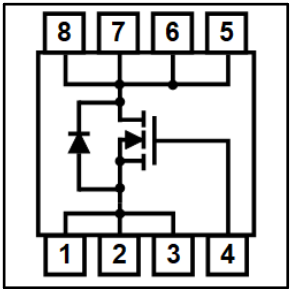
General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

$V_{DS}$	100	V
$R_{DS(on)}$	4.0	mΩ
$I_D$ (chip limited)	130	A



Type	Package	Marking
IAUCN10S7N040	PG-TDSON-8-34	7N10N040

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## Maximum Ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS} = 10\text{ V}$ , Chip limitation <sup>1,2)</sup>	130	A
		$V_{GS} = 10\text{ V}$ , DC current	120	
		$T_a = 100^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,3)</sup>	18	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C = 25^\circ\text{C}$ , $t_p = 100\text{ }\mu\text{s}$	363	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D = 44\text{ A}$	68	mJ
Avalanche current, single pulse	$I_{AS}$	–	88	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C = 25^\circ\text{C}$	142	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	$^\circ\text{C}$

## Thermal Characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	1.06	K/W
Thermal resistance, junction - ambient <sup>3)</sup>	$R_{thJA}$	–	–	26.1	–	

## Electrical Characteristics

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static Characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	100	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 66\text{ }\mu\text{A}$	2.3	2.8	3.2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25^\circ\text{C}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 100^\circ\text{C}^{2)}$	–	–	17	
Gate-source leakage current	$I_{GSS}$	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 7\text{ V}$ , $I_D = 30\text{ A}$	–	4.1	4.7	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 60\text{ A}$	–	3.6	4.0	
Gate resistance <sup>2)</sup>	$R_G$	–	–	1.3	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics <sup>2)</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz	–	2815	3660	pF
Output capacitance	C <sub>oss</sub>		–	1177	1531	
Reverse transfer capacitance	C <sub>rss</sub>		–	14	21	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 60 A, R <sub>G</sub> = 3.5 Ω	–	10.1	–	ns
Rise time	t <sub>r</sub>		–	8.0	–	
Turn-off delay time	t <sub>d(off)</sub>		–	16.8	–	
Fall time	t <sub>f</sub>		–	9.9	–	

<b>Gate Charge Characteristics<sup>2)</sup></b>						
Gate to source charge	$Q_{gs}$	$V_{DD} = 50\text{ V}, I_D = 60\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$	–	13.2	17.2	nC
Gate to drain charge	$Q_{gd}$		–	6.7	10.1	
Gate charge total	$Q_g$		–	39.3	51.1	
Gate plateau voltage	$V_{plateau}$		–	4.6	–	V

<b>Reverse Diode</b>						
Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C = 25^\circ\text{C}$	–	–	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C = 25^\circ\text{C}, t_p = 100\ \mu\text{s}$	–	–	363	
Diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_F = 60\text{ A}, T_j = 25^\circ\text{C}$	–	0.9	1.0	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R = 50\text{ V}, I_F = 50\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$	–	35	53	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		–	23	46	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

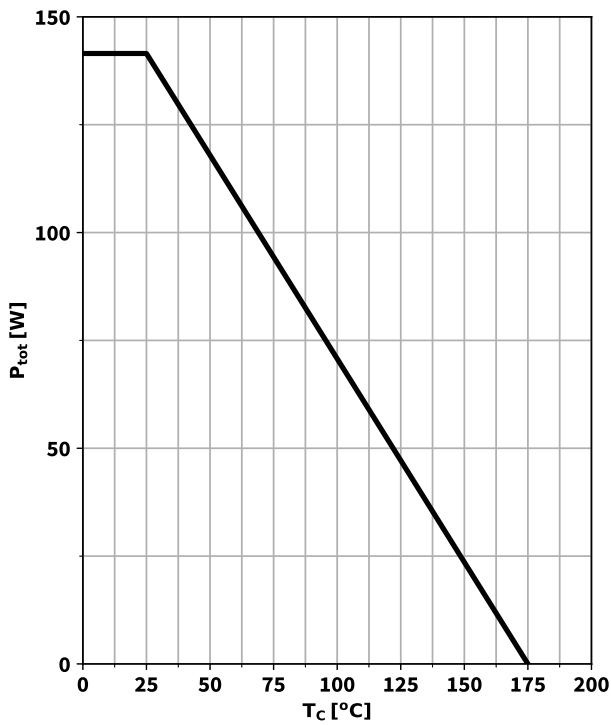
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

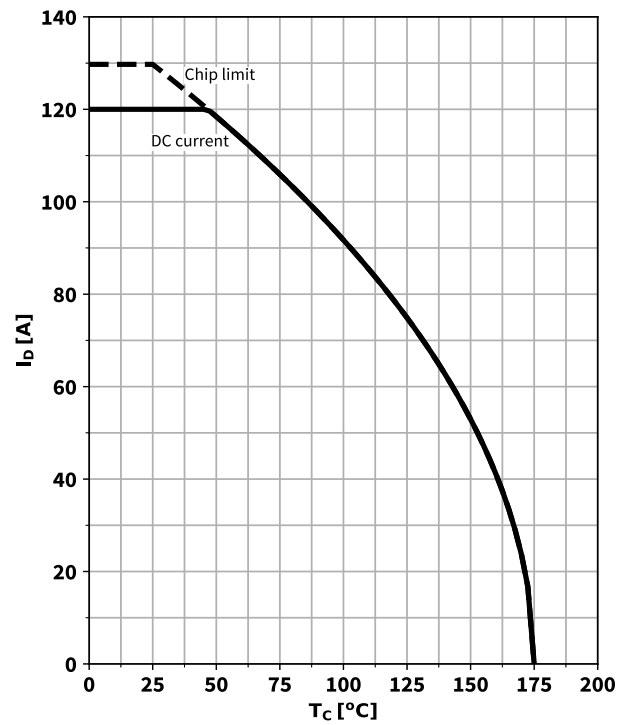
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



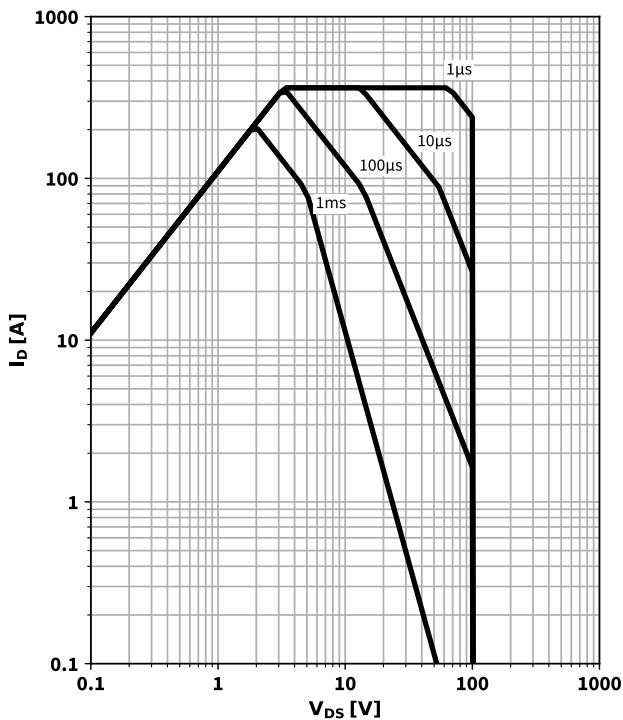
### 2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



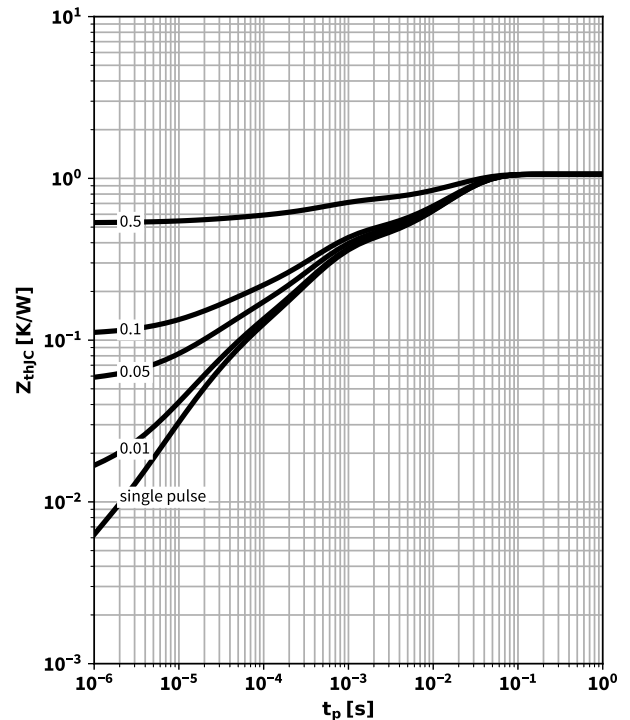
### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^{\circ}\text{C}; D = 0; \text{parameter: } t_p$$



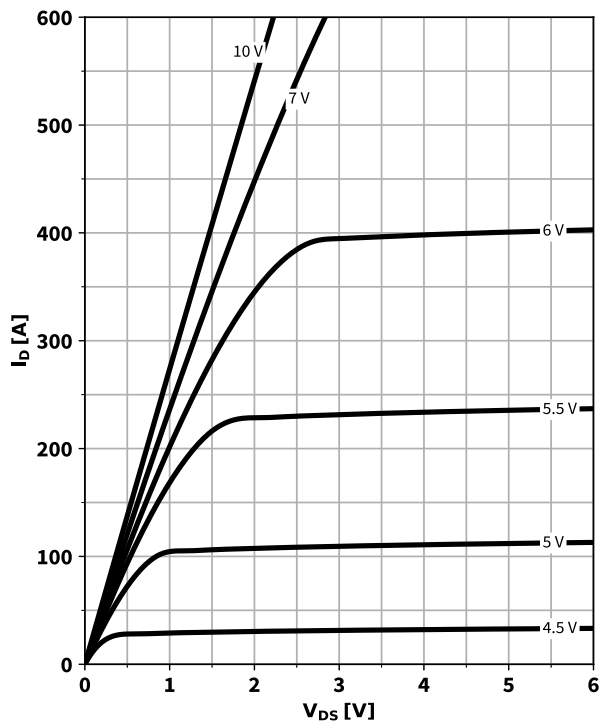
### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



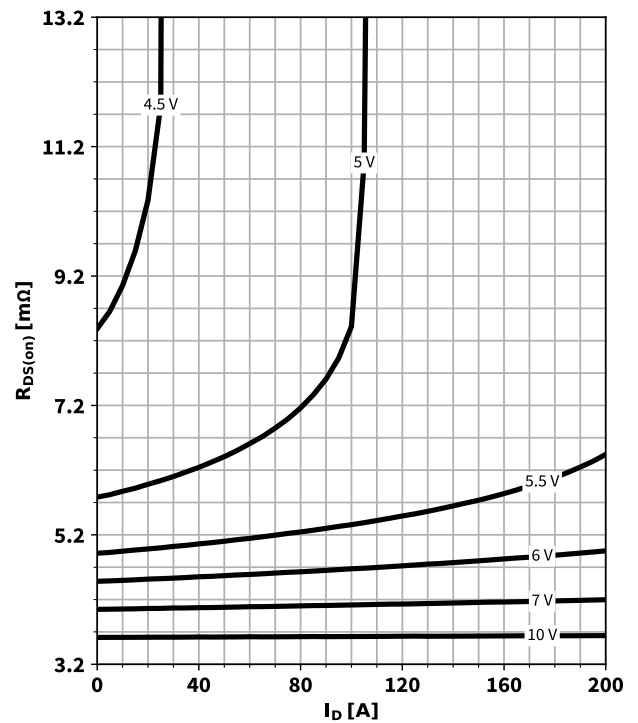
## 5 Typ. output characteristics

$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$



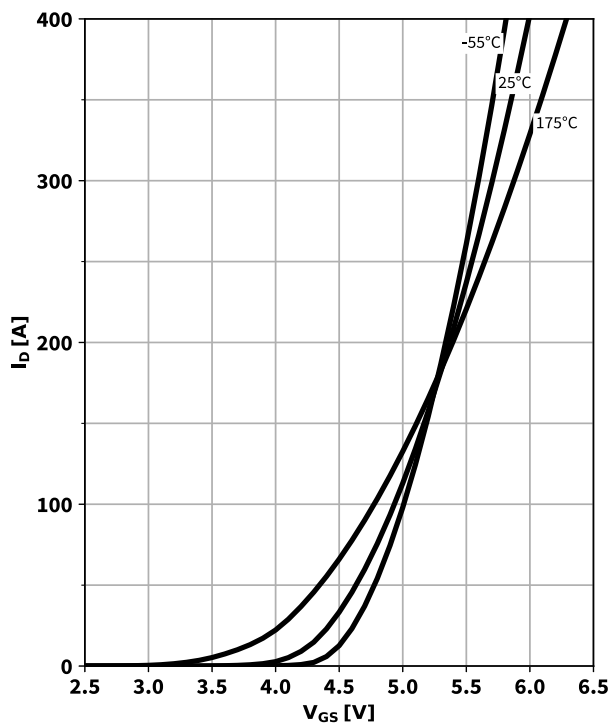
## 6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$



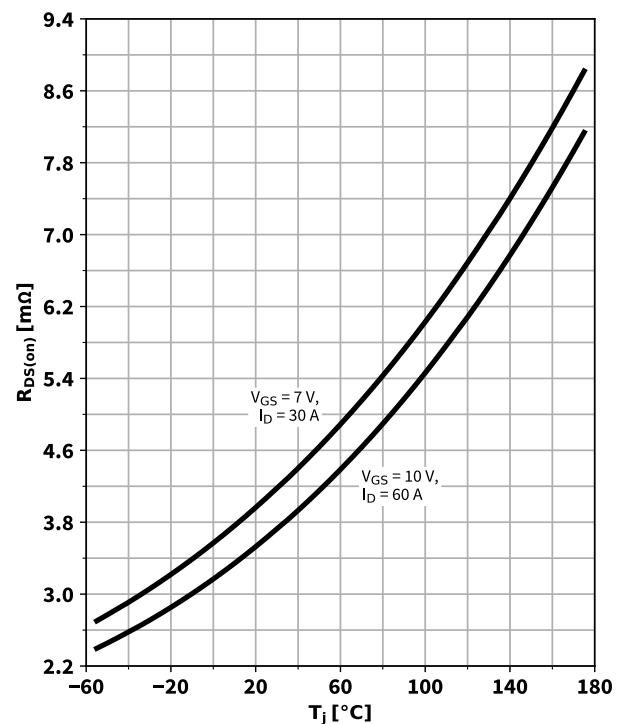
## 7 Typ. transfer characteristics

$I_D = f(V_{GS})$ ;  $V_{DS} = 6\text{ V}$ ; parameter:  $T_j$



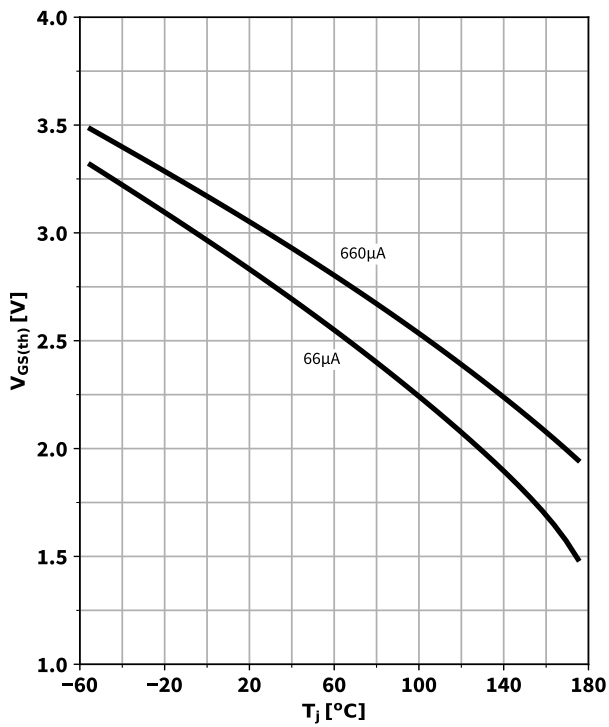
## 8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$ ; parameter:  $I_D$ ,  $V_{GS}$



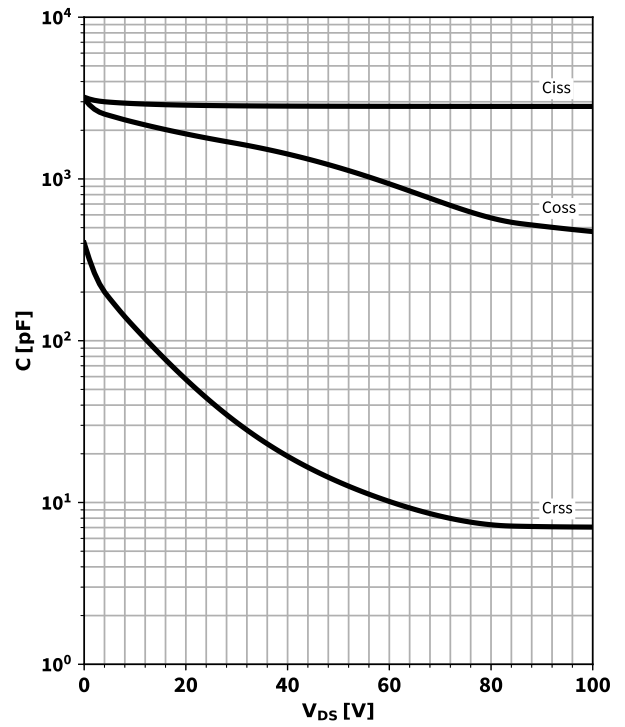
## 9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$



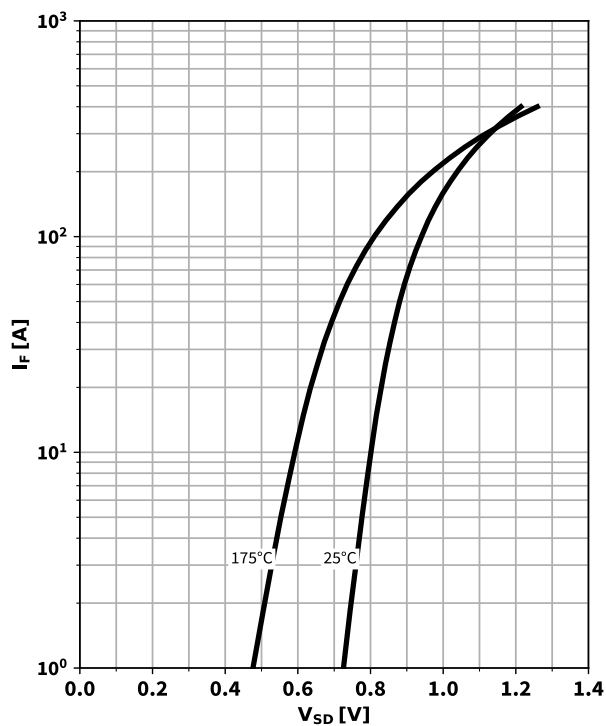
## 10 Typ. capacitances

$C = f(V_{DS})$ ;  $V_{GS} = 0$  V;  $f = 1$  MHz



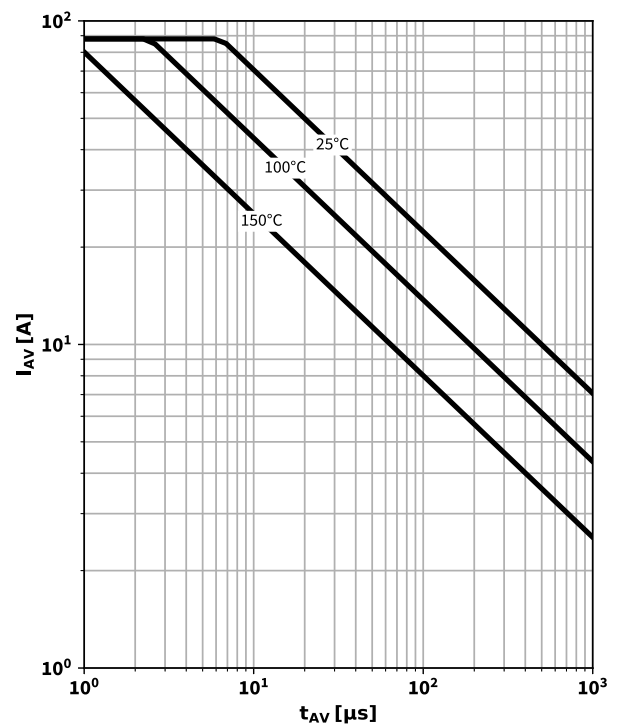
## 11 Typ. forward diode characteristics

$I_F = f(V_{SD})$ ; parameter:  $T_j$



## 12 Typ. avalanche characteristics

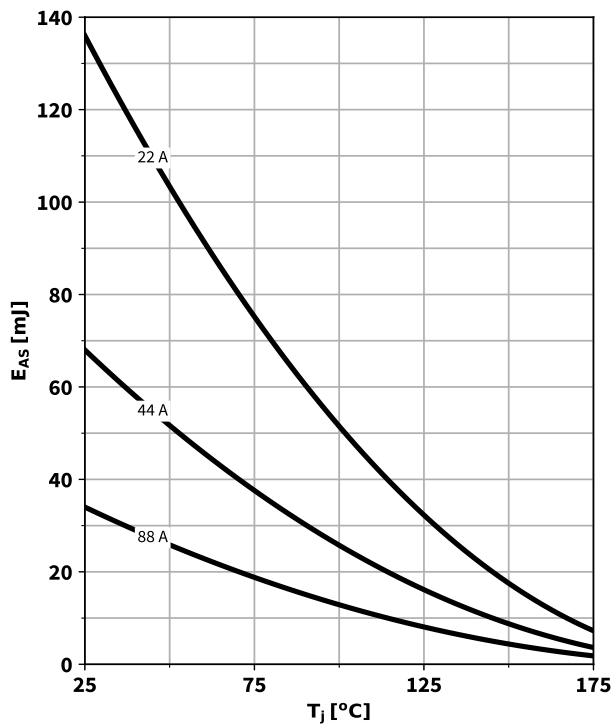
$I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$





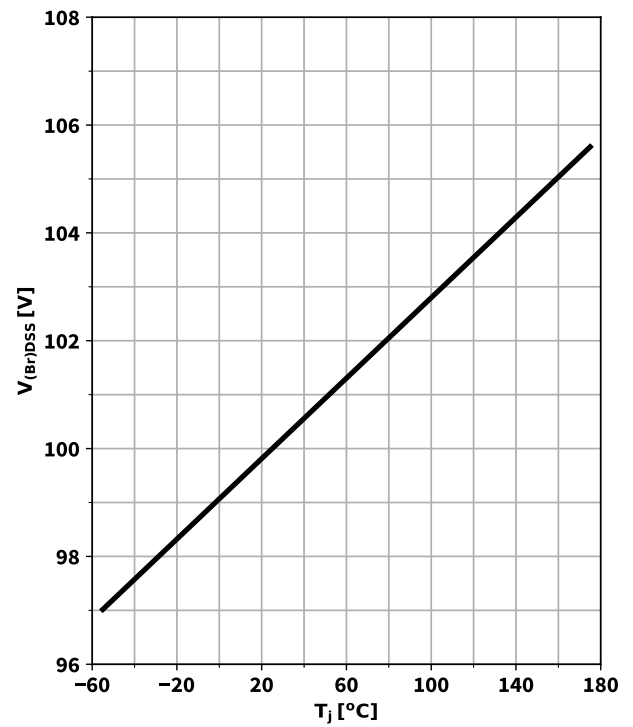
## 13 Typical avalanche energy

$E_{AS} = f(T_j)$ ; parameter:  $I_D$



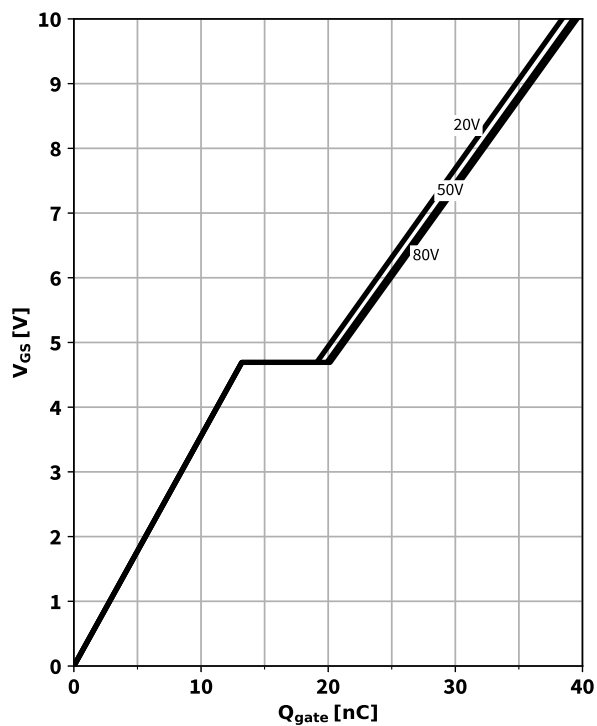
## 14 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$ ;  $I_D = 1$  mA



## 15 Typ. gate charge

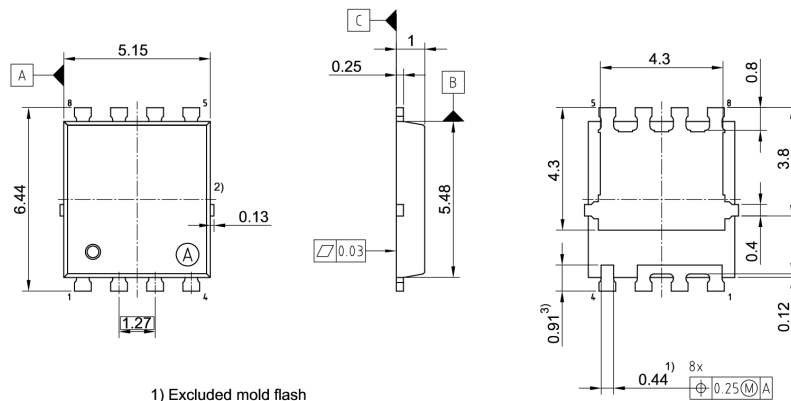
$V_{GS} = f(Q_{gate})$ ;  $I_D = 60$  A pulsed; parameter:  $V_{DD}$



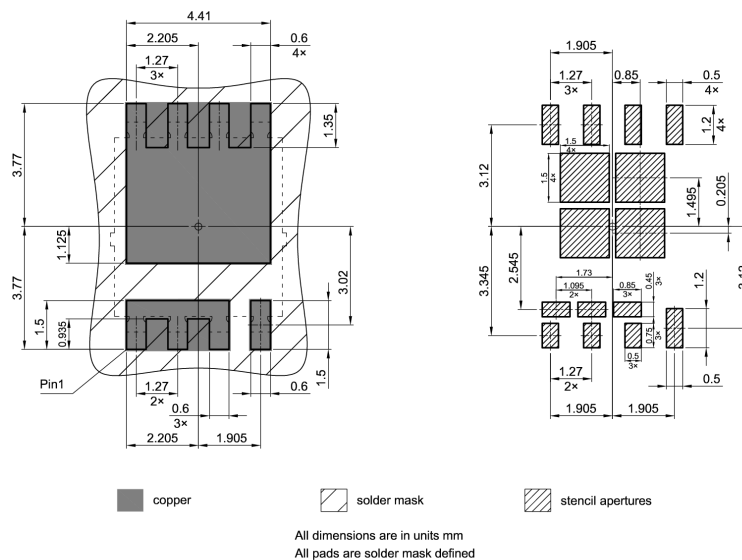
## 16 Gate charge waveforms



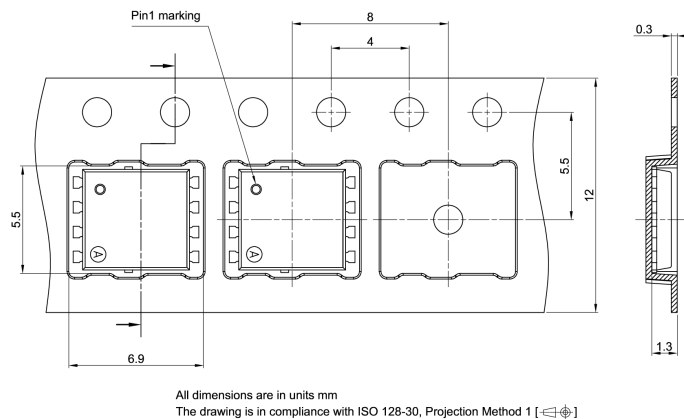
## Package Outline



## Footprint



## Packaging



**Revision History**

Revision	Date	Changes
Revision 1.0	2024-10-14	final data sheet

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**Document reference**

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