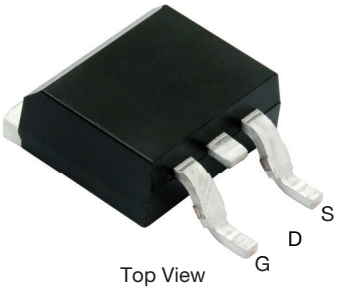
N-Channel 100 V (D-S) MOSFET



FEATURES

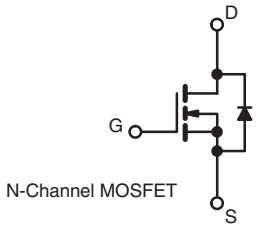
- TrenchFET® power MOSFETs
- 175 °C junction temperature
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Power supply
  - Secondary synchronous rectification
- Industrial
- Primary switch

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0082
Q_g typ. (nC)	97
I_D (A)	90 [d]
Configuration	Single



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free	SUM90N10-8m2P-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 175 °C)	T_C = 25 °C	I_D	90 [d]	A
	T_C = 70 °C		90 [d]	
Pulsed drain current		I_{DM}	240	
Avalanche current		I_{AS}	60	
Single avalanche energy [a]	L = 0.1 mH	E_{AS}	180	mJ
Maximum power dissipation [a]	T_C = 25 °C	P_D	300 [b]	W
	T_A = 25 °C [c]		3.75	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) [c]	R_{thJA}	40	°C/W
Junction-to-case (drain)	R_{thJC}	0.5	

Notes

a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR4 material).
d. Package limited.

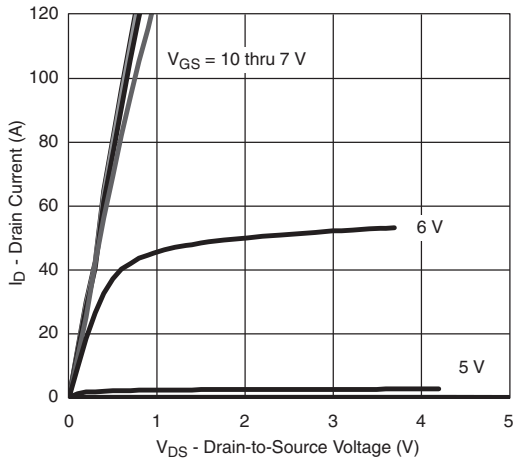
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{DS} = 0 V, I_D = 250 µA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.5	-	4.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 250	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125 °C	-	-	50	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 10 V, V_{GS} = 10 V	70	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.0067	0.0082	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C	-	0.0127	0.0170	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	-	62	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	-	6290	-	pF
Output capacitance	C_{oss}		-	535	-	
Reverse transfer capacitance	C_{rss}		-	182	-	
Total gate charge [c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 85 A	-	97	150	nC
Gate-source charge [c]	Q_{gs}		-	32	-	
Gate-drain charge [c]	Q_{gd}		-	25	-	
Gate resistance	R_g	f = 1 MHz	0.28	1.4	2.8	W
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 0.588 Ω I_D ≅ 85 A, V_{GEN} = 10 V, R_g = 1 Ω	-	23	35	ns
Rise time [c]	t_r		-	17	26	
Turn-off delay time [c]	$t_{d(off)}$		-	34	52	
Fall time [c]	t_f		-	9	18	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C) [b]						
Continuous current	I_S		-	-	85	A
Pulsed current	I_{SM}		-	-	240	
Forward voltage [a]	V_{SD}	I_F = 30 A, V_{GS} = 0 V	-	0.85	1.5	V
Reverse recovery time	t_{rr}	I_F = 75 A, di/dt = 100 A/µs	-	61	100	ns
Peak reverse recovery current	$I_{RM(REC)}$		-	3	4.5	A
Reverse recovery charge	Q_{rr}		-	91	130	nC

Notes

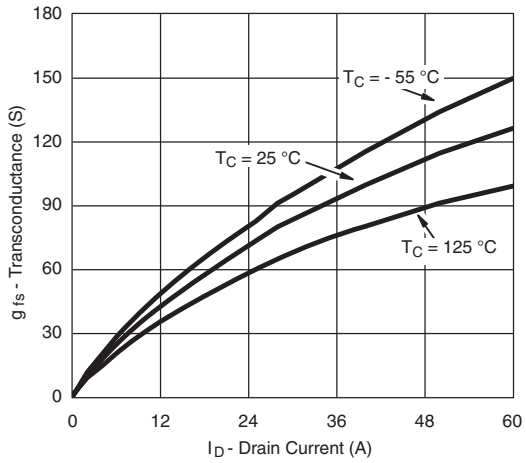
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

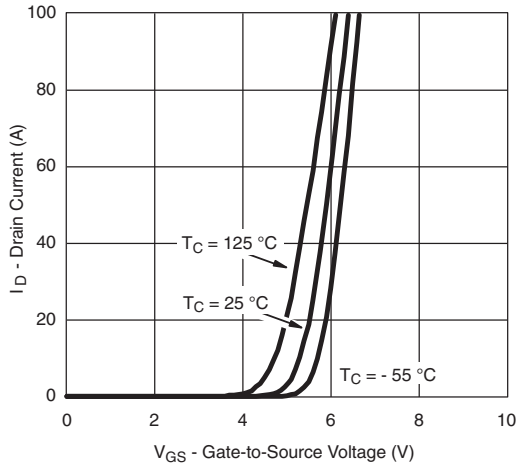
TYPICAL CHARACTERISTICS (25 °C, UNLESS OTHERWISE NOTED)



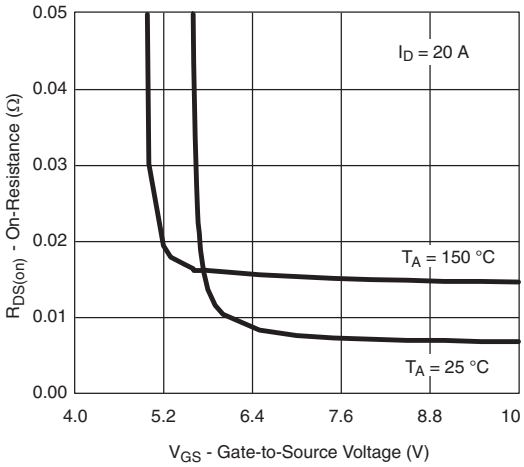
Output Characteristics



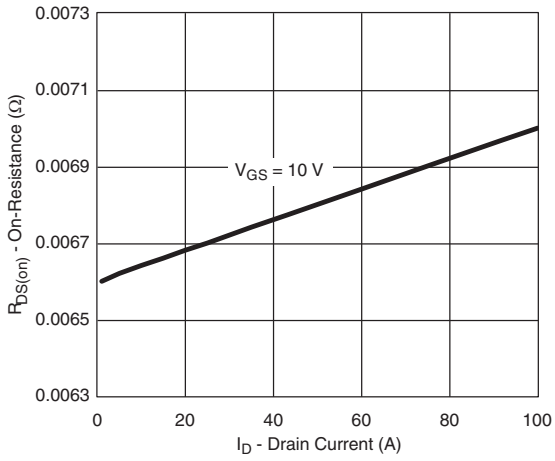
Transconductance



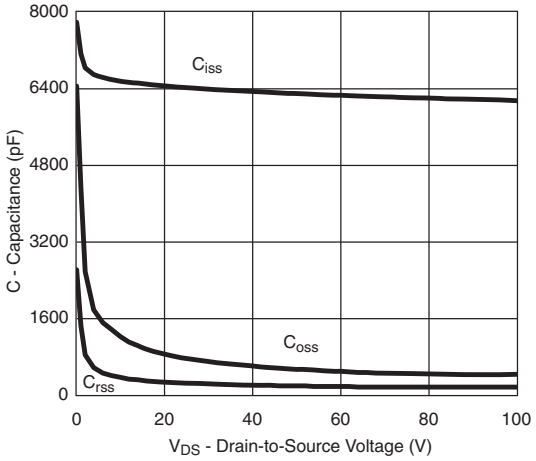
Transfer Characteristics



On-resistance vs. Gate-to-Source Voltage

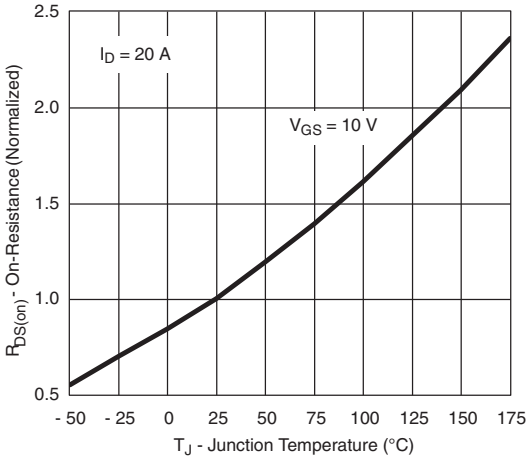


On-Resistance vs. Drain Current

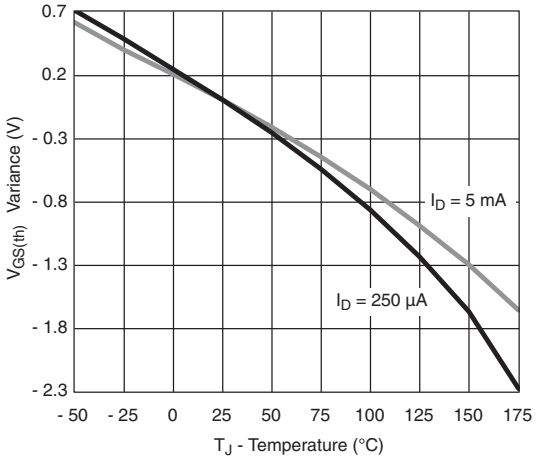


Capacitance

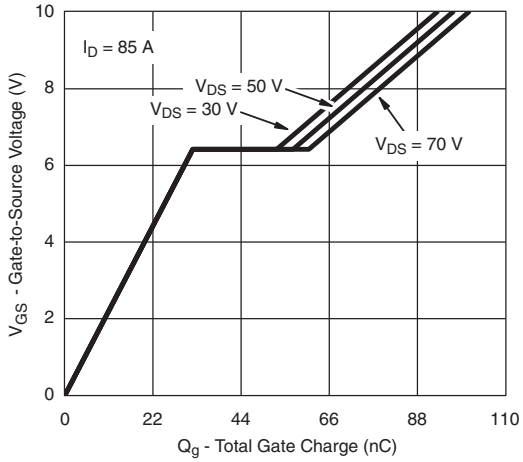
TYPICAL CHARACTERISTICS (25 °C, UNLESS OTHERWISE NOTED)



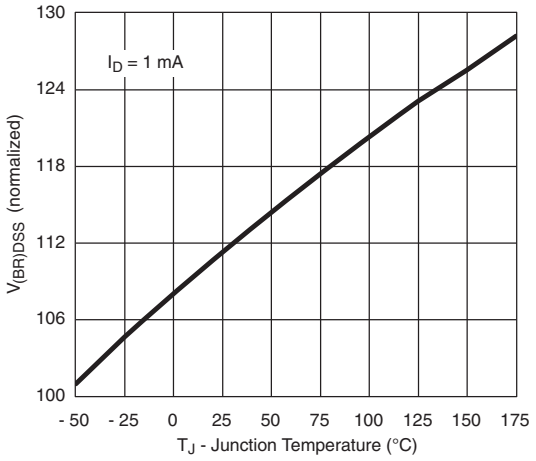
On-Resistance vs. Junction Temperature



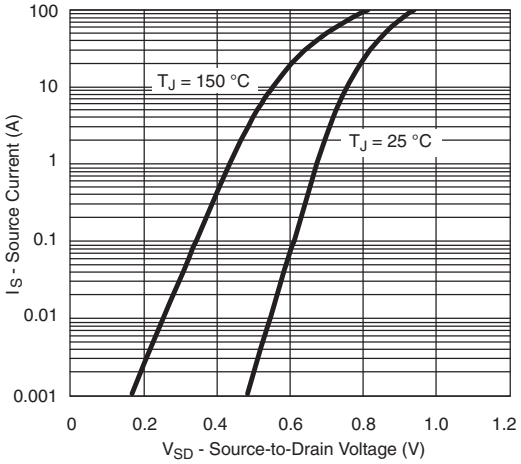
Threshold Voltage



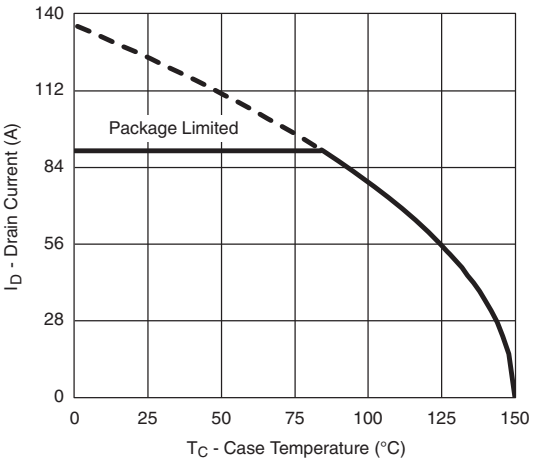
Gate Charge



Drain Source Breakdown vs. Junction Temperature

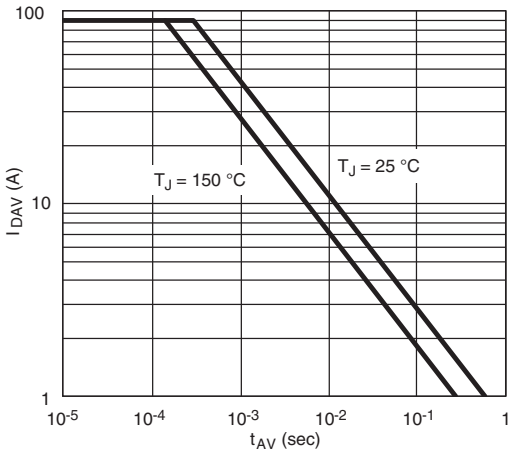


Source-Drain Diode Forward Voltage

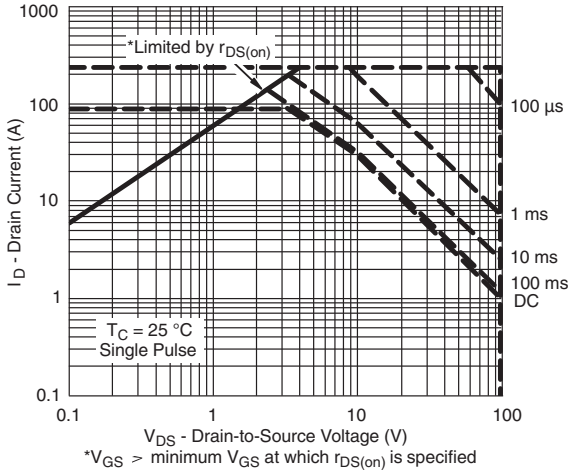


Maximum Drain Current vs. Case Temperature

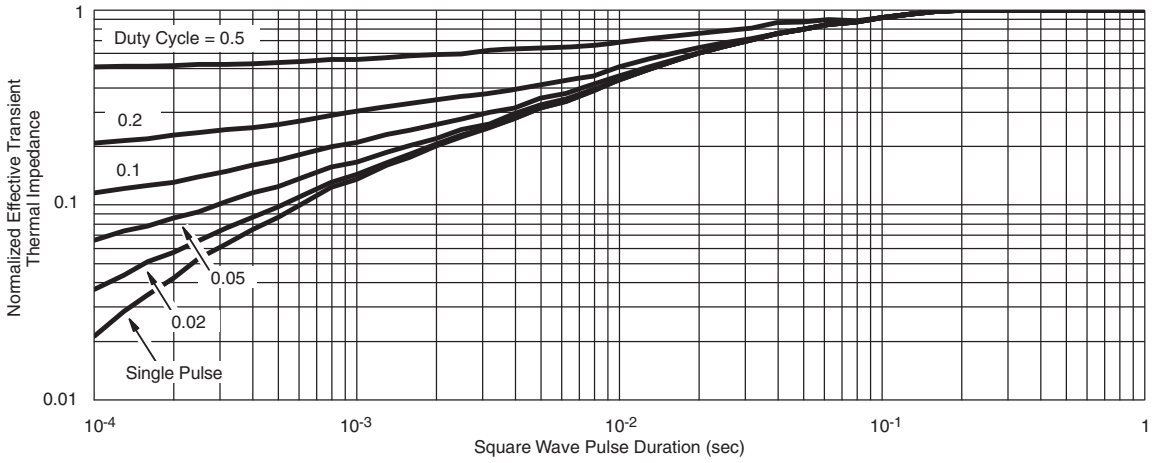
TYPICAL CHARACTERISTICS (25 °C, UNLESS OTHERWISE NOTED)



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area

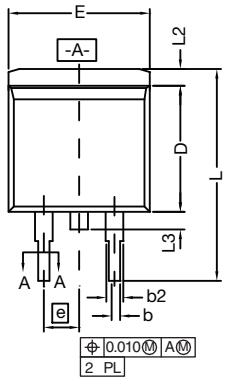


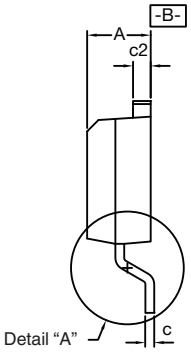
Normalized Thermal Transient Impedance, Junction-to-Case

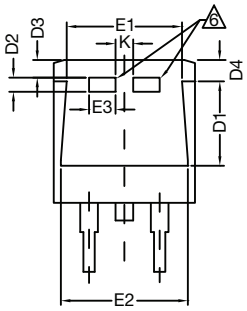
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74643.

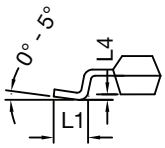
TO-263 (D²PAK): 3-LEAD

VERSION 1: FACILITY CODE = T

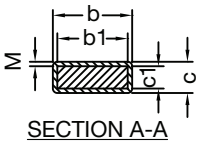








DETAIL A (ROTATED 90°)



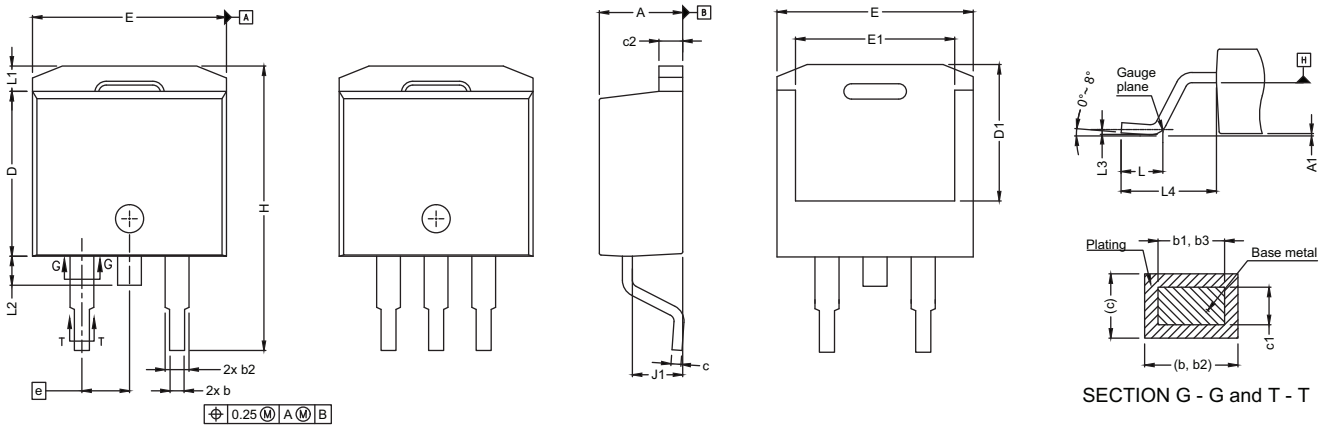
SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

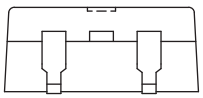
Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

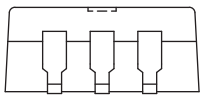
VERSION 2: FACILITY CODE = N



SECTION G - G and T - T



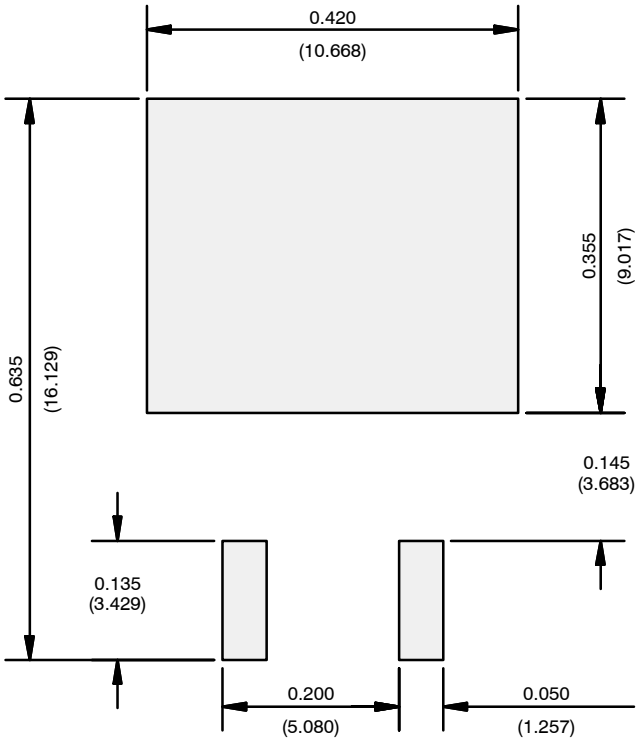
OPTION 1
2 leads



OPTION 2
3 leads

DIM.	MIN.	MAX.
A	4.36	4.56
A1	0	0.25
b	0.70	0.90
b1	0.51	0.89
b2	1.20	1.46
b3	1.17	1.37
c	0.38	0.694
c1	0.38	0.534
c2	1.19	1.34
D	8.60	9.00
D1	6.9	7.5
E	10.15	10.55
E1	8.1	8.7
e	2.54 BSC	
H	15.0	15.6
L	1.9	2.5
L1	-	1.65
L2	-	1.78
L3	0.25 typ.	
L4	4.78	5.28
J1	2.56	2.96
ECN: S24-1080-Rev. L, 28-Oct-2024 DWG: 5843		

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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