

MOSFET – Power, Single N-Channel, STD Gate, SO8FL

40 V, 3.1 mΩ, 94 A

NVMFWS2D9N04XM

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

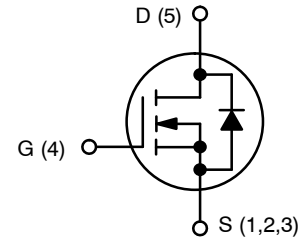
- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

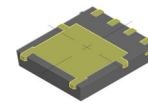
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage		DC	V_{GS}	± 20	V
Continuous Drain Current	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	94	A
		$T_C = 100^{\circ}\text{C}$		66	
Power Dissipation		$T_C = 25^{\circ}\text{C}$	P_D	50	W
Continuous Drain Current $R_{\theta JA}$	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	25	A
		$T_A = 100^{\circ}\text{C}$		18	
Pulsed Drain Current		$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$	I_{DM}	440	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to 175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	42	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 4.6\text{ A}$)			E_{AS}	133	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	3.1 mΩ @ 10 V	94 A

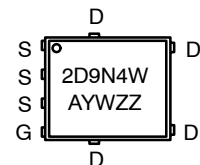


N-CHANNEL MOSFET



DFN5
(SO8FL WF)
CASE 507BA

MARKING DIAGRAM



2D9N4W = Specific Device code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFWS2D9N04XM

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	41.6	

- Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$		2.7	3.1	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 40\text{ μA}, T_J = 25^\circ\text{C}$	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 40\text{ μA}$		-7.2		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$		79.6		S

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1000		pF
Output Capacitance	C_{OSS}			645		
Reverse Transfer Capacitance	C_{RSS}			12.3		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 32\text{ V}, I_D = 50\text{ A}, V_{GS} = 10\text{ V}$		15.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.9		
Gate-to-Source Charge	Q_{GS}			4.8		
Gate-to-Drain Charge	Q_{GD}			3		
Gate Resistance	R_G			1		
		$f = 1\text{ MHz}$				Ω

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}$, $V_{DD} = 32\text{ V}, I_D = 50\text{ A}, R_G = 0\text{ Ω}$		13.1		ns
Rise Time	t_r			4.5		
Turn-Off Delay Time	$t_{d(OFF)}$			19.8		
Fall Time	t_f			3.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}, T_J = 25^\circ\text{C}$		0.84	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 20\text{ A}, T_J = 125^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$, $di/dt = 100\text{ A/μs}, V_{DD} = 32\text{ V}$		107		ns
Charge Time	t_a			38		ns
Discharge Time	t_b			69		ns
Reverse Recovery Time	Q_{RR}			391		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

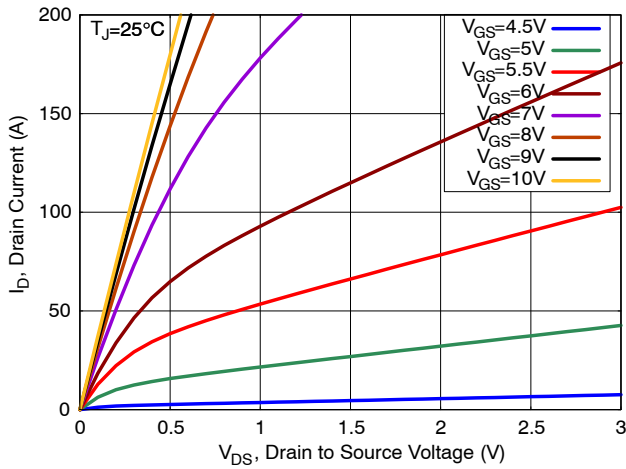


Figure 1. On-Region Characteristics

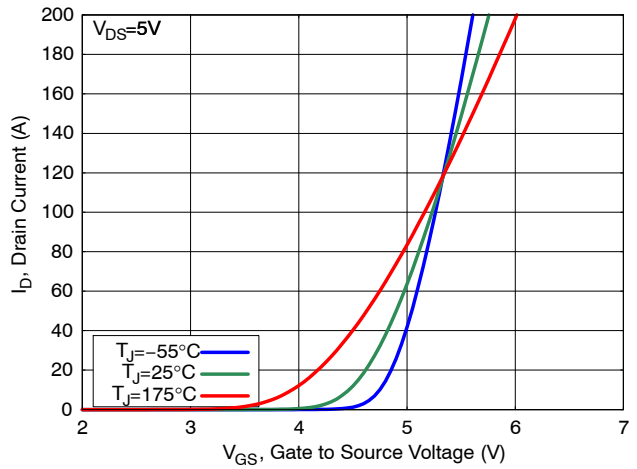


Figure 2. Transfer Characteristics

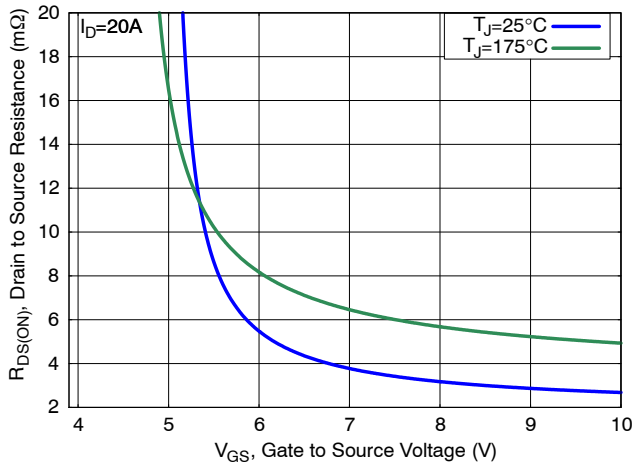


Figure 3. On-Resistance vs. Gate Voltage

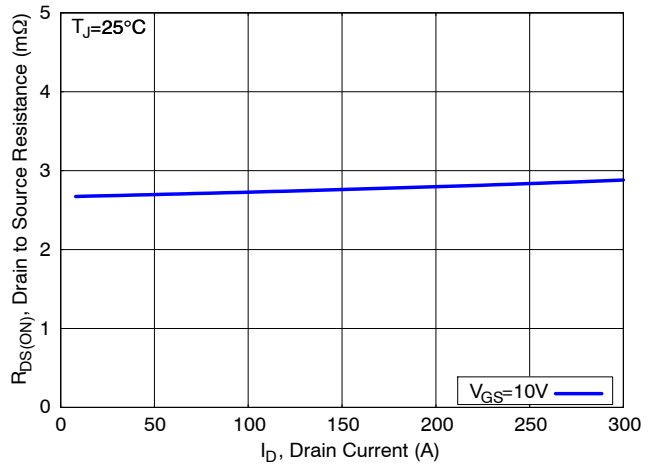


Figure 4. On-Resistance vs. Drain Current

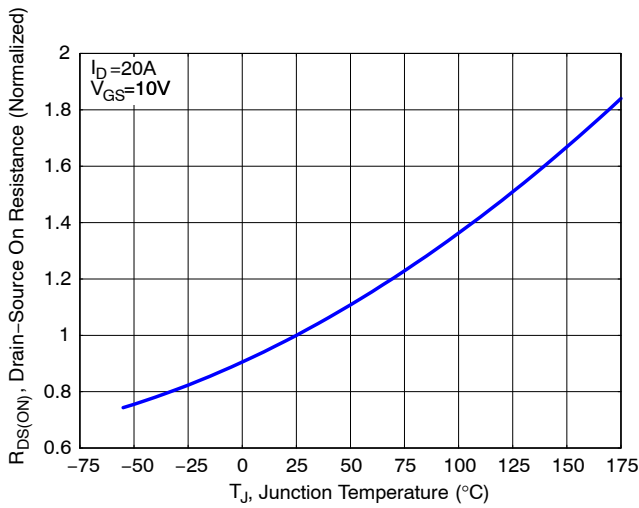


Figure 5. Normalized ON Resistance vs. Junction Temperature

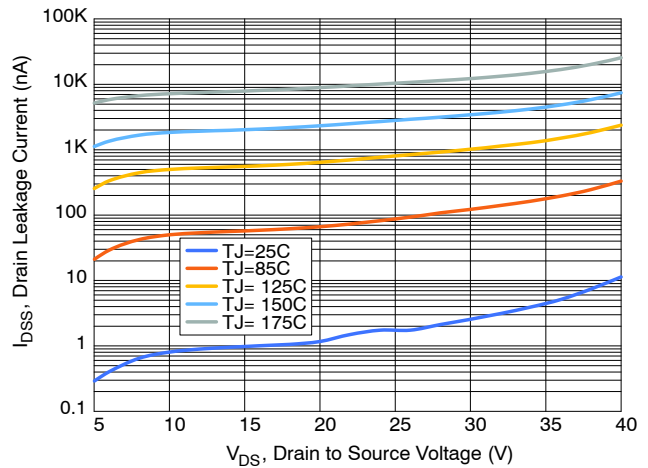


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

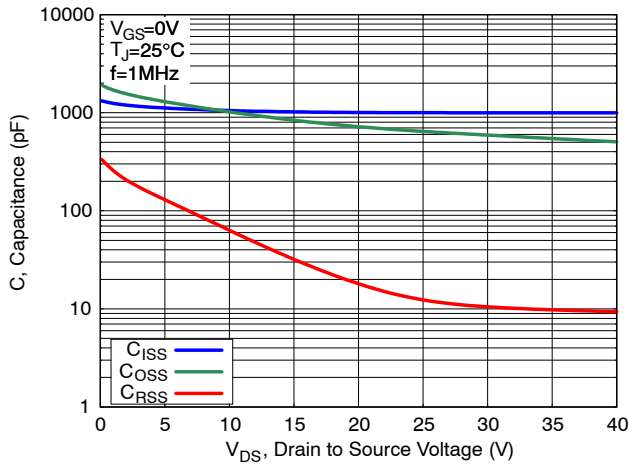


Figure 7. Capacitance Characteristics

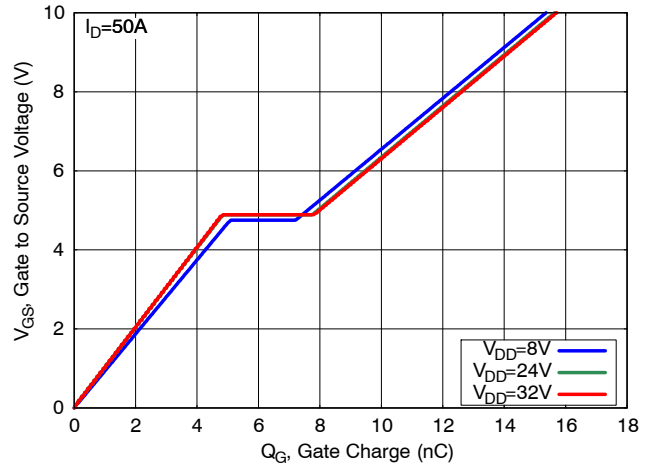


Figure 8. Gate Charge Characteristics

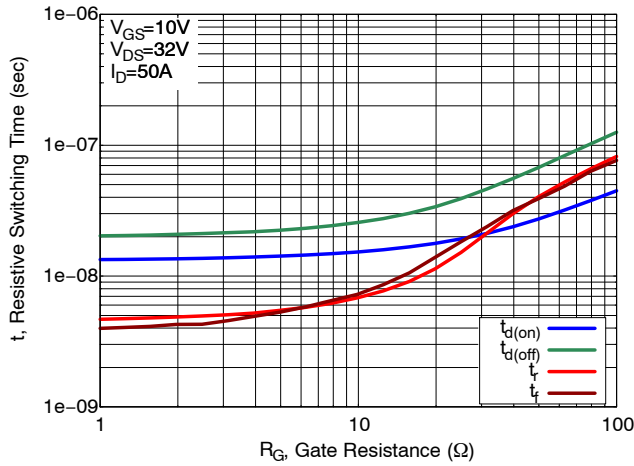


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

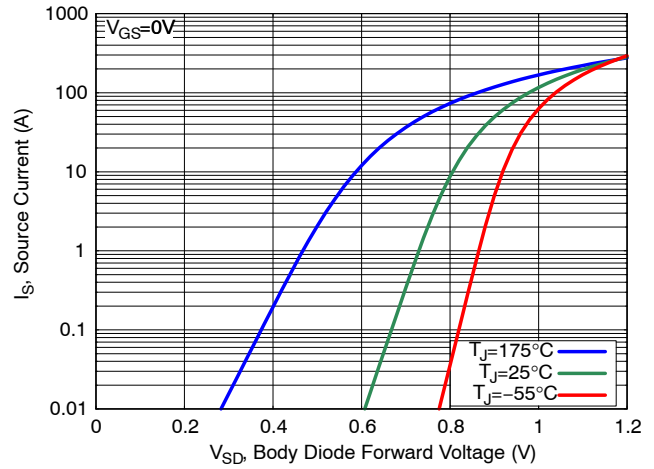


Figure 10. Diode Forward Characteristics

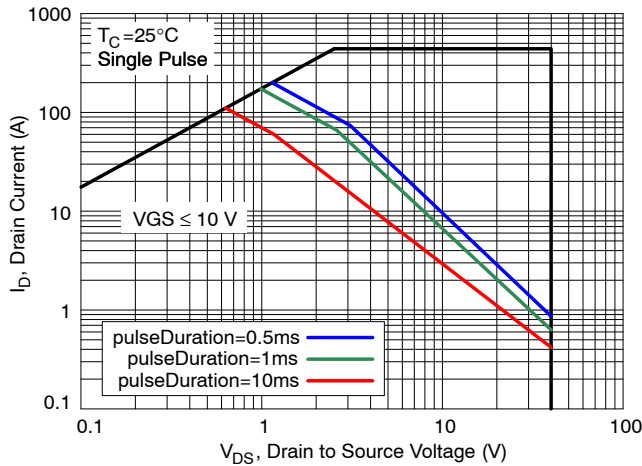


Figure 11. Safe Operating Area (SOA)

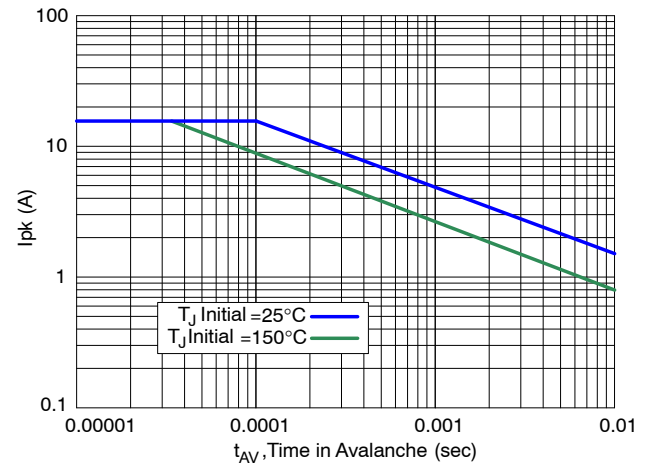


Figure 12. Ipeak vs. Time in Avalanche

NVMFWS2D9N04XM

TYPICAL CHARACTERISTICS

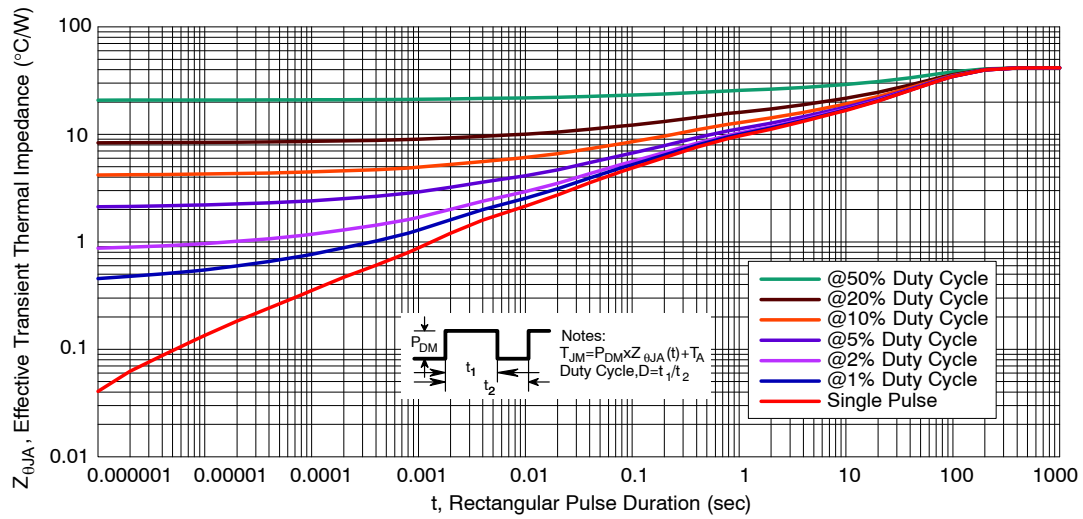
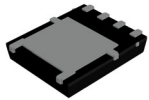


Figure 13. Transient Thermal Response

DEVICE ORDERING INFORMATION

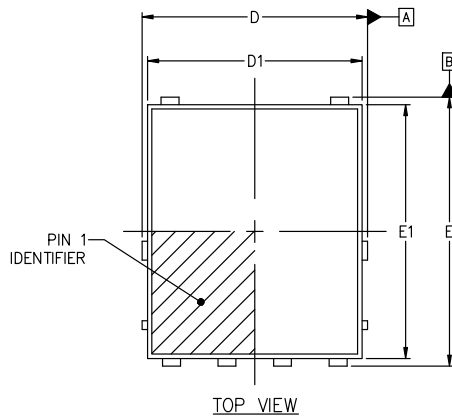
Device	Marking	Package	Shipping [†]
NVMFWS2D9N04XMT1G	2D9N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

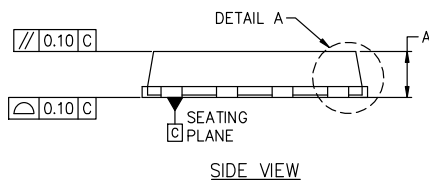


DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

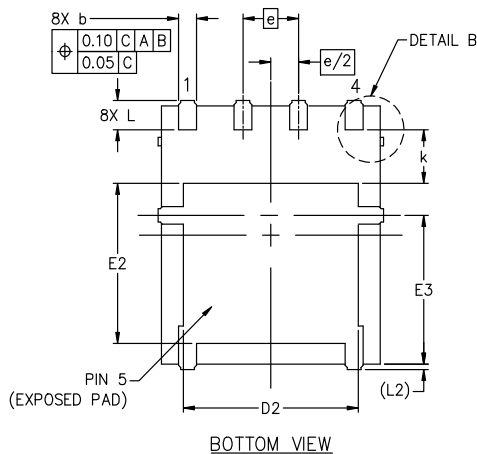
DATE 19 SEP 2024



TOP VIEW



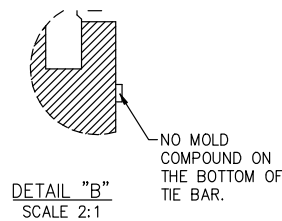
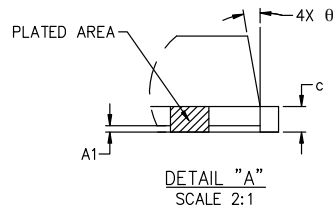
SIDE VIEW



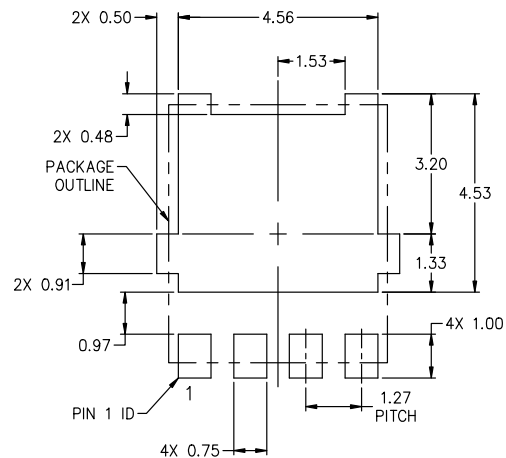
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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