Vishay Siliconix

# N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY					
V <sub>DS</sub> (V)	60				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 10 V	0.0195				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0250				
Q <sub>g</sub> typ. (nC)	5.2				
I <sub>D</sub> (A)	11.3				
Configuration	Single				

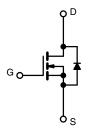
### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



### **APPLICATIONS**

- Synchronous rectification
- Primary side switch
- DC/DC converters
- Power supplies
- · Motor drive control
- · Battery and load switch



N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free and halogen-free	Si4850BDY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	60	
Gate-source voltage		$V_{GS}$	± 20	V
	T <sub>C</sub> = 25 °C		11.3	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 . [	9	
	T <sub>A</sub> = 25 °C	† I <sub>D</sub>	8.4 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C	1	6.8 <sup>a, b</sup>	^
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	40	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		3.8	
	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 25 °C	2.1 <sup>a, b</sup>	
Single pulse avalanche current		I <sub>AS</sub>	15	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	11.3	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		4.5	
	T <sub>C</sub> = 70 °C	1 5	2.8	w
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>a, b</sup>	VV
	T <sub>A</sub> = 70 °C	1	1.6 <sup>a, b</sup>	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	
Soldering recommendations (peak temperature) c		1	260	°C

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum junction-to-ambient <sup>a</sup>	t ≤ 10 s	$R_{thJA}$	38	50	°C ///		
Maximum junction-to-foot (drain)	Steady state	$R_{thJF}$	22	28	°C/W		

### Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. Maximum under steady state conditions is 85 °C/W



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			<u>'</u>		•		
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	33	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4.8	-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	2.8	٧	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA	
Zana and a silvan darka a sanat		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μА	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	10		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10	-	-	Α	
5		V <sub>GS</sub> =10 V, I <sub>D</sub> = 10 A	-	0.0160	0.0195	Ω	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	0.0200	0.0250		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	-	39	-	S	
Dynamic <sup>b</sup>			1	1	•	<u> </u>	
Input capacitance	C <sub>iss</sub>		-	790	-		
Output capacitance	C <sub>oss</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	330	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>		-	14	-	'	
Total gate charge	$Q_g$	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	-	11.1	17	nC	
			-	5.2	8		
Gate-source charge	$Q_{gs}$	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	2.2	-		
Gate-drain charge	$Q_{gd}$		-	1.1	-		
Gate resistance	$R_g$	f = 1 MHz	0.1	0.6	1.2	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	7	15		
Rise time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_L = 6 \Omega, I_D \cong 5 \text{ A},$	-	21	40		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$	-	10	20		
Fall time	t <sub>f</sub>		-	10	20		
Turn-on delay time	t <sub>d(on)</sub>		-	13	25	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, \text{ R}_L = 6 \Omega, \text{ I}_D \cong 5 \text{ A},$	-	25	50	1	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	10	20		
Fall time	t <sub>f</sub>		-	22	45		
<b>Drain-Source Body Diode Characteristi</b>	cs		<u>'</u>		•	·	
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	3.8		
Pulse diode forward current	I <sub>SM</sub>		-	-	40	A	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.79	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	30	60	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>		-	60	120	nC	
Reverse recovery fall time	t <sub>a</sub>	$I_F = 5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	15	-		
Reverse recovery rise time	t <sub>b</sub>		-	15	-	ns	

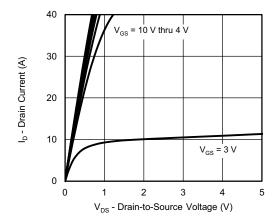
#### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

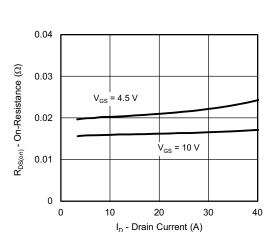
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



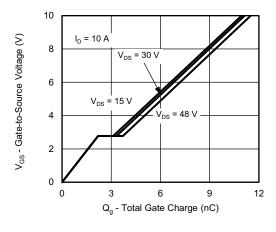
# TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



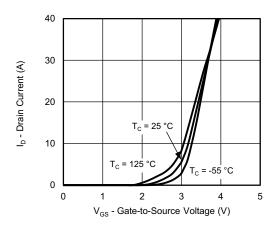
### **Output Characteristics**



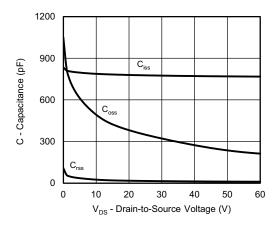
On-Resistance vs. Drain Current and Gate Voltage



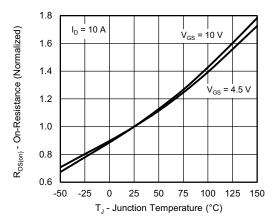
**Gate Charge** 



**Transfer Characteristics** 



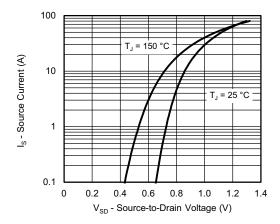
Capacitance



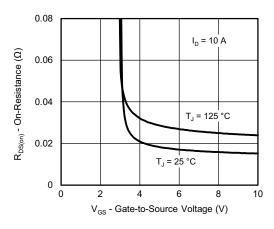
On-Resistance vs. Junction Temperature



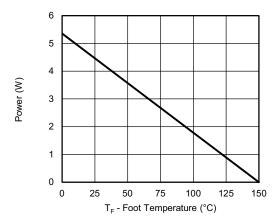
# TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Source-Drain Diode Forward Voltage

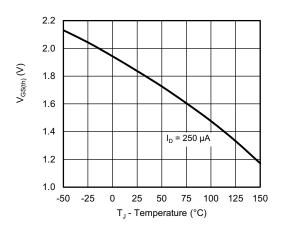


On-Resistance vs. Gate-to-Source Voltage

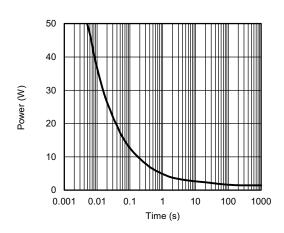


Power, Junction-to-Foot

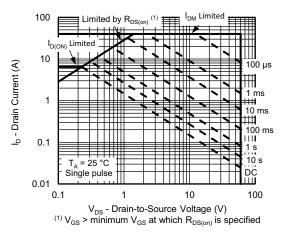
S17-1486-Rev. A, 25-Sep-17



Threshold Voltage



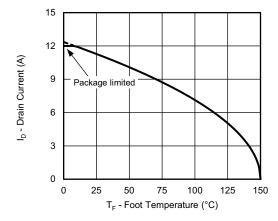
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

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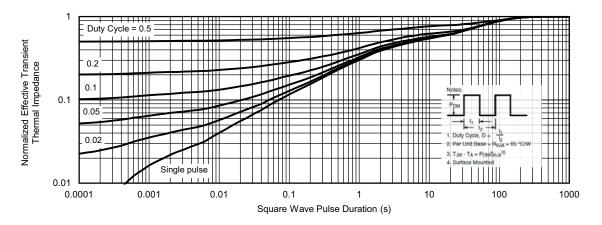
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



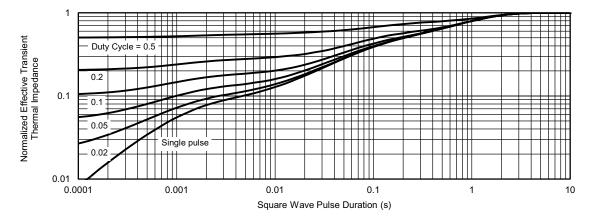
#### Note

a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

### Current Derating a



### Normalized Thermal Transient Impedance, Junction-to-Ambient



### Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg275489">www.vishay.com/ppg275489</a>.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS		INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I. 11-Sep-06					

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



## **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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