

# **MOSFET** – Power, Single, N-Channel

60 V, 2.0 mΩ, 185 A

## NTMYS2D2N06CL

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage	Э		V <sub>GS</sub>	±20	V
Continuous Drain	Steady State			185	Α
Current R <sub>θJC</sub> (Notes 1, 2, 3)	State	T <sub>C</sub> = 100°C		131	
Power Dissipation		T <sub>C</sub> = 25°C	$P_{D}$	134	W
R <sub>θJC</sub> (Notes 1, 2)		T <sub>C</sub> = 100°C		67	
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	31	Α
Current R <sub>θJA</sub> (Notes 1, 2, 3)	State	State T <sub>A</sub> = 100°C		22	
Power Dissipation	T <sub>A</sub> = 25°C		$P_{D}$	3.9	W
R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 100°C		1.9	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I <sub>DM</sub>	900	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	ç
Source Current (Body Diode)			I <sub>S</sub>	112	Α
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, I <sub>L(pk)</sub> = 11.9 A)			E <sub>AS</sub>	941	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

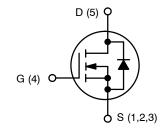
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.12	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	39	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
60 V	2.0 mΩ @ 10 V	10F A
60 V	2.7 mΩ @ 4.5 V	185 A



**N-CHANNEL MOSFET** 



#### LFPAK4 CASE 760AB



2D6N06CL = Specific Device Code A = Assembly Location

WL = Wafer Lot
 Y = Year
 W = Work Week

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS				ı	1		1
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu$	A	60	_	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /	- 1		-	26	-	mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C	-	_	10	μΑ
		V <sub>DS</sub> = 60 V	T <sub>J</sub> = 125°C	-	_	100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V	V	-	_	100	nA
ON CHARACTERISTICS (Note 4)	<u></u>			ı			1
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 180 I	uА	1.2	_	2.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-	-5.3	-	mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 50 A	-	1.6	1.9	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 50 A	-	2.1	2.6	
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A		-	135	-	S
CHARGES, CAPACITANCES & GATE RESIS	STANCE						1
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz,	V <sub>DS</sub> = 25 V	_	4850	-	pF
Output Capacitance	Coss			_	2450	-	
Reverse Transfer Capacitance	C <sub>RSS</sub>			-	25	-	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 50 A		_	31	-	nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 50 A		_	69	-	1
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 50 A		_	6.3	-	1
Gate-to-Source Charge	$Q_{GS}$			_	11.5	-	1
Gate-to-Drain Charge	$Q_{GD}$			_	7.6	-	1
Plateau Voltage	$V_{GP}$			-	2.7	-	V
SWITCHING CHARACTERISTICS (Note 5)	•				•		
Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V,		-	13	-	ns
Rise Time	t <sub>r</sub>	$I_D = 50 \text{ A}, R_G = 2.5 \Omega$		-	20	-	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			-	53	-	
Fall Time	t <sub>f</sub>			-	9.4	-	
DRAIN-SOURCE DIODE CHARACTERISTIC	cs				•		
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C	-	0.8	1.2	V
		I <sub>S</sub> = 50 A	T <sub>J</sub> = 125°C	-	0.7	-	1
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dIS/dt = 20 A/μs,		-	64	-	ns
Charge Time	t <sub>a</sub>	I <sub>S</sub> = 50 A		-	40	-	
Discharge Time	t <sub>b</sub>			-	24	-	
Reverse Recovery Charge	Q <sub>RR</sub>			-	84	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**

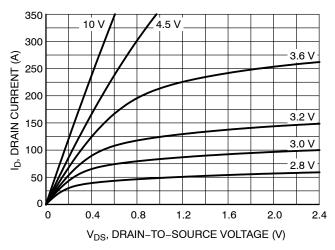


Figure 1. On-Region Characteristics

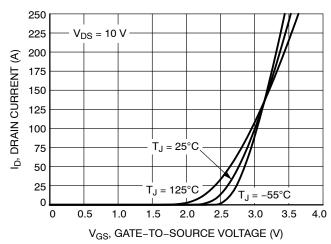


Figure 2. Transfer Characteristics

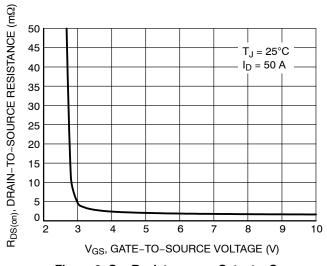


Figure 3. On-Resistance vs. Gate-to-Source Voltage

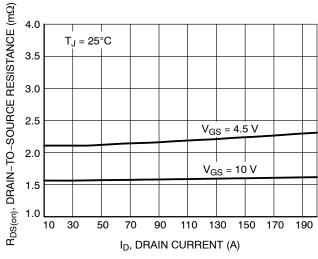


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

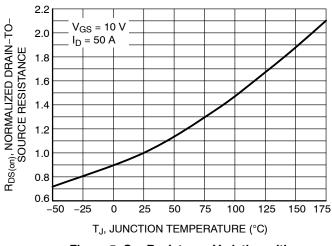


Figure 5. On–Resistance Variation with Temperature

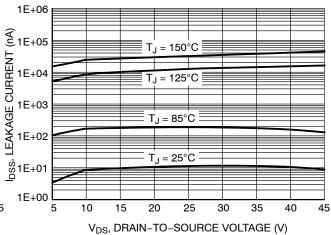


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**

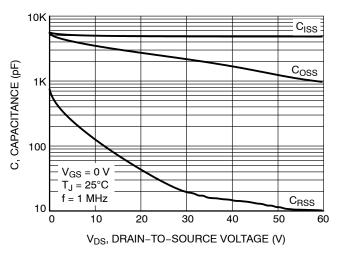


Figure 7. Capacitance Variation

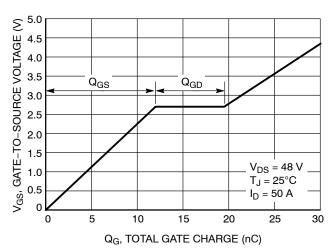


Figure 8. Gate-to-Source Voltage vs. Total Charge

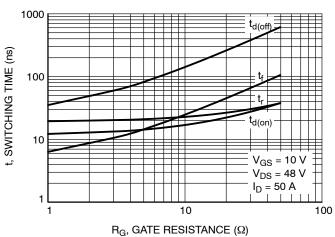


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

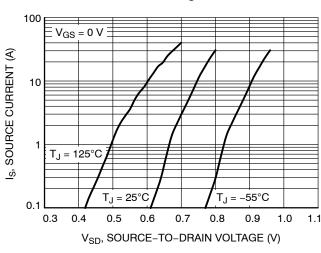


Figure 10. Diode Forward Voltage vs. Current

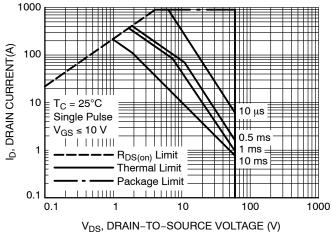


Figure 11. Maximum Rated Forward Biased Safe Operating Area

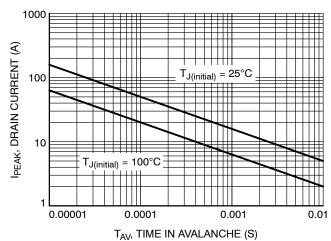


Figure 12. Maximum Drain Current vs. Time in Avalanche

#### **TYPICAL CHARACTERISTICS**

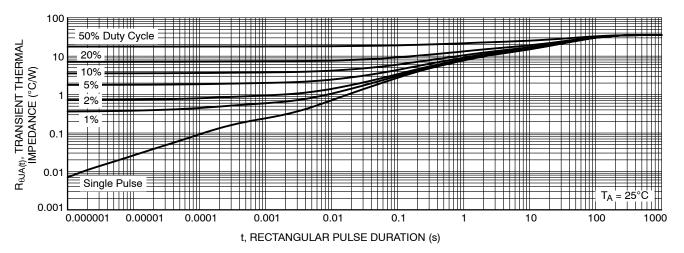


Figure 13. Thermal Response

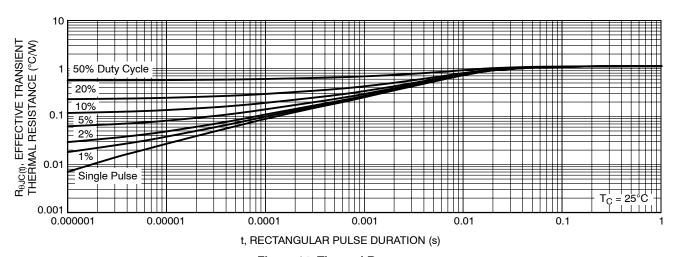


Figure 14. Thermal Response

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTMYS2D2N06CLTWG	2D2N06CL	LFPAK4 (Pb-Free)	3,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





**DATE 22 MAY 2024** 





#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
- 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.



0.70		-   1.27   -	
RECOM	IMENDI	ED LAND	PATTERN

1.30

1.06

0.60

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

# GENERIC MARKING DIAGRAM\*

**BOTTOM VIEW** 

(D8)

XXXXXX XXXXXX AWLYW XXXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot Y = Year W = Work Week

MILLIMETER						
DIM	MIN	NOM	MAX			
Α	1.10	1.20	1.30			
A1	0.00	0.08	0.15			
A2	1.10	1.15	1.20			
А3	C	).25 BSC	)			
b	0.40	0.45	0.50			
b2	3.80	4.10	4.40			
b4	0.45	0.55	0.65 0.25			
C	0.19	0.22	0.25			
c2	0.19	0.22	0.25			
D	4	4.15 BS0				
D1	3.80	4.00	4.20			
D2	3.00	3.10	3.20			
D3	0.30	0.40	0.50			
D4	0.90	1.00	1.10			
D5	0.70	0.80	0.90			
D6	0.55	0.65	0.75			
D7		0.31 REI				
D8	(	0.40 REF				
Ε	4	4.90 BS	2			
E1	4.85	4.95	5.05			
E2	3.10	3.20	3.30			
E3	0.00	0.10	0.20			
E4	2.00	2.10	2.20			
е	1.27 BSC					
e/2	0.635 BSC					
e1	0.40 REF					
Н	6.00	6.15	6.30			
L	0.50	0.70	0.90			
L1	0.80	0.90	1.00			
L2	1.10 REF					
θ	0°	4°	8°			

## DOCUMENT NUMBER: 98

(D7)

98AON82777G

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**DESCRIPTION:** LFPAK4 4.90x4.15x1.15MM, 1.27P

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