

MOSFETs Silicon N-channel MOS (U-MOSVIII-H)

# TK56E12N1

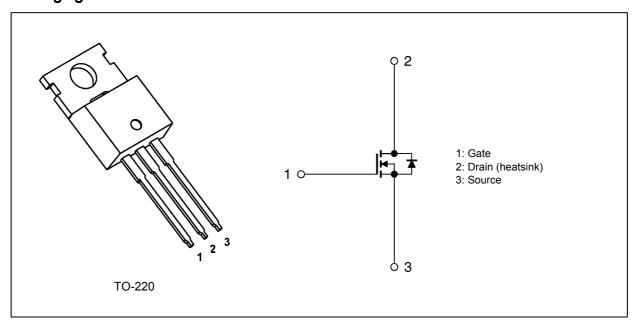
#### 1. Applications

• Switching Voltage Regulators

#### 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 5.8 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (2) Low leakage current:  $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 120 \text{ V)}$
- (3) Enhancement mode:  $V_{th}$  = 2.0 to 4.0 V ( $V_{DS}$  = 10 V,  $I_{D}$  = 1.0 mA)

#### 3. Packaging and Internal Circuit



# 4. Absolute Maximum Ratings (Note) (T<sub>a</sub> = 25°C unless otherwise specified)

Characterist	ics		Symbol	Rating	Unit
Drain-source voltage			$V_{DSS}$	120	V
Gate-source voltage			V <sub>GSS</sub>	±20	
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I <sub>D</sub>	112	Α
Drain current (DC)		(Note 1), (Note 3)	I <sub>D</sub>	56	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I <sub>DP</sub>	219	]
Power dissipation	(T <sub>c</sub> = 25°C)		$P_{D}$	168	W
Single-pulse avalanche energy		(Note 4)	E <sub>AS</sub>	110	mJ
Avalanche current			I <sub>AR</sub>	56	Α
Channel temperature			T <sub>ch</sub>	150	°C
Storage temperature			T <sub>stg</sub>	-55 to 150	1

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



#### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R <sub>th(ch-c)</sub>	0.74	°C/W
Channel-to-ambient thermal resistance	R <sub>th(ch-a)</sub>	83.3	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100 A.

Note 3: Device mounted with heatsink so that  $R_{th(ch-a)}$  becomes 2.77°C/W.

Note 4:  $V_{DD}$  = 80 V,  $T_{ch}$  = 25°C (initial), L = 34.4  $\mu H,\ I_{AR}$  = 56 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



#### 6. Electrical Characteristics

# 6.1. Static Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$		_	±0.1	μΑ
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	-	-	10	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	120	_	_	V
Drain-source breakdown voltage (Note 5)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	90	_	_	
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA	2.0	_	4.0	
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 28 A		5.8	7.0	mΩ

Note 5: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

# 6.2. Dynamic Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	4200		pF
Reverse transfer capacitance	C <sub>rss</sub>		_	19	_	
Output capacitance	C <sub>oss</sub>			650		
Gate resistance	r <sub>g</sub>	_	_	2.1		Ω
Switching time (rise time)	t <sub>r</sub>	See Figure 6.2.1	_	20	_	ns
Switching time (turn-on time)	t <sub>on</sub>		_	45	_	
Switching time (fall time)	t <sub>f</sub>		_	23	_	
Switching time (turn-off time)	t <sub>off</sub>		_	73	_	

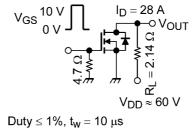


Fig. 6.2.1 Switching Time Test Circuit

# 6.3. Gate Charge Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 96 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 56 \text{ A}$	ı	69	1	nC
Gate-source charge 1	Q <sub>gs1</sub>			25		
Gate-drain charge	$Q_{gd}$		_	19	_	
Gate switch charge	$Q_{SW}$		_	29	_	

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# 6.4. Source-Drain Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 6)	I <sub>DR</sub>	_	_	_	56	Α
Reverse drain current (pulsed)	(Note 6)	I <sub>DRP</sub>	_	_	_	219	
Diode forward voltage		$V_{DSF}$	I <sub>DR</sub> = 56 A, V <sub>GS</sub> = 0 V	_	_	-1.2	V
Reverse recovery time	(Note 7)	t <sub>rr</sub>	I <sub>DR</sub> = 56 A, V <sub>GS</sub> = 0 V	_	86	_	ns
Reverse recovery charge	(Note 7)	Q <sub>rr</sub>	-dl <sub>DR</sub> /dt = 100 A/μs	_	210		nC

Note 6: Ensure that the channel temperature does not exceed 150°C.

Note 7: Ensure that  $V_{DS}$  peak does not exceed  $V_{DSS}$ .

### 7. Marking

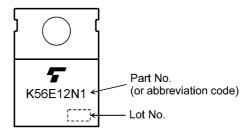
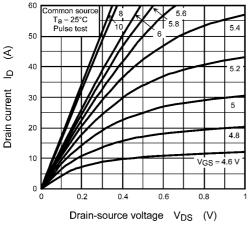


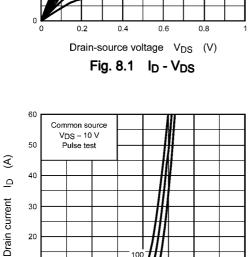
Fig. 7.1 Marking

20

10

#### 8. Characteristics Curves (Note)





Gate-source voltage V<sub>GS</sub> Fig. 8.3 I<sub>D</sub> - V<sub>GS</sub>

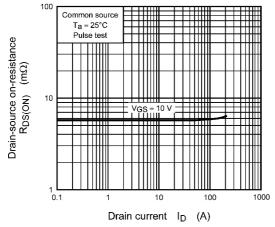


Fig. 8.5 R<sub>DS(ON)</sub> - I<sub>D</sub>

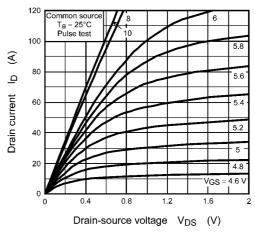


Fig. 8.2 I<sub>D</sub> - V<sub>DS</sub>

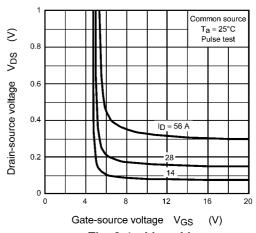


Fig. 8.4 V<sub>DS</sub> - V<sub>GS</sub>

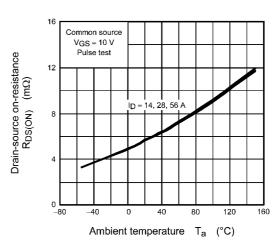


Fig. 8.6 R<sub>DS(ON)</sub> - T<sub>a</sub>

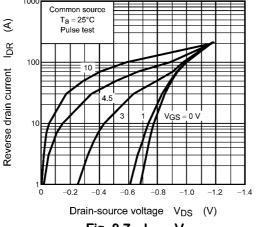


Fig. 8.7 IDR - VDS

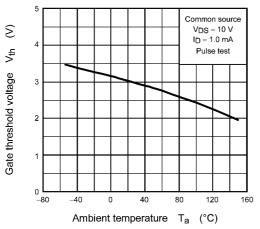
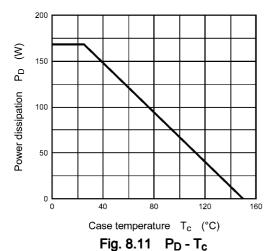


Fig. 8.9 V<sub>th</sub> - T<sub>a</sub>



(Guaranteed Maximum)

10000

1000

1000

1000

Coss

Coss

Coss

Common source

VGS = 0 V

f = 1 MHz

Ta = 25°C

Coss

Drain-source voltage VDS (V)

Fig. 8.8 Capacitance - V<sub>DS</sub>

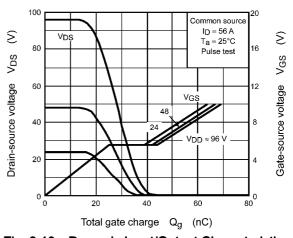


Fig. 8.10 Dynamic Input/Output Characteristics

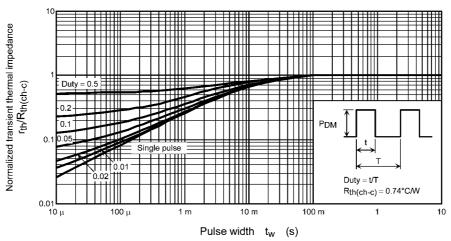


Fig. 8.12 r<sub>th</sub>/R<sub>th(ch-c)</sub> - t<sub>w</sub> (Guaranteed Maximum)

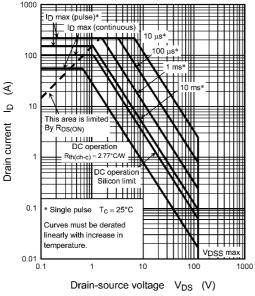


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

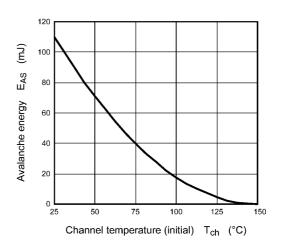


Fig. 8.14 E<sub>AS</sub> - T<sub>ch</sub> (Guaranteed Maximum)

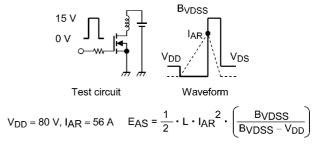


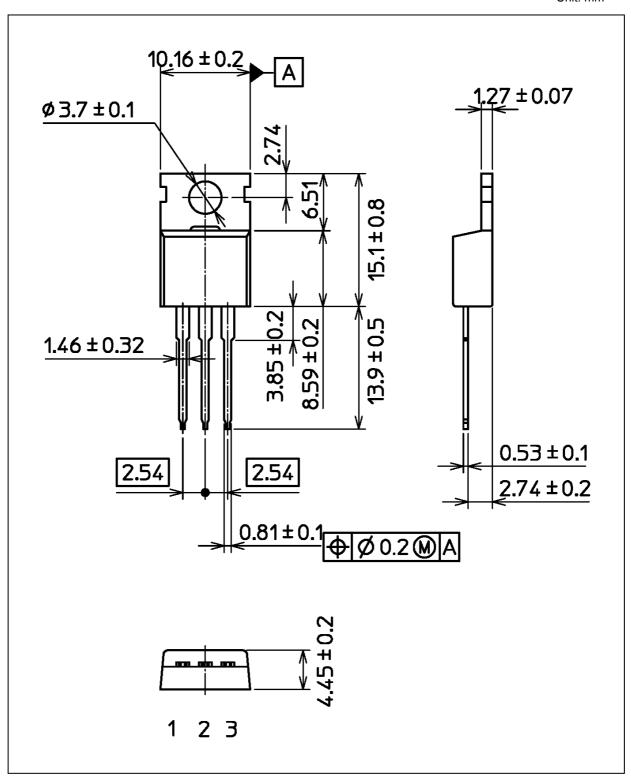
Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



# **Package Dimensions**

Unit: mm



Weight: 1.93 g (typ.)

	Package Name(s)
TOSHIBA: 2-10X1A	
Nickname: TO-220	



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