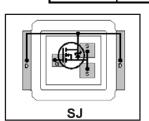
DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

V _{DSS}	V _{GS}	R _{DS(on)}
100V max	±20V max	28mΩ@ 10V
Q _{g tot}	\mathbf{Q}_{gd}	$V_{gs(th)}$
14nC	4.8nC	4.0V





• RoHS Compliant, Halogen-Free 2

- Lead-Free (Qualified up to 260°C Reflow) ①
- Application Specific MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)

SH	SJ	SP	MZ	MN			

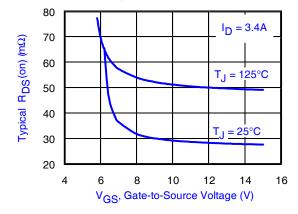
Description

The IRF6645PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an Micro8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note <u>AN-1035</u> is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6645PbF is optimized for primary side bridge topologies in isolated DC-DC applications, for wide range universal input Telecom applications (36V - 75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	100	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V ③	5.7	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V ③	4.5	Α
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ④	25	
I _{DM}	Pulsed Drain Current ®	45	
E _{AS}	Single Pulse Avalanche Energy ®	29	mJ
I _{AR}	Avalanche Current ©	3.4	Α



 $\textbf{Fig 1.} \ \ \textbf{Typical On-Resistance vs. Gate Voltage}$

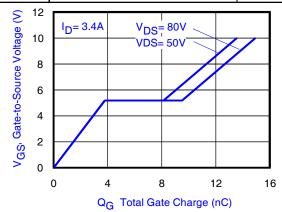


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- 3 Surface mounted on 1 in. square Cu board, steady state.
- $\ \, \mbox{$\oplus$} \mbox{$\mathsf{T}_{\mathbb{C}}$ measured with thermocouple mounted to top (Drain) of part.}$
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- © Starting $T_J = 25$ °C, L = 5.0mH, $R_G = 25\Omega$, $I_{AS} = 3.4$ A.



Electrical Characteristic @ $T_J = 25$ °C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.12		V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance		28	35	mΩ	V _{GS} = 10V, I _D = 5.7A ⑦
$V_{GS(th)}$	Gate Threshold Voltage	3.0		4.9	V	$V_{DS} = V_{GS}$, $I_D = 50\mu A$
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Coefficient		-12		mV/°C	
I _{DSS}	Drain-to-Source Leakage Current			20	μΑ	$V_{DS} = 100V, V_{GS} = 0V$
				250		$V_{DS} = 80V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V _{GS} = -20V
gfs	Forward Transconductance	7.4			S	$V_{DS} = 10V, I_{D} = 3.4A$
Q_g	Total Gate Charge		14	20		
Q _{gs1}	Pre-Vth Gate-to-Source Charge		3.1			$V_{DS} = 50V$
Q _{gs2}	Post-Vth Gate-to-Source Charge		8.0		nC	V _{GS} = 10V
Q _{gd}	Gate-to-Drain Charge		4.8	7.2		$I_D = 3.4A$
Q_{godr}	Gate Charge Overdrive		5.3			See Fig. 15
Q_{sw}	Switch Charge (Q _{gs2} + Q _{gd})		5.6			
Q _{oss}	Output Charge		7.2		nC	V _{DS} = 16V, V _{GS} = 0V
R_G	Gate Resistance		1.0		Ω	
t _{d(on)}	Turn-On Delay Time		9.2			$V_{DD} = 50V, V_{GS} = 10V$ ⑦
t _r	Rise Time		5.0			$I_D = 3.4A$
$t_{d(off)}$	Turn-Off Delay Time		18		ns	$R_G=6.2\Omega$
t _f	Fall Time		5.1			
C _{iss}	Input Capacitance		890			$V_{GS} = 0V$
C _{oss}	Output Capacitance		180		pF	$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance		40			f = 1.0MHz
C _{oss}	Output Capacitance		870			V _{GS} = 0V, V _{DS} = 1.0V, f=1.0MHz
C _{oss}	Output Capacitance		100			$V_{GS} = 0V, V_{DS} = 80V, f=1.0MHz$

Diode Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
I _S	Continuous Source Current			25		MOSFET symbol
	(Body Diode)				Α	showing the
I _{SM}	Pulsed Source Current			45		integral reverse
	(Body Diode) ⑤					p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 3.4A, V_{GS} = 0V$ ⑦
t _{rr}	Reverse Recovery Time		31	47	ns	$T_J = 25^{\circ}C, I_F = 3.4A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge		40	60	nC	di/dt = 100A/μs ①

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

Pulse width $\leq 400 \mu s;$ duty cycle $\leq 2\%.$



Absolute Maximum Ratings

	Parameter	Max.	Units
P _D @T _A = 25°C	Power Dissipation ③	2.2	W
P _D @T _A = 70°C	Power Dissipation ③	1.4	
P _D @T _C = 25°C	Power Dissipation ④	42	
T _P	Peak Soldering Temperature	270	°C
TJ	Operating Junction and	-40 to + 150	
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient 30		58	
$R_{\theta JA}$	Junction-to-Ambient ®®	12.5		
$R_{\theta JA}$	Junction-to-Ambient	20		°C/W
$R_{\theta JC}$	Junction-to-Case ⊕ ⑩	_	3.0	
R _{0J-PCB}	Junction-to-PCB Mounted	1.0		

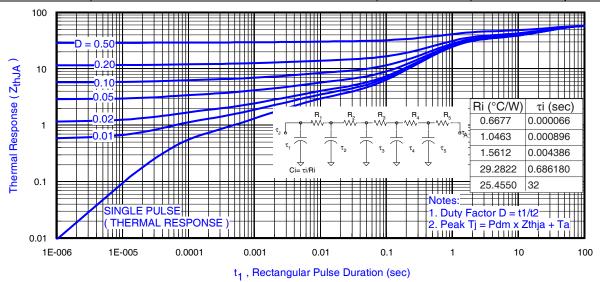
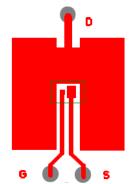


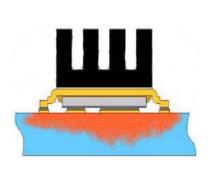
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

- 3 Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.
- ® Used double sided cooling, mounting pad with large heatsink.
- Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- $^{\circledR}$ R $_{\theta}$ is measured at T $_{J}$ of approximately 90°C.



3 Surface mounted on 1 in. square Cu board (still air).



Mounted to a PCB with small clip heatsink (still air)



 Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)



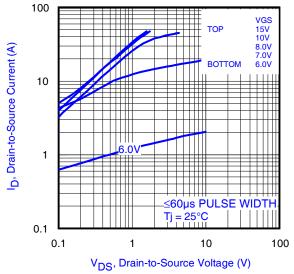


Fig 4. Typical Output Characteristics

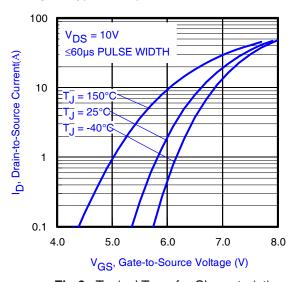


Fig 6. Typical Transfer Characteristics

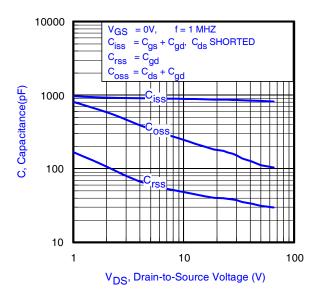


Fig 8. Typical Capacitance vs.Drain-to-Source Voltage

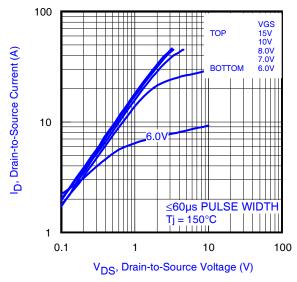


Fig 5. Typical Output Characteristics

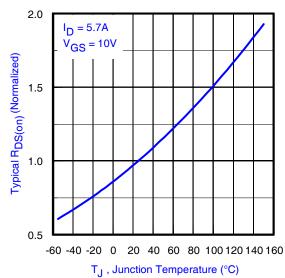


Fig 7. Normalized On-Resistance vs. Temperature

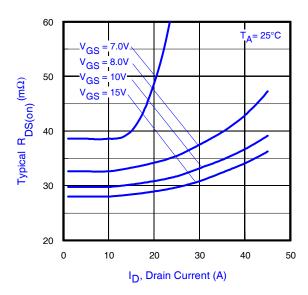


Fig 9. Typical On-Resistance vs. Drain Current



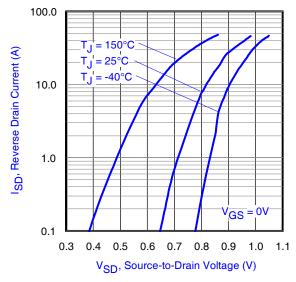


Fig 10. Typical Source-Drain Diode Forward Voltage

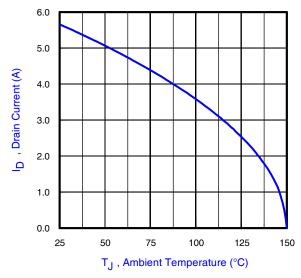


Fig 12. Maximum Drain Current vs. Ambient Temperature

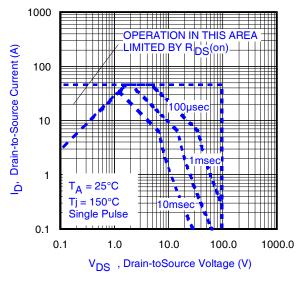


Fig11. Maximum Safe Operating Area

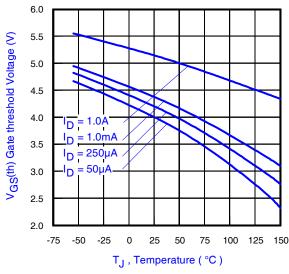


Fig 13. Typical Threshold Voltage vs. Junction Temperature

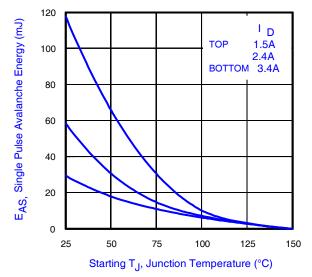


Fig 14. Maximum Avalanche Energy vs. Drain Current



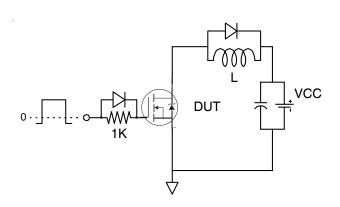


Fig 15a. Gate Charge Test Circuit

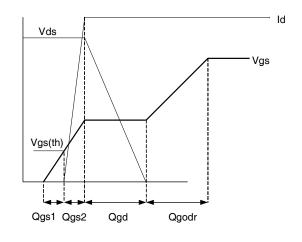


Fig 15b. Gate Charge Waveform

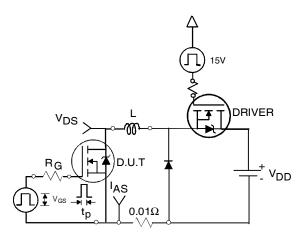


Fig 16b. Unclamped Inductive Test Circuit

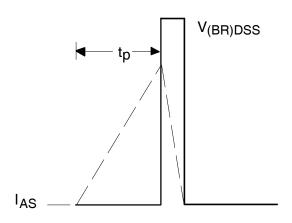


Fig 16c. Unclamped Inductive Waveforms

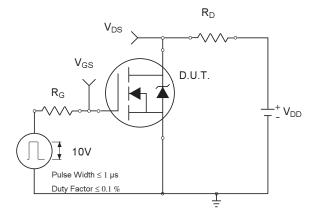


Fig 17a. Switching Time Test Circuit

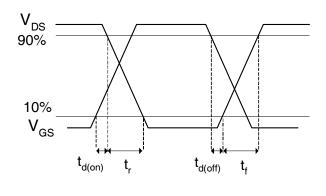


Fig 17b. Switching Time Waveforms



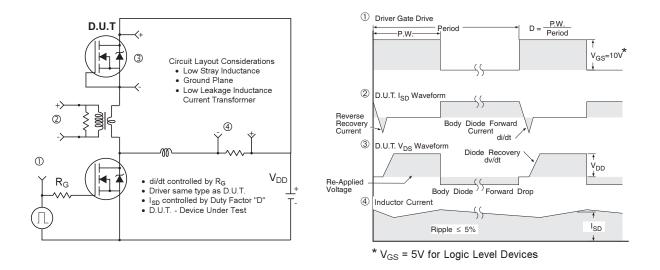
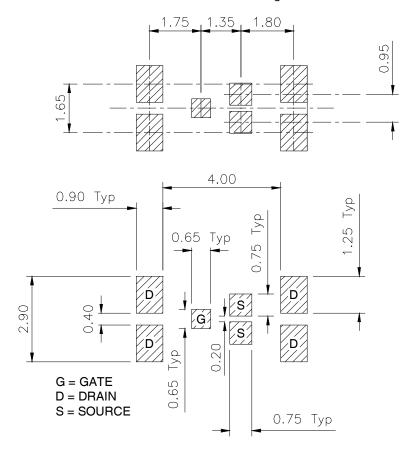


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Substrate and PCB Layout, SJ Outline (Small Size Can, J-Designation).

Please see DirectFET application note $\underline{\text{AN-}1035}$ for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.



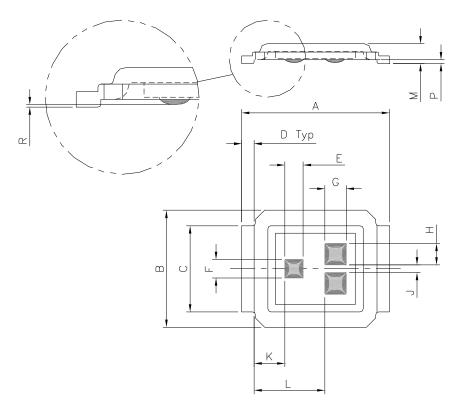
Note: For the most current drawing please refer to IR website at http://www.irf.com/package



DirectFET™ Outline Dimension, SJ Outline (Small Size Can, J-Designation).

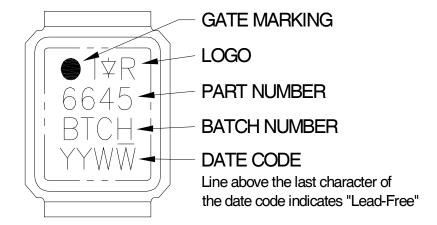
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.



	DIMENSIONS							
	MET	RIC	IMPE	RIAL				
CODE	MIN	MAX	MIN	MAX				
Α	4.75	4.85	0.187	0.191				
В	3.70	3.95	0.146	0.156				
С	2.75	2.85	0.108	0.112				
D	0.35	0.45	0.014	0.018				
E	0.58	0.62	0.023	0.024				
F	0.58	0.62	0.023	0.024				
G	0.68	0.72	0.027	0.028				
Н	0.68	0.72	0.027	0.028				
J	0.23	0.27	0.009	0.010				
K	0.95	1.05	0.037	0.041				
L	2.25	2.35	0.089	0.093				
М	0.59	0.70	0.023	0.028				
Р	0.08	0.17	0.003	0.007				
R	0.020	0.080	0.0008	0.0031				

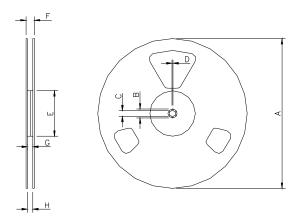
DirectFET™ Part Marking



Note: For the most current drawing please refer to IR website at http://www.irf.com/package

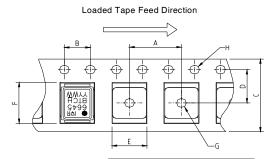


DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm Std reel quantity is 4800 parts. (ordered as IRF6645TRPBF). For 1000 parts on 7" reel, order IRF6645TR1PBF

	REEL DIMENSIONS							
S.	TANDARI	OPTION	(QTY 48	00)	TR	1 OPTION	(QTY 10	00)
	ME	TRIC	IMP	ERIAL	ME	TRIC	IMP	ERIAL
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
Α	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
В	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
С	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
Е	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
Н	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



DIMENSIONS							
	ME	TRIC	IMPERIAL				
CODE	MIN	MAX	MIN	MAX			
Α	7.90	8.10	0.311	0.319			
В	3.90	4.10	0.154	0.161			
С	11.90	12.30	0.469	0.484			
D	5.45	5.55	0.215	0.219			
E	4.00	4.20	0.158	0.165			
F	5.00	5.20	0.197	0.205			
G	1.50	N.C	0.059	N.C			
Н	1.50	1.60	0.059	0.063			

Note: For the most current drawing please refer to IR website at http://www.irf.com/package

Revision History

Date	Comments
12/10/2012	Updated package outline, on page 8.
2/26/2013	Updated P_D @ T_A = 25C from 3W to 2.2W, on page 3.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

Data and specifications subject to change without notice.



IR WORLD HEADQUARTERS: 101N Sepulveda Blvd, El Segundo, California 90245, USA

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