

Automotive MOSFET

OptiMOS™-5 Power-Transistor

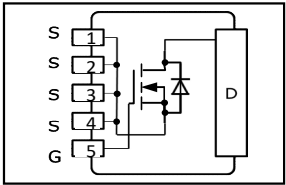


Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.



Product Summary

$V_{DS}$	100	V
$R_{DS(on)}$	3.1	mΩ
$I_D$ (chip limited)	170	A

Type	Package	Marking
IAUA170N10S5N031	PG-HSOF-5-4	5N10031



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1)</sup>	170	A
		$V_{GS}=10\text{ V}$ , DC current <sup>2)</sup>	170	
		$T_a=85\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,3)</sup>	22	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	519	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=85\text{ A}$	165	mJ
Avalanche current, single pulse	$I_{AS}$	-	130	A
Gate source voltage	$V_{GS}$	-	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	197	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	0.76	K/W
Thermal resistance, junction - ambient <sup>3)</sup>	$R_{thJA}$	–	–	22.9	–	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	100	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=110\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	–	0.1	1	$\mu\text{A}$
		$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=100\text{ °C}^{2)}$	–	1	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$ , $I_D=40\text{ A}$	–	3.4	4.0	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=85\text{ A}$	–	2.7	3.1	
Gate resistance <sup>2)</sup>	$R_G$	–	–	1.2	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$	-	4927	6405	pF
Output capacitance	$C_{oss}$		-	791	1029	
Reverse transfer capacitance	$C_{rss}$		-	32	48	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=85\text{ A}, R_G=3.5\ \Omega$	-	11	-	ns
Rise time	$t_r$		-	6	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	$t_f$		-	14	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=50\text{ V}, I_D=85\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	23	30	nC
Gate to drain charge	$Q_{gd}$		-	14	21	
Gate charge total	$Q_g$		-	67	88	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	-	-	170	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	519	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=85\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	53	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	79	-	nC

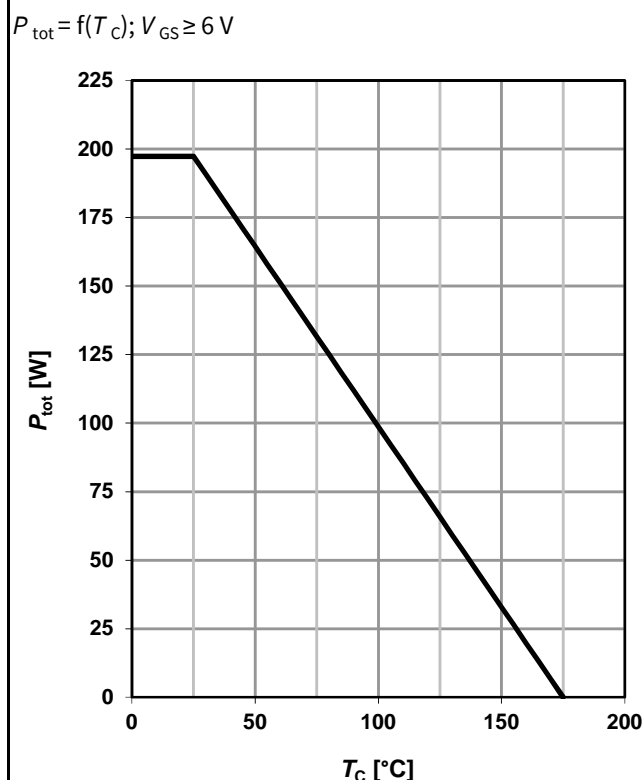
<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

<sup>2)</sup> The parameter is not subject to production testing – specified by design.

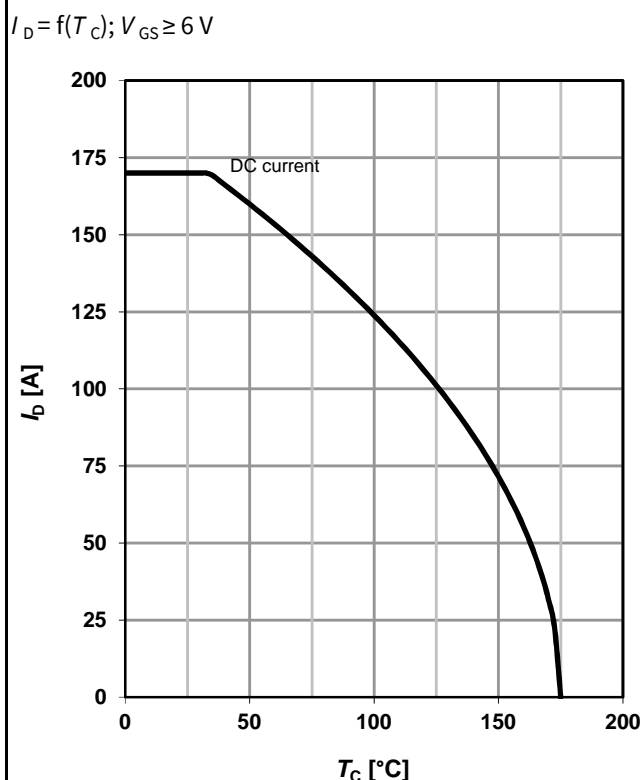
<sup>3)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

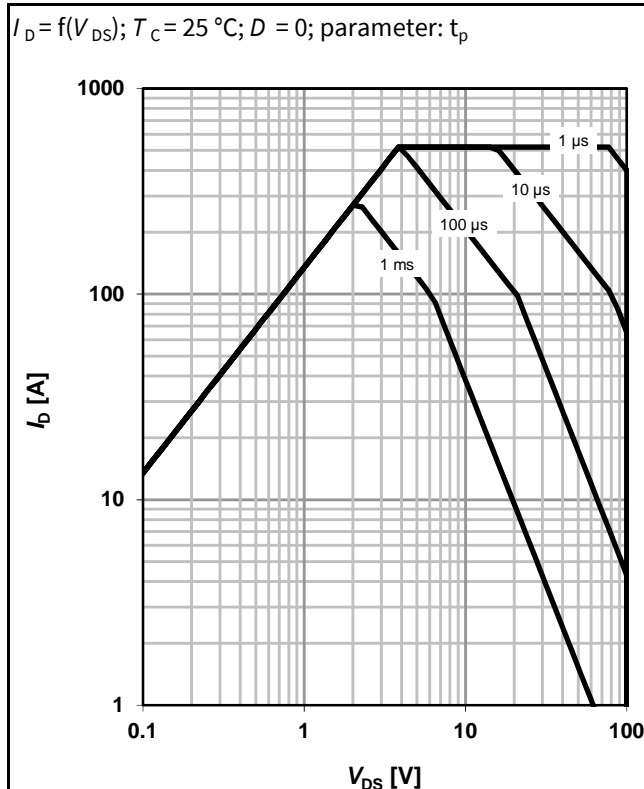
### 1 Power dissipation



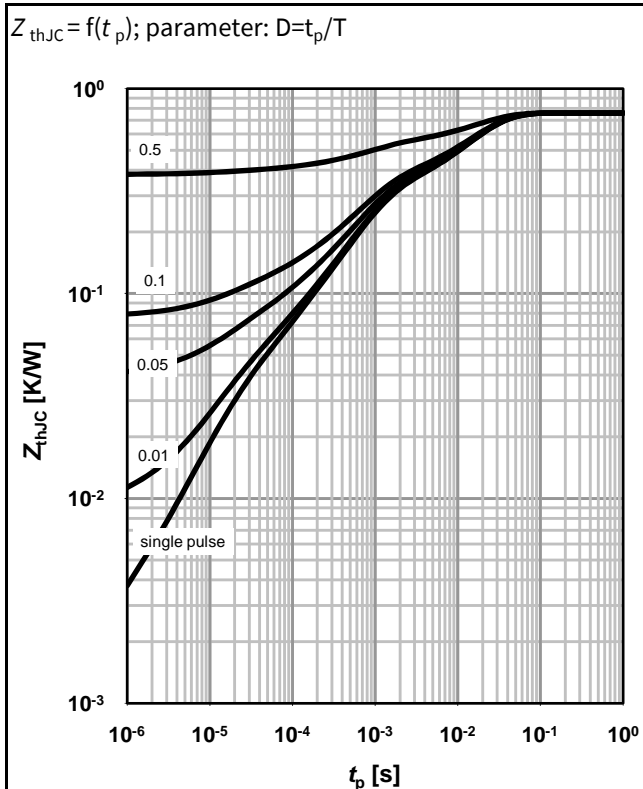
### 2 Drain current



### 3 Safe operating area

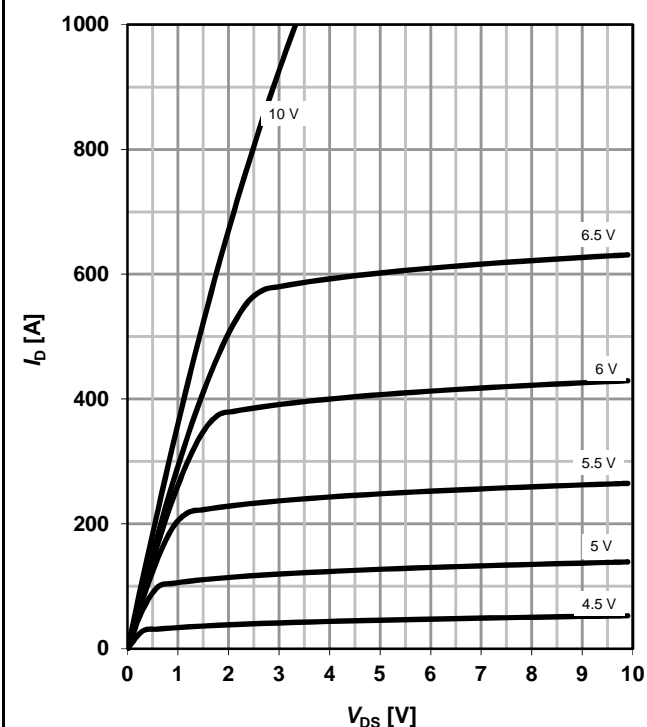


### 4 Max. transient thermal impedance



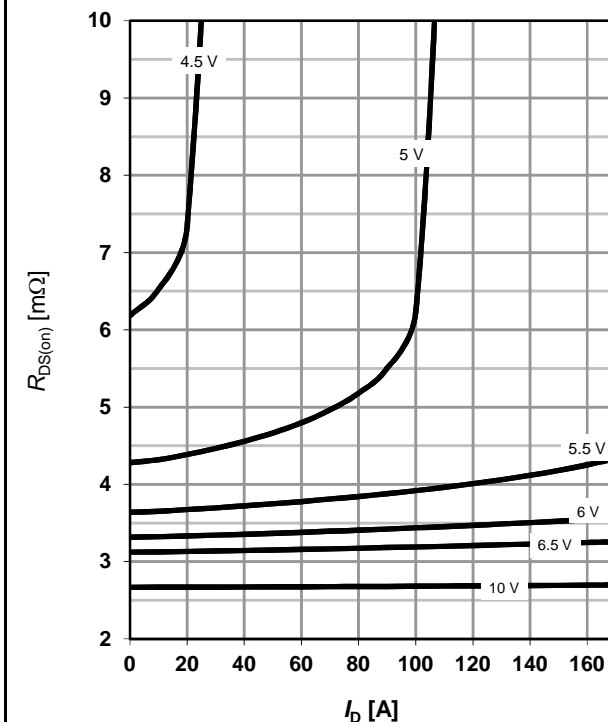
## 5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



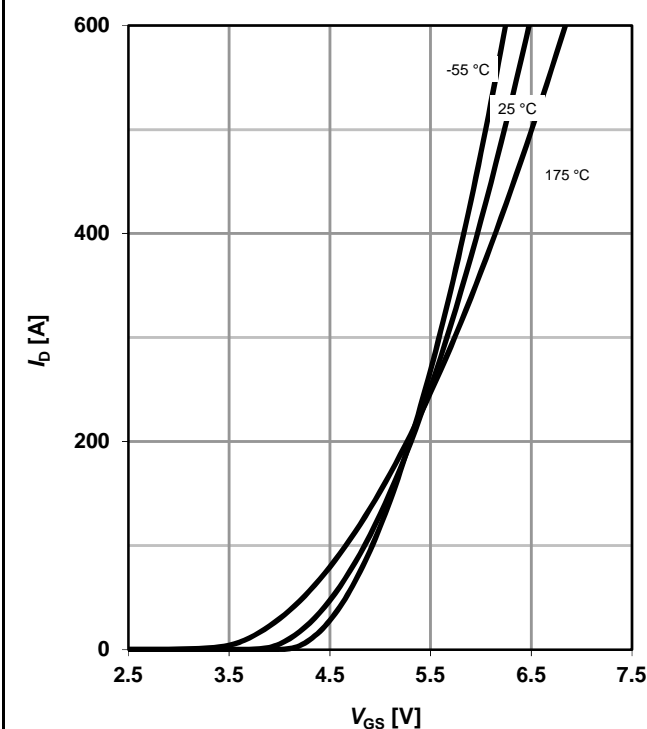
## 6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



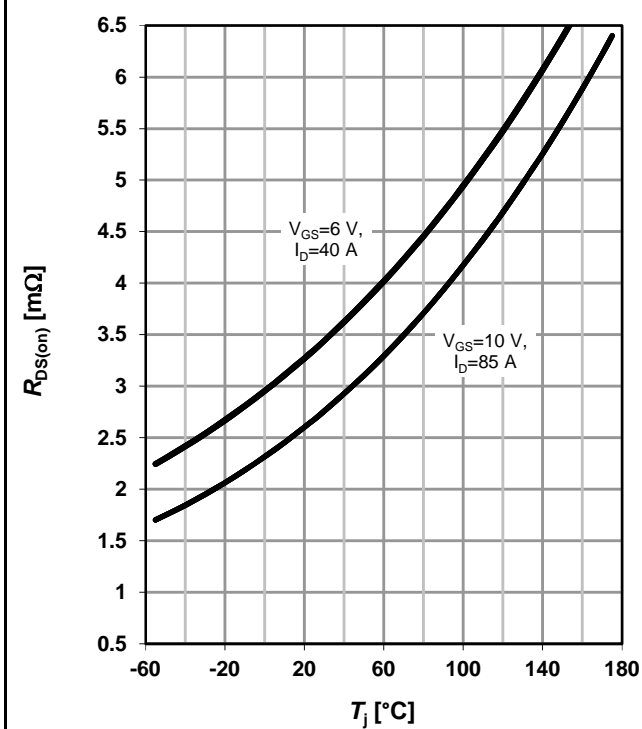
## 7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{V}; \text{parameter: } T_j$



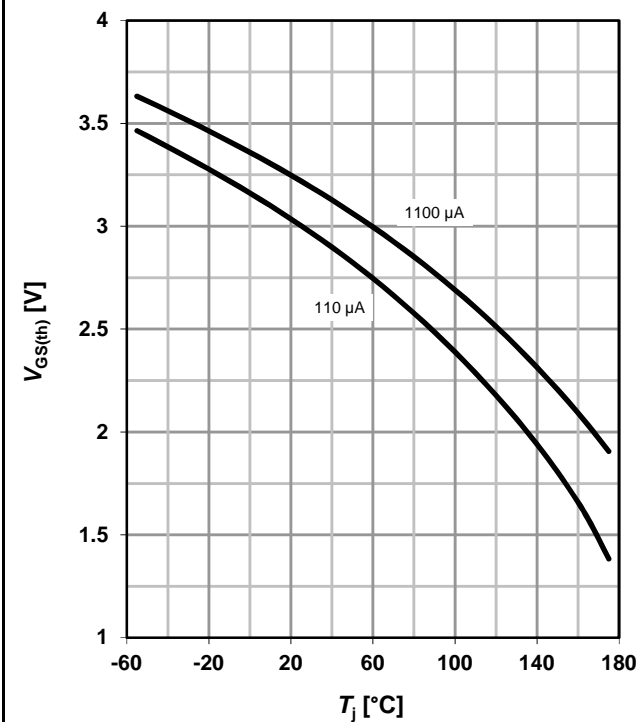
## 8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



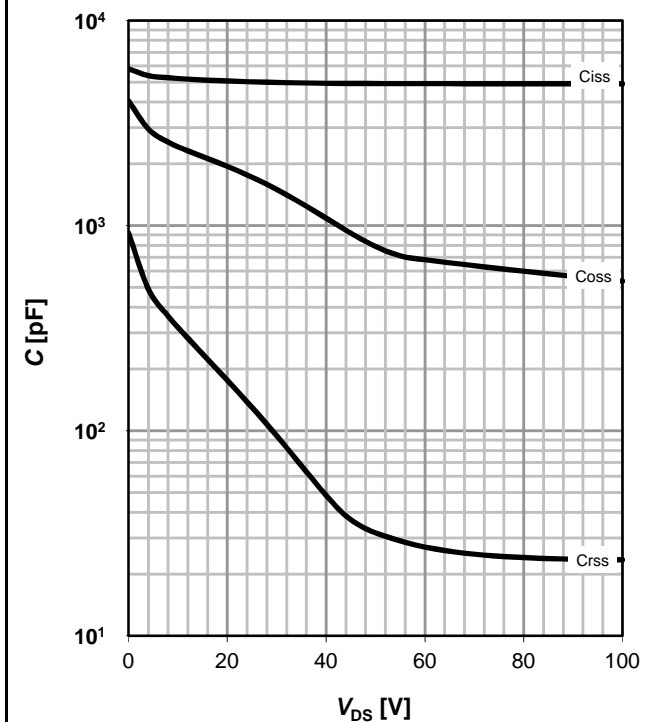
## 9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$



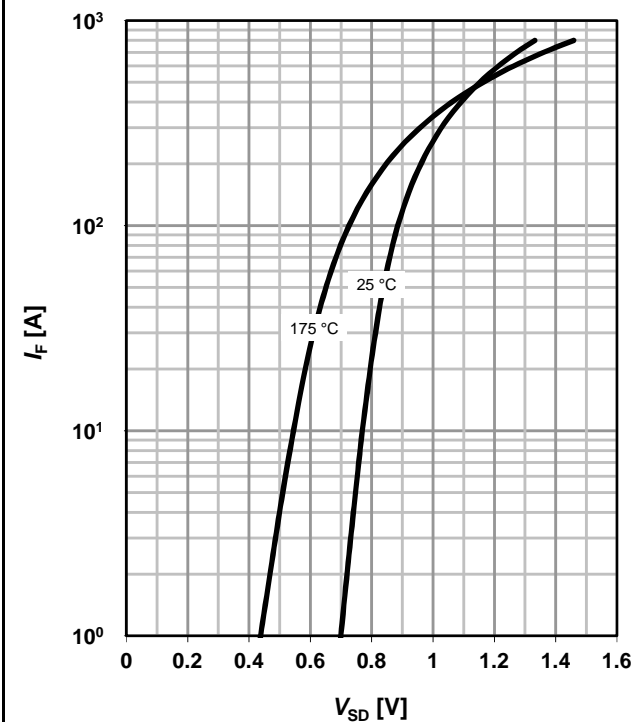
## 10 Typ. capacitances

$C = f(V_{DS})$ ;  $V_{GS} = 0$  V;  $f = 1$  MHz



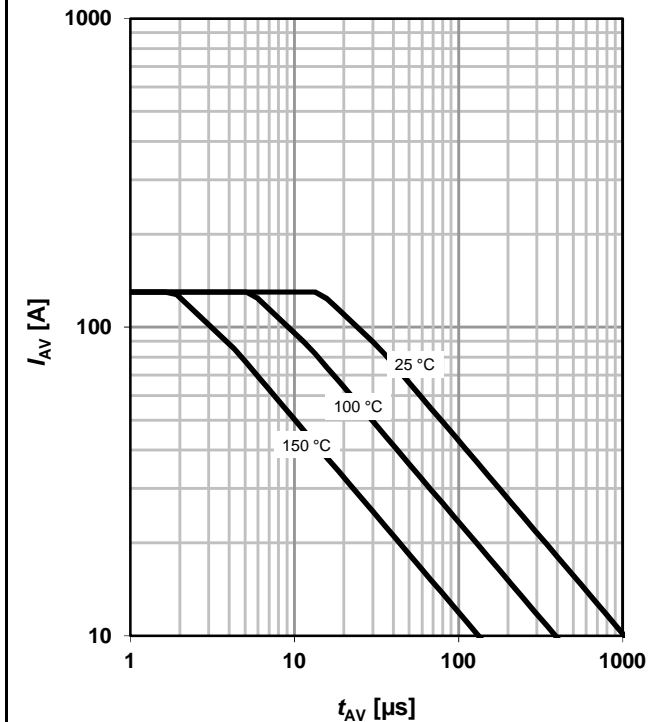
## 11 Typical forward diode characteristics

$I_F = f(V_{SD})$ ; parameter:  $T_j$



## 12 Typ. avalanche characteristics

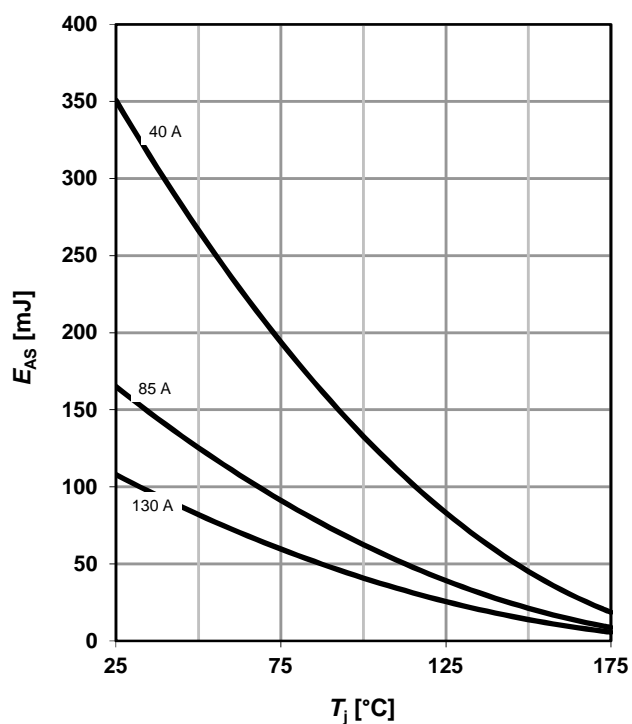
$I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$





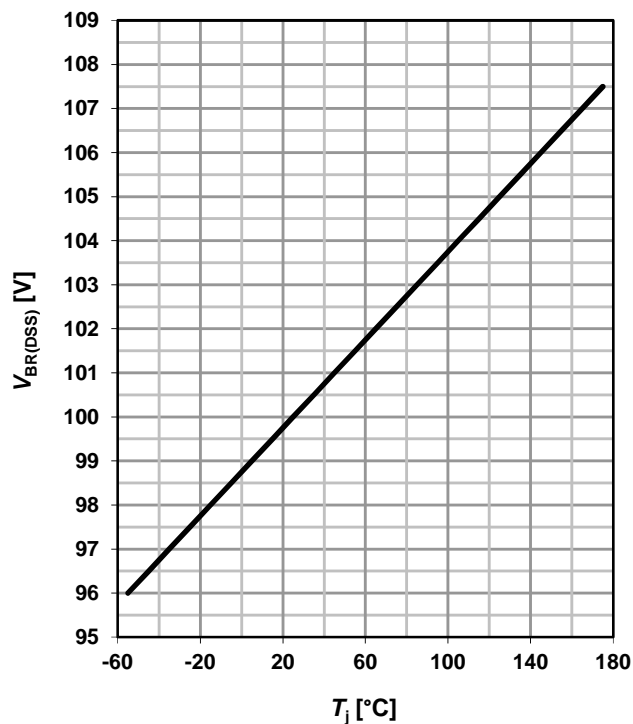
## 13 Typical avalanche energy

$E_{AS} = f(T_j)$ ; parameter:  $I_D$



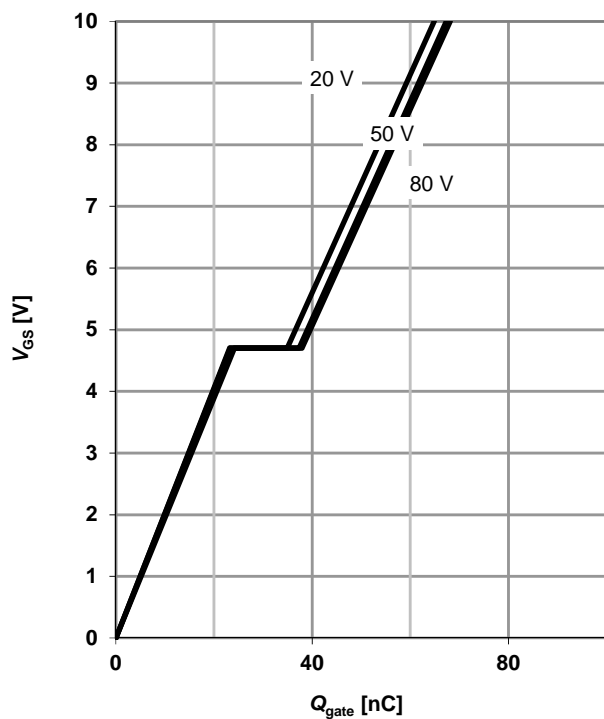
## 14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$ ;  $I_{D\_typ} = 1$  mA

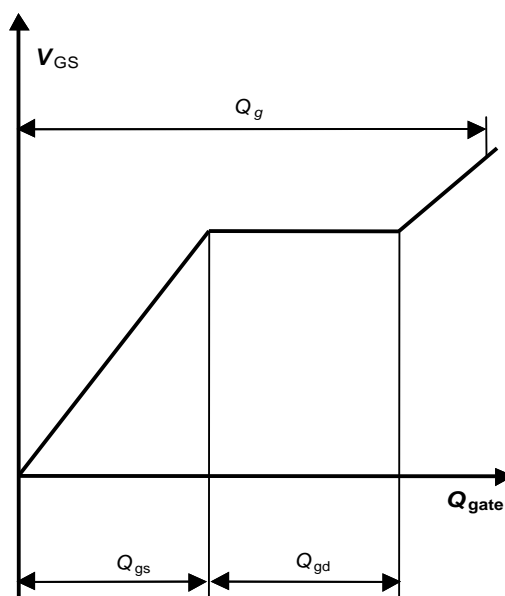


## 15 Typ. gate charge

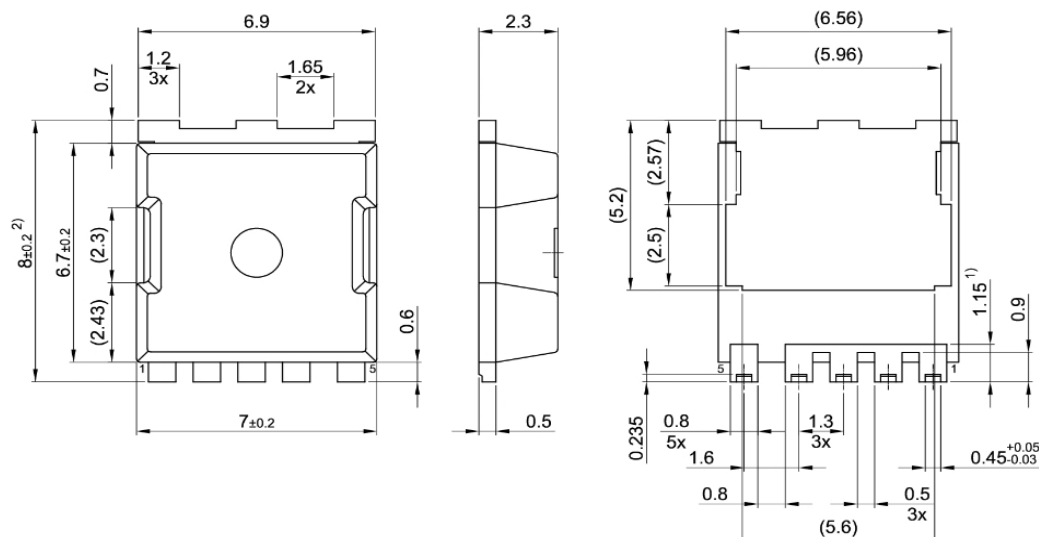
$V_{GS} = f(Q_{gate})$ ;  $I_D = 85$  A pulsed; parameter:  $V_{DD}$



## 16 Gate charge waveforms



### Package Outline



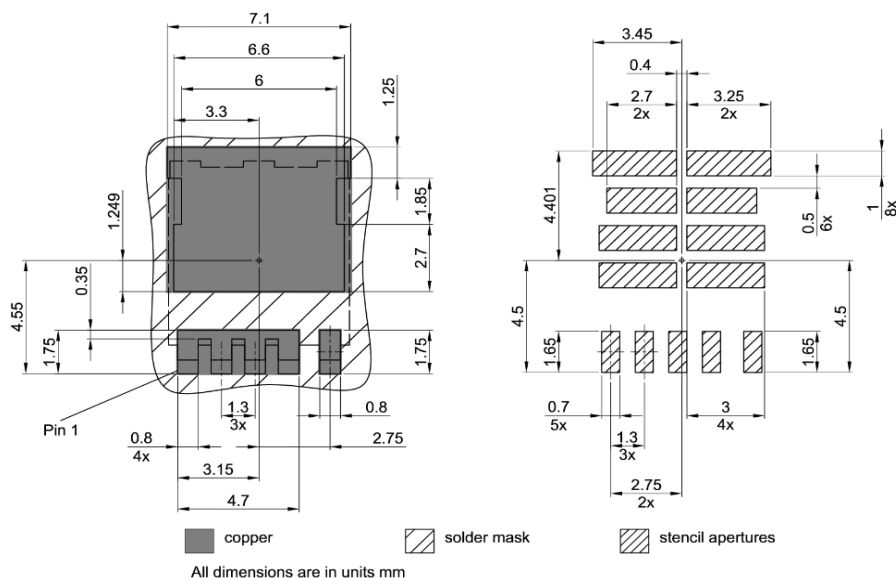
1) Lead length up to anti flash profile; mold flashes excluded

2) Excluding burr

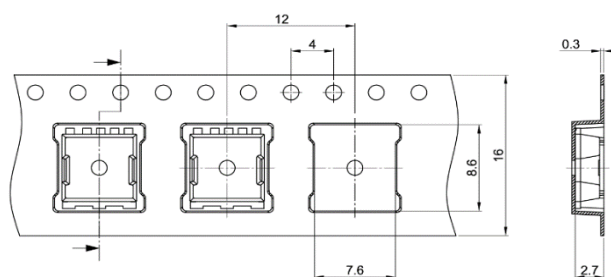
All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

### Footprint



### Packaging



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

**Revision History**

Revision	Date	Changes
Revision 1.0	23.03.2021	Final Datasheet
Revision 1.1	12.11.2021	Corrected figure 14

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**Edition 2021-11-12**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

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