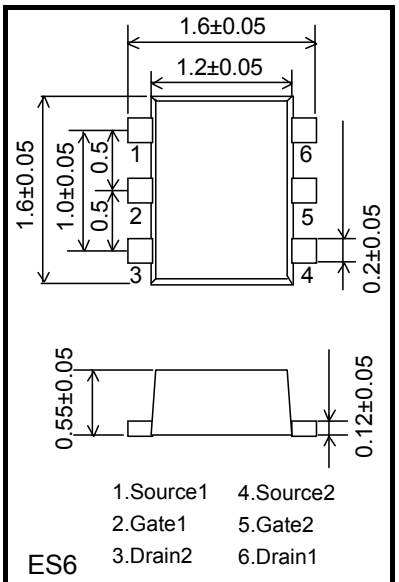
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N44FE

High Speed Switching Applications
Analog Switching Applications

- Compact package suitable for high-density mounting
- Low ON-resistance : $R_{DS(ON)}$ = 4.0 Ω (max) (@V_{GS} = 4 V)
  : $R_{DS(ON)}$ = 7.0 Ω (max) (@V_{GS} = 2.5 V)

Unit: mm



1.Source1 4.Source2
2.Gate1 5.Gate2
3.Drain2 6.Drain1

ES6

JEDEC	—
JEITA	—
TOSHIBA	2-2N1D

Weight: 3 mg (typ.)

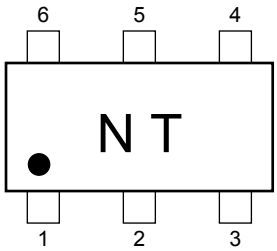
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	30	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

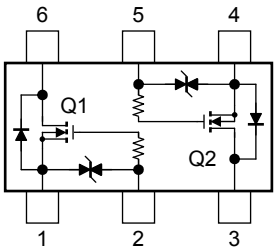
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm^2 × 6)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

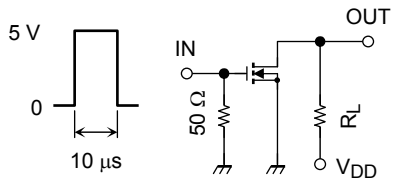
Start of commercial production
2009-04

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±14 V, V_{DS} = 0 V	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.8	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V	—	2.2	4.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V	—	4.0	7.0	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	8.5	—	pF
Reverse transfer capacitance		C_{rss}		—	5.3	—	
Output capacitance		C_{oss}		—	9.4	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 5 V	—	50	—	ns
	Turn-off time	t_{off}		—	200	—	

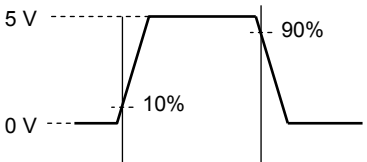
Switching Time Test Circuit

(a) Test circuit

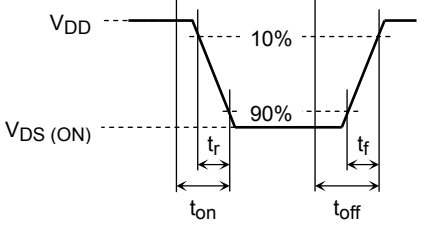


V_{DD} = 5 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}



(c) V_{OUT}



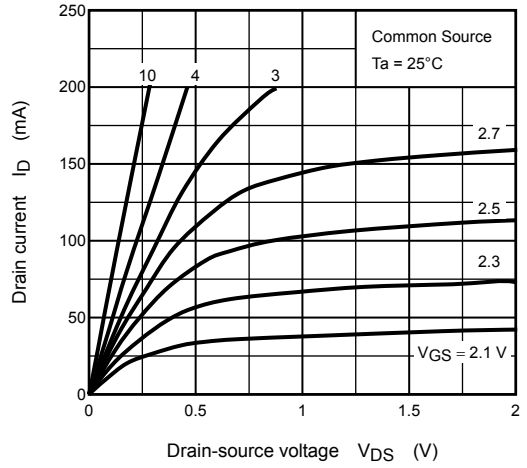
Precaution

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM6N44FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

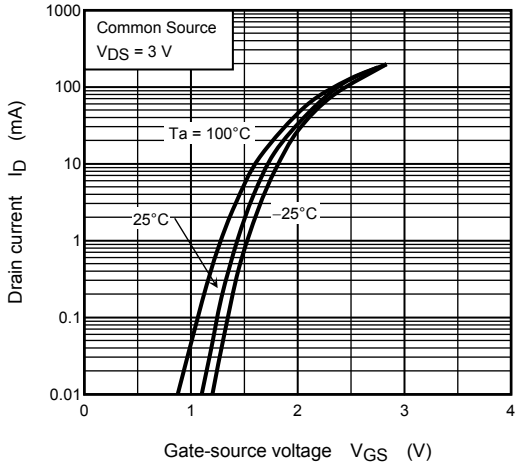
Take this into consideration when using the device

(Q1, Q2 Common)

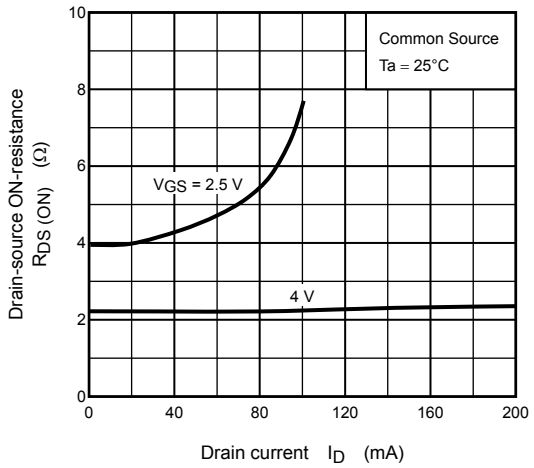
$I_D - V_{DS}$



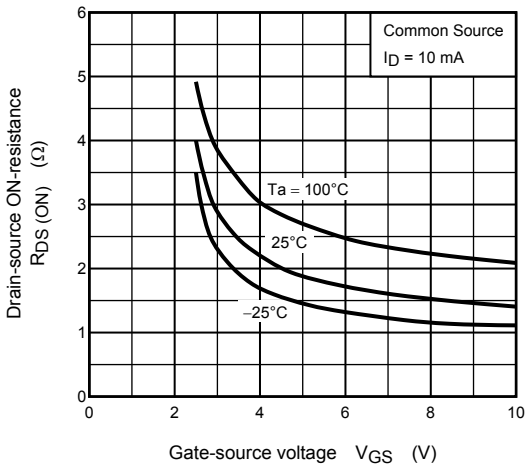
$I_D - V_{GS}$



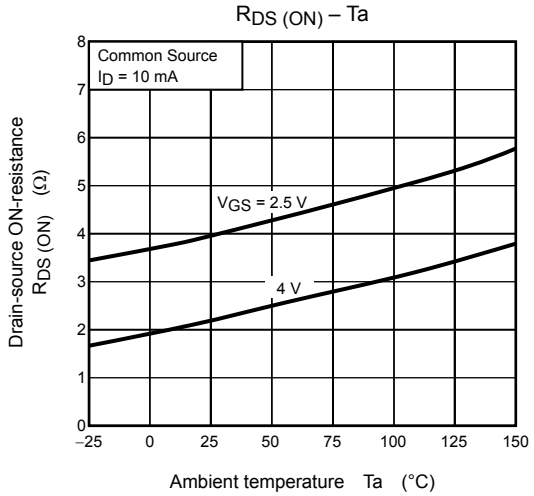
$R_{DS\ (ON)} - I_D$



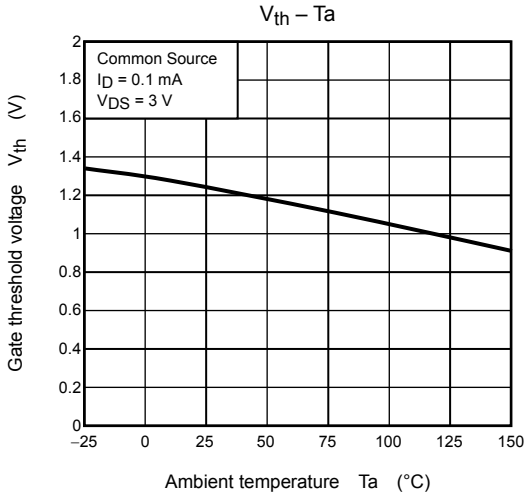
$R_{DS\ (ON)} - V_{GS}$



$R_{DS\ (ON)} - Ta$

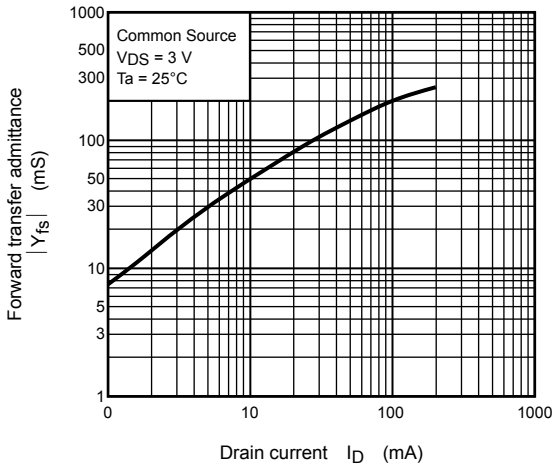


$V_{th} - Ta$

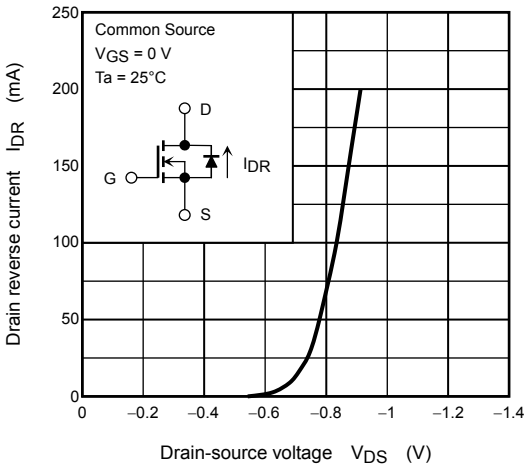


(Q1, Q2 Common)

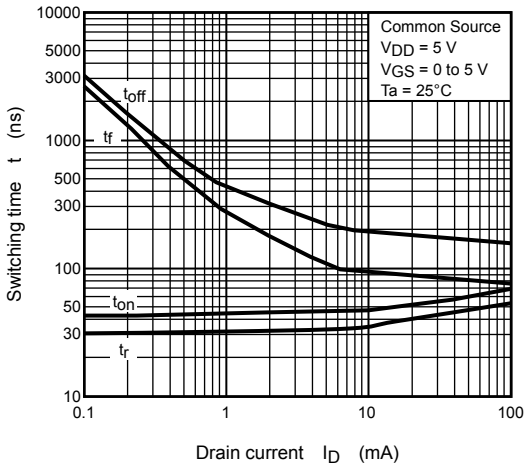
$|Y_{fs}| - I_D$



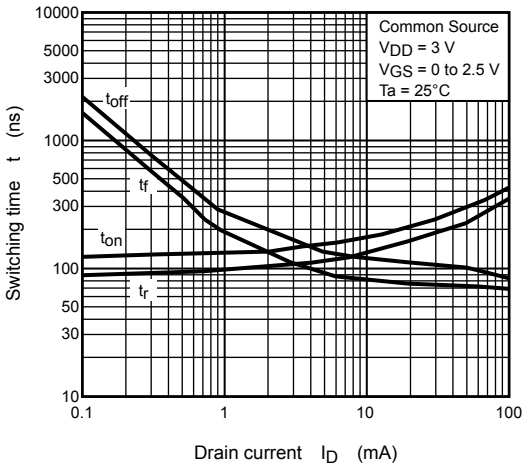
$I_{DR} - V_{DS}$



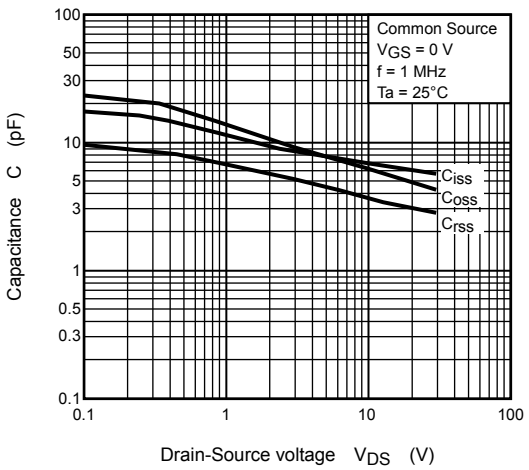
$t - I_D$



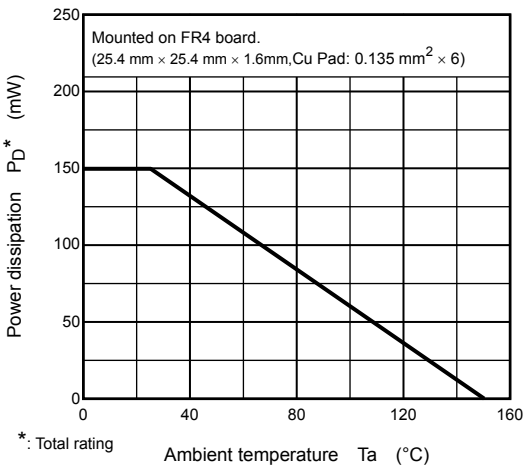
$t - I_D$



$C - V_{DS}$



$P_D^* - Ta$



*: Total rating

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