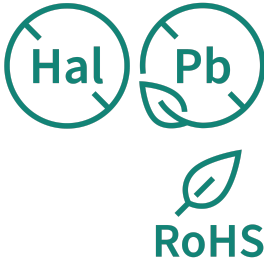
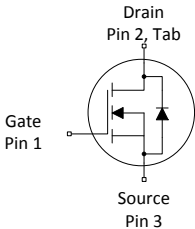
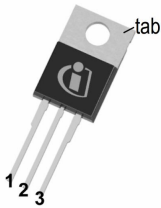


PG-TO220-3



MOSFET  
StrongIRFET™2 Power-Transistor, 60 V

- Features
- Optimized for wide range of applications
  - N-channel, normal level
  - 100% avalanche tested
  - Pb-free lead plating; RoHS compliant
  - Halogen-free according to IEC61249-2-21

Product validation  
Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	1.9	mΩ
$I_D$	190	A
$Q_{oss}$	108	nC
$Q_G(0V..10V)$	108	nC

Type/Ordering Code	Package	Marking	Related Links
IPP019N06NF2S	PG-TO220-3	019N06NS	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	190 146 33	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	760	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	349	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	231 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.65	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$ , $I_D=129\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.5 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance <sup>6)</sup>	$R_{DS(on)}$	-	1.7 2.1	1.9 2.9	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=50\text{ A}$
Gate resistance	$R_G$	-	2.7	-	$\Omega$	-
Transconductance <sup>7)</sup>	$g_{fs}$	110	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$ , $I_D=100\text{ A}$

<sup>6)</sup>  $R_{DS(on)}$  is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	7300	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1550	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	63	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	31	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	48	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	17	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics <sup>8)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	33	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	20	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	20	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	$Q_{sw}$	-	33	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>9)</sup>	$Q_g$	-	108	162	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	100	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	108	-	nC	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	153	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	760	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.92	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=100\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	46	-	ns	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	53	-	nC	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time	$t_{rr}$	-	33	-	ns	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	164	-	nC	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$

## 4 Electrical characteristics diagrams

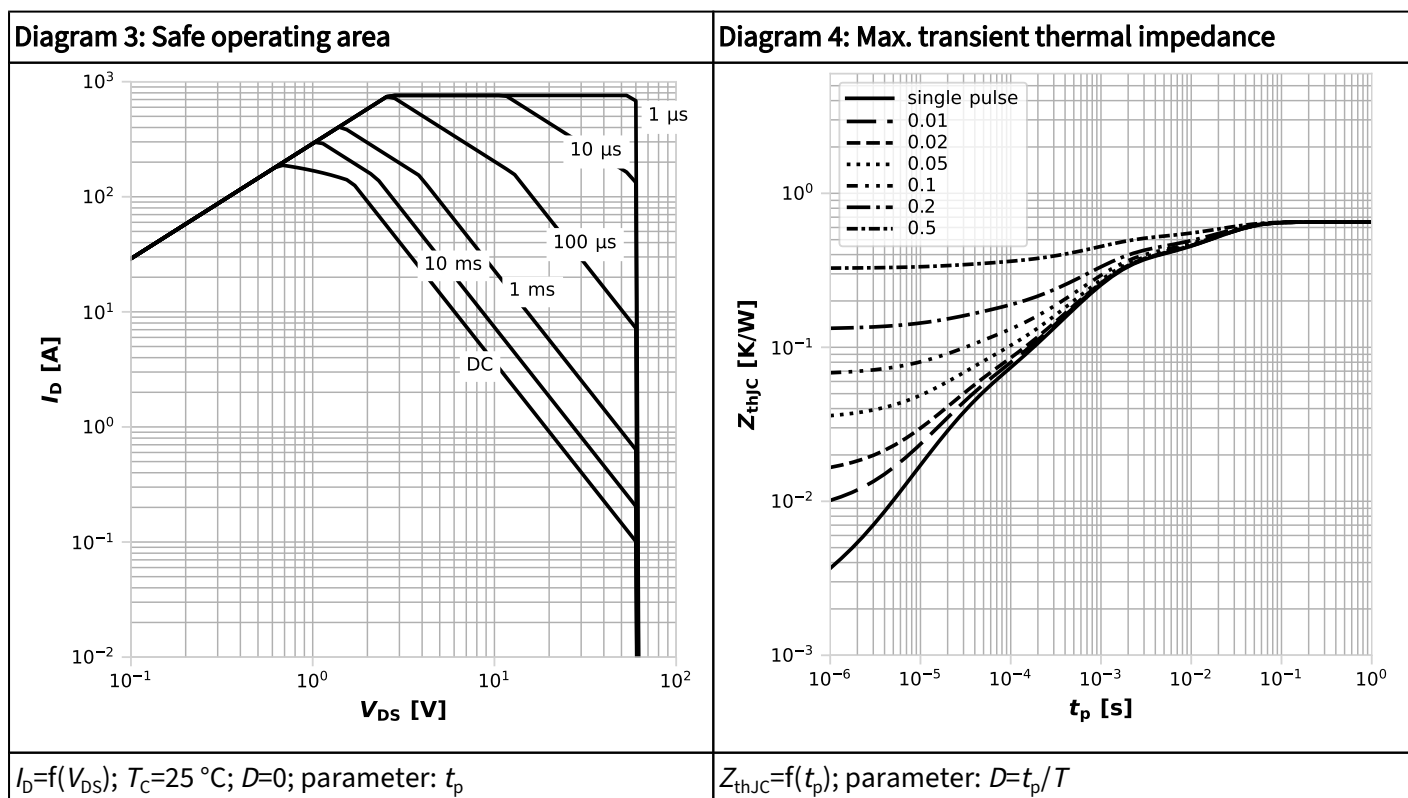
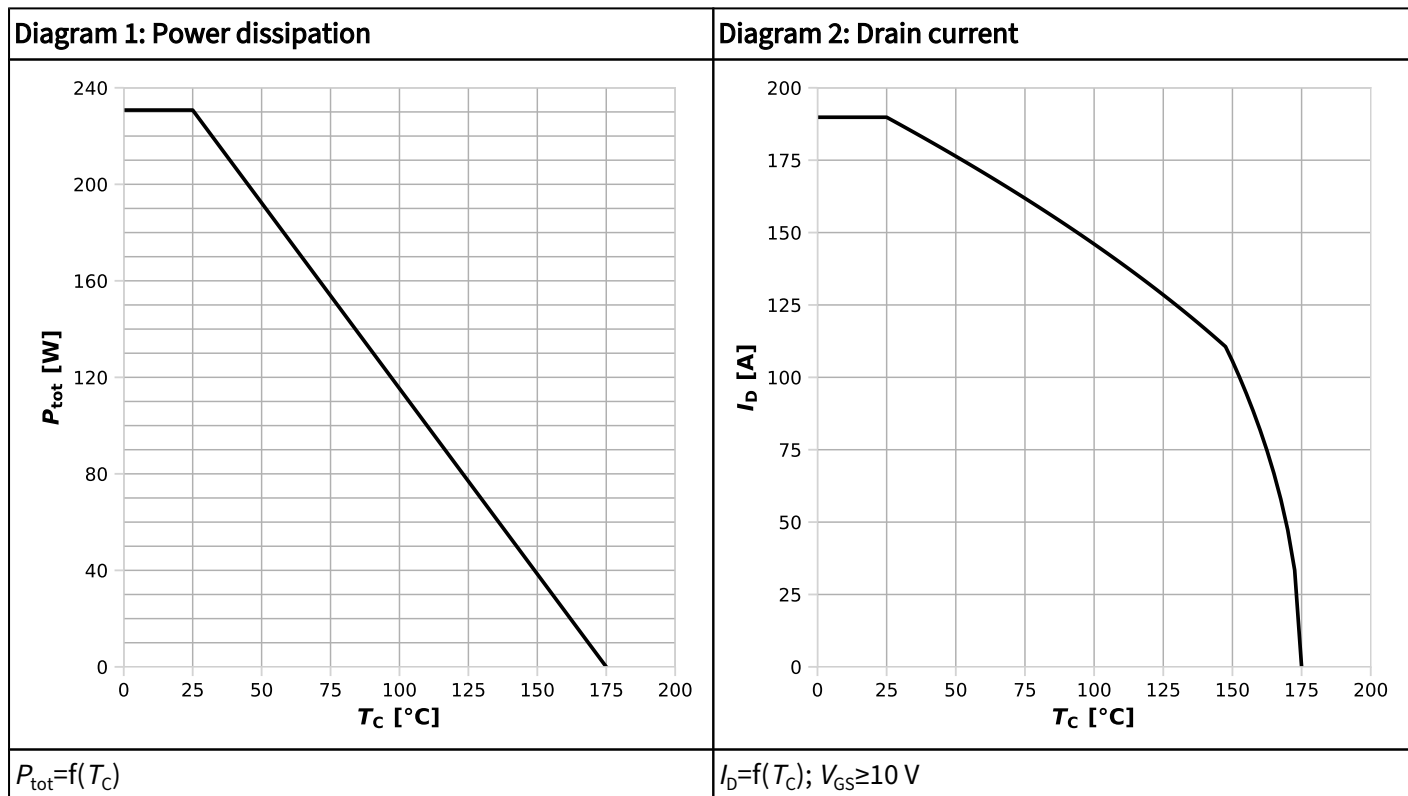
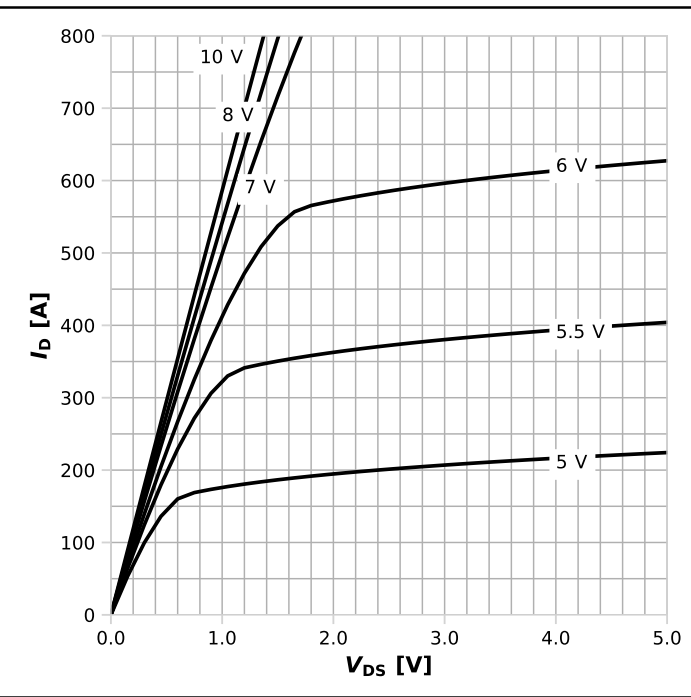
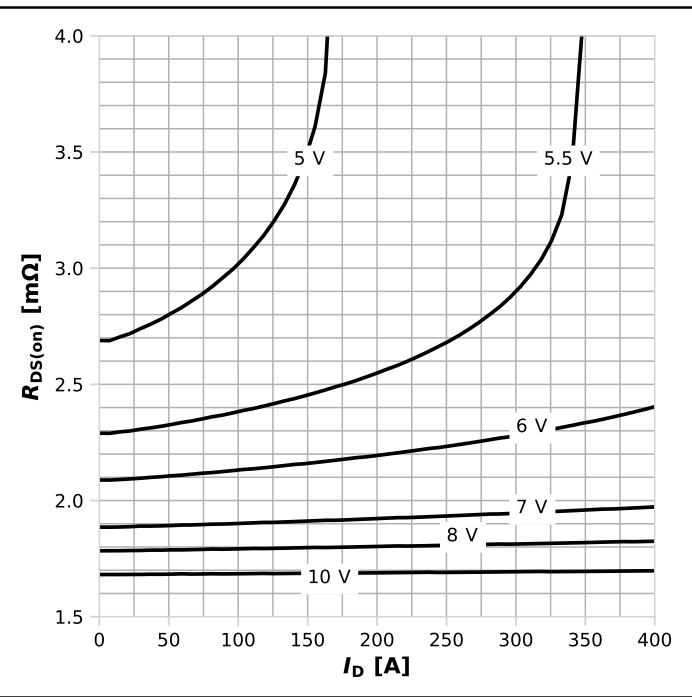


Diagram 5: Typ. output characteristics



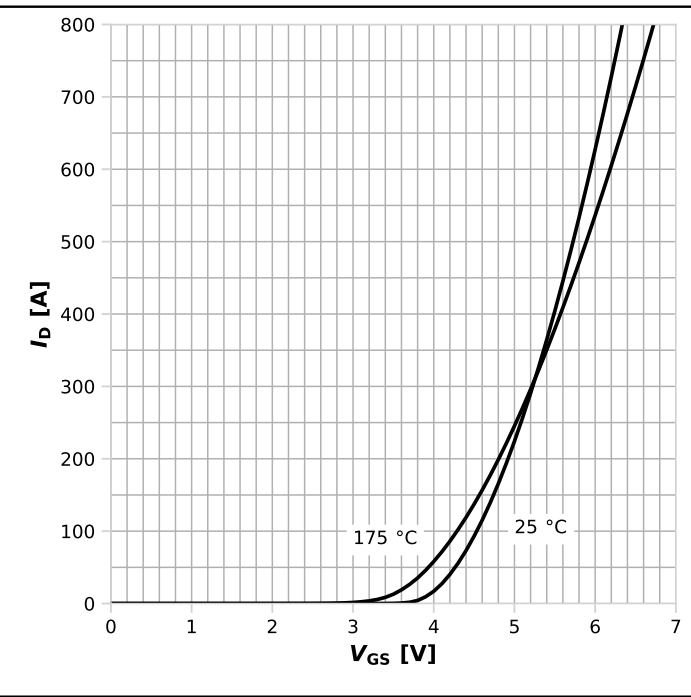
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



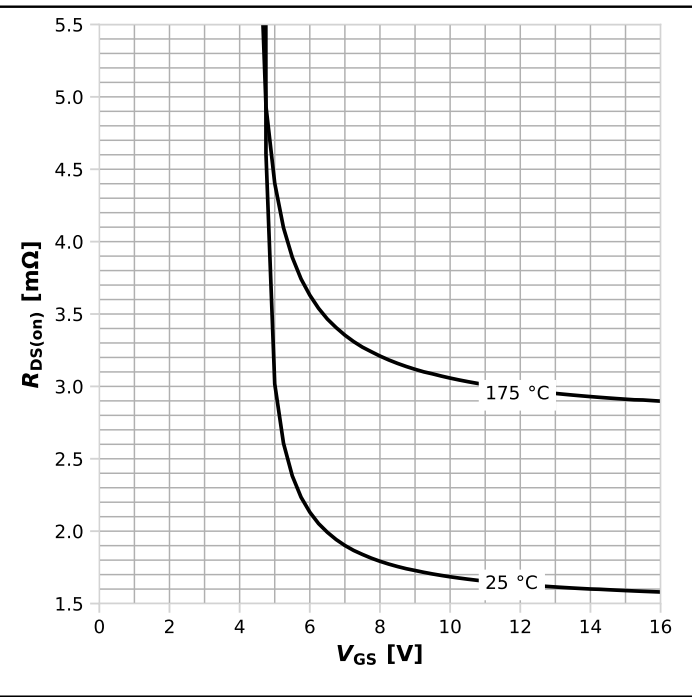
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

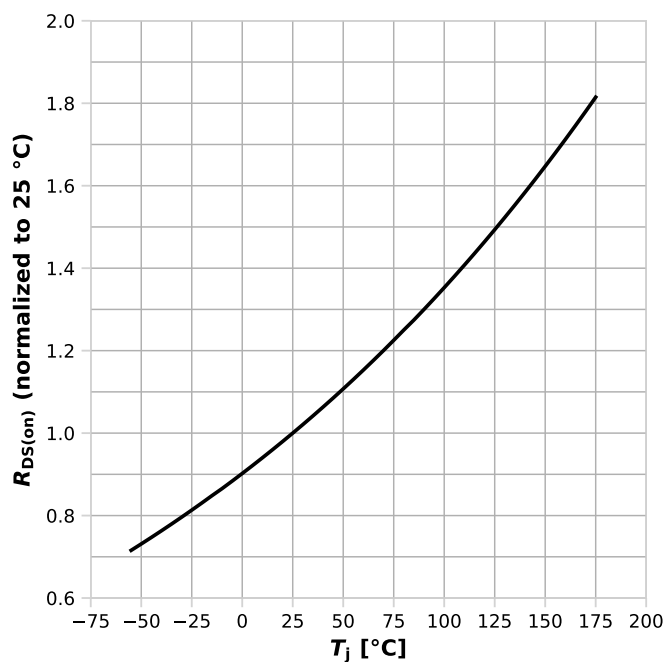
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 100\text{ A}$ ; parameter:  $T_j$

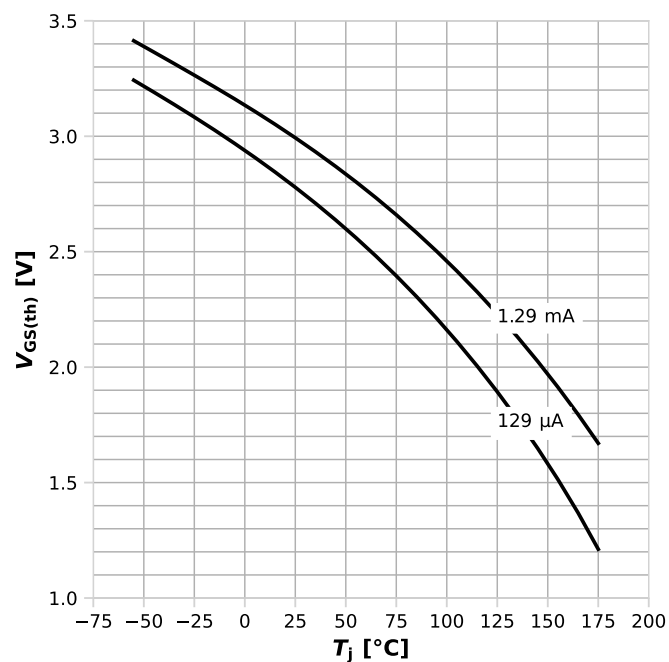


Diagram 9: Normalized drain-source on resistance



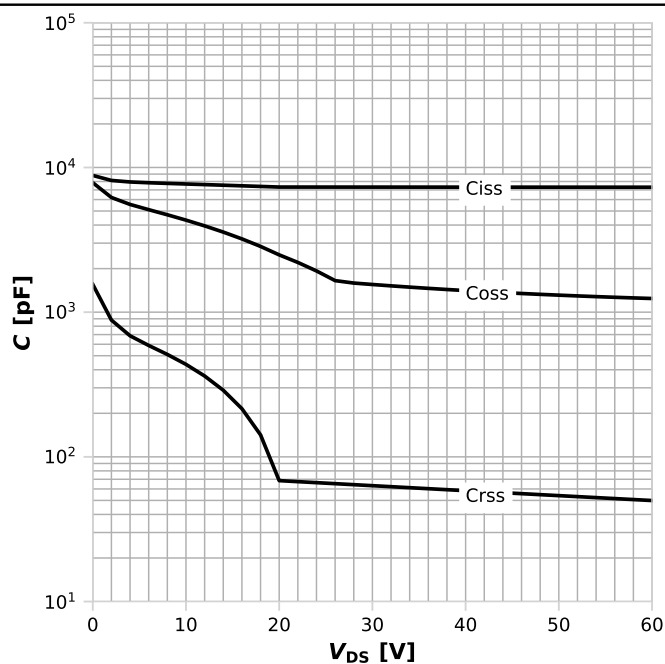
$$R_{DS(on)} = f(T_j), I_D = 100 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



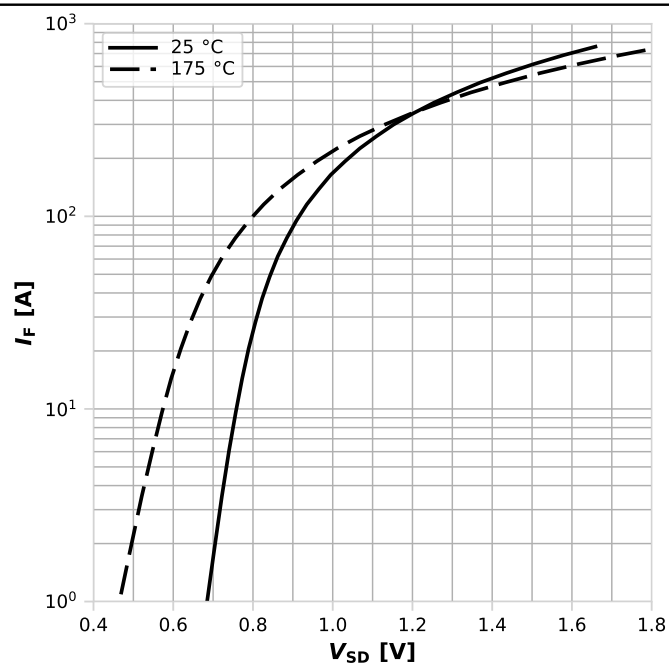
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



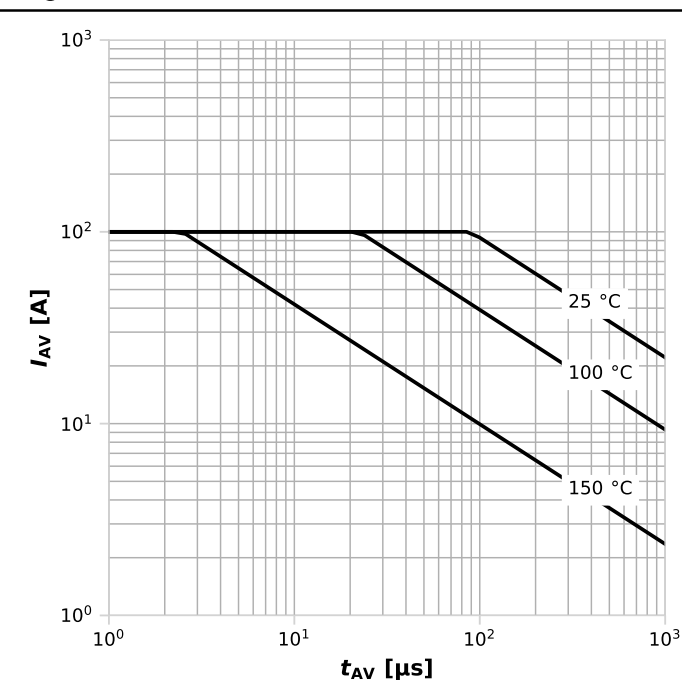
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



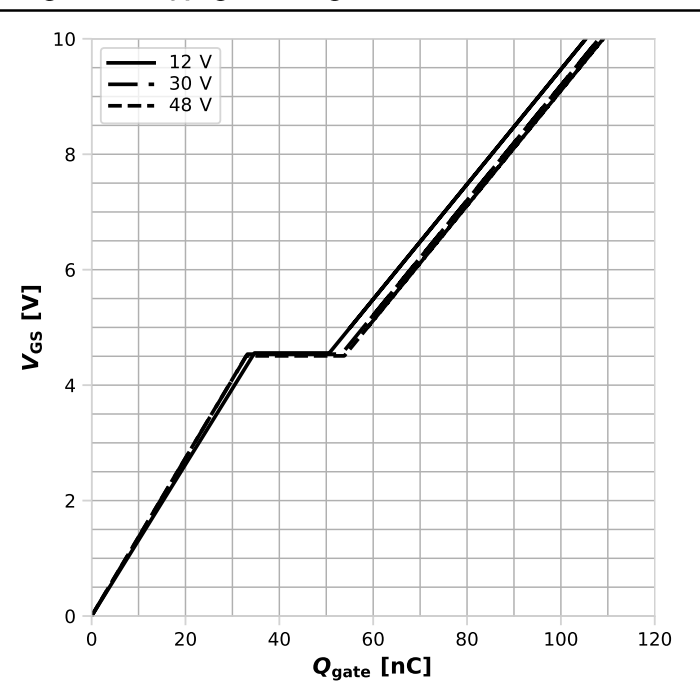
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



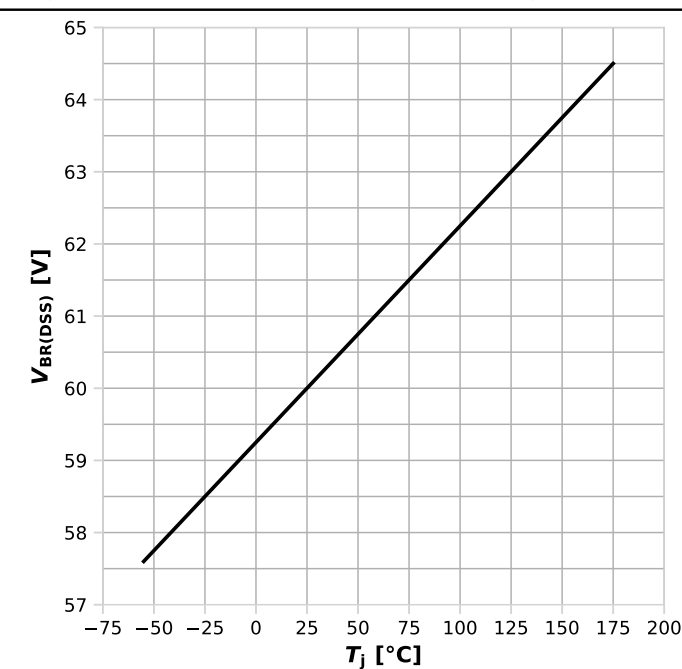
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



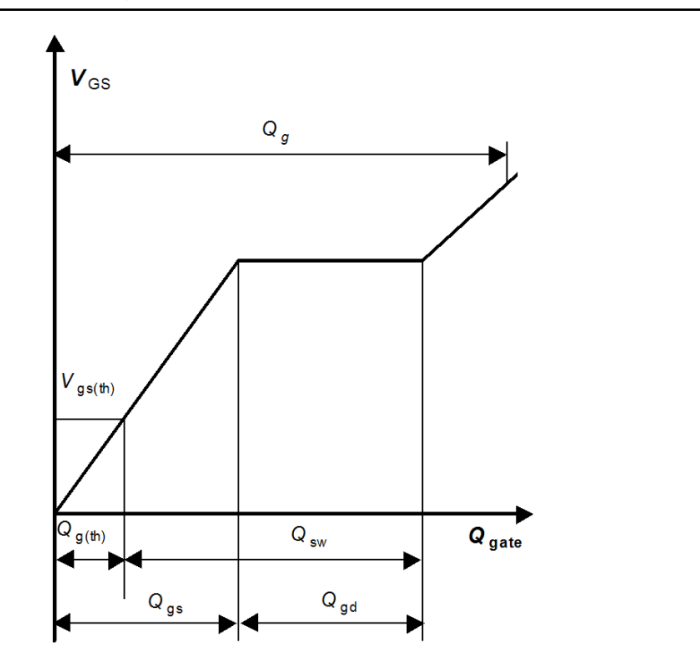
$V_{GS}=f(Q_{gate})$ ,  $I_D=100\text{ A}$  pulsed,  $T_j=25\text{ °C}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

Gate charge waveforms



5 Package Outlines

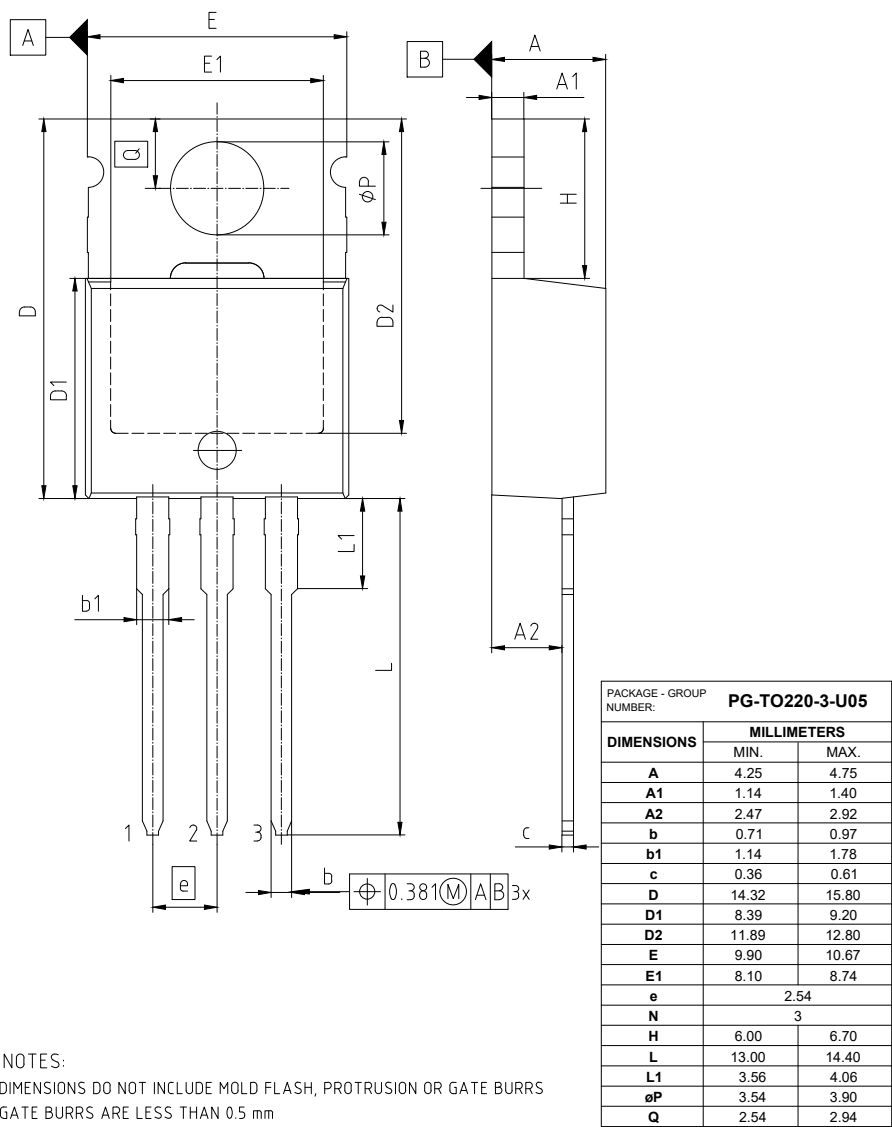


Figure 1 Outline PG-TO220-3, dimensions in mm

## Revision History

IPP019N06NF2S

### Revision 2024-10-14, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-02-14	Release of final version
2.1	2022-05-19	Updated diagram 12 title
2.2	2024-10-14	Added trr and Qrr at diF/dt=100 A/μs

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### Published by

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