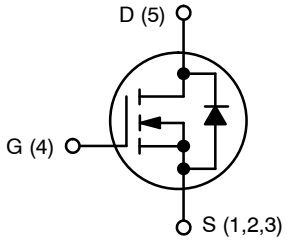
MOSFET - Power, Single N-Channel, Logic Level, SO8FL

40 V, 0.9 mΩ, 278 A

NTMFS0D9N04XL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.9 mΩ @ 10 V	278 A
	1.5 mΩ @ 4.5 V	



N−CHANNEL MOSFET

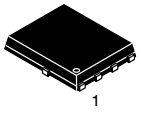
Features

- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low Q_{RR} with Soft Recovery to Minimize E_{RR} Loss and Voltage Spike
- Low Q_G and Capacitance to Minimize Driving and Switching Loss
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

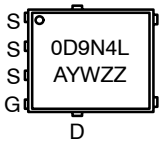
Typical Applications

- High Switching Frequency DC−DC Conversion
- Synchronous Rectification

MARKING DIAGRAM



DFN5 (SO−8FL)
CASE 488AA



0D9N4L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	40	V
Gate−to−Source Voltage	DC	V_{GS}	±20	V
Continuous Drain Current (Note 2)	T_C = 25°C	I_D	278	A
	T_C = 100°C		196	
Power Dissipation (Note 2)	T_C = 25°C	P_D	136	W
	T_C = 100°C		68	
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	1193	A
Pulsed Source Current (Body Diode)		I_{SM}	1193	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	207	A
Single Pulse Avalanche Energy (I_{PK} = 74 A) (Note 3)		E_{AS}	273	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 273 mJ is based on started T_J = 25°C, I_{AS} = 74 A, V_{DD} = 32 V, V_{GS} = 10 V, 100% avalanche tested.
4. $R_{\theta JCT}$ Thermal Resistance − Junction to Case Top = 20 °C/W.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.1	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	38	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA. Referenced to 25°C		16.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, T_J = 25°C			10	μA
		V_{DS} = 40 V, T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 35 A		0.77	0.9	mΩ
		V_{GS} = 6 V, I_D = 35 A		0.86	1.1	
		V_{GS} = 4.5 V, I_D = 28 A		1	1.5	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 180 μA	1.3		2.2	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 180 μA		−5.35		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 35 A		178		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		5160		pF
Output Capacitance	C_{OSS}			1350		
Reverse Transfer Capacitance	C_{RSS}			23		
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DS} = 20 V		52		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DD} = 20 V; I_D = 35 A		31		
		V_{GS} = 6 V, V_{DD} = 20 V; I_D = 35 A		41		
		V_{GS} = 10 V, V_{DD} = 20 V; I_D = 35 A		70		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DD} = 20 V; I_D = 35 A		8		
Gate−to−Source Charge	Q_{GS}			15		
Gate−to−Drain Charge	Q_{GD}			5		
Gate Plateau Voltage	V_{GP}			2.88		V
Gate Resistance	R_G	f = 1 MHz		0.6		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 20 V, I_D = 35 A, R_G = 2.5 Ω		21		ns
Rise Time	t_r			6		
Turn−Off Delay Time	$t_{d(OFF)}$			53		
Fall Time	t_f			4		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 35 A, T_J = 25°C		0.79	1.2	V
		V_{GS} = 0 V, I_S = 35 A, T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 300 A/μs, I_S = 35 A, V_{DD} = 20 V		31		ns
Charge Time	t_a			18		
Discharge Time	t_b			13		
Reverse Recovery Charge	Q_{RR}			67		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

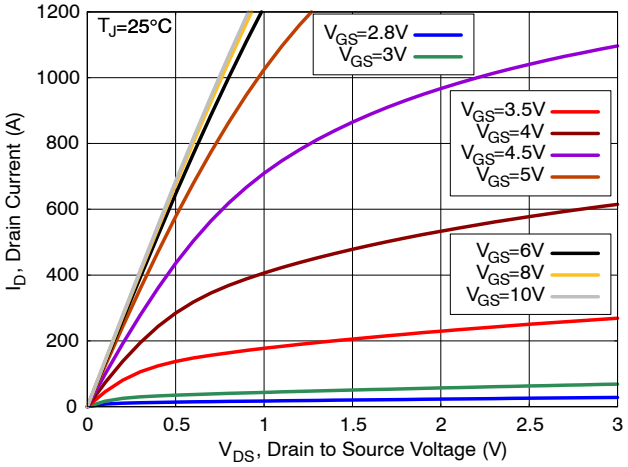


Figure 1. On−Region Characteristics

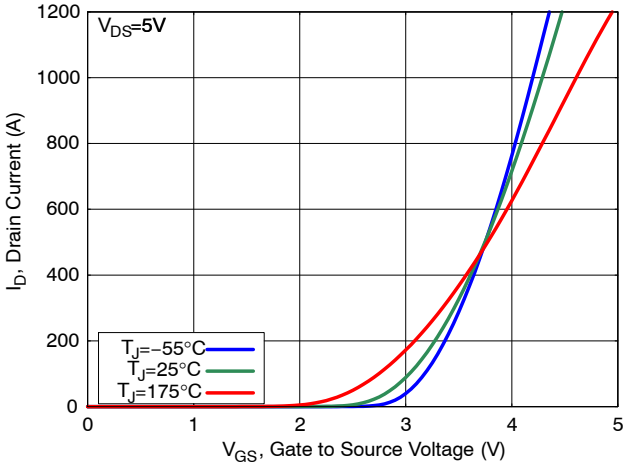


Figure 2. Transfer Characteristics

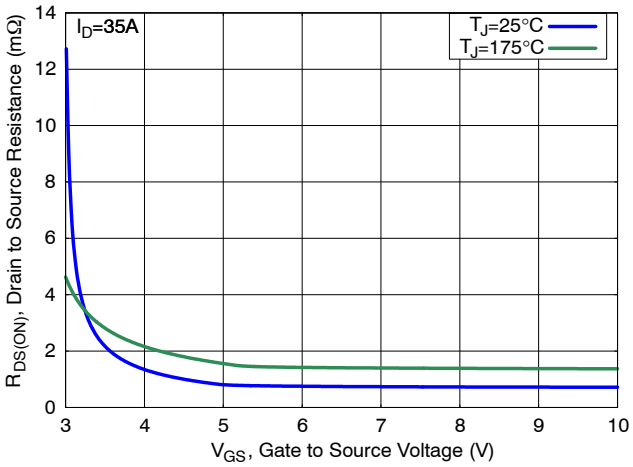


Figure 3. On−Resistance vs. Gate Voltage

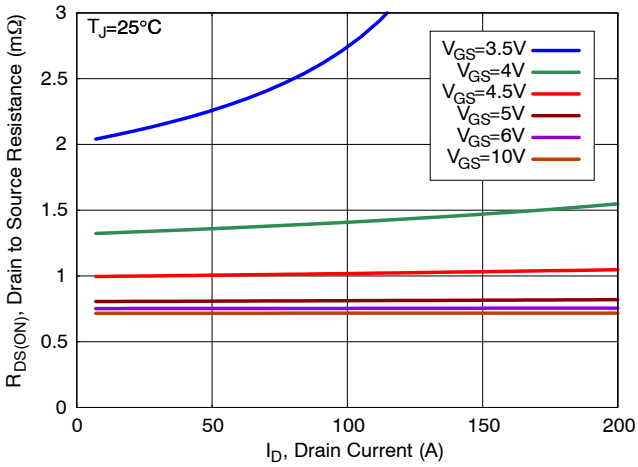


Figure 4. On−Resistance vs. Drain Current

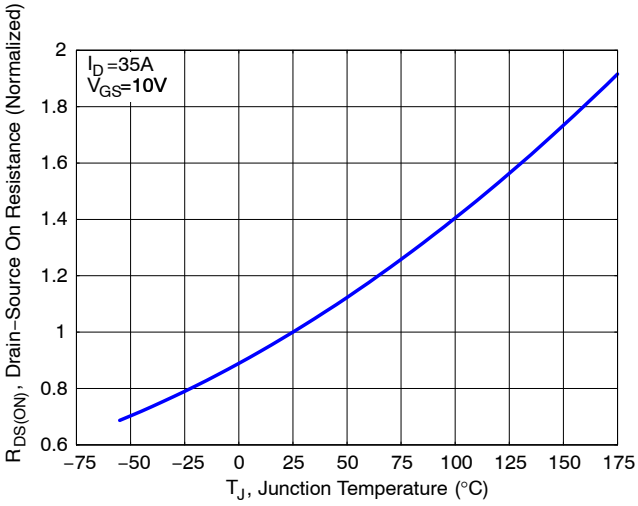


Figure 5. Normalized ON Resistance vs. Junction Temperature

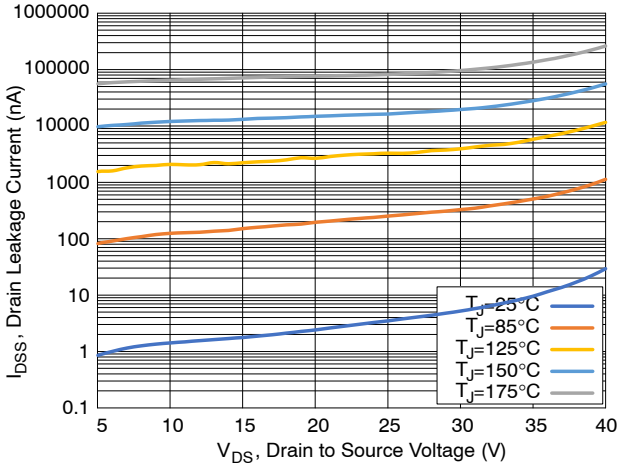


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

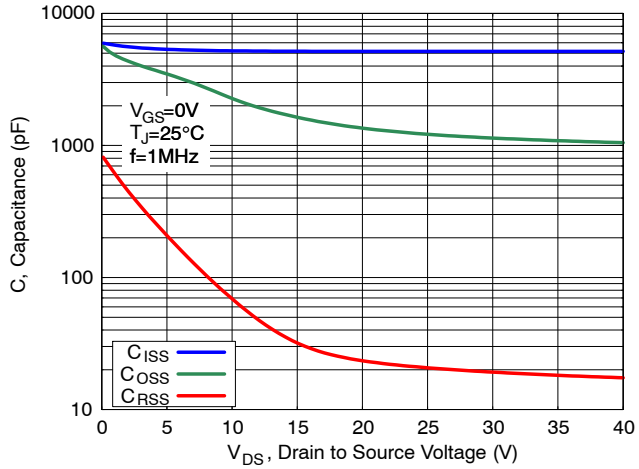


Figure 7. Capacitance Characteristics

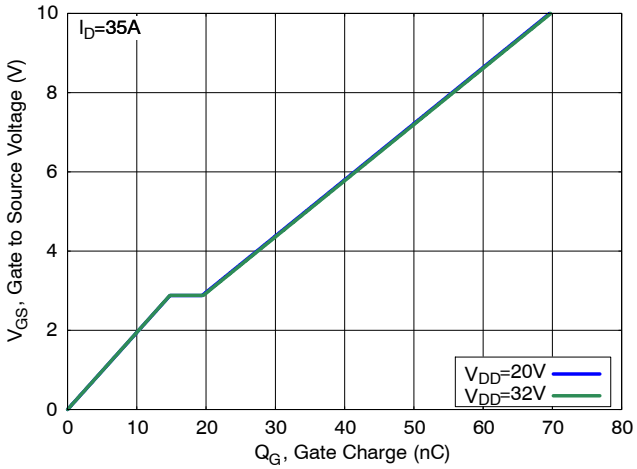


Figure 8. Gate Charge Characteristics

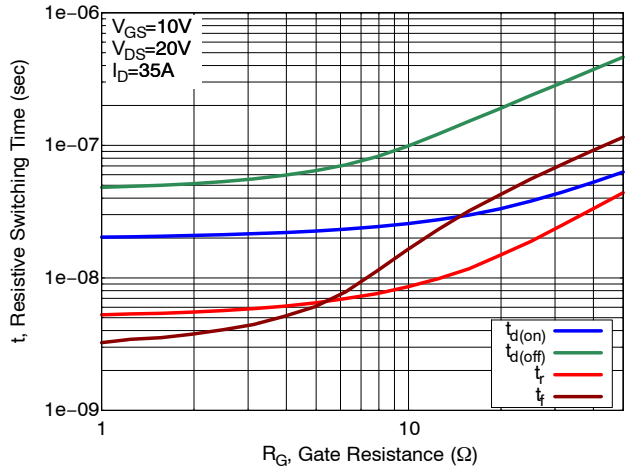


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

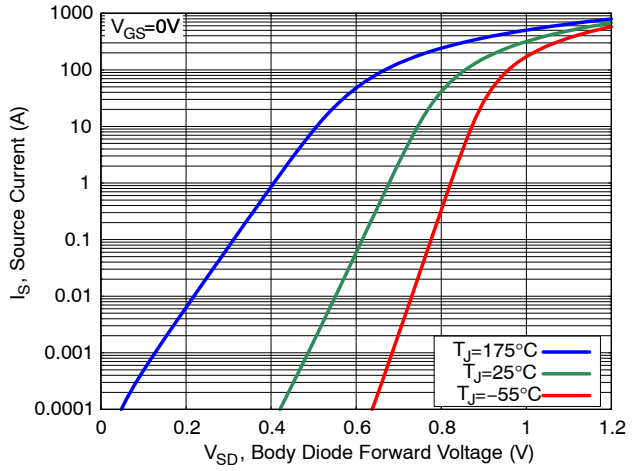


Figure 10. Diode Forward Characteristics

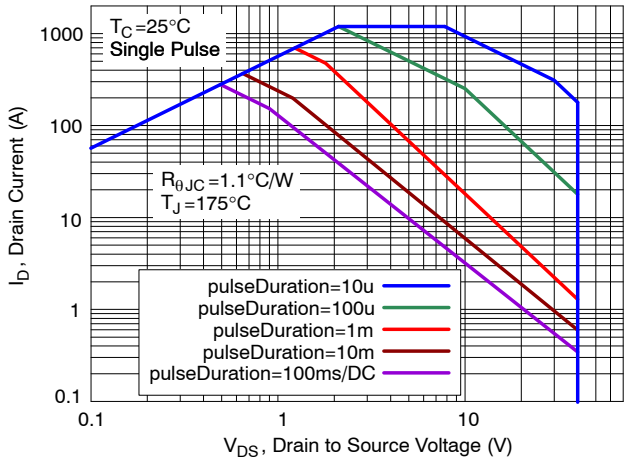


Figure 11. Safe Operating Area (SOA)

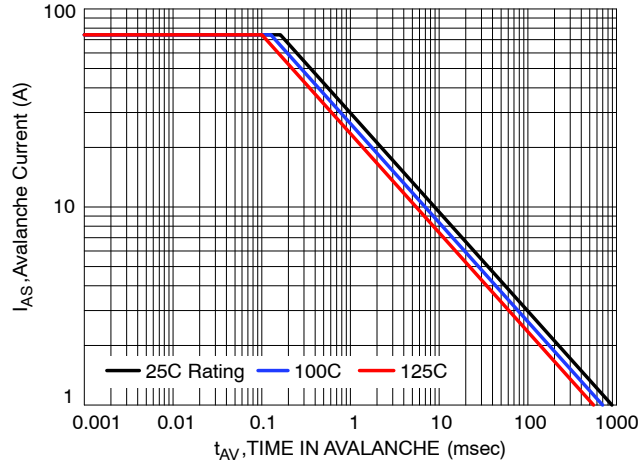


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS (CONTINUED)

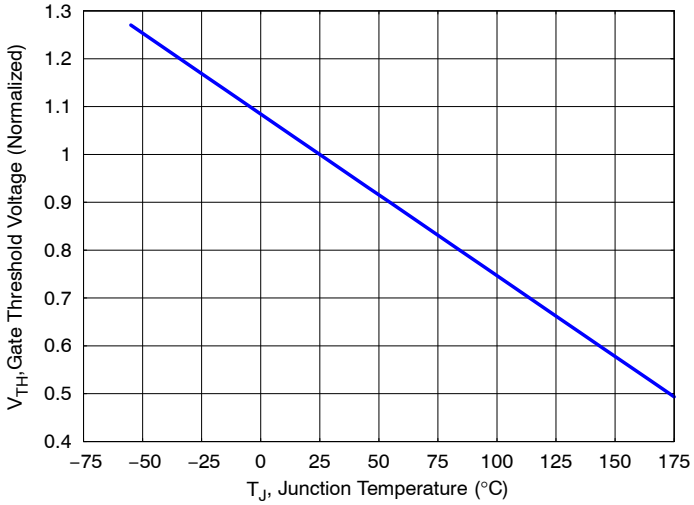


Figure 13. Gate Threshold Voltage vs. Junction Temperature

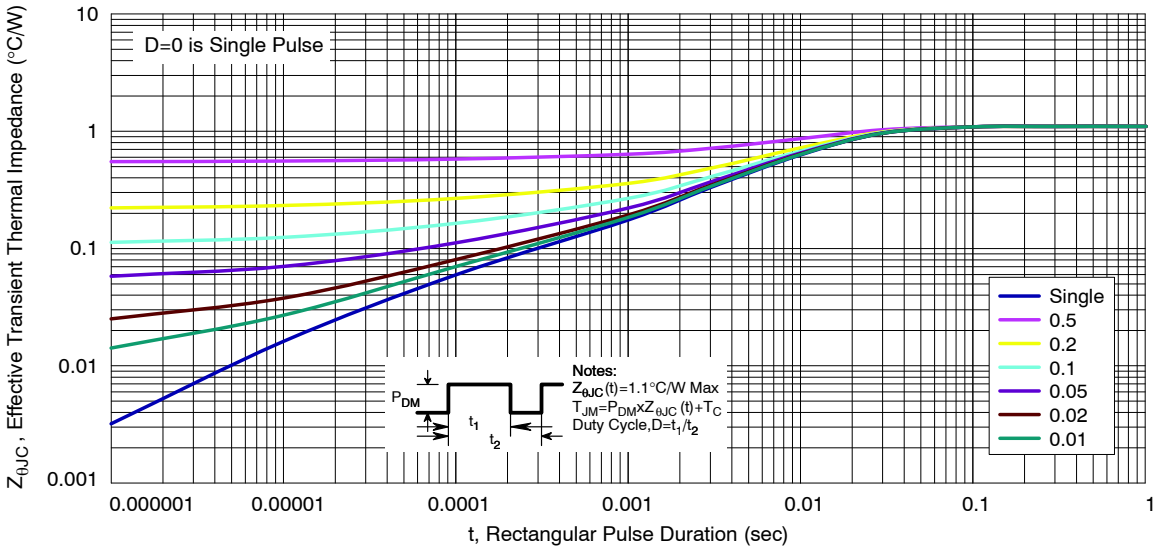
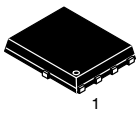


Figure 14. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS0D9N04XLT1G	0D9N4L	DFN5 (Pb−Free)	1500 / Tape & Reel

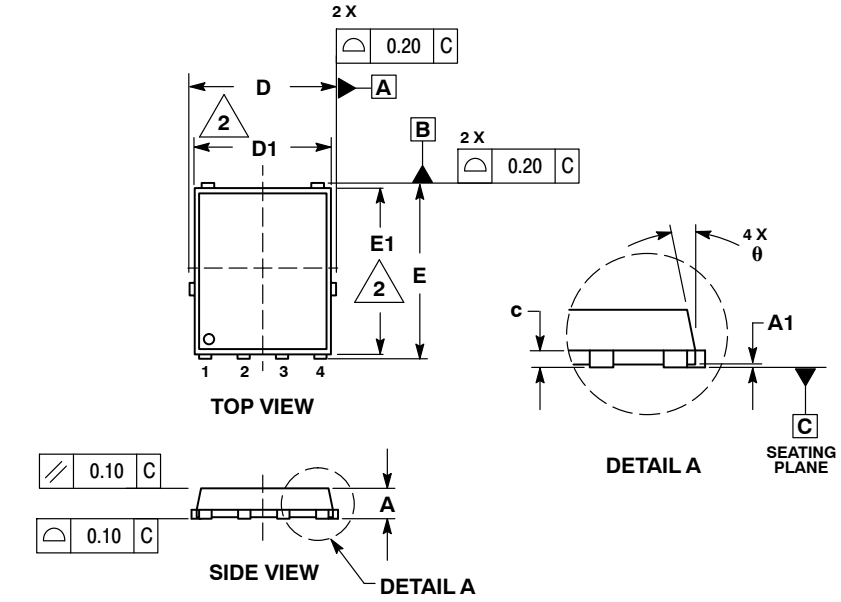
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

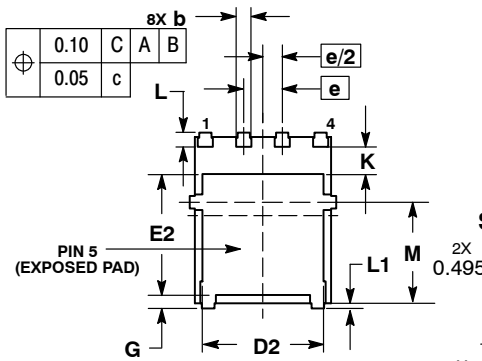
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

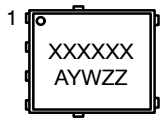


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



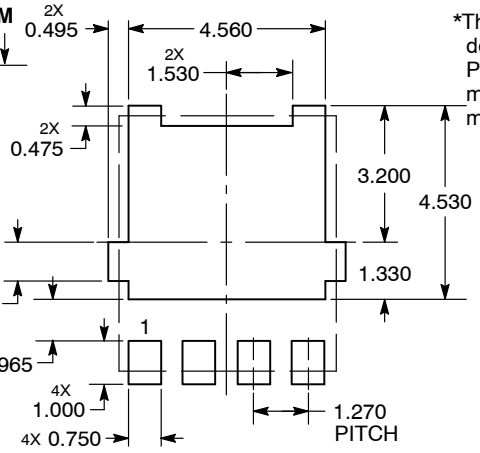
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales