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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild guestions@onsemi.com.

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April 2015

FDP083N15A

N-Channel PowerTrench[®] MOSFET 150 V, 117 A, 8.3 m Ω

Features

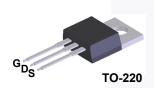
- $R_{DS(on)}$ = 6.85 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 75 A
- · Fast Switching Speed
- Low Gate Charge, Q_G = 64.5 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- · High Power and Current Handling Capability
- RoHS Compliant

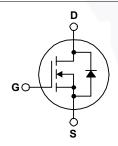
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- · Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter	FDP083N15A_F102	Unit
V _{DSS}	Drain to Source Voltage		150	V
V	Cata to Course Voltage	- DC	±20	V
V_{GSS}	Gate to Source Voltage	- AC (f > 1 Hz)	±30	_ v
	- Continuous (T _C = 25°C, Silicon Limited)		117	Α
ID	Drain Current	- Continuous (T _C = 100°C, Silicon Limited)	83	A
I _{DM}	Drain Current	- Pulsed (Note 1)	468	Α
E _{AS}	Single Pulsed Avalanche Ene	ergy (Note 2)	542	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6	V/ns
D	Power Dissipation	(T _C = 25°C)	294	W
P_{D}	Power Dissipation	- Derate Above 25°C	1.96	W/oC
T _J , T _{STG}	Operating and Storage Temp	erature Range	-55 to +175	°C
T _L	Maximum Lead Temperature	for Soldering, 1/8" from Case for 5 Seconds	300	οС

Thermal Characteristics

Symbol	Parameter	FDP083N15A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.51	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP083N15A_F102	FDP083N15A	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ}C$	150	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.08	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V	-	-	1	
		$V_{DS} = 120 \text{ V}, T_{C} = 150^{\circ}\text{C}$	-	-	500	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 75 A	-	6.85	8.30	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 75 A	-	139	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05.V.V 0.V		-	4645	6040	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	1445	1880	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		-\	100	-	pF
C _{iss}	Input Capacitance	7.57/.//		- \	4570	6040	pF
Coss	Output Capacitance	V _{DS} = 7 5V, V _{GS} = 0 V, f = 1 MHz		- \	460	1880	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		-	20	-	pF
Q _{g(tot)}	Total Gate Charge at 10V			-	64.5	84	nC
Q _{gs}	Gate to Source Gate Charge	V _{DS} = 120 V, I _D = 75 A,		-	19.1	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau	V _{GS} = 10 V		-	8.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	13.5	-	nC
ESR	Equivalent Series Resistance(G-S)	f = 1 MHz		-	2.5	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 75 V, I _D = 75 A,	-	22	54	ns
t _r		$V_{GS} = 10 \text{ V}, R_{G} = 4.7 \Omega$	/-	58	126	ns
t _{d(off)}	Turn-Off Delay Time		-	61	132	ns
t _f	Turn-Off Fall Time	(Note 4)	-	26	62	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	117	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	468	Α
V_{SD}	Drain to Source Diode Forward Voltage V _{GS} = 0 V, I _{SD} = 75 A		-	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 75 A,	-	96	//-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	268	-	nC

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. Starting T $_{J}$ = 25°C, L = 3 mH, I $_{SD}$ = 19 A.
- 3. I $_{SD} \leq 75$ A, di/dt ≤ 200 A/µs, V $_{DD} \leq BV_{DSS},$ starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

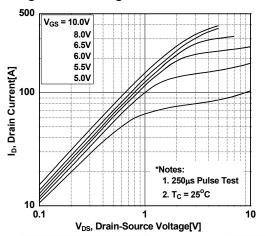


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

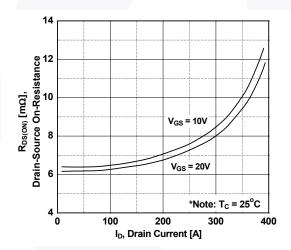


Figure 5. Capacitance Characteristics

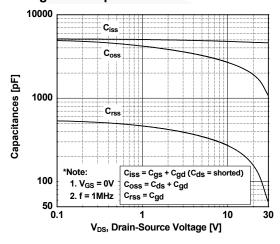


Figure 2. Transfer Characteristics

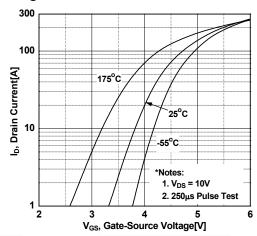


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

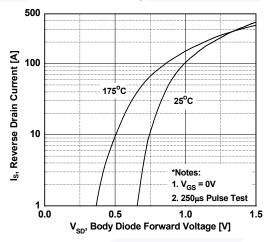
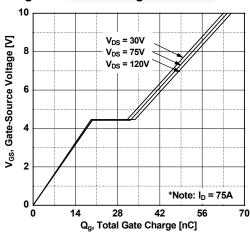


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

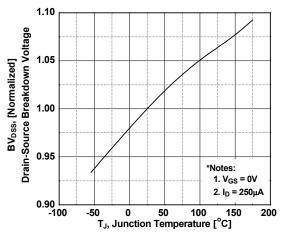


Figure 9. Maximum Safe Operating Area

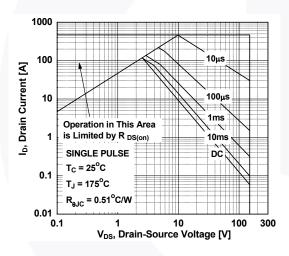


Figure 11. Unclamped Inductive Switching Capability

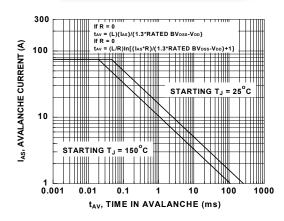


Figure 8. On-Resistance Variation vs. Temperature

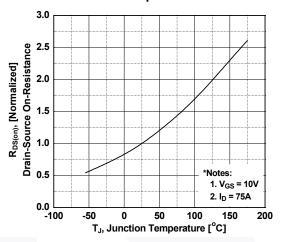
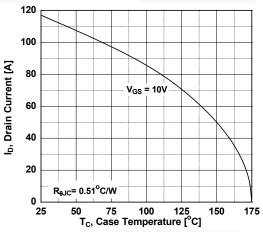
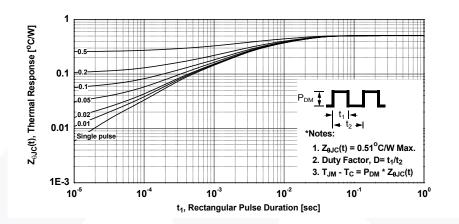


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



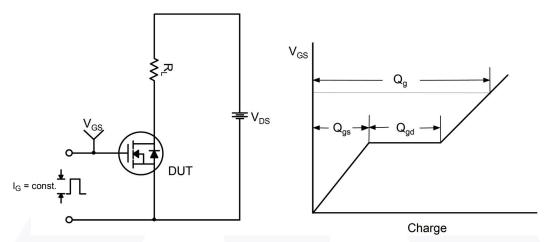


Figure 13. Gate Charge Test Circuit & Waveform

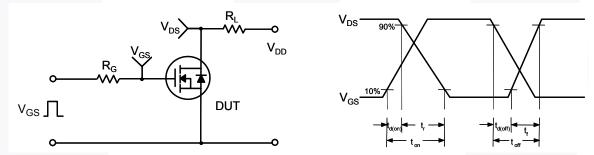


Figure 14. Resistive Switching Test Circuit & Waveforms

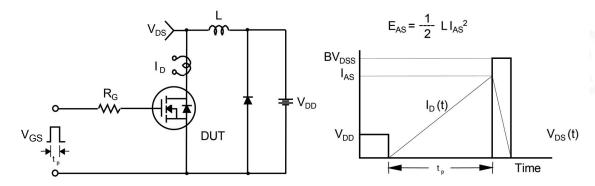


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

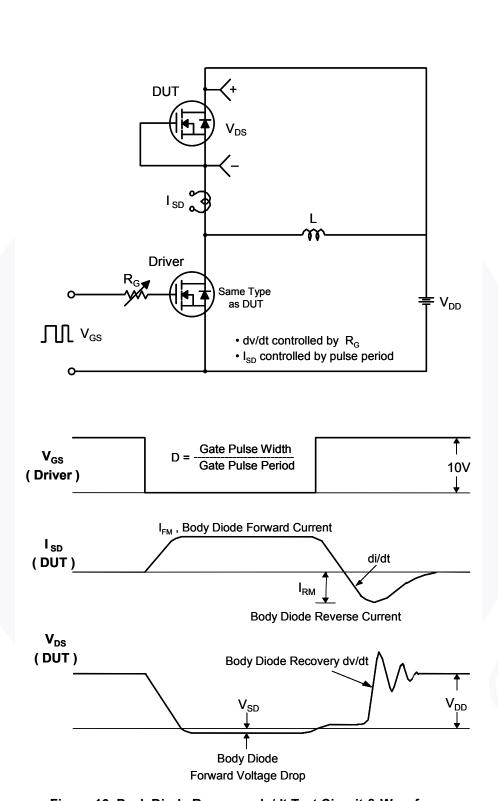
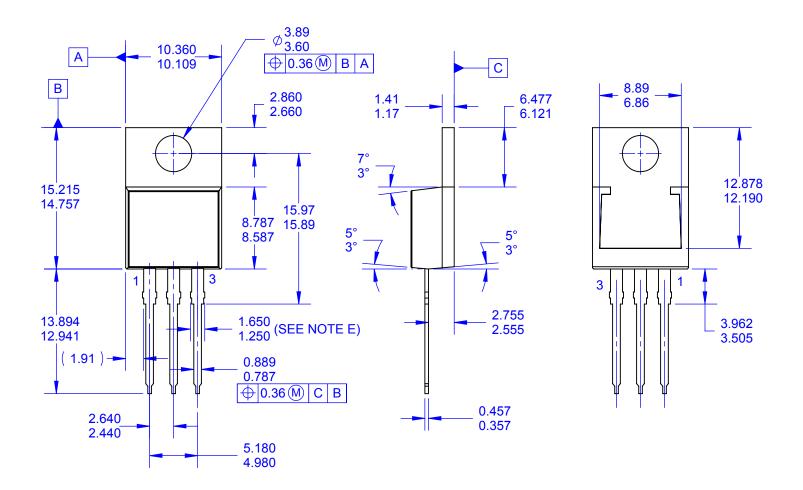
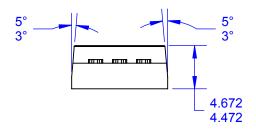


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms





NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm. F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.

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