

# PSMN1R0-100ASF

NextPower 100 V, 0.99 mOhm, N-channel MOSFET in CCPAK1212 package

6 December 2024

Product data sheet

## 1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

### 2. Features and benefits

- Low Q<sub>rr</sub> for higher efficiency and lower spiking
- 460 Amps I<sub>D(max)</sub> continuous current rating
- Low  $Q_G \times R_{DSon}$  FOM for high efficiency switching applications
- Strong avalanche energy rating (E<sub>as</sub>)
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212 package

## 3. Applications

- · Battery protection
- · High power full and half-bridge configurations
- · BLDC motor control
- OR-ing

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	-	-	460	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	-	1.55	kW
Static chara	acteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11	-	0.78	0.99	mΩ
Dynamic cl	haracteristics					
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	21	69.5	160	nC



# 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	S	source		
4	S	source	12 11 10 9 8 7	
5	S	source	<u> </u>	
6	S	source		D
7	D	drain		
8	D	drain		G T T
9	D	drain		mbb076 S
10	D	drain	1 2 3 4 5 6 CCPAK1212 (SOT8000A)	
11	D	drain	OOI AR1212 (0010000A)	
12	D	drain		
mb	D	mounting base; connected to drain		

# 6. Ordering information

**Table 3. Ordering information** 

Type number	number Package					
	Name	Description	Version			
PSMN1R0-100ASF	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A			

# 7. Marking

### Table 4. Marking codes

Type number	Marking code
PSMN1R0-100ASF	XP1F0S10A

## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_i$  = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	100	V
$V_{DGR}$	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ		-	100	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	1.55	kW
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	460	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	460	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 3		-	3296	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain	diode		'		•	
Is	source current	T <sub>mb</sub> = 25 °C		-	460	Α
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 µs; T <sub>mb</sub> = 25 °C		-	3296	Α
Avalanche ru	ıggedness				•	
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 117 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 218 μs; Fig. 4	[1]	-	1630	mJ
I <sub>AS</sub>	non-repetitive avalanche current	$V_{sup} \le 100 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 \text{ °C}; R_{GS} = 50 \Omega; Fig. 4$	[1]	-	117	А

#### [1] Protected by 100% test

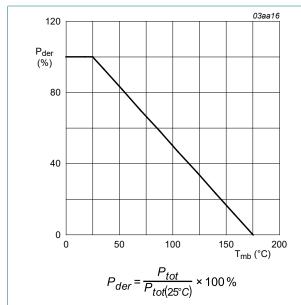
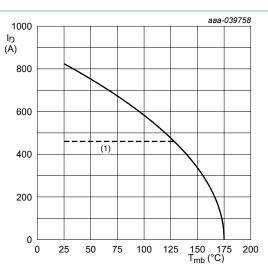


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



 $V_{GS} \ge 10 \text{ V}$  (1) 460 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

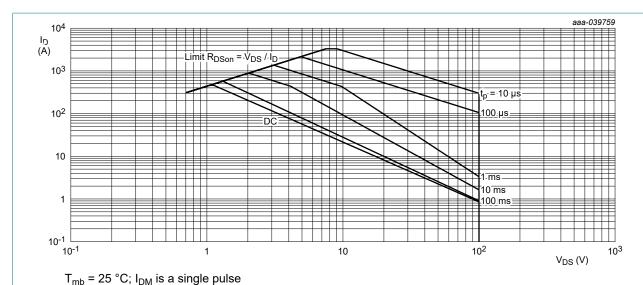


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

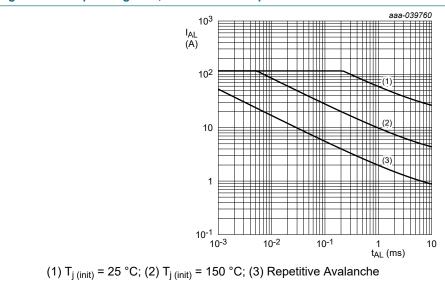


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	0.075	0.1	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	Fig. 6	-	58	-	K/W
		Fig. 7	-	29	-	K/W

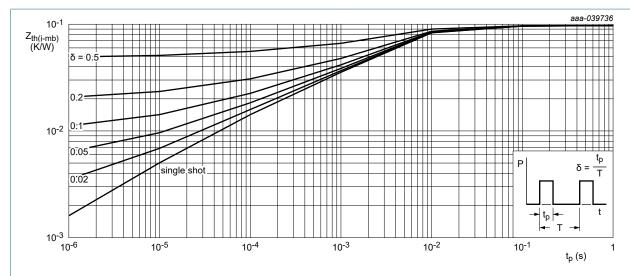
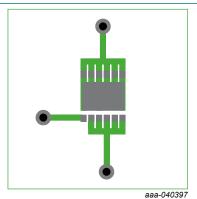
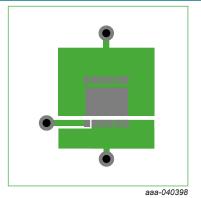


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



70 µm thick Copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



Copper area 25.4mm square; 70  $\mu$ m thick on FR4 board

Fig. 7. PCB layout for thermal resistance from junction to ambient

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	cteristics					_
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	100	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	90	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C	2	3	4	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>i</sub> = 175 °C	-	1.46	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>i</sub> = -55 °C	-	3.5	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-9.3	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.14	2	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	48	200	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>i</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>i</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; Fig. 11	-	0.78	0.99	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 100 °C; Fig. 12	-	1.2	1.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 12	-	1.7	2.3	mΩ
		V <sub>GS</sub> = 7 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	0.9	1.35	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>i</sub> = 25 °C	0.6	1.28	2.6	Ω
Dynamic cha	aracteristics		l			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>i</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	180	359	539	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C	-	314	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;	61	102	143	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	69.5	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	32.3	-	nC
$Q_{GD}$	gate-drain charge		21	69.5	160	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; Fig. 13; Fig. 14	-	4.3	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	14410	24017	33624	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	3334	5556	8889	pF
C <sub>rss</sub>	reverse transfer capacitance		12	123	321	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \Omega; V_{GS} = 10 \text{ V};$	-	92	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	90	-	ns
$t_{d(off)}$	turn-off delay time		-	232	-	ns
t <sub>f</sub>	fall time	1	-	129	-	ns
Source-drain	n diode		1	1	1	
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 25 °C; <u>Fig. 16</u>	_	0.74	1	V

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>rr</sub>		$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	75	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <u>Fig. 17</u>	-	99	-	nC

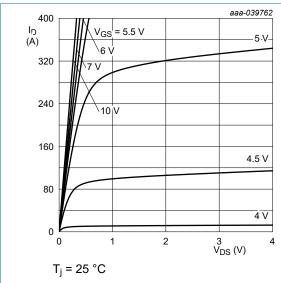


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

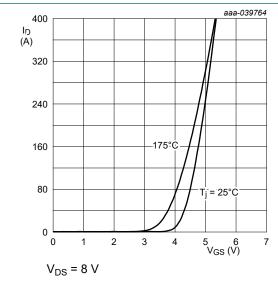


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

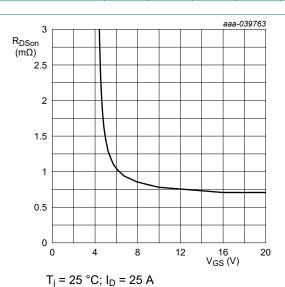


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

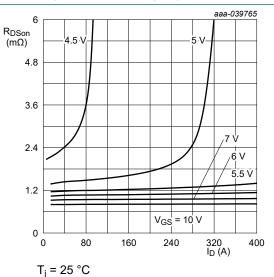


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

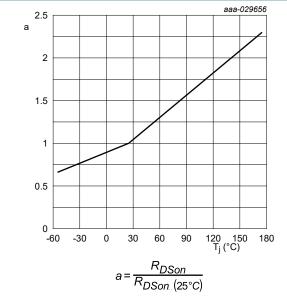


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

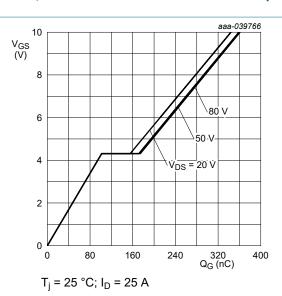


Fig. 13. Gate-source voltage as a function of gate charge; typical values

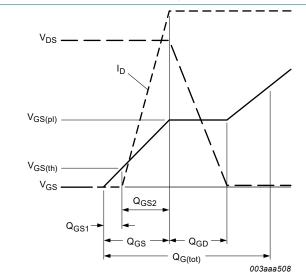


Fig. 14. Gate charge waveform definitions

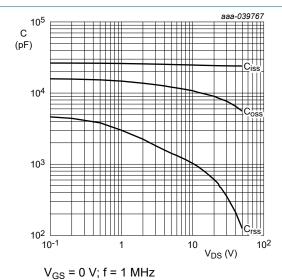


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

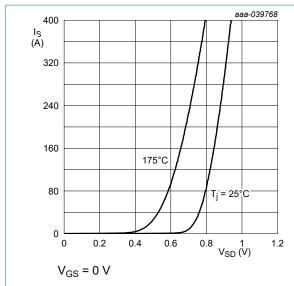


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

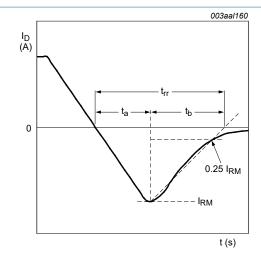


Fig. 17. Reverse recovery timing definition

# 11. Package outline

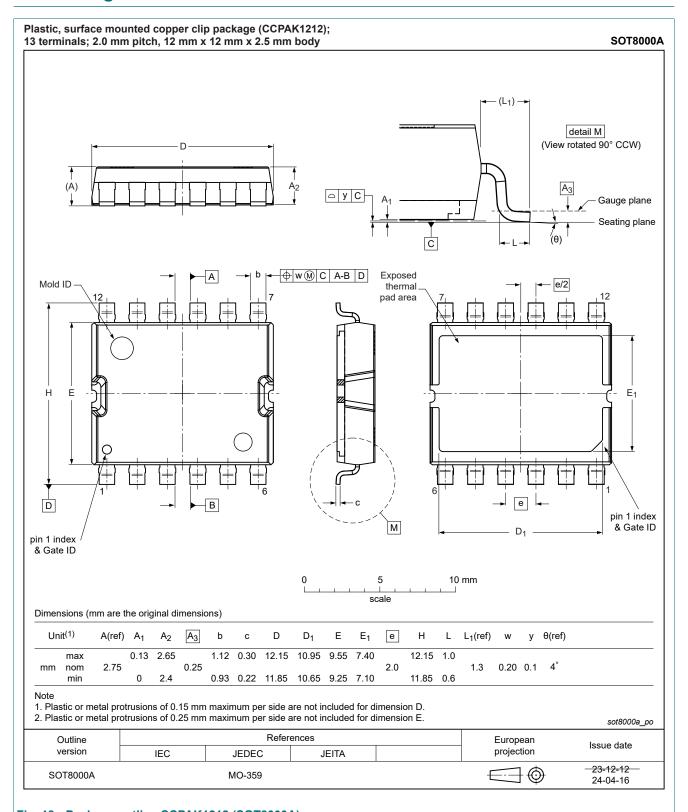
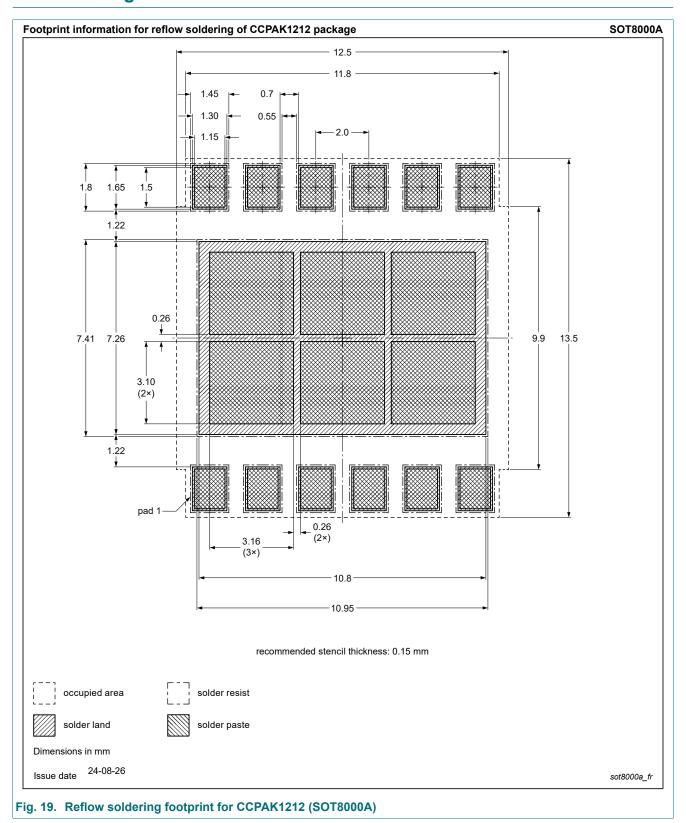


Fig. 18. Package outline CCPAK1212 (SOT8000A)

# 12. Soldering



## 13. Legal information

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## **Contents**

1.	General description	1
2.	Features and benefits	1
3.	Applications	1
4.	Quick reference data	1
5.	Pinning information	2
6.	Ordering information	2
7.	Marking	2
8.	Limiting values	3
9.	Thermal characteristics	4
10	. Characteristics	6
11.	. Package outline	10
12	. Soldering	11
13	Legal information	12

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