

MOSFET

PG-T0247-3

StrongIRFET™ Power MOSFET, 100 V

Features

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- 175°C operating temperature
- Hard Switched and High Frequency Circuits
- Product validation according to JEDEC standard

Benefits

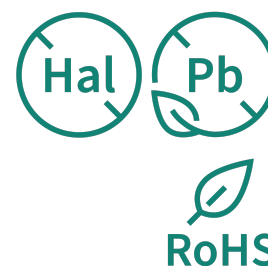
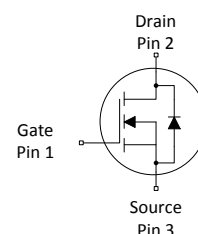
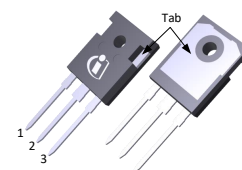
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Pb-free lead plating; RoHS compliant
- Lead free, Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	2.6	mΩ
I_D	195	A
Q_{oss}	149	nC
Q_G (0V..10V)	363	nC



Type / Ordering code	Package	Marking	Related links
IRFPW4468PbF	PG-T0247-3	IRFPW4468	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	195 150 25	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	780	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	740	mJ	$I_D=180\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	517 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 13 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.2	0.29	°C/W	-
Thermal resistance, junction - ambient ⁵⁾	R_{thJA}	-	-	40	°C/W	
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.24	-	°C/W	

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS}=V_{GS}$, $I_D=1000\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.27	2.60	m Ω	$V_{GS}=10\text{ V}$, $I_D=180\text{ A}$
Gate resistance	R_G	-	0.90	-	Ω	-
Transconductance ⁶⁾	g_{fs}	185	370	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=180\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	22000	29000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}	-	1300	1700	pF	
Reverse transfer capacitance ⁷⁾	C_{rss}	-	580	1000	pF	
Turn-on delay time	$t_{d(on)}$	-	53	-	ns	$V_{DD}=65\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=180\text{ A}$, $R_{G,ext}=2.7\text{ }\Omega$
Rise time	t_r	-	245	-	ns	
Turn-off delay time	$t_{d(off)}$	-	171	-	ns	
Fall time	t_f	-	278	-	ns	

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	104	-	nC	$V_{DD}=50\text{ V}$, $I_D=180\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	65	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}	-	96	144	nC	
Switching charge	Q_{sw}	-	134	-	nC	
Gate charge total ⁹⁾	Q_g	-	363	540	nC	
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	312	-	nC	
Output charge ⁹⁾	Q_{oss}	-	149	224	nC	

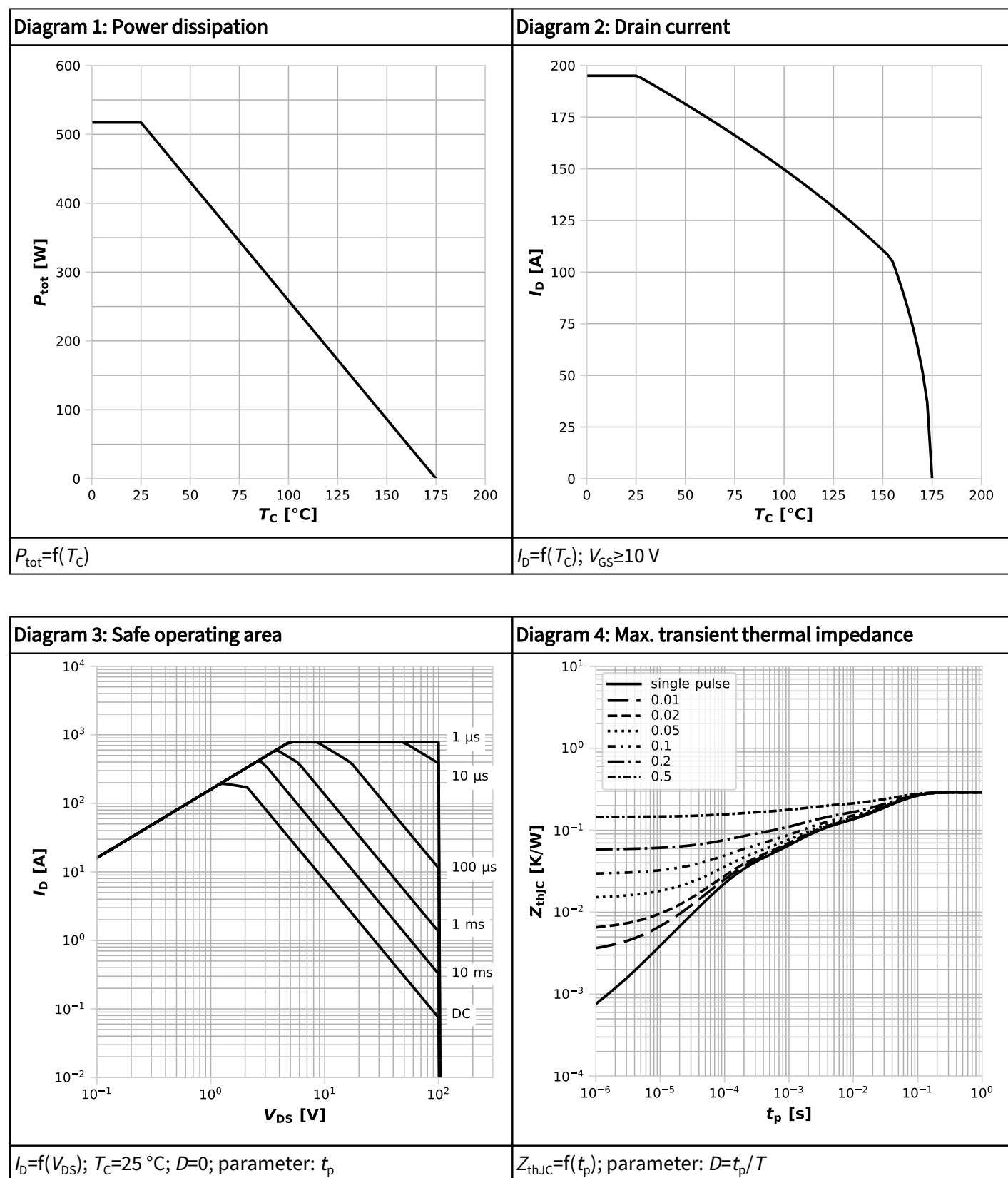
⁸⁾ See figure 16 for gate charge parameter definition.

⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	177	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	780	A	
Diode forward voltage	V_{SD}	-	0.96	1.3	V	$V_{GS}=0\text{ V}$, $I_F=180\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	88	-	ns	$V_R=85\text{ V}$, $I_F=180\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	333	-	nC	

4 Electrical characteristics diagrams



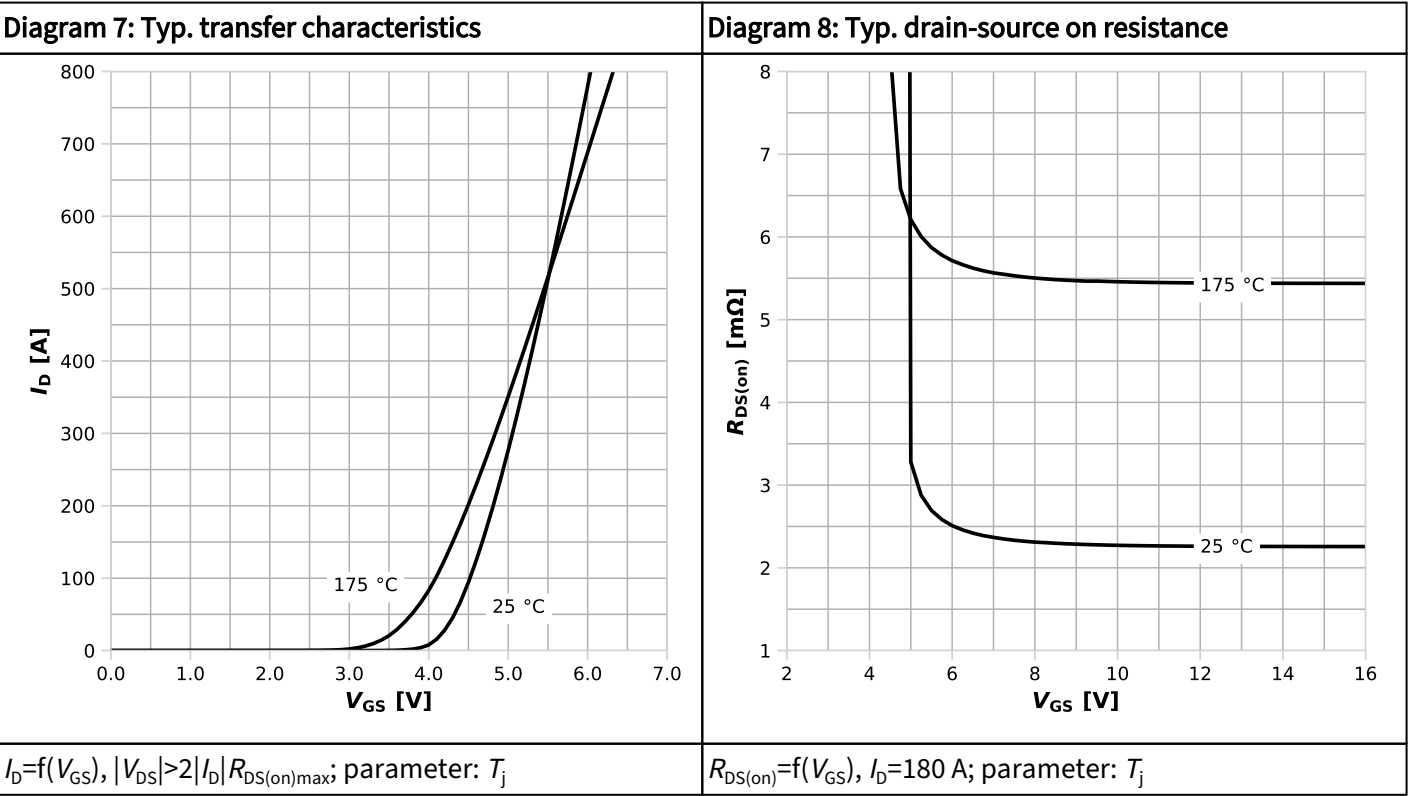
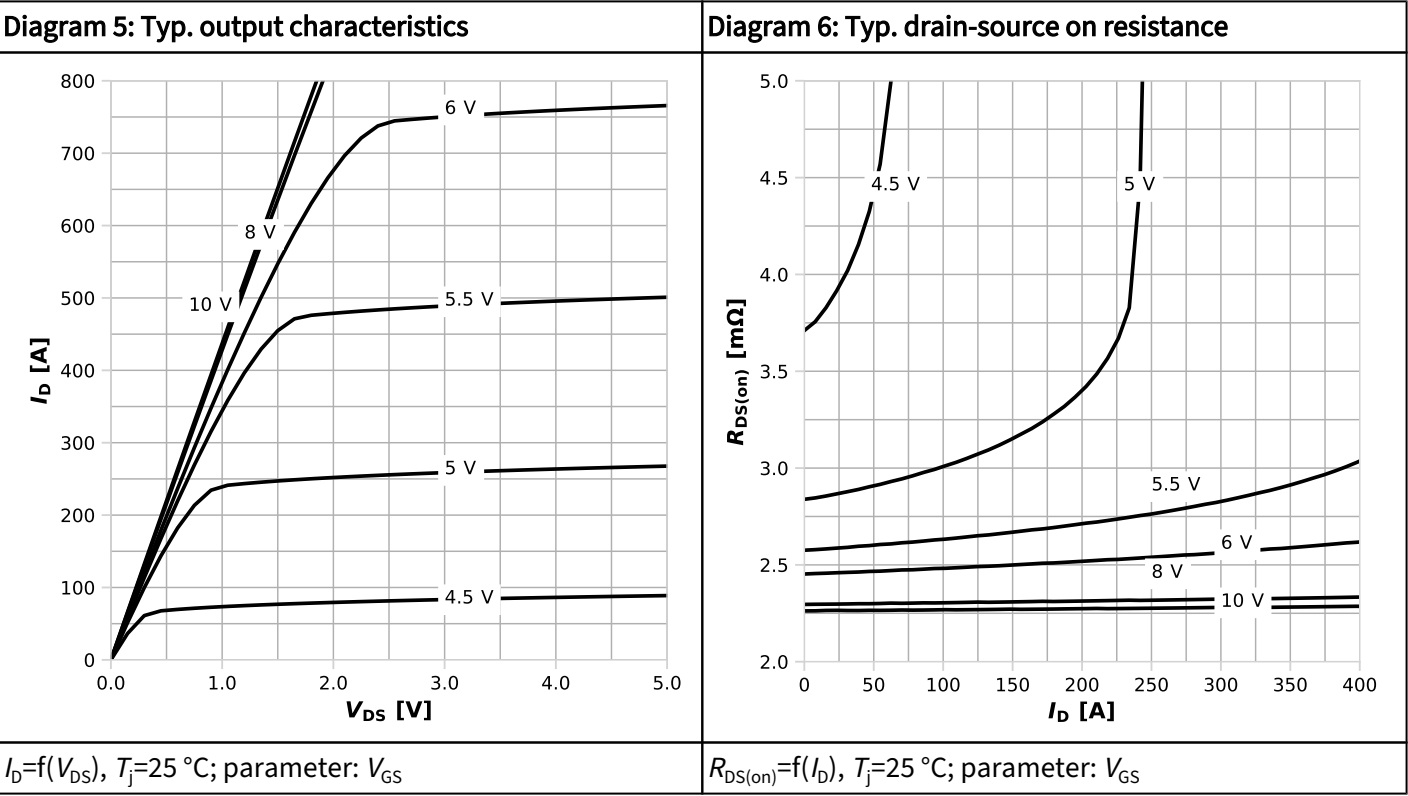
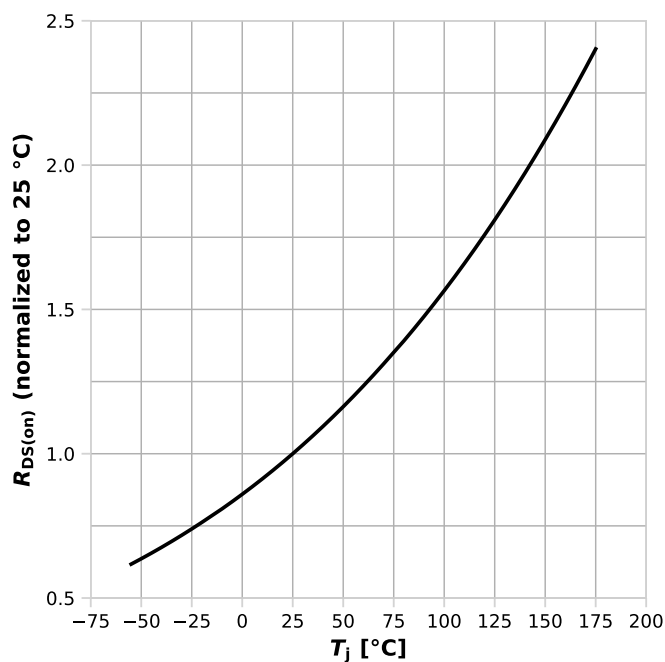
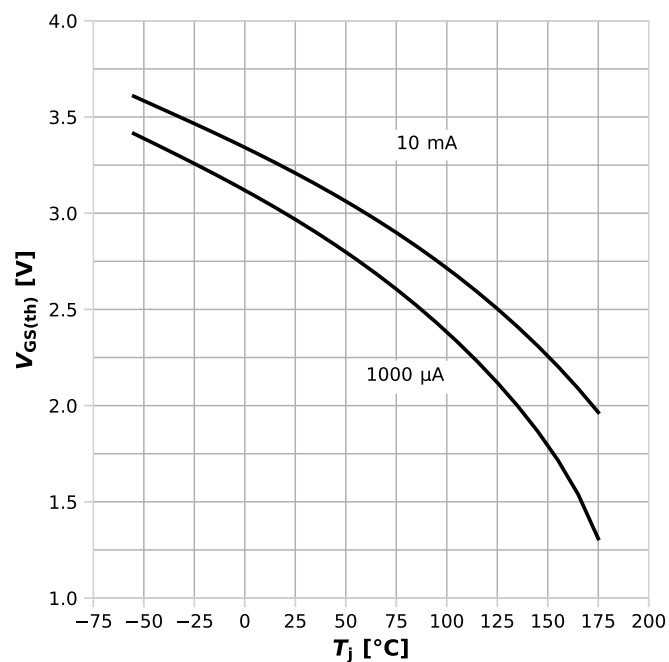


Diagram 9: Normalized drain-source on resistance



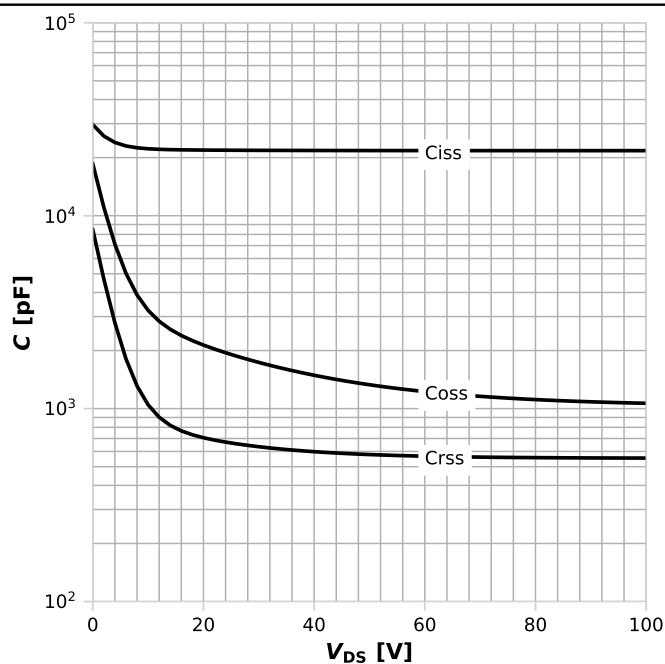
$R_{DS(on)} = f(T_j)$, $I_D = 180$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



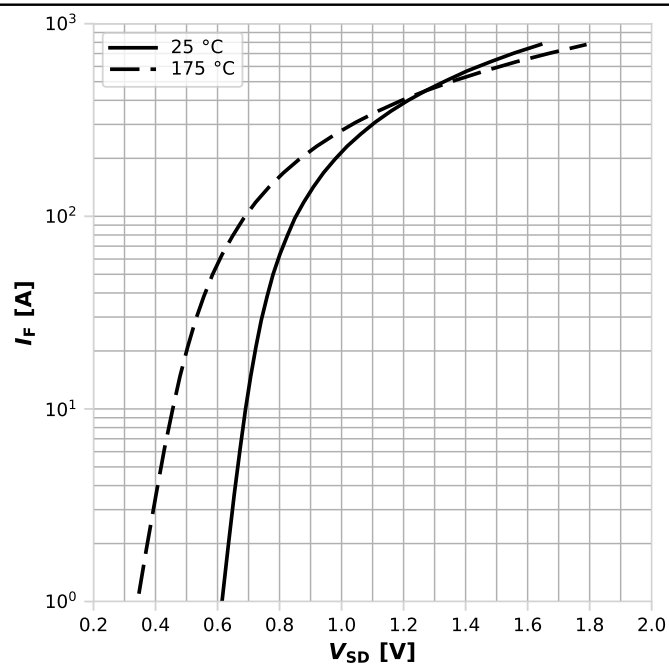
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



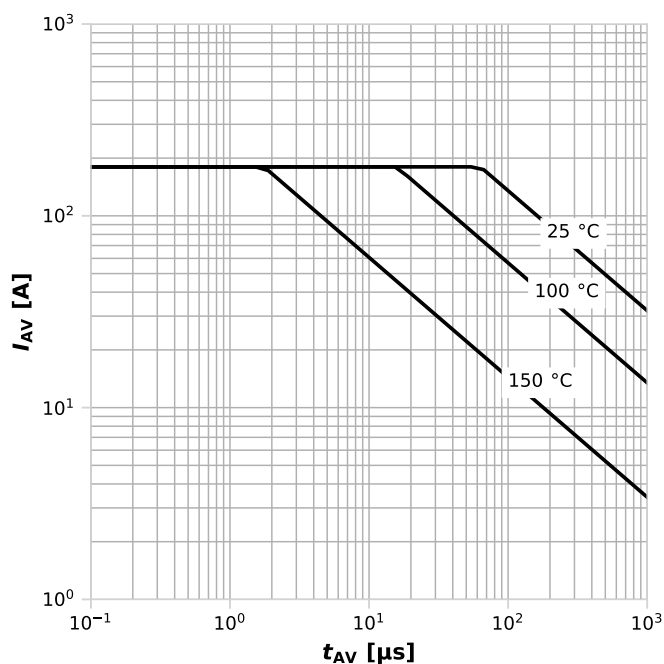
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



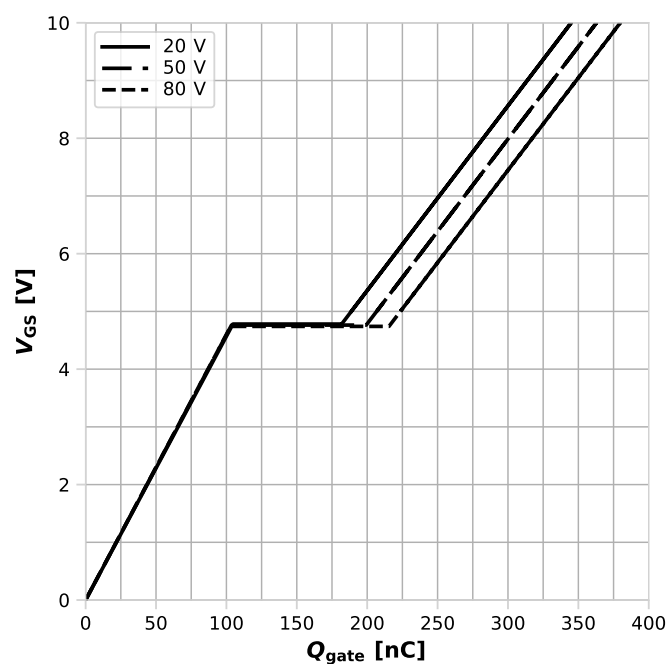
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



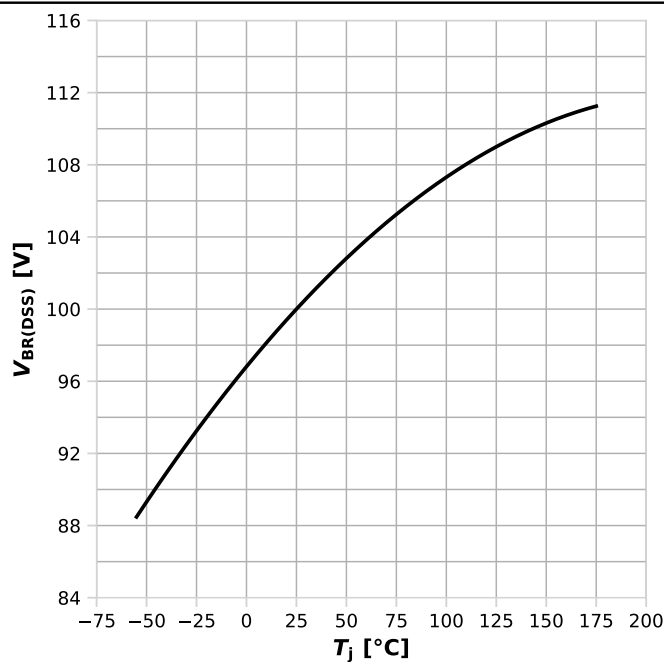
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



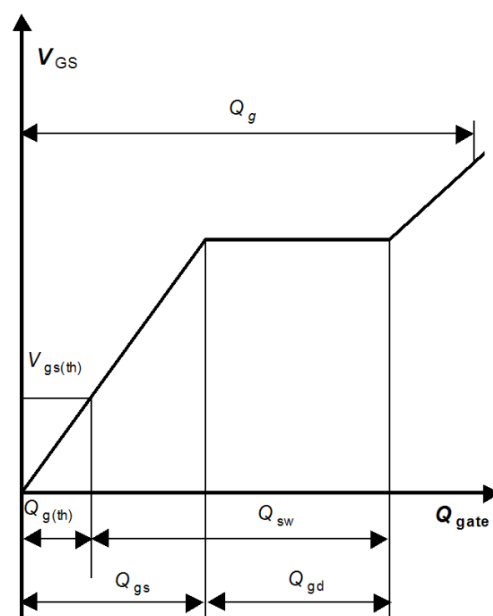
$V_{GS}=f(Q_{gate})$, $I_D=180\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



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5 Package outlines

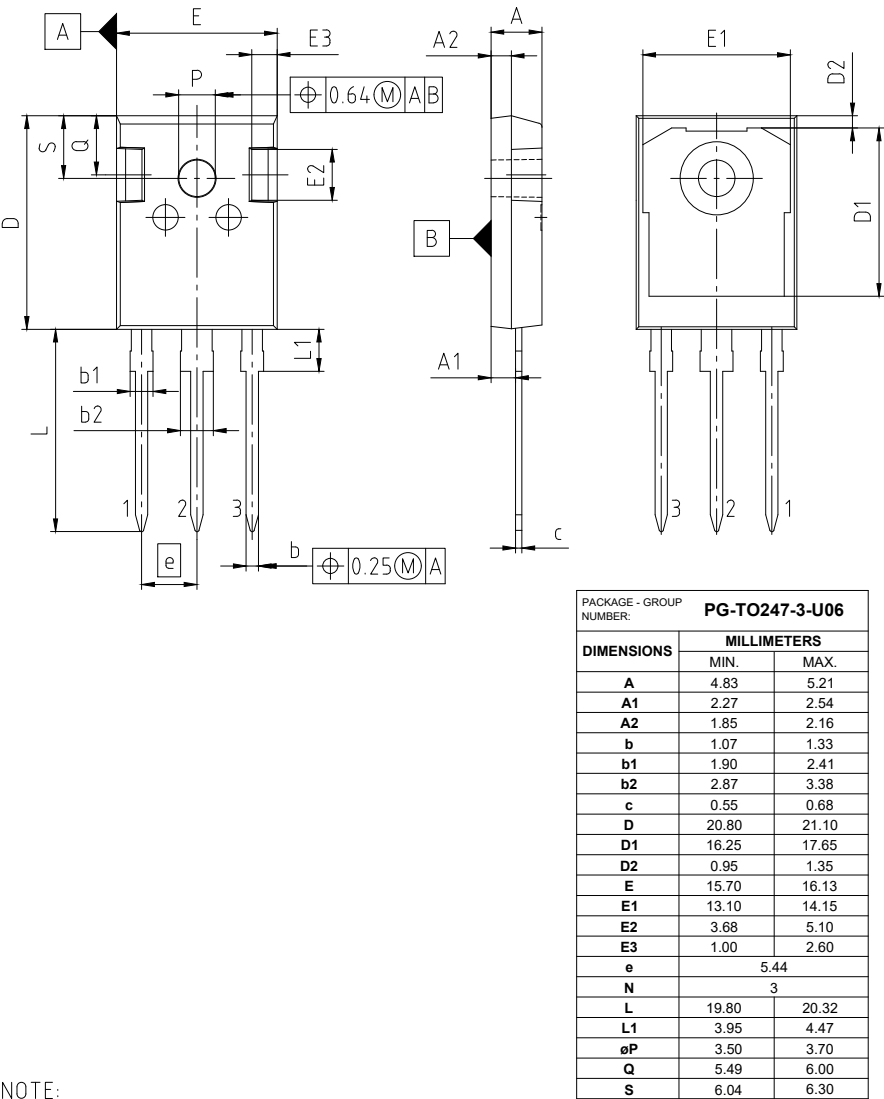


Figure 1 Outline PG-T0247-3, dimensions in mm

Revision history

IRFPW4468PbF

Revision 2025-01-10, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-01-10	Release of final datasheet

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81726 München, Germany
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