

## CoolSiC™ M1

### CoolSiC™ MOSFET 650 V G1

The 650 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 650V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

## Features

- Optimized switching behavior at higher currents
- Commutation robust fast body diode with low  $Q_{fr}$
- Superior gate oxide reliability
- $T_{j,max}=175^{\circ}\text{C}$  and excellent thermal behavior
- Lower  $R_{DS(on)}$  and pulse current dependency on temperature
- Increased avalanche capability
- Compatible with standard drivers
- Kelvin source provides up to 4 times lower switching losses

## Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Suitable for topologies with continuous hard commutation
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density

## Potential applications

- Telecom and Server SMPS
- UPS (uninterruptable power supplies)
- Solar PV inverters
- EV charging infrastructure
- Energy storage and battery formation
- Class D amplifiers

## Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J = 25^{\circ}\text{C}$	650	V
$R_{DS(on),typ}$	107	mΩ
$R_{DS(on),max}$	141	mΩ
$Q_{G,typ}$	15	nC
$I_{DM,max}$	47	A
$Q_{oss} @ 400 \text{ V}$	35	nC
$E_{oss} @ 400 \text{ V}$	5.3	μJ

Type/Ordering Code	Package	Marking	Related Links
IMBG65R107M1H	PG-TO263-7	65R107M1	see Appendix A

PG-TO263-7

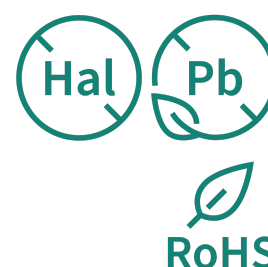
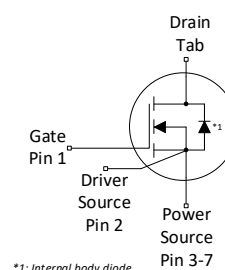
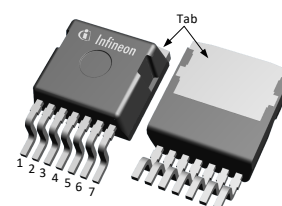




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## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current <sup>1)</sup>	$I_{\text{DDC}}$	-	-	24 17	A	$T_c = 25\text{ °C}$ $T_c = 100\text{ °C}$
Peak drain current <sup>2)</sup>	$I_{\text{DM}}$	-	-	47	A	$T_c = 25\text{ °C}$ , $V_{\text{GS}} = 18\text{ V}$
Avalanche energy, single pulse	$E_{\text{AS}}$	-	-	76	mJ	$I_D = 2.8\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11
Avalanche energy, repetitive	$E_{\text{AR}}$	-	-	0.38	mJ	$I_D = 2.8\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11
Avalanche current, single pulse	$I_{\text{AS}}$	-	-	2.8	A	-
MOSFET $dv/dt$ ruggedness	$dv/dt$	-	-	200	V/ns	$V_{\text{DS}} = 0\ldots 400\text{ V}$
Gate source voltage (static) <sup>3)</sup>	$V_{\text{GS}}$	-5	-	23	V	-
Gate source voltage (transient)	$V_{\text{GS}}$	-7	-	25	V	$t_{\text{pulse}} \leq 1\%$ duty cycle/ $f_{\text{sw}}$
Power dissipation	$P_{\text{tot}}$	-	-	110	W	$T_c = 25\text{ °C}$
Storage temperature	$T_{\text{stg}}$	-55	-	150	°C	-
Operating junction temperature	$T_j$	-55	-	175	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous reverse drain current <sup>1)</sup>	$I_{\text{SDC}}$	-	-	24 16	A	$V_{\text{GS}} = 18\text{ V}$ , $T_c = 25\text{ °C}$ $V_{\text{GS}} = 0\text{ V}$ , $T_c = 25\text{ °C}$
Peak reverse drain current <sup>2)</sup>	$I_{\text{SM}}$	-	-	47	A	$T_c = 25\text{ °C}$ , $t_p \leq 250\text{ ns}$
Insulation withstand voltage	$V_{\text{ISO}}$	-	-	n.a.	V	$V_{\text{rms}}$ , $T_c = 25\text{ °C}$ , $t = 1\text{ min}$

<sup>1)</sup> Limited by  $T_{j,\text{max}}$ .

<sup>2)</sup> Pulse width  $t_{\text{pulse}}$  limited by  $T_{j,\text{max}}$ .

<sup>3)</sup> The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	1.36	°C/W	-
Thermal resistance, junction - ambient	$R_{th(j-a)}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient, SMD version	$R_{th(j-a)}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Operating range

**Table 4** Operating range

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots <sup>4)</sup>	$V_{GS}$	-2	-	20	V	-
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

4)

**Important notice:** If the gate source voltage of the device in application exceeds the operating range (Table 4), the device  $R_{DS(on)}$  and  $V_{GS(th)}$  might exceed the maximum value stated in the datasheet at the end of the lifetime of the device. In order to ensure sound operation of the device over the planned lifetime, the maximum ratings (Table 2) and the CoolSiC™ MOSFET 650V M1 trench power device application note AN\_1907\_PL52\_1911\_144109 must be considered.

## 4 Electrical characteristics

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 5 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS}$	650	-	-	V	$V_{GS} = 0\text{ V}$ , $I_D = 0.26\text{ mA}$
Gate threshold voltage <sup>5)</sup>	$V_{GS(th)}$	3.5	4.5	5.7	V	$V_{DS} = V_{GS}$ , $I_D = 2.6\text{ mA}$
Zero gate voltage drain current	$I_{DSS}$	-	1 3	100 -	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$ $V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 175\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	107 150	141 -	m $\Omega$	$V_{GS} = 18\text{ V}$ , $I_D = 8.9\text{ A}$ , $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$ , $I_D = 8.9\text{ A}$ , $T_j = 175\text{ °C}$
Internal gate resistance	$R_{G,int}$	-	12.0	-	$\Omega$	$f = 1\text{ MHz}$

<sup>5)</sup> Tested after 1 ms pulse at  $V_{GS} = +20\text{ V}$ .

**Table 6 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	496	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Reverse transfer capacitance	$C_{rss}$	-	6.5	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Output capacitance <sup>6)</sup>	$C_{oss}$	-	58	75	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$ , $f = 250\text{ kHz}$
Output charge <sup>6)</sup>	$Q_{oss}$	-	35	46	nC	calculation based on $C_{oss}$
Effective output capacitance, energy related <sup>7)</sup>	$C_{o(er)}$	-	66	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0...400\text{ V}$
Effective output capacitance, time related <sup>8)</sup>	$C_{o(tr)}$	-	87	-	pF	$I_D = \text{constant}$ , $V_{GS} = 0\text{ V}$ , $V_{DS} = 0...400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	5.8	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ , $I_D = 8.9\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ; see table 10
Rise time	$t_r$	-	6.7	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ , $I_D = 8.9\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ; see table 10
Turn-off delay time	$t_{d(off)}$	-	10.1	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ , $I_D = 8.9\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ; see table 10
Fall time	$t_f$	-	7.0	-	ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = 0/18\text{ V}$ , $I_D = 8.9\text{ A}$ , $R_{G,ext} = 1.8\text{ }\Omega$ ; see table 10

- 6) Maximum specification is defined by calculated six sigma upper confidence bound.
- 7)  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.
- 8)  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

**Table 7 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	4	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 8.9\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	$Q_{GD}$	-	3	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 8.9\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Total gate charge	$Q_G$	-	15	-	nC	$V_{DD} = 400\text{ V}$ , $I_D = 8.9\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$

**Table 8 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	$V_{SD}$	-	4.0	-	V	$V_{GS} = 0\text{ V}$ , $I_S = 8.9\text{ A}$ , $T_j = 25\text{ °C}$
MOSFET forward recovery time	$t_{fr}$	-	17.7	-	ns	$V_{DD} = 400\text{ V}$ , $I_S = 8.9\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET forward recovery charge <sup>9)</sup>	$Q_{fr}$	-	47	-	nC	$V_{DD} = 400\text{ V}$ , $I_S = 8.9\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET peak forward recovery current	$I_{frm}$	-	5.2	-	A	$V_{DD} = 400\text{ V}$ , $I_S = 8.9\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9

- <sup>9)</sup>  $Q_{fr}$  includes  $Q_{oss}$ .

5 Electrical characteristics diagrams

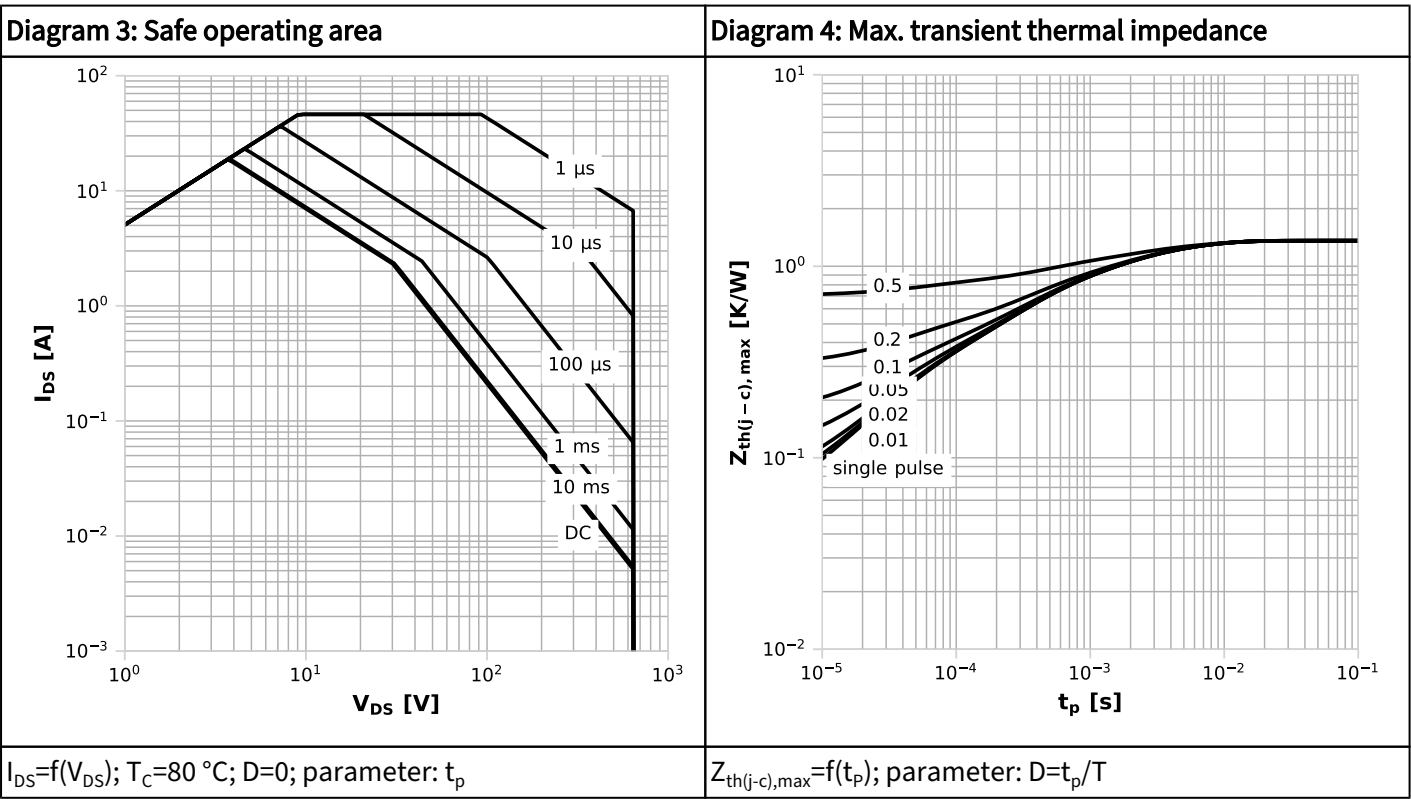
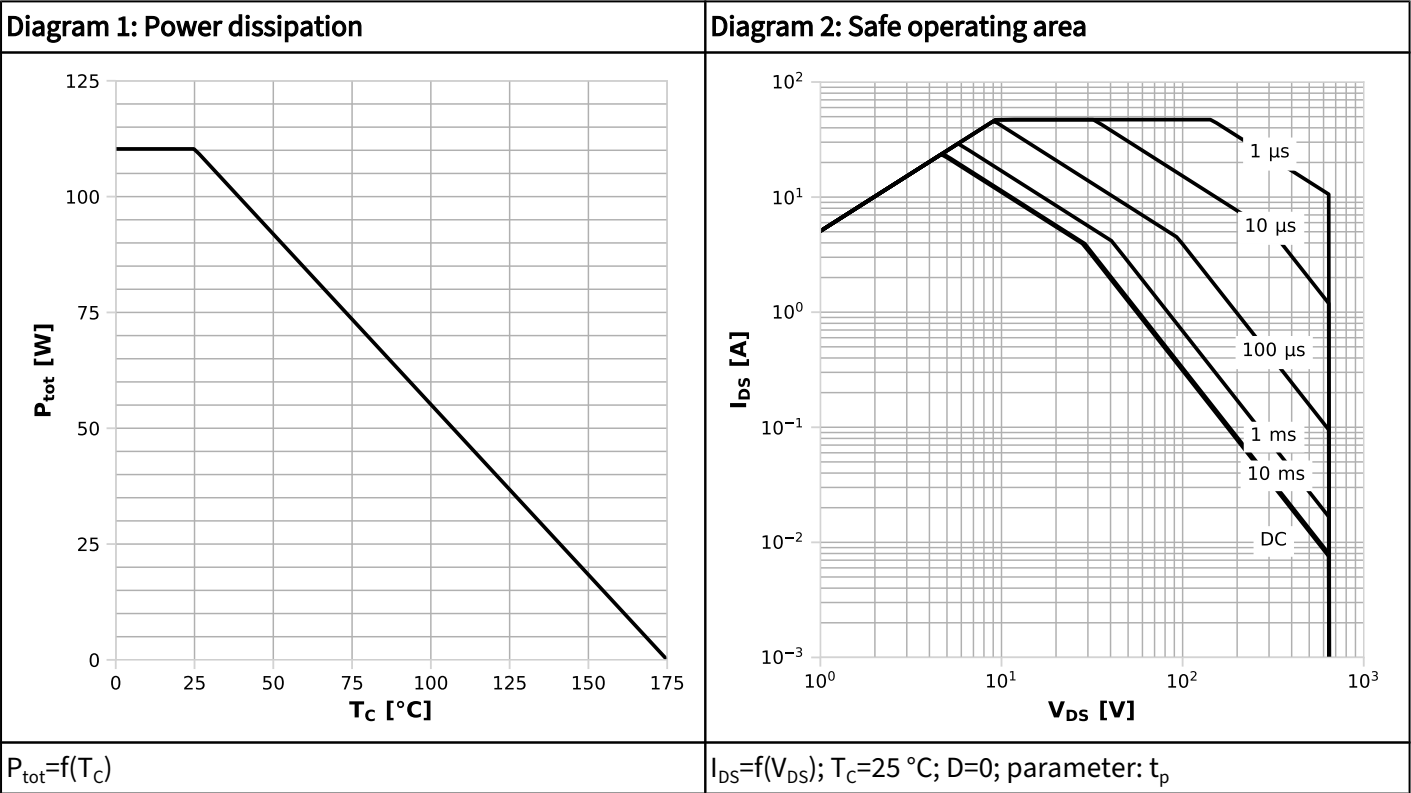
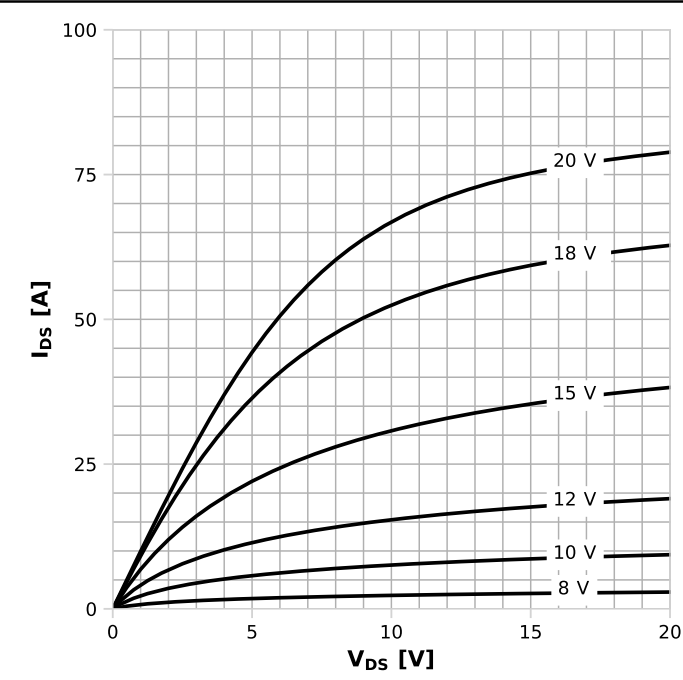


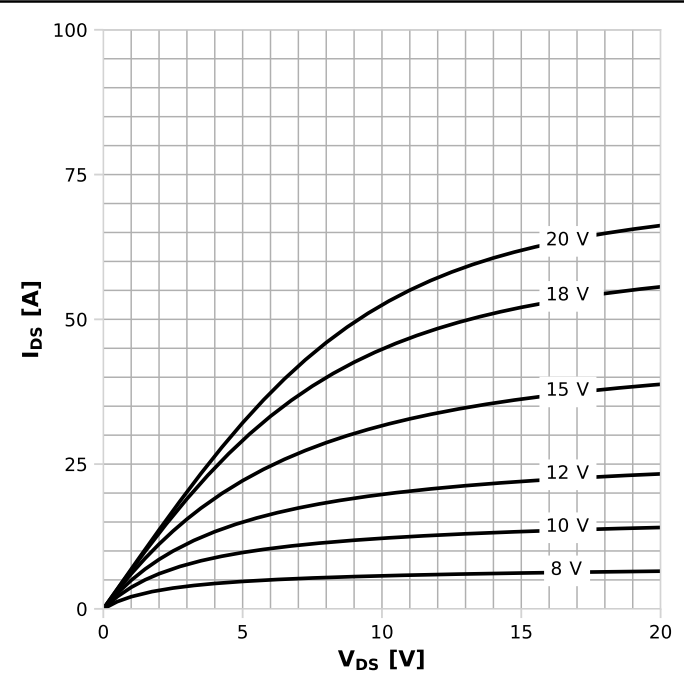


Diagram 5: Typ. output characteristics



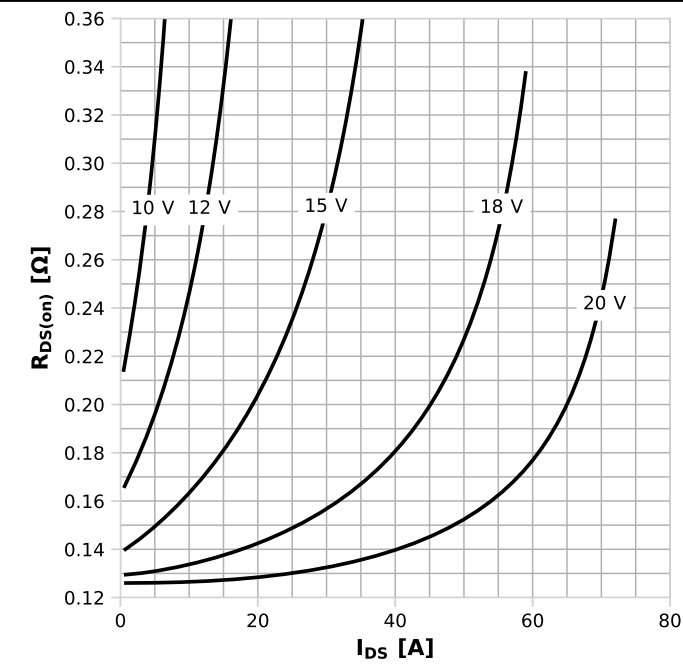
$I_{DS}=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



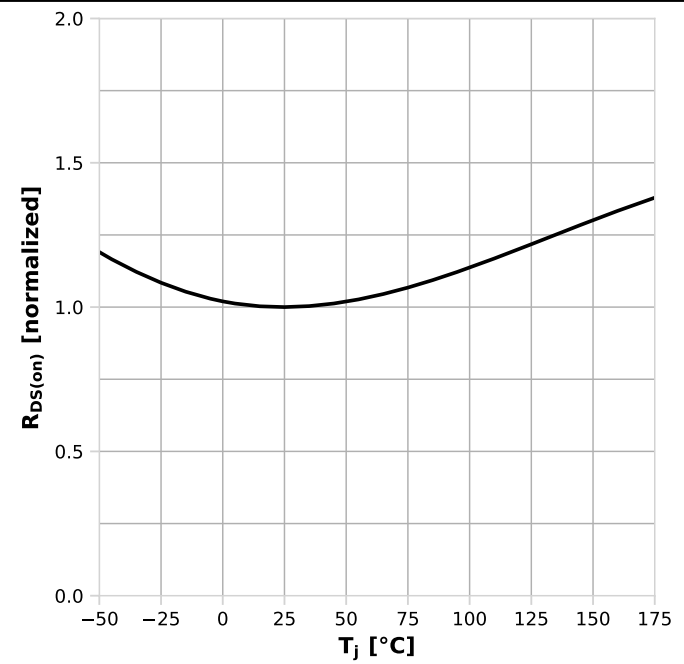
$I_{DS}=f(V_{DS})$ ;  $T_j=175\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



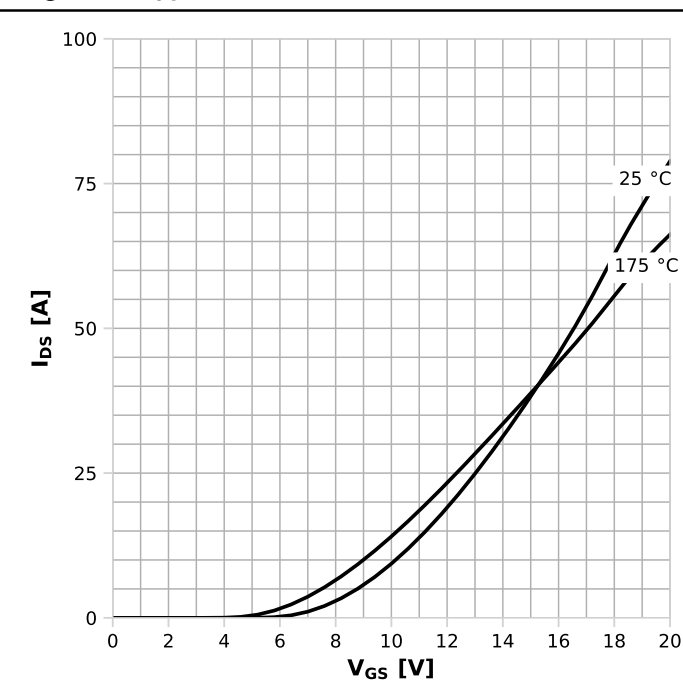
$R_{DS(on)}=f(I_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



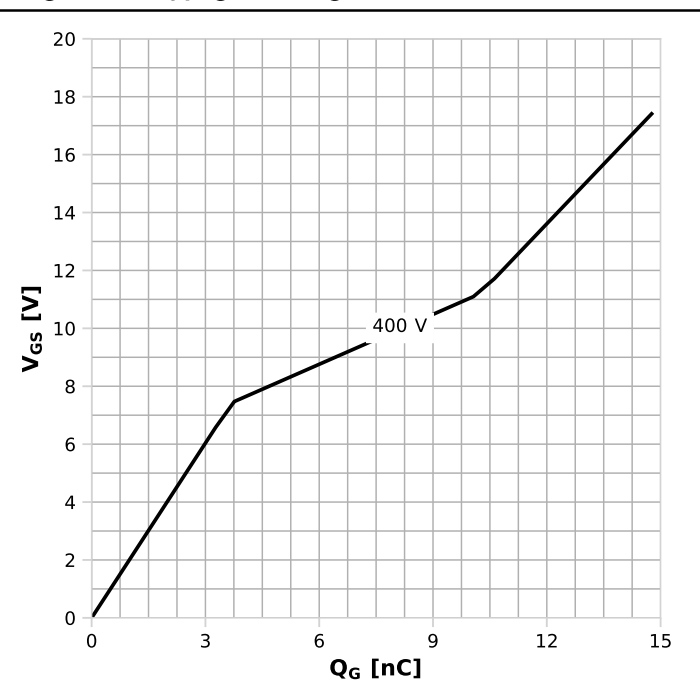
$R_{DS(on)}=f(T_j)$ ;  $I_D=8.9\text{ A}$ ;  $V_{GS}=18\text{ V}$

Diagram 9: Typ. transfer characteristics



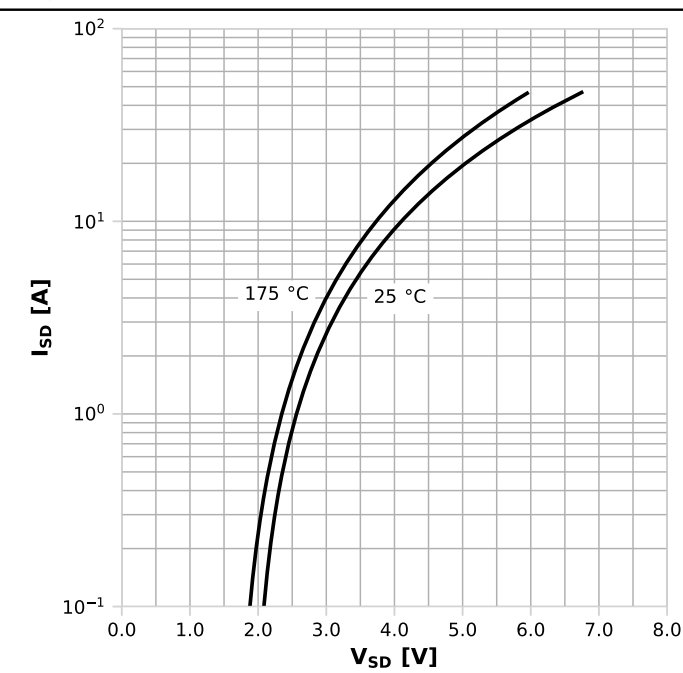
$I_{DS}=f(V_{GS})$ ;  $V_{DS}=20\text{V}$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



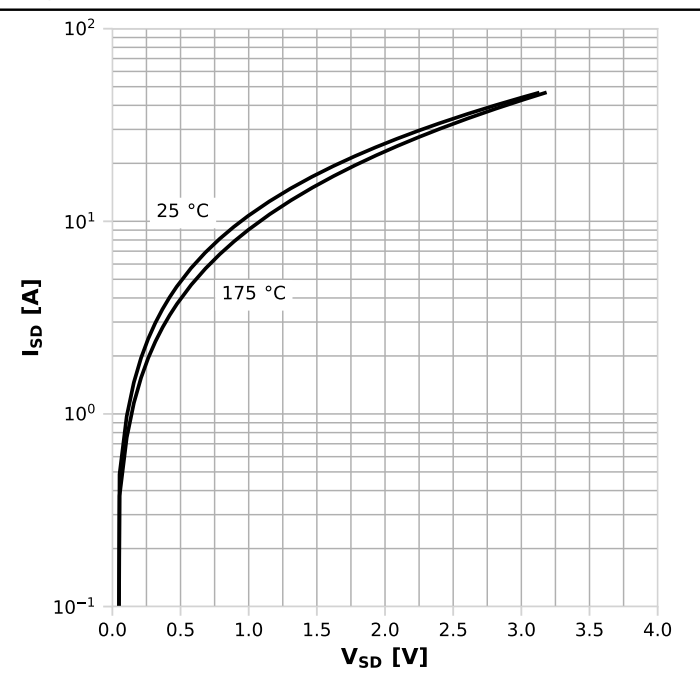
$V_{GS}=f(Q_G)$ ;  $I_D=8.9\text{ A}$  pulsed; parameter:  $V_{DD}$

Diagram 11: Typ. reverse drain current characteristics



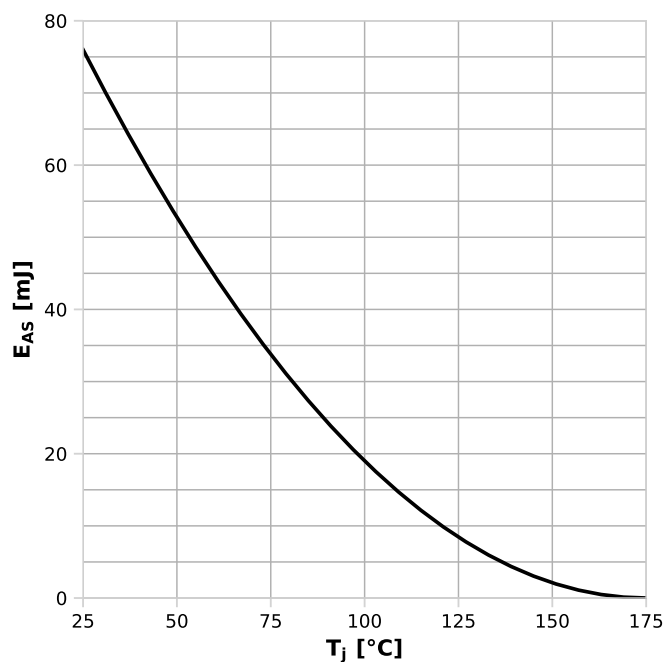
$I_{SD}=f(V_{SD})$ ;  $V_{GS}=0\text{ V}$ ; parameter:  $T_j$

Diagram 12: Typ. reverse drain current characteristics



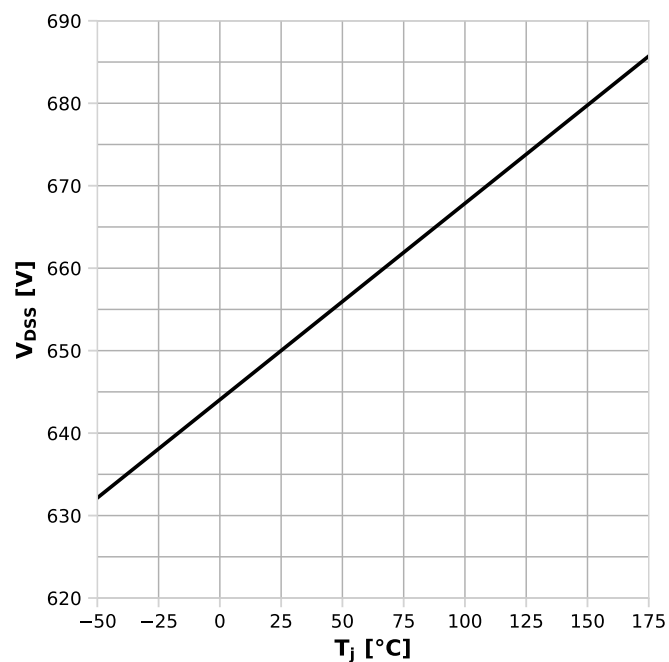
$I_{SD}=f(V_{SD})$ ;  $V_{GS}=18\text{ V}$ ; parameter:  $T_j$

Diagram 13: Avalanche energy



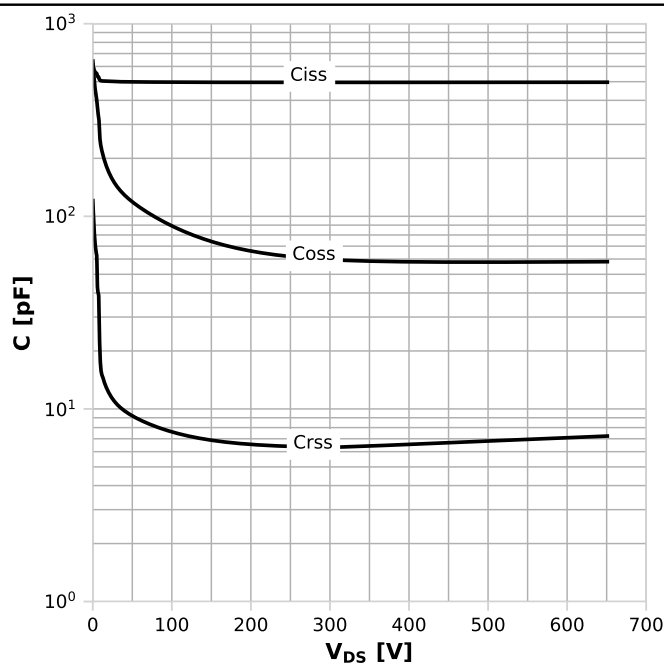
$E_{AS}=f(T_J)$ ;  $I_D=2.8$  A;  $V_{DD}=50$  V

Diagram 14: Drain-source breakdown voltage



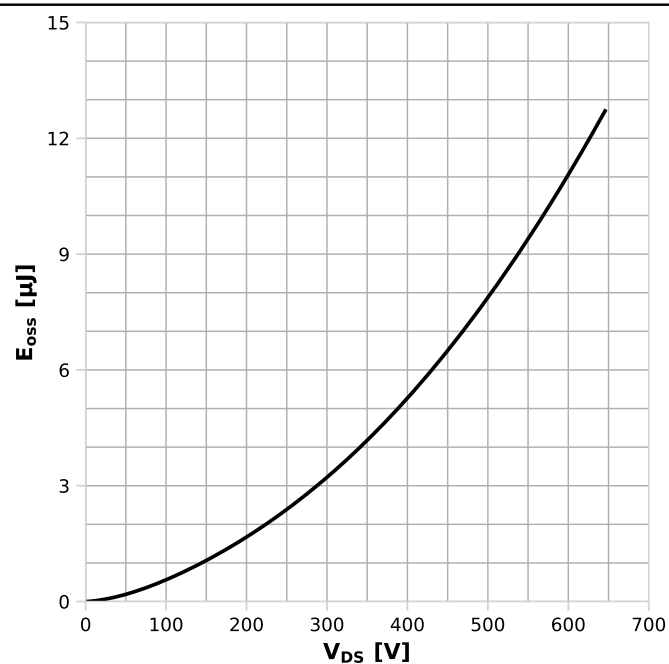
$V_{DSS}=f(T_J)$ ;  $I_D=0.26$  mA

Diagram 15: Typ. capacitances

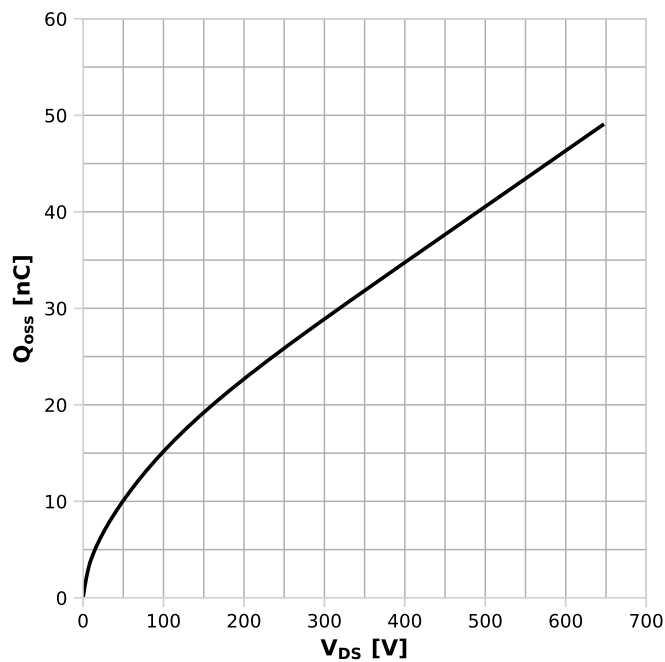


$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=250$  kHz

Diagram 16: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

**Diagram 17: Typ. Qoss output charge**

$$Q_{oss}=f(V_{DS})$$

6 Test Circuits

Table 9 Body diode characteristics (CoolSiC)



Table 10 Switching times (CoolSiC)



Table 11 Unclamped inductive load



7 Package Outlines

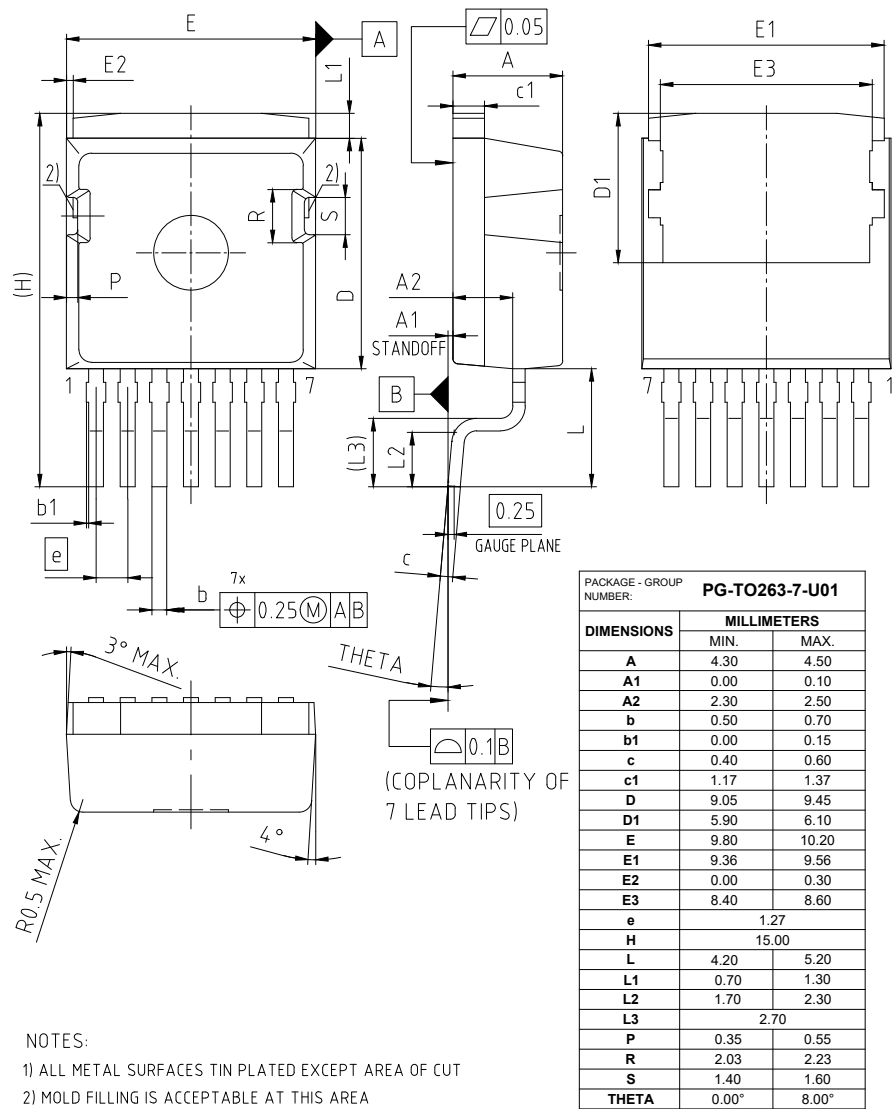


Figure 1 Outline PG-T0263-7, dimensions in mm

## 8 Appendix A

**Table 12**    **Related Links**

- [IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Application Note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Simulation Model](#)
- [IFX Design tools](#)

## Revision History

IMBG65R107M1H

### Revision 2024-08-26, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-12-10	Release of final version
2.1	2024-08-26	IDSS update, nomenclature update, datasheet layout update

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