

MOSFETs Silicon N-channel MOS (U-MOSVIII-H)

TK72E08N1

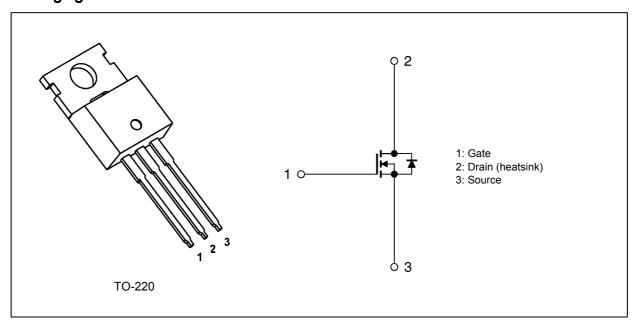
1. Applications

• Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 3.6 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (2) Low leakage current: $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 80 \text{ V)}$
- (3) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_{D} = 1.0 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characterist	Symbol	Rating	Unit		
Drain-source voltage			V_{DSS}	80	V
Gate-source voltage			V _{GSS}	±20	
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I _D	157	Α
Drain current (DC)		(Note 1), (Note 3)	I _D	72	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I _{DP}	344]
Power dissipation	(T _c = 25°C)		P_{D}	192	W
Single-pulse avalanche energy		(Note 4)	E _{AS}	161	mJ
Avalanche current			I _{AR}	72	Α
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150]

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R _{th(ch-c)}	0.65	°C/W
Channel-to-ambient thermal resistance	R _{th(ch-a)}	83.3	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100 A.

Note 3: Device mounted with heatsink so that $R_{th(ch-a)}$ becomes 2.77°C/W.

Note 4: V_{DD} = 64 V, T_{ch} = 25°C (initial), L = 24.0 $\mu H,\ I_{AR}$ = 72 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±0.1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	_	-	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	80	_	_	V
Drain-source breakdown voltage (Note 5)	V _{(BR)DSX}	I _D = 10 mA, V _{GS} = -20 V	60	_	_	
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 1.0 mA	2.0	_	4.0	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 36 A	_	3.6	4.3	mΩ

Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	nbol Test Condition		Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	_	5500	_	pF
Reverse transfer capacitance	C _{rss}		_	38	_	
Output capacitance	C _{oss}		_	1300	_	
Gate resistance	r _g	_	_	3.2	_	Ω
Switching time (rise time)	t _r	See Figure 6.2.1	_	19	_	ns
Switching time (turn-on time)	t _{on}		_	42	_	
Switching time (fall time)	t _f		_	28	_	
Switching time (turn-off time)	t _{off}		_	93	_	

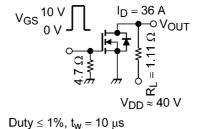


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 64 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 72 \text{ A}$	_	81	_	nC
Gate-source charge 1	Q _{gs1}			29		
Gate-drain charge	Q_{gd}			21		
Gate switch charge	Q_SW		_	33	_	



6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 6)	I _{DR}	_	_	_	72	Α
Reverse drain current (pulsed)	(Note 6)	I _{DRP}	_	_	_	344	
Diode forward voltage		V_{DSF}	I _{DR} = 72 A, V _{GS} = 0 V	_	_	-1.2	V
Reverse recovery time	(Note 7)	t _{rr}	I _{DR} = 72 A, V _{GS} = 0 V	_	77	_	ns
Reverse recovery charge	(Note 7)	Q _{rr}	-dI _{DR} /dt = 100 A/μs	_	150		nC

Note 6: Ensure that the channel temperature does not exceed 150°C.

Note 7: Ensure that V_{DS} peak does not exceed V_{DSS} .

7. Marking

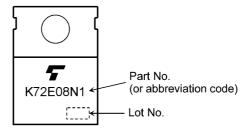


Fig. 7.1 Marking

8. Characteristics Curves (Note)

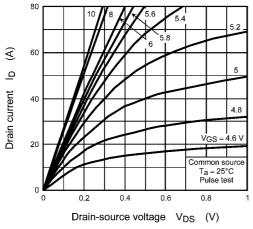
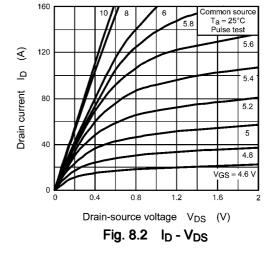


Fig. 8.1 $I_D - V_{DS}$



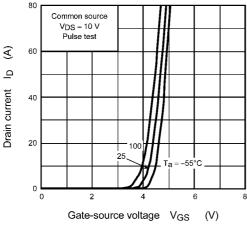


Fig. 8.3 ID - VGS

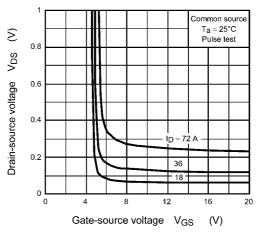


Fig. 8.4 VDS - VGS

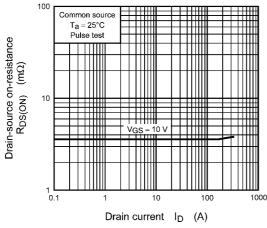


Fig. 8.5 $R_{DS(ON)}$ - I_D

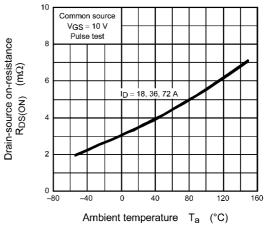


Fig. 8.6 R_{DS(ON)} - T_a

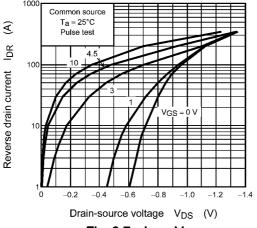


Fig. 8.7 IDR - VDS

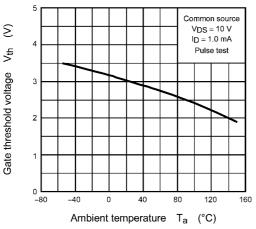


Fig. 8.9 Vth - Ta

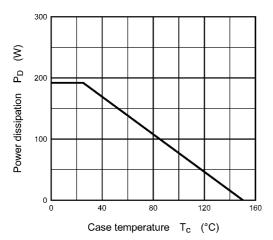


Fig. 8.11 P_D - T_c (Guaranteed Maximum)

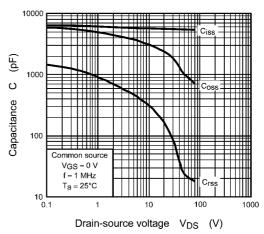


Fig. 8.8 Capacitance - V_{DS}

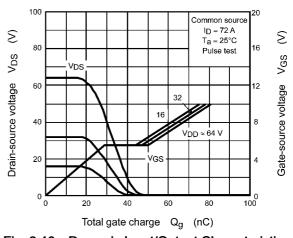


Fig. 8.10 Dynamic Input/Output Characteristics

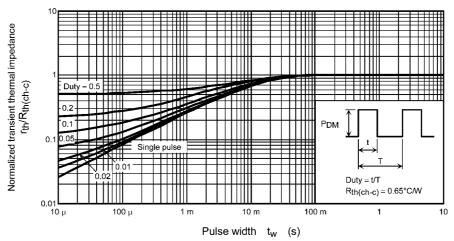


Fig. 8.12 r_{th}/R_{th(ch-c)} - t_w (Guaranteed Maximum)

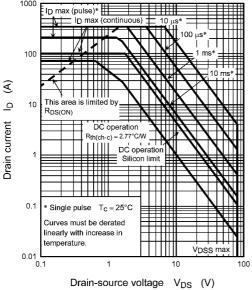


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

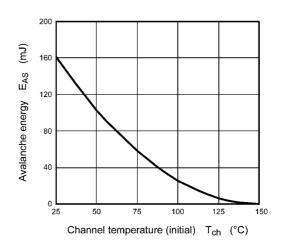


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)

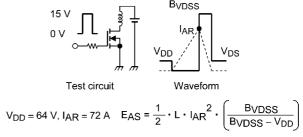


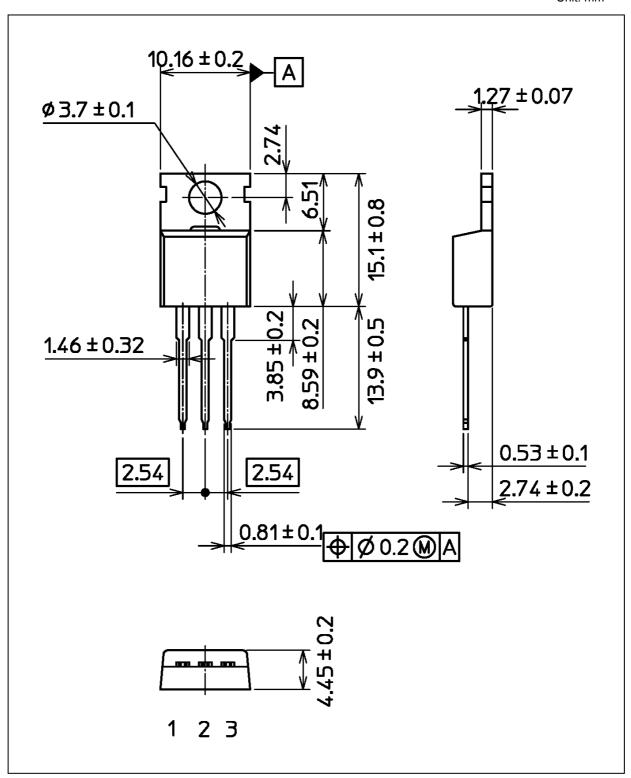
Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 1.93 g (typ.)

Package Name(s)
TOSHIBA: 2-10X1A
Nickname: TO-220



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