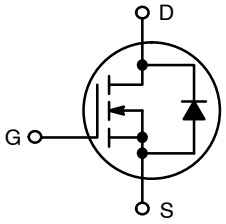
MOSFET – N-Channel, POWERTRENCH®

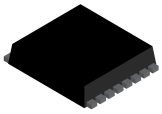
100 V, 240 A, 2.6 mΩ

FDBL86063-F085AW

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	2.6 mΩ @ 10 V	240 A



N-CHANNEL MOSFET



H–PSOF8L
CASE 100BQ

Features

- Typical $R_{DS(on)}$ = 2 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 73 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

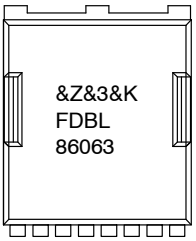
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous, (V_{GS} = 10 V) (Note 1) T_C = 25°C	240	A
	Pulsed Drain Current, T_C = 25°C	(See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	160	mJ
P_D	Power Dissipation	357	W
	Derate Above 25°C	2.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature	–55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.42	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 50 μH, I_{AS} = 80 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86063	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS						
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 25°C	–	–	1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175°C (Note 4)	–	–	1.5	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	2.9	4.0	V
$R_{DS(on)}$	Drain−to−Source On−Resistance	I_D = 80 A, V_{GS} = 10 V, T_J = 25°C	–	2.0	2.6	mΩ
		I_D = 80 A, V_{GS} = 10 V, T_J = 175°C (Note 4)	–	4.2	5.6	
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	5120	–	pF
C_{oss}	Output Capacitance		–	3220	–	pF
C_{rss}	Reverse Transfer Capacitance		–	32	–	pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz	–	0.4	–	Ω
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 80 A	–	73	95	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V; V_{DD} = 50 V, I_D = 80 A	–	9	–	nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 50 V, I_D = 80 A	–	22	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge	V_{DD} = 50 V, I_D = 80 A	–	17	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10V, R_{GEN} = 6 Ω	–	–	53	ns
$t_{d(on)}$	Turn−On Delay		–	25	–	ns
t_r	Rise Time		–	16	–	ns
$t_{d(off)}$	Turn−Off Delay		–	32	–	ns
t_f	Fall Time		–	8	–	ns
t_{off}	Turn−Off Time		–	–	51	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V I_{SD} = 40 A, V_{GS} = 0 V	–	0.9 0.8	1.25 1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 80 A, $\Delta I_{SD}/\Delta t$ = 100 A/μs	–	107	139	ns
Q_{rr}	Reverse−Recovery Charge		–	175	260	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
FDBL86063−F085AW	FDBL86063	H−PSOF8L (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

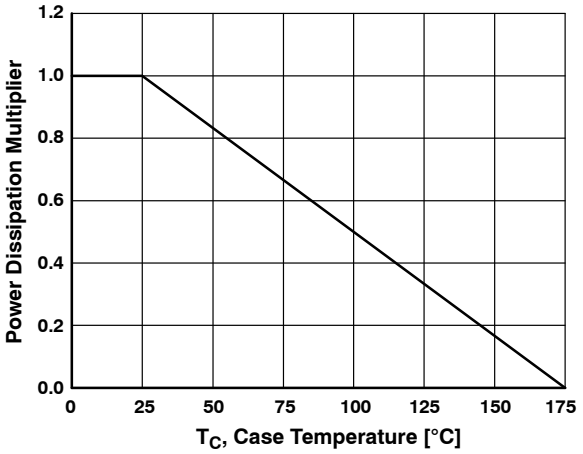


Figure 1. Normalized Power Dissipation vs. Case Temperature

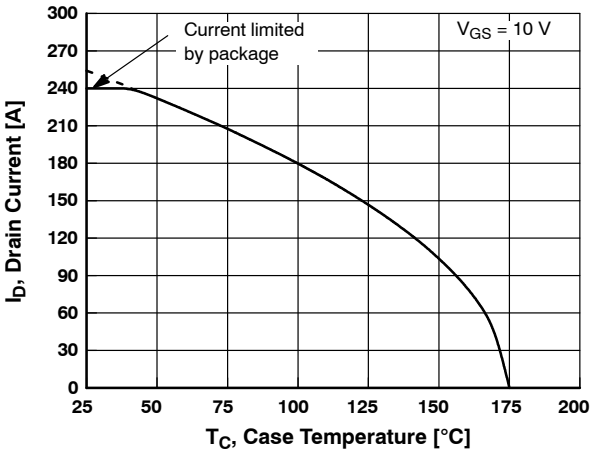


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

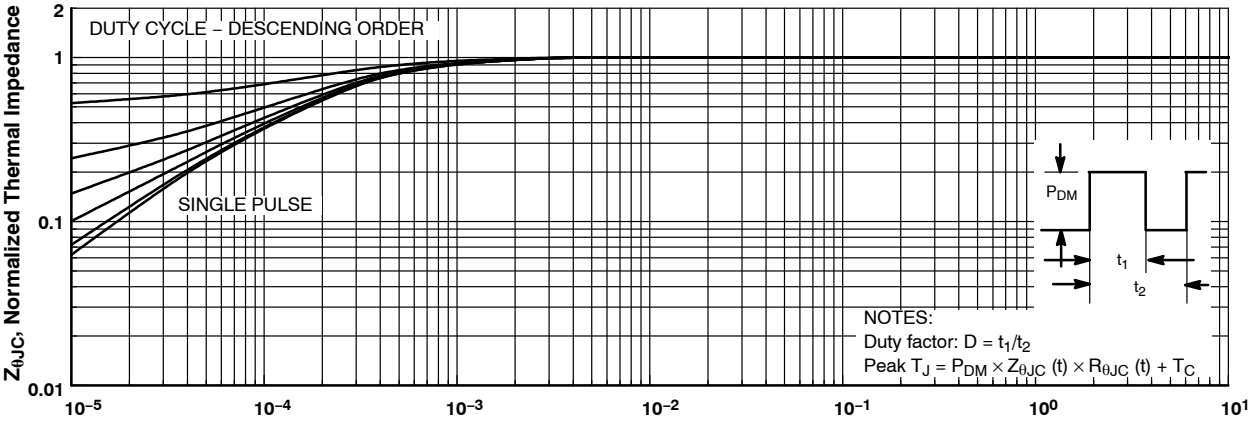


Figure 3. Normalized Maximum Transient Thermal Impedance

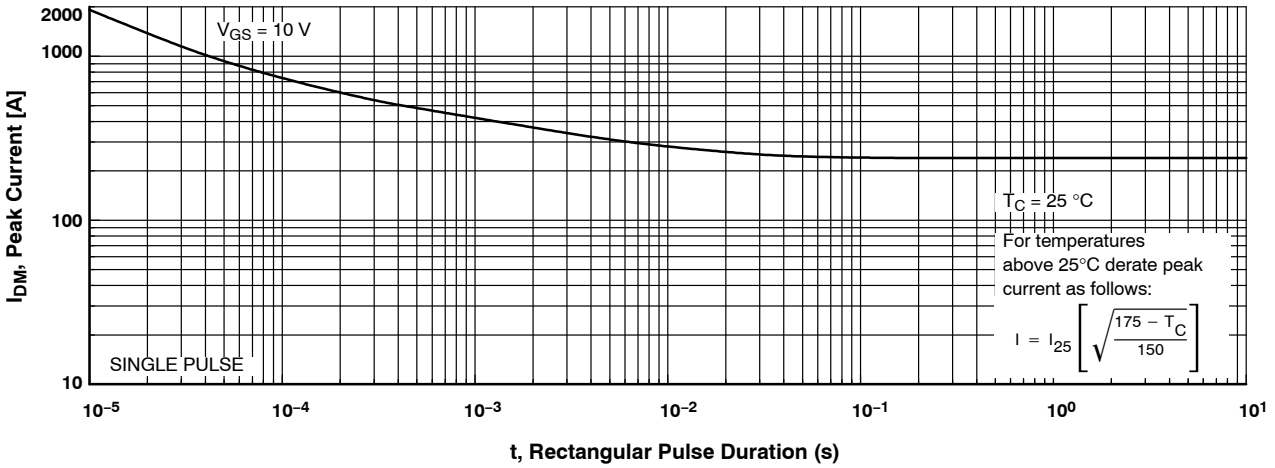


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

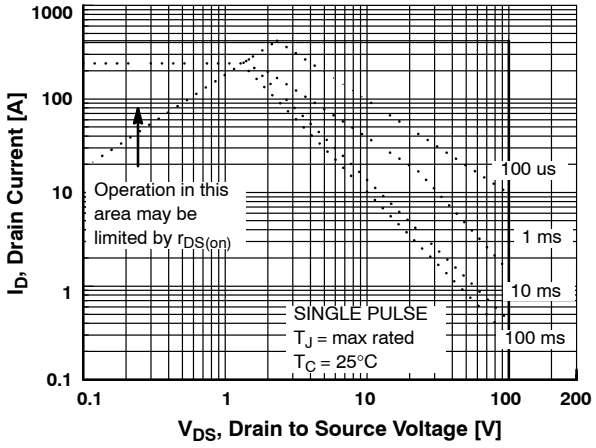
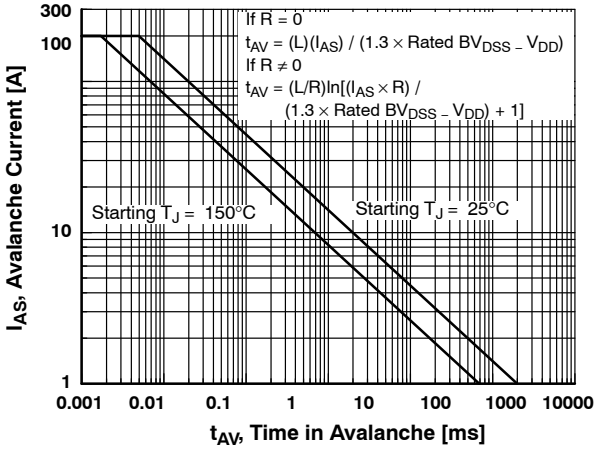


Figure 5. Forward Bias Safe Operating Area



Refer to **onsemi** Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

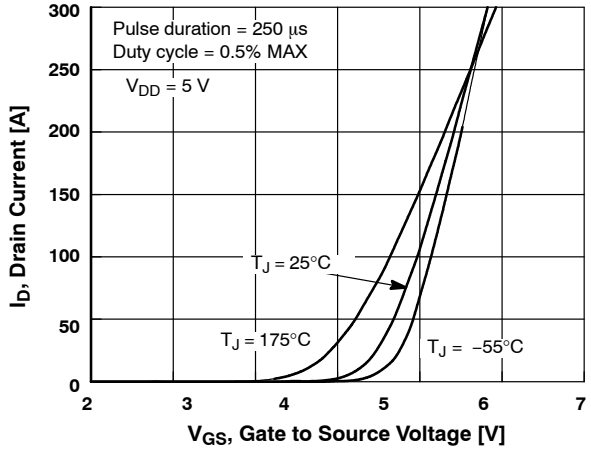


Figure 7. Transfer Characteristics

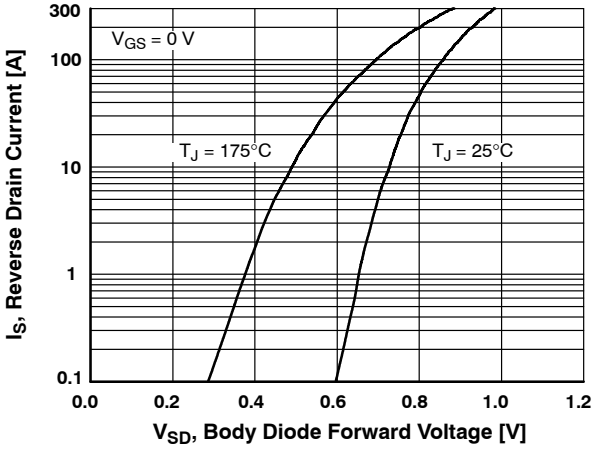


Figure 8. Forward Diode Characteristics

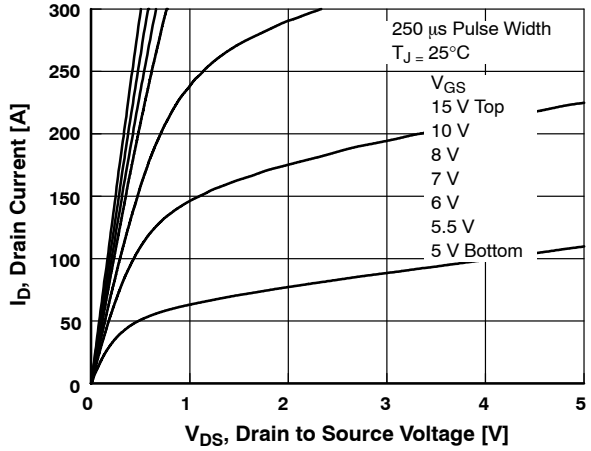


Figure 9. Saturation Characteristics

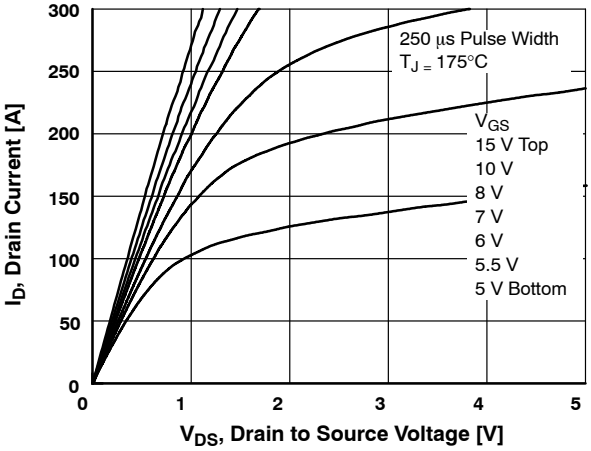


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

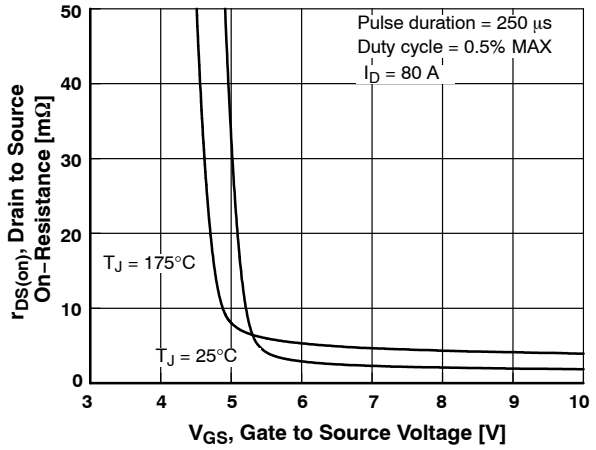


Figure 11. R_{DSON} vs. Gate Voltage

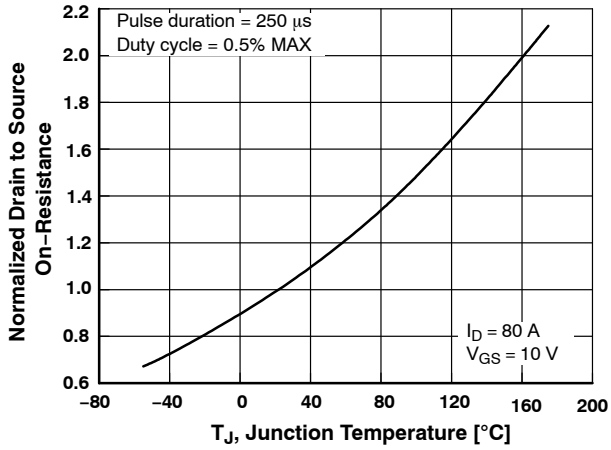


Figure 12. Normalized R_{DSON} vs. Junction Temperature

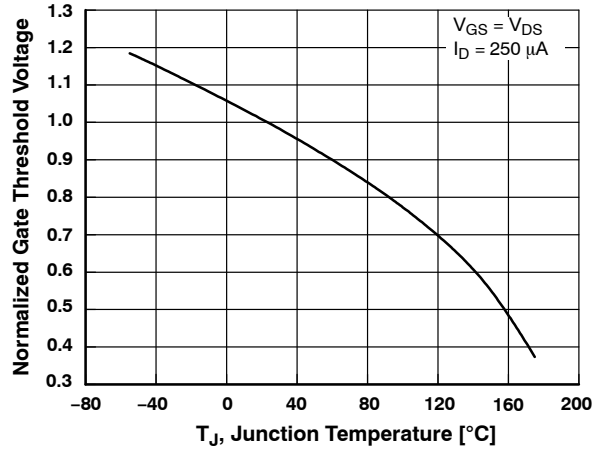


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

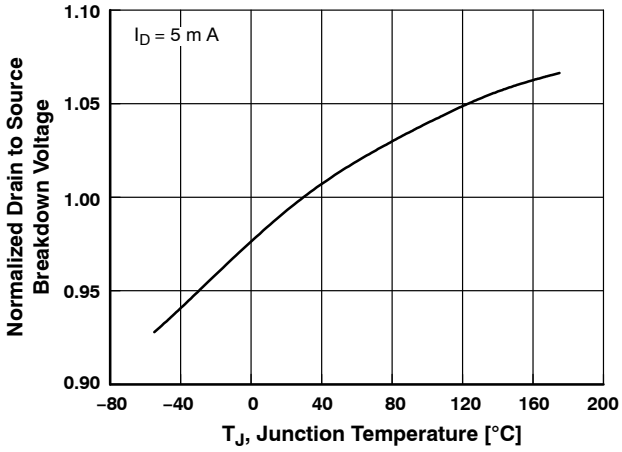


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

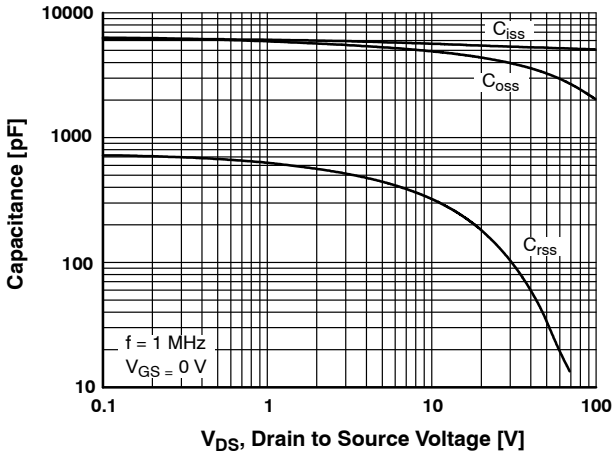


Figure 15. Capacitance vs. Drain to Source Voltage

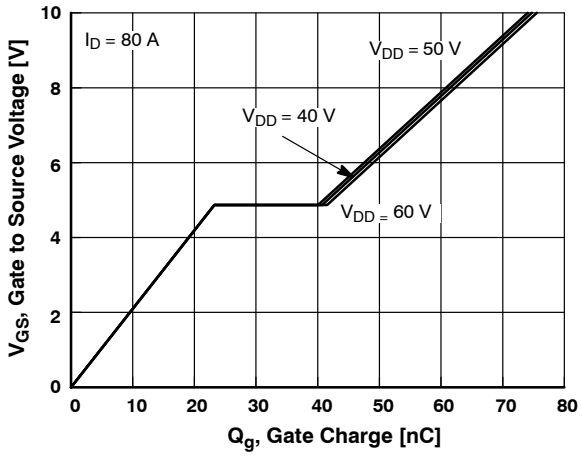
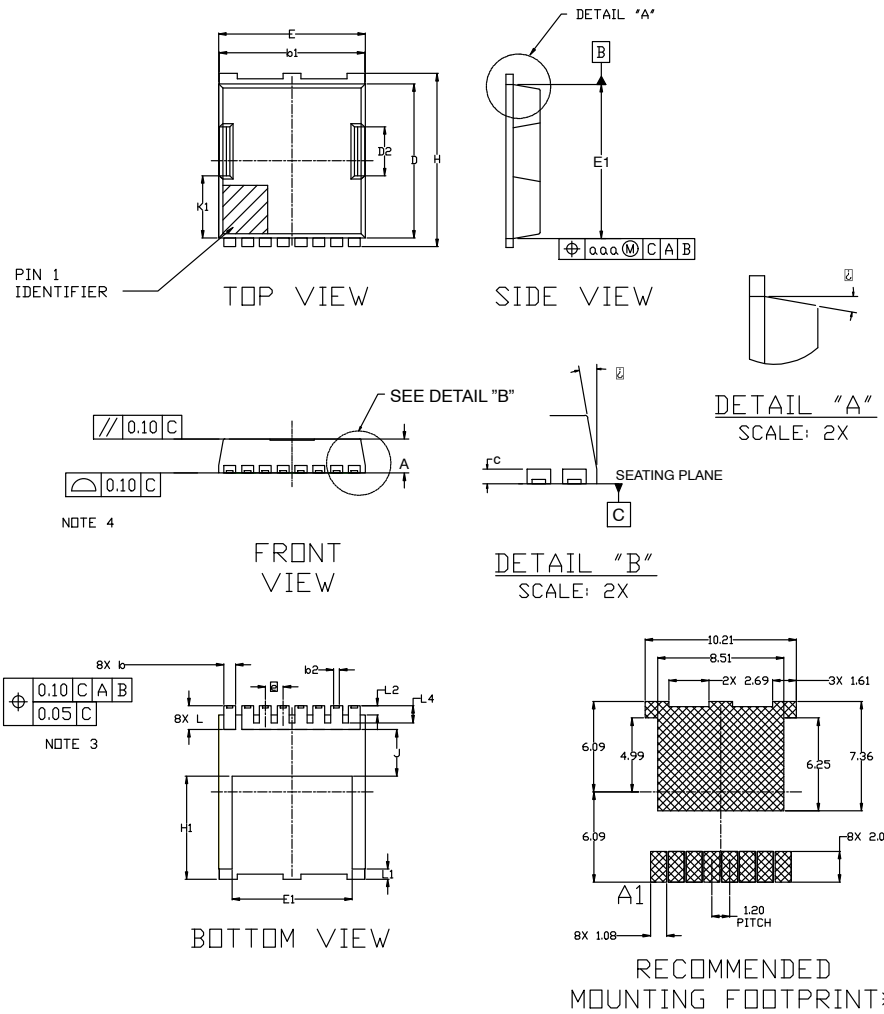


Figure 16. Gate Charge vs. Gate to Source Voltage

PACKAGE DIMENSIONS

H−PSOF8L 9.90x10.38x2.30
CASE 100BQ
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	2.20	---	2.40
b	0.70	---	0.90
b1	9.70	---	9.90
b2	0.42	---	0.50
c	0.40	---	0.60
D	10.28	---	10.58
D2	3.10	3.30	3.50
E	9.70	9.90	10.10
E1	7.90	8.10	8.30
e	1.20 BSC		
H	11.48	11.68	11.880
H1	6.75	6.95	7.15
N	8		
J	3.00	3.15	3.30
K1	3.98	4.18	4.38
L	1.40	1.60	1.80
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L4	1.00	1.15	1.30
$\hat{\theta}$	4°	7°	10°

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales