

# MOSFET

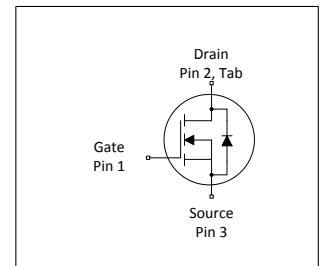
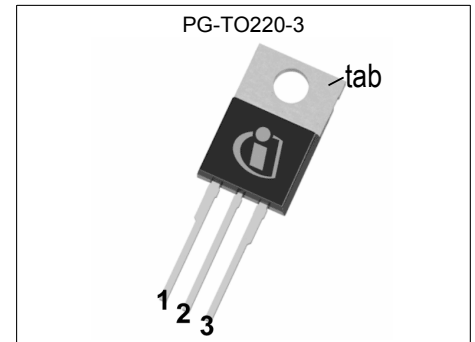
## StrongIRFET™ 2 Power-Transistor

### Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard



RoHS

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	80	V
$R_{DS(on),max}$	4.0	$m\Omega$
$I_D$	115	A
$Q_{oss}$	65	nC
$Q_G$	54	nC

Type / Ordering Code	Package	Marking	Related Links
IPP040N08NF2S	PG-TO220-3	040N08NS	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	115 88 83 22	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^{(2)}$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	460	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	119	mJ	$I_D=95\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	150 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^{(2)}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3	3.8	V	$V_{DS}=V_{GS}$ , $I_D=85\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance <sup>1)</sup>	$R_{DS(on)}$	-	3.6 4.5	4.0 5.6	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=40\text{ A}$
Gate resistance	$R_G$	-	1.9	-	$\Omega$	-
Transconductance <sup>2)</sup>	$g_{fs}$	63	-	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=80\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	3800	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	620	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	29	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	54	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	28	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	13	-	ns	$V_{DD}=40\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=80\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>3)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	19	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	12	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	19	-	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>2)</sup>	$Q_g$	-	54	81	nC	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.9	-	V	$V_{DD}=40\text{ V}$ , $I_D=80\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	65	-	nC	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup>  $R_{DS(on)}$  is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 m $\Omega$ /mm per leg.

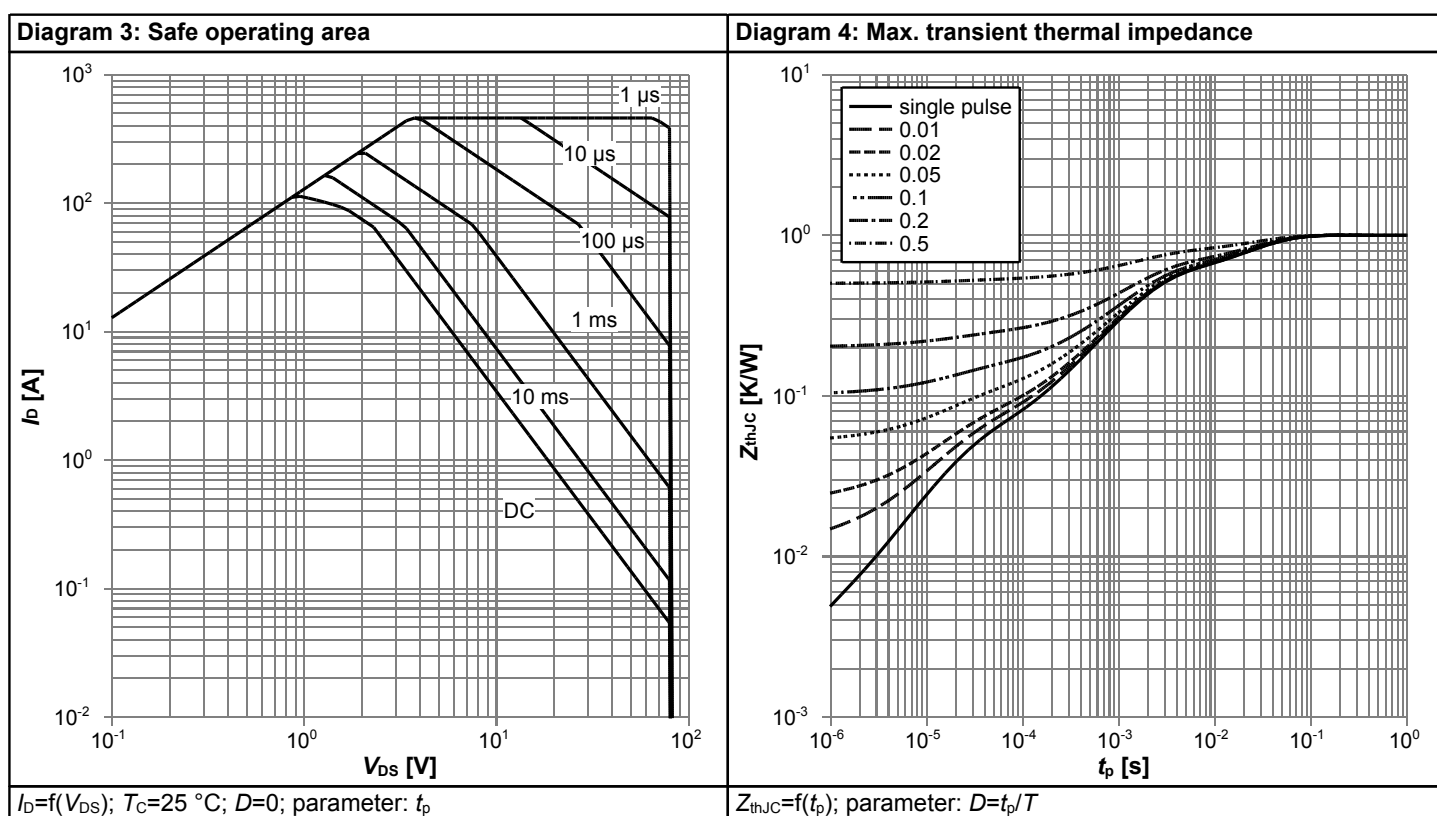
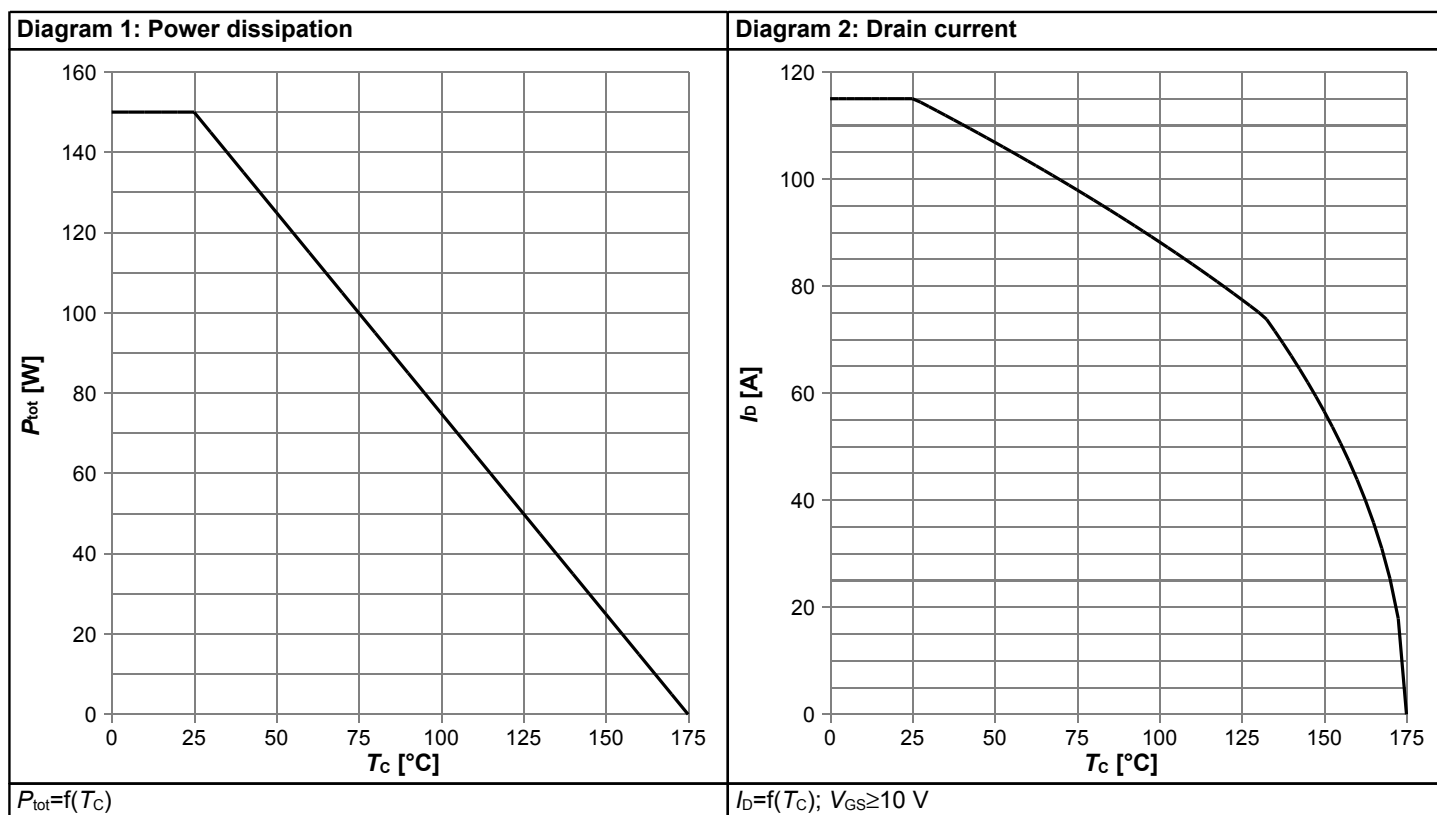
<sup>2)</sup> Defined by design. Not subject to production test.

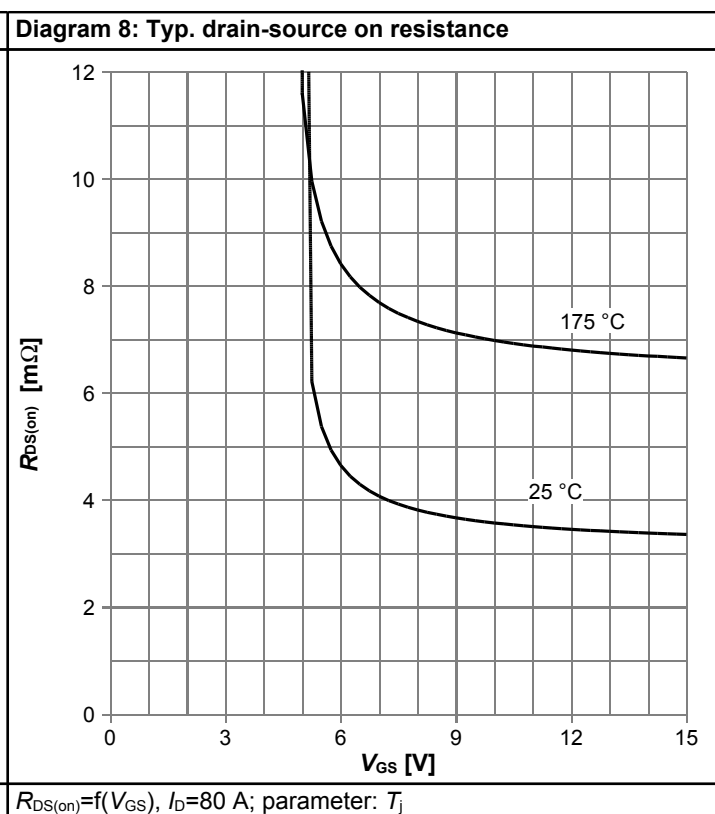
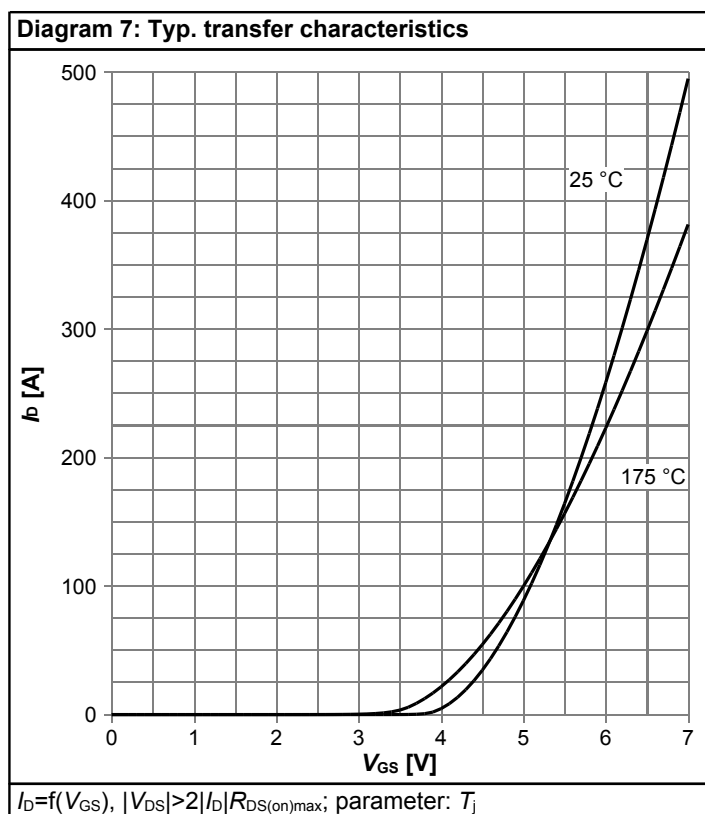
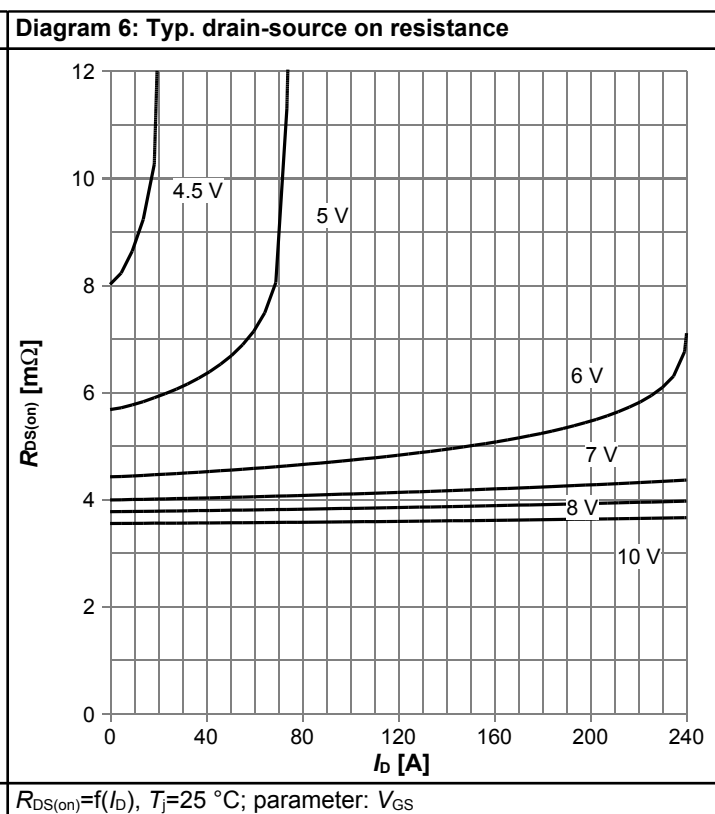
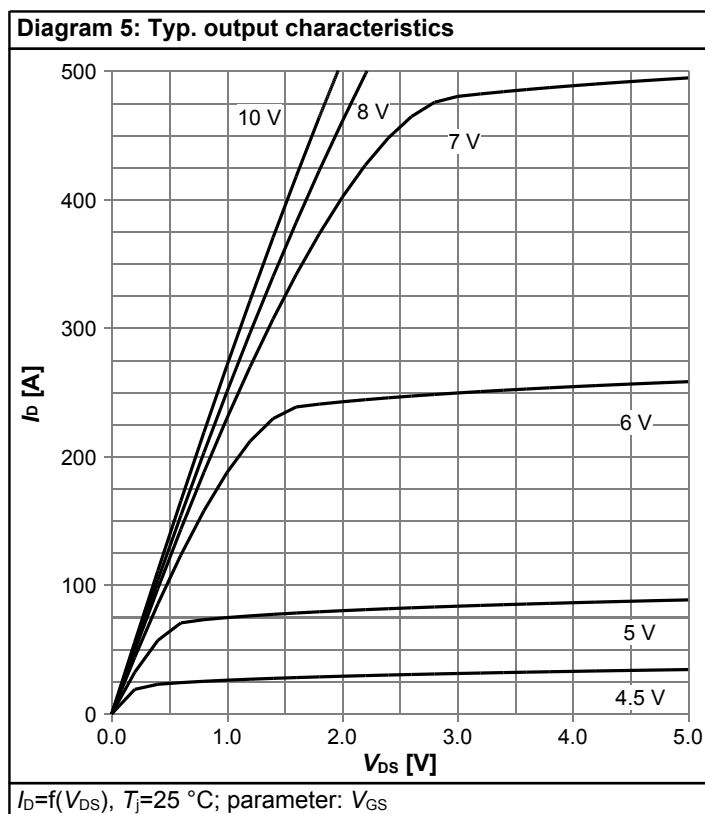
<sup>3)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

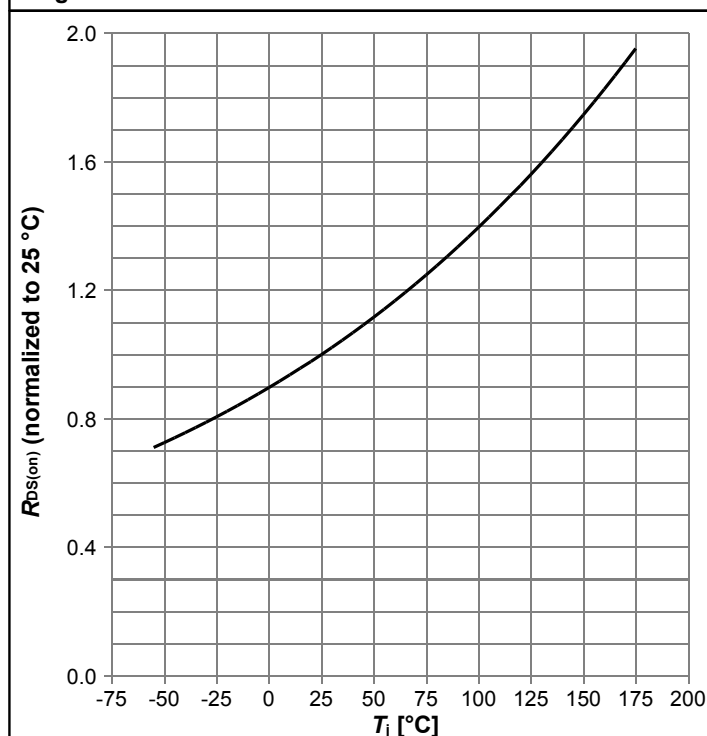
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	94	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	460	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.95	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=80\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	33	-	ns	$V_R=40\text{ V}$ , $I_F=80\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	189	-	nC	$V_R=40\text{ V}$ , $I_F=80\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$

## 4 Electrical characteristics diagrams



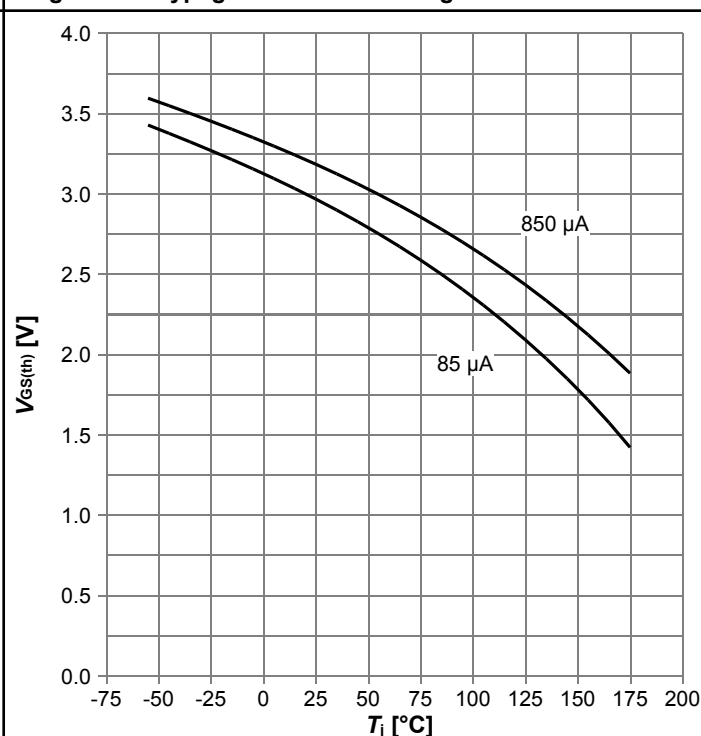


**Diagram 9: Normalized drain-source on resistance**



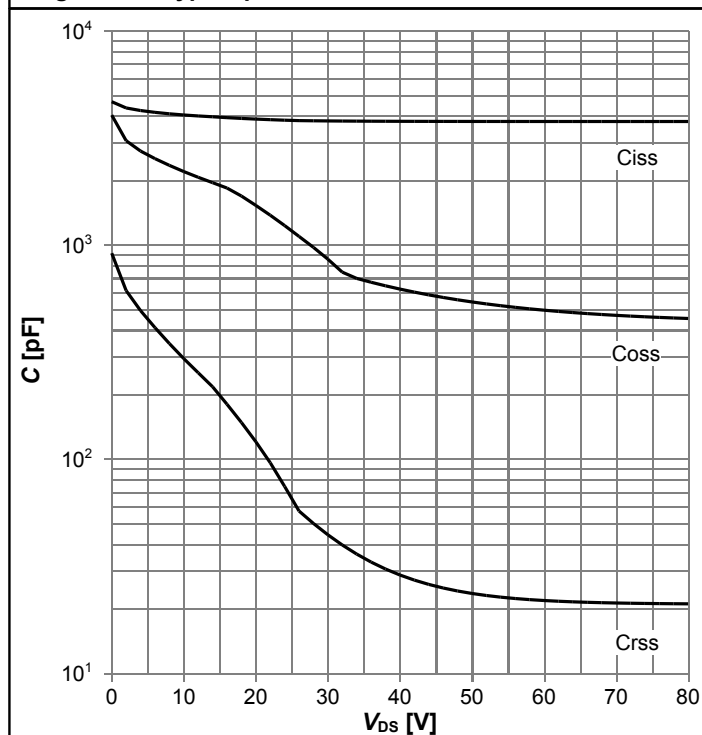
$R_{DS(on)}=f(T_j)$ ,  $I_D=80$  A,  $V_{GS}=10$  V

**Diagram 10: Typ. gate threshold voltage**



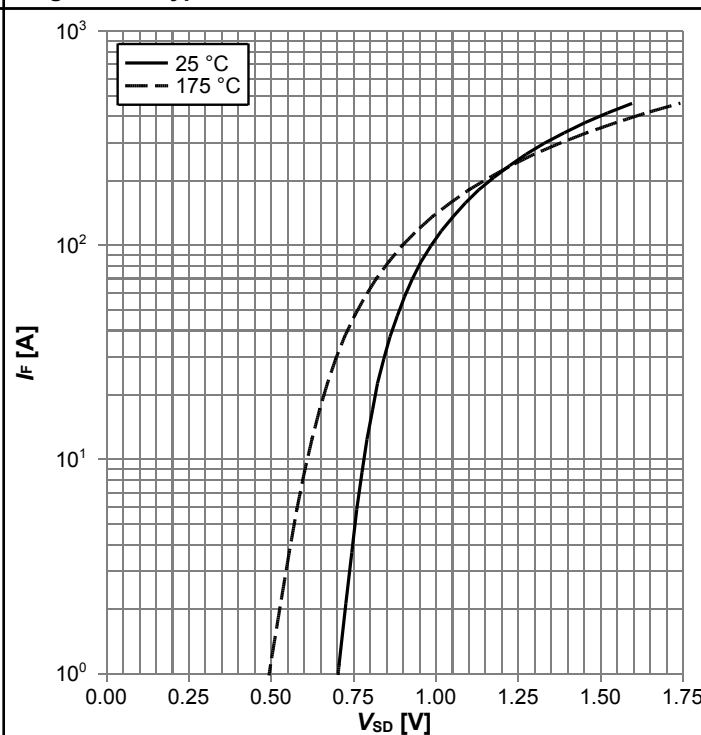
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

**Diagram 11: Typ. capacitances**



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

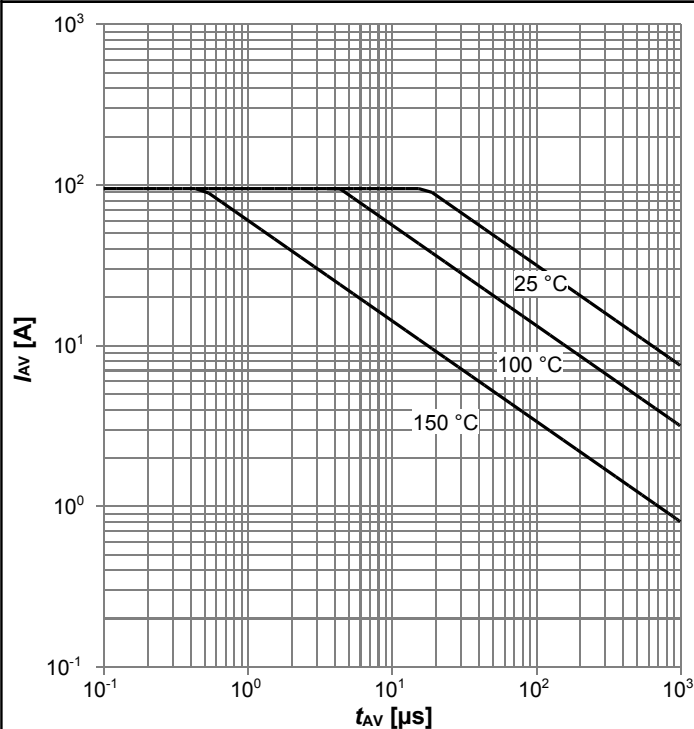
**Diagram 12: Typ. forward characteristics of reverse diode**



$I_F=f(V_{SD})$ ; parameter:  $T_j$

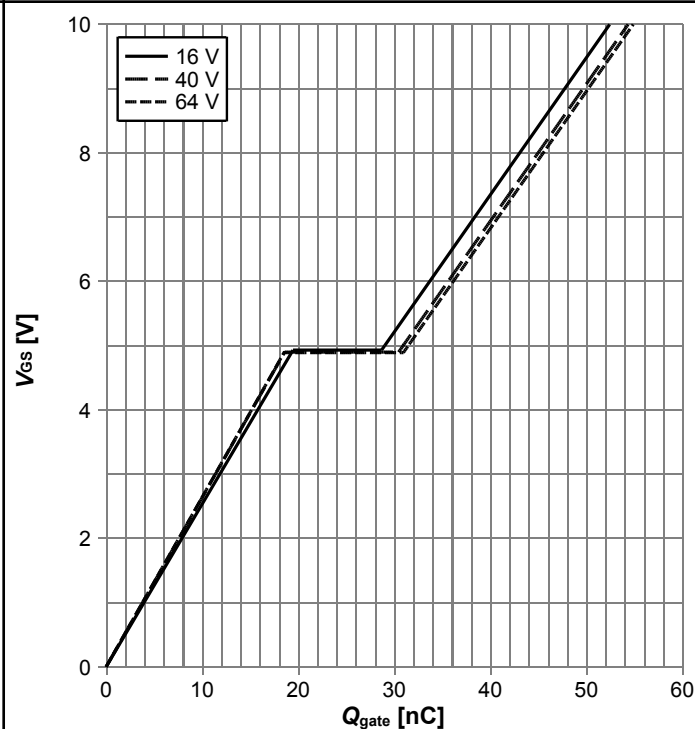


**Diagram 13: Avalanche characteristics**



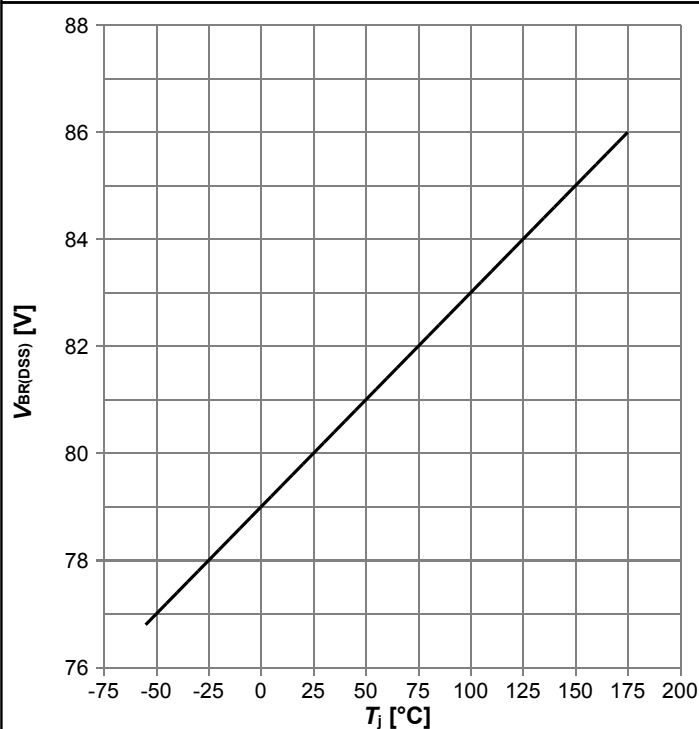
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



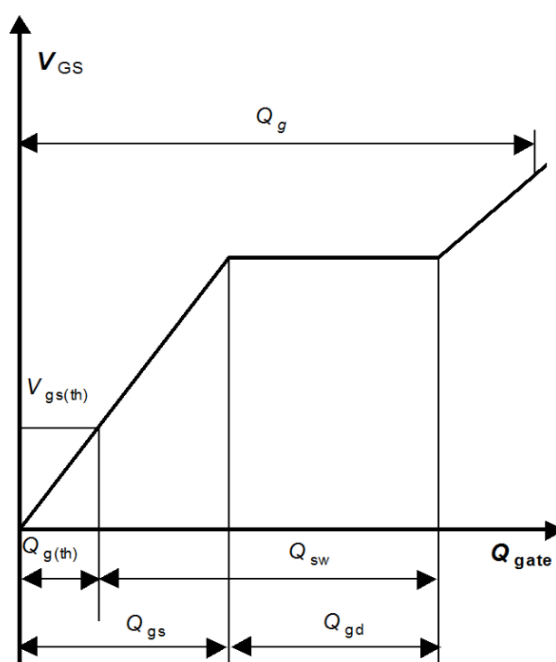
$V_{GS}=f(Q_{gate})$ ,  $I_D=80\text{ A}$  pulsed,  $T_j=25\text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

**Diagram Gate charge waveforms**



## 5 Package Outlines

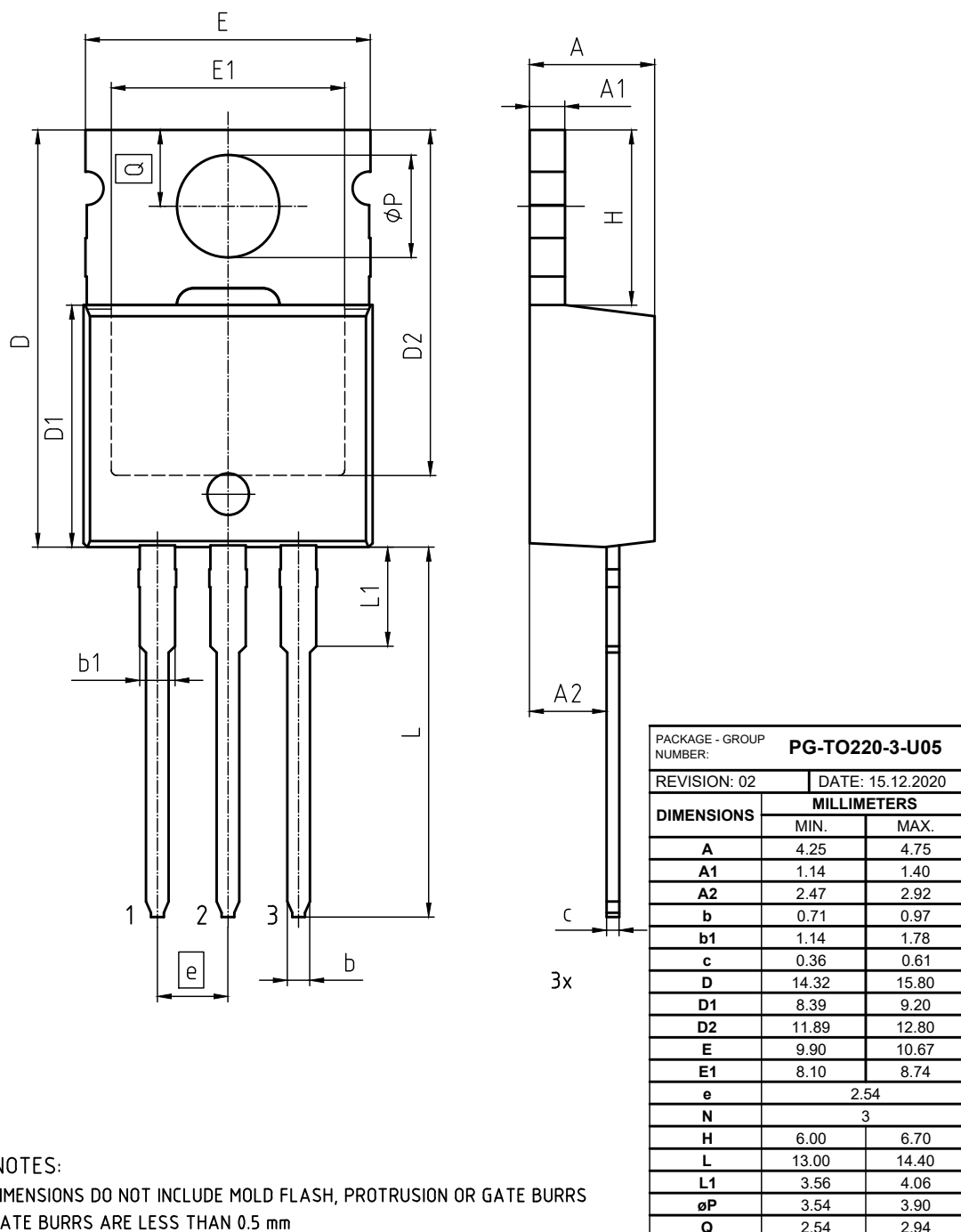


Figure 1 Outline PG-TO220-3, dimensions in mm

## Revision History

IPP040N08NF2S

**Revision: 2022-06-15, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-12-18	Release of final version
2.1	2022-06-15	Skip condition "Operating and storage tempt.", update trr and Qrr, footnotes and Diagram 12

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