



General Description

The SQD40N10-25-T4_GE3 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness.

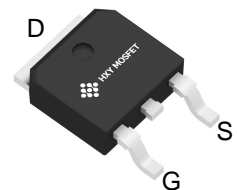
General Features

$V_{DS} = 100V$ $I_D = 40A$

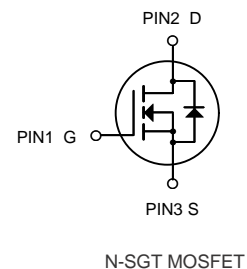
$R_{DS(ON)} < 23m\Omega$ @ $V_{GS} = 10V$

Applications

Consumer electronic power supply
Motor control
Synchronous-rectification
Isolated DC
Synchronous-rectification applications



TO-252-2L



Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SQD40N10-25-T4_GE3	TO-252-2L	HXY MOSFET	2500

Absolute Maximum Ratings at $T_j = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Unit
VDS	Drain source voltage	100	V
VGS	Gate source voltage	± 20	V
ID	Continuous drain current ¹⁾ , $T_C = 25^\circ C$	40	A
ID, pulse	Pulsed drain current ²⁾ , $T_C = 25^\circ C$	100	A
P _D	Power dissipation ³⁾ , $T_C = 25^\circ C$	27	W
EAS	Single pulsed avalanche energy ⁵⁾	16	mJ
Tstg, T _j	Operation and storage temperature	-55 to 150	$^\circ C$
R θ JC	Thermal resistance, junction-case	4.65	$^\circ C/W$
R θ JA	Thermal resistance, junction-ambient ⁴⁾	62	$^\circ C/W$



Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	100	-	-	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} = 80V, V _{GS} = 0V	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.6	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 15A	-	20	23	mΩ
		V _{GS} = 4.5V, I _D = 10A	-	-	33	mΩ
g _{fs}	Forward Threshold Voltage	V _{DS} = 10V, I _D = 20A	-	22	-	S
R _g	Gate Resistance	V _{DS} = V _{GS} =0V, f = 1.0MHz	-	1.62	-	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 50V, V _{GS} = 0V, f = 1.0MHz	-	822	-	pF
C _{oss}	Output Capacitance		-	310	-	pF
C _{rss}	Reverse Transfer Capacitance		-	23.5	-	pF
Switching Characteristics						
Q _g	Total Gate Charge	V _{DS} = 50V, I _D = 20A, V _{GS} = 10V	-	22.7	-	nC
Q _{gs}	Gate-Source Charge		-	6.2	-	
Q _{gd}	Gate-Drain(“Miller”) Charge		-	5.3	-	
t _{d(on)}	Turn-On Delay Time	V _{DS} = 50V, I _D = 20A, R _G = 3Ω, V _{GS} =10V	-	15	-	ns
t _r	Turn-On Rise Time		-	3.2	-	
t _{d(off)}	Turn-Off Delay Time		-	30	-	
t _f	Turn-Off Fall Time		-	7.6	-	
Diode Characteristics						
I _S	Continuous Source Current		-	-	40	A
V _{SD}	Diode Forward Voltage	I _S =20A . V _{GS} = 0V	-	0.88	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} =20A,	-	45	-	ns
Q _{rr}	Reverse Recovery Charge	dI _{SD} /dt=100A/μs	-	59	-	nC

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with $T_A = 25^\circ\text{C}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
2. The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is $V_{DS} = 50V, V_{GS} = 10V, L = 0.5mH$



Electrical Characteristics Diagrams

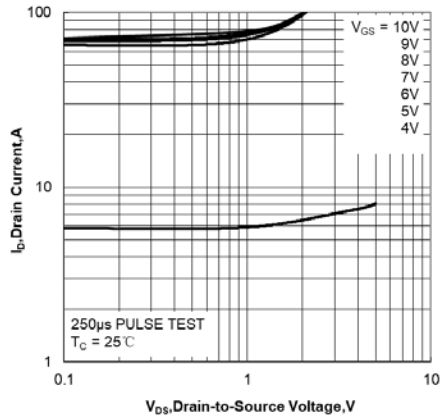


Figure 1. Output Characteristics

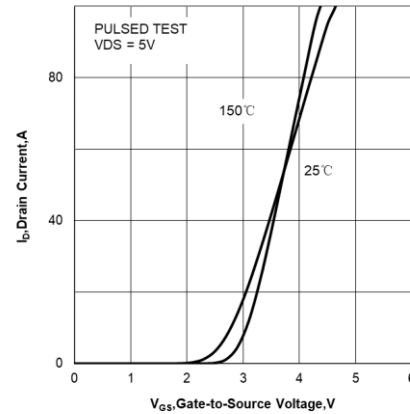


Figure 2. Transfer Characteristics

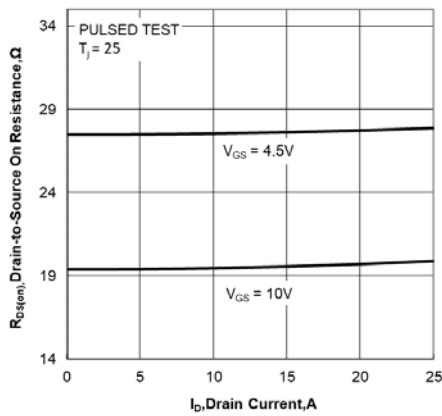


Figure 3. Drain-to-Source On Resistance
vs Drain Current

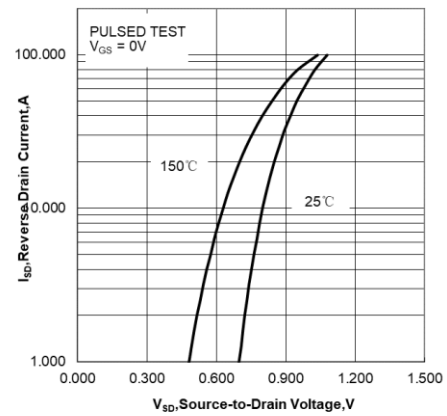


Figure 4. Body Diode Forward Voltage
vs Source Current and Temperature

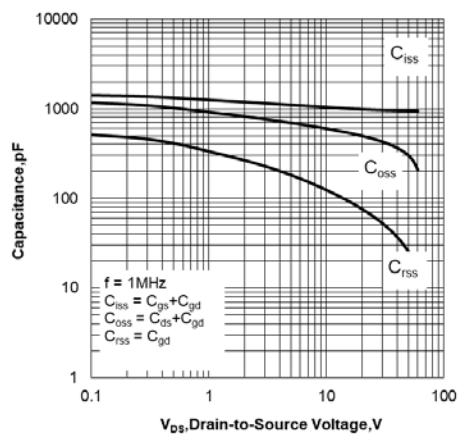


Figure 5. Capacitance Characteristics

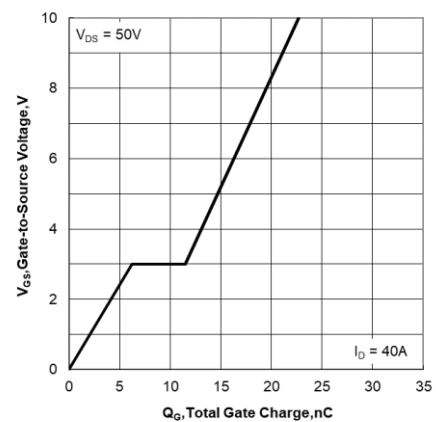


Figure 6. Gate Charge Characteristics

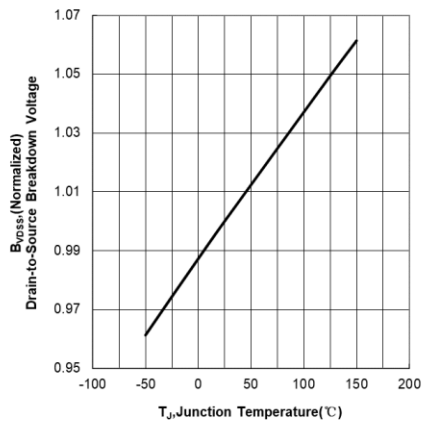


Figure 7. Normalized Breakdown Voltage
vs Junction Temperature

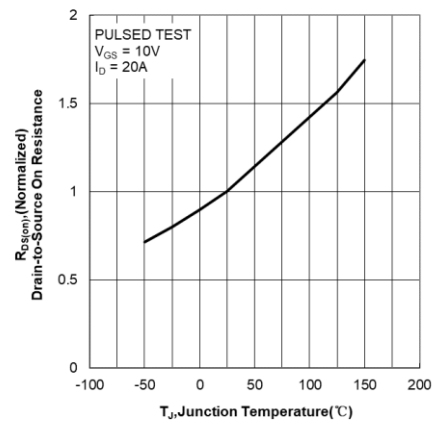


Figure 8. Normalized On Resistance vs
Junction Temperature

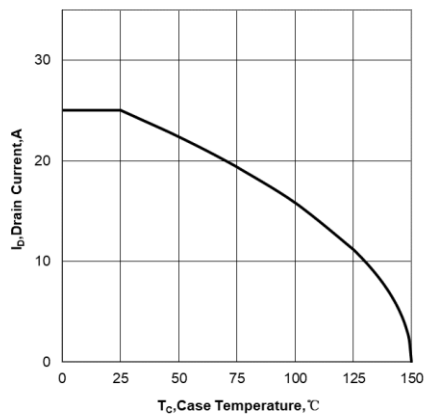


Figure 9. Maximum Continuous Drain Current
vs Case Temperature

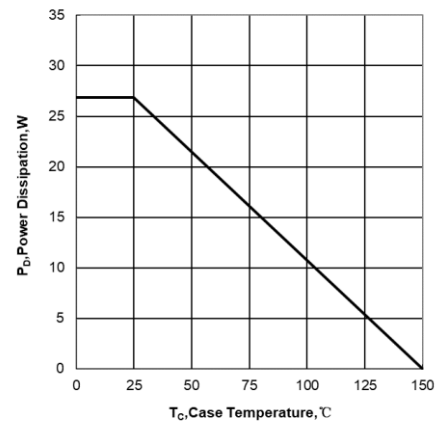


Figure 10. Maximum Power Dissipation
vs Case Temperature

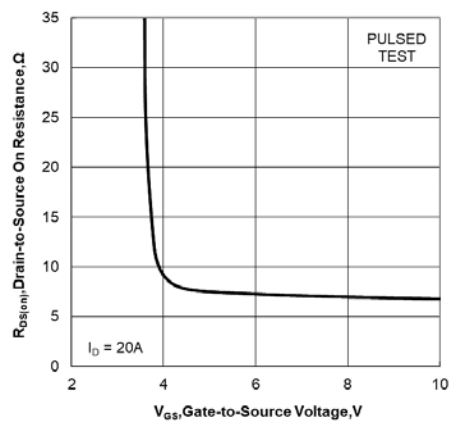


Figure 11. Drain-to-Source On Resistance vs Gate

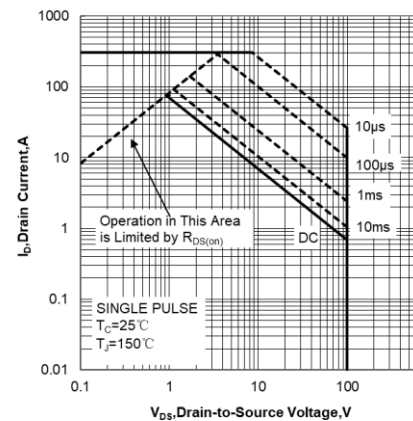


Figure 12. Maximum Safe Operating Area

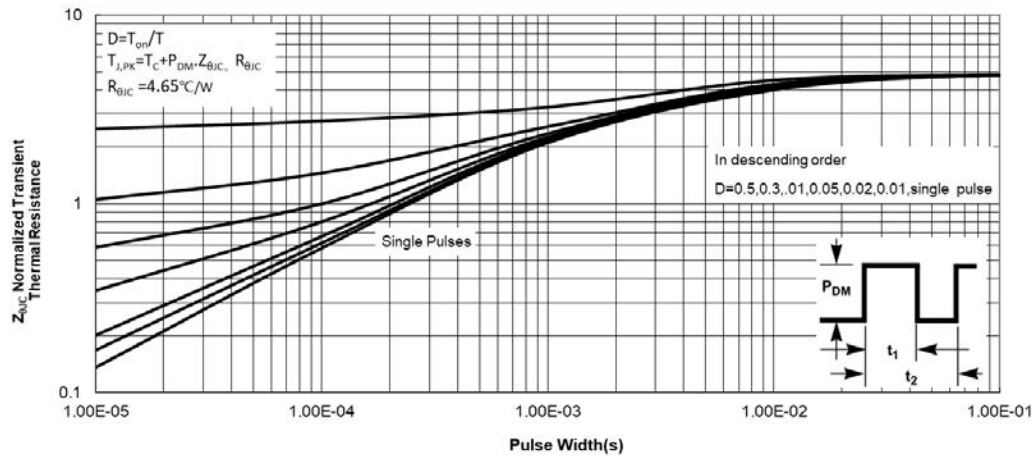
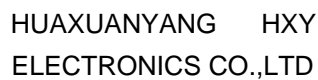
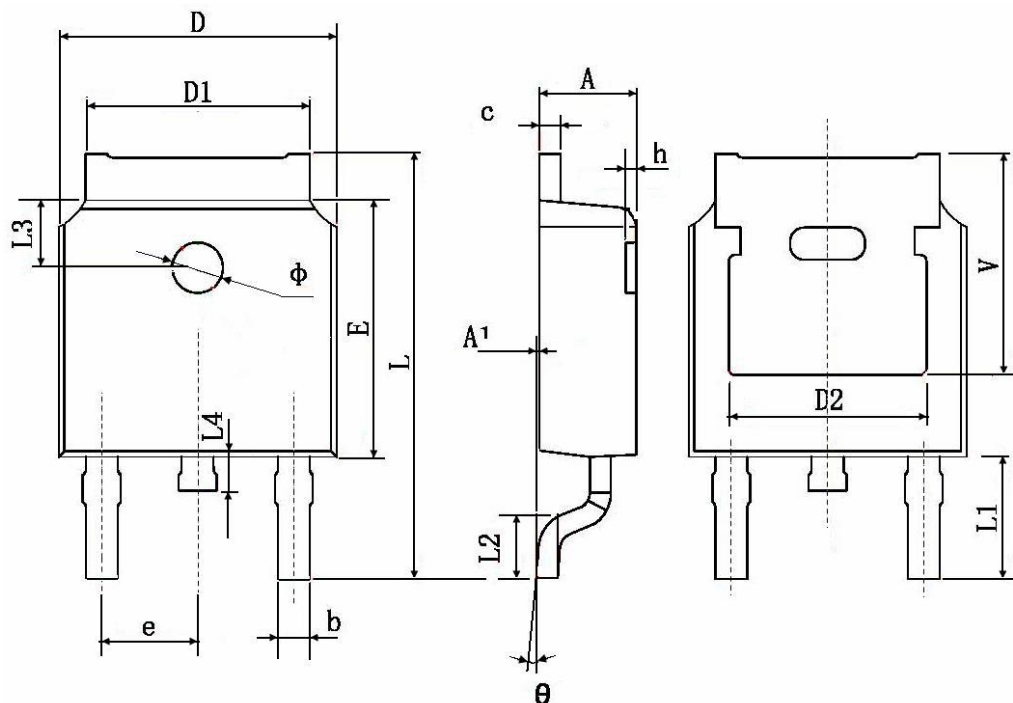


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case



SQD40N10-25-T4_GE3
N-SGT Enhancement Mode MOSFET

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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