

MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process.

Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)} * Q_g$ and $R_{DS(on)} * E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product validation

Fully qualified according to JEDEC for Industrial Applications

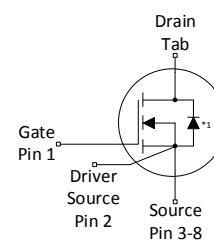
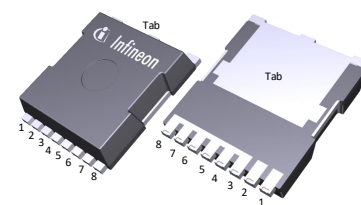
Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	45	mΩ
$Q_{g,typ}$	79	nC
$I_{D,pulse}$	153	A
$E_{oss} @ 400V$	9.1	μJ
Body diode di_F/dt	1300	A/μs

Part number	Package	Marking	Related links
IPT60R045CFD7	PG-HSOF-8	60R045F7	see Appendix A

TOLL



*1: Internal body diode

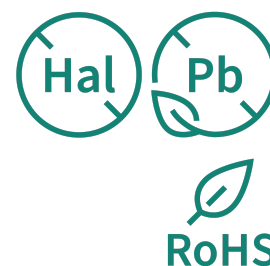




Table of contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Test circuits 11

Package outlines 12

Appendix A 15

Revision history 16

Trademarks 17

Disclaimer 17

1 Maximum ratings

at $T_J = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	52	A	$T_C = 25^\circ\text{C}$
				33		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	153	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	180	mJ	$I_D = 6.5\text{A}$; $V_{DD} = 50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}			0.90		
Avalanche current, single pulse	I_{AS}	-	-	6.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	272	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_J	-55		150	$^\circ\text{C}$	
Mounting torque	-	-		n.a.	Ncm	
Continuous diode forward current ¹⁾	I_S	-	-	52	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$			153		
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 38\text{A}$, $T_J = 25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di_F/dt			1300	A/ μs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C = 25^\circ\text{C}$, $t = 1\text{min}$

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.46	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.9mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600V, V_{GS}=0V, T_j=25^\circ\text{C}$
Zero gate voltage drain current ⁴⁾	I_{DSS}	-	19	75	μA	$V_{DS}=600V, V_{GS}=0V, T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.038	0.045	Ω	$V_{GS}=10V, I_D=18.0A, T_j=25^\circ\text{C}$
			0.086	-		$V_{GS}=10V, I_D=18.0A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	5.8	-	Ω	$f=1MHz$, open drain

⁴⁾ Maximum specification is defined by calculated six sigma upper confidence bound

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3194	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	C_{oss}		62			
Effective output capacitance, energy related ⁵⁾	$C_{o(er)}$	-	114	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ⁶⁾	$C_{o(tr)}$	-	1166	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	27	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=13.7A, R_G=3.0\Omega$; see table 9
Rise time	t_r		19			
Turn-off delay time	$t_{d(off)}$		101			
Fall time	t_f		5			

⁵⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

⁶⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

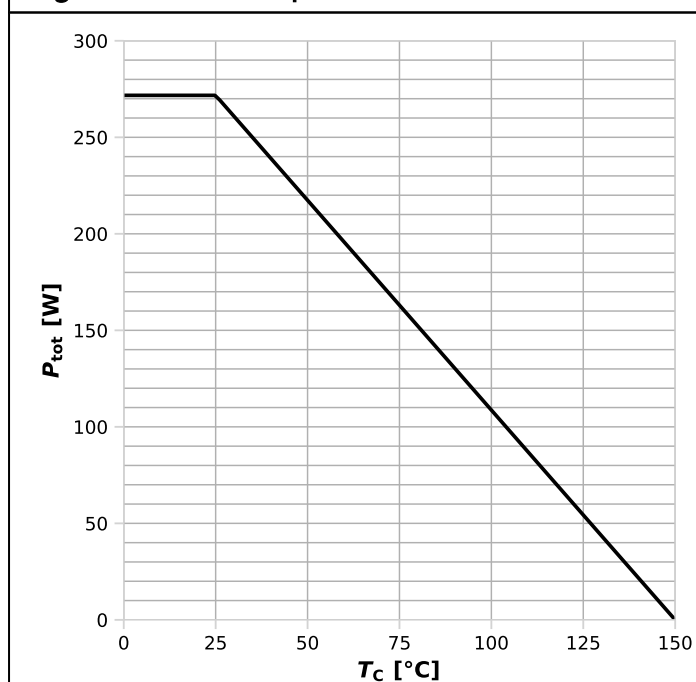
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	18	-	nC	$V_{DD}=400V$, $I_D=13.7A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}		28		nC	
Gate charge total	Q_g		79		nC	
Gate plateau voltage	$V_{plateau}$		5.5		V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V$, $I_F=18.0A$, $T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	132	198	ns	$V_R=400V$, $I_F=13.7A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}		0.68	1.37	μC	
Peak reverse recovery current	I_{rrm}		8.8	-	A	

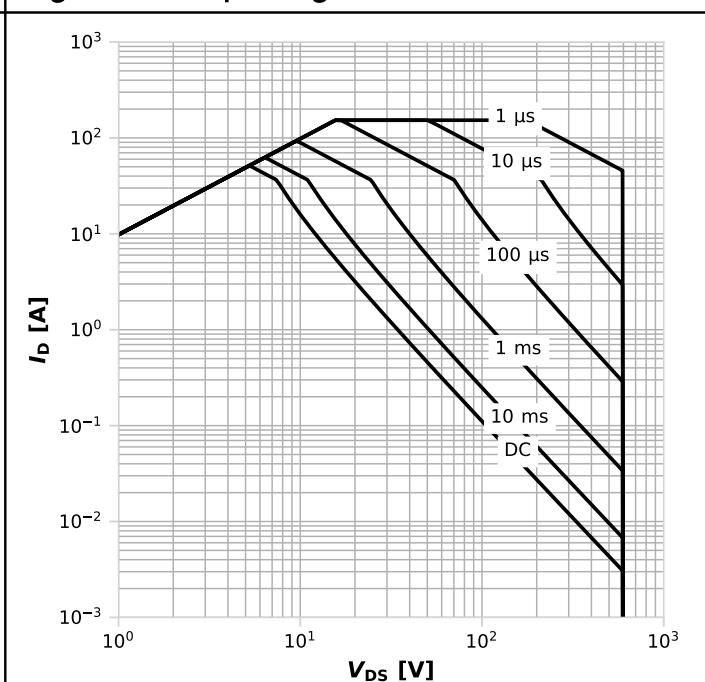
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



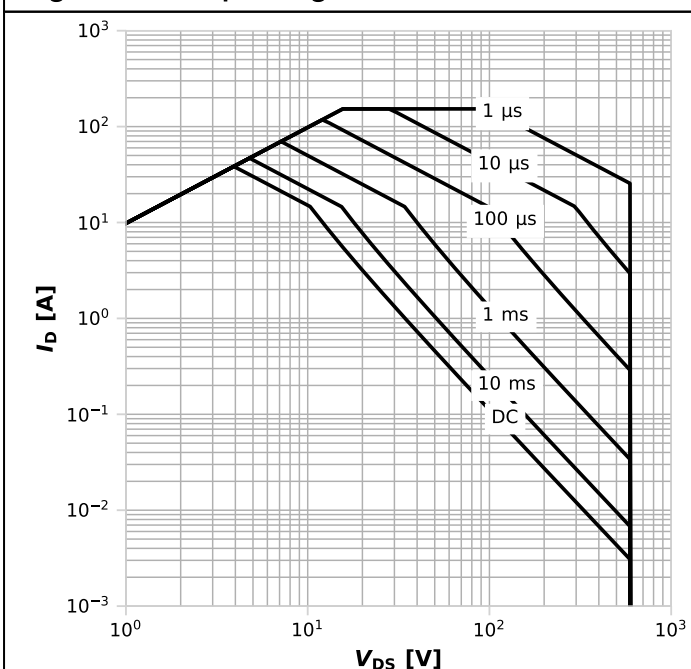
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Safe operating area



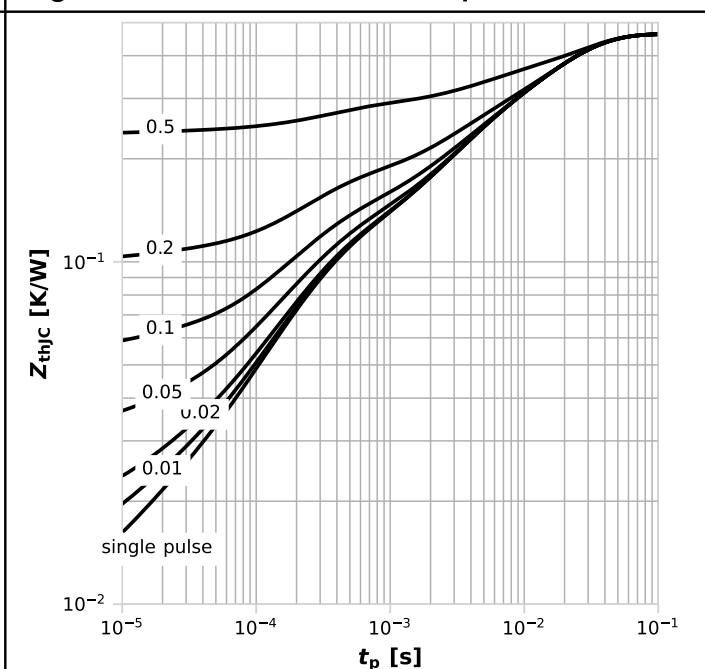
$$I_D = f(V_{DS}); T_c = 25\text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 3: Safe operating area



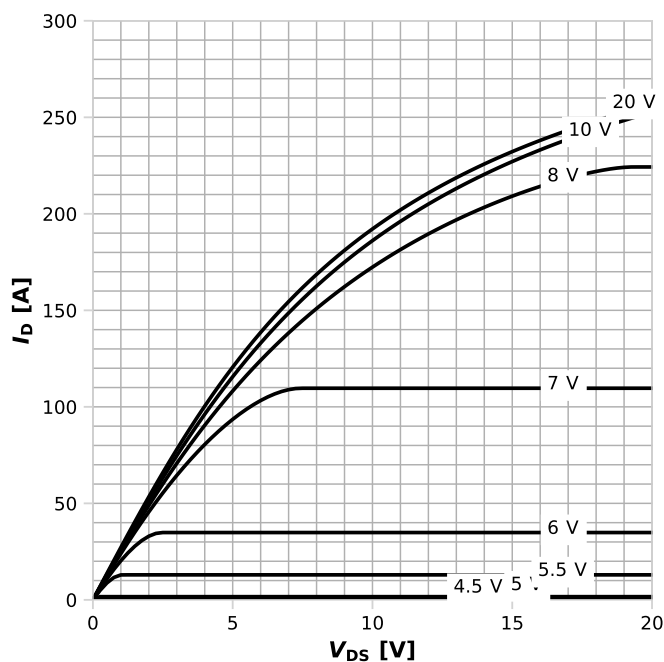
$$I_D = f(V_{DS}); T_c = 80\text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



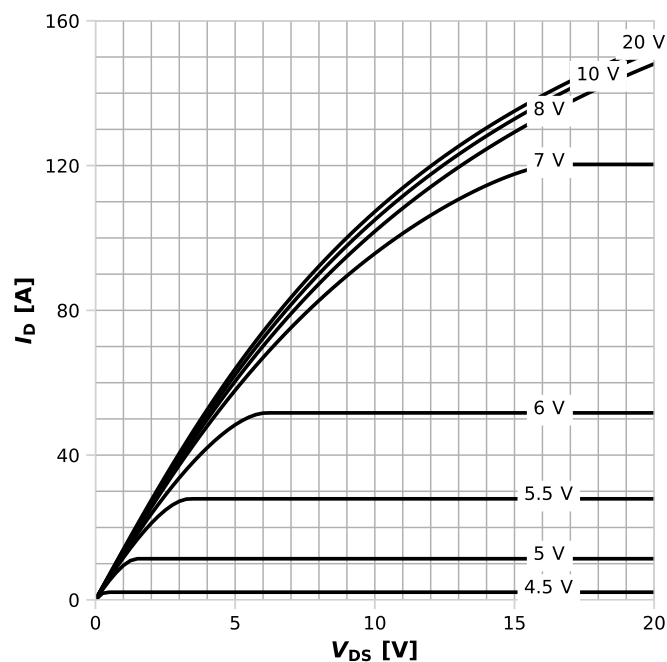
$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics



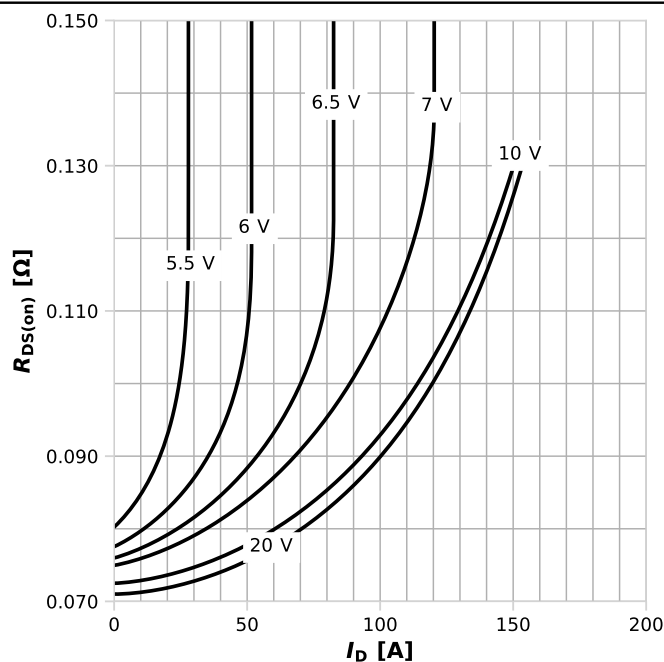
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics



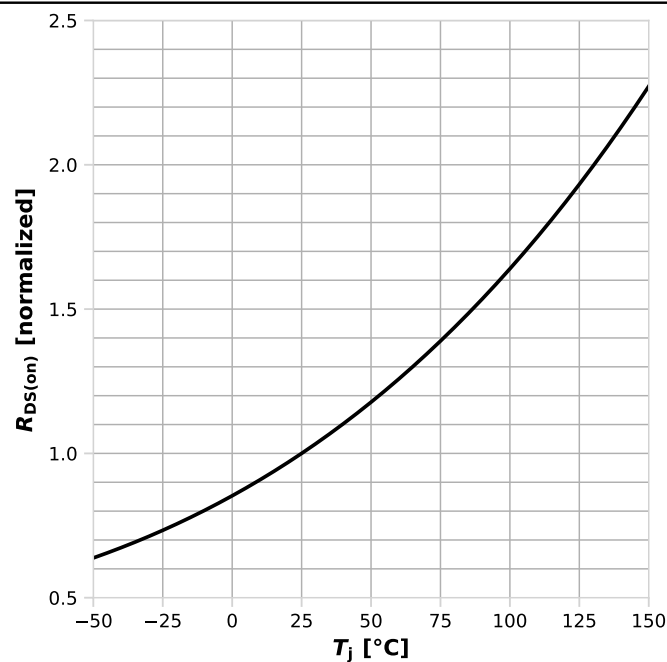
$I_D = f(V_{DS}); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



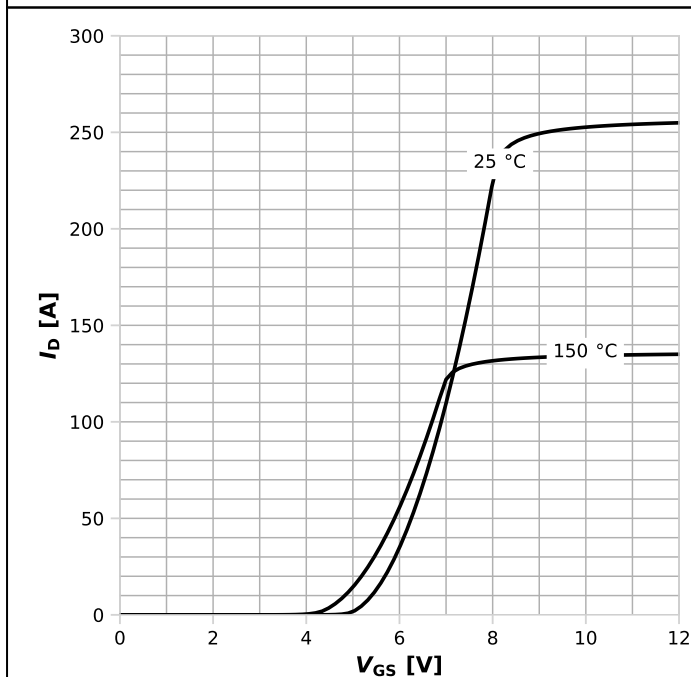
$R_{DS(on)} = f(I_D); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance



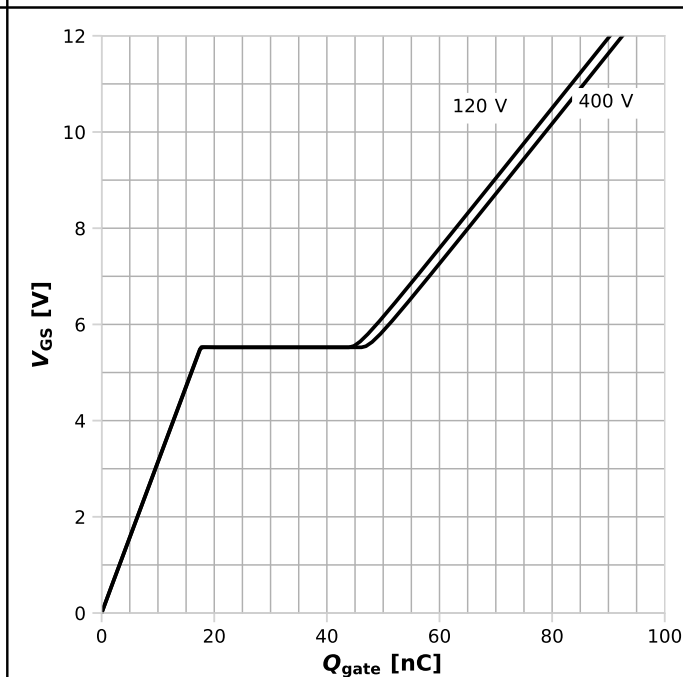
$R_{DS(on)} = f(T_j); I_D = 18.0\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



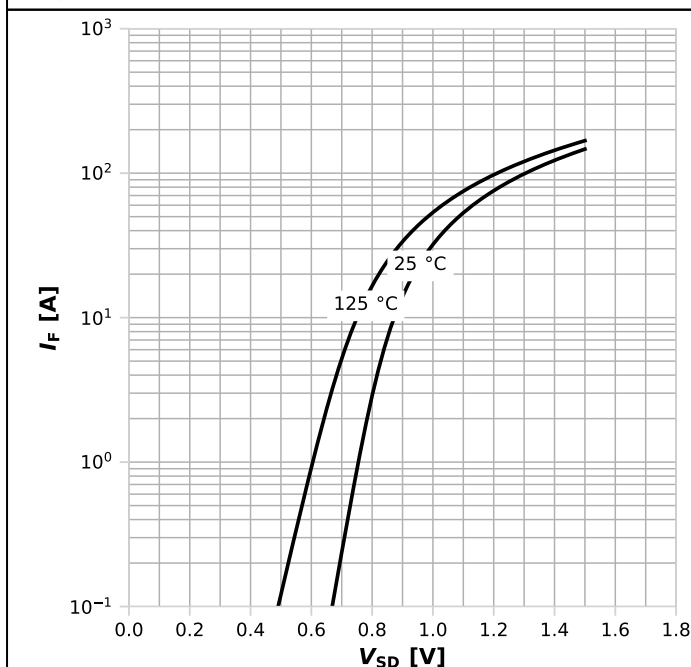
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



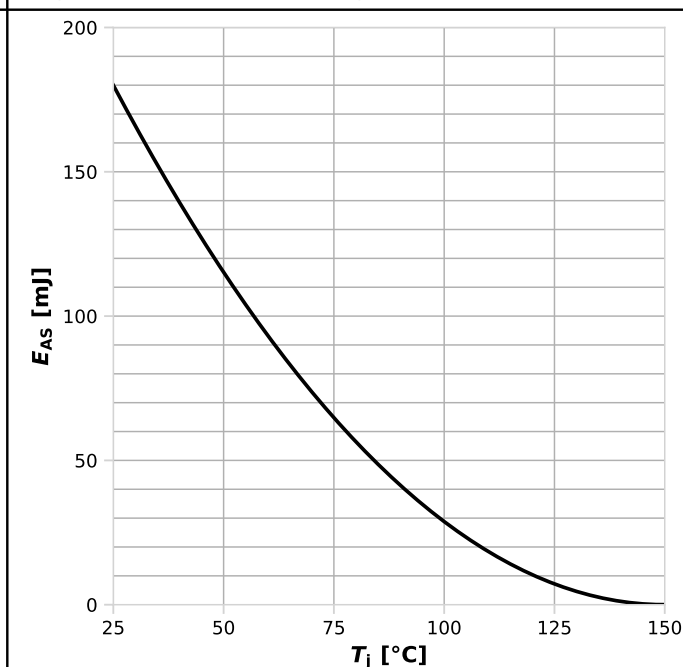
$V_{GS} = f(Q_{gate})$; $I_D = 13.7$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



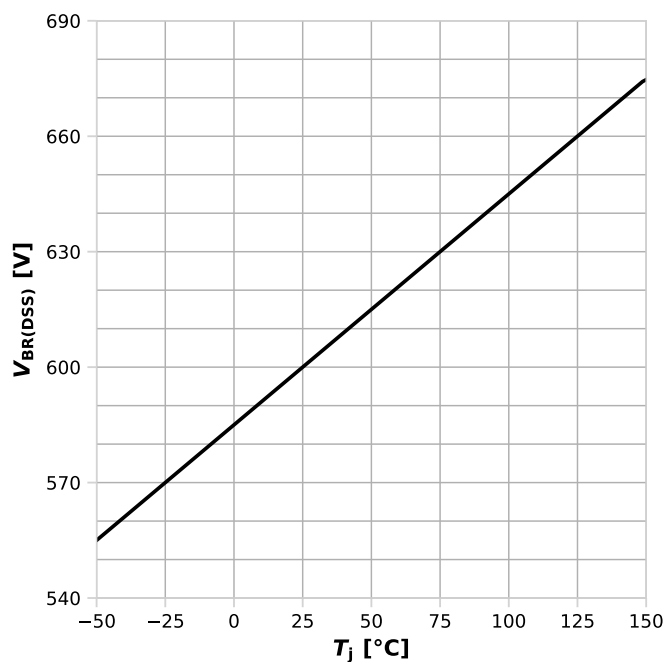
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



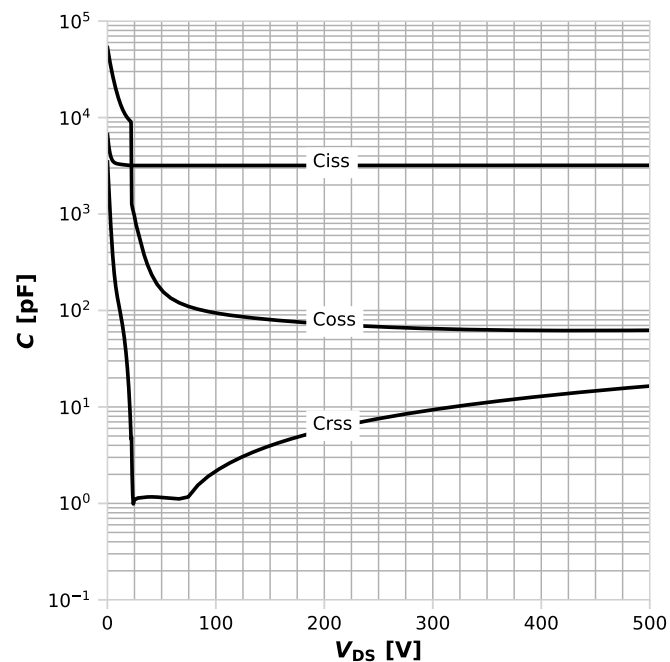
$E_{AS} = f(T_j)$; $I_D = 6.5$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



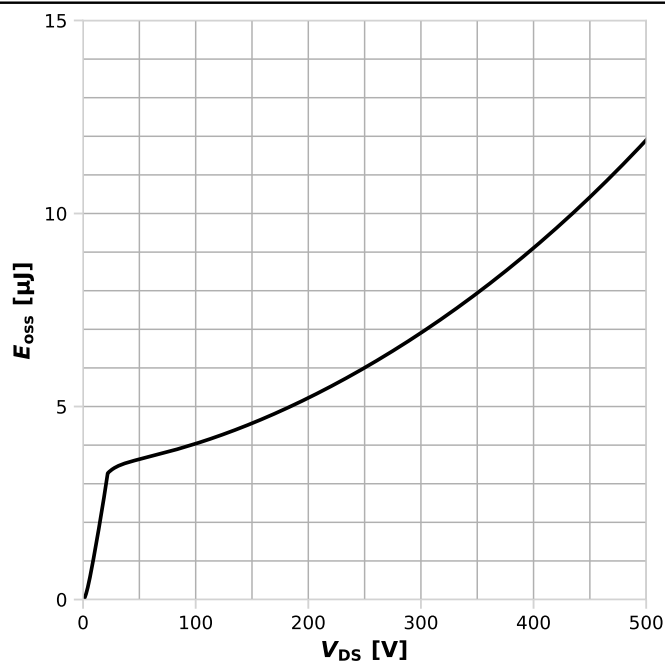
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

5 Test circuits

Table 8 Diode characteristics

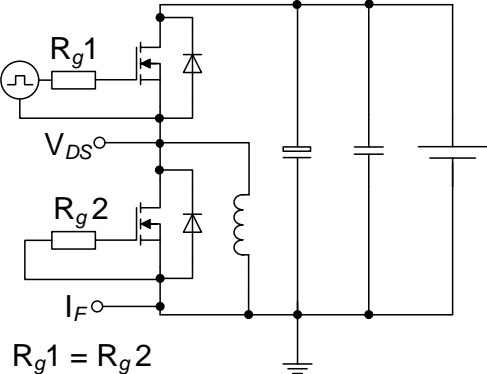
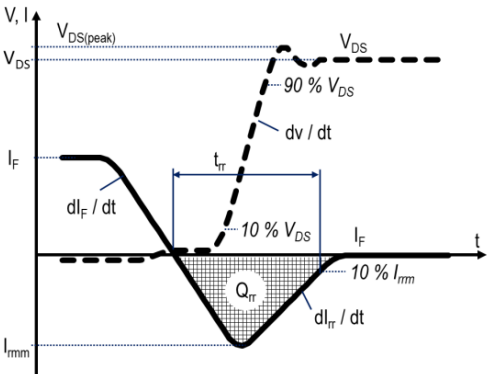
Test circuit for diode characteristics	Diode recovery waveform
 <p>$R_{g1} = R_{g2}$</p>	

Table 9 Switching times (ss)

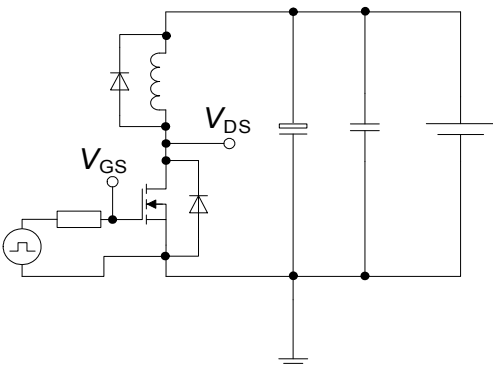
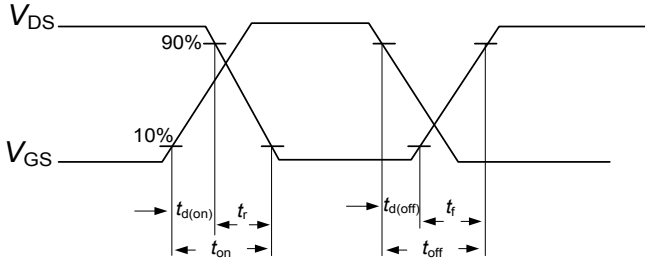
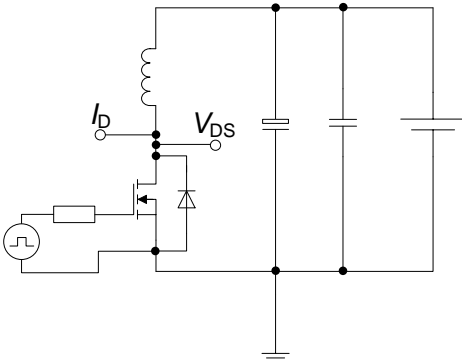
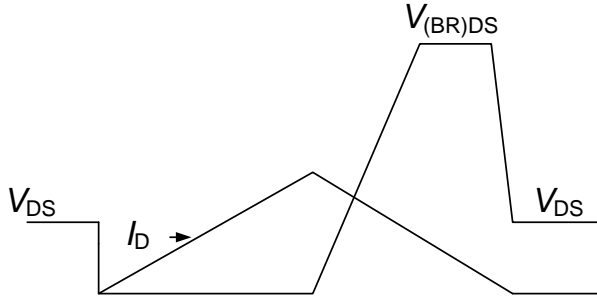
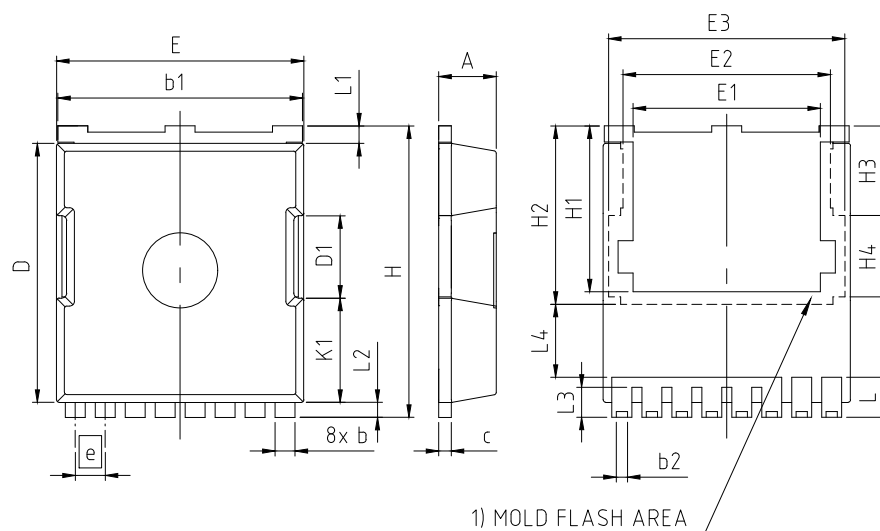
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



PACKAGE - GROUP NUMBER: PG-HSOF-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

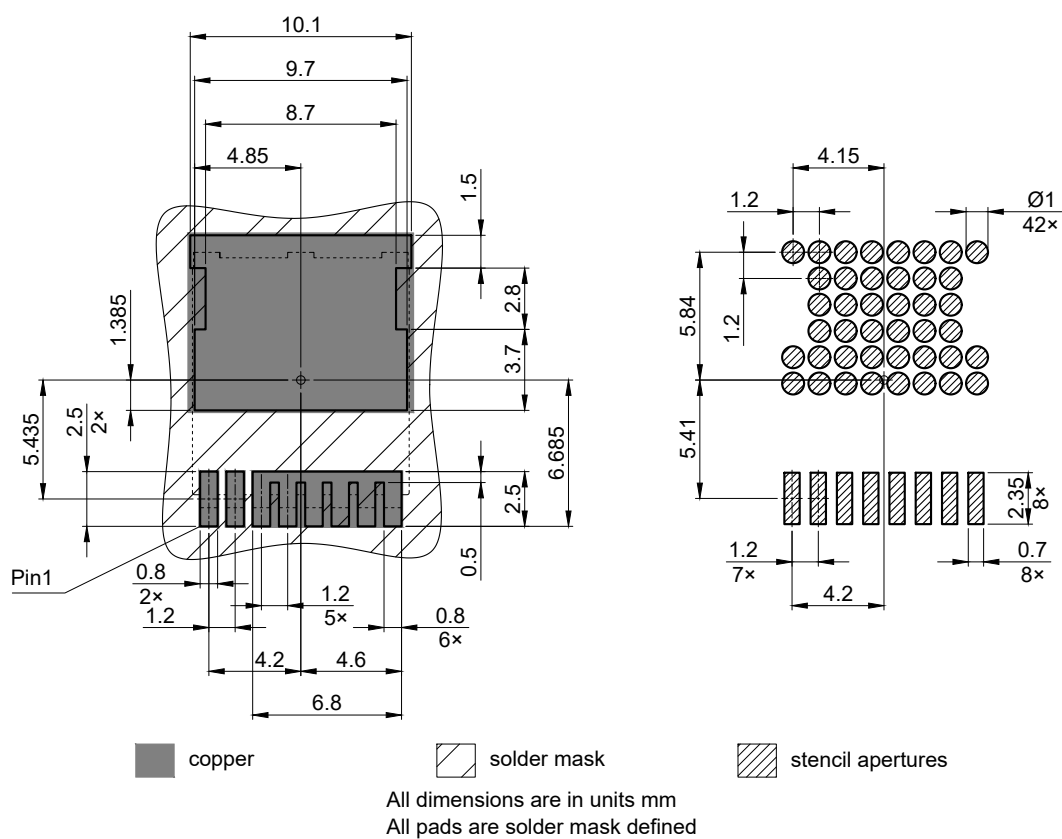
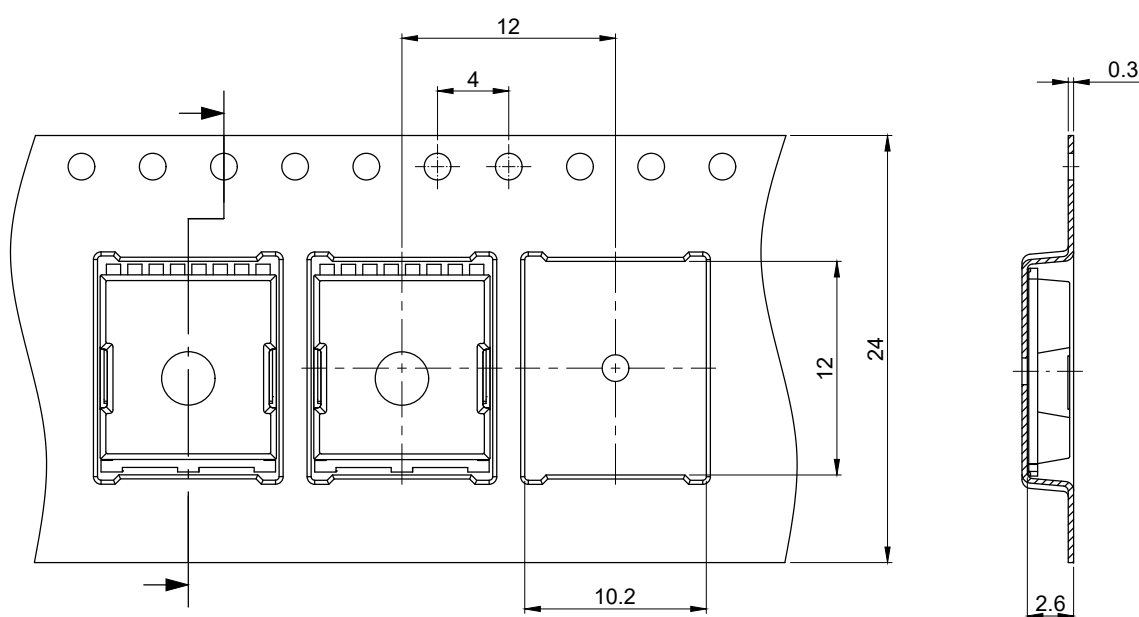


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm


The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 **Related links**

- [IFX CoolMOS™ CFD7 Webpage](#)
- [IFX CoolMOS™ CFD7 application note](#)
- [IFX CoolMOS™ CFD7 simulation model](#)
- [IFX Design tools](#)

Revision history

IPT60R045CFD7

Revision 2025-02-03, Rev. 2.4

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2020-04-22	Release of final version
2.1	2020-06-23	Changed diode commutation speed current
2.2	2020-08-28	Changed trr value
2.3	2020-11-11	Changed diagram 2, 3, 7, 8, 9; Changed typical static and dynamic parameters
2.4	2025-02-03	Implementation of standardized Infineon Umbrella-Templates for package drawings. H1 Extension from 6.75 to 6.95 MAX

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG

81726 München, Germany

© 2025 Infineon Technologies AG

All Rights Reserved.

Important notice

The products which may also include samples and may be comprised of hardware or software or both ("Product") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Product or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

If the Product includes security features:

Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:

The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).