

# MOSFET – N-Channel, POWER TRENCH®

100 V, 11.2 A, 9.8 mΩ

## FDS86140

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWER TRENCH process that has been optimized for  $R_{DS(on)}$ , switching performance and ruggedness.

### Features

- Max  $R_{DS(on)}$  = 9.8 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 11.2 A
- Max  $R_{DS(on)}$  = 16 mΩ at  $V_{GS}$  = 6 V,  $I_D$  = 9 A
- High Performance Trench Technology for extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- DC/DC Converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier

### MOSFET MAXIMUM RATINGS ( $T_A$ = 25°C unless otherwise noted)

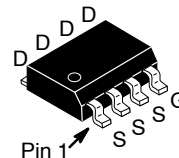
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current	Continuous	11.2 A
		Pulsed	50
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	264	mJ
$P_D$	Power Dissipation	$T_C$ = 25°C (Note 1)	5.0 W
		$T_A$ = 25°C (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

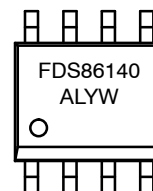
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

$V_{DS}$	$R_{DS(on)}$ Max	$I_D$ MAX
100 V	9.8 mΩ @ 10 V	11.2 A



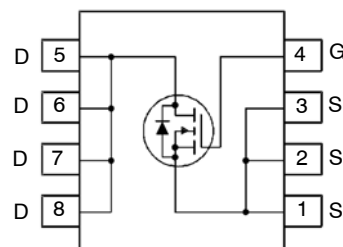
SOIC8  
CASE 751EB

### MARKING DIAGRAM



FDS86140 = Device Code  
A = Assembly Site  
L = Wafer Lot Number  
YW = Assembly Start Week

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping†
FDS86140	SOIC8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

# FDS86140

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	70	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$ , $V_{GS} = 0\ \text{V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage, Forward	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	–11	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 11.2\ \text{A}$	–	8.1	9.8	m $\Omega$
		$V_{GS} = 6\ \text{V}$ , $I_D = 9\ \text{A}$	–	10.8	16	
		$V_{GS} = 10\ \text{V}$ , $I_D = 11.2\ \text{A}$ , $T_J = 125^\circ\text{C}$	–	13.1	17	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}$ , $I_D = 11.2\ \text{A}$	–	35	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 50\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	–	1940	2580	pF
$C_{oss}$	Output Capacitance		–	440	585	pF
$C_{rss}$	Reverse Transfer Capacitance		–	20	30	pF
$R_g$	Gate Resistance		–	0.9	–	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$ , $I_D = 11.2\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$	–	13.7	25	ns
$t_r$	Rise Time		–	5.6	11	ns
$t_{d(off)}$	Turn-Off Delay Time		–	23	38	ns
$t_f$	Fall Time		–	4.8	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$ , $V_{DD} = 50\ \text{V}$ , $I_D = 11.2\ \text{A}$	–	29	41	nC
		$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$ , $V_{DD} = 50\ \text{V}$ , $I_D = 11.2\ \text{A}$	–	16.5	23	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\ \text{V}$ , $I_D = 11.2\ \text{A}$	–	8.0	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	6.5	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 11.2\ \text{A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\ \text{V}$ , $I_S = 2\ \text{A}$ (Note 2)	–	0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 11.2\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$	–	53	85	ns
$Q_{rr}$	Reverse Recovery Charge		–	59	94	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



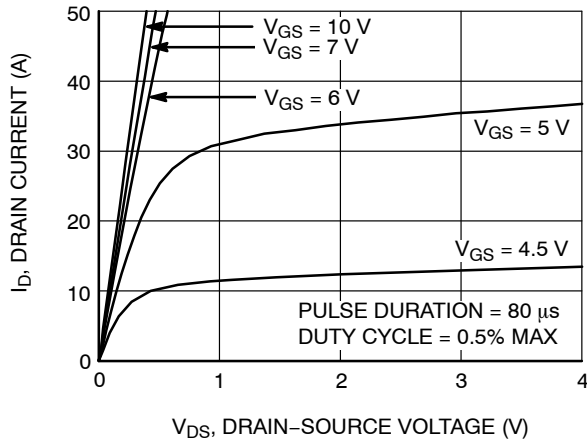
a)  $50^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz. copper.



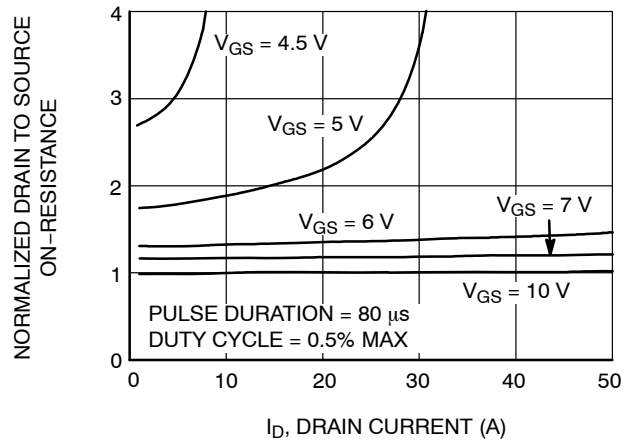
b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 23\ \text{A}$ ,  $V_{DD} = 90\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

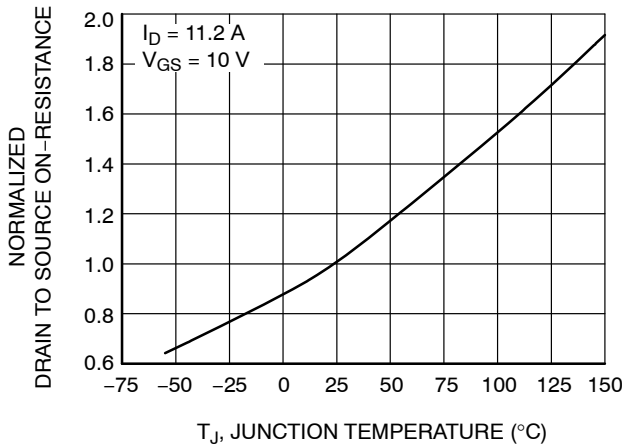
**TYPICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)



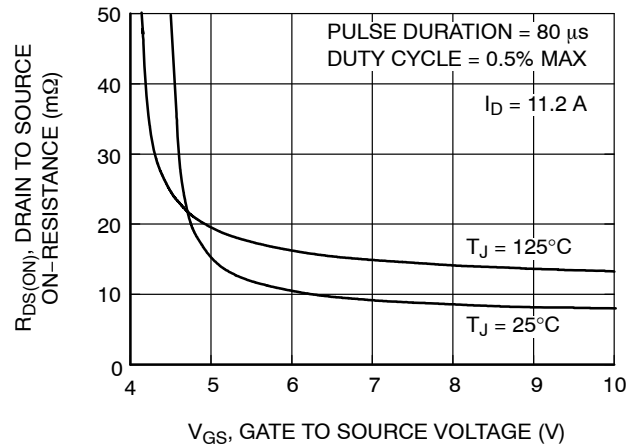
**Figure 1. On Region Characteristics**



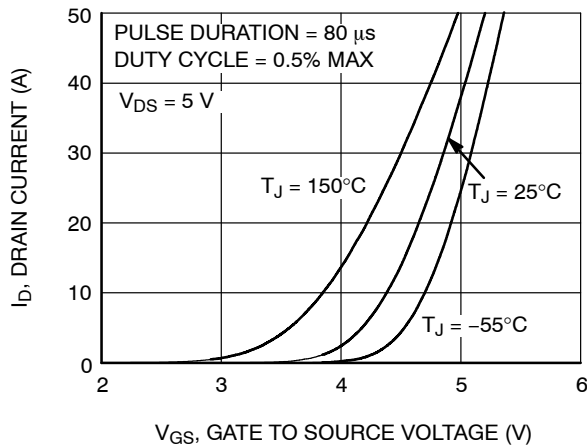
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



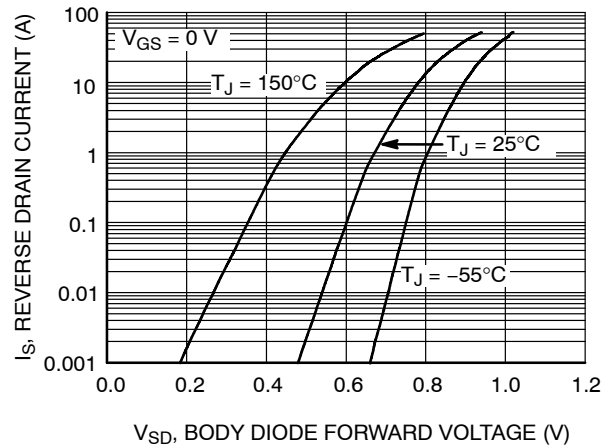
**Figure 3. Normalized On-Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

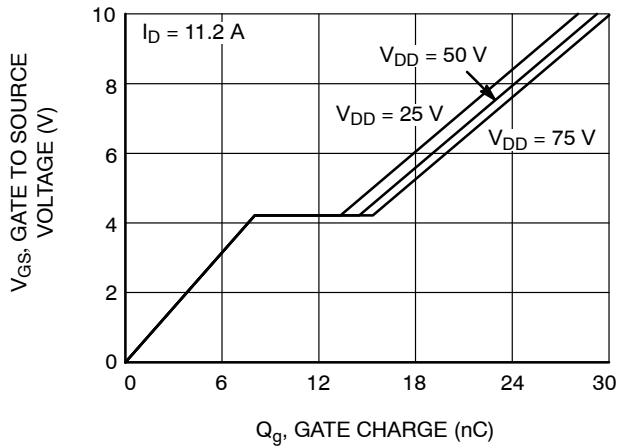


**Figure 5. Transfer Characteristics**

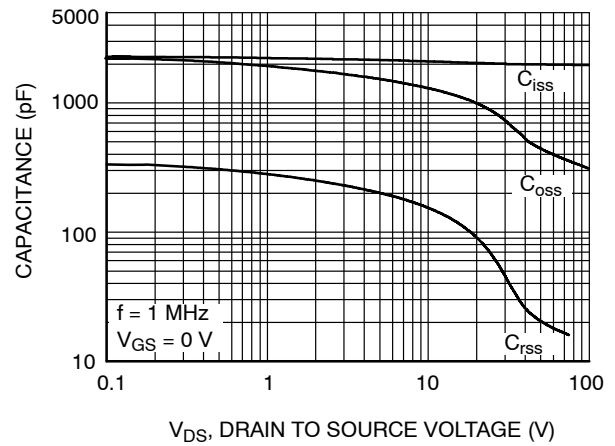


**Figure 6. Body to Drain Diode Forward Voltage vs. Source Current**

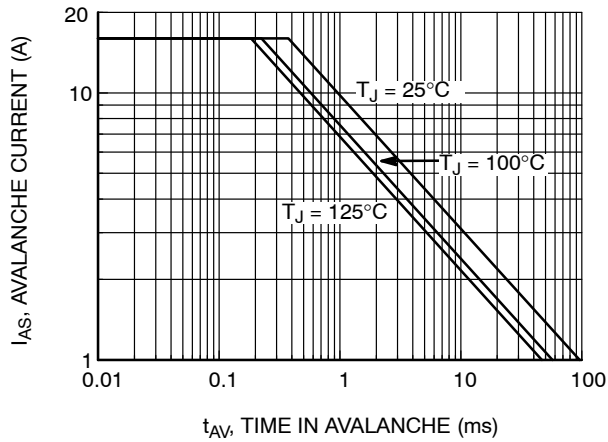
**TYPICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)



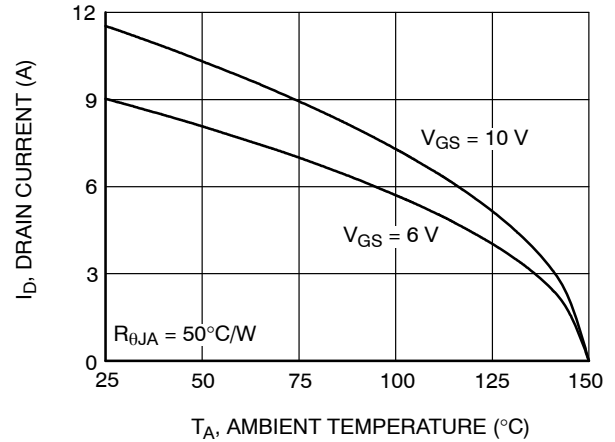
**Figure 7. Gate Charge Characteristics**



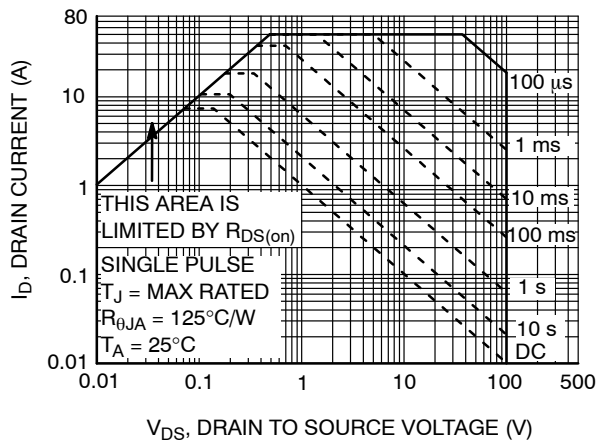
**Figure 8. Capacitance vs. Drain to Source Voltage**



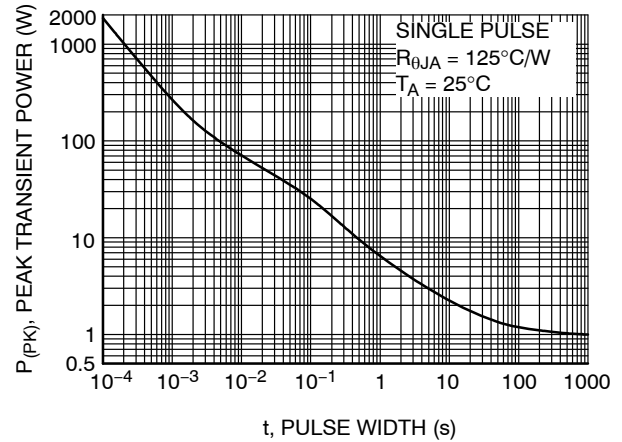
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

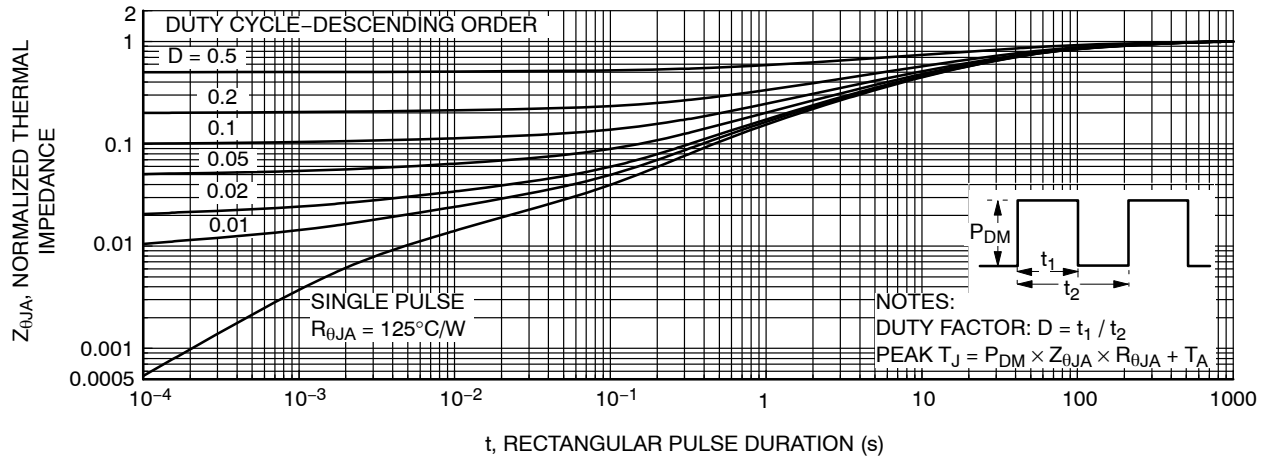
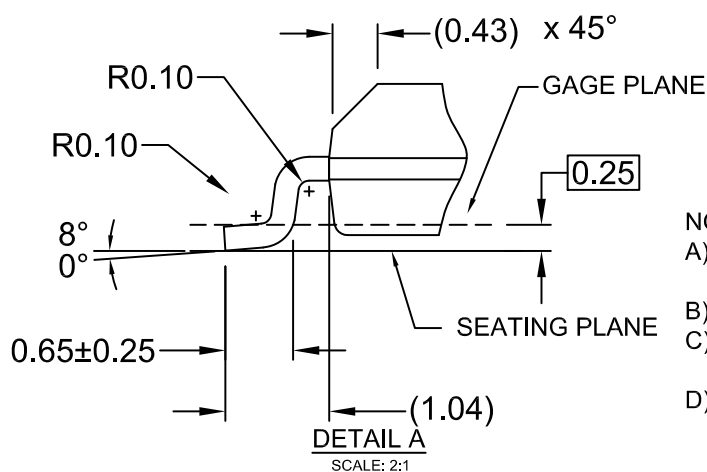
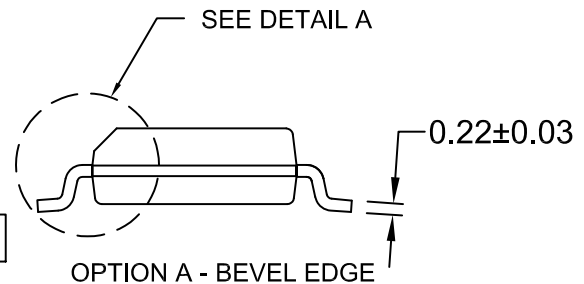
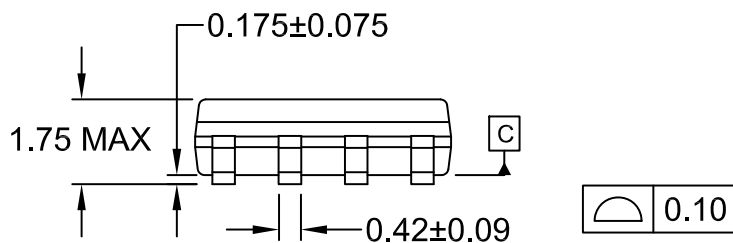
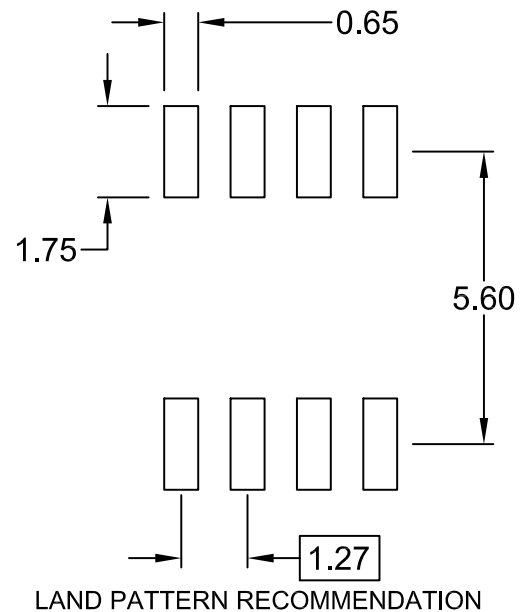
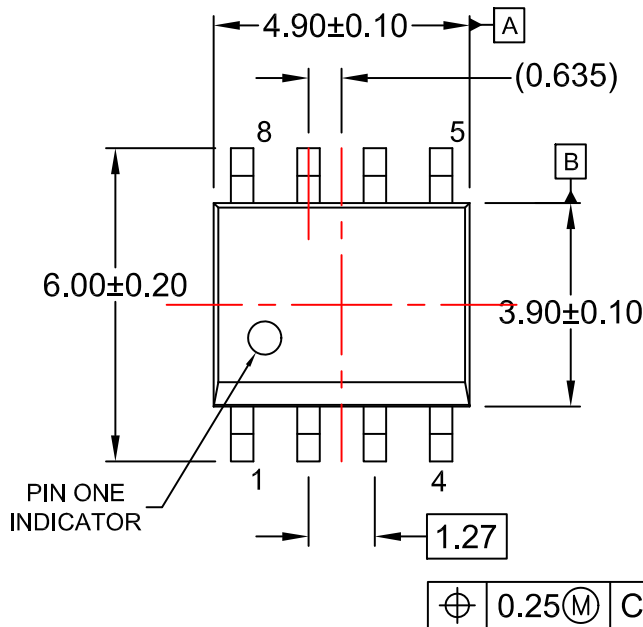
TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

Figure 13. Junction-to-Ambient Thermal Response Curve

**SOIC8**  
**CASE 751EB**  
**ISSUE A**

DATE 24 AUG 2017



**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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