

MOSFET - Power, Single N-Channel, Source Down DualCool 33, WDFN9

80 V, 4 mΩ, 102 A

Product Preview

NTTFSSCH4D0N08XL

Features

- Excellent Thermal Conduction by Advanced Source-Down Center Gate Dual-Cooling Package Technology (3.3x3.3mm)
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Low Q_G and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectifier

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

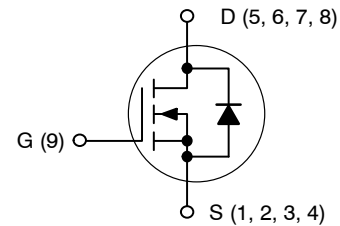
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25^{\circ}\text{C}$	I_D	102	A
	$T_C = 100^{\circ}\text{C}$		72	
Power Dissipation (Notes 1, 2)	$T_C = 25^{\circ}\text{C}$	P_D	102	W
Pulsed Drain Current	$T_C = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$	I_{DM}	668	A
Pulsed Source Current (Body Diode)		I_{SM}	668	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)		I_S	155	A
Single Pulse Avalanche Energy ($I_{PK} = \text{TBD A}$)		E_{AS}	TBD	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

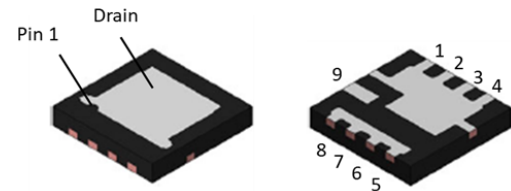
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	4 mΩ @ 10 V	102 A
	6 mΩ @ 4.5 V	

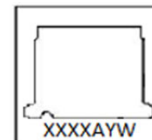


N-CHANNEL MOSFET



WDFN9
CASE 511BX

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NTTFSSCH4D0N08XL

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	1.47	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	1.24	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		31		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 80\text{ V}, T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$		3.3	4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		4.8	6	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 115\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	1.5		2.1	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 115\text{ }\mu\text{A}$		-6.3		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 23\text{ A}$		120		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		3420		pF
Output Capacitance	C_{OSS}			550		
Reverse Transfer Capacitance	C_{RSS}			18		
Output Charge	Q_{OSS}			45		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V}; I_D = 23\text{ A}$		22		nC
				47		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}; I_D = 23\text{ A}$		7		
Gate-to-Source Charge	Q_{GS}			11		
Gate-to-Drain Charge	Q_{GD}			5		
Gate Plateau Voltage	V_{GP}			3.2		V
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.4		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 23\text{ A}, R_G = 2.5\text{ }\Omega$		18		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(OFF)}$			40		
Fall Time	t_f			5		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 25^\circ\text{C}$		0.82		V
		$V_{GS} = 0\text{ V}, I_S = 23\text{ A}, T_J = 125^\circ\text{C}$		0.66		

NTTFSSCH4D0N08XL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 23 A, dI/dt = 1000 A/μs, V _{DD} = 40 V		19		ns
Charge Time	t _a			11		
Discharge Time	t _b			8		
Reverse Recovery Charge	Q _{RR}			116		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

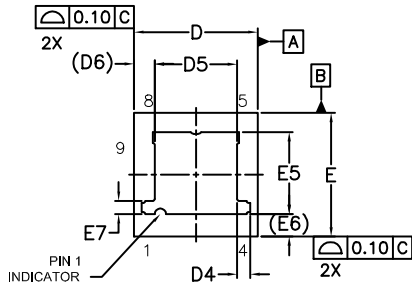
Device	Marking	Package	Shipping [†]
NTTFSSCH4D0N08XLTWG	TBD	WDFN9 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

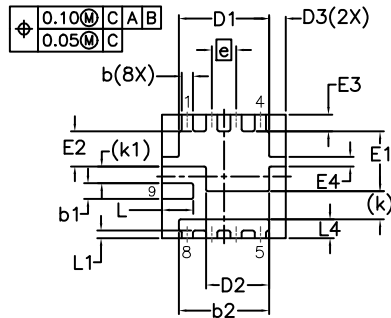
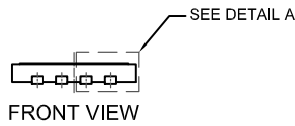
NTTFSSCH4D0N08XL

PACKAGE DIMENSIONS

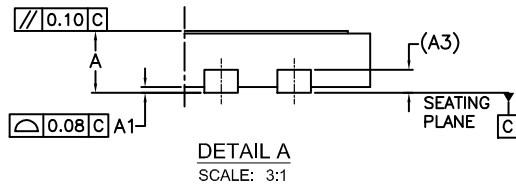
WDFN9 3.3x3.3, 0.65P
CASE 511BX
ISSUE A



TOP VIEW

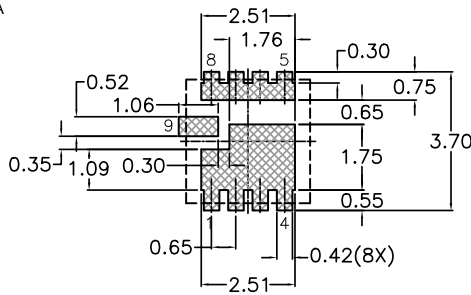


BOTTOM VIEW



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH. SEATING PLANE IS DEFINED BY THE TERMINALS.
5. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.48	0.58	0.68
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
b1	0.37	0.42	0.47
b2	0.37	0.42	0.47
D	3.20	3.30	3.40
D1	2.31	2.41	2.51
D2	1.58	1.68	1.78
D3	0.35	0.45	0.55
D4	0.25	0.35	0.45
D5	2.10	2.20	2.30
D6	0.55 REF		
E	3.20	3.30	3.40
E1	1.50	1.60	1.70
E2	0.84	0.94	1.04
E3	0.35	0.45	0.55
E4	0.20	0.25	0.30
E5	2.15	2.20	2.35
E6	0.60 REF		
E7	0.25	0.35	0.45
e	0.65 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L4	0.40	0.50	0.60

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