

Taiwan Semiconductor

PerFET[™]Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

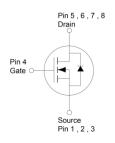
PRODUCT SUMMARY				
PARAMETER		VALUE	UNIT	
V_{DS}		40	V	
R _{DS(on)} (max)	$V_{GS} = 10V$	3.2	0	
	$V_{GS} = 4.5V$	4.5	mΩ	
Q_g	$V_{GS} = 4.5V$	23.7	nC	



APPLICATIONS

- DC-DC Converters
- · Solenoid and Motor Drivers
- Load Switch





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±16	V
Continuous Drain Current, Silicon limited	T _C = 25°C	I_{D}	143	Α
	$T_C = 25^{\circ}C$	I _D	81	
Continuous Drain Current (Note 1)	$T_C = 100$ °C		81	Α
	$T_A = 25$ °C		23	
Pulsed Drain Current		I_{DM}	324	Α
Single Pulse Avalanche Current (Note 2)		I _{AS}	31.8	Α
Single Pulse Avalanche Energy (Note 2)		E _{AS}	152	mJ
Total Power Discipation	T _C = 25°C	P _D	115	W
Total Power Dissipation	T _C = 125°C		38	VV
Operating Junction and Storage Temperature Range		T_J,T_STG	-55 to +175	°C

THERMAL RESISTANCE				
PARAMETER	SYMBOL	MAXIMUM	UNIT	
Thermal Resistance – Junction to Case	R _{eJC}	1.3	°C/W	
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W	

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

1

Taiwan Semiconductor

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 1mA$	BV _{DSS}	40			V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	1.4	1.8	2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 16V, V_{DS} = 0V$	I _{GSS}			±100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 40V$				1	μA
	$V_{GS} = 0V, V_{DS} = 40V$ $T_{J} = 125^{\circ}C$	I _{DSS}			100	
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 40A$	_		2.5	3.2	_
(Note 3)	$V_{GS} = 4.5V, I_D = 40A$	R _{DS(on)}		3.2	4.5	mΩ
Forward Transconductance (Note 3)	V _{DS} = 10V, I _D = 10A	g _{fs}		93		S
Dynamic						
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 20V,$ $I_{D} = 23A$	Q_g		23.7		
Total Gate Charge		Qg		50		nC
Gate-Source Charge	$V_{GS} = 10V, V_{DS} = 20V,$	Q_{gs}		9.8		
Gate-Drain Charge	I _D = 23A	Q_{gd}		6.9		
Input Capacitance	., ., ., ., .,	C _{iss}		3007		
Output Capacitance	$V_{GS} = 0V, V_{DS} = 25V,$ f = 1.0MHz	C _{oss}		562		рF
Reverse Transfer Capacitance	1 = 1.000112	C _{rss}		34		
Gate Resistance	f = 1.0MHz	R_g		0.7		Ω
Switching (Note 4)						
Turn-On Delay Time		t _{d(on)}		11.3		
Rise Time	$V_{GS} = 10V, V_{DS} = 20V,$	t _r		72.5		~ C
Turn-Off Delay Time	$I_D = 23A, R_G = 3.3\Omega$	t _{d(off)}			nS	
Fall Time		t _f		33.7		
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0V, I_{S} = 40A$	V _{SD}			1.1	V
Reverse Recovery Time	I _S = 23A,	t _{rr}		42		nS
Reverse Recovery Charge	di/dt = 100A/µs	Q _{rr}		41		nC

Notes:

- 1. Package current limit.
- 2. $L=0.3mH,\ V_{GS}=10V,\ R_G=25\Omega,\ Starting\ T_J=25^{\circ}C.$
- 3. Pulse test: Pulse Width \leq 300 μ s, duty cycle \leq 2%.
- 4. Switching time is essentially independent of operating temperature.

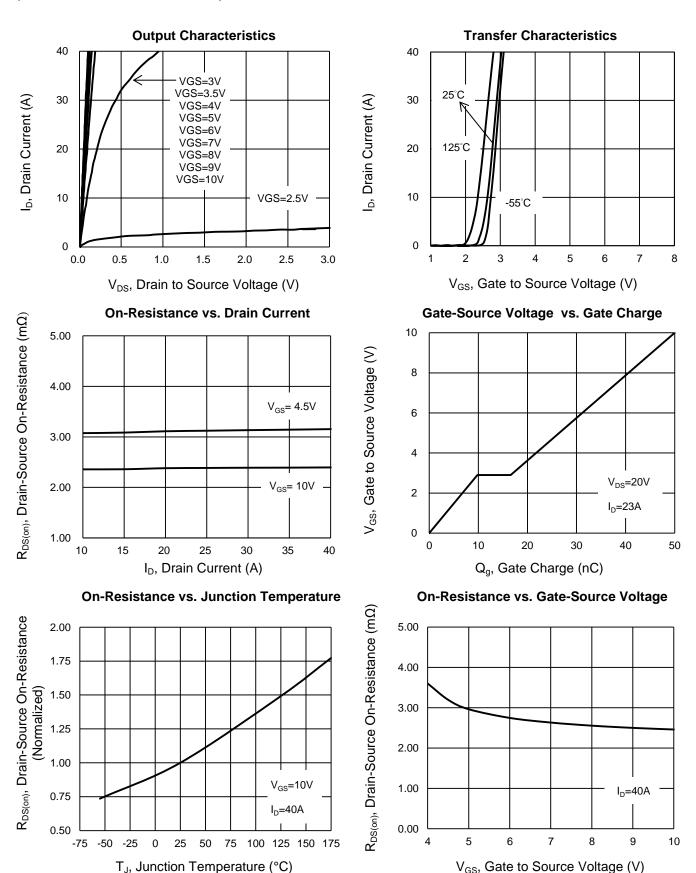
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM032NH04LCR RLG	PDFN56U	2,500pcs / 13" Reel



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

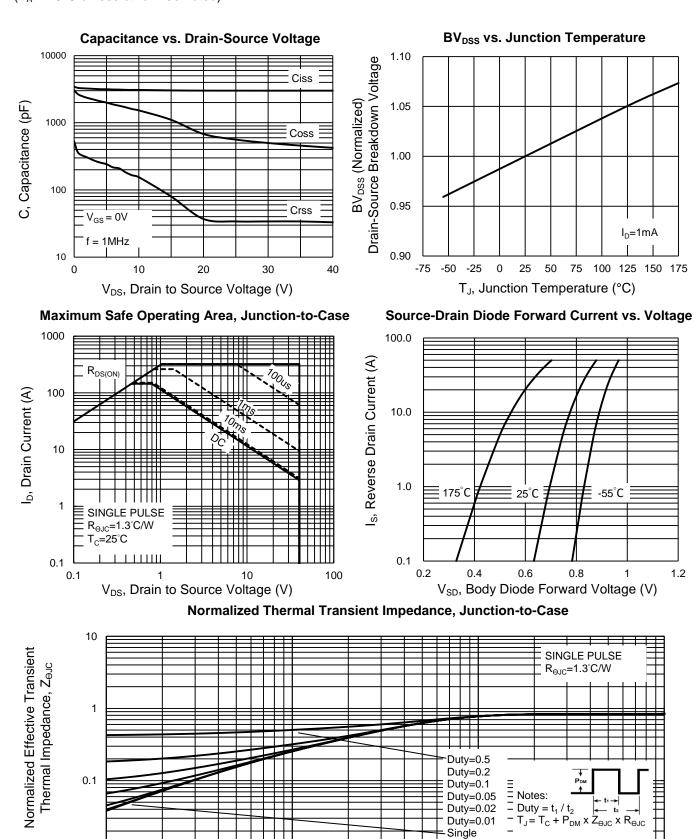




0.0001

CHARACTERISTICS CURVES

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$



t, Square Wave Pulse Duration (sec)

0.001

4 Version: D2207

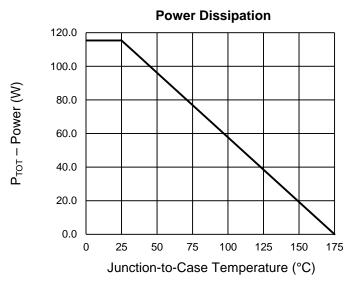
0.1

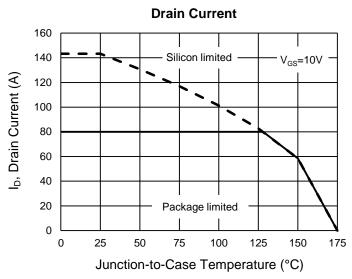
0.01



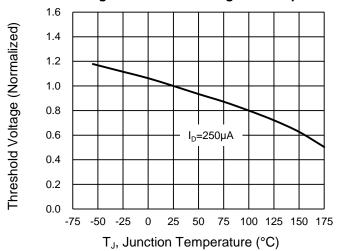
CHARACTERISTICS CURVES

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$





Normalized gate threshold voltage vs Temperature



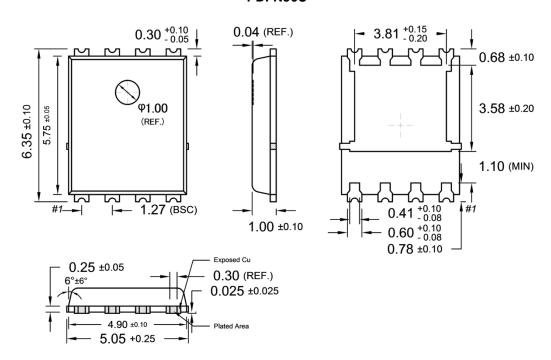
Version: D2207

5

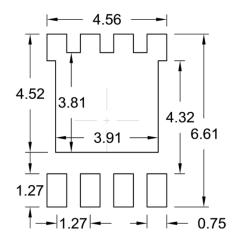


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U



SUGGESTED PAD LAYOUT (Unit: Millimeters)



6

MARKING DIAGRAM



Y = Year Code

WW = Week Code (01~52)

 $\mathbf{L} = \text{Lot Code } (1 \sim 9, A \sim Z)$

F = Factory Code



Taiwan Semiconductor

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Purchasers are solely responsible for the choice, selection, and use of TSC products and TSC assumes no liability for application assistance or the design of Purchasers' products.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.