

# MOSFET – N-Channel, QFET

**100 V, 70 A, 23 mΩ**

## FQA70N10

### Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 70 A, 100 V,  $R_{DS(on)} = 23 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 35 \text{ A}$
- Low Gate Charge (Typ. 85 nC)
- Low  $C_{RSS}$  (Typ. 150 pF)
- 100% Avalanche Tested
- 175 °C Maximum Junction Temperature Rating
- This is a Pb-Free Device

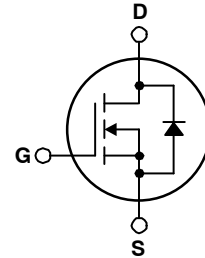
### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	100	V
$I_D$	Drain Current –Continuous ( $T_C = 25^\circ\text{C}$ )	70	A
	–Continuous ( $T_C = 100^\circ\text{C}$ )	49.5	A
$I_{DM}$	Drain Current –Pulsed (Note 1)	280	A
$V_{GSS}$	Gate–Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1300	mJ
$I_{AR}$	Avalanche Current (Note 1)	70	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	21.4	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	6.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	214	W
	–Derate Above $25^\circ\text{C}$	1.43	W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+175$	°C
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 seconds	300	°C

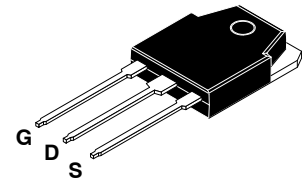
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 0.4 \text{ mH}$ ,  $I_{AS} = 70 \text{ A}$ ,  $V_{DD} = 25 \text{ V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 70 \text{ A}$ ,  $di/dt \leq 300 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

$V_{DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	23 mΩ @ 10 V	70 A

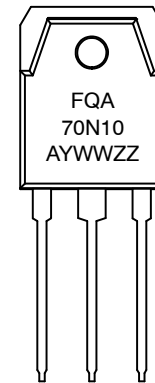


N-CHANNEL MOSFET



TO-3P-3LD  
CASE 340BZ

### MARKING DIAGRAM



FQA70N10	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

### ORDERING INFORMATION

Device	Package	Shipping
FQA70N10	TO-3P-3LD (Pb-Free)	450 Units / Tube

# FQA70N10

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	0.1	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\ \text{V}, V_{GS} = 0\ \text{V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 80\ \text{V}, T_C = 150^\circ\text{C}$	–	–	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\ \text{V}, V_{DS} = 0\ \text{V}$	–	–	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\ \text{V}, V_{DS} = 0\ \text{V}$	–	–	–100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 35\ \text{A}$	–	0.019	0.023	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\ \text{V}, I_D = 35\ \text{A}$	–	48	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1.0\ \text{MHz}$	–	2500	3300	pF
$C_{oss}$	Output Capacitance		–	720	940	pF
$C_{rss}$	Reverse Transfer Capacitance		–	150	200	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 70\ \text{A},$ $R_G = 25\ \Omega$ (Note 4)	–	30	70	ns
$t_r$	Turn-On Rise Time		–	470	950	ns
$t_{d(off)}$	Turn-Off Delay Time		–	130	270	ns
$t_f$	Turn-Off Fall Time		–	160	330	ns
$Q_g$	Total Gate Charge	$V_{DS} = 80\ \text{V}, I_D = 70\ \text{A},$ $V_{GS} = 10\ \text{V}$ (Note 4)	–	85	110	nC
$Q_{gs}$	Gate-Source Charge		–	16	–	nC
$Q_{gd}$	Gate-Drain Charge		–	42	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	70	A
I <sub>SM</sub>	Maximum Pulsed Drain–Source Diode Forward Current		–	–	280	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 70 A	–	–	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 70 A, dI <sub>F</sub> /dt = 100 A/μs	–	110	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	430	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature.

## TYPICAL CHARACTERISTICS (continued)

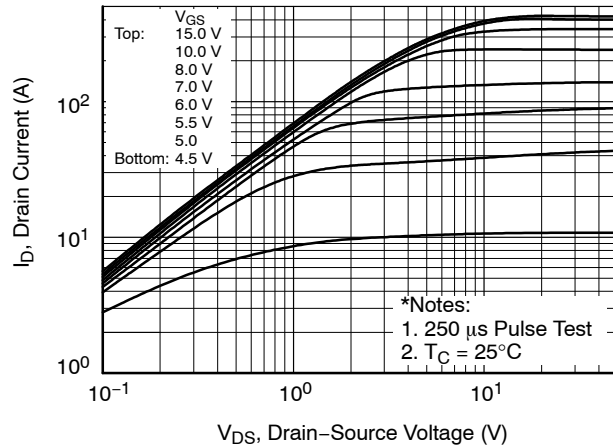


Figure 1. On-Region Characteristics

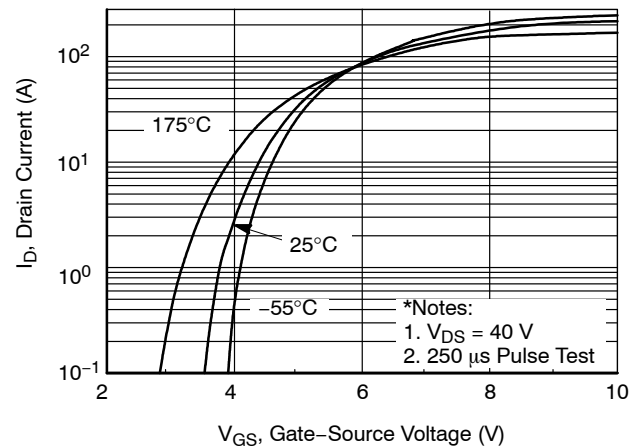


Figure 2. Transfer Characteristics

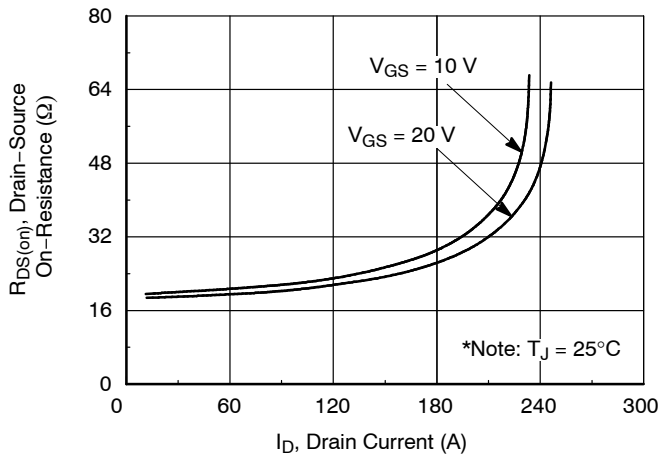


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

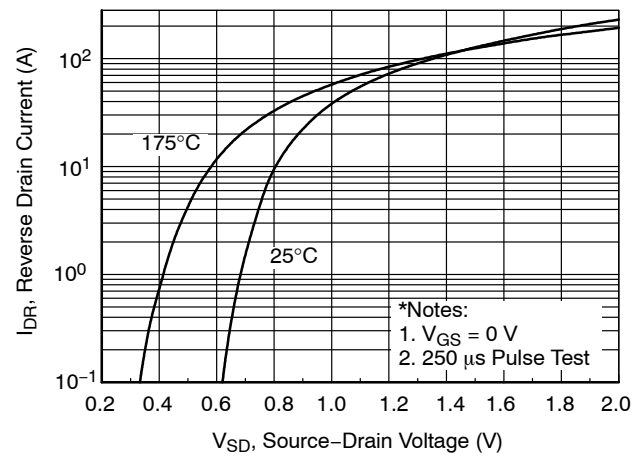


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

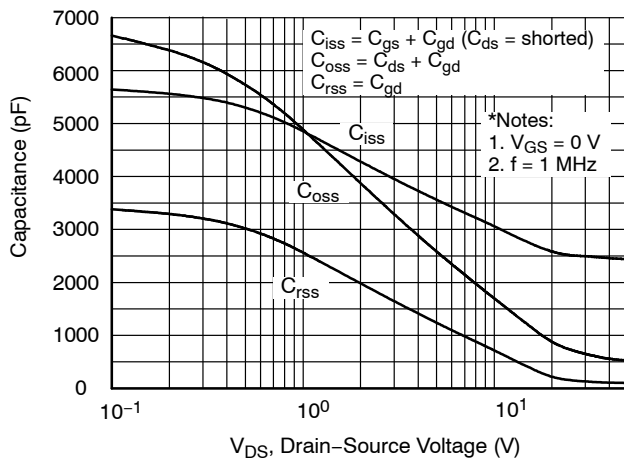


Figure 5. Capacitance Characteristics

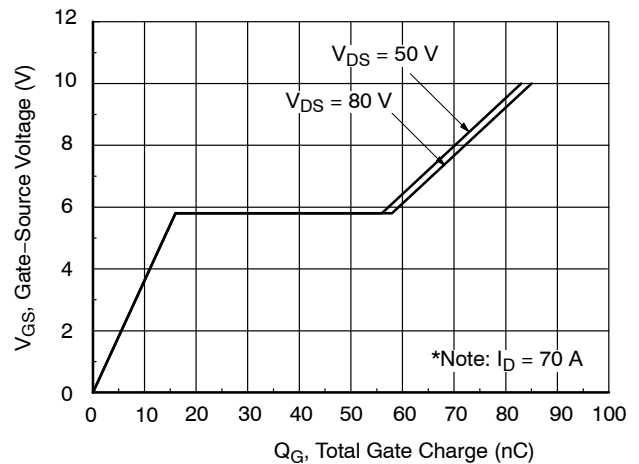


Figure 6. Gate Charge Characteristics

## TYPICAL CHARACTERISTICS

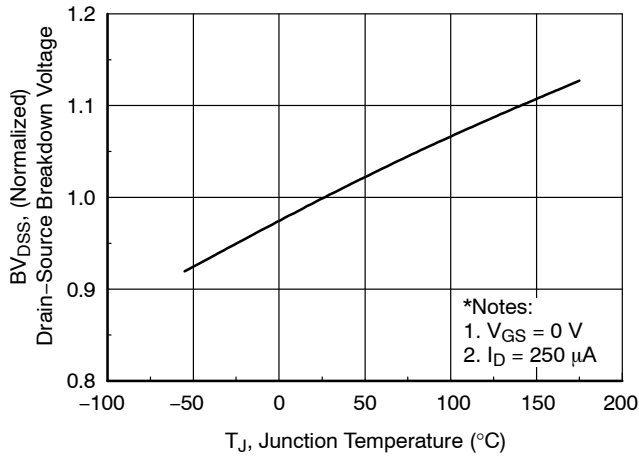


Figure 7. Breakdown Voltage Variation vs. Temperature

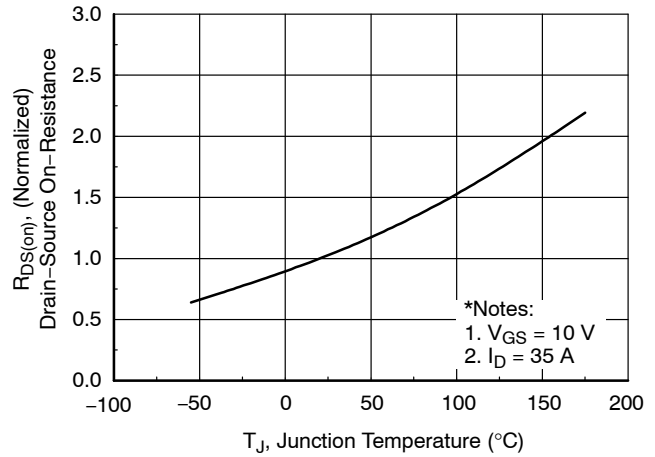


Figure 8. On-Resistance Variation vs. Temperature

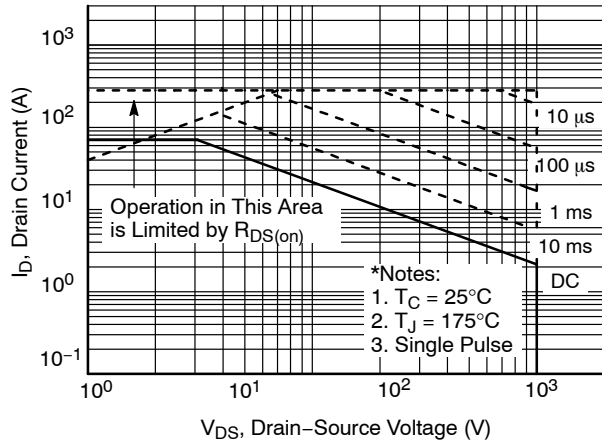


Figure 9. Maximum Safe Operating Area

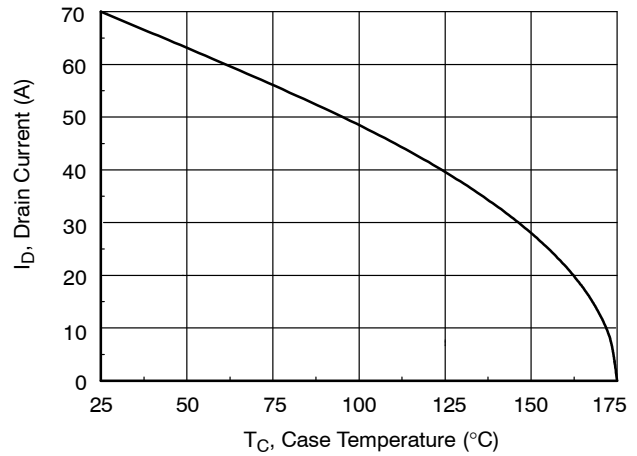


Figure 10. Maximum Drain Current vs. Case Temperature

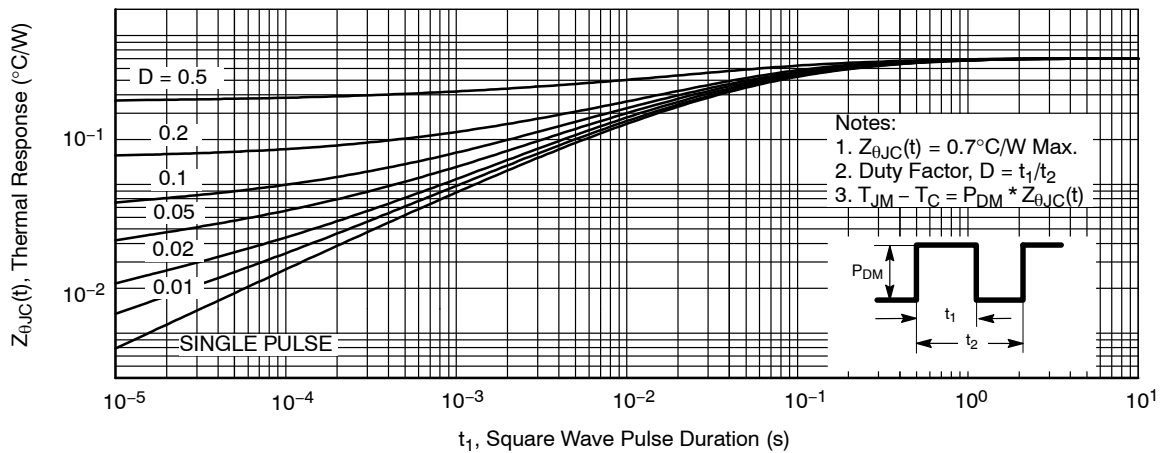


Figure 11. Transient Thermal Response Curve

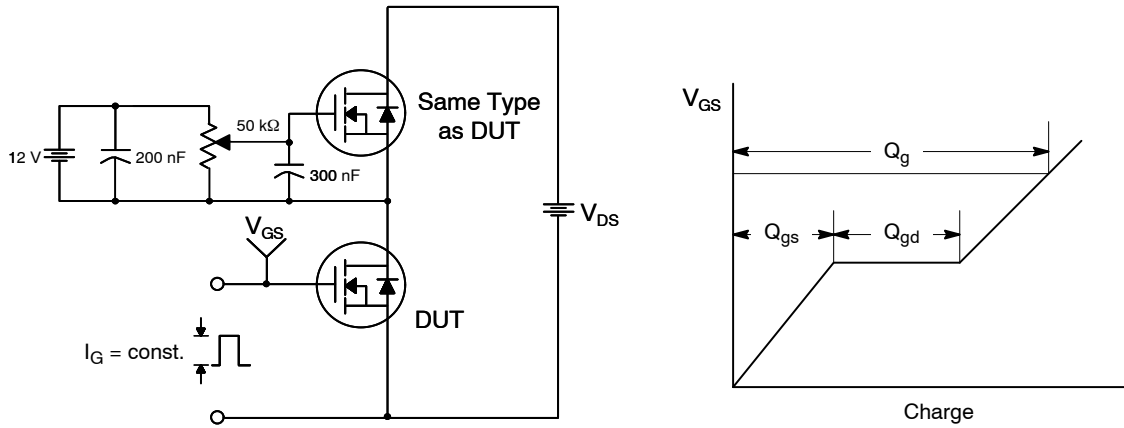


Figure 12. Gate Charge Test Circuit & Waveform

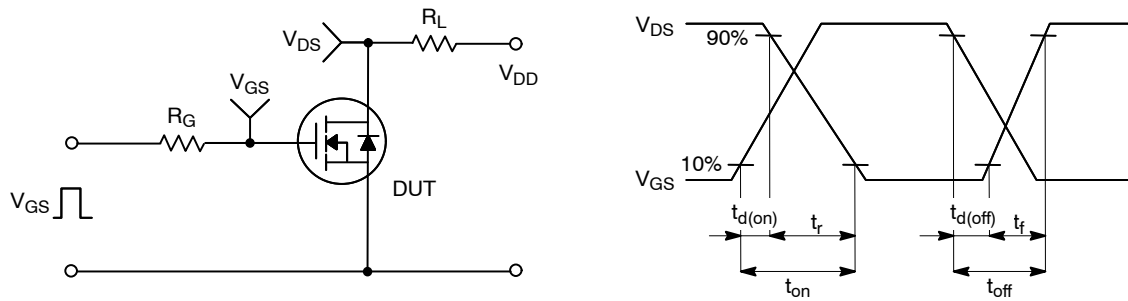


Figure 13. Resistive Switching Test Circuit & Waveforms

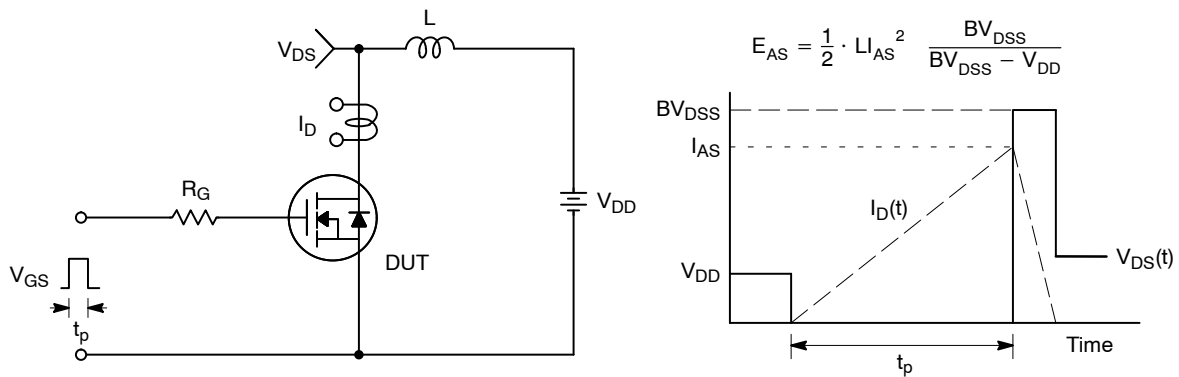
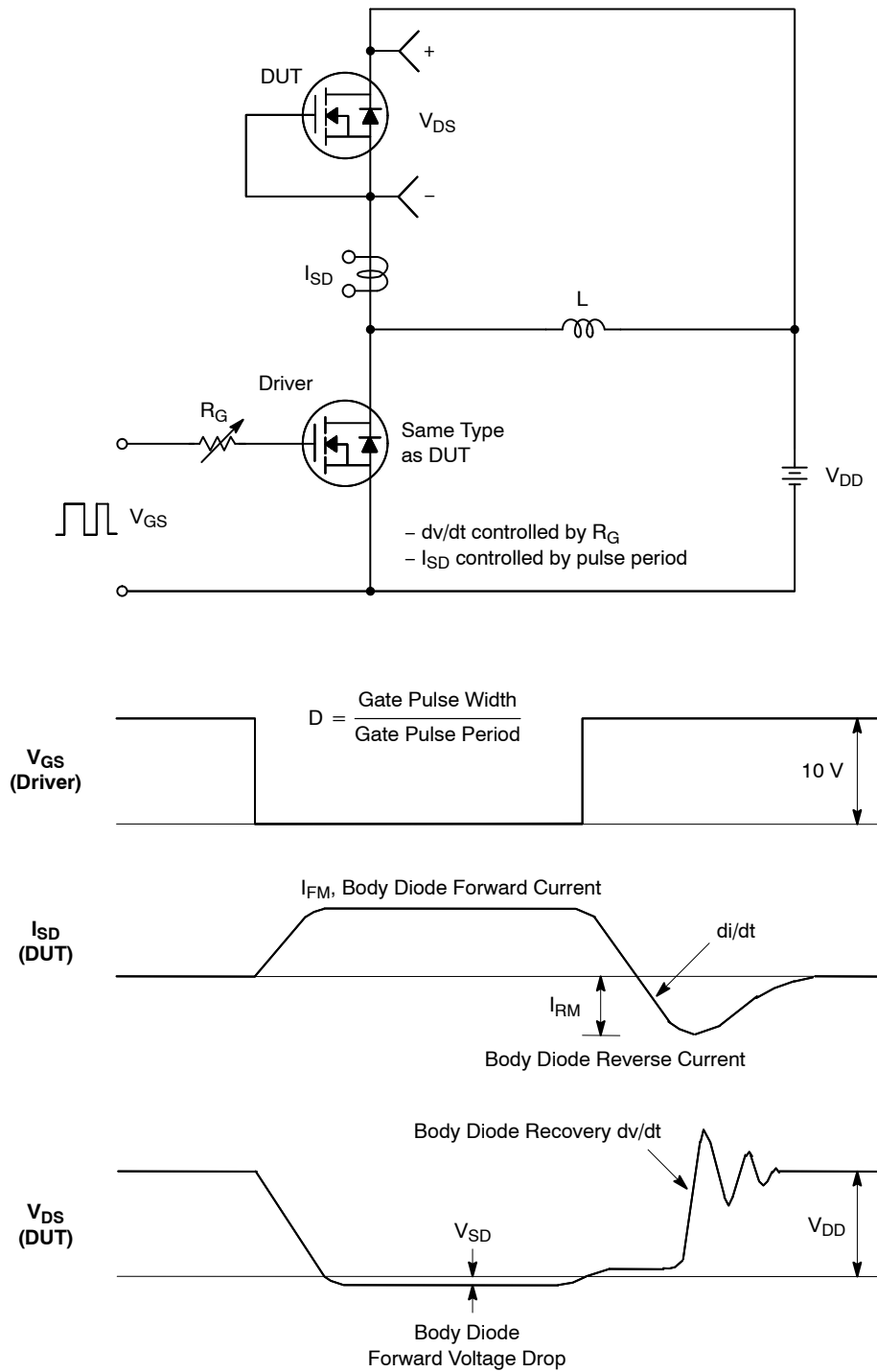


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

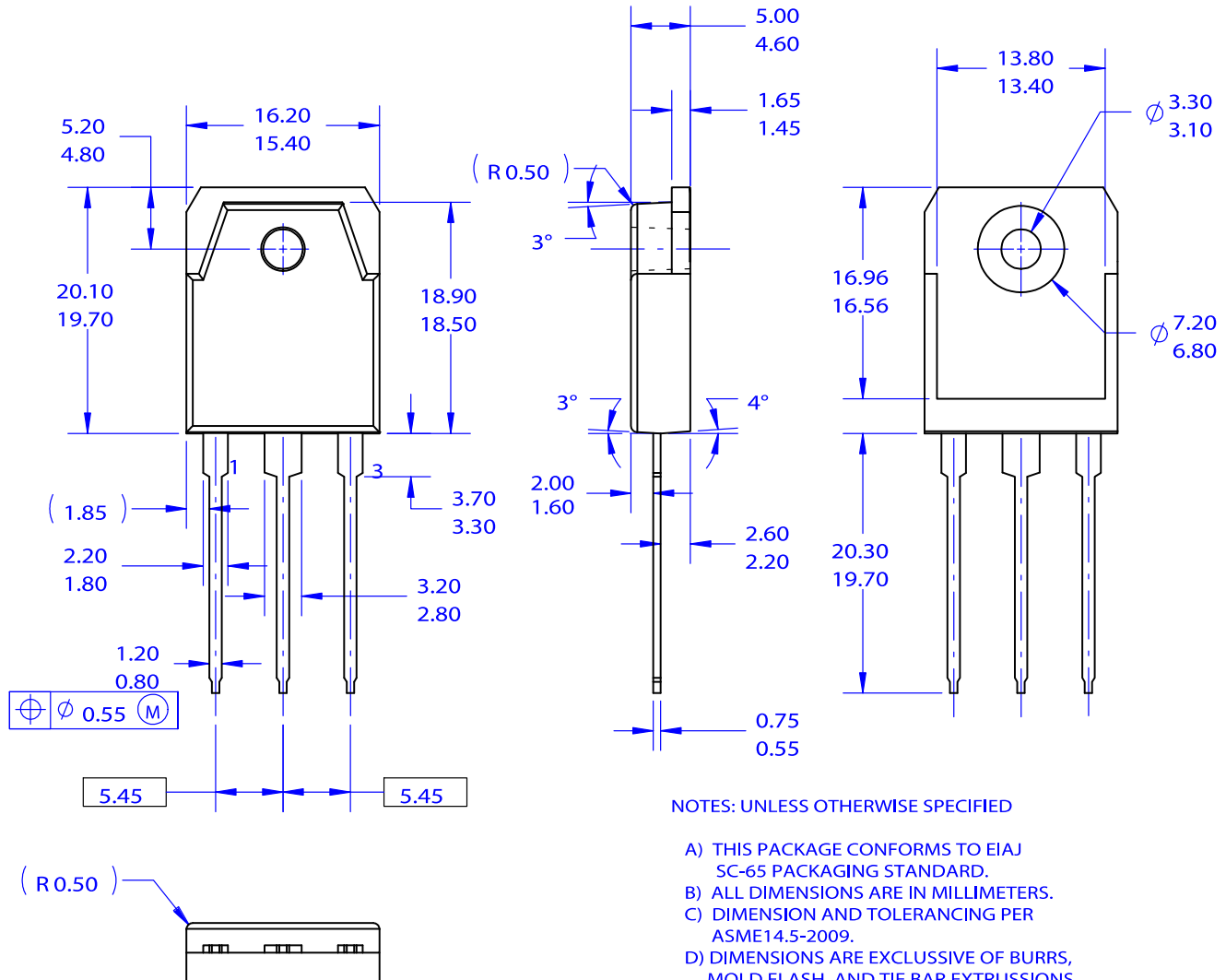
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**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

TO-3P-3LD / EIAJ SC-65, ISOLATED  
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DATE 31 OCT 2016



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