

MOSFET

OptiMOS™ 6 Power-Transistor, 40 V

Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- Optimized design for double side cooling
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

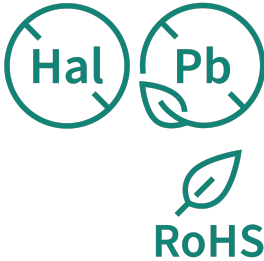
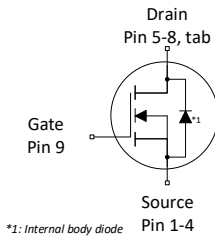
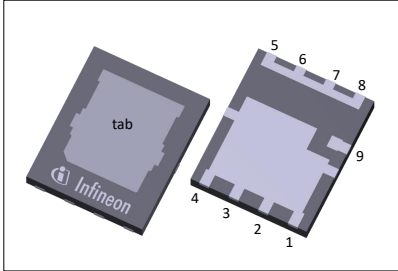
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS}$	40	V
$R_{DS(on),max}$	0.49	mΩ
$I_D$	597	A
$Q_{oss}$	142	nC
$Q_G$	130	nC

PG-WHTFN-9



Type / Ordering code	Package	Marking	Related links
IQD005N04NM6CGSC	PG-WHTFN-9	NA	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	597 422 402 57	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{THJA}=50\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	2388	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	1115	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	333 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	0.45	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	0.56	°C/W	
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50	°C/W	

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.8	2.3	2.8	V	$V_{DS}=V_{GS}$ , $I_D=1449\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.42 0.48	0.49 0.54	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=50\text{ A}$
Gate resistance	$R_G$	-	0.68	-	$\Omega$	-
Transconductance	$g_{fs}$	185	370	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance <sup>6)</sup>	$C_{iss}$	-	9000	12000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>6)</sup>	$C_{oss}$	-	2900	3800	pF	
Reverse transfer capacitance <sup>6)</sup>	$C_{rss}$	-	69	120	pF	
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	6	-	ns	
Turn-off delay time	$t_{d(off)}$	-	42	-	ns	
Fall time	$t_f$	-	9	-	ns	

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>7)</sup>

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	30	-	nC	$V_{DD}=20\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	21	-	nC	
Gate to drain charge <sup>8)</sup>	$Q_{gd}$	-	18	26	nC	
Switching charge	$Q_{sw}$	-	27	-	nC	
Gate charge total <sup>8)</sup>	$Q_g$	-	130	163	nC	
Gate plateau voltage	$V_{plateau}$	-	3.3	-	V	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	122	-	nC	
Output charge <sup>8)</sup>	$Q_{oss}$	-	142	189	nC	

<sup>7)</sup> See "Gate charge waveforms" for parameter definition

<sup>8)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	294	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	2388	A	
Diode forward voltage	$V_{SD}$	-	0.78	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=50\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	58	116	ns	$V_R=20\text{ V}$ , $I_F=25\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	79	158	nC	
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	29	58	ns	$V_R=20\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	221	442	nC	

<sup>9)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

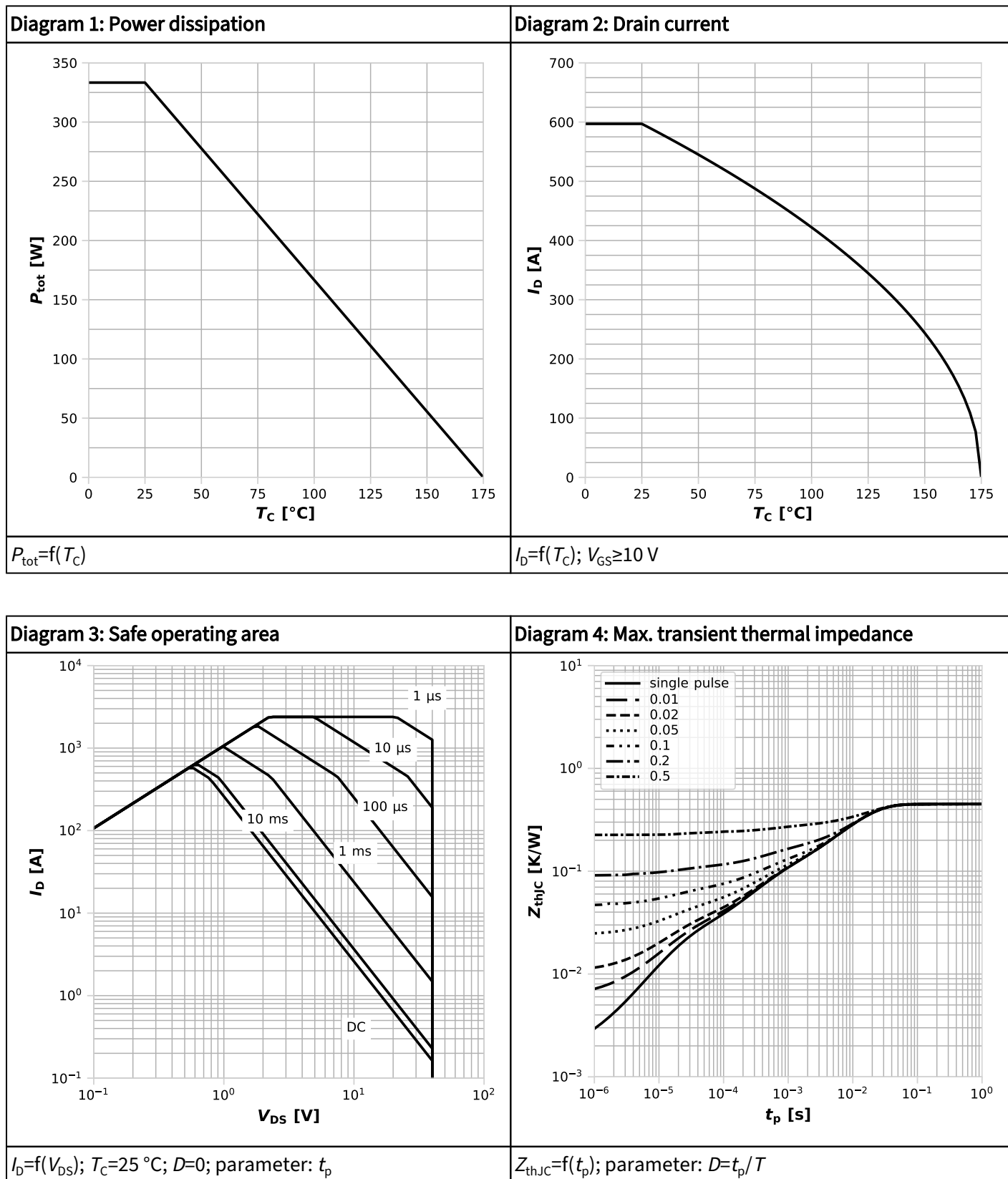
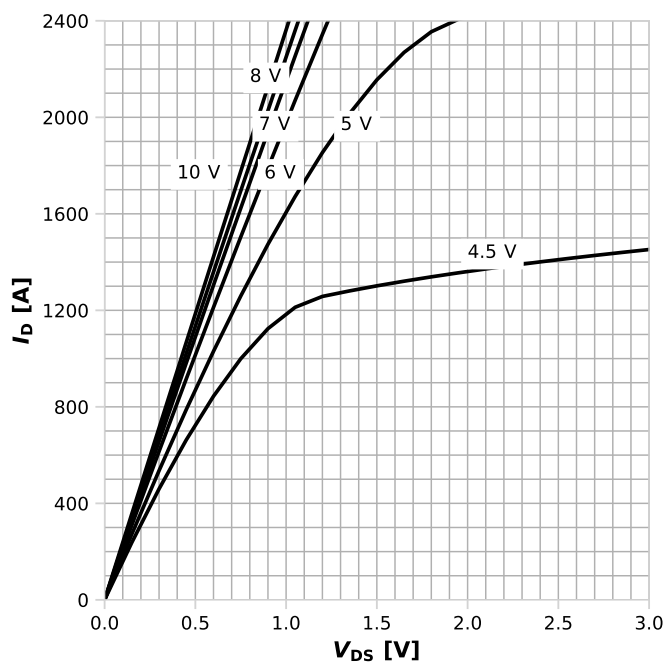
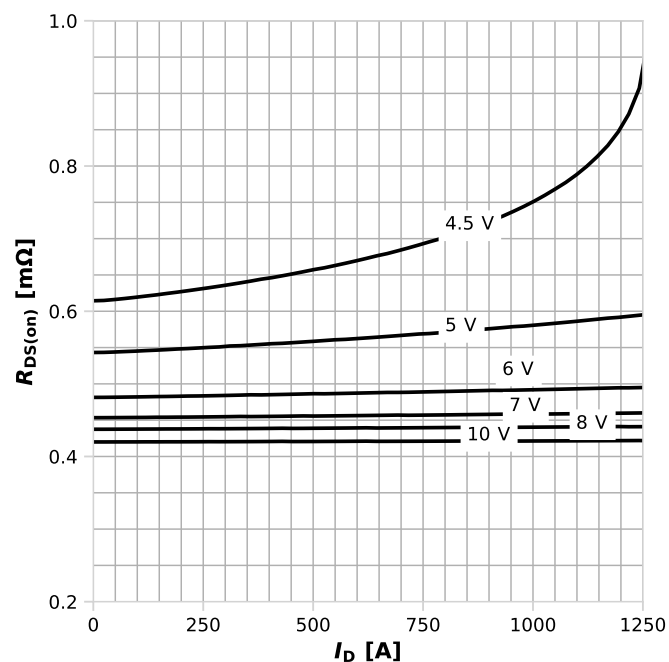


Diagram 5: Typ. output characteristics



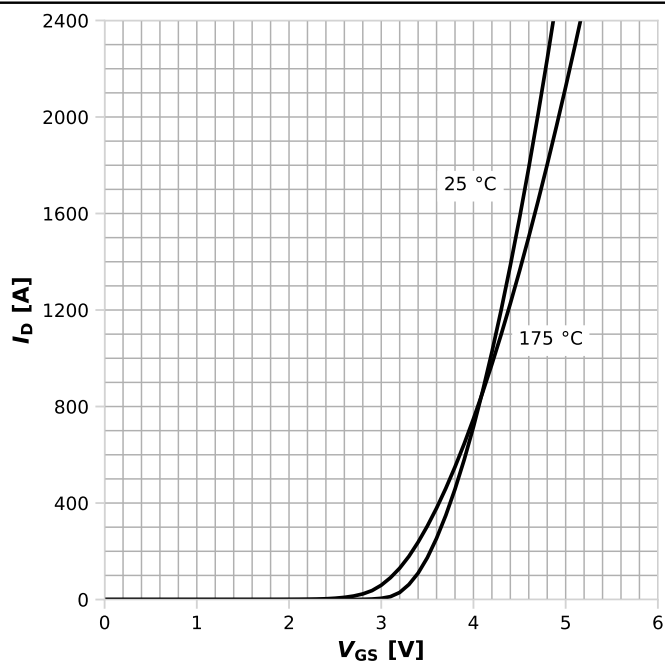
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



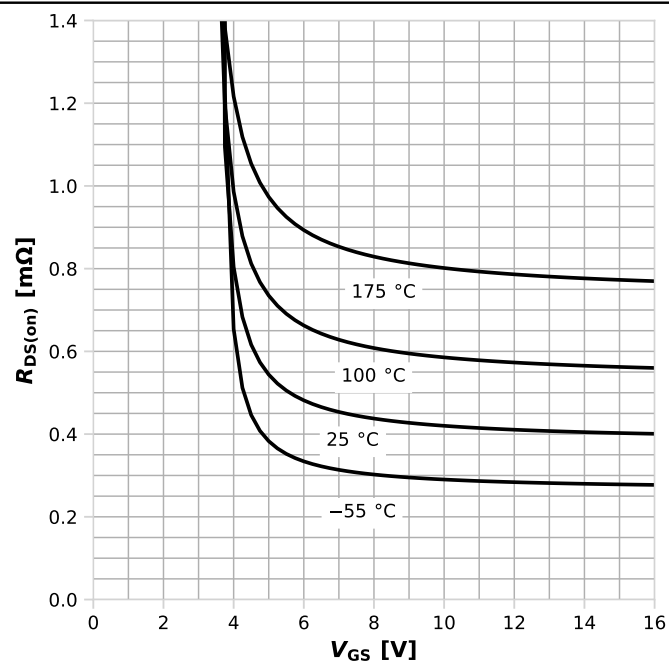
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



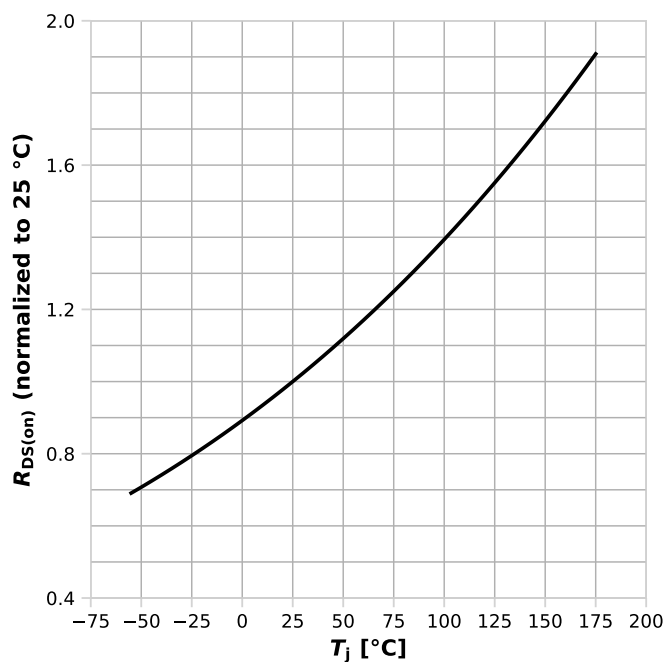
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)\max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



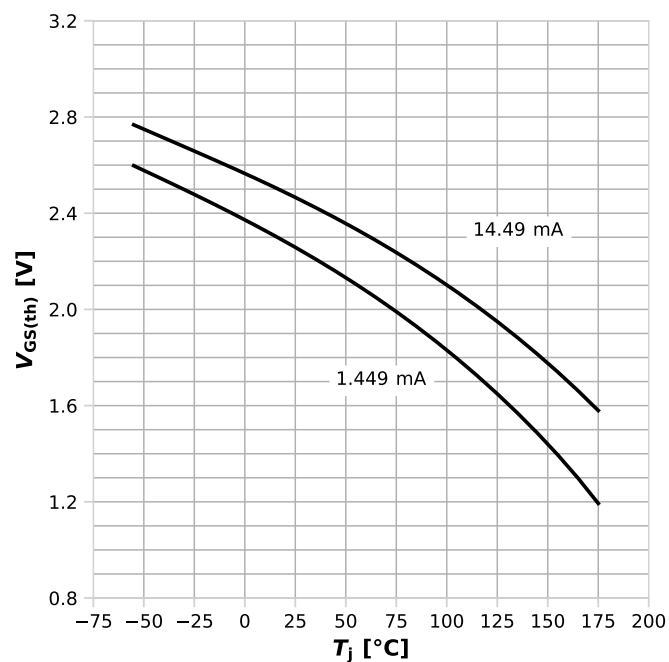
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 50\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



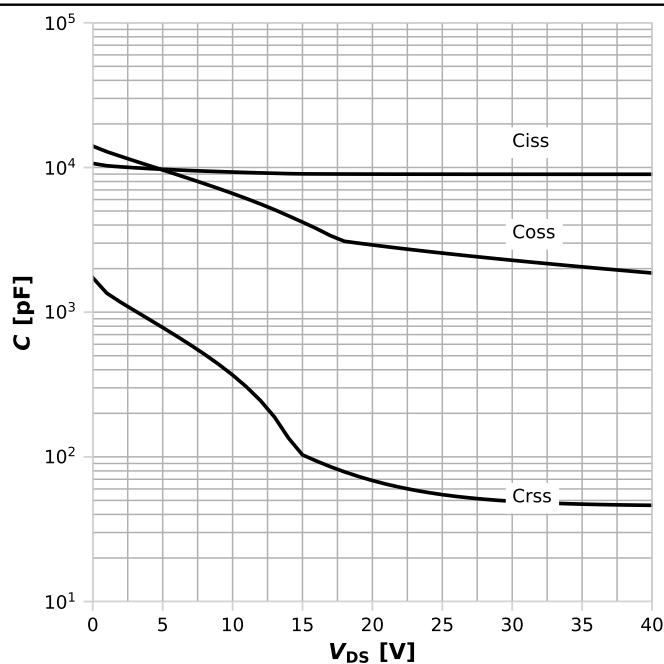
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



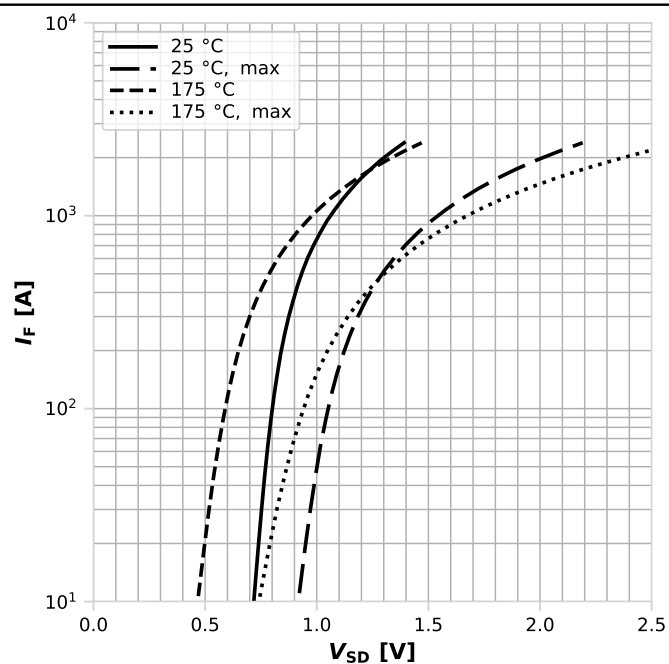
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

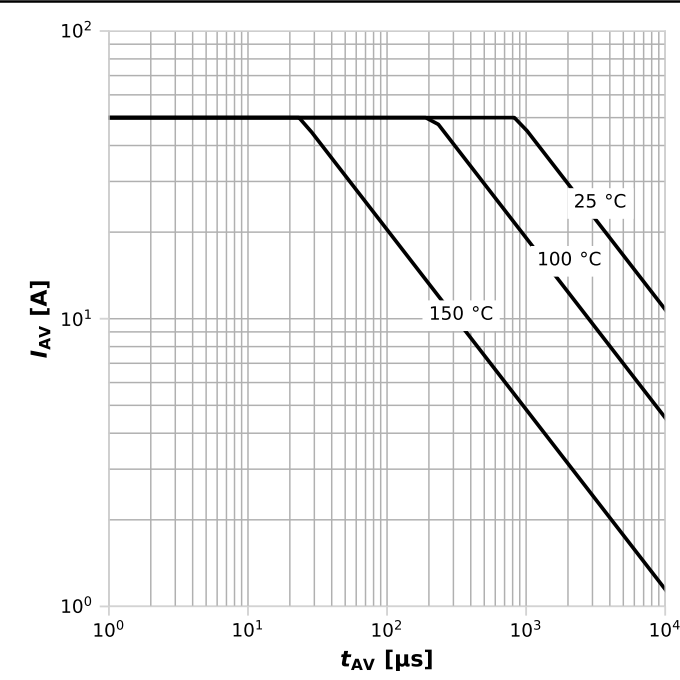
Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

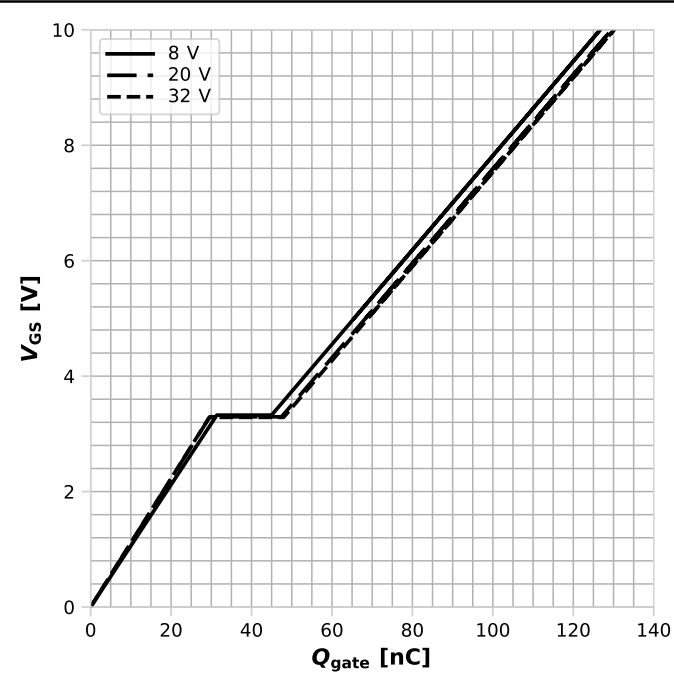


Diagram 13: Avalanche characteristics



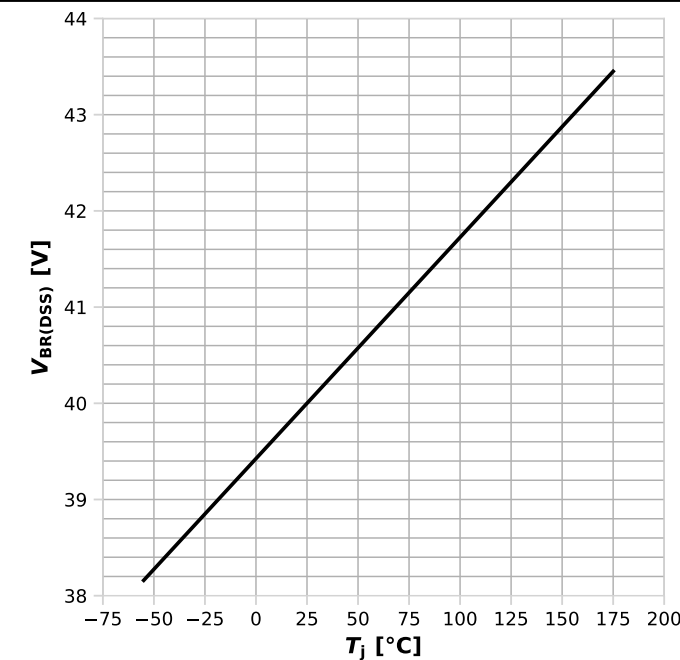
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



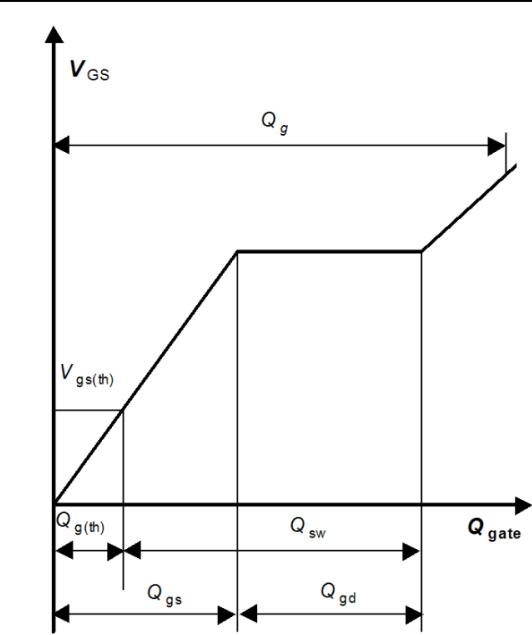
$V_{GS}=f(Q_{gate})$ ,  $I_D=50\text{ A}$  pulsed,  $T_j=25\text{ }^{\circ}\text{C}$ ; parameter:  $V_{DD}$

Diagram 15: Min. drain-source breakdown voltage

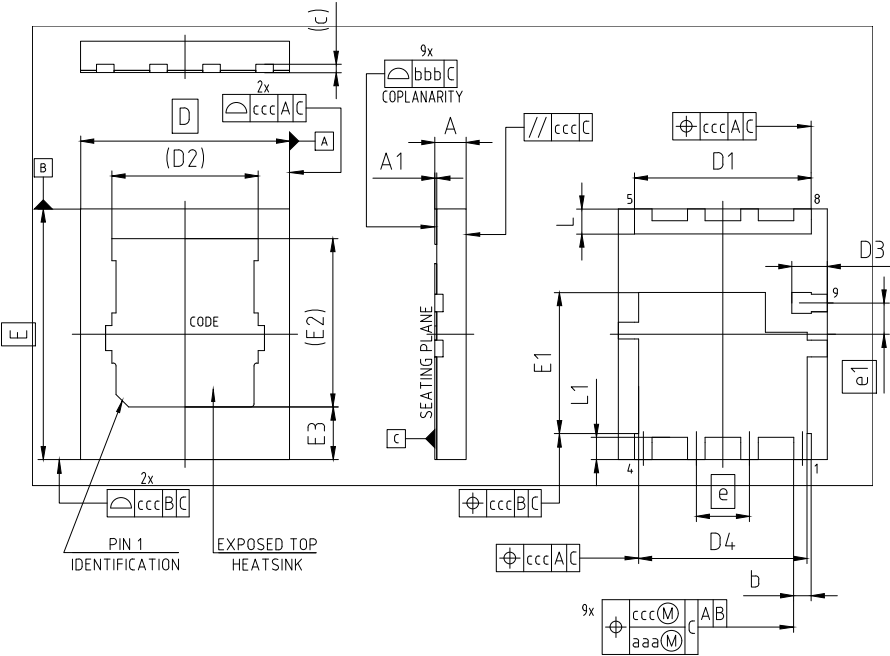


$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

Gate charge waveforms



5 Package outlines



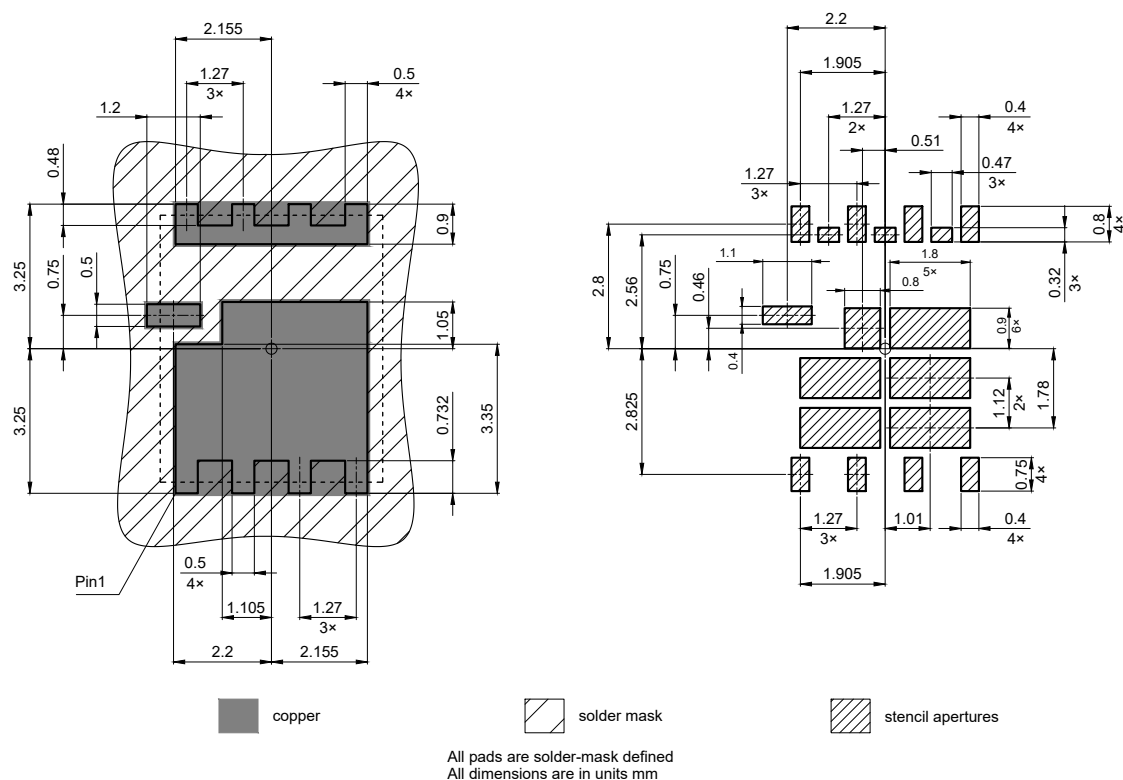
PACKAGE - GROUP  
NUMBER:

PG-WHTFN-9-U02

DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	e1	0.75	
b	0.32	0.52	L	0.50	0.70
c	0.20		L1	0.44	0.64
D	5.00		aaa	0.05	
D1	4.13	4.33	bbb	0.08	
D2	3.50		ccc	0.10	
D3	0.75	0.95			
D4	3.93	4.13			
E	6.00				
E1	3.28	3.48			
E2	4.03				
E3	1.16	1.36			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WHTFN-9, dimensions in mm



**Figure 2** Footprint drawing PG-WHTFN-9, dimensions in mm

## Revision history

IQD005N04NM6CGSC

### Revision 2024-10-16, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-06-13	Release of final
2.1	2024-07-16	Updated max Rdson
2.2	2024-10-16	Update package drawing and diagram circuit

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