

Automotive MOSFET

OptiMOS™ 6 Power-Transistor



Features

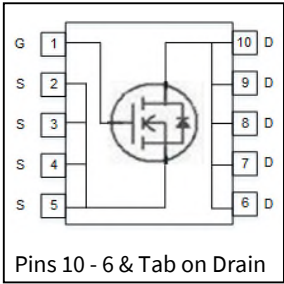
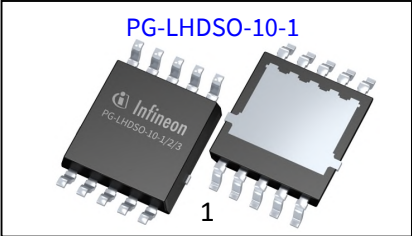
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- Top Side Cooling

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

$V_{DS}$	40	V
$R_{DS(on)}$	1.73	mΩ
$I_D$ (chip limited)	200	A

Type	Package	Marking
IAUCN04S6N017T	PG-LHDSO-10-1	6D4



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>	200	A
		$V_{GS}=10\text{V}$ , DC current <sup>1)</sup>	120	
		$T_a=85\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJH}$ on 2s2p <sup>2,4)</sup>	58	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	520	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=40\text{ A}$	130	mJ
Avalanche current, single pulse	$I_{AS}$	–	40	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	103	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	°C

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	—	—	0.73	1.46	K/W
Thermal characterization parameter, source pin <sup>5)</sup>	$\psi_{source}$		—	5.4	—	
Thermal characterization parameter, drain pin <sup>6)</sup>	$\psi_{drain}$		—	5.3	—	
Thermal resistance, junction - heatsink <sup>4)</sup>	$R_{thJH}$		—	7.5	—	
Thermal resistance, junction - ambient <sup>3)</sup>	$R_{thJA}$	—	—	49	—	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	40	—	—	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=40\text{ }\mu\text{A}$	2.2	2.6	3.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	—	—	1	$\mu\text{A}$
		$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}^{2)}$	—	—	14	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	—	—	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$ , $I_D=60\text{ A}$	—	1.78	2.05	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$	—	1.52	1.73	
Gate resistance <sup>2)</sup>	$R_G$	—	—	2.5	—	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	–	2500	3250	pF
Output capacitance	$C_{oss}$		–	750	975	
Reverse transfer capacitance	$C_{rss}$		–	42	63	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=120\text{ A}, R_G=3.5\ \Omega$	–	7	–	ns
Rise time	$t_r$		–	4	–	
Turn-off delay time	$t_{d(off)}$		–	15	–	
Fall time	$t_f$		–	7	–	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=32\text{ V}, I_D=120\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	–	11	14	nC
Gate to drain charge	$Q_{gd}$		–	8	12	
Gate charge total	$Q_g$		–	38	49	
Gate plateau voltage	$V_{plateau}$		–	4.3	–	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	–	–	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	–	–	520	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=60\text{ A}, T_J=25\text{ °C}$	–	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=20\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	–	24	–	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		–	8	–	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7) without thermal vias, heatsink of 71x110x2 mm is attached through 3 W/(m²K) 400µm to top side pad. Heatsink fixed to 85°C ambient temperature.

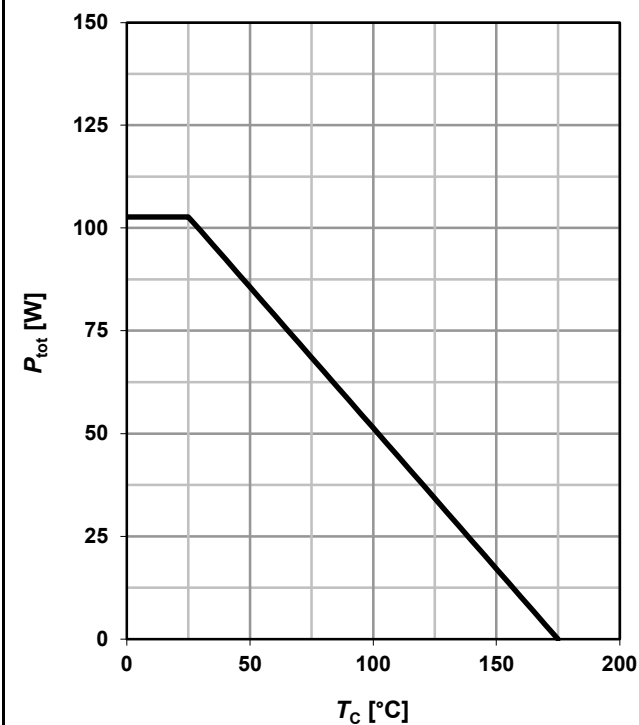
<sup>5)</sup> Thermal characterization parameter, calculated as  $\psi_{source} = (T_{source} - T_{ambient})/P_{dis}$  in condition of 4). Used to determine PCB temperature at source pins for given power.

<sup>6)</sup> Thermal characterization parameter, calculated as  $\psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$  in condition of 4). Used to determine PCB temperature at drain pins for given power.

## Electrical characteristics diagrams

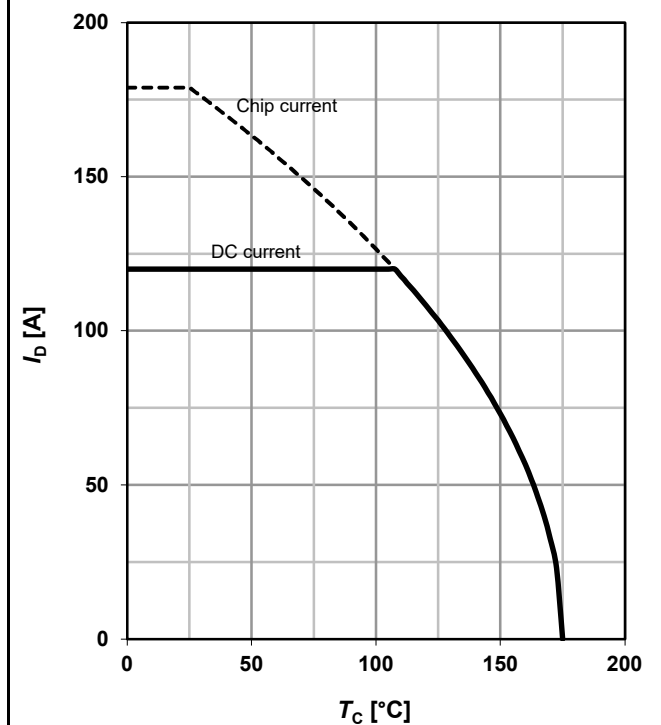
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



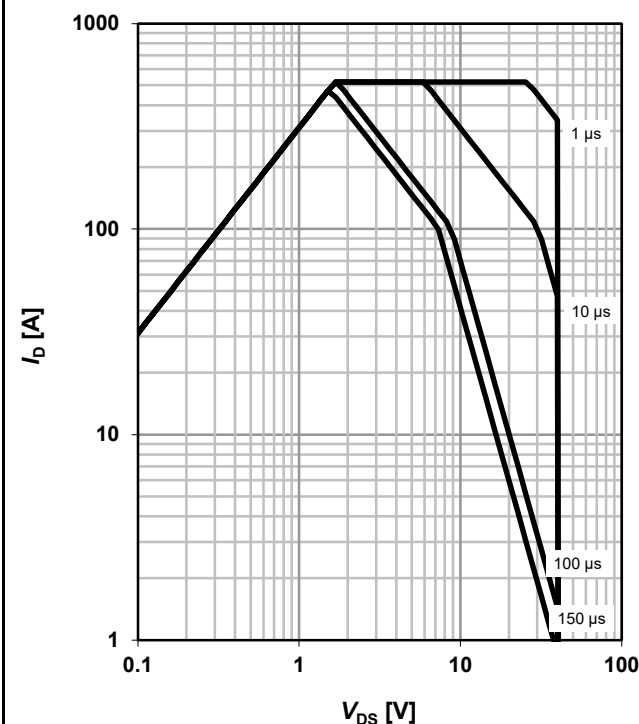
### 2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



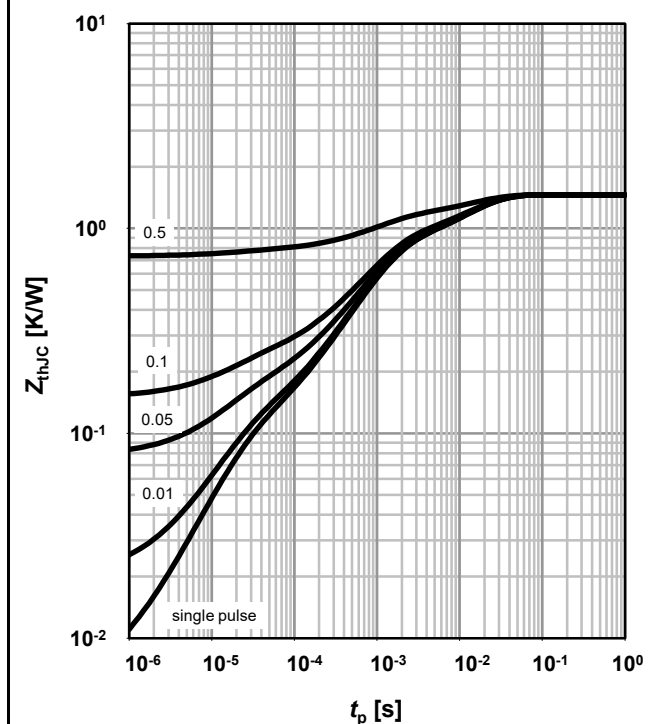
### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{ parameter: } t_p$$



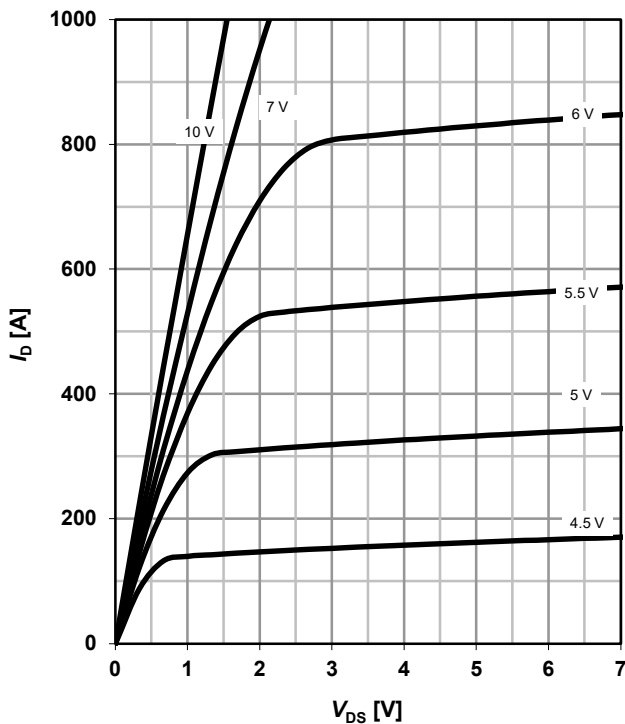
### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{ parameter: } D = t_p/T$$



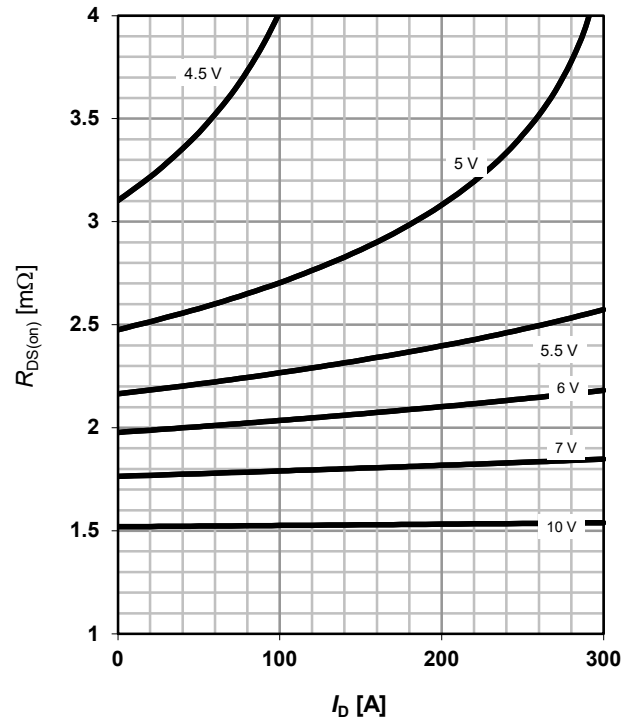
## 5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



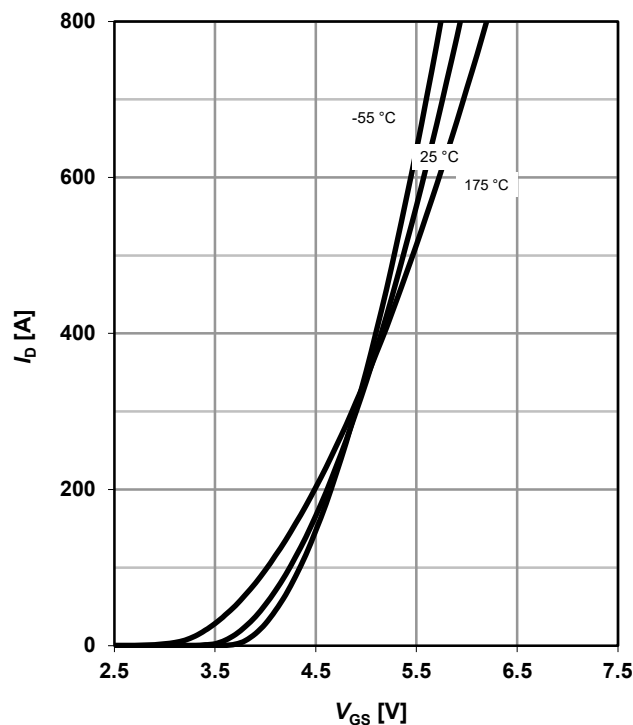
## 6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



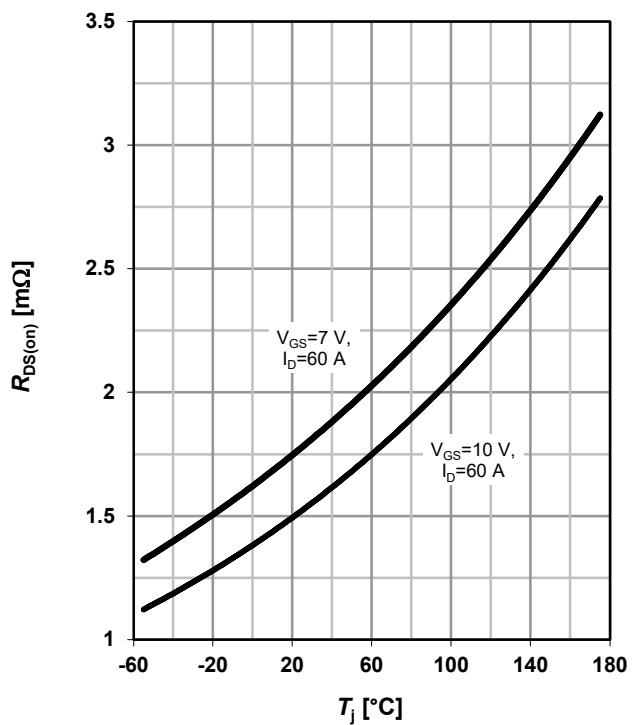
## 7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$



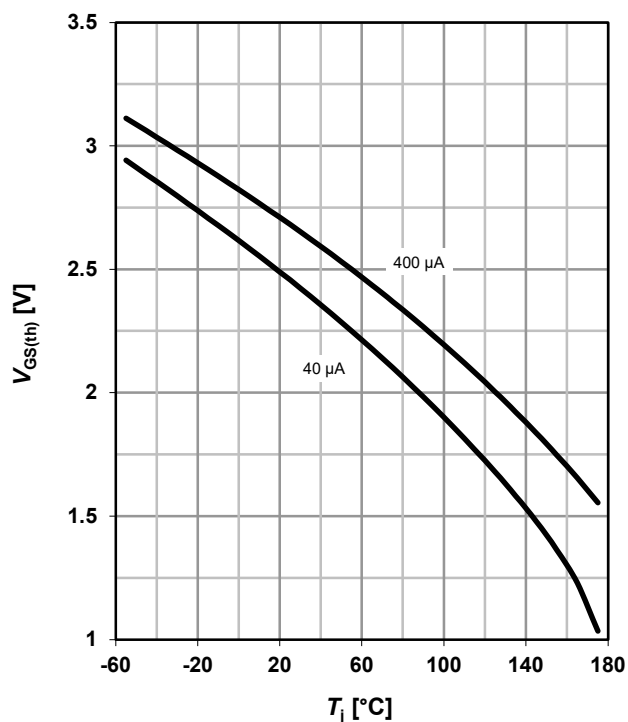
## 8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



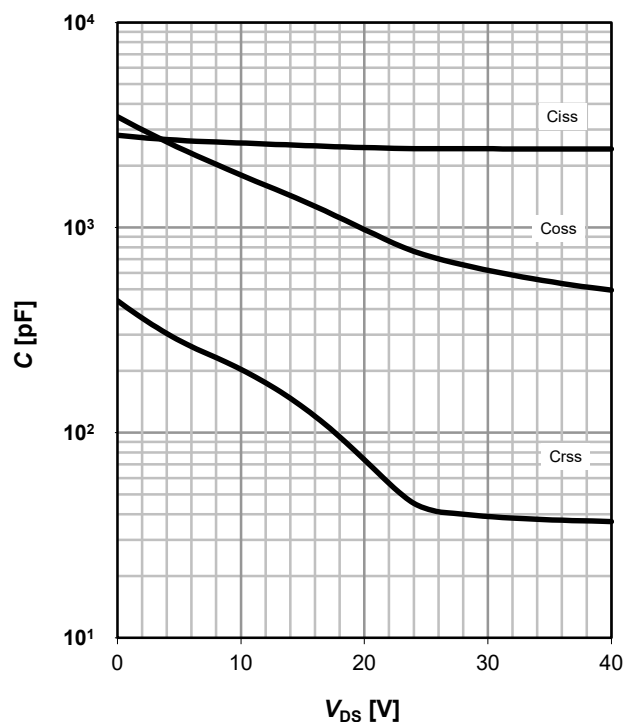
## 9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$



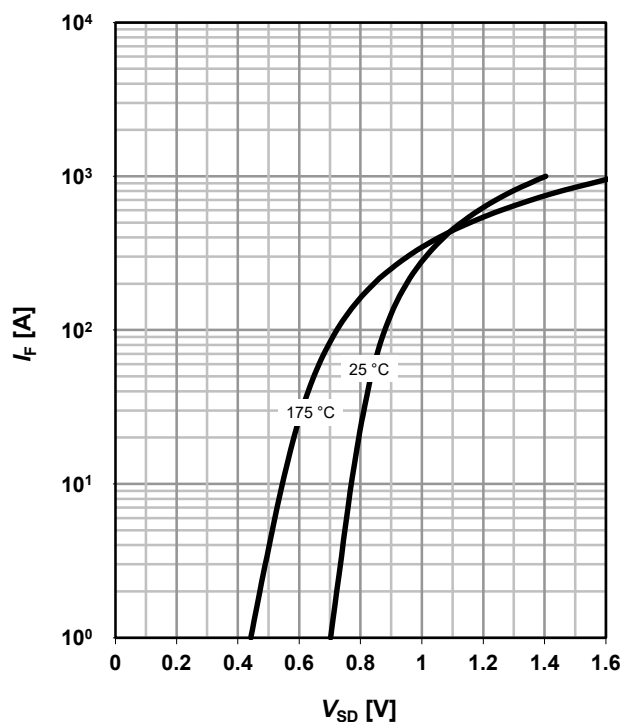
## 10 Typ. capacitances

$C = f(V_{DS})$ ;  $V_{GS} = 0 V$ ;  $f = 1 MHz$



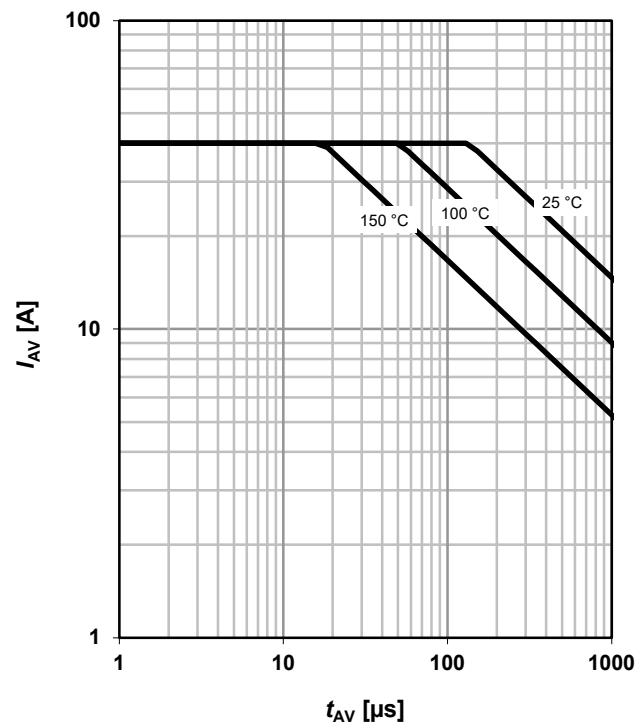
## 11 Typical forward diode characteristics

$I_F = f(V_{SD})$ ; parameter:  $T_j$



## 12 Typ. avalanche characteristics

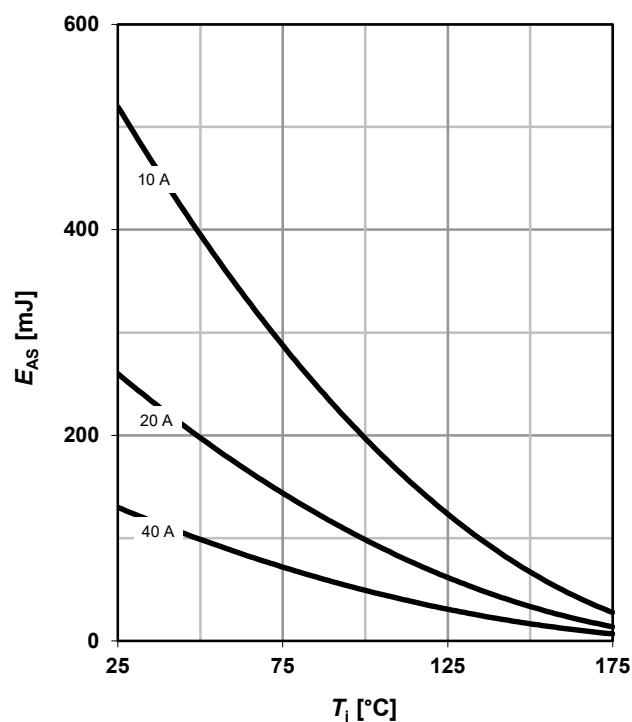
$I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$





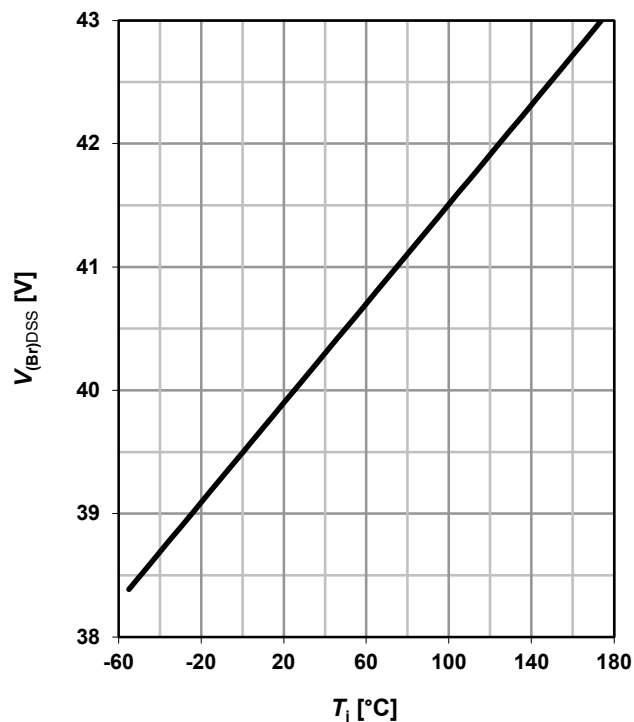
## 13 Typical avalanche energy

$E_{AS} = f(T_j)$ ; parameter:  $I_D$



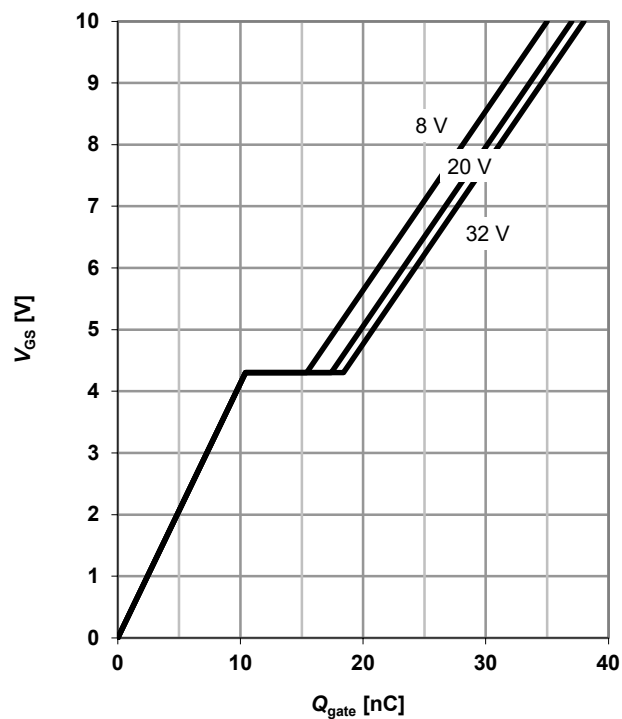
## 14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$ ;  $I_{D\_typ} = 1$  mA

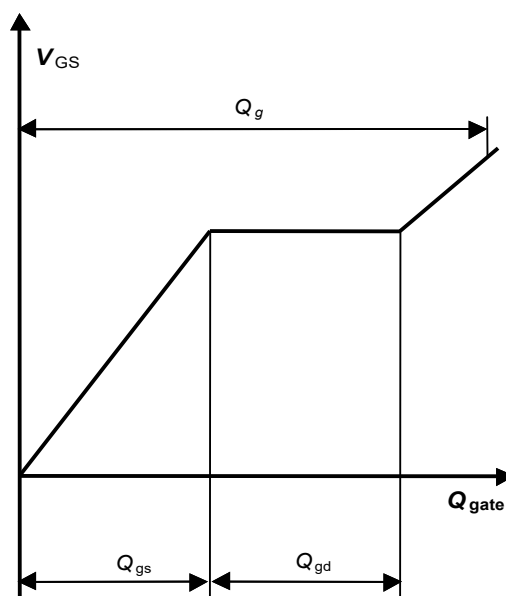


## 15 Typ. gate charge

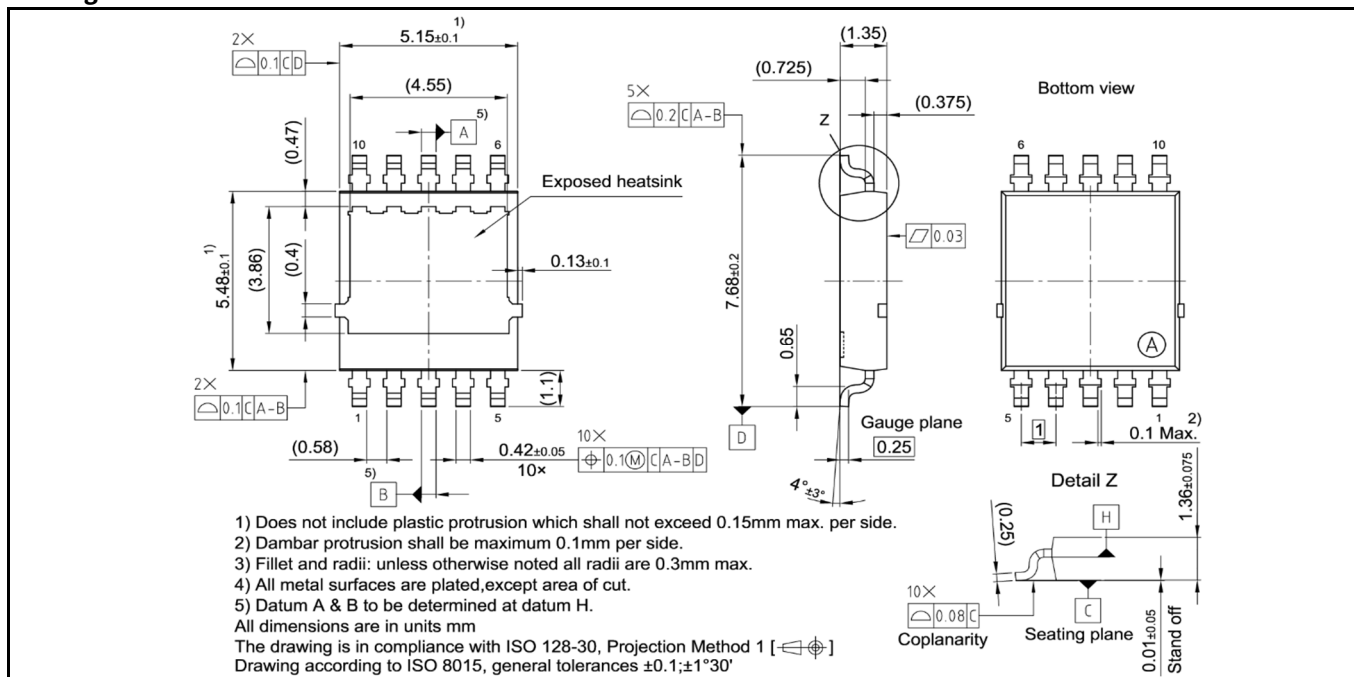
$V_{GS} = f(Q_{gate})$ ;  $I_D = 120$  A pulsed; parameter:  $V_{DD}$



## 16 Gate charge waveforms

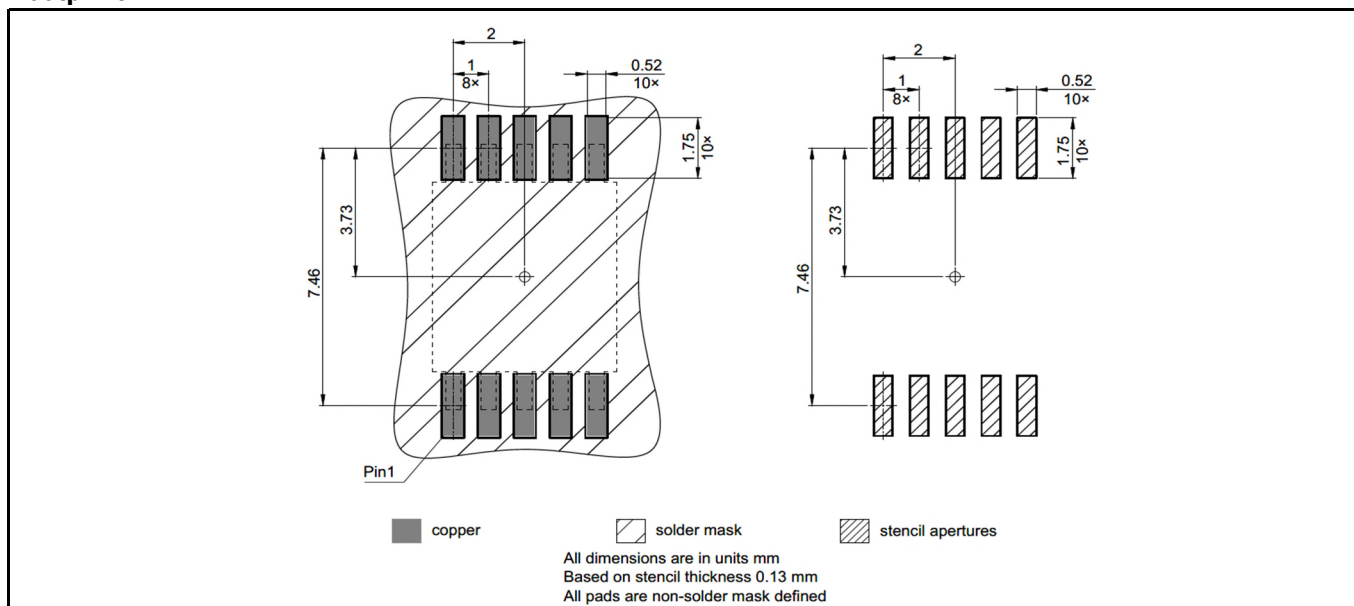


## Package Outline

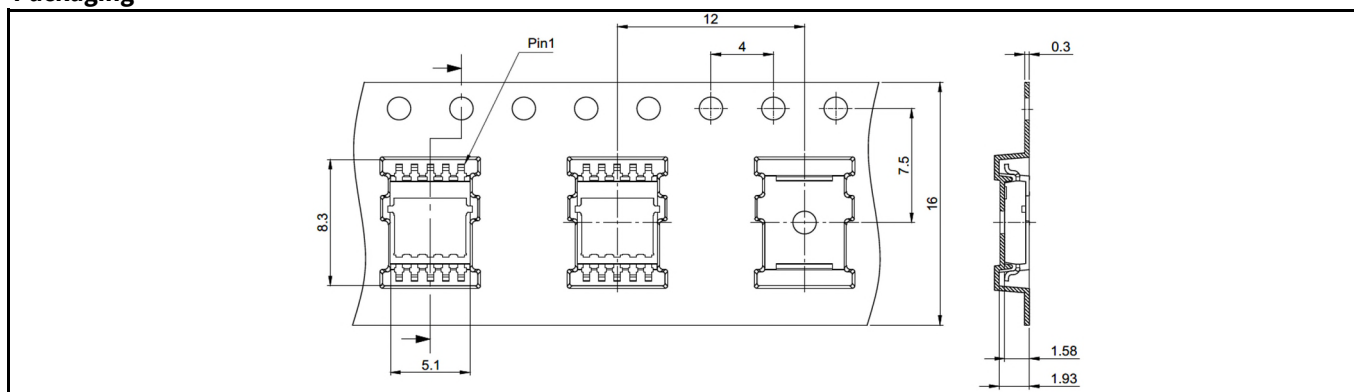


<https://www.infineon.com/cms/en/product/packages/PG-LHDSO/PG-LHDSO-10-1>

## Footprint



## Packaging



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all dimensions in mm



Revision History

Revision	Date	Changes
Revision 1.1	21.08.2023	Final Data Sheet
Revision 1.2	31.07.2024	updated package drawing with harmonized & standardized tolerance writing methodology

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