

## Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

## Applications

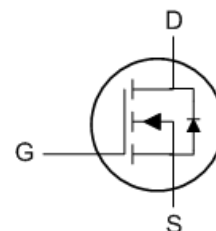
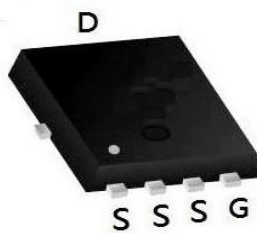
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

## Product Summary



BVDSS	RDSON	ID
85V	4.3mΩ	100A

## PDFN5060-8L Pin Configuration

Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	85	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	100	A
	$T_C = 100^\circ\text{C}$		63.3	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	400	A
Single Pulse Avalanche Energy <sup>2</sup>		EAS	273.8	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	107.8	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	60	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.16	$^\circ\text{C/W}$

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	85	-	-	V
Gate-body Leakage current		$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^{\circ}C$	$I_{DSS}$	$V_{DS} = 85V, V_{GS} = 0V$	-	-	1	$\mu A$
	$T_J=100^{\circ}C$			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
Drain-Source on-Resistance <sup>4</sup>		$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	4.3	5.6	m $\Omega$
Forward Transconductance <sup>4</sup>		$g_{fs}$	$V_{DS} = 5V, I_D = 20A$	-	57.8	-	S
Dynamic Characteristics <sup>5</sup>							
Input Capacitance		$C_{iss}$	$V_{DS} = 40V, V_{GS} = 0V, f = 1MHz$	-	4645	-	pF
Output Capacitance		$C_{oss}$		-	673	-	
Reverse Transfer Capacitance		$C_{rss}$		-	41	-	
Gate Resistance		$R_g$	f=1MHz	-	2.0	-	$\Omega$
Switching Characteristics <sup>5</sup>							
Total Gate Charge		$Q_g$	$V_{GS} = 10V, V_{DS} = 40V, I_D = 20A$	-	61.3	-	nC
Gate-Source Charge		$Q_{gs}$		-	21	-	
Gate-Drain Charge		$Q_{gd}$		-	11	-	
Turn-on Delay Time		$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 40V, R_G = 3\Omega, I_D = 20A$	-	16.5	-	ns
Rise Time		$t_r$		-	51.8	-	
Turn-off Delay Time		$t_{d(off)}$		-	37.1	-	
Fall Time		$t_f$		-	8.2	-	
Body Diode Reverse Recovery Time		$t_{rr}$	$I_F = 20A, di/dt = 100A/\mu S$	-	69	-	ns
Body Diode Reverse Recovery Charge		$Q_{rr}$		-	141	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage <sup>4</sup>		$V_{SD}$	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V
Continuous Source Current	$T_C=25^{\circ}C$	$I_S$	-	-	-	100	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature  $T_J(\text{MAX}) = 150^\circ\text{C}$
2. The EAS data shows Max. rating . The test condition is  $V_{DD} = 50V, V_{GS} = 10V, L = 0.4\text{mH}, I_{AS} = 37A$
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.

### Typical Characteristics

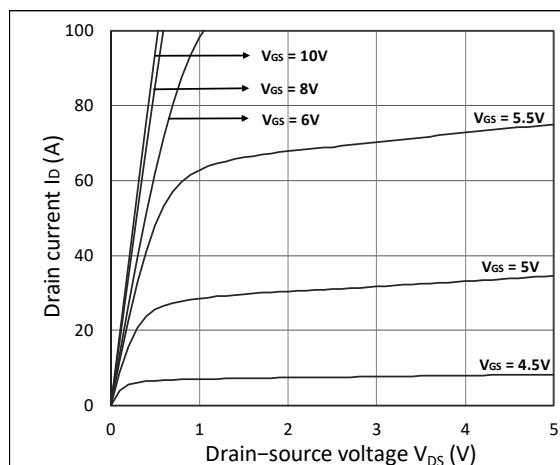


Figure 1. Output Characteristics

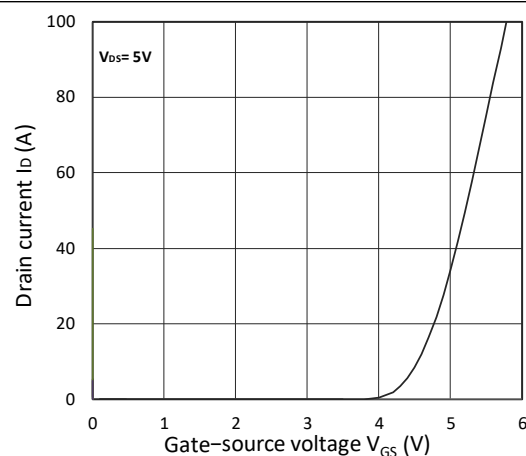


Figure 2. Transfer Characteristics

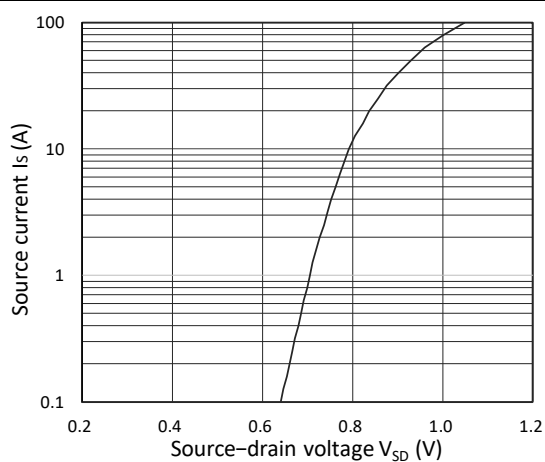


Figure 3. Forward Characteristics of Reverse

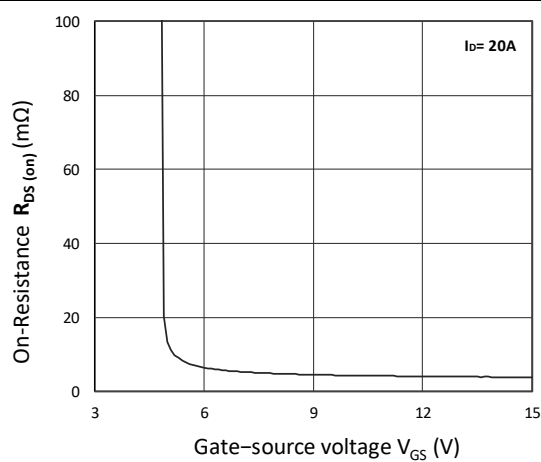


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

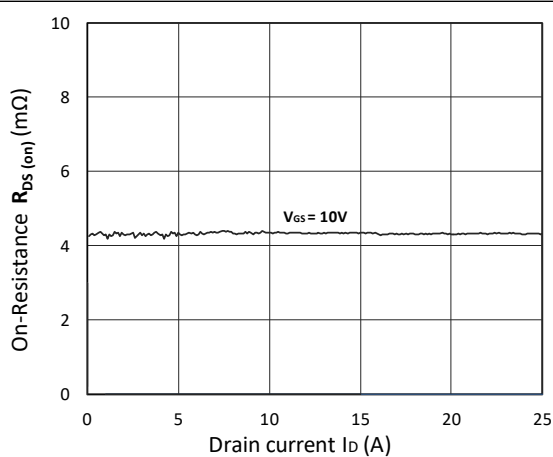


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

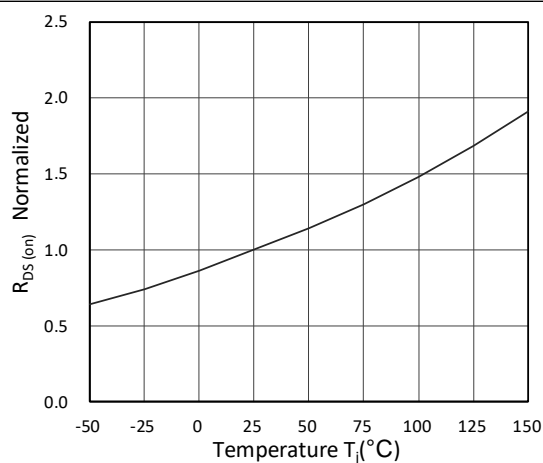


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

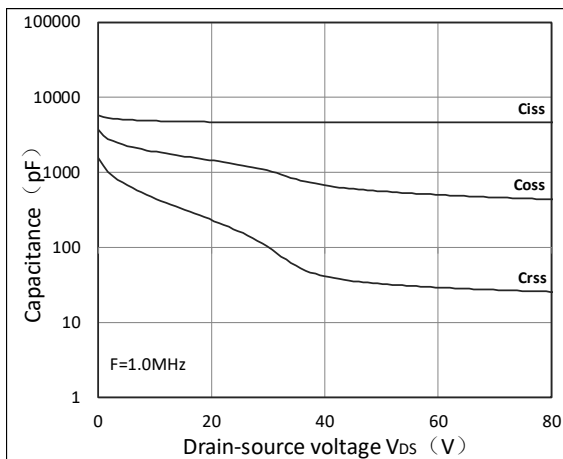


Figure 7. Capacitance Characteristics

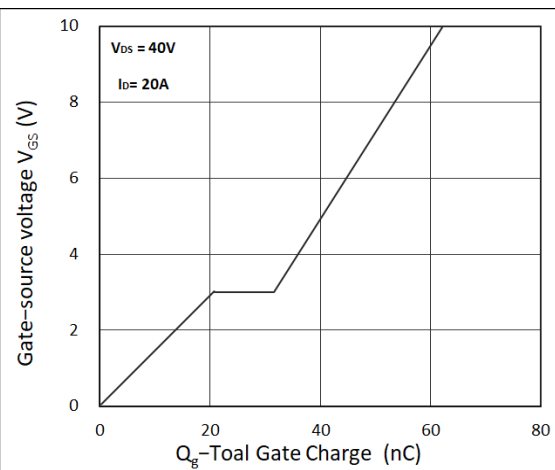


Figure 8. Gate Charge Characteristics

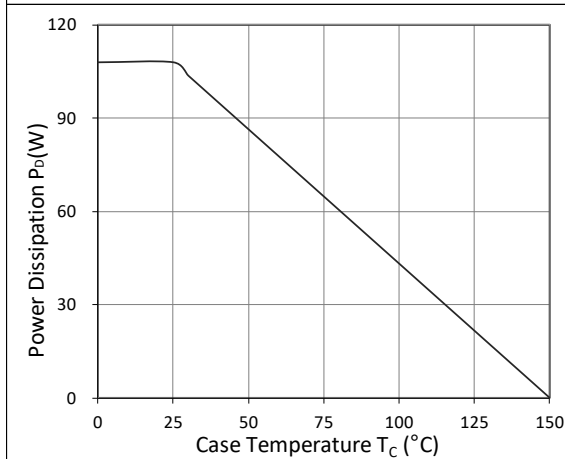


Figure 9. Power Dissipation

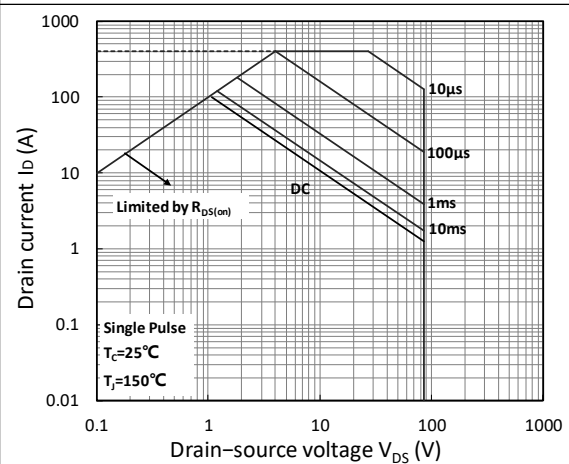


Figure 10. Safe Operating Area

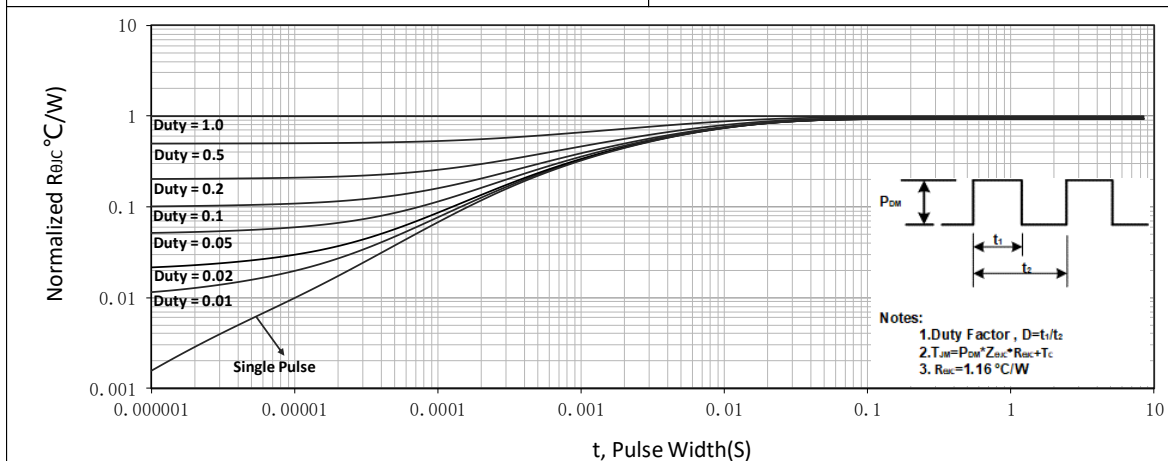
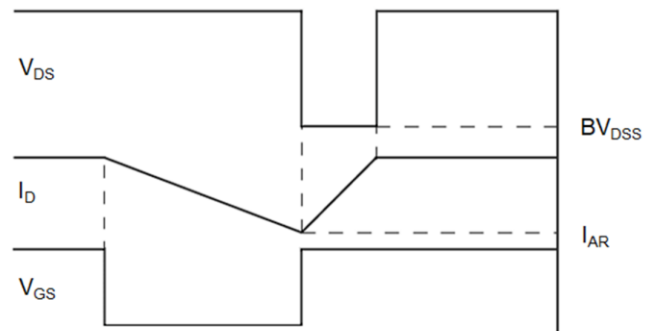
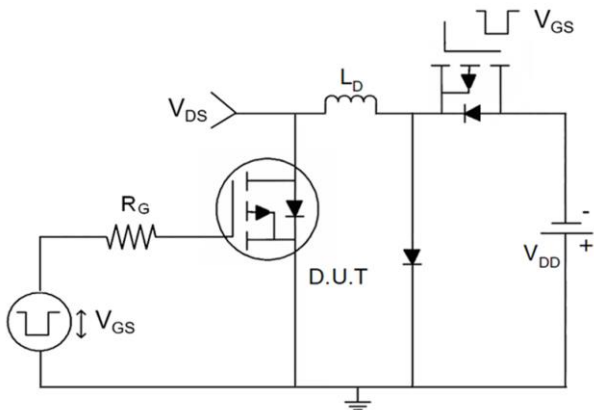
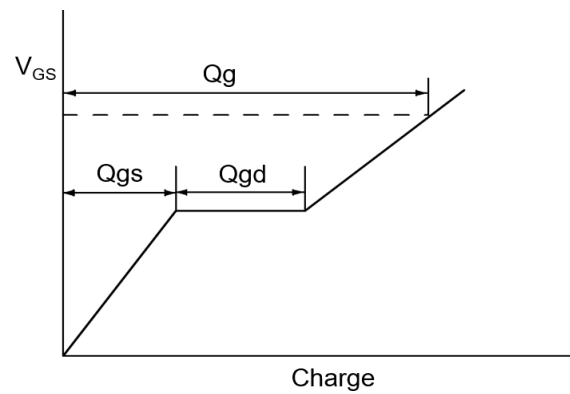
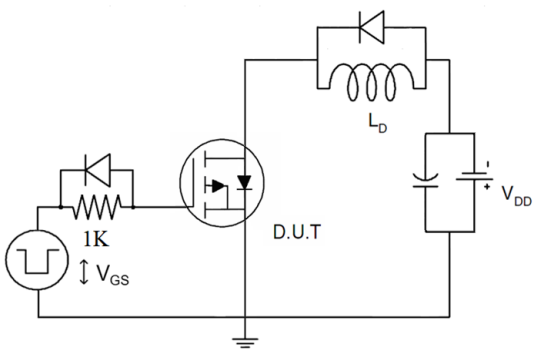


Figure 11. Normalized Maximum Transient Thermal Impedance

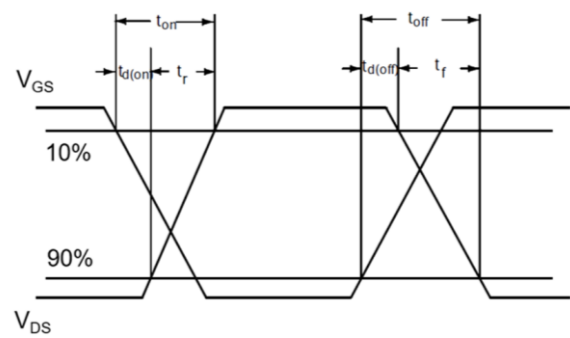
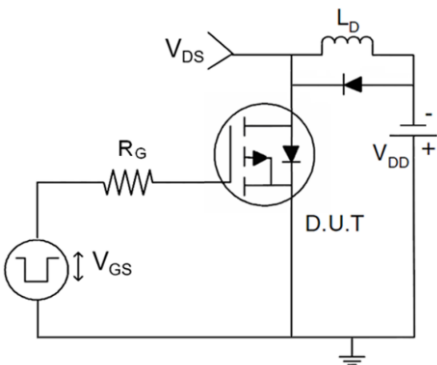
### 1) $E_{AS}$ Test Circuits



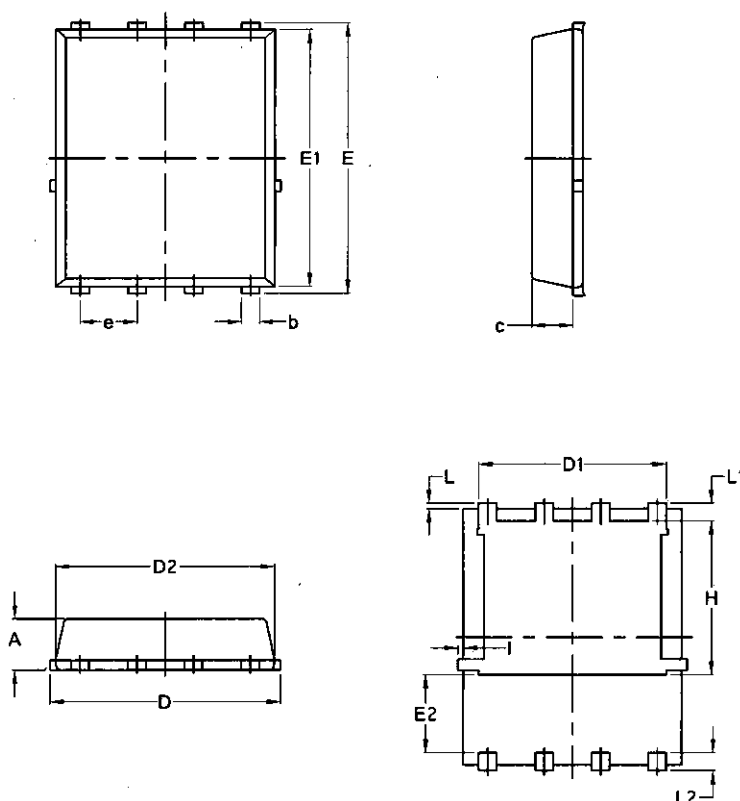
### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit



### Package Mechanical Data-PDFN5060-8L -Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070