

MOSFET  
OptiMOS™ 5 Linear FET 2, 100 V

Features

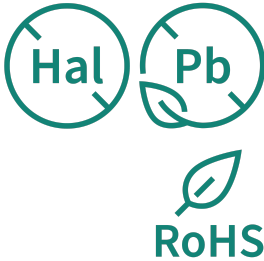
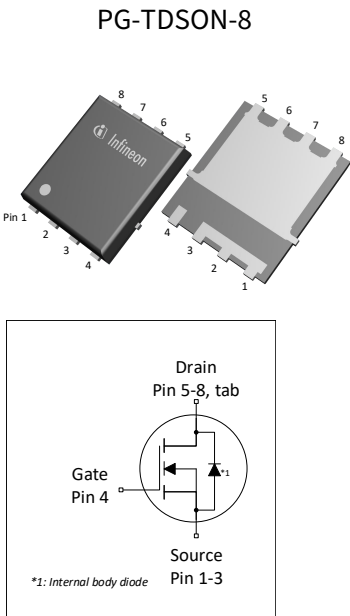
- Ideal for hot-swap, battery protection and e-fuse applications
- Very low on-resistance  $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}$	3.5	mΩ
$I_D$	164	A
$I(V_{DS}=50\text{ V}, t_p=10\text{ ms})$	7.4	A



Type / Ordering code	Package	Marking	Related links
ISC035N10NM5LF2	PG-TDSON-8	35N10LF2	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	164 116 19	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	656	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	398	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	217 3	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagrams 3 and 4 for more detailed information

<sup>4)</sup> See Diagram 14 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	0.7	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.9	V	$V_{DS}=V_{GS}$ , $I_D=115\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.0	3.5	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$
Gate resistance	$R_G$	-	1.5	2.3	$\Omega$	-
Transconductance <sup>6)</sup>	$g_{fs}$	26	52	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance <sup>7)</sup>	$C_{iss}$	-	5500	7200	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>7)</sup>	$C_{oss}$	-	780	1000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>7)</sup>	$C_{rss}$	-	19	33	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	11	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	10	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	35	-	nC	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	17	-	nC	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>9)</sup>	$Q_{gd}$	-	12	18	nC	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	30	-	nC	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>9)</sup>	$Q_g$	-	70	88	nC	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	$V_{DD}=50\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>9)</sup>	$Q_{oss}$	-	90	115	nC	$V_{DS}=50\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	159	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	656	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.84	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=50\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	49	98	ns	$V_R=50\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	72	144	nC	$V_R=50\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>10)</sup> Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

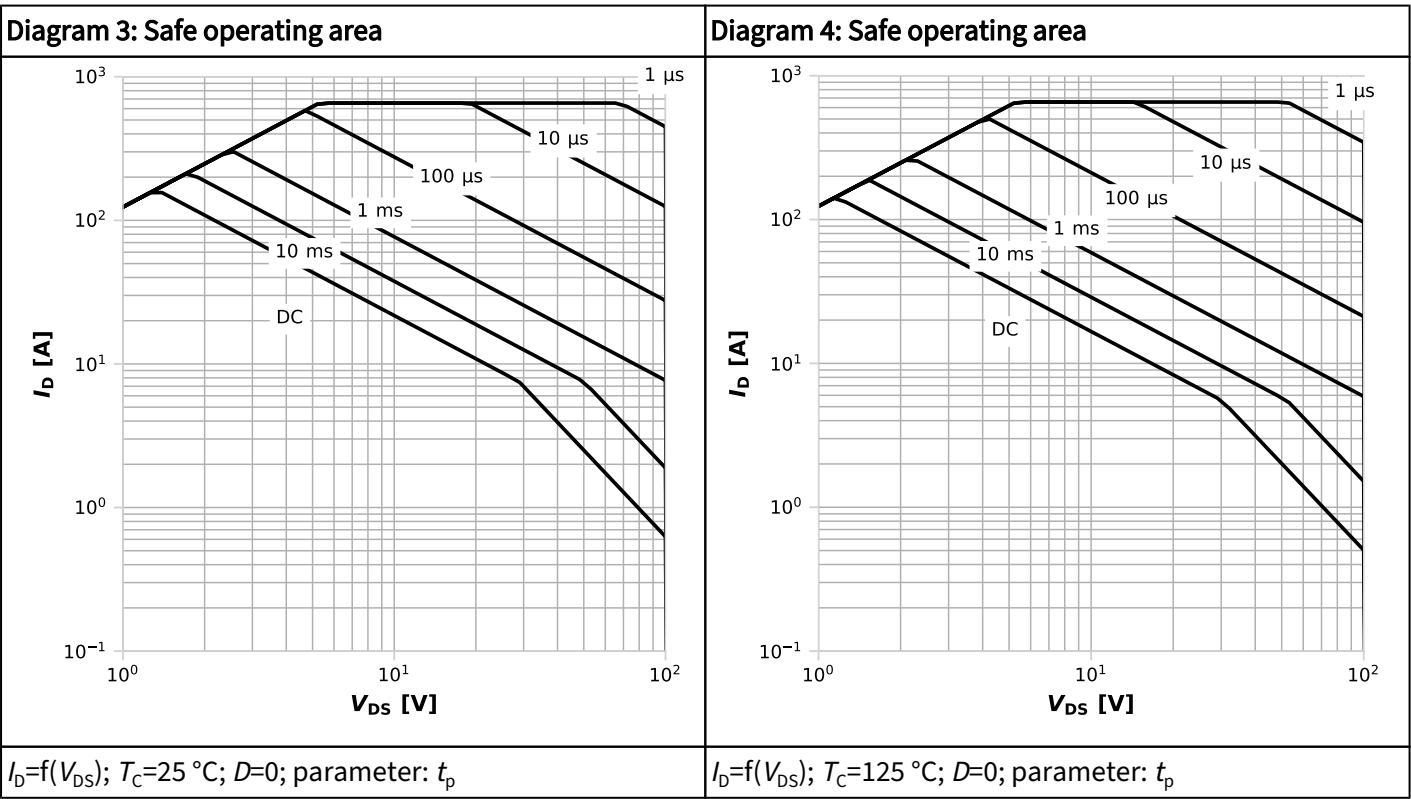
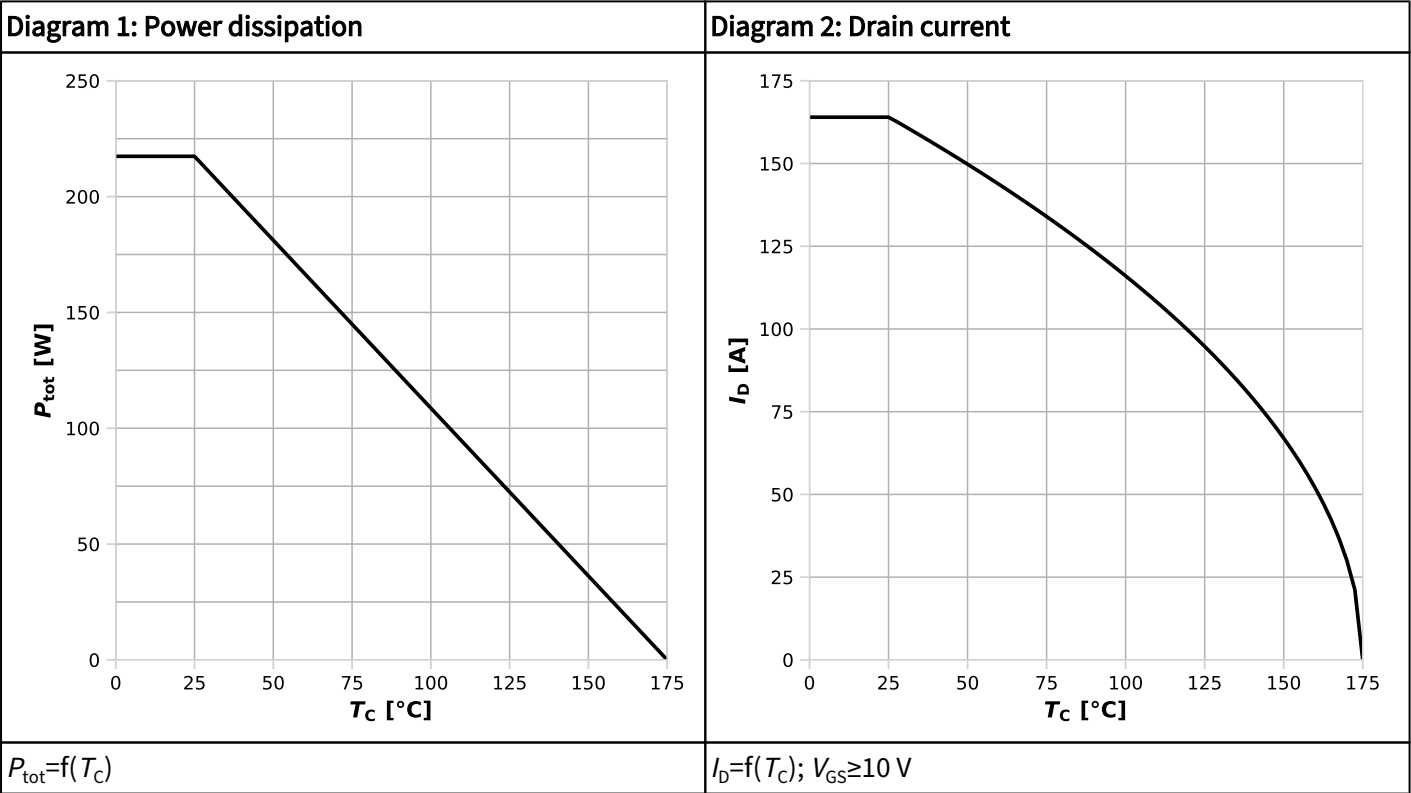
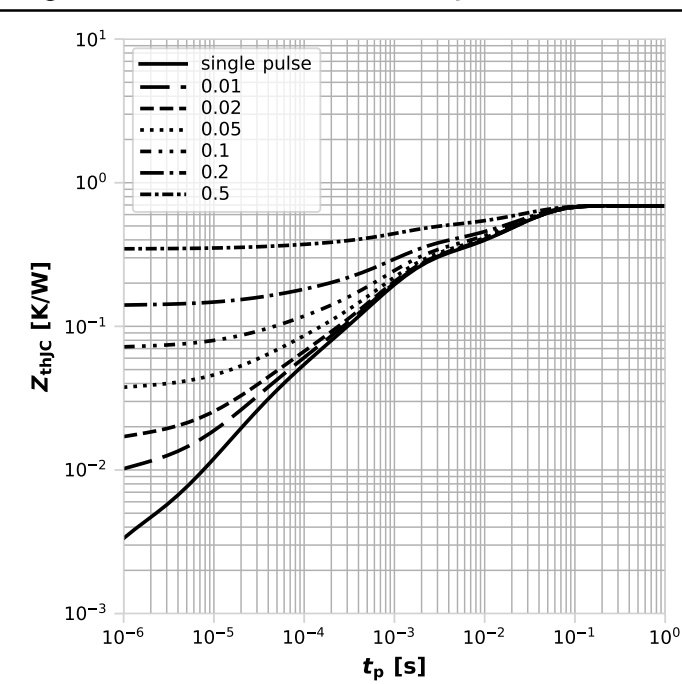
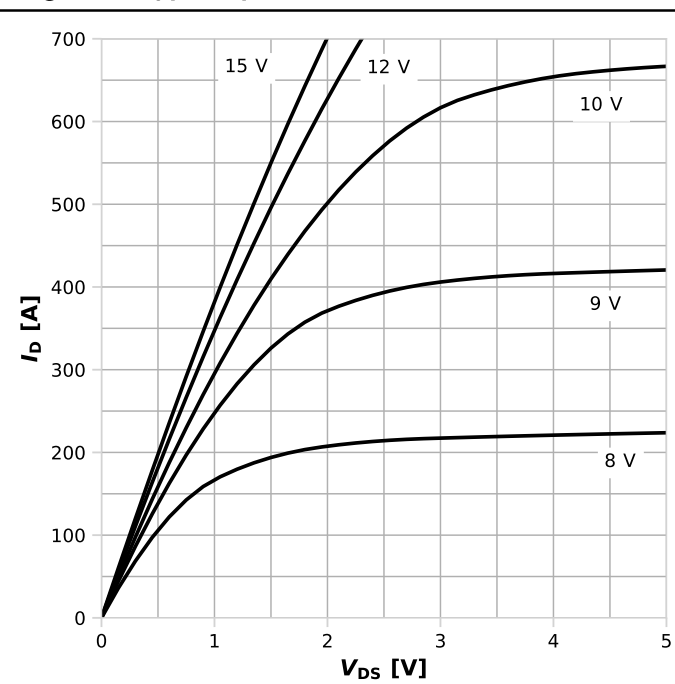


Diagram 5: Max. transient thermal impedance



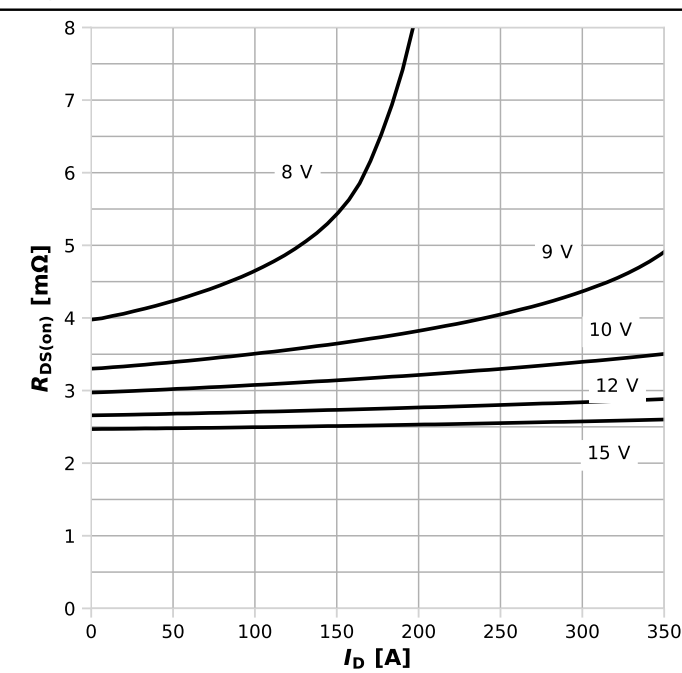
$Z_{thJC} = f(t_p)$ ; parameter:  $D = t_p / T$

Diagram 6: Typ. output characteristics



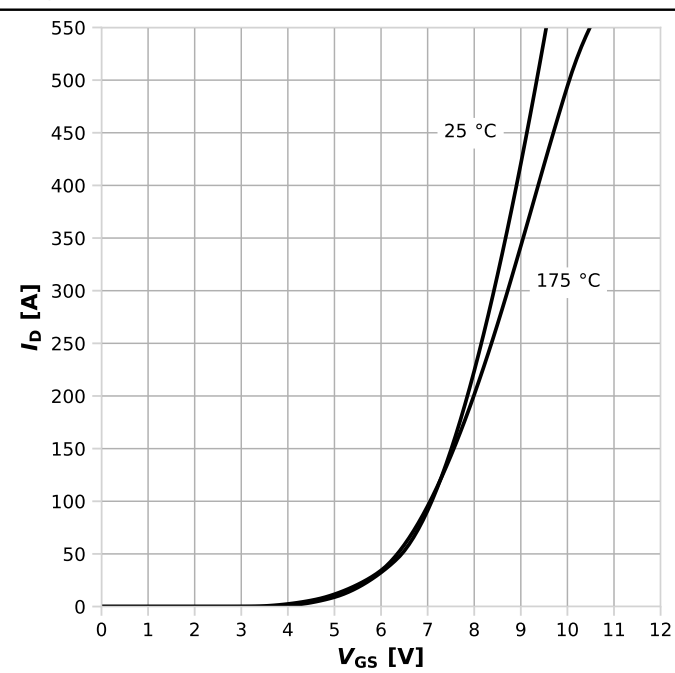
$I_D = f(V_{DS}, T_j = 25^\circ\text{C})$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on resistance



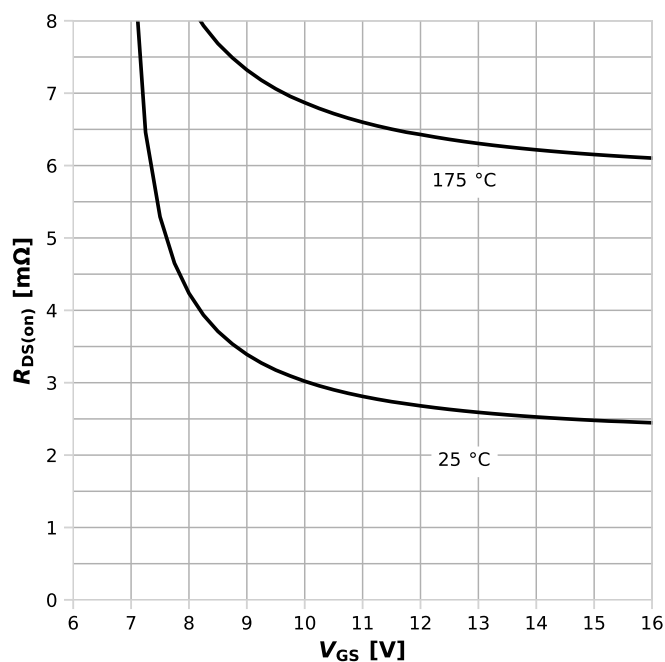
$R_{DS(on)} = f(I_D, T_j = 25^\circ\text{C})$ ; parameter:  $V_{GS}$

Diagram 8: Typ. transfer characteristics



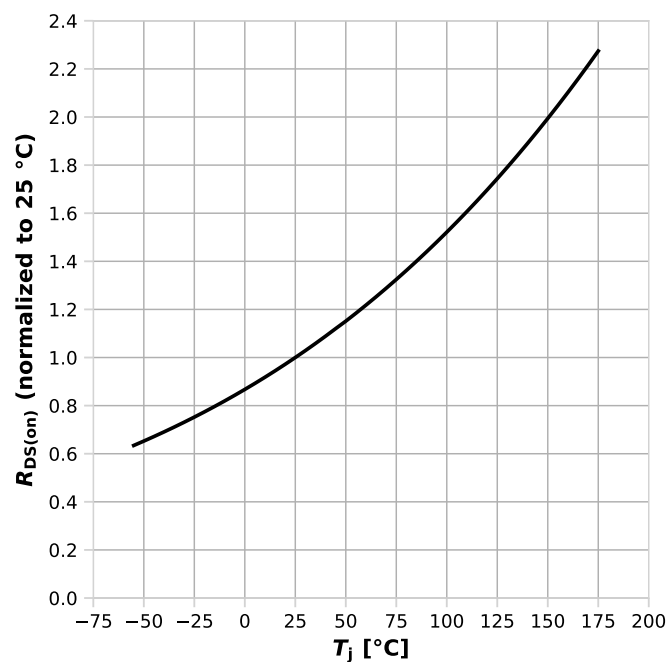
$I_D = f(V_{GS}, |V_{DS}| > 2|I_D|R_{DS(on)max})$ ; parameter:  $T_j$

Diagram 9: Typ. drain-source on resistance



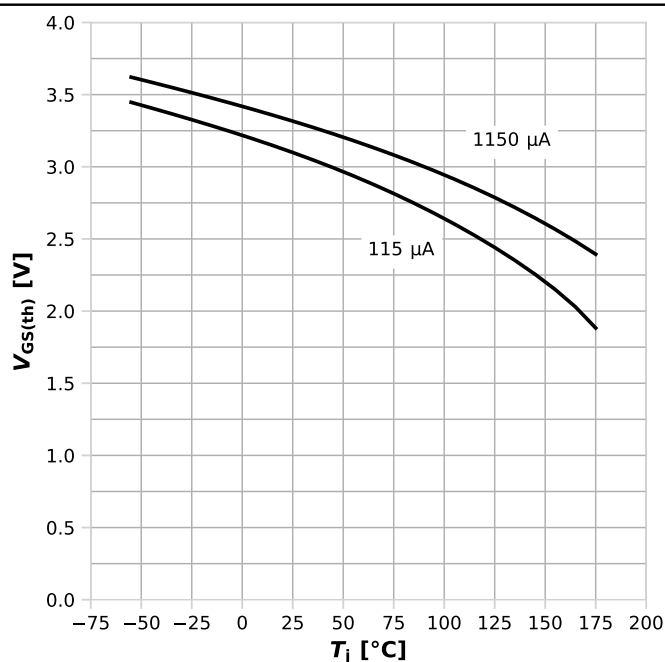
$$R_{DS(on)} = f(V_{GS}), I_D = 50 \text{ A; parameter: } T_j$$

Diagram 10: Normalized drain-source on resistance



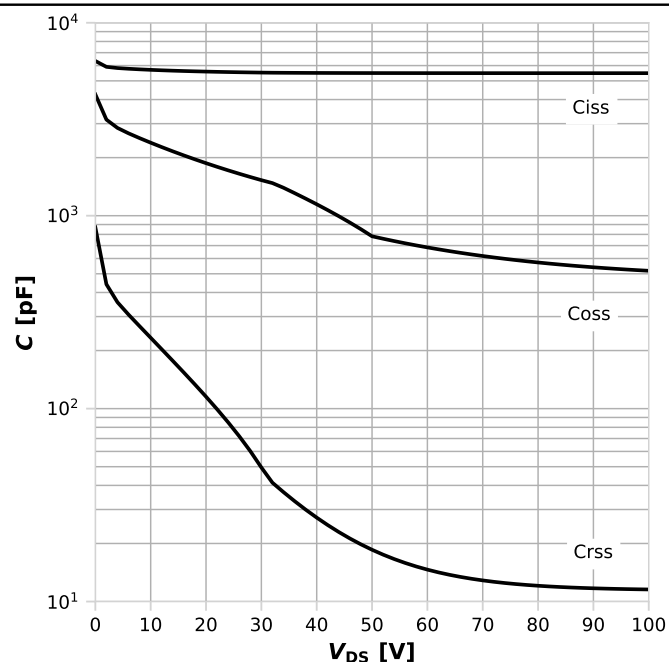
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A, } V_{GS} = 10 \text{ V}$$

Diagram 11: Typ. gate threshold voltage



$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 12: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V; } f = 1 \text{ MHz}$$



Diagram 13: Forward characteristics of reverse diode

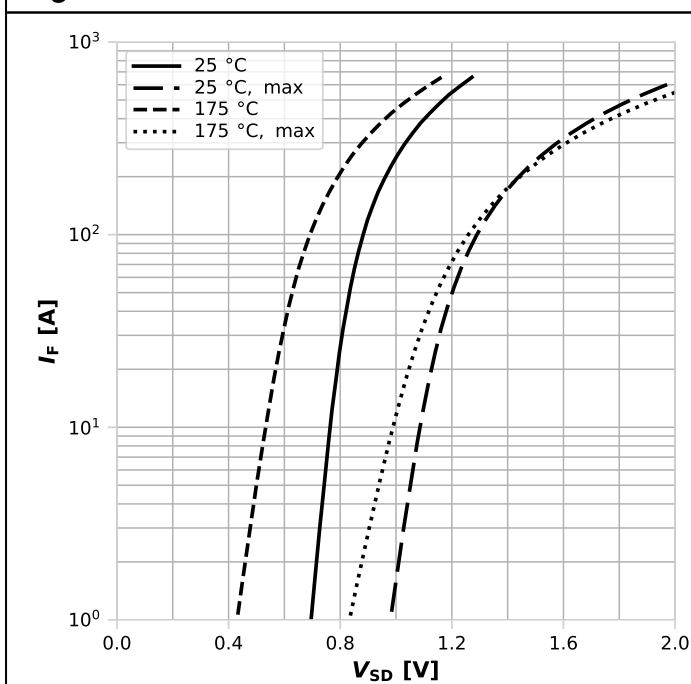

 $I_F = f(V_{SD}); \text{parameter: } T_j$ 

Diagram 14: Avalanche characteristics

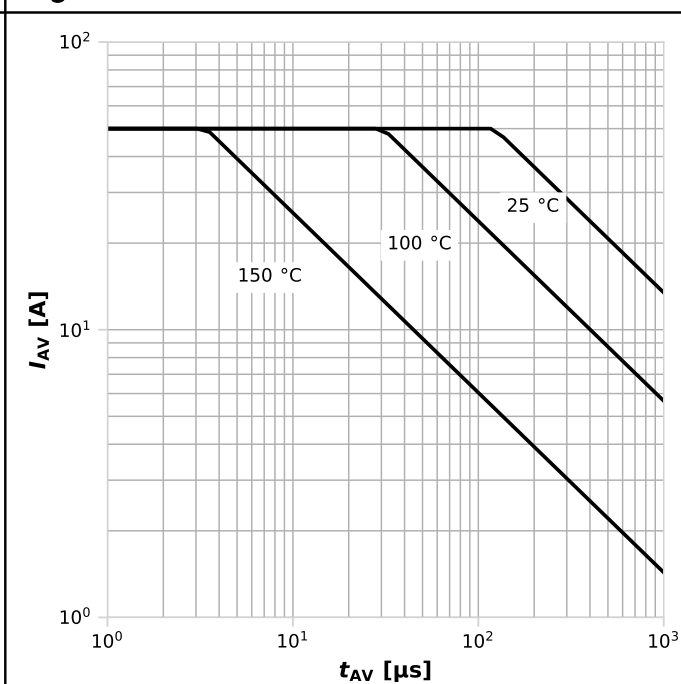

 $I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega; \text{parameter: } T_{j, \text{start}}$ 

Diagram 15: Typ. gate charge

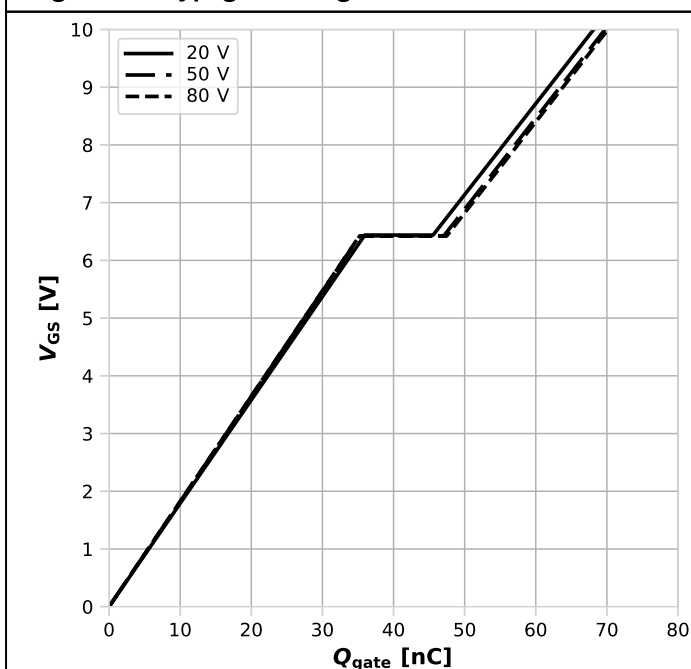
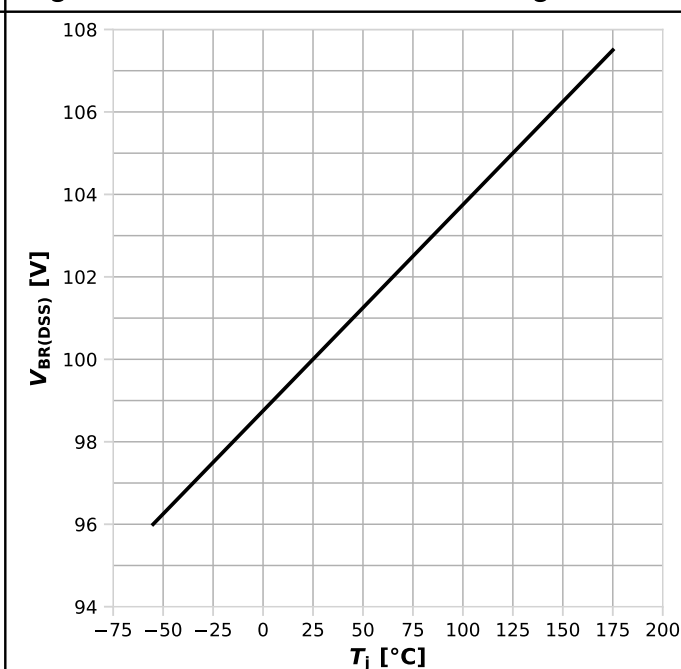
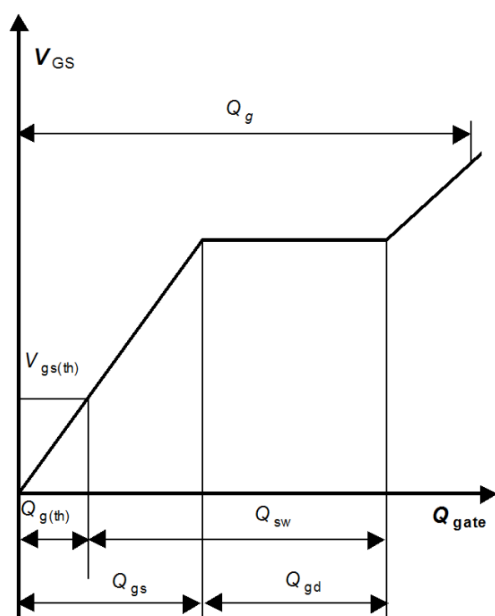

 $V_{GS} = f(Q_{\text{gate}}), I_D = 50 \text{ A pulsed}, T_j = 25 \text{ °C}; \text{parameter: } V_{DD}$ 

Diagram 16: Drain-source breakdown voltage


 $V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

Gate charge waveforms



## 5 Package outlines

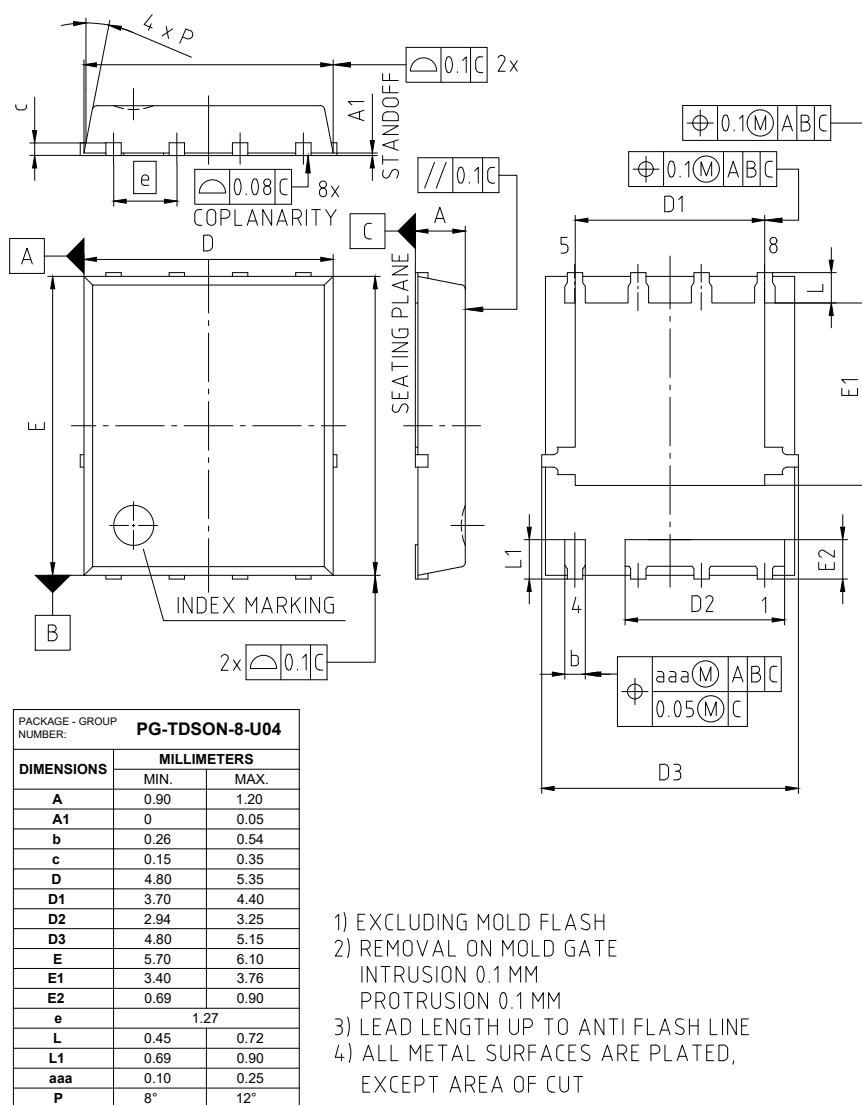
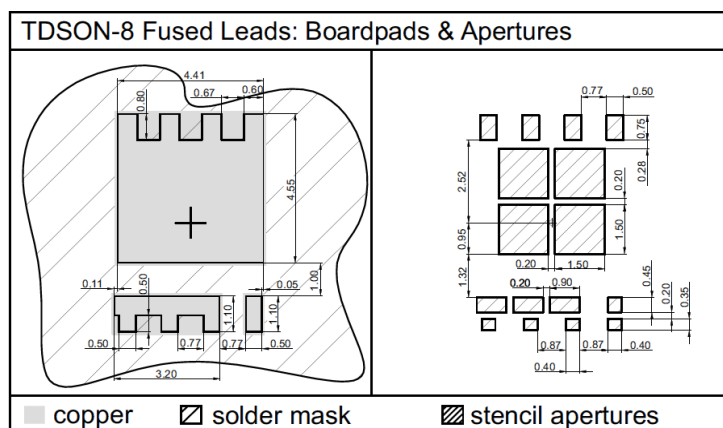
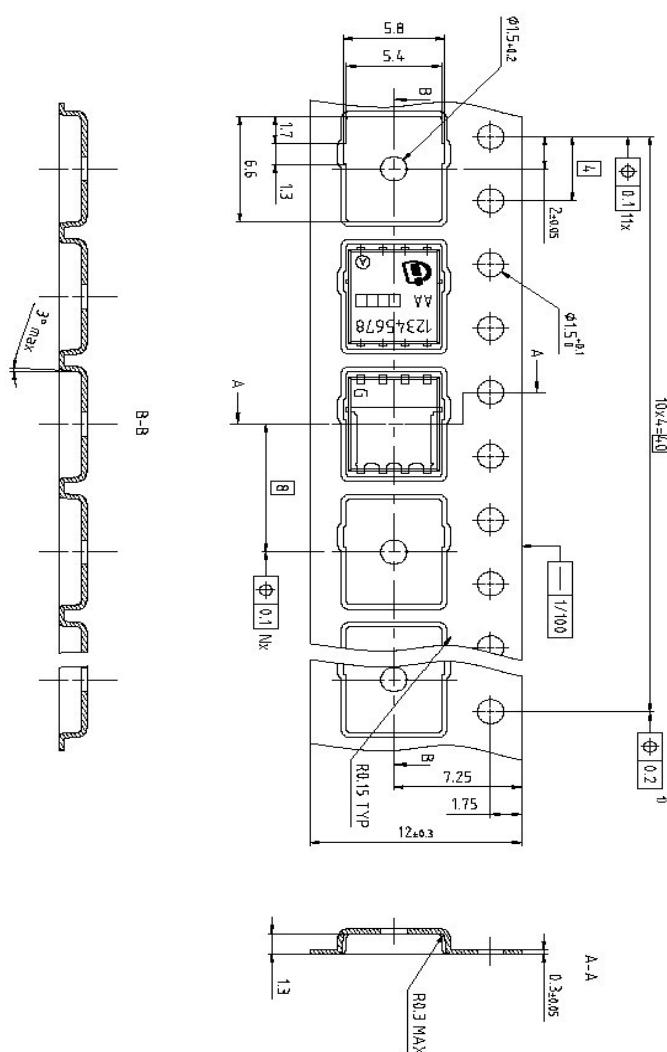


Figure 1 Outline PG-TDSON-8, dimensions in mm



**Figure 2** Footprint drawing PG-TDSO-8, dimensions in mm



**Figure 3** Packaging variant PG-TDSON-8, dimensions in mm

## Revision history

ISC035N10NM5LF2

### Revision 2024-10-22, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.1	2023-11-08	Update sales name and marking
2.2	2024-10-22	Update SOA and transient thermal impedance diagrams

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