Vishay Siliconix

## N-Channel 80 V (D-S) 175 °C MOSFET

### PowerPAK® 8 x 8 BWL



Top View

**Bottom View** 

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	80			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.00115			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.00135			
Q <sub>g</sub> typ. (nC)	140			
I <sub>D</sub> (A) <sup>a</sup>	608			
Configuration	Single			

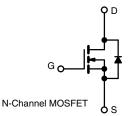
#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- · Wettable flanks enhances solderability
- Fully lead (Pb)-free device
- Very low R<sub>DS</sub> x Q<sub>g</sub> figure of merit (FOM)
- 50 % smaller footprint than D2PAK (TO-263)
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



### **APPLICATIONS**

- Synchronous rectification
- OR-ing
- · Motor drive control
- · Battery management



ORDERING INFORMATION	
Package	PowerPAK® 8 x 8 BWL
Lead (Pb)-free and halogen-free	SiEH4800EW-T1-GE3

ABSOLUTE MAXIMUM RATING	13 (1 <sub>A</sub> = 23 0, t	1			
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	80	V	
Gate-source voltage		V <sub>GS</sub>	± 20		
Continuous drain current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C		381		
	T <sub>C</sub> = 70 °C	T , [	319		
	T <sub>A</sub> = 25 °C	l <sub>D</sub>	34 <sup>b</sup>		
	T <sub>A</sub> = 70 °C	Ī F	29 <sup>b</sup>	Α .	
Pulsed drain current (t = 100 µs)		I <sub>DM</sub>	700		
Continuous source-drain diode current	T <sub>C</sub> = 25 °C	1	379		
	T <sub>A</sub> = 25 °C	ls –	3.1 <sup>b</sup>		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	87		
Single pulse avalanche energy	L = 0.1 IIII	E <sub>AS</sub>	380	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		417		
	T <sub>C</sub> = 70 °C		292	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.4 b	VV	
	T <sub>A</sub> =70 °C	1	2.4 <sup>b</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient <sup>b</sup>	Steady state	R <sub>thJA</sub>	33	44	°C/W	
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	0.27	0.36	C/VV	

#### Notes

a.  $T_C = 25$  °C

b. Surface mounted on 1" x 1" FR4 board

S24-0396-Rev. A, 22-Apr-2024

b. Surface mounted on 1 x 1 FR4 board
c. See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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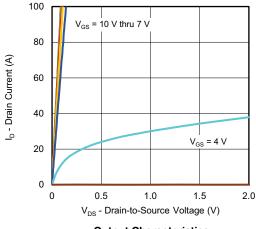
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				•			
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80	-	-	٧	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 10 mA	-	55	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-10	mV/		
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	-	4	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	-	-	± 100	nA	
Zero gate voltage drain current		V <sub>DS</sub> = 80 V, V <sub>GS</sub> =0 V	-	-	1	μА	
	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15		
Drain-source on-state resistance <sup>a</sup>	В	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.00088	0.00115	Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.00091	0.00135		
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A	-	150	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	29 000	-	рF	
Output capacitance	C <sub>oss</sub>		-	1650	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	42	-		
Total colored con	0	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	ı	185	278	nC	
Total gate charge	$Q_g$		ı	140	210		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 7.5 \text{ V}, I_{D} = 10 \text{ A}$	-	51	-		
Gate-drain charge	Q <sub>gd</sub>		-	24	-		
Gate resistance	$R_{g}$	f = 1 MHz	0.24	1.2	2.4	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	23	45		
Rise time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_1 = 4 \Omega, I_D \cong 10 \text{ A},$	-	17	30		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	71	140		
Fall time	t <sub>f</sub>		-	20	40		
Turn-on delay time	t <sub>d(on)</sub>		-	30	60	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_L = 4 \Omega, I_D \cong 10 \text{ A},$	-	26	50		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	64	130		
Fall time	t <sub>f</sub>		ı	20	40		
Drain-Source Body Diode Characterist	cs			•			
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	379	_	
Pulse diode forward current	I <sub>SM</sub>		-	-	700	A	
Body diode voltage	$V_{SD}$	$I_S = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.68	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	83	165	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>		-	252	500	nC	
Reverse recovery fall time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	60	-		
Reverse recovery rise time	t <sub>b</sub>		_	23	-	ns	

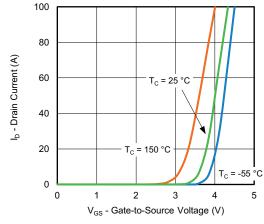
#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

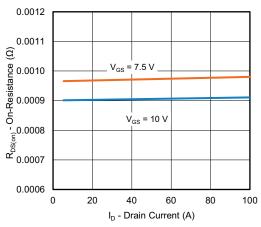


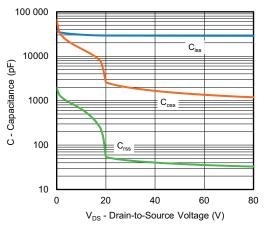






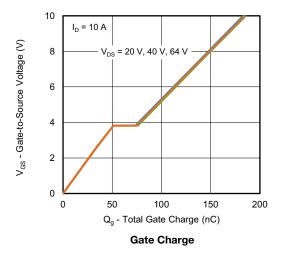


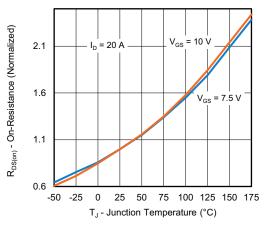




On-Resistance vs. Drain Current and Gate Voltage

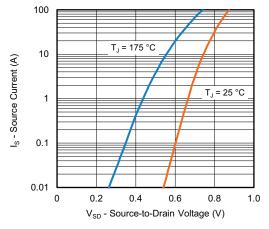
Capacitance



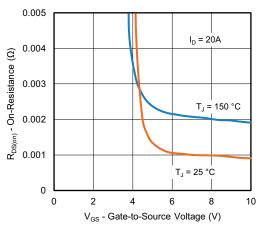


On-Resistance vs. Junction Temperature

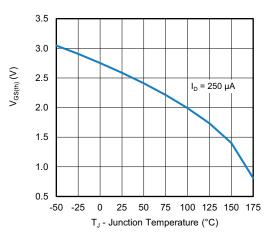




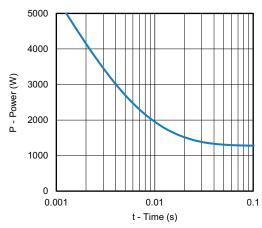
### Source-Drain Diode Forward Voltage



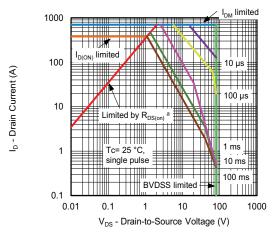
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power, Junction-to-Case

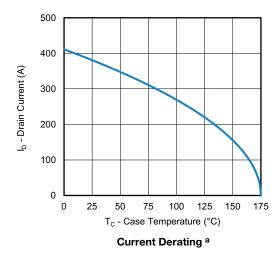


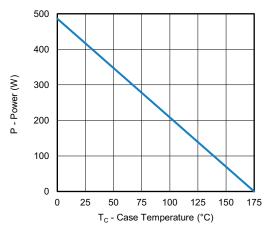
Safe Operating Area, Junction-to-Case

## Note

a.  $V_{GS} > minimum V_{GS}$  at which  $R_{DS(on)}$  is specified





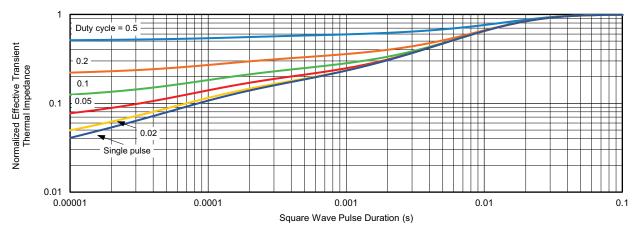


Power, Junction-to-Case

#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



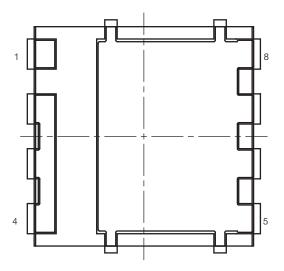


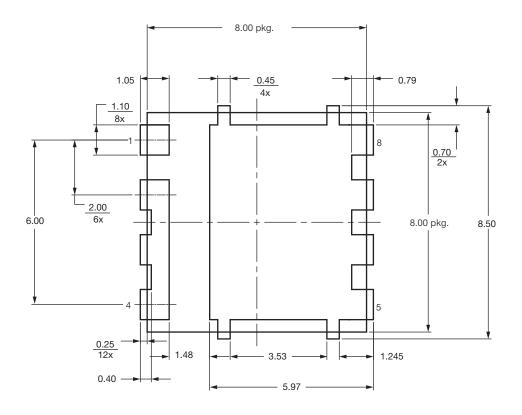
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?61532">www.vishay.com/ppg?61532</a>.



## Recommended Land Pattern PowerPAK® 8 x 8 SW





## Note

Dimensions in mm

Revision: 09-Sep-2024

ECN: T24-0312-Rev. B, 09-Sep-2024

DWG: 3020

Document Number: 62294



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