

PSMN1R1-80ASF

NextPower 80 V, 1.11 mOhm, N-channel MOSFET in CCPAK1212 package

6 December 2024

Product data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 385 A I_{D(max)} continuous current rating
- Low Q_G × R_{DSon} FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212 package

3. Applications

- · Battery protection
- · High power full and half-bridge configurations
- · BLDC motor control
- OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	385	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	935	W
Static characte	eristics					'	
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 25 A; T_{j} = 25 °C; Fig. 11		-	0.87	1.11	mΩ
Dynamic chara	acteristics						
Q_{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		11	37.3	86	nC
Source-drain diode							
Q _r	recovered charge	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 40 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 17$		-	68	-	nC



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	S	source		
4	S	source	12 11 10 9 8 7	
5	S	source	88888	
6	S	source		D
7	D	drain		
8	D	drain		G T
9	D	drain		mbb076 S
10	D	drain	1 2 3 4 5 6 CCPAK1212 (SOT8000A)	
11	D	drain	COPAR1212 (3010000A)	
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN1R1-80ASF	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A		

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R1-80ASF	XP1F1S80A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_i = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	80	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	935	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	385	А
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>	-	385	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3	-	2420	Α

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain	diode					'
Is	source current	T _{mb} = 25 °C		-	385	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	2420	Α
Avalanche ru	ggedness					'
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 109 A; $V_{sup} \le 80$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 230 μs; Fig. 4	[1]	-	1300	mJ
I _{AS}	non-repetitive avalanche current	V_{sup} = 80 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω ; Fig. 4	[1]	-	109	А

[1] Protected by 100% test

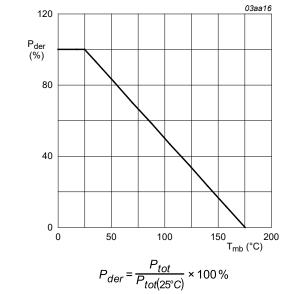
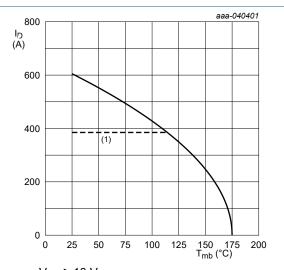
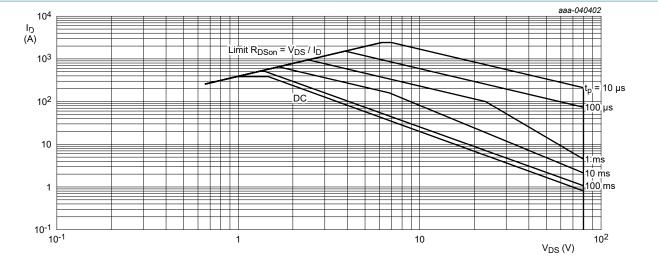


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



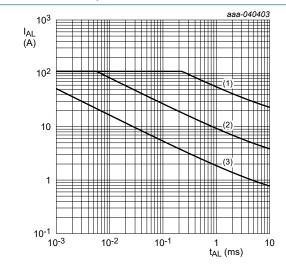
 $V_{GS} \ge 10 \text{ V}$ (1) 385 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j \text{ (init)}}$ = 25 °C; (2) $T_{j \text{ (init)}}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	0.123	0.16	K/W
$R_{th(j-a)}$	thermal resistance from	Fig. 6	-	58	-	K/W
	junction to ambient	Fig. 7	-	29	-	K/W

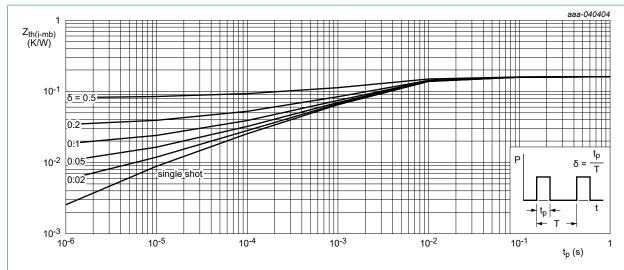
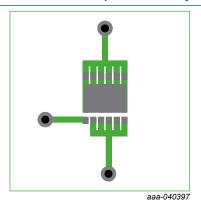
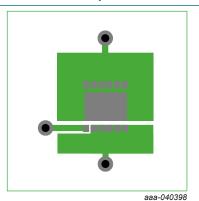


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



70 µm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	cteristics					
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	80	-	-	V
	breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	72	-	-	V
V _{GS(th)}	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	2	3.1	4	V
	voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C	-	1.65	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	3.7	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C	-	-9.19	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	2	μΑ
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 125 °C	-	39	160	μΑ
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 25 A; T_{j} = 25 °C; Fig. 11	-	0.87	1.11	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 12	-	1.3	1.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12	-	1.9	2.6	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>	-	1.16	1.74	mΩ
R_G	gate resistance	f = 1 MHz; T _j = 25 °C	0.65	1.3	2.6	Ω
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	121	242	363	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 ^{\circ}\text{C}$	-	221	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	43	72.2	101	nC
Q _{GS(th)}	pre-threshold gate- source charge		-	47	-	nC
Q _{GS(th-pl)}	post-threshold gate- source charge		-	22.6	-	nC
Q_{GD}	gate-drain charge		11	37.3	86	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _j = 25 °C; Fig. 13; Fig. 14	-	4.3	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 1 MHz;	10554	17591	24627	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	2557	4261	6818	pF
C _{rss}	reverse transfer capacitance		8	83	250	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \Omega; V_{GS} = 10 \text{ V};$	-	66	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	51	-	ns
t _{d(off)}	turn-off delay time	Ţ i	-	155	-	ns
t _f	fall time		-	69	-	ns
Source-drai	n diode		1			
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.76	1	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	61	-	ns
Q _r	recovered charge	V _{DS} = 40 V; T _i = 25 °C; <u>Fig. 17</u>		68		nC

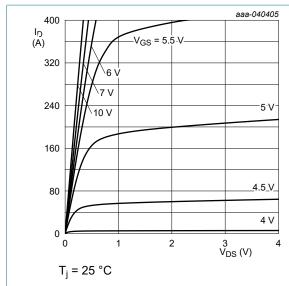


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

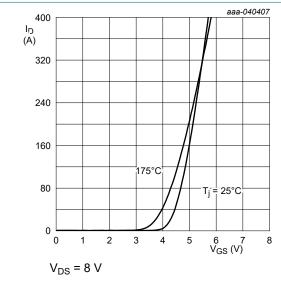


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

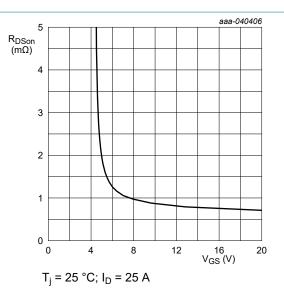


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

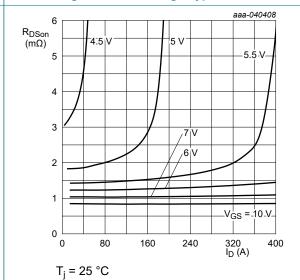


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

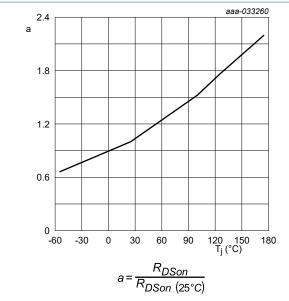


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

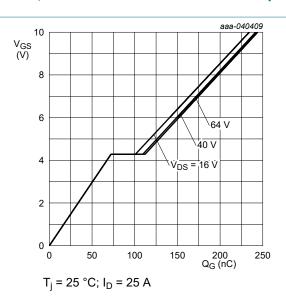


Fig. 13. Gate-source voltage as a function of gate charge; typical values

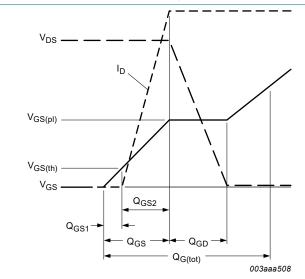
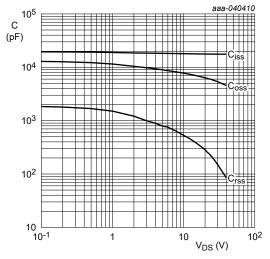


Fig. 14. Gate charge waveform definitions



 $V_{GS} = 0 V$; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

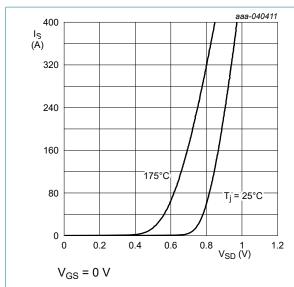


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

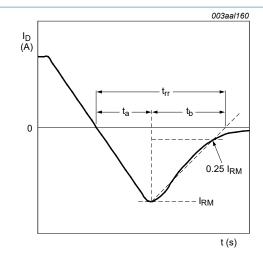


Fig. 17. Reverse recovery timing definition

11. Package outline

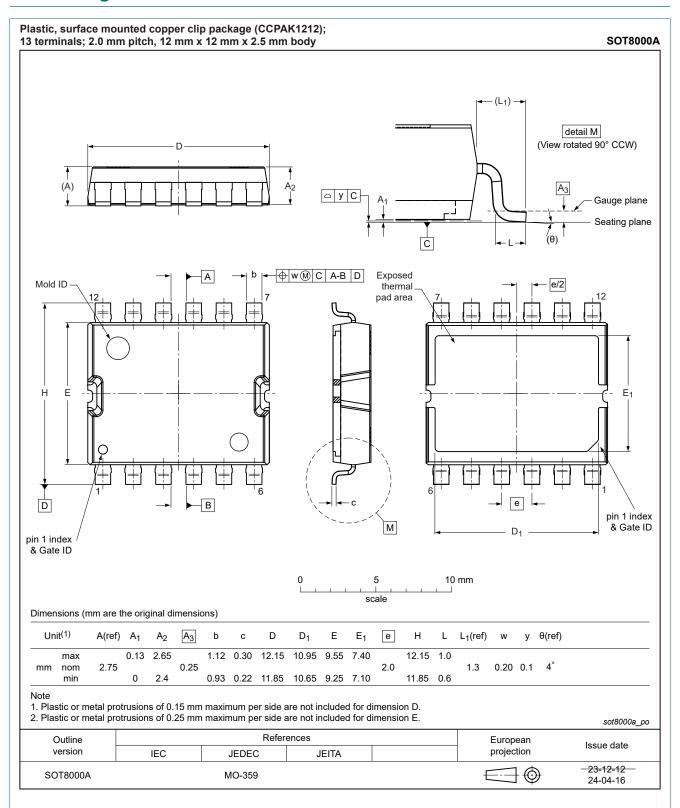
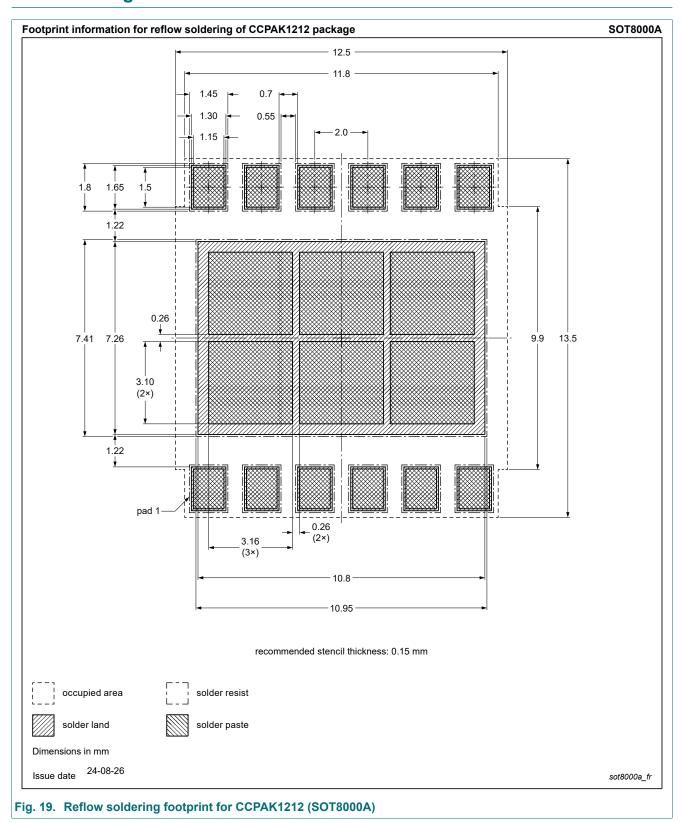


Fig. 18. Package outline CCPAK1212 (SOT8000A)

12. Soldering



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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