

Polar™ Power MOSFET HiPerFET™

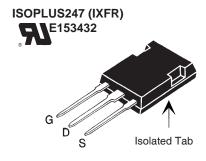
IXFR20N120P

N-Channel Enhancement Mode Avalanche Rated Fast Intrinsic Diode



V _{DSS}	=	1200V
I _{D25}	=	13A
R _{DS(on)}	≤	$630 \mathrm{m}\Omega$
t _{rr}	\leq	300ns

Symbol	Test Conditions	Maximum Ra	atings
V _{DSS}	$T_J = 25^{\circ}C \text{ to } 150^{\circ}C$	1200	V
V _{DGR}	$T_{_J}$ = 25°C to 150°C, $R_{_{GS}}$ = 1M Ω	1200	V
\mathbf{V}_{GSS}	Continuous	± 30	V
V _{GSM}	Transient	± 40	V
I _{D25}	T _C = 25°C	13	Α
I _{DM}	$T_{\rm c} = 25^{\circ}$ C, pulse width limited by $T_{\rm JM}$	50	Α
I _A	T _C = 25°C	10	Α
E _{AS}	$T_{c} = 25^{\circ}C$	1	J
dV/dt	$I_{_{S}} \le I_{_{DM}}, \ V_{_{DD}} \le V_{_{DSS}}, T_{_{J}} \le 150^{\circ}C$	15	V/ns
P _D	T _C = 25°C	290	W
T		-55 +150	°C
T _{JM}		150	°C
T_{stg}		-55 +150	°C
T _L	Maximum lead temperature for soldering	300	°C
T _{SOLD}	Plastic body for 10s	260	°C
V _{ISOL}	50/60 Hz, RMS, 1 minute	2500	٧~
F _c	Mounting force	20120/4.527	N/lb.
Weight		5	g



G = Gate= Drain S = Source

Features

- Silicon chip on Direct-Copper-Bond substrate
 - High power dissipation
- Isolated mounting surface
- 2500V electrical isolation
- Low drain to tab capacitance(<30pF)
- Low R_{DS (on)} HDMOS™ process
 Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- · Fast intrinsic Rectifier

Advantages

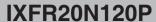
- Easy assembly
- Space savings
- High power density

Symbol Test Conditions Characteristic Values $(T_1 = 25^{\circ}C, unless otherwise specified)$ Min. Typ. Max.

BV _{DSS}	$V_{GS} = 0V, I_D = 1mA$	1200		V
V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 1 \text{mA}$	3.5	6.5	V
I _{GSS}	$V_{GS} = \pm 30V, V_{DS} = 0V$		± 200	nA
I _{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$ T_{J}	= 125°C	25 5	μA mA
R _{DS(on)}	$V_{GS} = 10V, I_{D} = 10A, Note 1$		630	mΩ

Applications:

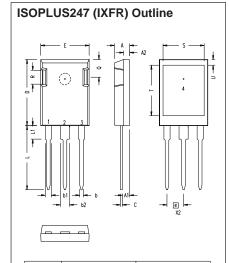
- High Voltage Switched-mode and resonant-mode power supplies
- High Voltage Pulse Power Applications
- High Voltage Discharge circuits in Lasers Pulsers, Spark Igniters, RF Generators
- High Voltage DC-DC converters
- High Voltage DC-AC inverters





Symbol (T ₁ = 25°C u	Test Conditions nless otherwise specified)	Char Min.	acteristic Typ.	Values Max.
g _{fs}	$V_{DS} = 20V, I_{D} = 10A, Note 1$	10	16	S
C _{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		11.1 600	nF pF
C _{rss} J	Gate input resistance		1.60	pF Ω
t _{d(on)}	Resistive Switching Times		49	ns
t _r	$V_{GS} = 10V$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_{D} = 10A$ $R_{G} = 1\Omega$ (External)		45 72	ns ns
t _f			70	ns
$Q_{g(on)}$	V 40V V 05 V 1 40A		193	nC
Q_{gs} Q_{gd}	$V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_{D} = 10A$		74 85	nC nC
R _{thJC}				0.43 °C/W
\mathbf{R}_{thCS}			0.15	°C/W

Source-Drain Diode Chara		acteristic Values		
$T_J = 25^{\circ}\text{C}$ unless otherwise specified) Min.	Тур.	Max.		
I_s $V_{GS} = 0V$		20 A		
$\mathbf{I}_{\mathtt{SM}}$ Repetitive, pulse width limited by $T_{\mathtt{JM}}$		80 A		
V_{SD} $I_F = I_S$, $V_{GS} = 0V$, Note 1		1.5 V		
\mathbf{t}_{rr}		300 ns		
ο } '	0.84	μС		
I_{RM} $\int V_{R} = 100V, V_{GS} = 0V$	9	A		



MYZ	INCHES		MILLIMETERS		
2114	MIN	MAX	MIN	MAX	
Α	.190	.205	4.83	5.21	
A1	.090	.100	2.29	2.54	
A2	.075	.085	1.91	2.16	
b	.045	.055	1.14	1.40	
b1	.075	.084	1.91	2.13	
b2	.115	.123	2.92	3.12	
С	.024	.031	0.61	0.80	
D	.819	.840	20.80	21.34	
E	.620	.635	15.75	16.13	
е	.215 BSC		5.45 BSC		
L	.780	.800	19.81	20.32	
L1	.150	.170	3.81	4.32	
Q	.220	.244	5.59	6.20	
R	.170	.190	4.32	4.83	
S	.520	.540	13.21	13.72	
Т	.620	.640	15.75	16.26	
U	.065	.080	1.65	2.03	

1 - GATE

2 - DRAIN (COLLECTOR) 3 - SOURCE (EMITTER) 4 - NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Note 1: Pulse test, $t \le 300\mu s$; duty cycle, $d \le 2\%$.



Fig. 1. Output Characteristics @ 25°C

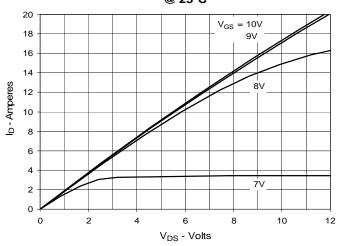


Fig. 2. Extended Output Characteristics @ 25°C

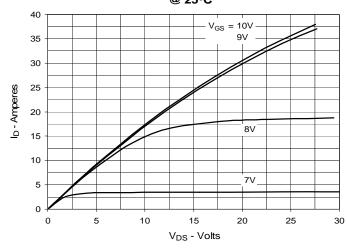


Fig. 3. Output Characteristics @ 125°C

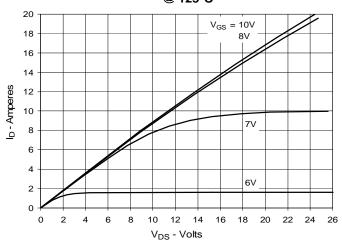


Fig. 4. R_{DS(on)} Normalized to I_D = 10A Value vs. Junction Temperature

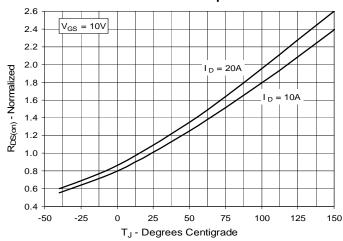


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 10A Value vs. Drain Current

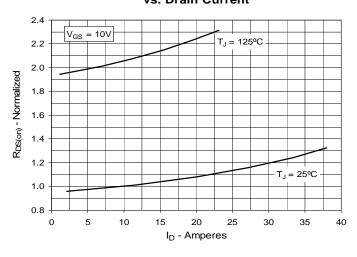


Fig. 6. Maximum Drain Current vs.

Case Temperature

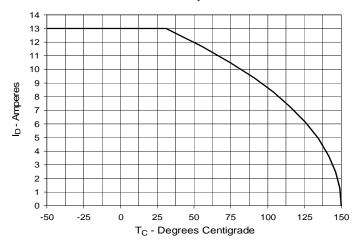




Fig. 7. Input Admittance

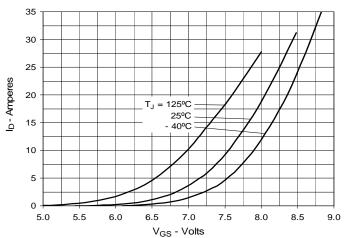


Fig. 8. Transconductance

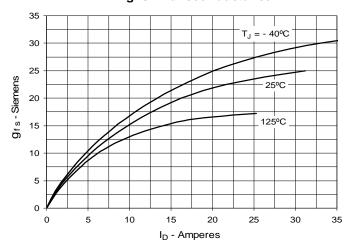


Fig. 9. Forward Voltage Drop of Intrinsic Diode

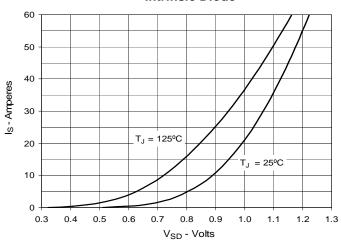


Fig. 10. Gate Charge

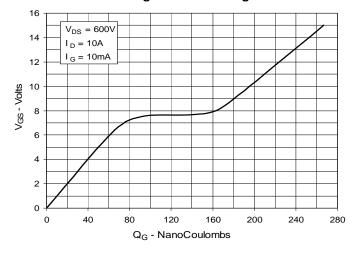


Fig. 11. Capacitance

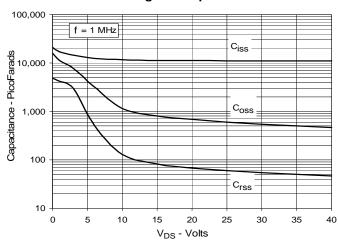
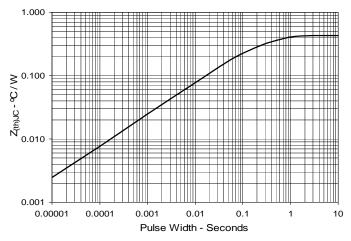


Fig. 12. Maximum Transient Thermal Impedance



IXYS reserves the right to change limits, test conditions, and dimensions.

