

CoolSiC™

PG-TO247-3

400V CoolSiC™ G2 MOSFET

Features

- Ideal for high frequency switching and synchronous rectification
- Commutation robust fast body diode with low Q_{fr}
- Low $R_{DS(on)}$ dependency on temperature
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5\text{ V}$
- Recommended gate driving voltage 0 V to 18 V
- .XT interconnection technology for best-in-class thermal performance
- 100% avalanche tested

Potential applications

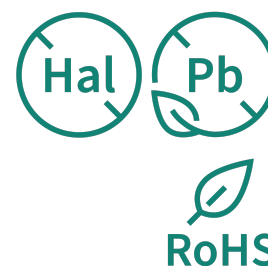
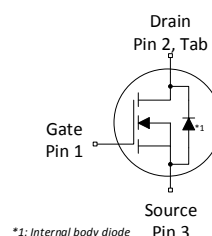
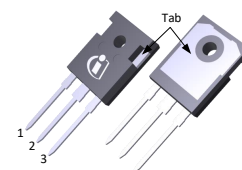
- SMPS
- Solar PV inverters
- Energy storage, UPS and battery formation
- Class-D audio
- Motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	400	V
$R_{DS(on),typ}$	11.5	mΩ
I_D	104	A
Q_{oss}	138	nC
E_{oss}	9.9	μJ
Q_G	85	nC



Part number	Package	Marking	Related links
IMW40R011M2H	PG-TO247-3	40R011M2	-



Table of contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Operating range 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Test circuits 13

Package outlines 14

Revision history 16

Trademarks 17

Disclaimer 17

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	104	A	$V_{GS}=18\text{ V}$, $T_C=25\text{ °C}$
				80		$V_{GS}=18\text{ V}$, $T_C=100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	312	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	220	mJ	$I_D=37.1\text{ A}$, $R_{GS}=25\text{ }\Omega$
Avalanche energy, repetitive	E_{AR}			1.1		
Gate source voltage (static)	$V_{GS,DC}$	-7	-	23	V	-
Gate source voltage (transient)	$V_{GS,AC}$	-10	-	25	V	$t_{pulse}\leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	341	W	$T_C=25\text{ °C}$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ See Diagram 3 for more detailed information.

³⁾ See Diagram 19 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.44	°C/W	-

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$		0			

4 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	400	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1.33\text{ mA}$
Gate threshold voltage ⁴⁾	$V_{GS(th)}$	3.5	4.5	5.6	V	$V_{DS}=V_{GS}$, $I_D=13.3\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	1	75	μA	$V_{DS}=400\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			2	-		$V_{DS}=400\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=175\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	11.5	14.4	m Ω	$V_{GS}=18\text{ V}$, $I_D=37.1\text{ A}$, $T_j=25\text{ °C}$
			16.7	-		$V_{GS}=18\text{ V}$, $I_D=37.1\text{ A}$, $T_j=175\text{ °C}$
			13.9	-		$V_{GS}=15\text{ V}$, $I_D=37.1\text{ A}$, $T_j=25\text{ °C}$
Gate resistance	R_G	-	2.3	-	Ω	-

⁴⁾ Tested after 1ms pulse at $V_{GS} = +20\text{V}$.

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=200\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		410			
Reverse transfer capacitance	C_{rss}		33			
Effective output capacitance, energy related ⁵⁾	$C_{o(er)}$	-	494	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=0\ldots 200\text{ V}$
Effective output capacitance, time related ⁶⁾	$C_{o(tr)}$	-	690	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{ V}$, $V_{DS}=0\ldots 200\text{ V}$
Turn-on delay time ⁷⁾	$t_{d(on)}$	-	13.9	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=0\ldots 18\text{ V}$, $I_D=37.1\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Rise time ⁷⁾	t_r		22.4			
Turn-off delay time ⁷⁾	$t_{d(off)}$	-	27.7	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=18\ldots 0\text{ V}$, $I_D=37.1\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Fall time ⁷⁾	t_f		7.1			

⁵⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 200 V.

⁶⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 200 V.

⁷⁾ Refer to Table 9 for test setup.

Table 7 Gate Charge Characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	23	-	nC	$V_{DD}=200\text{ V}$, $I_D=37.1\text{ A}$, $V_{GS}=0\text{ to }18\text{ V}$
Gate to drain charge	Q_{gd}		17.5			
Gate charge total	Q_g		85			
Gate charge total, sync. FET	$Q_{g(sync)}$	-	79	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }18\text{ V}$
Output charge	Q_{oss}	-	138	-	nC	$V_{DS}=200\text{ V}$, $V_{GS}=0\text{ V}$
Output Energy	E_{oss}		9.9		μJ	

⁸⁾ As per JEP192, Guidelines for Gate Charge (Q_g) Test Method for SiC MOSFET.

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	64	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	312	A	$T_C=25\text{ °C}$, $t_{pulse}\leq 250\text{ ns}$
Diode forward voltage	V_{SD}	-	3.5	4.3	V	$V_{GS}=0\text{ V}$, $I_S=37.1\text{ A}$, $T_J=25\text{ °C}$
MOSFET forward recovery time	t_{fr}	-	20.5	-	ns	$V_R=200\text{ V}$, $I_S=37.1\text{ A}$, $di_S/dt=1000\text{ A}/\mu\text{s}$
MOSFET forward recovery charge ⁹⁾	Q_{fr}		146		nC	

⁹⁾ Q_{fr} includes Q_{oss} . Refer to Table 10 for test setup.

5 Electrical characteristics diagrams

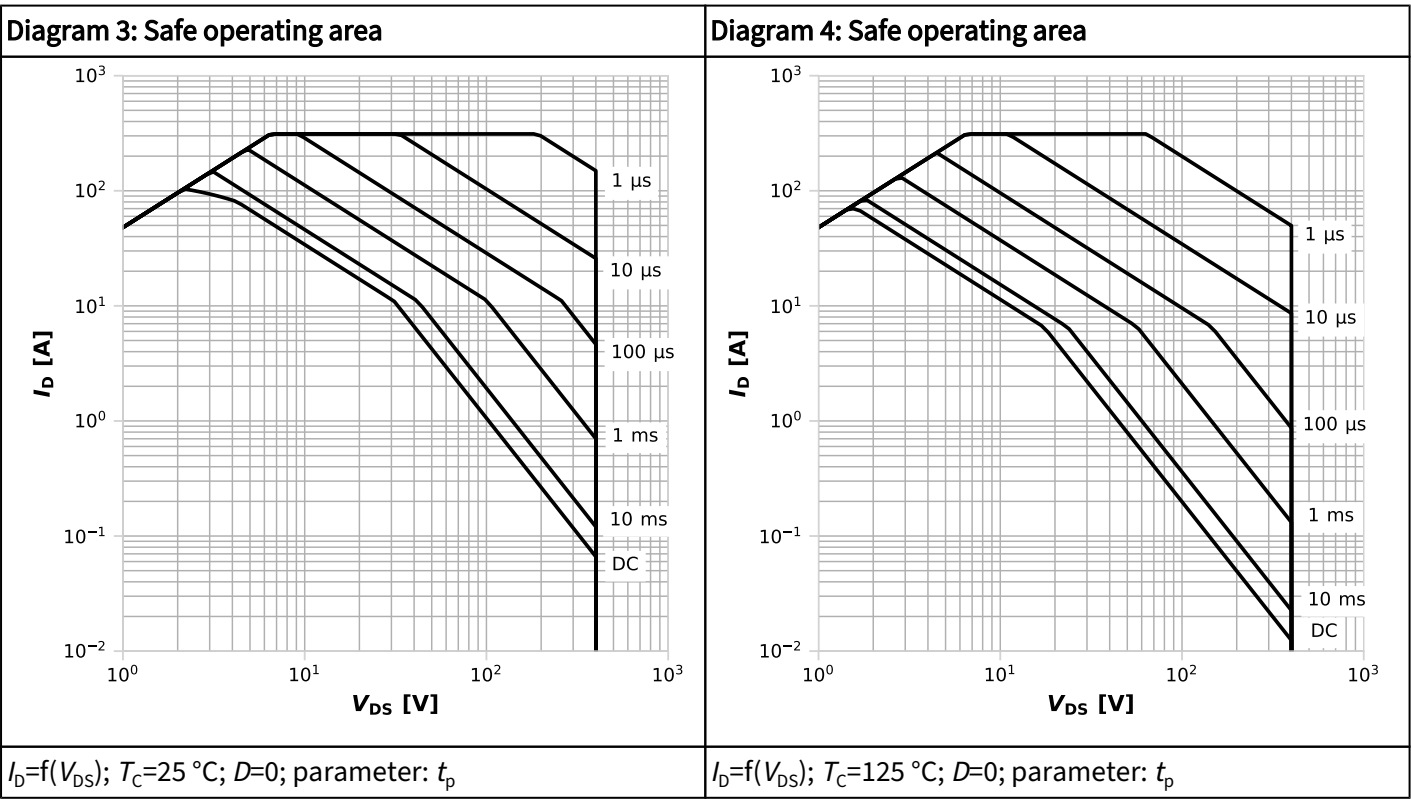
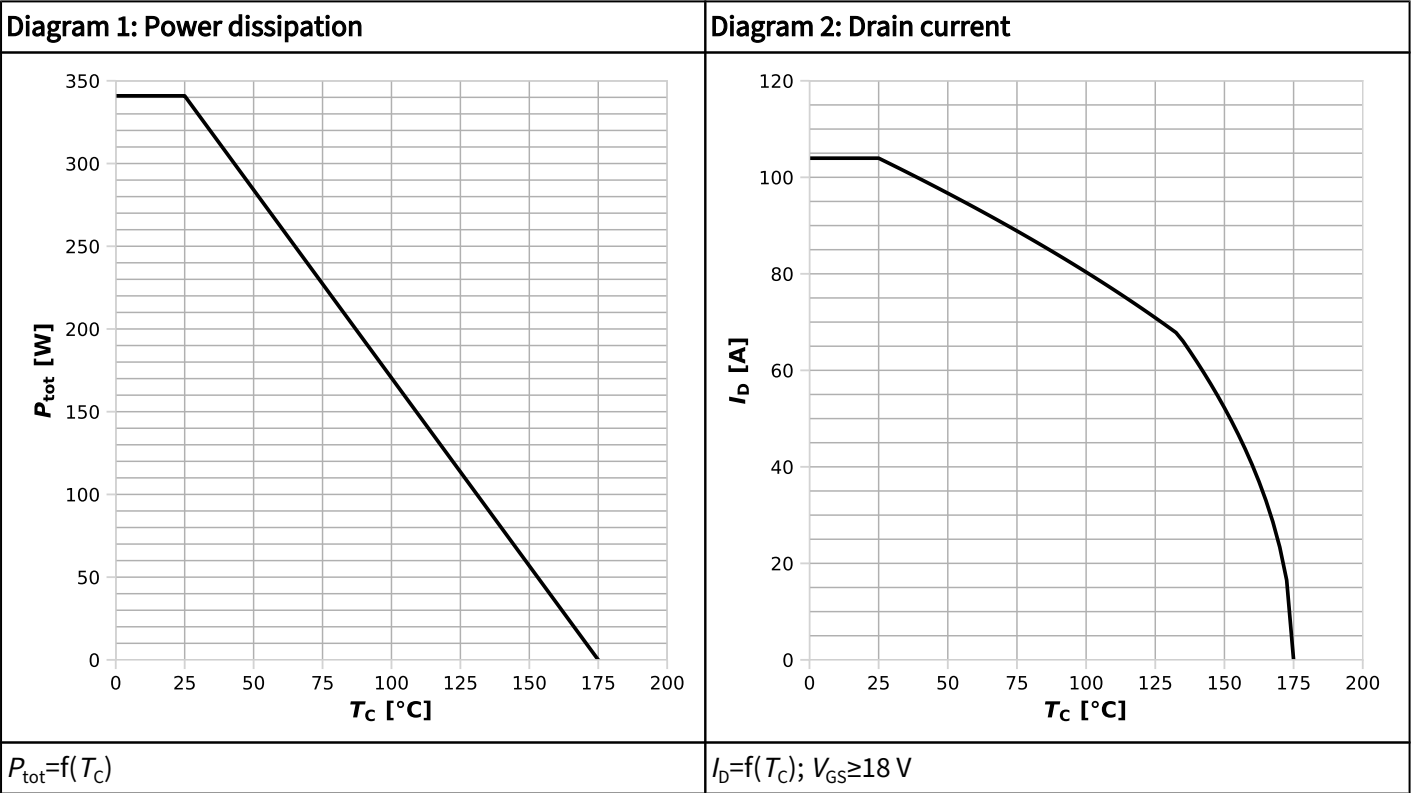
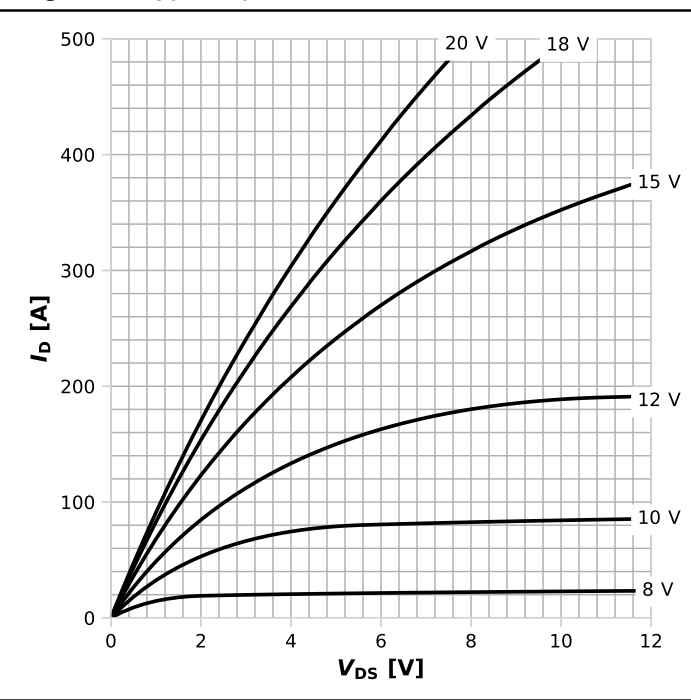
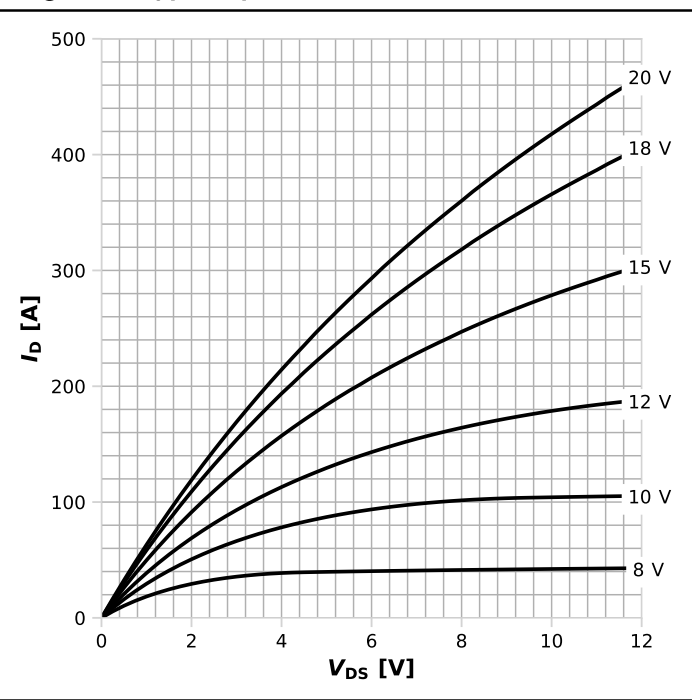


Diagram 5: Typ. output characteristics



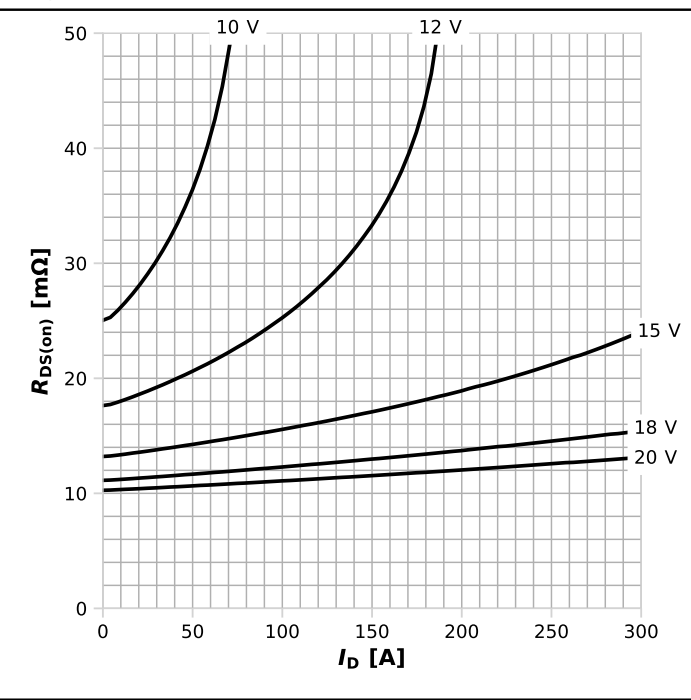
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



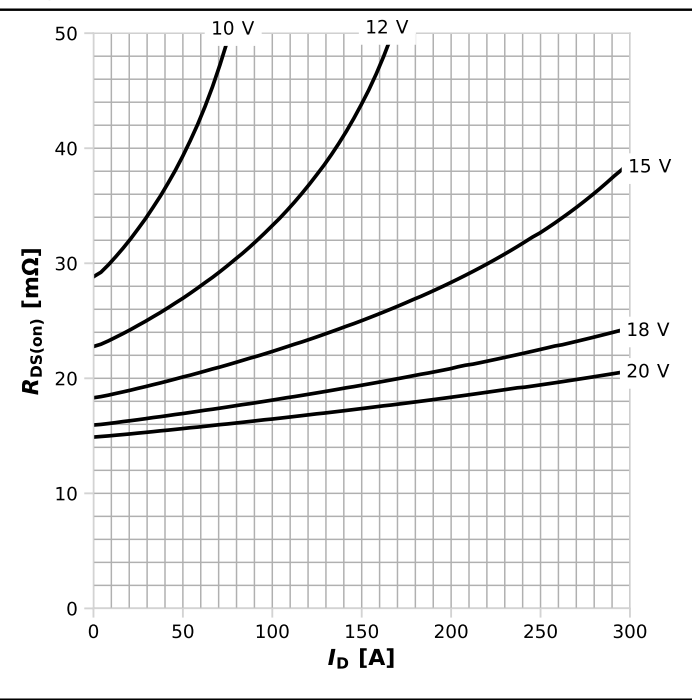
$I_D = f(V_{DS})$, $T_j = 175\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on resistance



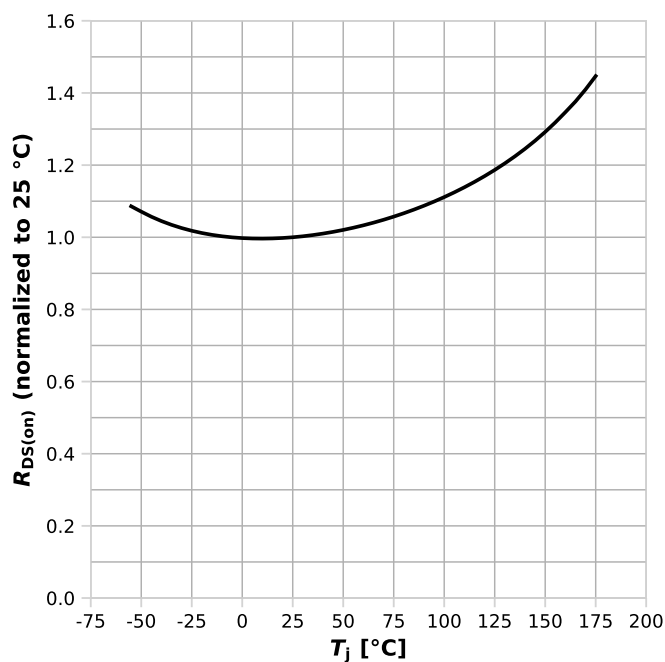
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 8: Typ. drain-source on resistance



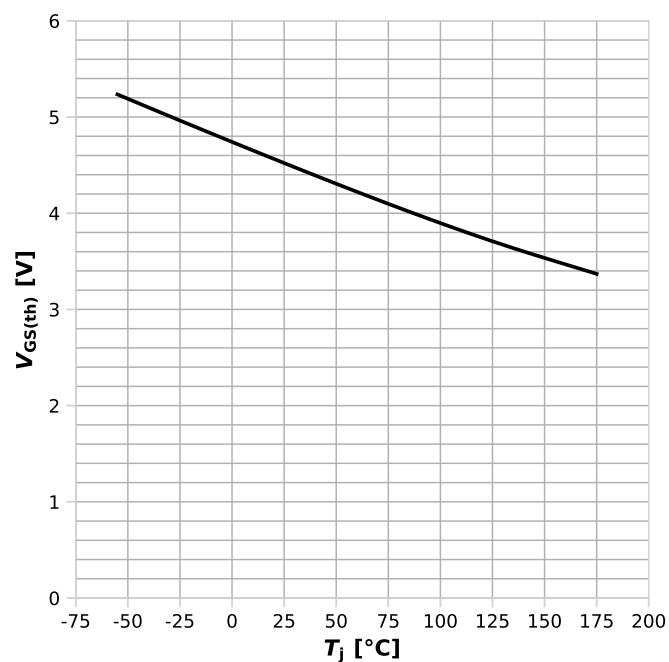
$R_{DS(on)} = f(I_D)$, $T_j = 175\text{ °C}$; parameter: V_{GS}

Diagram 9: Normalized drain-source on resistance



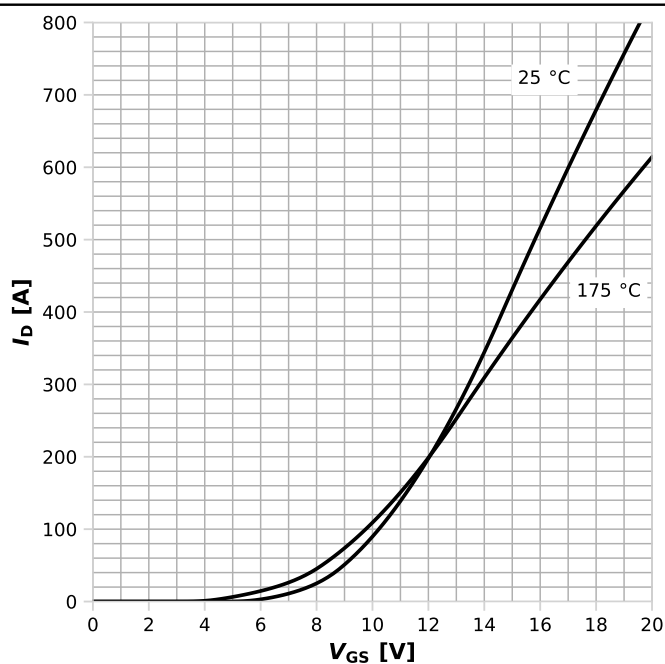
$$R_{DS(on)} = f(T_j), I_D = 37.1 \text{ A}, V_{GS} = 18 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



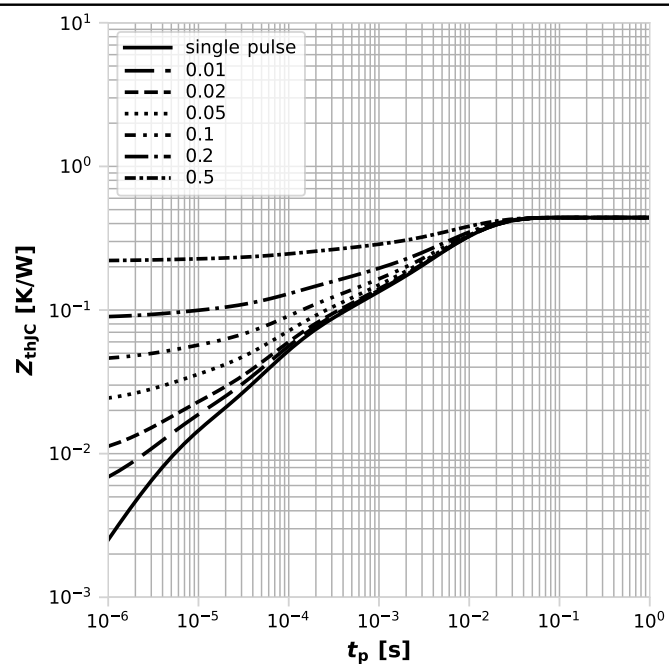
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}, I_D = 13.3 \text{ mA}$$

Diagram 11: Typ. transfer characteristics



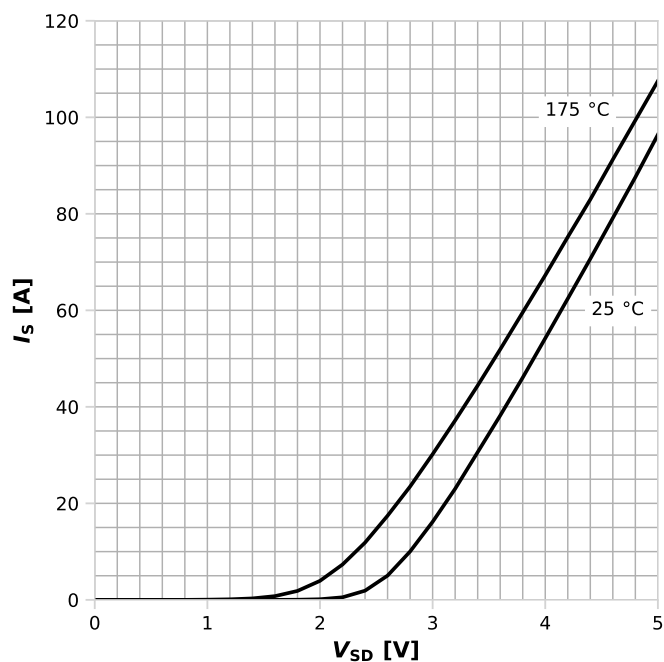
$$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max}, \text{ parameter: } T_j$$

Diagram 12: Max. transient thermal impedance



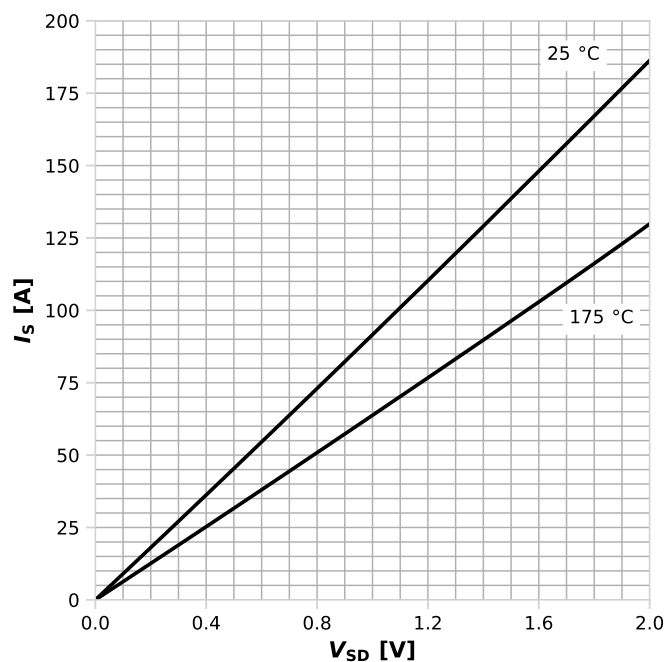
$$Z_{thJC} = f(t_p), \text{ parameter: } D = t_p / T$$

Diagram 13: Reverse output characteristics



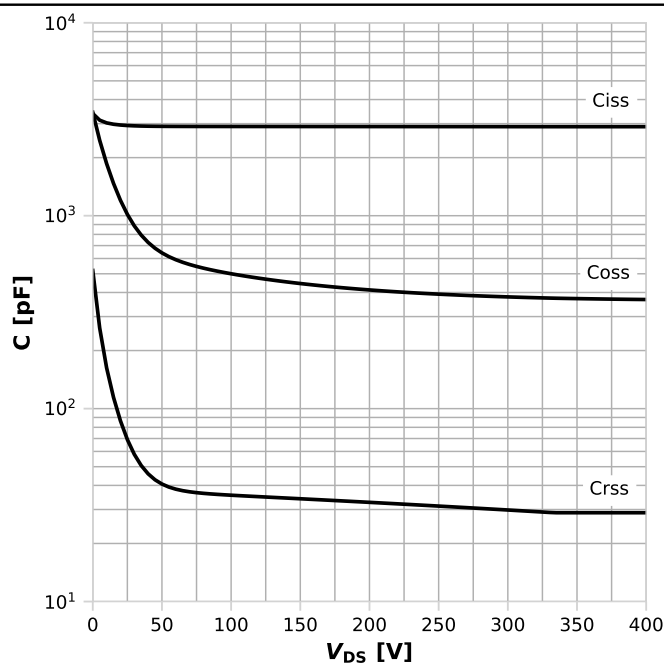
$I_F = f(V_{SD})$, $V_{GS} = 0\text{ V}$; parameter: T_j

Diagram 14: Reverse output characteristics



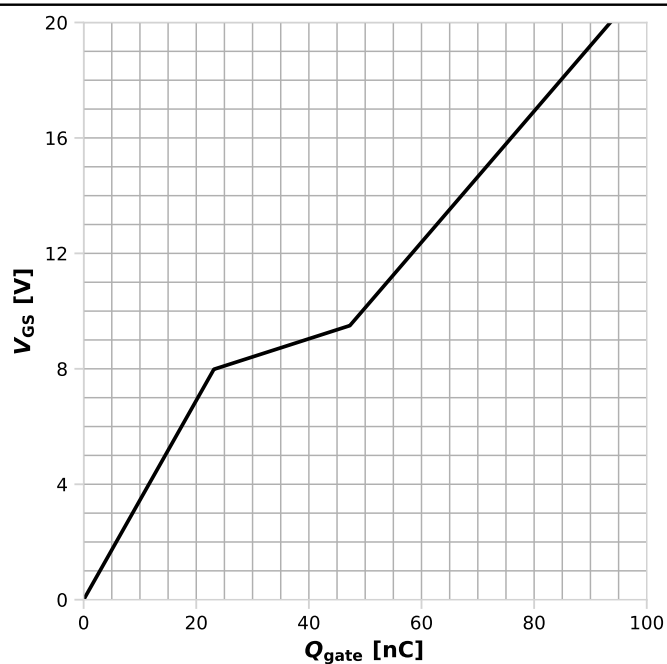
$I_F = f(V_{SD})$, $V_{GS} = 18\text{ V}$; parameter: T_j

Diagram 15: Typ. capacitances



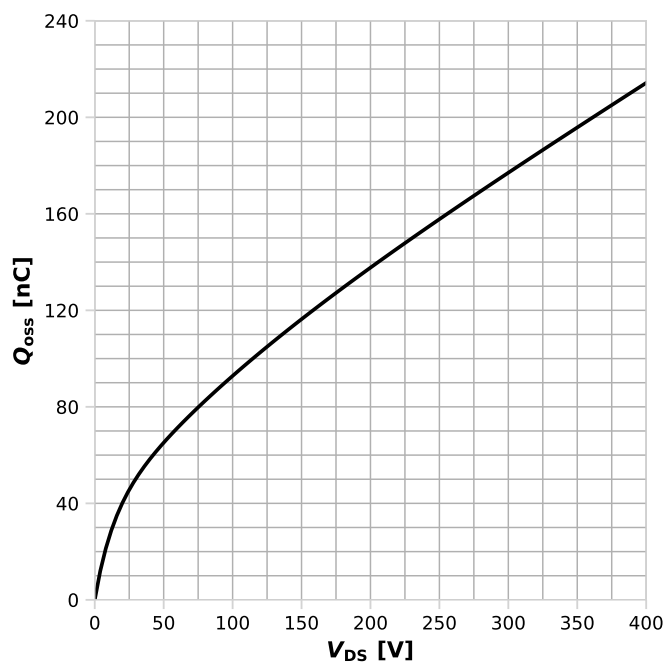
$C = f(V_{DS})$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Diagram 16: Typ. gate charge



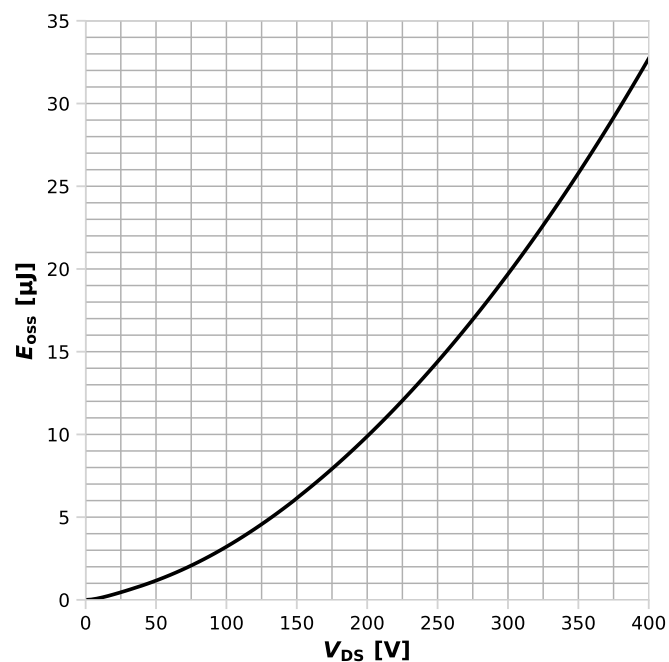
$V_{GS} = f(Q_{gate})$, $V_{DD} = 200\text{ V}$, $I_D = 37.1\text{ A}$ pulsed, $T_j = 25\text{ °C}$

Diagram 17: Typ. output charge



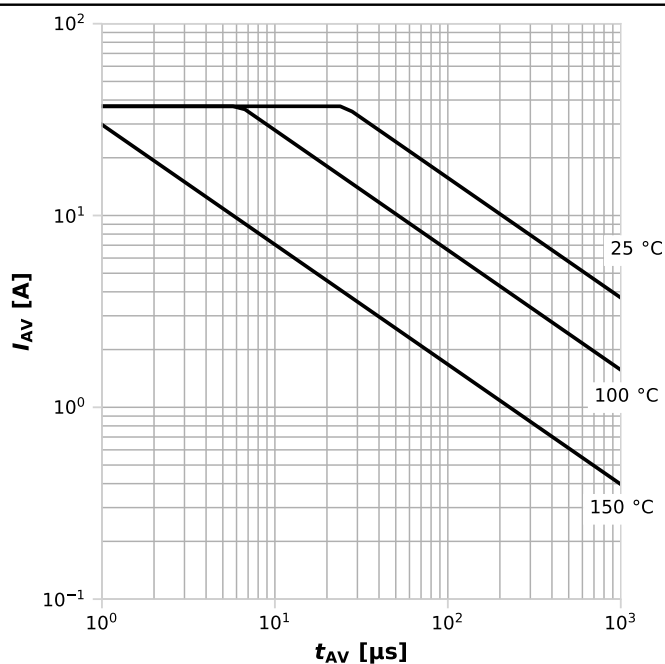
$$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 18: Typ. output energy



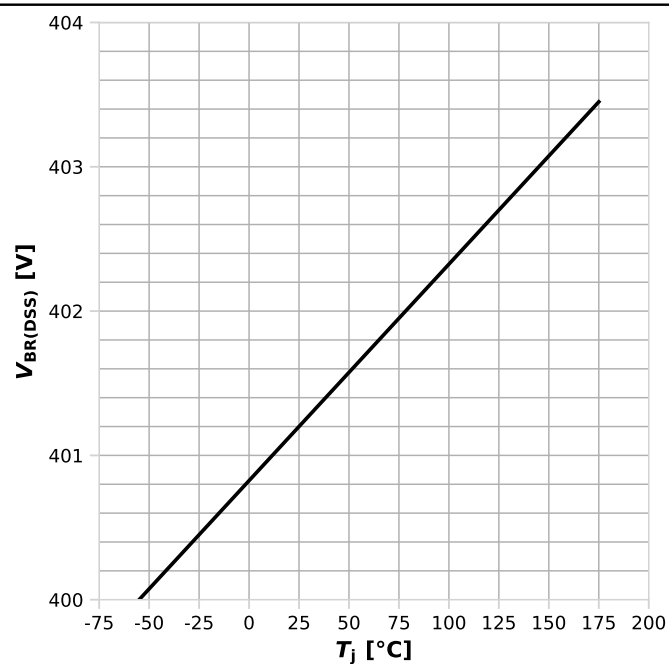
$$E_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 19: Avalanche characteristics



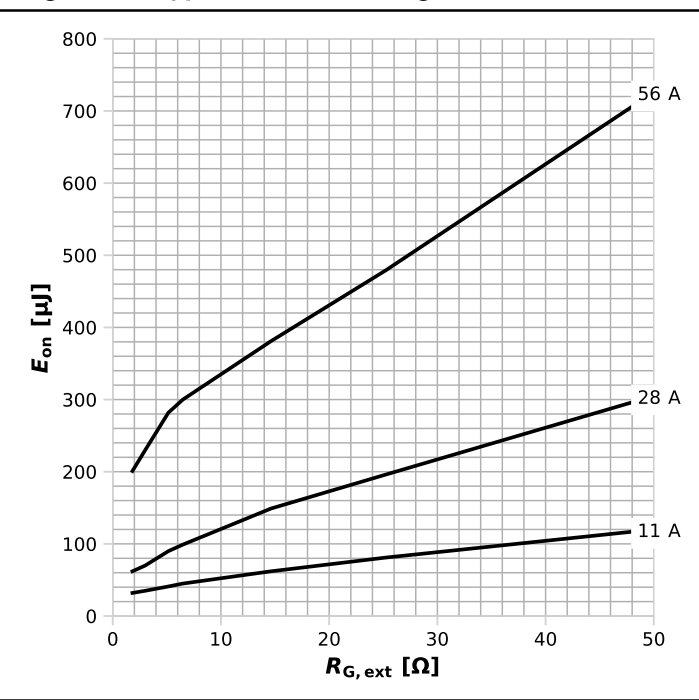
$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega; \text{parameter: } T_{j,\text{start}}$$

Diagram 20: Min. drain-source breakdown voltage



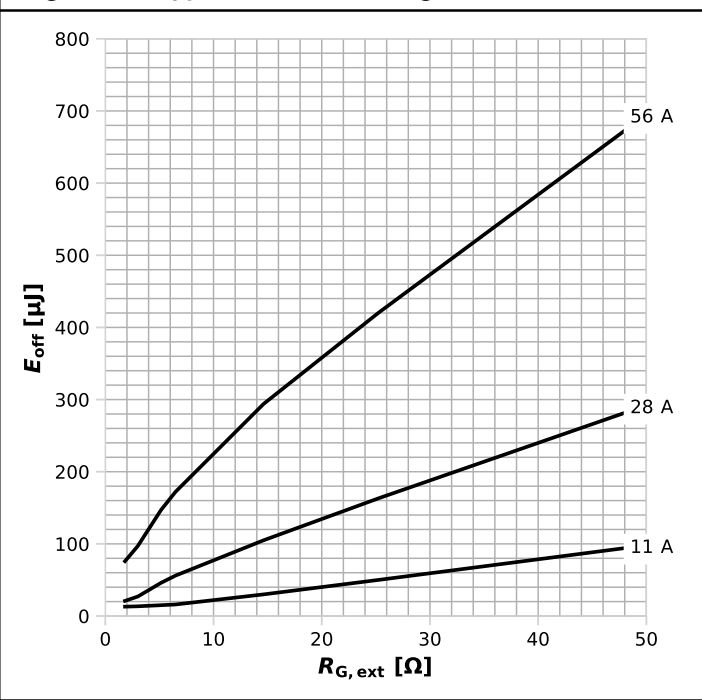
$$V_{BR(DSS)}=f(T_j); I_D=1.33\text{ mA}$$

Diagram 21: Typ. turn-on switching losses



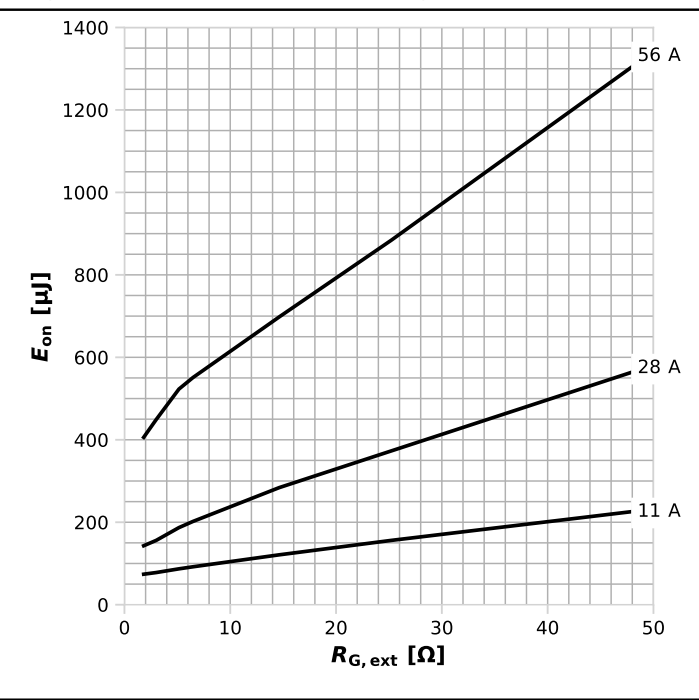
$E_{on}=f(R_{G,ext})$, $V_{DD}=200\text{ V}$, $V_G=0\ldots18\text{ V}$; parameter: I_D

Diagram 22: Typ. turn-off switching losses



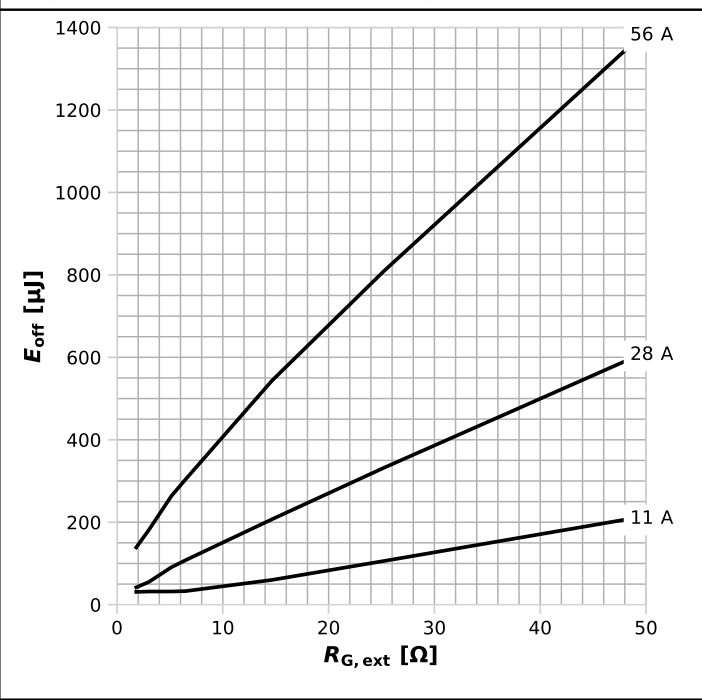
$E_{off}=f(R_{G,ext})$, $V_{DD}=200\text{ V}$, $V_G=18\ldots0\text{ V}$; parameter: I_D

Diagram 23: Typ. turn-on switching losses



$E_{on}=f(R_{G,ext})$, $V_{DD}=320\text{ V}$, $V_G=0\ldots18\text{ V}$; parameter: I_D

Diagram 24: Typ. turn-off switching losses



$E_{off}=f(R_{G,ext})$, $V_{DD}=320\text{ V}$, $V_G=18\ldots0\text{ V}$; parameter: I_D

6 Test circuits

Table 9 Switching times

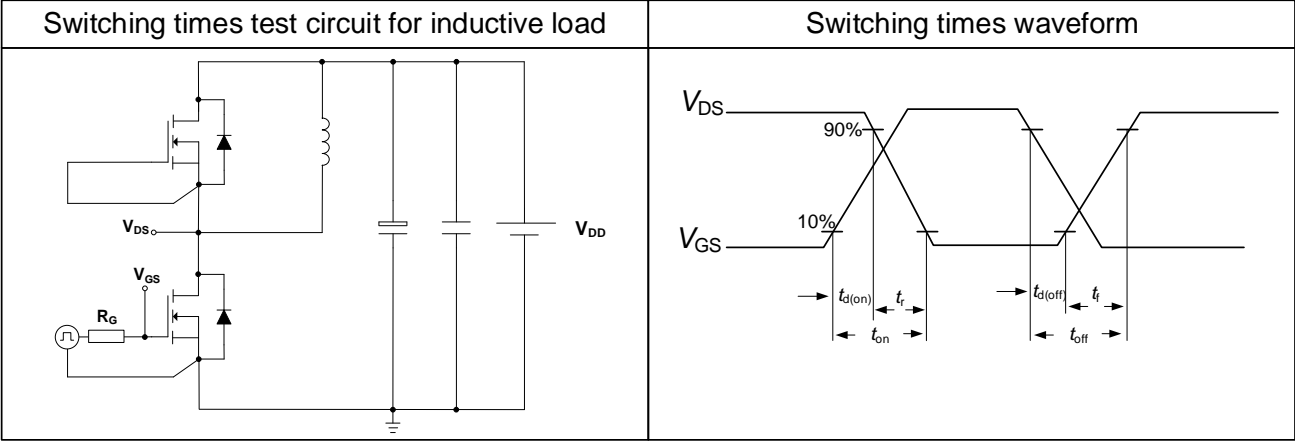
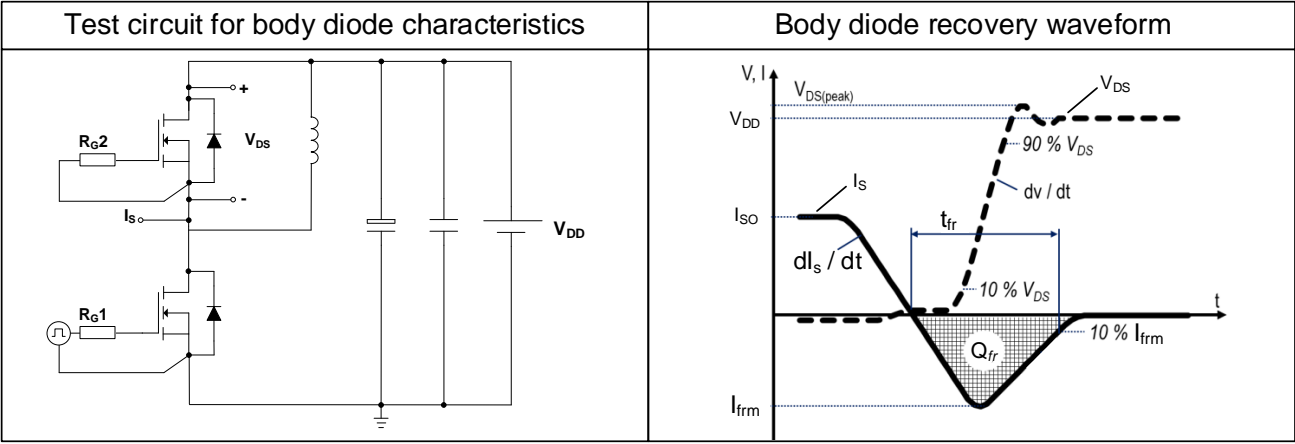
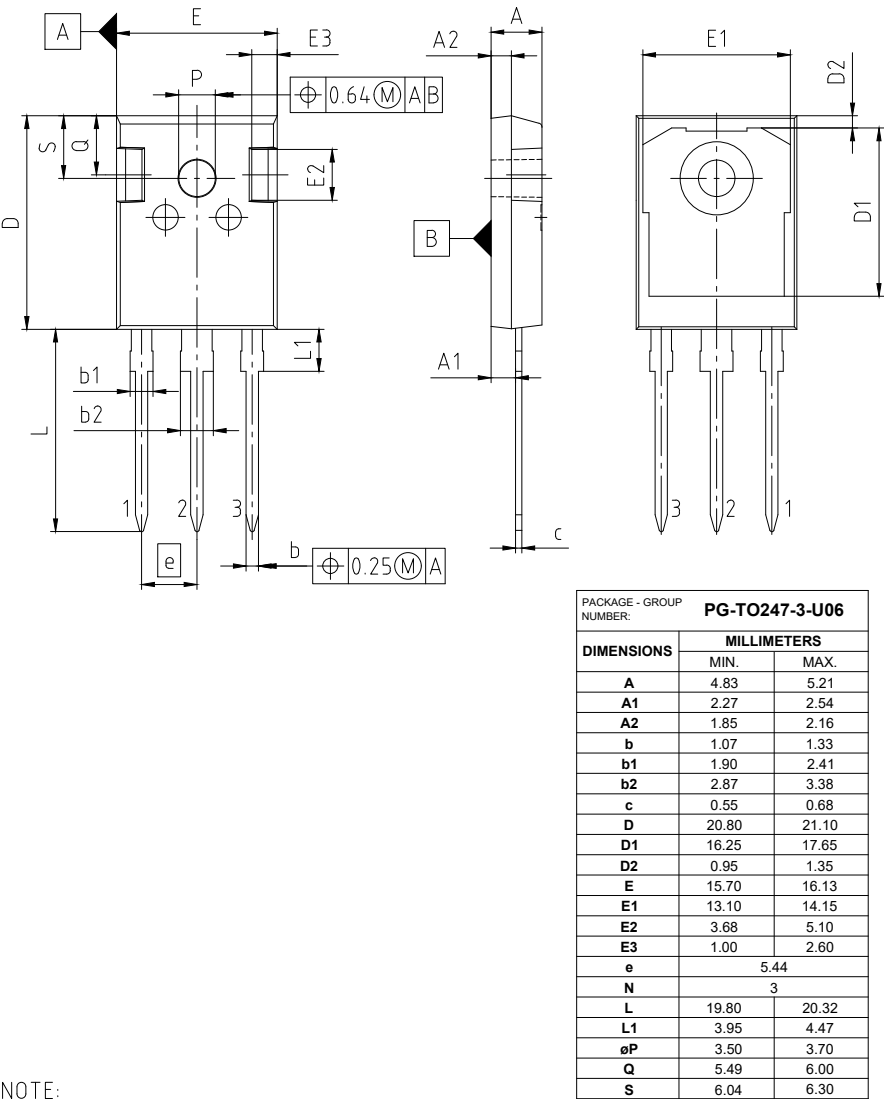


Table 10 Body diode characteristics

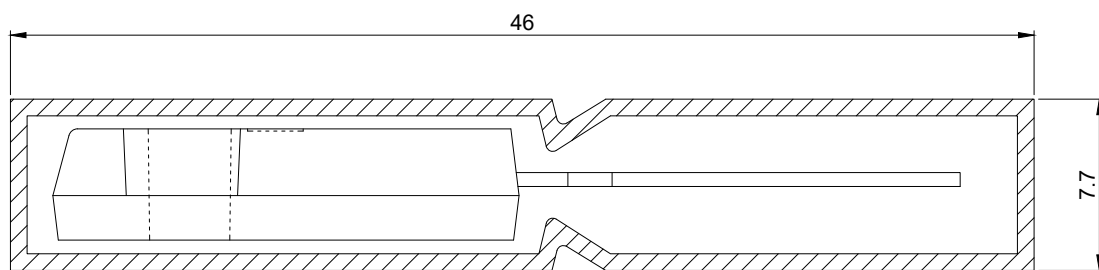


7 Package outlines



NOTE:
DIMENSIONS DO NOT INCLUDE MOLDFLASH; PROTRUSION OR GATE BURRS

Figure 1 Outline PG-T0247-3, dimensions in mm



All dimensions are in units mm


The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 2 Packaging variant PG-T0247-3, dimensions in mm

Revision history

IMW40R011M2H

Revision 2025-07-15, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-07-15	Release of final datasheet

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