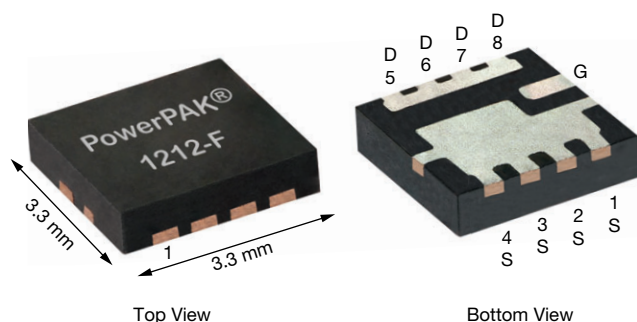


# N-Channel 40 V (D-S) MOSFET

**PowerPAK® 1212-F**


Top View

Bottom View

## PRODUCT SUMMARY

$V_{DS}$ (V)	40
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00207
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0031
$Q_g$ typ. (nC)	23
$I_D$ (A)	124 <sup>a</sup>
Configuration	Single

## FEATURES

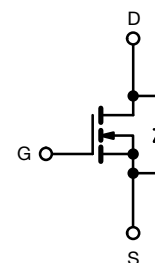
- TrenchFET® Gen IV power MOSFET
- Very low  $R_{DS} \times Q_g$  figure-of-merit (FOM)
- Source flip technology, enhance thermal performance
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
FREE

## APPLICATIONS

- DC/DC converter
- Synchronous rectification
- Battery management
- Oring and load switch



N-Channel MOSFET

## ORDERING INFORMATION

Package	PowerPAK 1212-F
Lead (Pb)-free and halogen-free	SiSD4402DN-T1-UE3

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	+20, -16	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	124
		$T_C = 70$ °C	99
		$T_A = 25$ °C	38 <sup>b, c</sup>
		$T_A = 70$ °C	31 <sup>b, c</sup>
Pulsed drain current ( $V_{GS} = 10$ V, $t = 100$ $\mu$ s)	$I_{DM}$	350	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	52
		$T_A = 25$ °C	4.9 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	33	
Single pulse avalanche energy	$E_{AS}$	53	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	57
		$T_C = 70$ °C	36
		$T_A = 25$ °C	5.4 <sup>b, c</sup>
		$T_A = 70$ °C	3.5 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SMYBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, f</sup>	$R_{thJA}$	18	23	°C/W
Maximum junction-to-case (source)	$R_{thJC}$	1.7	2.2	

### Notes

- Based on  $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-F is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 56 °C/W



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	26	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-5.5	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.1	-	2.4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	0.0017	0.00207	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	0.0023	0.0031	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A	-	145	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	3490	-	pF
Output capacitance	C <sub>oss</sub>		-	750	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	31	-	
C <sub>rss</sub> /C <sub>iss</sub> ratio			-	0.009	0.018	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	50	75	nC
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A	-	23	35	
Q <sub>gs</sub>	-		11	-		
Q <sub>gd</sub>	-		4.1	-		
Q <sub>oss</sub>	-	27	-			
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.18	0.9	1.8	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	12	25	ns
Rise time	t <sub>r</sub>		-	5	10	
Turn-off delay time	t <sub>d(off)</sub>		-	30	60	
Fall time	t <sub>f</sub>		-	5	10	
Turn-on delay time	t <sub>d(on)</sub>		-	27	60	
Rise time	t <sub>r</sub>	-	63	130		
Turn-off delay time	t <sub>d(off)</sub>	-	31	60		
Fall time	t <sub>f</sub>	-	9	20		
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	52	A
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>		-	-	350	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A	-	0.74	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	35	70	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	25	50	nC
Reverse recovery fall time	t <sub>a</sub>		-	18	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	17	-	

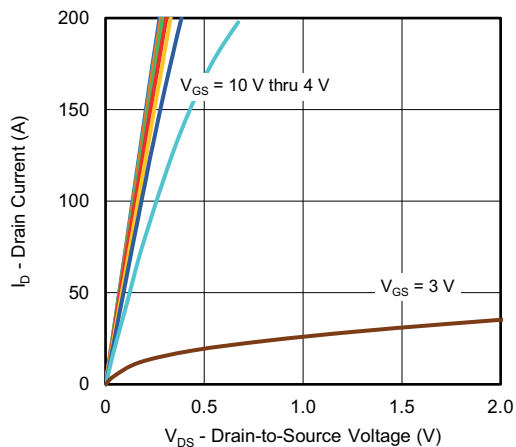
**Notes**

- a. Pulse test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Based on characterization, not subject to production testing

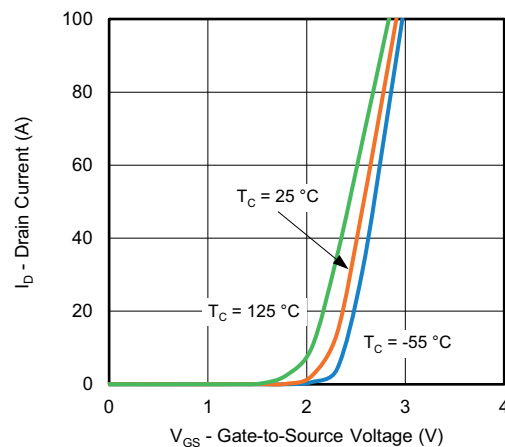
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



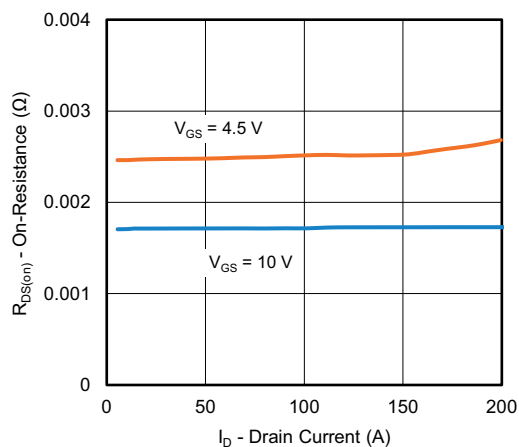
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



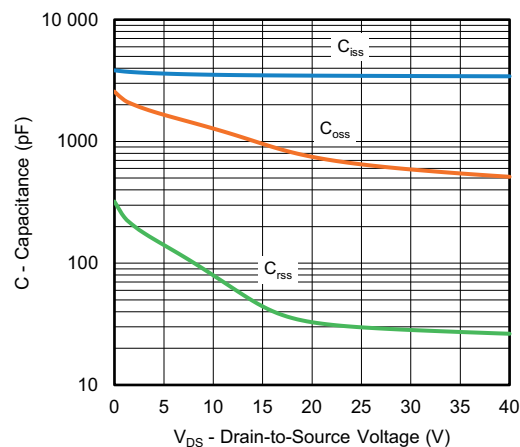
**Output Characteristics**



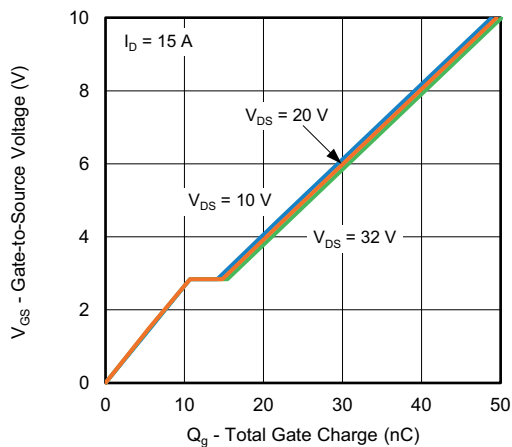
**Transfer Characteristics**



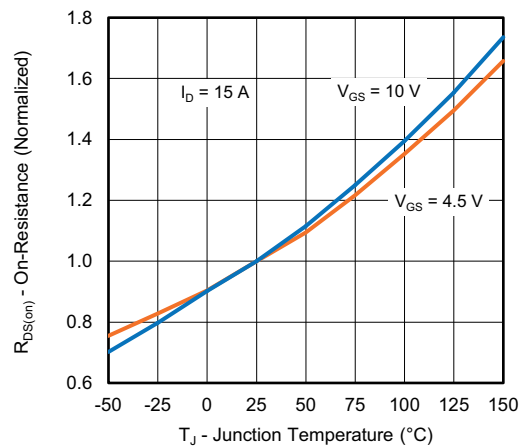
**On-Resistance vs. Drain Current**



**Capacitance**



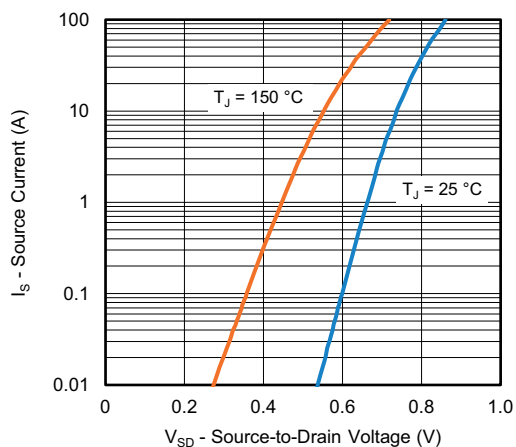
**Gate Charge**



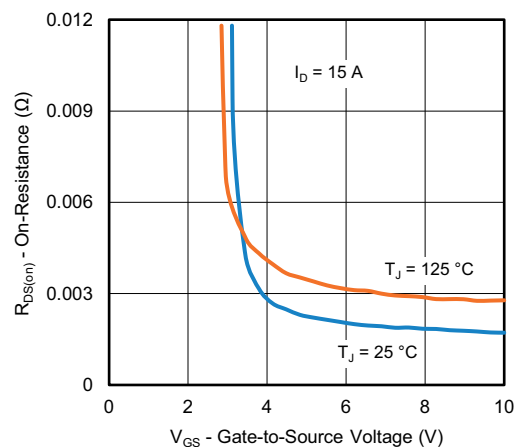
**On-Resistance vs. Junction Temperature**



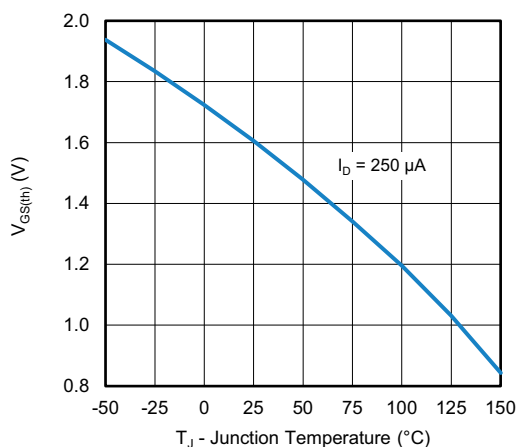
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



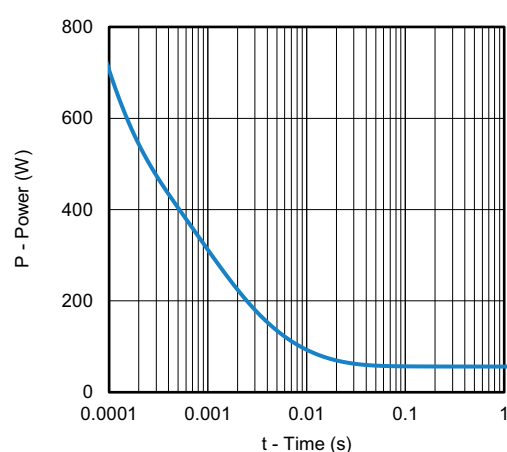
**Source-Drain Diode Forward Voltage**



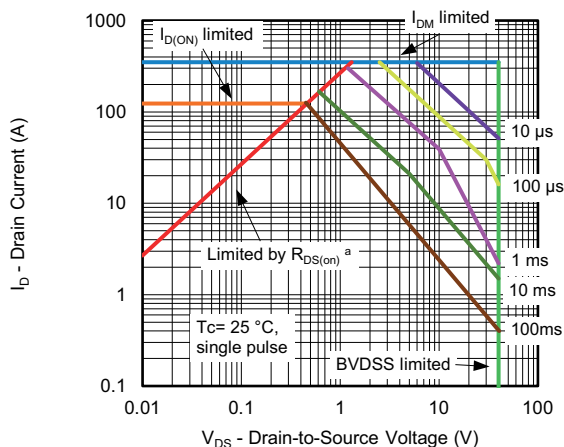
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Case**



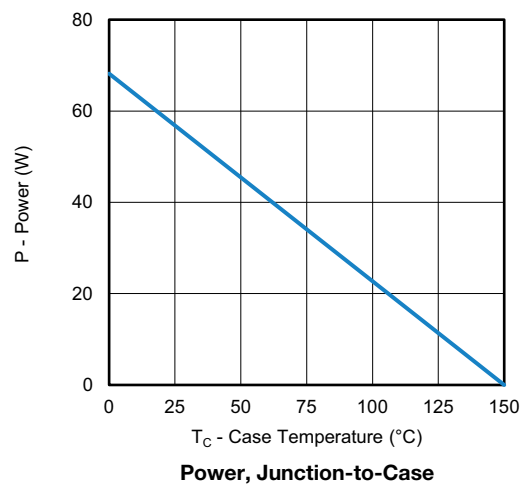
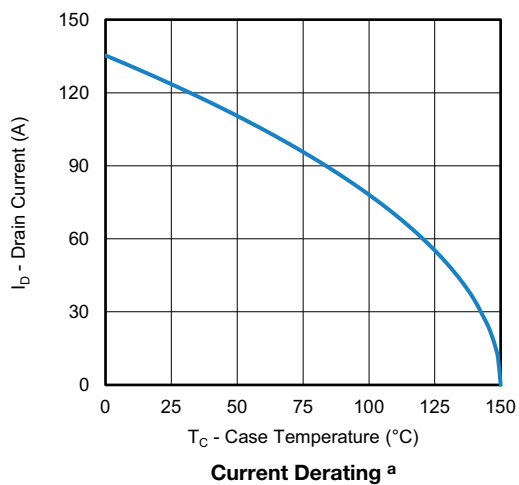
**Safe Operating Area**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

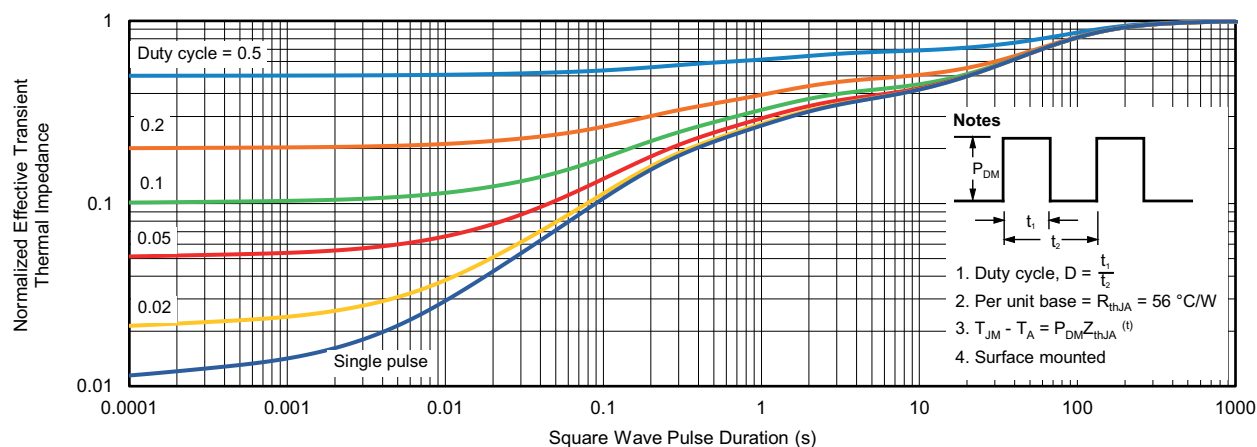


**Note**

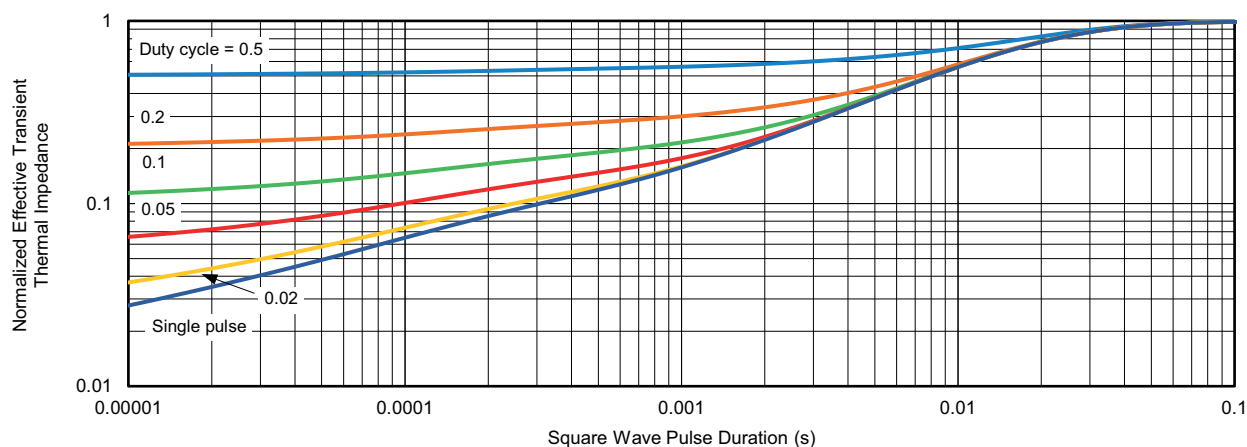
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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