

# MOSFET - Power, Single N-Channel, PQFN8 100 V, 7.6 mΩ, 110 A

# NTMFS7D8N10G

# **Features**

- Wide SOA for Linear Mode Operation
- Low R<sub>DS(on)</sub> to Minimize Conduction Loss
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (5x6 mm) for Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

# **Typical Applications**

• 48 V Hot Swap System, Load Switch, Soft Start, E-Fuse

# **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C, Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	100	٧
Gate-to-Source Voltag	Gate-to-Source Voltage			±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	Steady	7 7 0500	I <sub>D</sub>	110	Α
Power Dissipation R <sub>θJC</sub> (Note 2)	State	T <sub>C</sub> = 25°C	P <sub>D</sub>	187	W
Continuous Drain Current R <sub>0JA</sub> (Note 1, 2)	Steady State		I <sub>D</sub>	14	Α
Power Dissipation R <sub>θJA</sub> (Note 1, 2)	Olale		P <sub>D</sub>	3	W
Pulsed Drain Current	T <sub>A</sub> = 25°0	C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	1656	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	155	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>AV</sub> = 70 A, L = 0.1 mH)			E <sub>AS</sub>	245	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

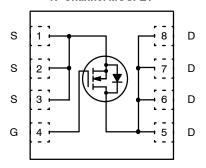
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

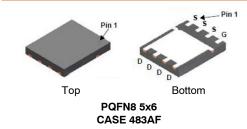
- 1. Surface-mounted on FR4 board using 1  $\rm in^2$  pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

1

V <sub>SSS</sub>	R <sub>SS(ON)</sub> MAX	I <sub>D</sub> MAX
100 V	7.6 mΩ @ 10 V	110 A

## **N-Channel MOSFET**





# **MARKING DIAGRAM**



7D8N10 = Specific Device Code A = Assembly Location Y = Year

Y = Year
W = Work Week
ZZ = Lot Traceability

# **ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

# THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{ heta JC}$	Junction-to-Case - Steady State	0.8	°C/W
$R_{ hetaJA}$	Junction-to-Ambient - Steady State	50	

Def   Characteristrics   Defin   Loss   V_{(BR)DSS}   V_{GS} = 0 V, I_D = 250 μA   100   100   V_{CRD}	ELECTRICAL CHARACTERISTICS	<b>3</b> (T <sub>J</sub> = 25°C un	ess otherwise noted)					
Drain - to - Source Breakdown Voltage   V <sub>(BR)DSS</sub>   V	Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
Drain – to — Source Breakdown Voltage Temperature Coefficient         V(BR)DSS / TJ $I_D = 250  \mu A$ , ref to $25^{\circ}C$ 87.9         mV/C           Zero Gate Voltage Drain Current         IDSS $V_{GS} = 0  V$ , $V_{DS} = 80  V$ $T_J = 25^{\circ}C$ 1 $\mu A$ Gate – to — Source Leakage Current         IGSS         VDS = 0 V, VDS = $\pm 20  V$ $\pm 100  O$ $\mu A$ OR CHARACTERISTICS (Note 3)         Gate Threshold Voltage         VGS(TH)         VGS = $\pm 100  V$ $\pm 100  O$	OFF CHARACTERISTICS							
Temperature Coefficient   Topic   T	Drain – to – Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100			V
Section	Drain – to – Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> / T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C			87.9		mV/°C
Section	Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V	T <sub>J</sub> = 25°C				μΑ
Continue	Gato to Source Leakage Current	1						nΛ
Gate Threshold Voltage         VGS(TH)         VGS = VDS, ID = 254 μA         2.0         4.0         V           Negative Threshold Temperature Coefficient         VGS(TH) / TJ         ID = 254 μA, ref to 25°C         -9.4         mV/°C           Drain – to – Source On Resistance         RDS(on)         VGS = 10 V, ID = 48 A         5.6         7.6         mQ           Forward Transconductance         9FS         VDS = 5 V, ID = 48 A         37         S         S           Gate – Resistance         RG         TA = 25°C         0.33         Ω         Ω           CHARGES & CAPACITANCES           Input Capacitance         CISS         VGS = 0 V, I = 1 MHz, VDS = 50 V         6180         pF           Output Capacitance         COSS         VGS = 0 V, I = 1 MHz, VDS = 50 V         624.5         PF           Reverse Transfer Capacitance         CRSS         99         nC         nC           Gate - to – Drain Charge         QGB         VGS = 10 V, VDS = 50 V, ID = 48 A         26         P           Plateau Voltage         VGB         40         40         V         V           WITCHING CHARACTERISTICS (Note 3)         VGS = 10 V, VDS = 50 V, ID = 48 A         32         ns           Turn – On Delay Time         t <sub>1</sub> VGS =		IGSS	v <sub>DS</sub> = 0 v, v <sub>GS</sub> =	1 120 V			±100	IIA
Negative Threshold Temperature   VGS(TH)   TJ   ID = 254 μA, ref to 25°C   -9.4   mV/FC   Coefficient			\ \ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	254 . 4	0.0		4.0	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$v_{GS} = v_{DS}$ , $I_D = 2$	254 μΑ	2.0		4.0	
Forward Transconductance $g_{FS}$ $V_{DS} = 5 \text{ V}$ , $I_D = 48 \text{ A}$ 37         S           Gate-Resistance         R <sub>G</sub> $T_A = 25^{\circ}\text{C}$ 0.33         Ω           CHARGES & CAPACITANCES           Input Capacitance $C_{ISS}$ $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{DS} = 50 \text{ V}$ 6180         pF           Output Capacitance $C_{ISS}$ $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{DS} = 50 \text{ V}$ 624.5         99           Total Gate Charge $Q_{GS}$ $Q_{G(TOT)}$ 92         nC           Gate-to-Source Charge $Q_{GS}$ $Q_{GD}$ 35         26           Plateau Voltage $V_{GS}$ $V_{CS} = 10 \text{ V}$ , $V_{DS} = 50 \text{ V}$ , $I_{D} = 48 \text{ A}$ 32         ns           WITCHING CHARACTERISTICS (Note 3) $V_{GS} = 10 \text{ V}$ , $V_{DS} = 50  $		V <sub>GS(TH)</sub> <sup>/</sup> T <sub>J</sub>	I <sub>D</sub> = 254 μA, ref t	o 25°C		-9.4		mV/°C
Comparison   Co	Drain - to - Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 48 A			5.6	7.6	mΩ
CHARGES & CAPACITANCES         Input Capacitance $C_{ISS}$ $V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}, V_{DS} = 50 \text{ V}$ 6180         pF           Output Capacitance $C_{OSS}$ $V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}, V_{DS} = 50 \text{ V}$ 624.5         pF           Reverse Transfer Capacitance $C_{RSS}$ 99         nC           Total Gate Charge $Q_{GITOT}$ 92         nC           Gate—to—Source Charge $Q_{GS}$ 35         26           Plateau Voltage $V_{GP}$ 26         V           WITCHING CHARACTERISTICS (Note 3)         Turn—On Delay Time $t_{d(ON)}$ 32         ns           Rise Time $t_r$ $V_{GS} = 10 \text{ V}, V_{DS} = 50  V$	Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 48 A			37		S
Disput Capacitance	Gate-Resistance	$R_{G}$	T <sub>A</sub> = 25°C			0.33		Ω
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	CHARGES & CAPACITANCES							
Reverse Transfer Capacitance   C <sub>RSS</sub>   99   10   10   10   10   10   10   10	Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 50 V			6180		pF
Total Gate Charge $Q_{G(TOT)}$ $Q_{GS}$ $Q_{GS$	Output Capacitance	C <sub>OSS</sub>				624.5		
Gate-to-Source Charge   Q <sub>GS</sub>   Q <sub>GD</sub>   V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 48 A   26   26   26   26   26   26   26	Reverse Transfer Capacitance	C <sub>RSS</sub>				99		
	Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 48 A			92		nC
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-to-Source Charge	Q <sub>GS</sub>				35		1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-to-Drain Charge	$Q_{GD}$				26		1
Turn – On Delay Time $t_{d(ON)}$ $V_{GS} = 10 \text{ V}, V_{DS} = 50 \text{ V}, V_{DS} = 48 \text{ A}, V_{DS} = 48$	Plateau Voltage	$V_{GP}$				6		V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	SWITCHING CHARACTERISTICS (Note	3)						·•
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn – On Delay Time	t <sub>d(ON)</sub>				32		ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Rise Time		Voc = 10 V Vpc	- 50 V		24		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn – Off Delay Time	t <sub>d(OFF)</sub>				51		1
Forward Diode Voltage $V_{SD} = V_{SS} = 0 \text{ V, } I_S = 48 \text{ A} $ $V_{GS} = 0 \text{ V, } I_S = 48 \text{ A} $ $T_J = 25^{\circ}\text{C}                                   $	Fall Time					14		1
$V_{GS} = 0 \text{ V, } I_S = 48 \text{ A} $ $T_J = 125^{\circ}\text{C} $ $0.73$ Reverse Recovery Time $ t_{RR} $ $V_{GS} = 0 \text{ V, } dI_S/dt = 300 \text{ A/$\mu$s}, $ $I_S = 24 \text{ A} $ $177 $ $nC$ Reverse Recovery Time $ t_{RR} $ $V_{GS} = 0 \text{ V, } dI_S/dt = 1000 \text{ A/$\mu$s}, $ $33 $ $ns$	DRAIN-SOURCE DIODE CHARACTER	ISTICS						
$V_{GS} = 0 \text{ V, } I_S = 48 \text{ A} $ $T_J = 125^{\circ}\text{C} $ $0.73$ Reverse Recovery Time $ t_{RR} $ $V_{GS} = 0 \text{ V, } dI_S/dt = 300 \text{ A/$\mu$s}, $ $I_S = 24 \text{ A} $ $177 $ $nC$ Reverse Recovery Time $ t_{RR} $ $V_{GS} = 0 \text{ V, } dI_S/dt = 1000 \text{ A/$\mu$s}, $ $33 $ $ns$	Forward Diode Voltage	$V_{SD}$	T. <sub>1</sub> = 25°C 0.84	0.84		V		
Reverse Recovery Charge $Q_{RR}$ $I_S = 24 \text{ A}$ 177 nC Reverse Recovery Time $t_{RR}$ $V_{GS} = 0 \text{ V, dI}_S/\text{dt} = 1000 \text{ A/µs},$ 33 ns	Ü		$V_{GS} = 0 \text{ V}, I_{S} = 48 \text{ A}$			0.73		V mV/°C mΩ S Ω Ω PF NC V
Reverse Recovery Charge $Q_{RR}$ $I_S = 24 \text{ A}$ 177 nC Reverse Recovery Time $t_{RR}$ $V_{GS} = 0 \text{ V, dI}_S/\text{dt} = 1000 \text{ A/µs},$ 33 ns	Reverse Recovery Time	t <sub>RR</sub>	Voo - 0 V dlo/dt - 1	300 A/us		42		ns
Reverse Recovery Time $t_{RR}$ $V_{GS} = 0 \text{ V, } dI_S/dt = 1000 \text{ A/}\mu\text{s,}$ 33 ns	·		V <sub>GS</sub> = 0 V, αι <sub>S</sub> /αι = 300 Α/μs, I <sub>S</sub> = 24 Α			177		nC
V <sub>G</sub> S = 0 V, αις/αι = 1000 / γ(ιο,	Reverse Recovery Time					33		ns
	Reverse Recovery Charge					411		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

# **TYPICAL CHARACTERISTICS**

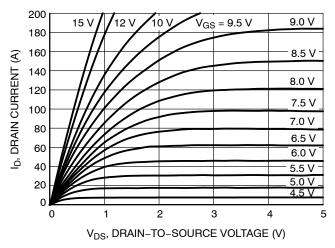


Figure 1. On-Region Characteristics

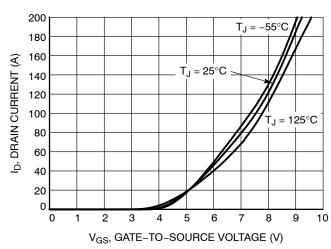


Figure 2. Transfer Characteristics

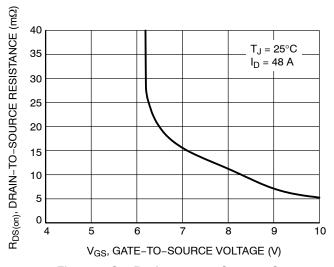


Figure 3. On-Resistance vs. Gate-to-Source Voltage

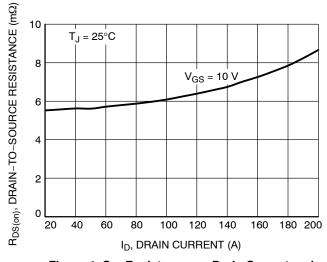


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

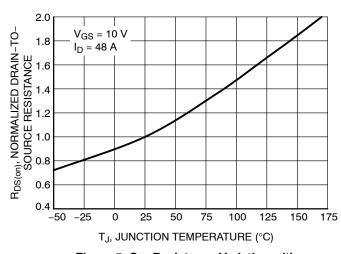


Figure 5. On–Resistance Variation with Temperature

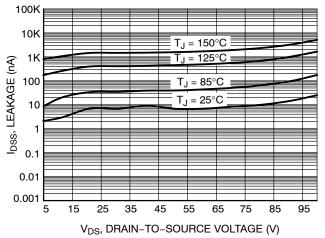


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL CHARACTERISTICS**

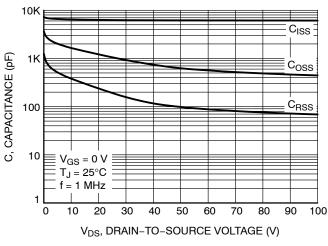


Figure 7. Capacitance Variation

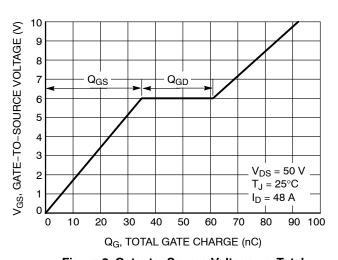


Figure 8. Gate-to-Source Voltage vs. Total Charge

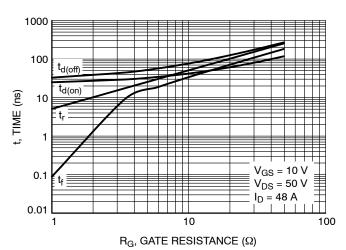


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

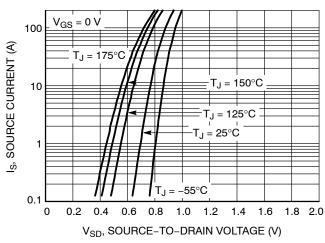


Figure 10. Diode Forward Voltage vs. Current

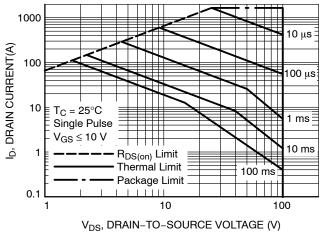


Figure 11. Maximum Rated Forward Biased Safe Operating Area

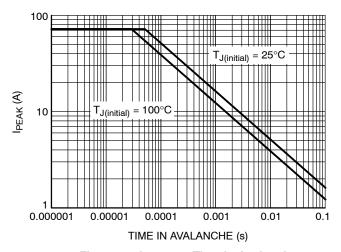


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

# **TYPICAL CHARACTERISTICS**

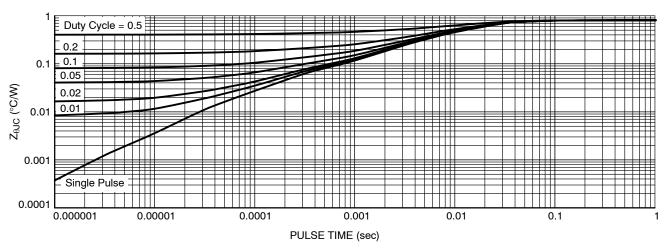


Figure 13. Thermal Characteristics

# **ORDERING INFORMATION**

Device	Device Marking	Package	Shipping <sup>†</sup>
NTMFS7D8N10GTWG	7D8N10	PQFN8 5x6 (Pb–Free/Halogen Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



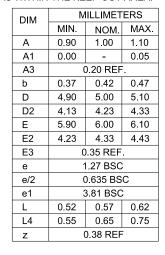


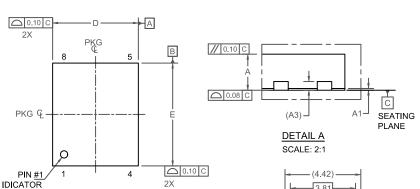
# PQFN8 5X6, 1.27P CASE 483AF ISSUE A

**DATE 06 JUL 2021** 

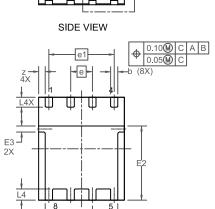
NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.





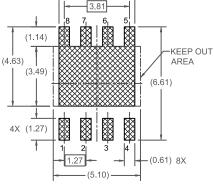
SEE DETAIL A



e/2

**BOTTOM VIEW** 

TOP VIEW



LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5X6, 1.27P		PAGE 1 OF 1	

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