



## Description

The PMV33UPE uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

## General Features

$V_{DS} = -20V, I_D = -5A$

$R_{DS(ON)} < 40m\Omega @ V_{GS} = -4.5V$

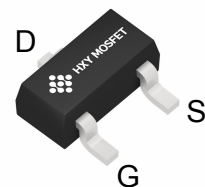
$R_{DS(ON)} < 60m\Omega @ V_{GS} = -2.5V$

ESD Rating: 1500V HBM

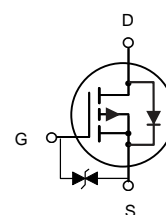
## Application

PWM application

Load switch



SOT-23



P-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
PMV33UPE	SOT-23	3415/AF4E	3000

## Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 10$	V
$I_D$	Drain Current-Continuous	-5	A
$I_{DM}$	Drain Current-Pulsed (Note 1)	-30	A
$P_D$	Maximum Power Dissipation	1.4	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	89.3	$^\circ C/W$



**Electrical Characteristics (TA=25 °C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-20		-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.35	-0.55	-0.9	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	-	30	40	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4A	-	44	60	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4A	8	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, F=1.0MHz	-	950	-	PF
Output Capacitance	C <sub>oss</sub>		-	165	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	120	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-10V, R <sub>L</sub> =2. 5Ω V <sub>GS</sub> =-4.5V, R <sub>GEN</sub> =3Ω	-	12		nS
Turn-on Rise Time	t <sub>r</sub>		-	10		nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	19		nS
Turn-Off Fall Time	t <sub>f</sub>		-	25		nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-4A, V <sub>GS</sub> =-4.5V	-	12		nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-4A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-4	A

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production



## Typical Electrical And Thermal Characteristics

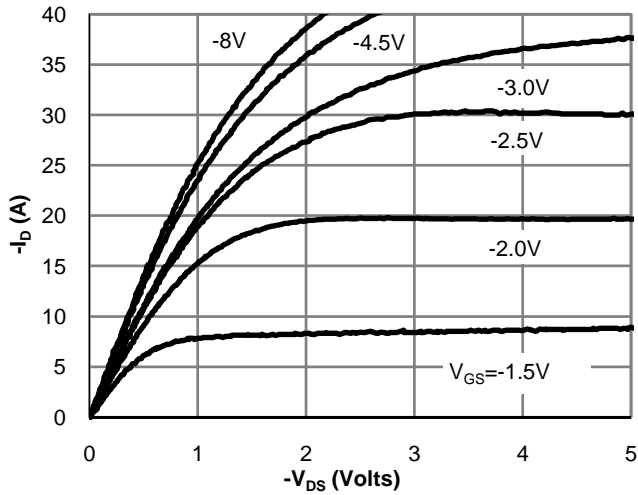


Fig 1: On-Region Characteristics (Note E)

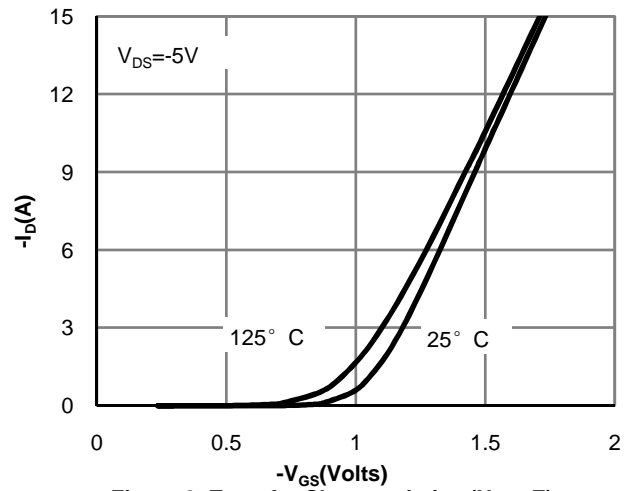


Figure 2: Transfer Characteristics (Note E)

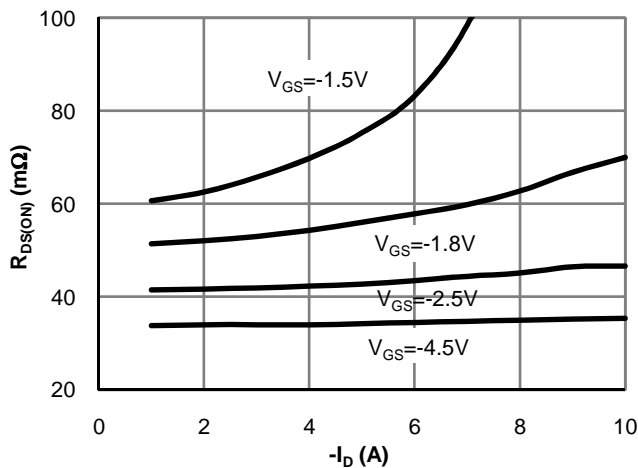


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

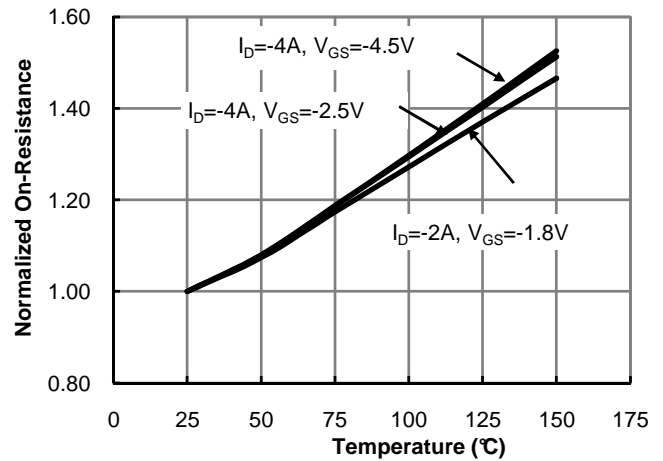


Figure 4: On-Resistance vs. Junction Temperature (Note E)

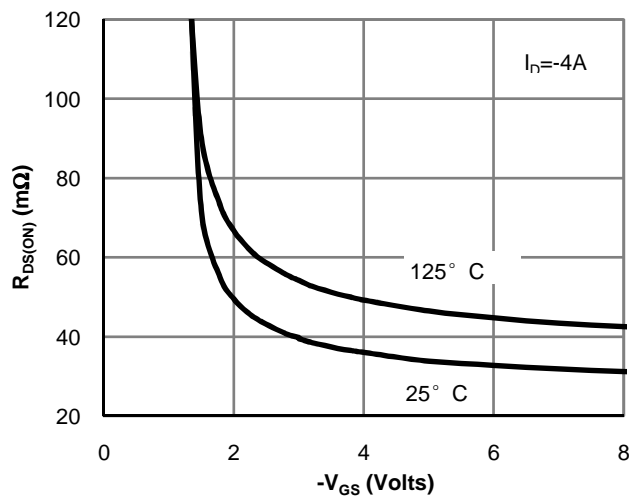


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

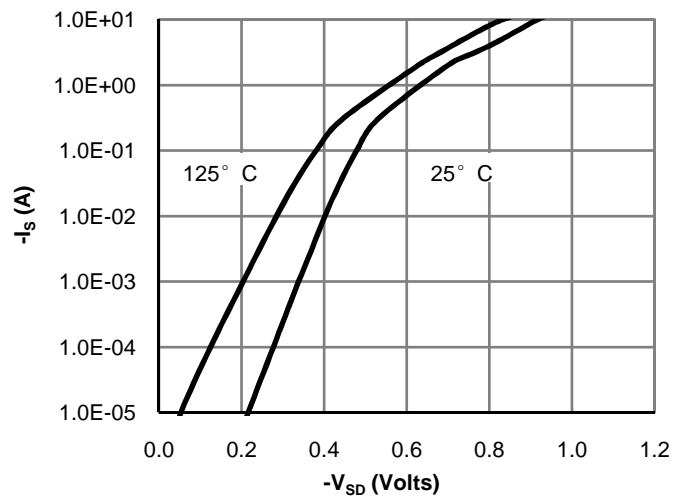


Figure 6: Body-Diode Characteristics (Note E)

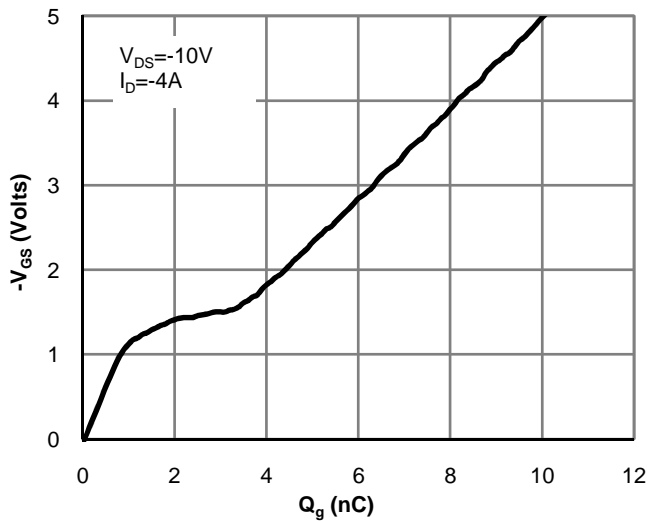


Figure 7: Gate-Charge Characteristics

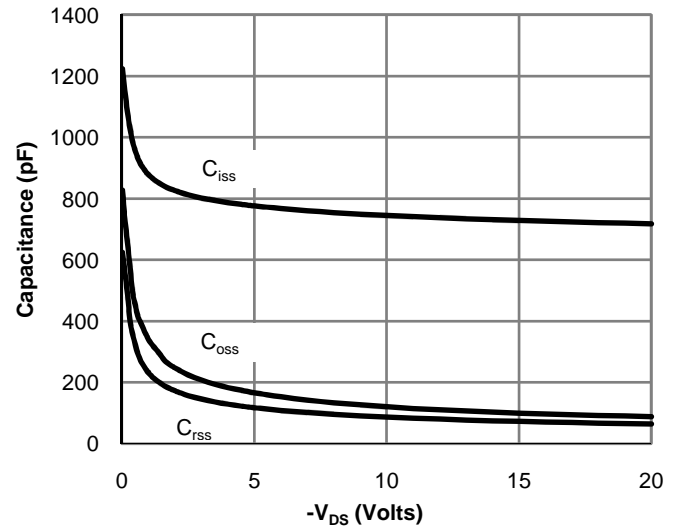


Figure 8: Capacitance Characteristics

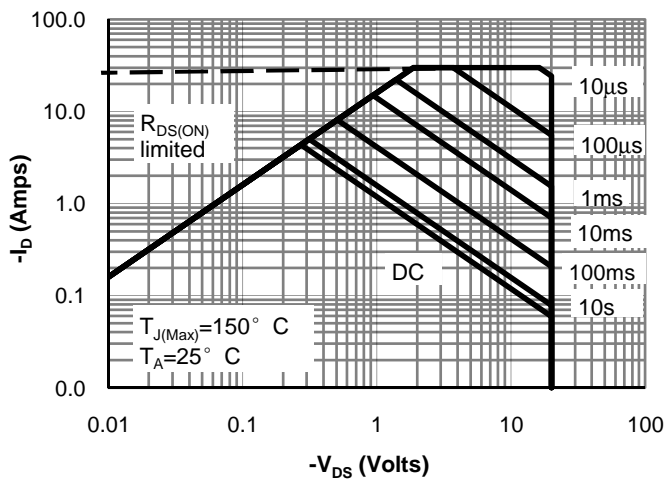


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

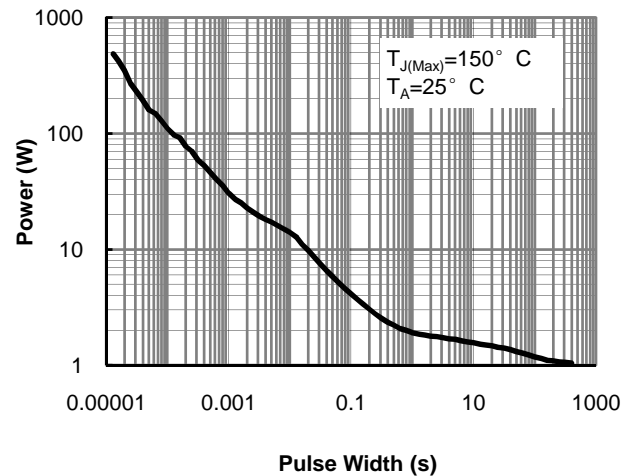


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

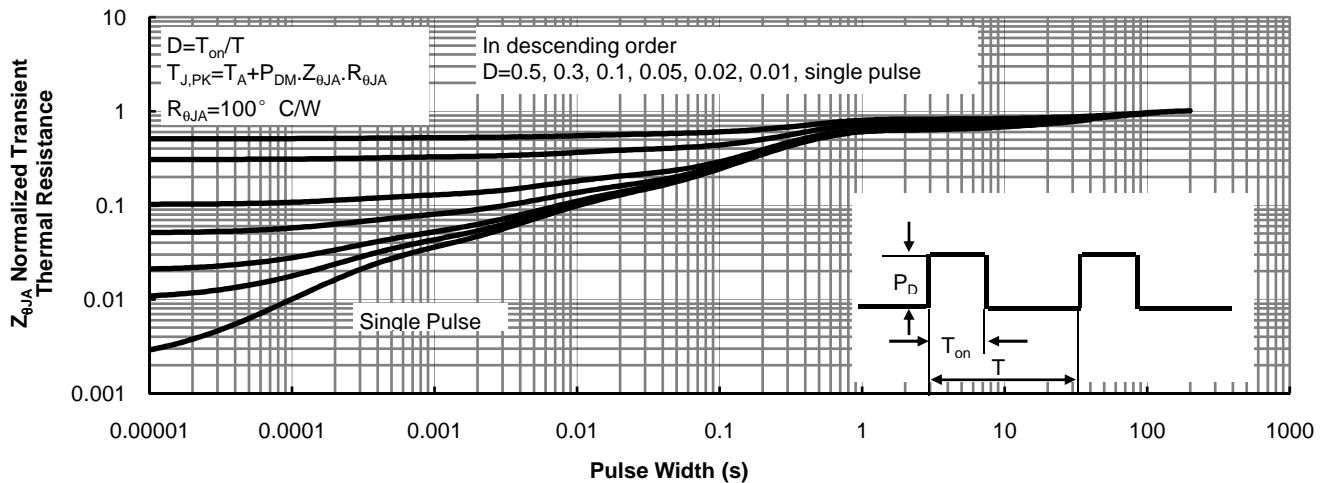
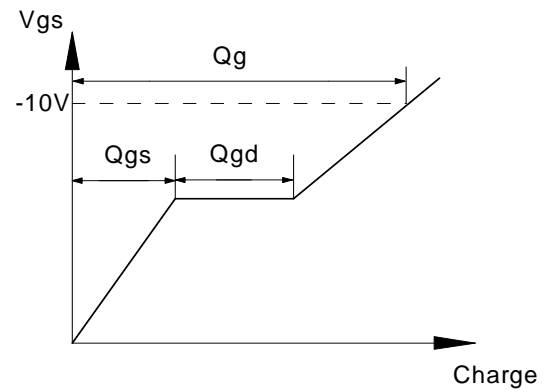
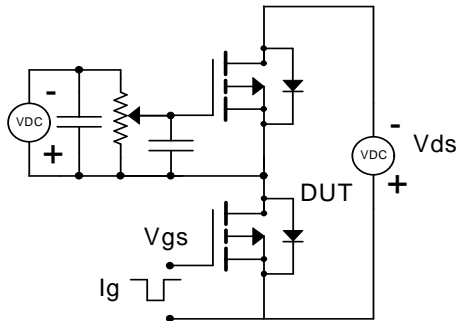


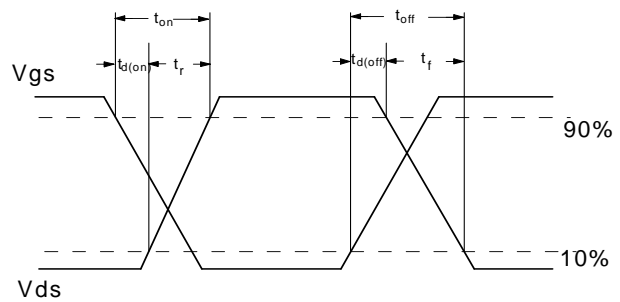
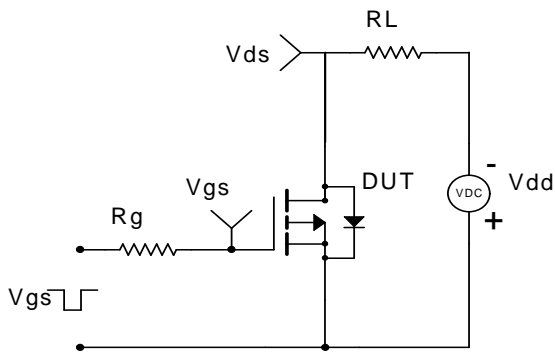
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



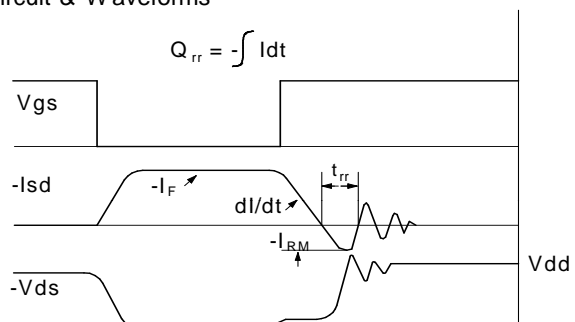
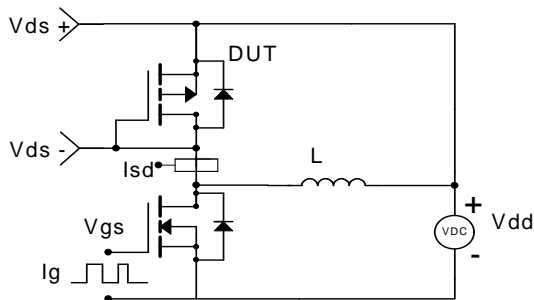
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

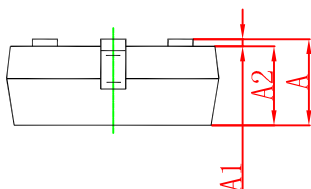
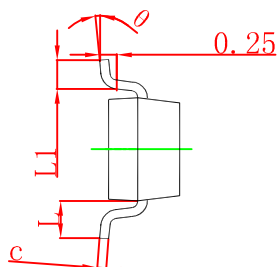
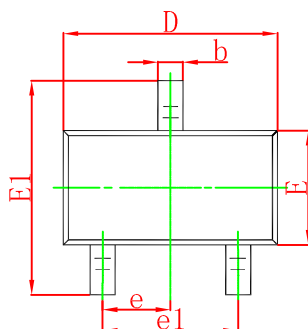


Diode Recovery Test Circuit & Waveforms



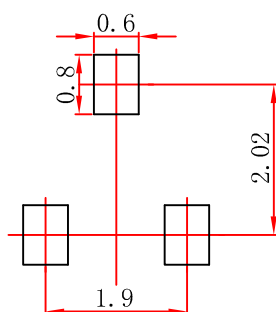


## SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

## SOT-23 Suggested Pad Layout



Note:  
1. Controlling dimension: in millimeters.  
2. General tolerance:  $\pm 0.05\text{mm}$ .  
3. The pad layout is for reference purposes only.



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