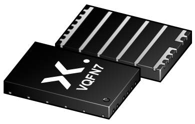


GANE3R9-150QBA

150 V, 3.9 mOhm Gallium Nitride (GaN) FET in a 4.0 mm x 6.0 mm Very-Thin-Profile Quad Flat No-Lead Package (VQFN)

30 April 2024 **Product data sheet**

1. General description

The GANE3R9-150QBA is a a general purpose 150 V, 3.9 mΩ Gallium Nitride (GaN) FET in a Very-Thin-Profile Quad Flat No-Lead Package (VQFN) package. It is a normally-off e-mode device offering superior performance and very low on-state resistance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Very-Thin-Profile Quad Flat No-Lead Package (VQFN) 4.0 mm x 6.0 mm

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, (secondary stage)
- High frequency DC-to-DC converters in 48 V systems
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- LiDAR (non-automotive)
- Class D audio amplifiers

4. Quick reference data

Table 1. Quick reference data

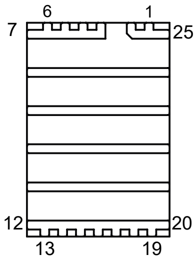
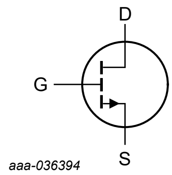
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-40 °C ≤ T_j ≤ 150 °C		-	-	150	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C		-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	65	W
T_j	junction temperature			-40	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 30 A; T_j = 25 °C; Fig. 8; Fig. 9		-	3.2	3.9	mΩ
		V_{GS} = 5 V; I_D = 30 A; T_j = 150 °C; Fig. 8; Fig. 10		-	7	-	mΩ
R_G	gate resistance	f = 5 MHz		-	1.9	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 30 A; V_{DS} = 75 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 11; Fig. 12		-	3.5	-	nC
$Q_{G(tot)}$	total gate charge			-	20	-	nC
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 75 V; Fig. 15	[1]	-	130	-	nC

[1] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1,2,25	G	gate	 Transparent top view **VQFN7 (SOT8091-1)**	
3-7,9,11, 21,23	S	source		
8,10,12-20,22,24	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANE3R9-150QBA	VQFN7	very thin quad flatpack; no leads	SOT8091-1

7. Marking

Table 4. Marking codes

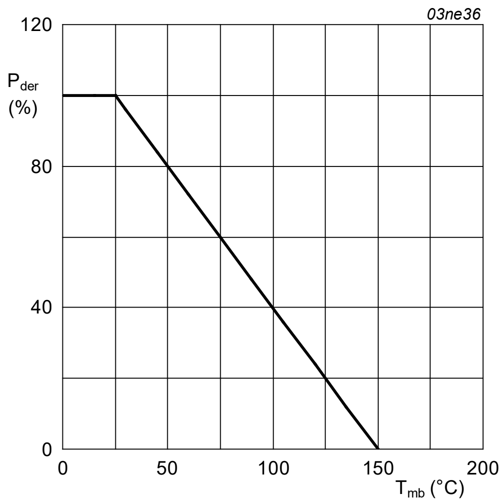
Type number	Marking code
GANE3R9-150QBA	3R9EQBA

8. Limiting values

Table 5. Limiting values

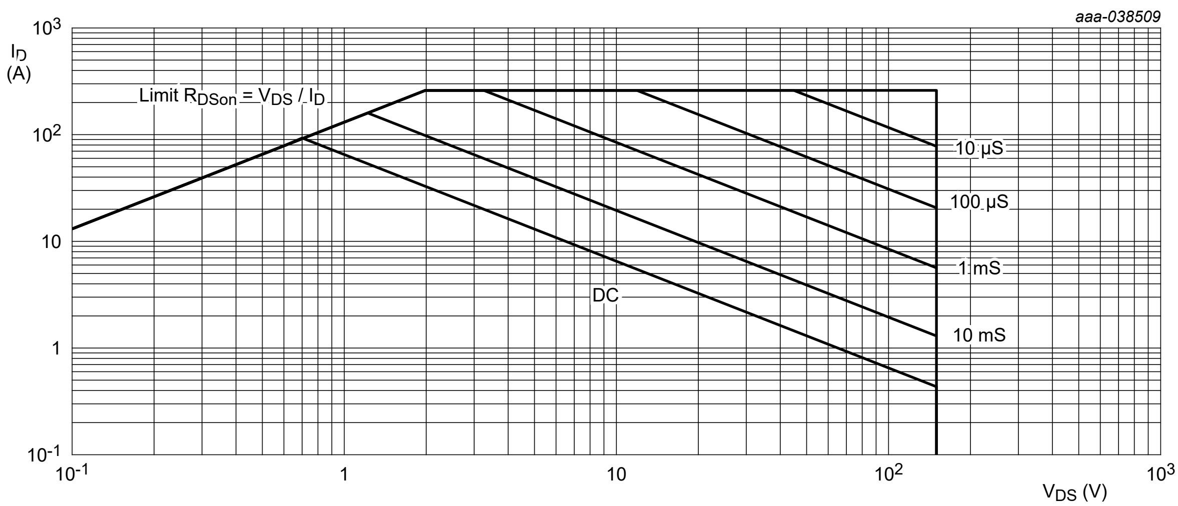
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-40 °C ≤ T_j ≤ 150 °C		-	150	V
V_{GS}	gate-source voltage			-4	6	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	65	W
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C		-	100	A
I_{DM}	peak drain current	pulsed; t_p = 100 µs; T_{mb} = 25 °C; Fig. 2		-	260	A
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-40	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case			-	13.96	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3		-	1.92	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	57.56	-	K/W

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

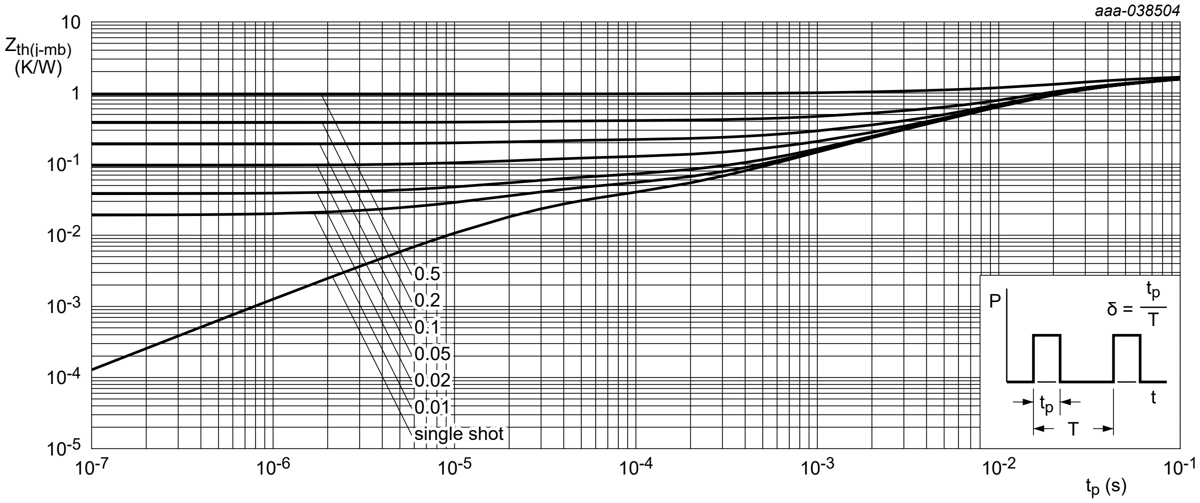


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 12 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 7		0.8	1.1	2.1	V
		I_D = 12 mA; V_{DS}=V_{GS}; T_j = 150 °C; Fig. 7		-	1	-	V
I_{DSS}	drain leakage current	V_{DS} = 150 V; V_{GS} = 0 V; T_j = 25 °C		-	2	150	µA
I_{GSS}	gate leakage current	V_{GS} = 5 V; T_j = 25 °C		-	2	100	µA
		V_{GS} = 6 V; T_j = 25 °C		-	6	1000	µA
		V_{GS} = -4 V; T_j = 25 °C		-	0.1	100	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 30 A; T_j = 25 °C; Fig. 8; Fig. 9		-	3.2	3.9	mΩ
		V_{GS} = 5 V; I_D = 30 A; T_j = 150 °C; Fig. 8; Fig. 10		-	7	-	mΩ
R_G	gate resistance	f = 5 MHz		-	1.9	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 30 A; V_{DS} = 75 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 11; Fig. 12		-	20	-	nC
Q_{GS}	gate-source charge			-	5	-	nC
Q_{GD}	gate-drain charge			-	3.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 30 A; V_{DS} = 75 V		-	2	-	V
C_{iss}	input capacitance	V_{DS} = 75 V; V_{GS} = 0 V; f = 100 kHz; T_j = 25 °C; Fig. 13		-	2200	-	pF
C_{oss}	output capacitance			-	900	-	pF
C_{rss}	reverse transfer capacitance			-	10.5	-	pF
$C_{o(er)}$	effective output capacitance, energy related	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 14		-	1300	-	pF
$C_{o(tr)}$	effective output capacitance, time related	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C		-	1700	-	pF
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 75 V; Fig. 15	[1]	-	130	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 0.5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16; Fig. 17; Fig. 18; Fig. 19		-	1.5	-	V

[1] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since Q_r = Q_{oss} + Q_D, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

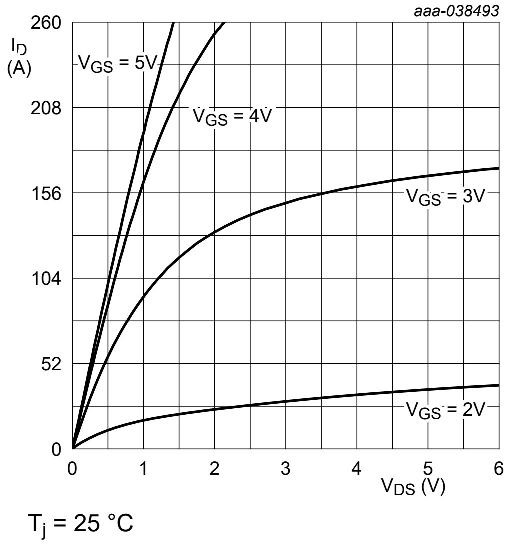


Fig. 4. Output characteristics: drain current as a function of drain-source voltage; typical values

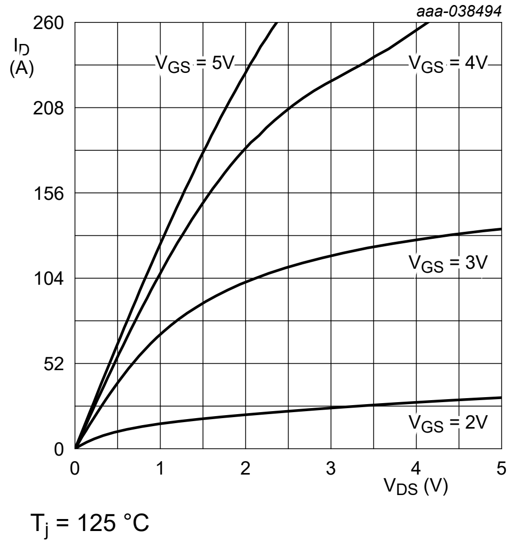


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

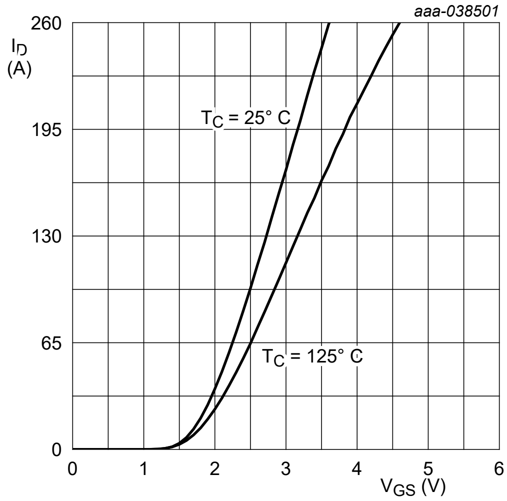


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

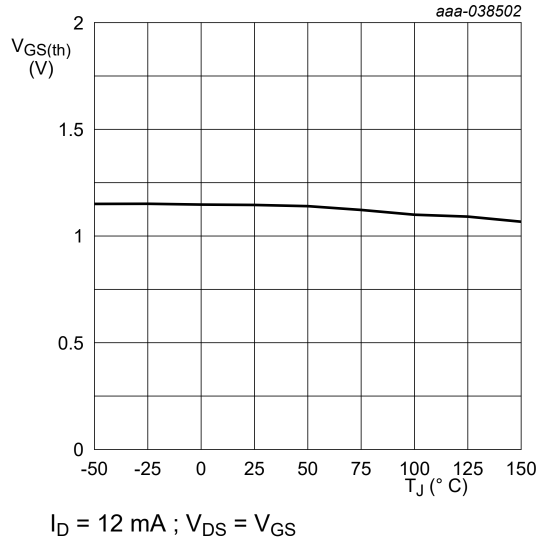
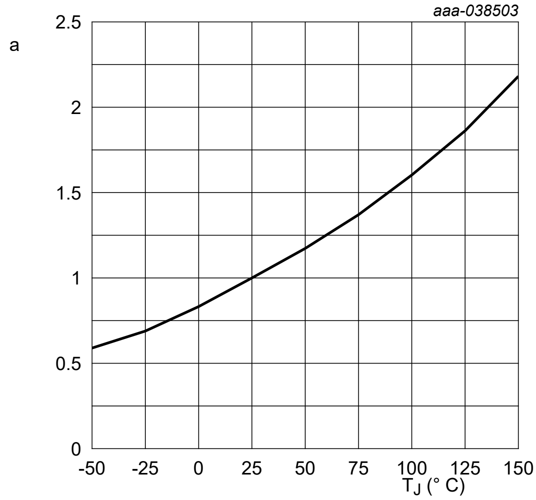
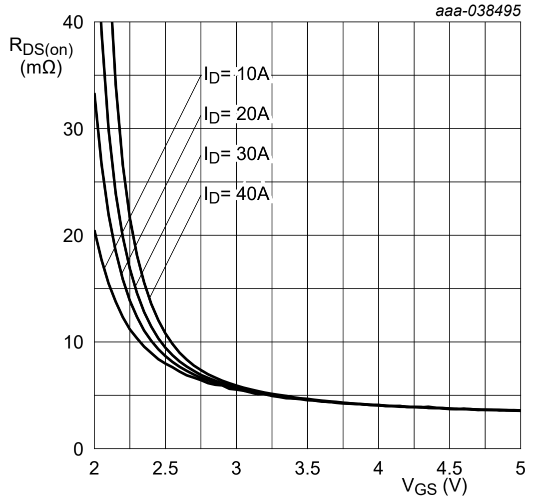


Fig. 7. Gate-source threshold voltage as a function of junction temperature



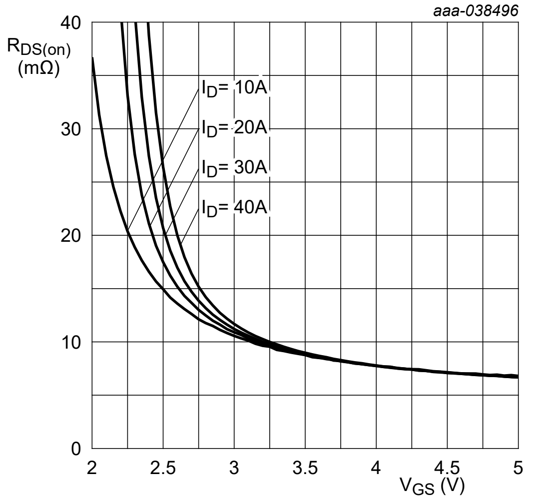
$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 8. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



T_j = 125 °C

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

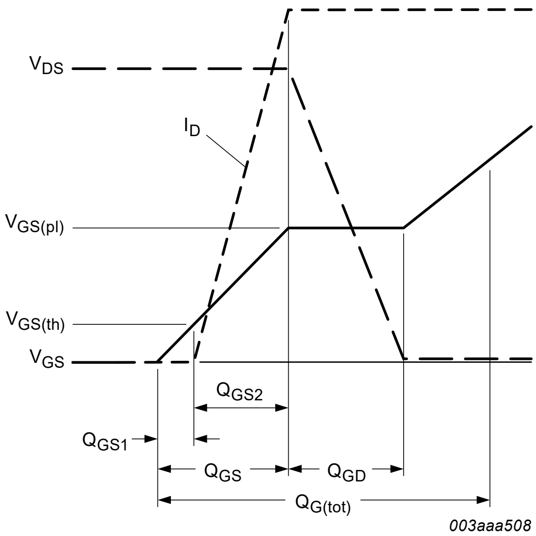
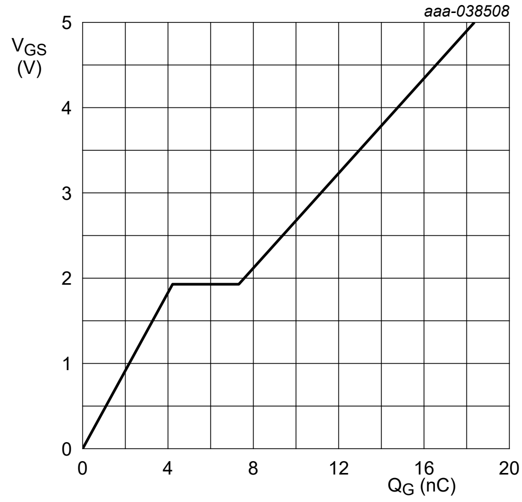
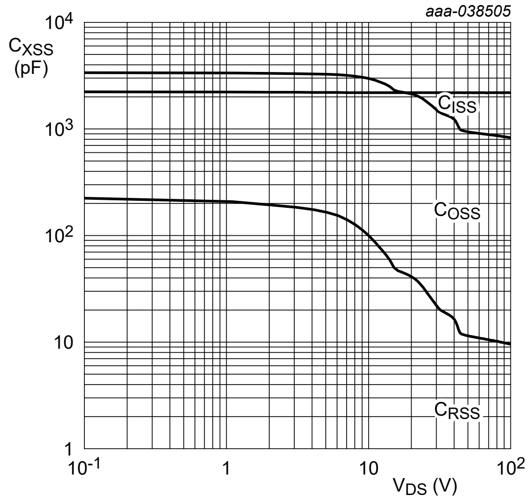


Fig. 11. Gate charge waveform definitions



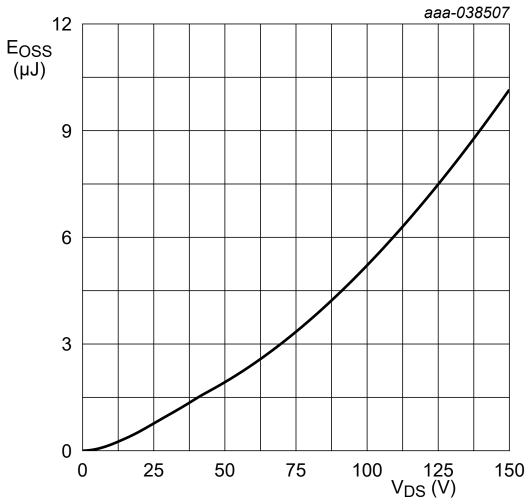
T_J = 25 °C ; I_D = 30A

Fig. 12. Gate-source voltage as a function of gate charge; typical values



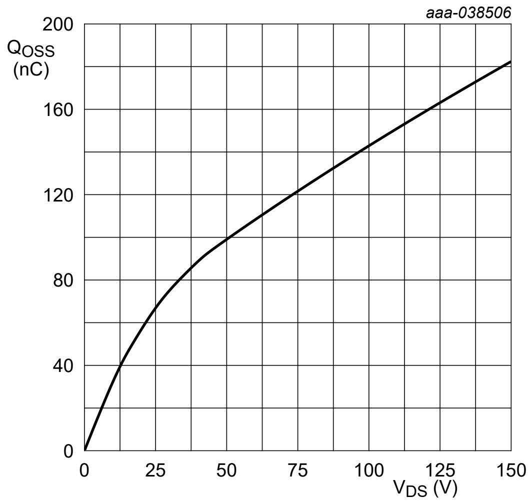
V_{GS} = 0 V; f = 100 kHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 14. COSS stored energy as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 15. Output charge as a function of drain-source voltage; typical values

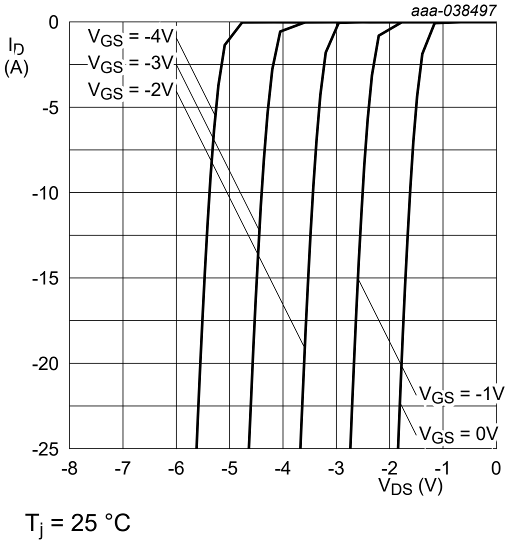


Fig. 16. Source current as a function of source-drain voltage; typical values

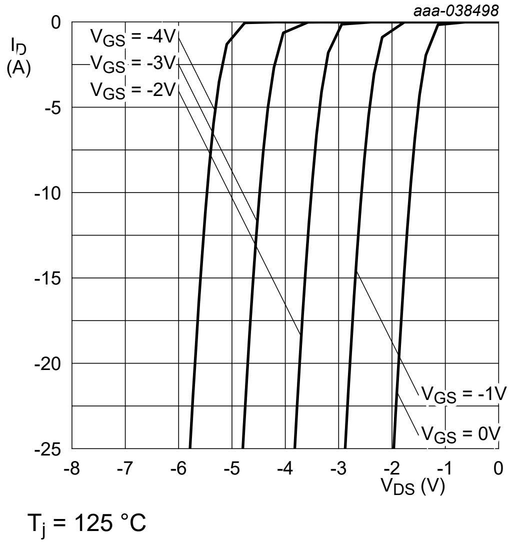


Fig. 17. Source current as a function of source-drain voltage; typical values

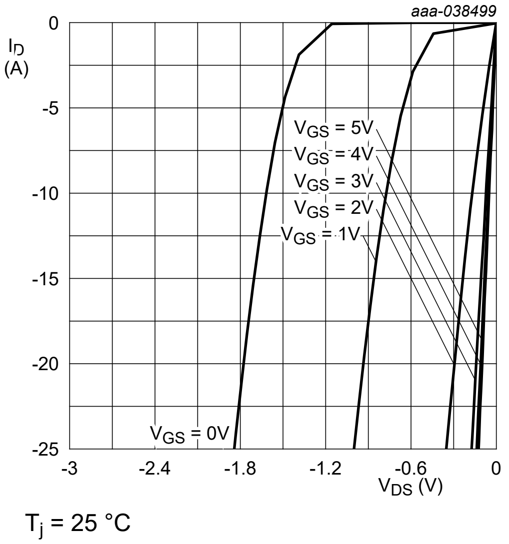


Fig. 18. Source current as a function of source-drain voltage; typical values

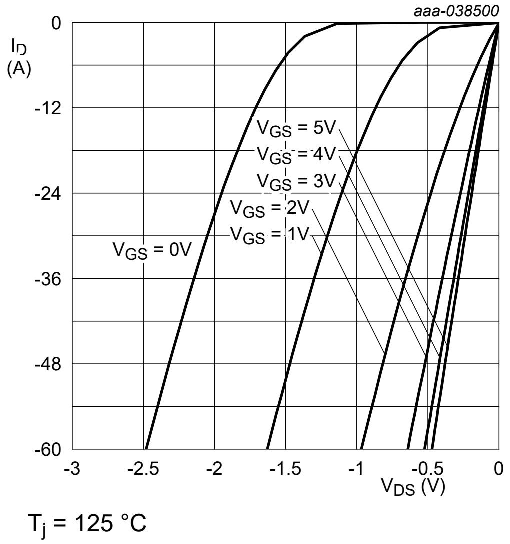
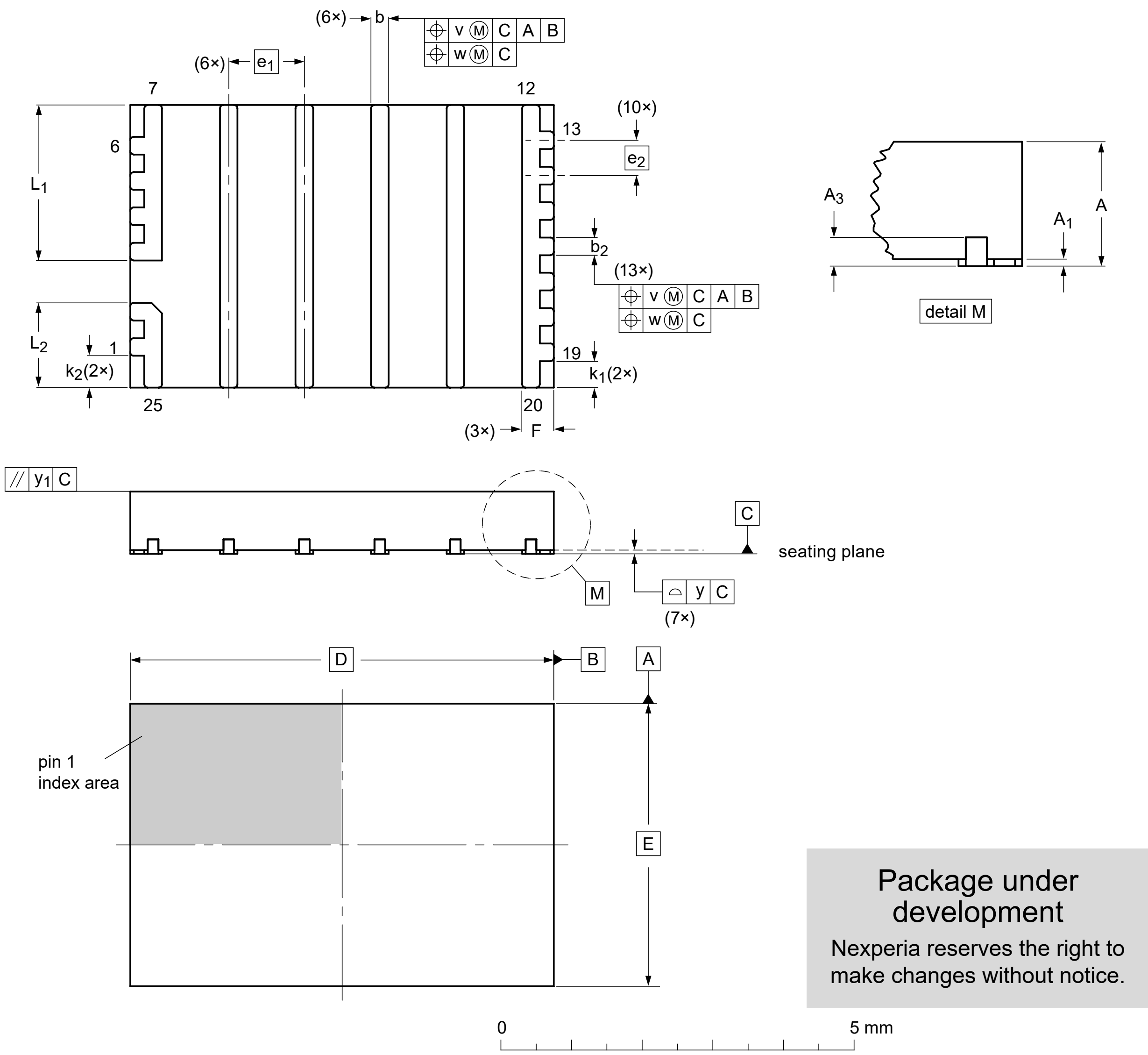


Fig. 19. Source current as a function of source-drain voltage; typical values

11. Package outline

Package description line 1
Package description line 2

SOT8091-1



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_3	b_1	b_2	D	E	e_1	e_2	k_1	k_2	F	L_1	L_2	v	w	y	y_1
mm	max	0.95	0.05	0.203 REF	0.30	0.30	6.10	4.10	1.07 BSC	0.50 BSC	0.375 REF	0.45 REF	0.55	2.30	1.30	0.10	0.05	0.08	0.10
	nom	0.85	0.02		0.25	0.25	6.00	4.00					0.45	2.20	1.20				
	min	0.75	0.00		0.20	0.20	5.90	3.90					0.35	2.10	1.10				

sot8091-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8091-1						24-02-19

Fig. 20. Package outline VQFN7 (SOT8091-1)

12. Soldering

Footprint information for reflow soldering of VQFN7 package **SOT8091-1**

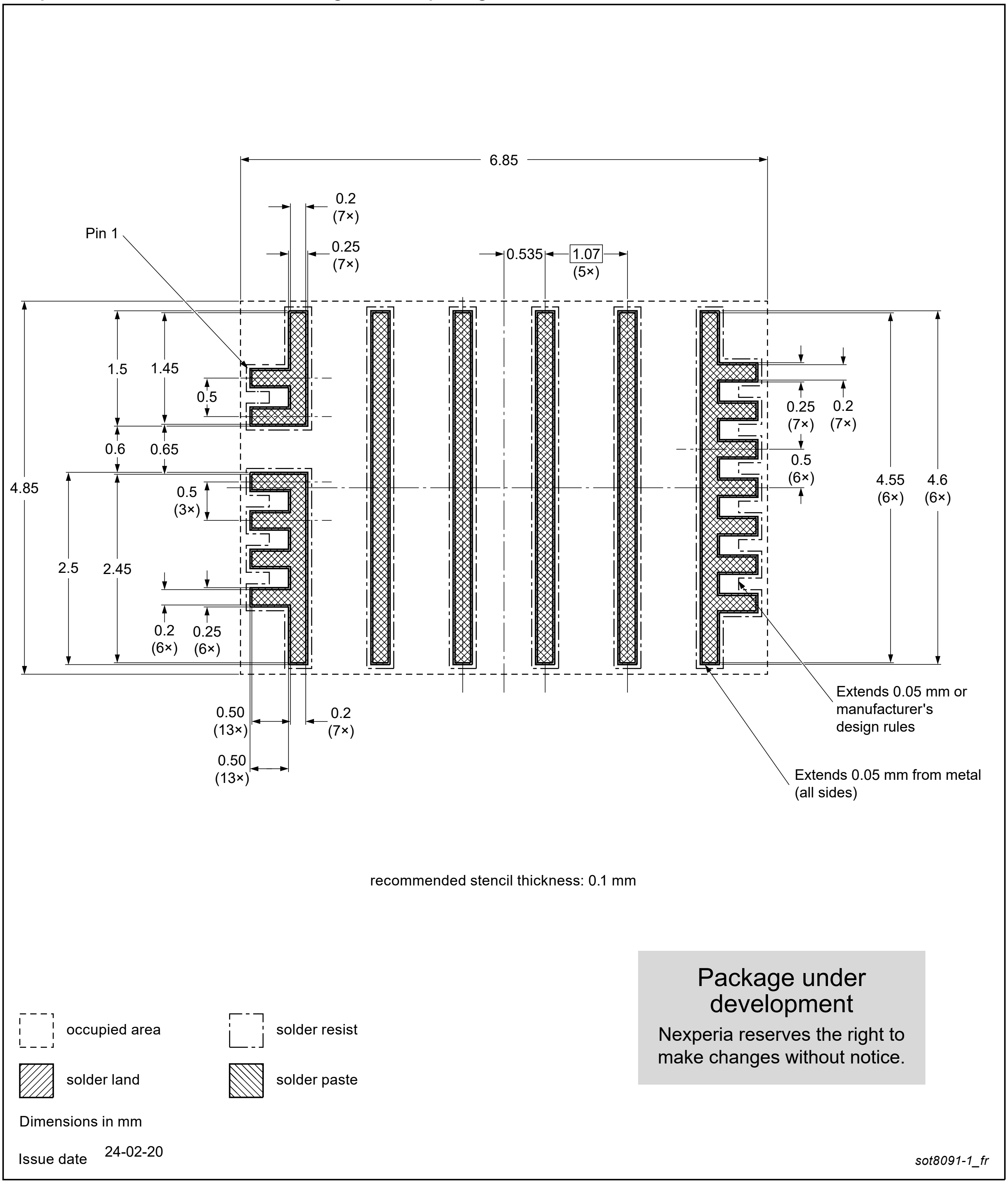


Fig. 21. Reflow soldering footprint for VQFN7 (SOT8091-1)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 30 April 2024