

# OptiMOS<sup>™</sup>-5 Power Transistor





#### **Features**

- OptiMOS™ power MOSFET for automotive applications
- N-channel Enhancement mode Normal level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

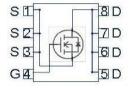
#### **Product Summary**

$V_{\mathrm{DS}}$	60	<b>V</b>
$R_{\mathrm{DS(on),max}}$	1.7	mΩ
I <sub>D</sub>	120	Α

#### PG-TDSON-8-43



Туре	Package	Marking
IAUC120N06S5N017	PG-TDSON-8-43	5N06N017



## **Maximum ratings,** at $T_i$ =25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I <sub>D</sub>	V <sub>GS</sub> =10 V, Chip limitation <sup>1,2)</sup>	226	А
		V <sub>GS</sub> =10V, DC current <sup>3)</sup>	120	
		$T_{\rm a}$ =85 °C, $V_{\rm GS}$ =10 V, $R_{\rm thJA}$ on 2s2p <sup>2,4)</sup>	30	
Pulsed drain current <sup>2)</sup>	I <sub>D,pulse</sub>	$T_{\rm C}$ =25 °C, $t_{\rm p}$ = 100 μs	757	
Avalanche energy, single pulse <sup>2)</sup>	E <sub>AS</sub>	I <sub>D</sub> =60 A	345	mJ
Avalanche current, single pulse	I <sub>AS</sub>	-	120	А
Gate source voltage	$V_{GS}$	-	±20	V
Power dissipation	$P_{\text{tot}}$	T <sub>C</sub> =25 °C	167	W
Operating and storage temperature	$T_{\rm j},T_{\rm stg}$	-	-55 <b>+</b> 175	°C



Parameter	Symbol	Conditions		Values		Unit
			min.	typ.	max.	
Thermal characteristics <sup>2)</sup>						
Thermal resistance, junction - case	$R_{\mathrm{thJC}}$	-	-	-	0.9	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	-	-	23.3	-	

**Electrical characteristics,** at  $T_j$ =25 °C, unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	$V_{GS}$ =0V, $I_D$ =1mA	60	ı	-	V
Gate threshold voltage	$V_{\rm GS(th)}$	$V_{\rm DS}=V_{\rm GS}, I_{\rm D}=94\mu{\rm A}$	2.2	2.8	3.4	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{\rm DS}$ =60V, $V_{\rm GS}$ =0V, $T_{\rm j}$ =25°C	ı	ı	1	μΑ
		$V_{\rm DS}$ =60V, $V_{\rm GS}$ =0V, $T_{\rm j}$ =125°C <sup>1)</sup>	-	ı	100	
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V	-	ı	100	nA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =7V, I <sub>D</sub> =30A	ı	1.6	1.9	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =60A	-	1.3	1.7	
Gate resistance <sup>2)</sup>	R <sub>G</sub>	-	-	1.6	-	Ω



Parameter	Symbol Conditions		Values			Unit
			min.	typ.	max.	
Dynamic characteristics <sup>2)</sup>						
Input capacitance	C <sub>iss</sub>		-	5348	6952	pF
Output capacitance	Coss	$V_{GS}$ =0V, $V_{DS}$ =30V, f=1MHz	-	1160	1507	1
Reverse transfer capacitance	C <sub>rss</sub>		-	56	84	
Turn-on delay time	$t_{\sf d(on)}$		-	13.4	-	ns
Turn-off delay time	$t_{d(off)}$	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V,	-	26.9	-	
Rise time	t <sub>r</sub>	$I_{\rm D}$ =60A, $R_{\rm G,ext}$ =3.5 $\Omega$	-	7.0	-	
Fall time	$t_{f}$		-	17.2	-	
Gate Charge Characteristics <sup>2)</sup>	To	I .				Τ_
Gate to source charge	Q <sub>gs</sub>		-	24.0	31.2	nC
Gate to drain charge	Q <sub>gd</sub>	$V_{\rm DD}$ =30V, $I_{\rm D}$ =60A, $V_{\rm GS}$ =0 to 10V	-	13.7	20.6	_
Gate charge total	Qg		-	73.7	95.9	
Gate plateau voltage	$V_{ m plateau}$		-	4.5	-	V
Reverse Diode						
Diode continous forward current <sup>2)</sup>	Is	T <sub>C</sub> =25 °C	-	-	120	А
Diode pulse current <sup>2)</sup>	I <sub>S,pulse</sub>	$T_{\rm C}$ =25 °C, $t_{\rm p}$ = 100 μs	-	-	757	
Diode forward voltage	$V_{\mathrm{SD}}$	$V_{\rm GS} = 0$ V, $I_{\rm F} = 60$ A, $T_{\rm j} = 25$ °C	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	t <sub>rr</sub>	V <sub>R</sub> =30V, I <sub>F</sub> =50A,	-	49	-	ns
Reverse recovery charge <sup>2)</sup>	Q <sub>rr</sub>	d <i>i<sub>F</sub></i> /d <i>t</i> =100A/µs	_	49	_	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

<sup>&</sup>lt;sup>2)</sup> The parameter is not subject to production test - verified by design/characterization.

<sup>&</sup>lt;sup>3)</sup> The product can operate at a specified current based on best practice to minimze electromigration at the solder joint. For rare events and inrush currents, the value may be exceeded.

<sup>&</sup>lt;sup>4)</sup> Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.



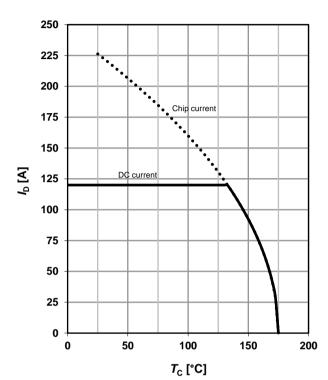
#### 1 Power dissipation

$$P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} = 10 \text{ V}$$

## 200 180 160 140 120 $P_{\rm tot}$ [W] 100 80 60 40 20 0 0 50 100 150 200 *T*<sub>C</sub> [°C]

#### 2 Drain current

$$I_{D} = f(T_{C}); V_{GS} = 10 \text{ V}$$



## 3 Safe operating area

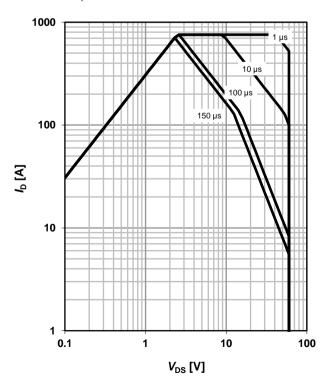
$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

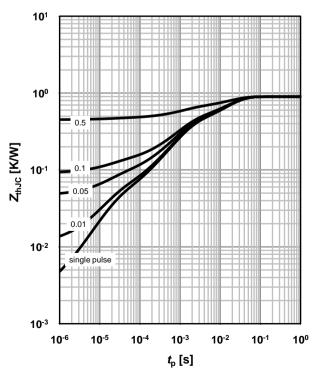
parameter:  $t_p$ 

#### 4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

parameter:  $D=t_p/T$ 



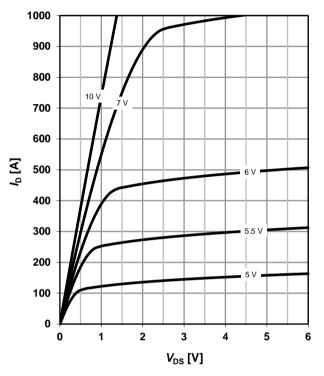




#### 5 Typ. output characteristics

 $I_{\rm D} = f(V_{\rm DS}); T_{\rm j} = 25 \,{}^{\circ}{\rm C}$ 

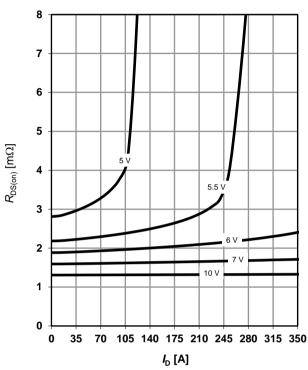
parameter:  $V_{\rm GS}$ 



#### 6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25 \text{ °C}$ 

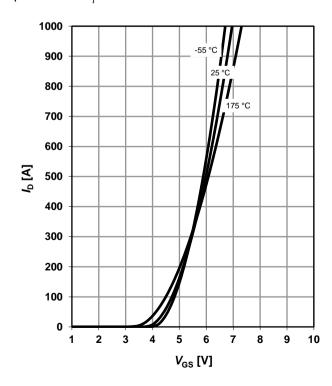
parameter: V<sub>GS</sub>



## 7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6V$ 

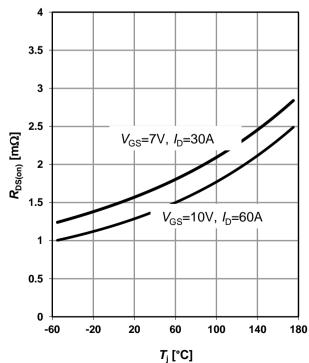
parameter: T<sub>i</sub>



## 8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j);$ 

parameter: I<sub>D.</sub> V<sub>GS</sub>





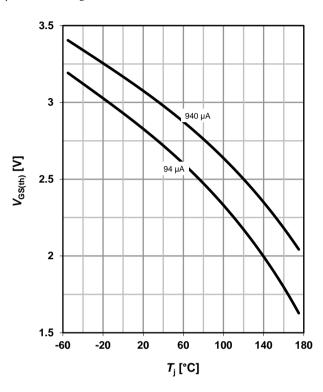
### 9 Typ. gate threshold voltage

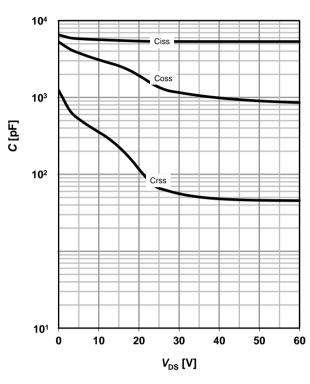
 $V_{GS(th)} = f(T_i); V_{GS} = V_{DS}$ 

parameter: I<sub>D</sub>

### 10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$ 





### 11 Typical forward diode characteristics

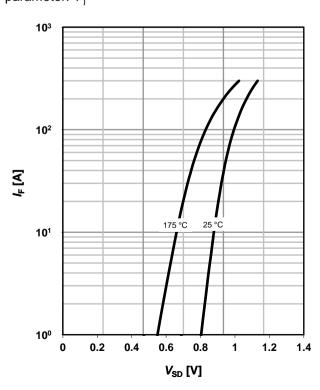
 $I_F = f(V_{SD})$ 

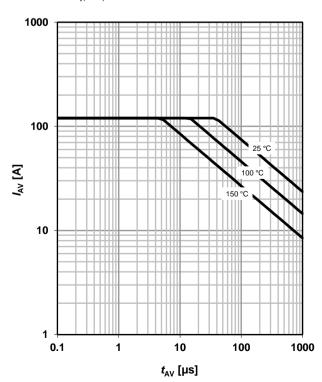
parameter:  $T_{\rm j}$ 

### 12 Avalanche characteristics

 $I_{AS} = f(t_{AV})$ 

parameter:  $T_{j(start)}$ 







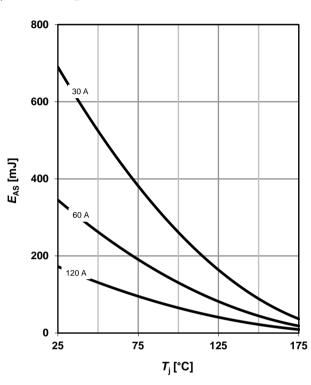
## 13 Avalanche energy

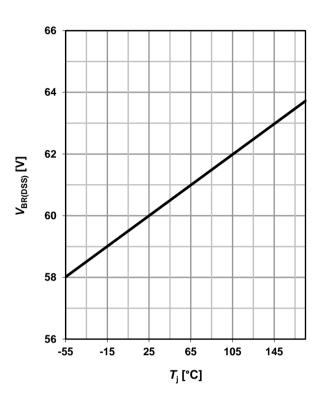
 $E_{AS} = f(T_i)$ 

parameter: I<sub>D</sub>

#### 14 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_i); I_D = 1 \text{ mA}$$

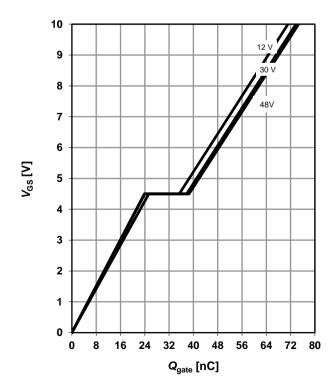




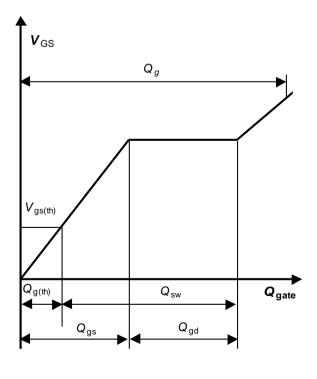
### 15 Typ. gate charge

 $V_{GS} = f(Q_{gate}); I_D = 60 A pulsed$ 

parameter: V<sub>DD</sub>

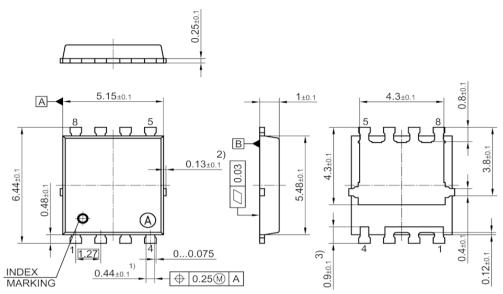


### 16 Gate charge waveforms



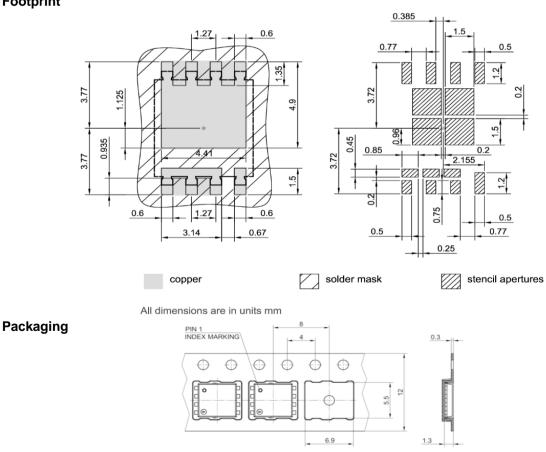


#### **Package Outline**



- 1) EXCLUDE MOLD FLASH
  2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
  3) LEAD LENGTH UP TO ANTI FLASH LINE
  4)ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
  ALL DIMENSIONS ARE IN UNITS MM
  THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [

#### **Footprint**





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### **Revision History**

Version	Date	Changes		
Revision 1.0	04.05.2020	Final Data Sheet		