## N-channel 650 V, 0.042 Ω typ., 60 A MDmesh™ DM2 Power MOSFET in a TO-247 long leads package

TO-247 long leads

D(2)

G(1)

S(3)

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Features
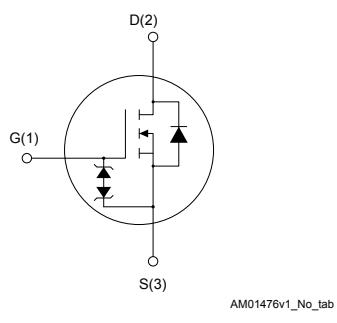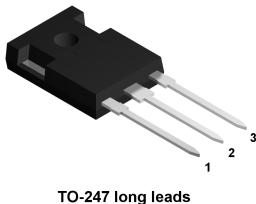
Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STWA63N65DM2	650 V	0.050 Ω	60 A	446 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link	
STWA63N65DM2	

Product summary	
Order code	STWA63N65DM2
Marking	63N65DM2
Package	TO-247 long leads
Packing	Tube

1   Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	60	A
	Drain current (continuous) at T_{case} = 100 °C	38	
I_{DM} [1]	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	446	W
dv/dt[2]	Peak diode recovery voltage slope	50	V/ns
dv/dt[3]	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*

2. $I_{SD} \leq 60$ A, di/dt=800 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

3. $V_{DS} \leq 520$ V

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.28	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive	8	A
E_{AS} [1]	Single pulse avalanche energy	1100	mJ

1. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2   Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			10	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C[1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 30 A		0.042	0.050	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	5500	-	pF
C_{oss}	Output capacitance		-	210	-	
C_{rss}	Reverse transfer capacitance		-	3	-	
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	456	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3.3	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 60 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	120	-	nC
Q_{gs}	Gate-source charge		-	27	-	
Q_{gd}	Gate-drain charge		-	58	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 30 A R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	33	-	ns
t_r	Rise time		-	13.5	-	
$t_{d(off)}$	Turn-off delay time		-	114	-	
t_f	Fall time		-	11.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		60	A
I_{SDM} [1]	Source-drain current (pulsed)		-		240	A
V_{SD} [2]	Forward on voltage	$V_{GS} = 0$ V, $I_{SD} = 60$ A	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 60$ A, di/dt = 100 A/µs, $V_{DD} = 60$ V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	154		ns
Q_{rr}	Reverse recovery charge		-	0.94		µC
I_{RRM}	Reverse recovery current		-	12.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 60$ A, di/dt = 100 A/µs, $V_{DD} = 60$ V, $T_j = 150$ °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	288		ns
Q_{rr}	Reverse recovery charge		-	3.65		µC
I_{RRM}	Reverse recovery current		-	25.4		A

1. *Pulse width is limited by safe operating area.*

2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area
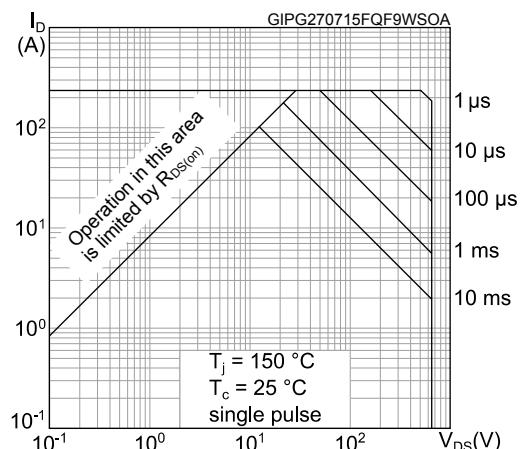
Figure 2. Thermal impedance
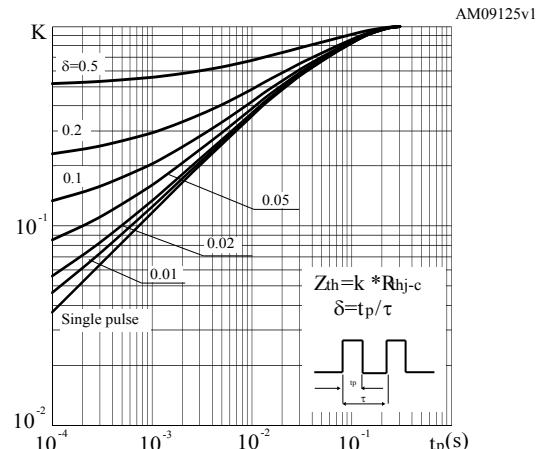
Figure 3. Output characteristics
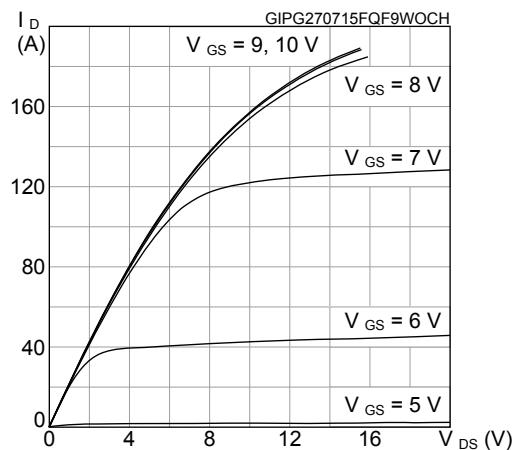
Figure 4. Transfer characteristics
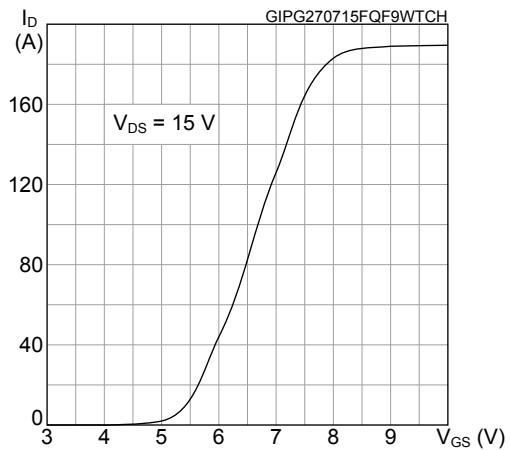
Figure 5. Gate charge vs gate-source voltage
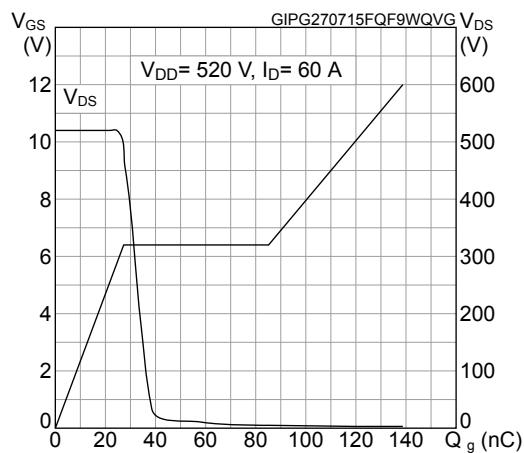
Figure 6. Static drain-source on-resistance
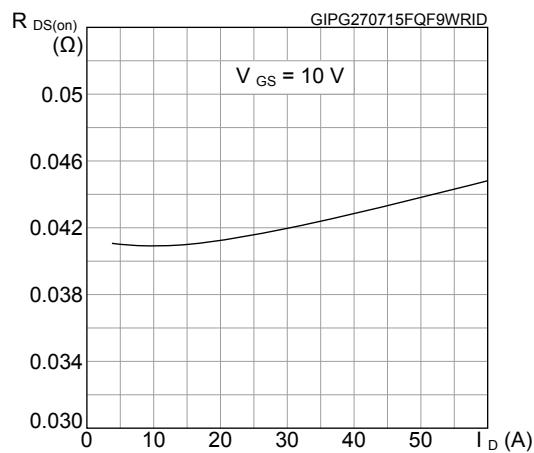
Figure 7. Capacitance variations
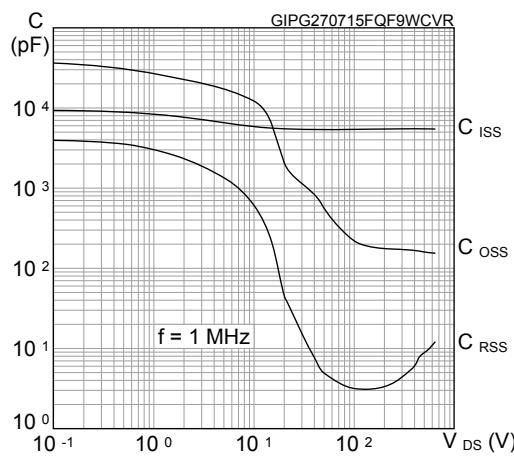
**Figure 8. Normalized gate threshold voltage vs temperature**
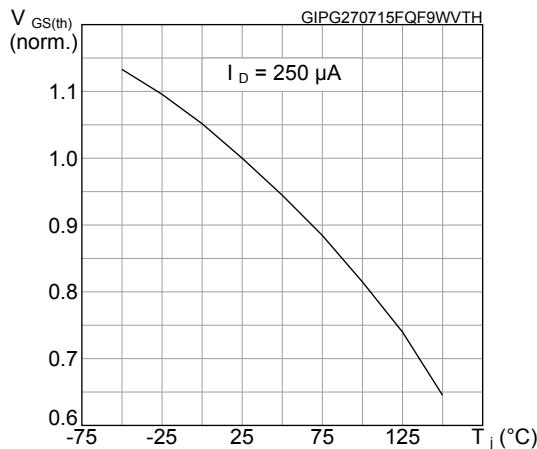

**Figure 9. Normalized on-resistance vs temperature**
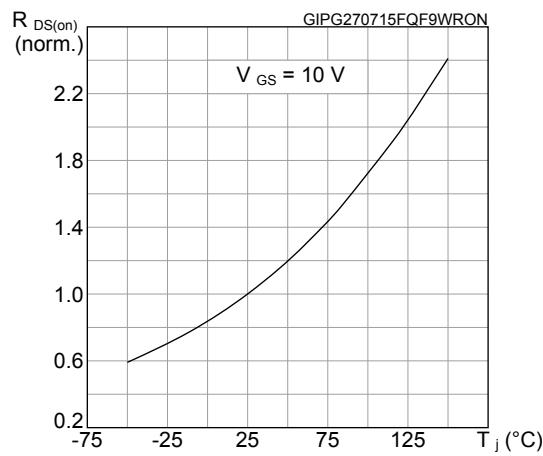
Figure 10. Normalized V(BR)DSS vs temperature
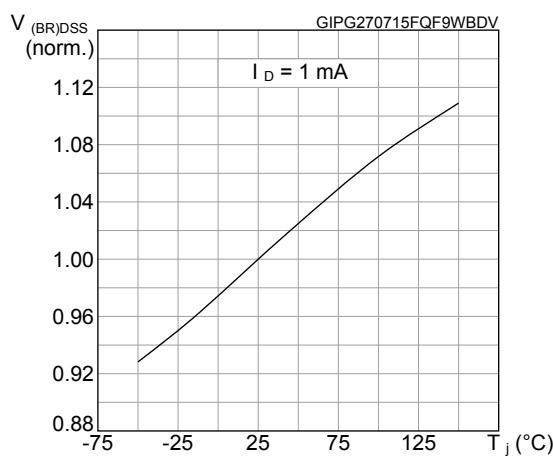
Figure 11. Output capacitance stored energy
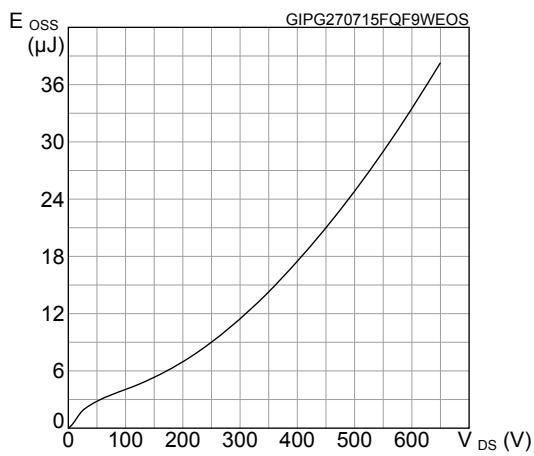
Figure 12. Source- drain diode forward characteristics
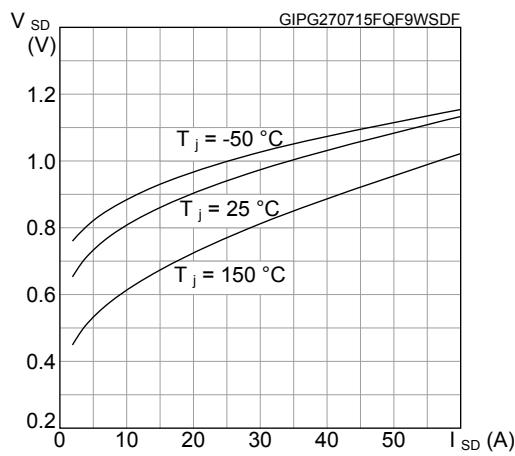
3 Test circuits

**Figure 13. Test circuit for resistive load switching times**
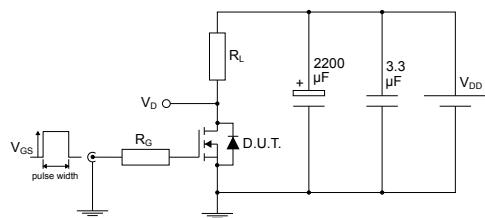

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Figure 14. Test circuit for gate charge behavior
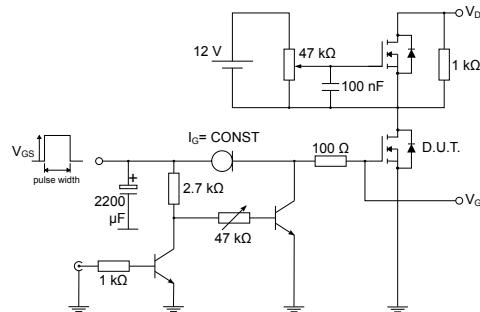
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Figure 15. Test circuit for inductive load switching and diode recovery times
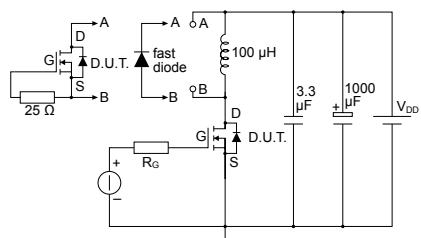

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Figure 16. Unclamped inductive load test circuit
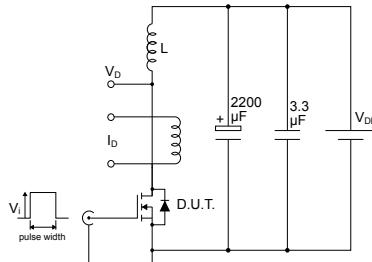
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Figure 17. Unclamped inductive waveform
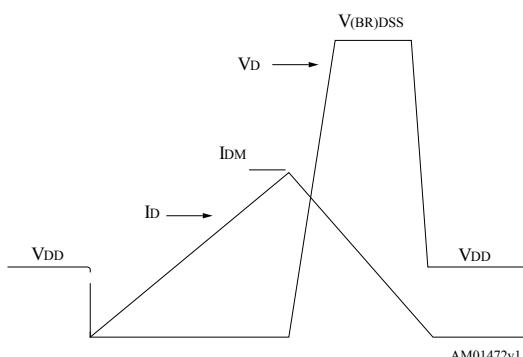
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Figure 18. Switching time waveform
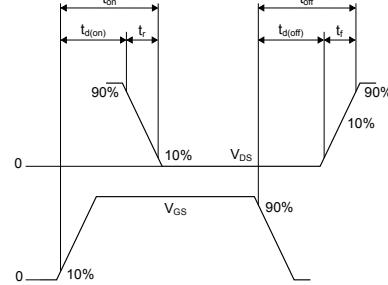
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline
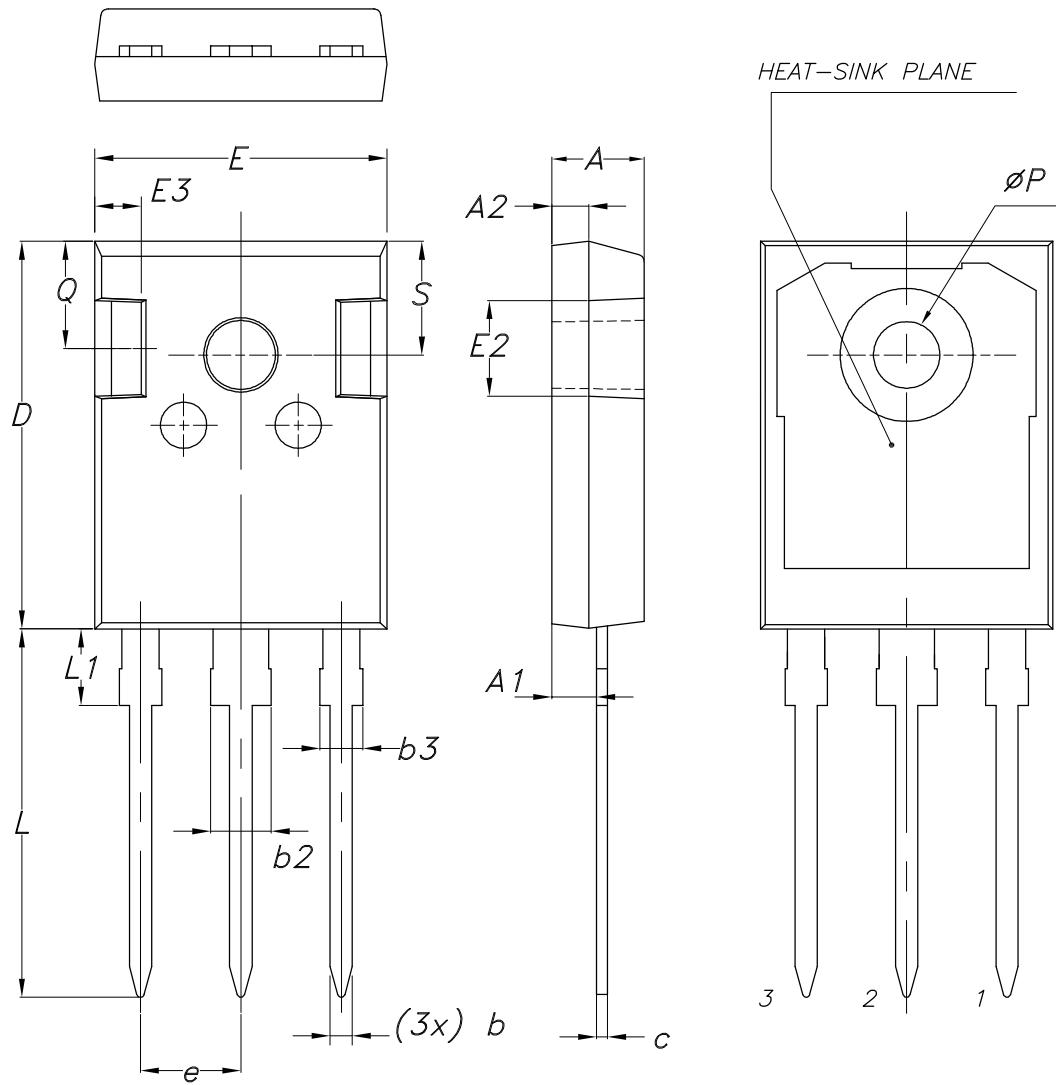
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Table 8. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Apr-2018	1	Initial release. The document status is production data.

Contents

IMPORTANT NOTICE – PLEASE READ CAREFULLY