

Taiwan Semiconductor

PerF∃T[™]Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

PRODUCT SUMMARY				
PARAMETER		VALUE	UNIT	
V_{DS}		40	V	
R _{DS(on)} (max)	$V_{GS} = 10V$	2.5	0	
	$V_{GS} = 4.5V$	3.5	mΩ	
Q_{g}	$V_{GS} = 4.5V$	29.5	nC	



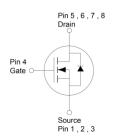




APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V_{DS}	40	V	
Gate-Source Voltage		V_{GS}	±16	V	
Continuous Drain Current, Silicon limited	$T_C = 25^{\circ}C$	I _D	174	Α	
	$T_C = 25^{\circ}C$	I _D	100		
Continuous Drain Current (Note 1)	$T_C = 100$ °C		100	Α	
	$T_A = 25^{\circ}C$		26		
Pulsed Drain Current		I _{DM}	400	А	
Single Pulse Avalanche Current (Note 2)		I _{AS}	34.6	А	
Single Pulse Avalanche Energy (Note 2)		E _{AS}	179.4	mJ	
Total Power Discipation	T _C = 25°C	P _D	136	W	
Total Power Dissipation	T _C = 125°C		45	VV	
Operating Junction and Storage Temperature Range		T_J,T_STG	- 55 to +175	°C	

THERMAL RESISTANCE				
PARAMETER	SYMBOL	MAXIMUM	UNIT	
Thermal Resistance – Junction to Case	R _{OJC}	1.1	°C/W	
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W	

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

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ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 1mA$	BV _{DSS}	40			V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	1.4	1.9	2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 16V, V_{DS} = 0V$	I _{GSS}			±100	nA
	$V_{GS} = 0V, V_{DS} = 40V$	I _{DSS}			1	μA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 40V$ $T_{J} = 125^{\circ}C$				100	
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 50A$	Б		1.8	2.5	mΩ
(Note 3)	$V_{GS} = 4.5V, I_D = 50A$	R _{DS(on)}		2.3	3.5	
Forward Transconductance (Note 3)	$V_{DS} = 10V, I_{D} = 12.5A$	g _{fs}		132.5		S
Dynamic						
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 25V,$ $I_{D} = 26A$	Q_g		29.5		
Total Gate Charge		Q_g		63.3		nC
Gate-Source Charge	$V_{GS} = 10V, V_{DS} = 25V,$	Q _{gs}		11.8		
Gate-Drain Charge	I _D = 26A	Q_{gd}		8.7		
Input Capacitance	., ., ., ., .,	C _{iss}		4179		
Output Capacitance	$V_{GS} = 0V, V_{DS} = 25V,$	C _{oss}		769		pF
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		43		
Gate Resistance	f = 1.0MHz	R_g		0.8		Ω
Switching (Note 4)						
Turn-On Delay Time		t _{d(on)}		11.8		
Rise Time	$V_{GS} = 10V, V_{DS} = 25V,$ $I_{D} = 26A, R_{G} = 0.8\Omega$	t _r		71		
Turn-Off Delay Time		t _{d(off)}		35		ns
Fall Time		t _f		5.8		
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0V, I_{S} = 50A$	V _{SD}			1.1	V
Reverse Recovery Time	I _S = 26A,	t _{rr}		45.9		ns
Reverse Recovery Charge	di/dt = 100A/µs	Q _{rr}		57.8		nC

Notes:

- 1. Package current limit.
- 2. L = 0.3 mH, $V_{GS} = 10 V$, $R_G = 25 \Omega$, Starting $T_J = 25 ^{\circ} C$.
- 3. Pulse test: Pulse Width \leq 300µs, duty cycle \leq 2%.
- 4. Switching time is essentially independent of operating temperature.

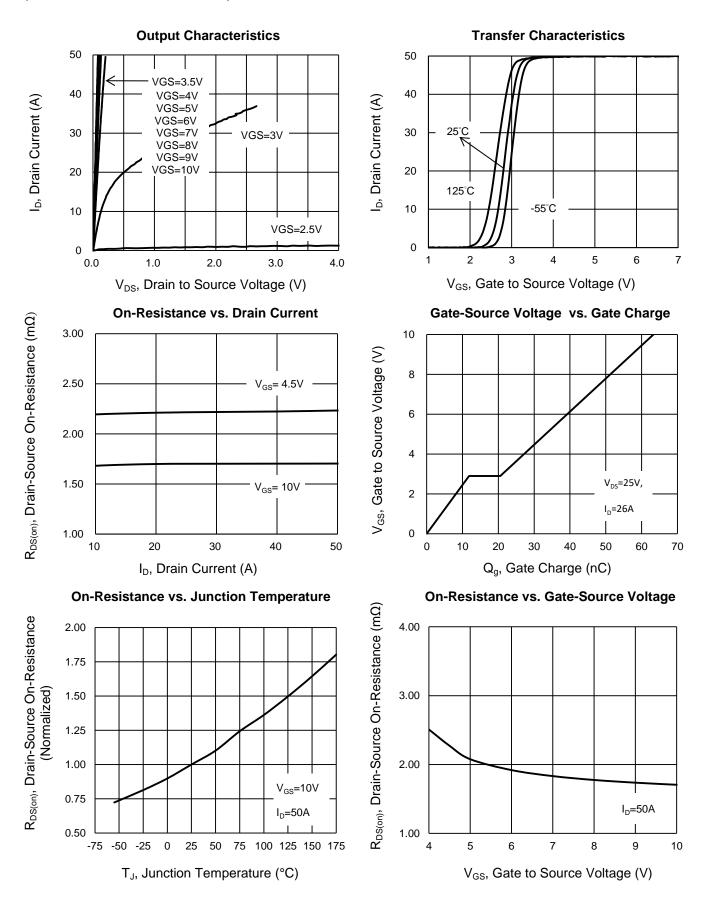
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM025NH04LCR RLG	PDFN56U	2,500pcs / 13" Reel



CHARACTERISTICS CURVES

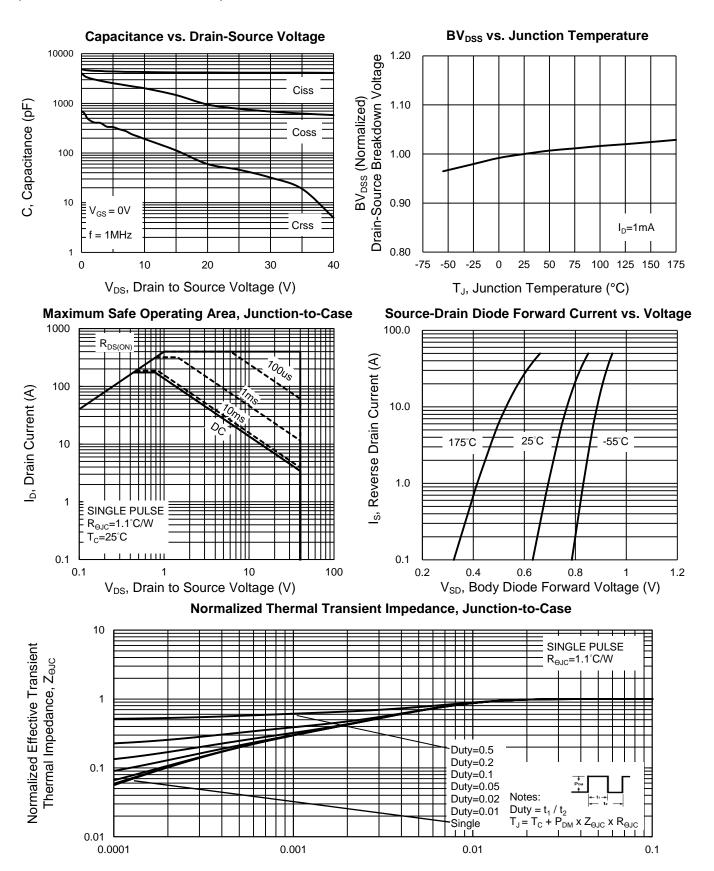
 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$





CHARACTERISTICS CURVES

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$

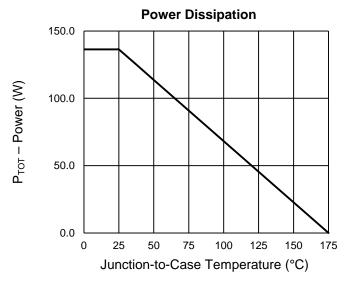


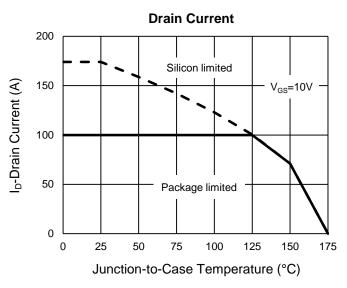
t, Square Wave Pulse Duration (sec)



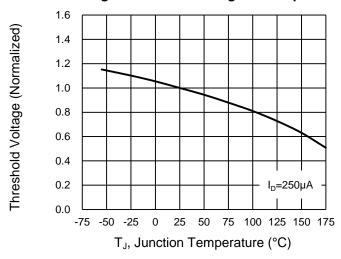
CHARACTERISTICS CURVES

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$





Normalized gate threshold voltage vs Temperature



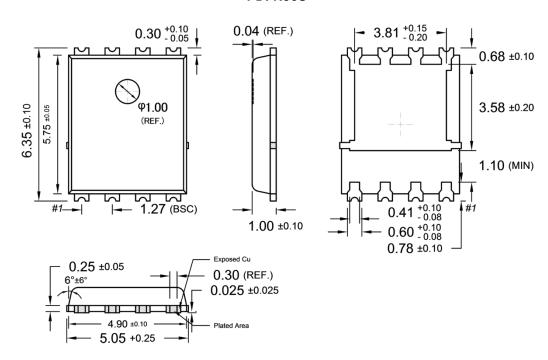
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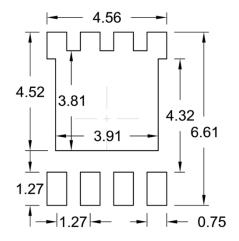


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

WW = Week Code (01~52)

 \mathbf{L} = Lot Code (1~9,A~Z)

F = Factory Code



Taiwan Semiconductor

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