N-channel 100 V, 2.9 mOhm, standard level Trench MOSFET in MLPAK56

16 August 2024

**Product data sheet** 

## 1. General description

General purpose MOSFET for standard applications, 180 A, standard level N-channel enhancement mode Power MOSFET in MLPAK56 package.

## 2. Features and benefits

- · Standard level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (5.15 mm x 6.15 mm footprint)

## 3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- · Home appliance
- · Motor drive
- Load switching
- · LED lighting
- E-bike

## 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C		-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	180	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	181	W
Tj	junction temperature			-55	-	150	°C
Static chara	acteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}; Fig. 9$		-	2.65	2.9	mΩ
Dynamic ch	naracteristics					'	
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;		-	19	-	nC
Q <sub>G(tot)</sub>	total gate charge	T <sub>j</sub> = 25 °C; <u>Fig. 11</u> ; <u>Fig. 12</u>		-	74	-	nC
Avalanche	ruggedness					'	
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 52.5 A; $V_{sup} \le 100 \text{ V}$ ; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	-	275.6	mJ



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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain d	iode						
Q <sub>r</sub>		$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 15$	[2]	-	48	-	nC

<sup>[1]</sup> Protected by 100% test

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4	
2	S	source		
3	S	source	<u> </u>	D T
4	G	gate		
5	D	drain		G—(F)
6	D	drain		mbb076 S
7	D	drain	8 7 6 5	
8	D	drain	MLPAK56 (SOT8038-1)	

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package				
	Name	Description	Version		
PXN2R9-100RS	MLPAK56	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 1.27 mm; 6 x 5 x 1.0 mm body	SOT8038-1		

# 7. Marking

Table 4. Marking codes

Type number	Marking code
PXN2R9-100RS	2R9-100

# 8. Limiting values

### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	181	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	-	180	А
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	-	114	A
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3	-	722	А
T <sub>stg</sub>	storage temperature		-55	150	°C

<sup>[2]</sup> includes capacitive recovery

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Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drai	n diode			'	•	
Is	source current	T <sub>mb</sub> = 25 °C		-	151	Α
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	722	Α
Avalanche r	uggedness		'		'	'
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 52.5 A; $V_{sup} \le 100$ V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	275.6	mJ
I <sub>AS</sub>	non-repetitive avalanche current	$T_{j(init)} = 25  ^{\circ}C$	[1]	-	52.5	А

#### [1] Protected by 100% test

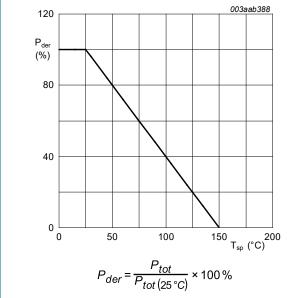


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

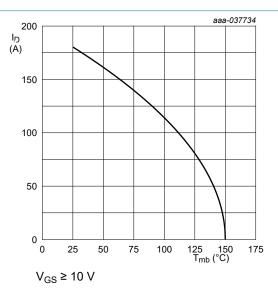
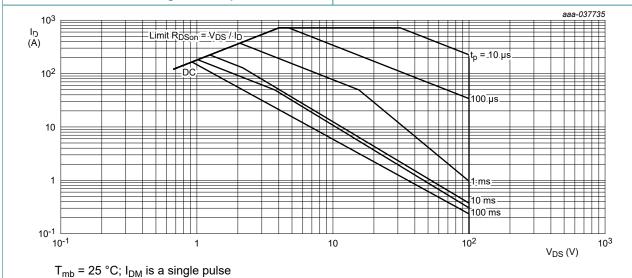


Fig. 2. Continuous drain current as a function of mounting base temperature



Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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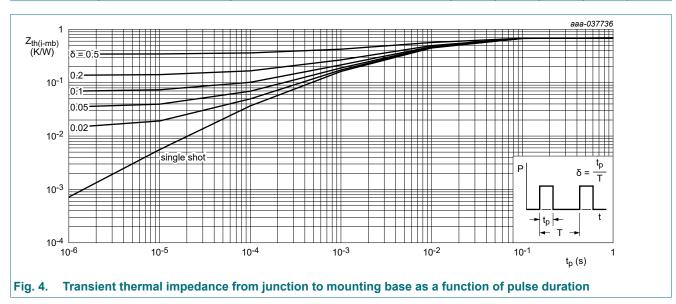
PXN2R9-100RS

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## 9. Thermal characteristics

#### **Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 4	-	0.57	0.69	K/W



## 10. Characteristics

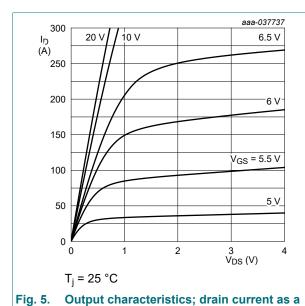
**Table 7. Characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	teristics		'	'		
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	100	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ °C};$ Fig. 8	2.5	3	4	V
		I <sub>D</sub> = 0.25 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 150 °C	-	1.6	-	V
		$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	3.7	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-11.2	-	mV/K
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.07	1	μΑ
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	74	-	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 9$	-	2.65	2.9	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; Fig. 10	-	-	5.6	mΩ
$R_G$	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	-	1.7	-	Ω

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Symbol	Parameter	Conditions	М	in Typ	Max	Unit
Dynamic ch	naracteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <u>Fig. 11</u> ; <u>Fig. 12</u>	-	74	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}$	-	62	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;	-	22	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	T <sub>j</sub> = 25 °C; <u>Fig. 11; Fig. 12</u>	-	13	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	9	-	nC
Q <sub>GD</sub>	gate-drain charge		-	19	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12	-	4.9	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	4892	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 13</u>	-	1948	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	29	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \Omega; V_{GS} = 10 \text{ V};$	-	21	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	27	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	46	-	ns
t <sub>f</sub>	fall time		-	33	-	ns
Q <sub>oss</sub>	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	145	-	nC
Source-dra	in diode	•			1	-
V <sub>SD</sub>	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}; Fig. 14$	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	47	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 50 \text{ V}; T_j = 25 \text{ °C}; Fig. 15$	[1] -	48	-	nC

#### [1] includes capacitive recovery



function of drain-source voltage; typical values

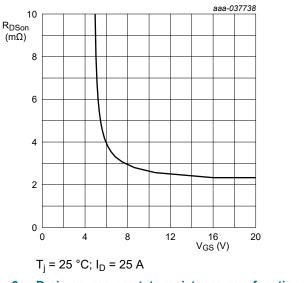


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

### N-channel 100 V, 2.9 mOhm, standard level Trench MOSFET in MLPAK56

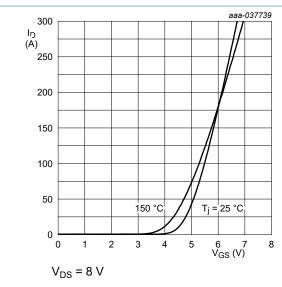


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

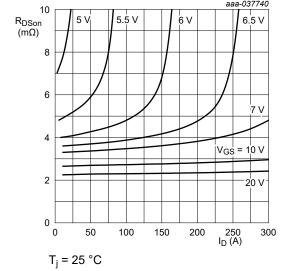


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

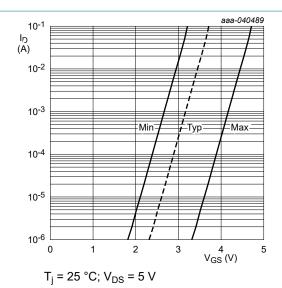


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

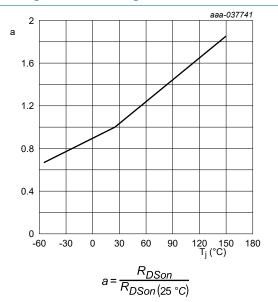


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

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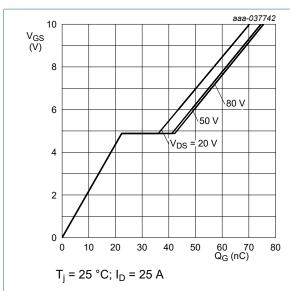


Fig. 11. Gate-source voltage as a function of gate charge; typical values

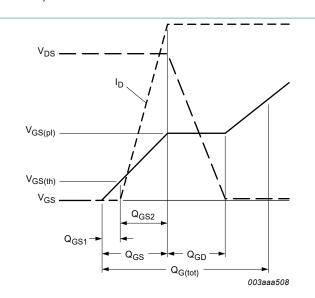


Fig. 12. Gate charge waveform definitions

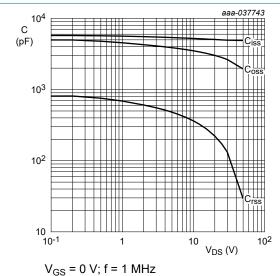
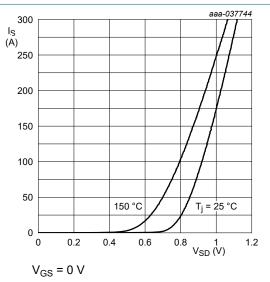


Fig. 13. Input, output and reverse transfer capacitances | Fig. 14. Source-drain (diode forward) current as a as a function of drain-source voltage; typical values



function of source-drain (diode forward) voltage; typical values

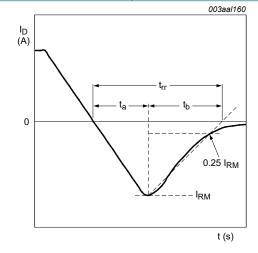


Fig. 15. Reverse recovery timing definition

#### N-channel 100 V, 2.9 mOhm, standard level Trench MOSFET in MLPAK56

# 11. Package outline

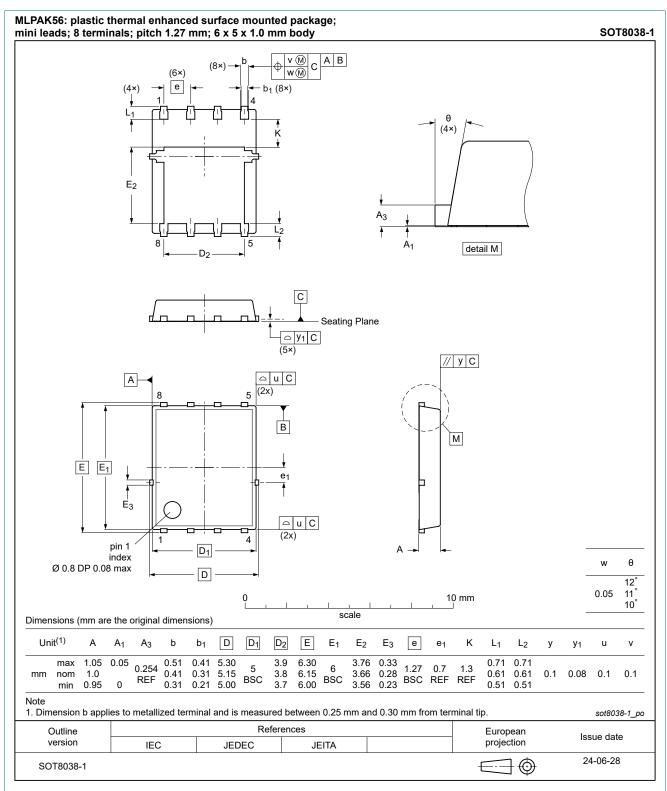
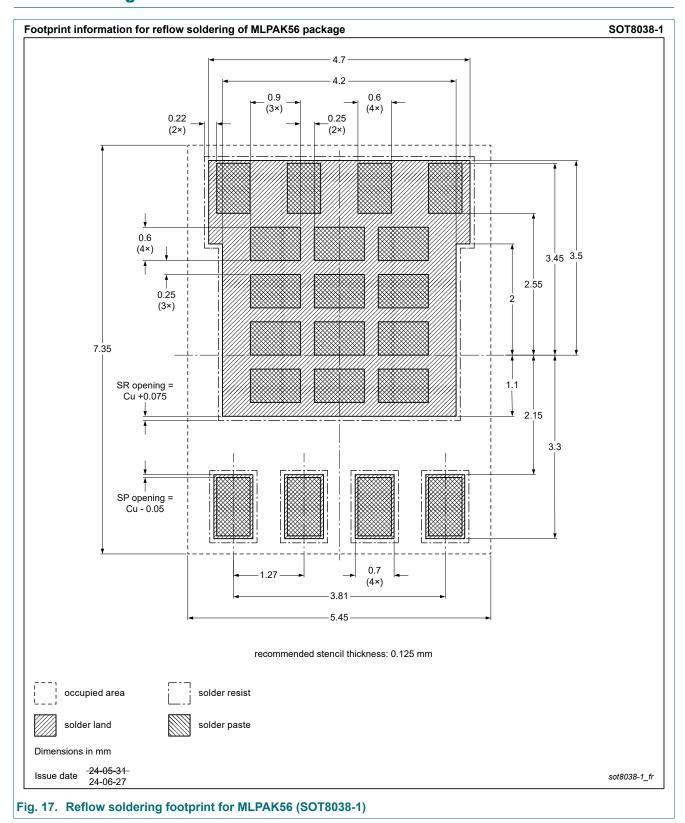


Fig. 16. Package outline MLPAK56 (SOT8038-1)

#### N-channel 100 V, 2.9 mOhm, standard level Trench MOSFET in MLPAK56

# 12. Soldering



#### N-channel 100 V, 2.9 mOhm, standard level Trench MOSFET in MLPAK56

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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