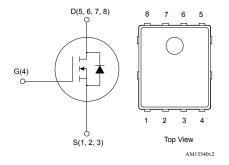


N-channel 100 V, 7 m Ω typ., 70 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V _{DS}	R _{DS(on)} max.	l _D	P _{TOT}
STL90N10F7	100 V	8 mΩ	70 A	100 W

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- · High avalanche ruggedness

Applications

· Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link STL90N10F7

Product summary		
Order code STL90N10F7		
Marking	90N10F7	
Package PowerFLAT 5x6		
Packing	Tape and reel	



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	100	V
V _{GS}	Gate-source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	70	А
ID(**)	Drain current (continuous) at T _C = 100 °C	50	Α
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 25 °C	16	Α
ID(=)	Drain current (continuous) at T _{pcb} = 100 °C	11	А
I _{DM} ⁽¹⁾⁽³⁾	Drain current (pulsed)	280	А
I _{DM} ⁽²⁾⁽³⁾	I _{DM} ⁽²⁾⁽³⁾ Drain current (pulsed)		Α
P _{TOT} ⁽¹⁾	Total power dissipation at T _C = 25 °C	100	W
P _{TOT} ⁽²⁾	$P_{TOT}^{(2)}$ Total power dissipation at $T_{pcb} = 25 ^{\circ}C$		W
E _{AS} ⁽⁴⁾	E _{AS} ⁽⁴⁾ Single pulse avalanche energy		mJ
T _{stg}	Storage temperature range	- 55 to 175	°C
T _J	Operating junction temperature range	- 55 (0 175	°C

- 1. This value is rated according to R_{thj-c} .
- 2. This value is rated according to $R_{thj-pcb}$.
- 3. Pulse width is limited by safe operating area.
- 4. Starting $T_J = 25$ °C, $I_D = 10$ A, $V_{DD} = 50$ V.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	1.5	°C/W
R _{thj-pcb} (1)	R _{thj-pcb} (1) Thermal resistance junction-pcb 31		C/VV

1. When mounted on 1 inch², 2 Oz. Cu FR-4 board.

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2 Electrical characteristics

(T_C = 25 $^{\circ}$ C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
lano	Zoro goto voltago drain ourrent	V _{GS} = 0 V, V _{DS} = 100 V			1	μA
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 100 V, T _C = 125 °C			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5	3.5	4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 8 A		7	8	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	3100	4030	pF
C _{oss}	Output capacitance		-	700	910	pF
C _{rss}	Reverse transfer capacitance		-	45	58	pF
Qg	Total gate charge	V _{DD} = 50 V, I _D = 16 A, V _{GS} = 10 V	-	45	60	nC
Q _{gs}	Gate-source charge	(see Figure 13. Test circuit for gate	-	18		nC
Q _{gd}	Gate-drain charge	charge behavior)	-	13		nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 8 A,	-	19	-	ns
t _r	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	32	-	ns
t _{d(off)}	Turn-off-delay time	(see Figure 12. Test circuit for resistive load switching times and		36	-	ns
t _f	Fall time	Figure 17. Switching time waveform)	-	13	-	ns

Table 6. Source-drain diode

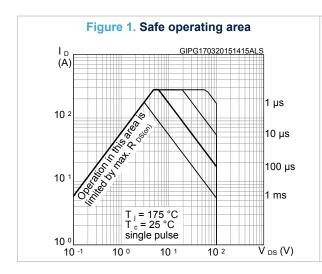
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 16 A	-		1.1	V
t _{rr}	Reverse recovery time	I _{SD} = 16 A, di/dt = 100 A/μs,	-	70	90	ns
Q _{rr}	Reverse recovery charge	V _{DD} = 80 V, T _J = 150 °C	-	125		nC
I _{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	3.6		Α

^{1.} Pulse test: pulse duration = 300 μ s, duty cycle 1.5%.

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2.1 Electrical characteristics (curves)



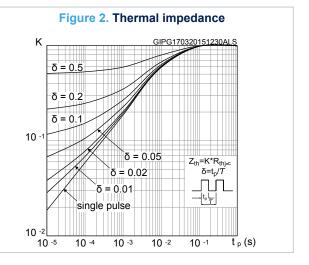
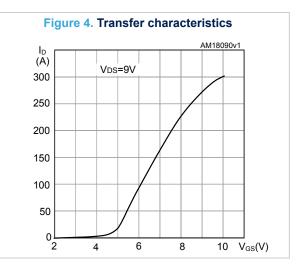
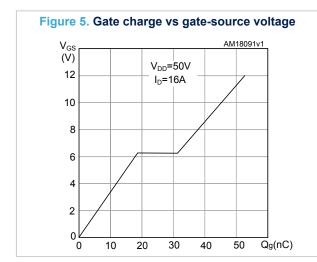
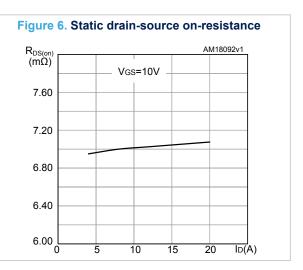


Figure 3. Output characteristics AM18089v1 I_D (A) Vgs=10V 300 9V 250 8V 200 7V 150 100 6V 50 5V 0 4 8 V_{DS}(V)







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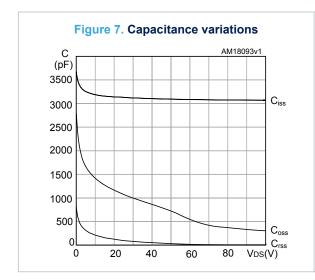
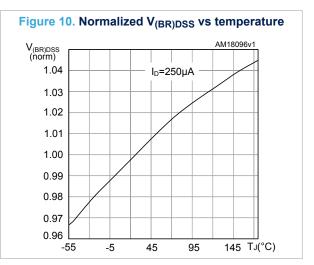
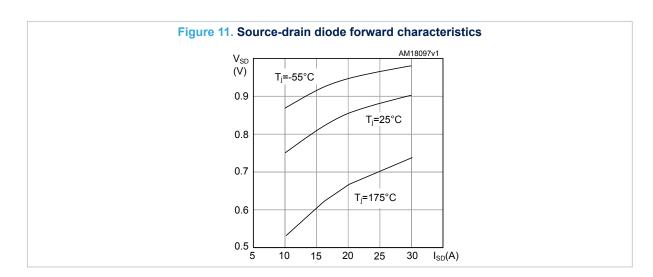


Figure 8. Normalized gate threshold voltage vs temperature VGS(th) AM18094v1 (norm) I_D=250μA 1.2 1.0 8.0 0.6 0.4 0.2 -5 45 95 145 T_J(°C) -55

RDS(on) (norm) 2.0 VGS=10V AM18095v1 (1.5 1.0 0.5 -55 -5 45 95 145 TJ(°C)





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3 Test circuits

Figure 12. Test circuit for resistive load switching times

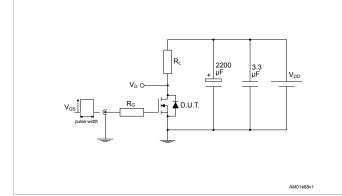


Figure 13. Test circuit for gate charge behavior

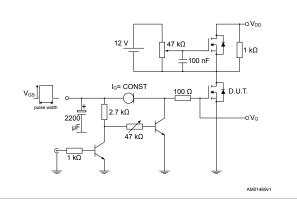


Figure 14. Test circuit for inductive load switching and diode recovery times

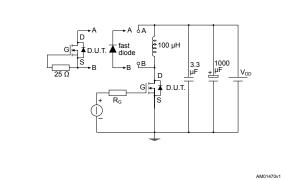


Figure 15. Unclamped inductive load test circuit

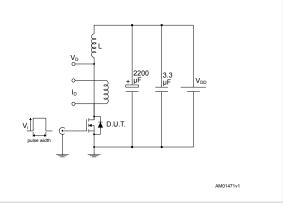


Figure 16. Unclamped inductive waveform

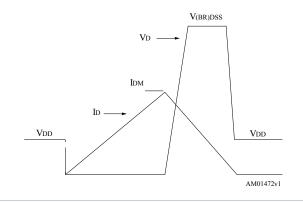
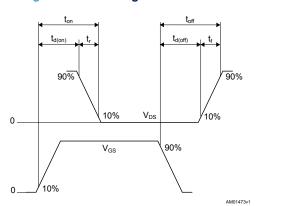


Figure 17. Switching time waveform



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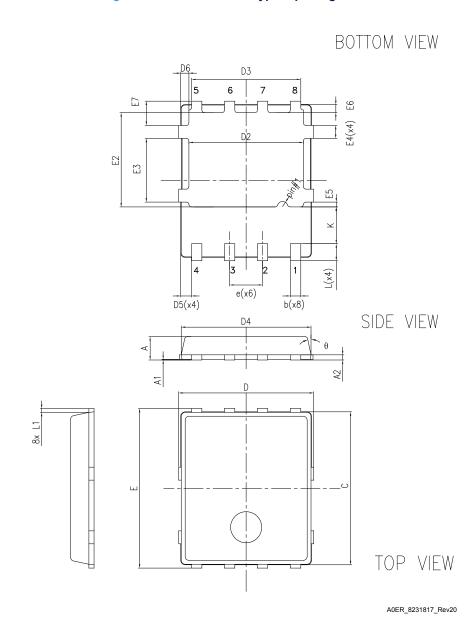


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 18. PowerFLAT 5x6 type R package outline



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Table 7. PowerFLAT 5x6 type R mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
С	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
е		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

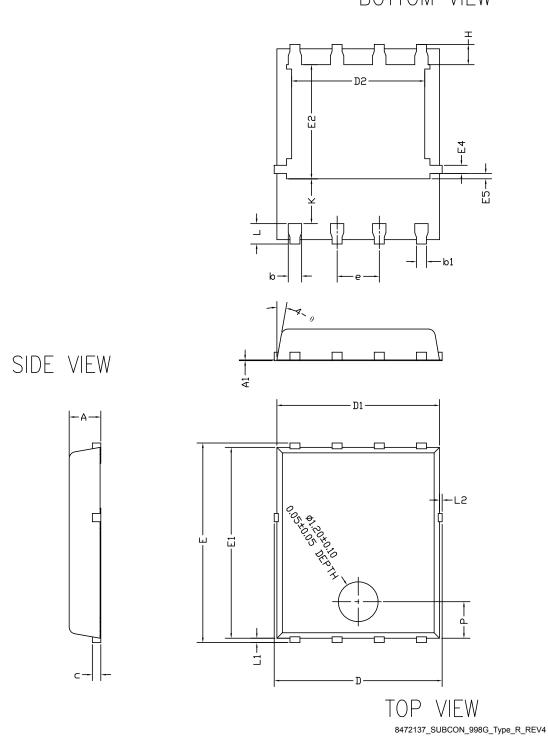
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4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 19. PowerFLAT 5x6 type R SUBCON package outline





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Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data

Dim.	mm				
Dim.	Min.	Тур.	Max.		
Α	0.90	0.95	1.00		
A1		0.02			
b	0.35	0.40	0.45		
b1		0.30			
С	0.21	0.25	0.34		
D			5.10		
D1	4.80	4.90	5.00		
D2	3.91	4.01	4.11		
е	1.17	1.27	1.37		
E	5.90	6.00	6.10		
E1	5.70	5.75	5.80		
E2	3.34	3.44	3.54		
E4	0.15	0.25	0.35		
E5	0.06	0.16	0.26		
Н	0.51	0.61	0.71		
K	1.10				
L	0.51	0.61	0.71		
L1	0.06	0.13	0.20		
L2			0.10		
Р	1.00	1.10	1.20		
θ	8°	10°	12°		

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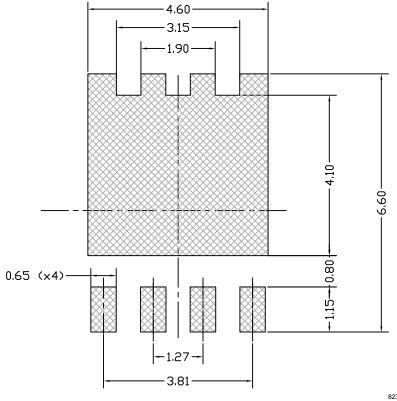


Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)

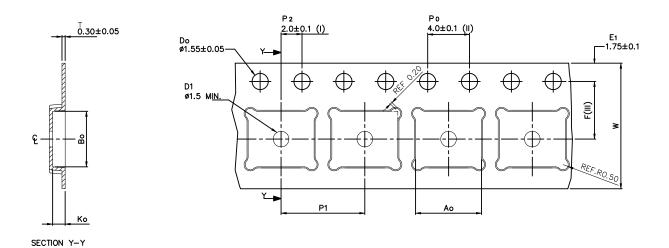
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4.3 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



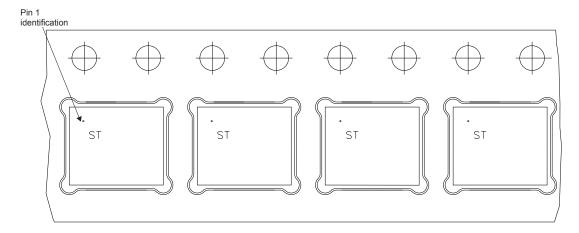
Ao	6.30 +/- 0.1
Во	5.30 +/- 0.1
Ko	1.20 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12 00 1/- 03

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ±0.20.
- (III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape



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PART NO.

R25.00

R25.00

R25.00

R25.00

R1.10

R27.02

R27.

Figure 23. PowerFLAT 5x6 reel

8234350_Reel_rev_C

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Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Apr-2013	1	First release.
		– Modified: R _{DS(on)} value in cover page
		– Modified: V _{GS(th)} values in Table 4
		– Modified: R _{DS(on)} typ. and max values in Table 4
06-Mar-2014	2	– Modified: typical values in Table 5, 6 and 7
00-iviai-2014	2	- Updated: Section 4: Package mechanical data
		- Added: Section 2.1: Electrical characteristics (curves)
		- Updated: Section 4: Package mechanical data
		- Document status promoted from preliminary data to production data
40 Dec 2044	2	- Updated title, features and description in cover page.
16-Dec-2014	3	– Updated R _{DS(on)} values and Figure 7: Static drain-source onresistance.
		-Text edits throughout document
		-Updated cover page title description
		-Updated cover page features table
		-In table 2. Absolute maximum ratings, added "EAS" information and footnote 4
17-Mar-2015	5 4	-In table 3. Thermal data, added footnote 1
17-IVIAI-2015	4	-Renamed table 4. Static (was On/off states)
		-Updated table 5. Dynamic
		-Updated table 7. Source drain diode
		-In Section 2.1 Electrical characteristics (curves), updated figures 2, 3, 10 and 11
		-Updated and renamed Section 4 Package information
		Updated Absolute maximum ratings.
01-Aug-2017	5	Updated Static and Source-drain diode.
017 kg 2017	O	Updated Internal schematic diagram.
		Minor text changes.
29-Aug-2017	6	Updated Table 3. Static.
		Minor text changes.
10-Feb-2020	7	Updated Section 4 Package information.
.5 . 65 2626	,	Minor text changes.

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3	Test	circuits	6
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	4.1	PowerFLAT 5x6 type R package information	7
	4.2	PowerFLAT 5x6 type R SUBCON package information	8
	4.3	PowerFLAT 5x6 packing information	. 11
Rev	Revision history		



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