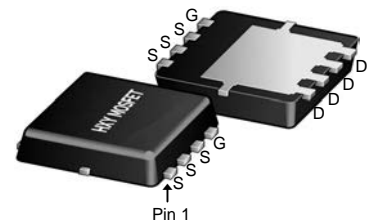




## General Description

The DMTH6004LPSQ-13 use advanced SGT MOSFET technology to provide low  $R_{DS(ON)}$ , low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness.



DFN5X6-8L

## General Features

$V_{DS} = 60V$   $I_D = 125A$

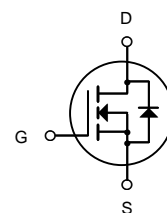
$R_{DS(ON)} < 2.9m\Omega @ V_{GS}=10V$

## Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMTH6004LPSQ-13	DFN5X6-8L	HXY MOSFET	5000

## Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	125	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	101	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	641	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	189	mJ
$P_D @ T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	113	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance from Junction-to-Ambient <sup>3</sup>	1.11	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	39.4	$^\circ C/W$



**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.2	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	2.4	2.9	mΩ
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V,V <sub>GS</sub> =0V, f=1.0MHz	-	4610	6915	pF
C <sub>oss</sub>	Output Capacitance		-	2188	3282	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	66	132	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =40A, V <sub>GS</sub> =10V	-	74.37	111.56	nC
Q <sub>gs</sub>	Gate-Source Charge		-	17.26	-	nC
Q <sub>gd</sub>	Gate-Drain(“Miller”) Charge		-	9.44	18.88	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =40A, R <sub>G</sub> =2.7Ω,V <sub>GS</sub> =10V	-	14.13	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	63.73	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	46.8	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	105.07	-	ns
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	125	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	641	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =40A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> =25℃, I <sub>F</sub> =40A,dI/dt=100A/μs	-	52.78	105.56	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	56.31	112.62	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=30V$ ,  $V_G=10V$ ,  $R_G=25\Omega$ ,  $L=0.5mH$ ,  $I_{AS}=12A$

3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$



## Typical Characteristics

Fig 1: Output Characteristics

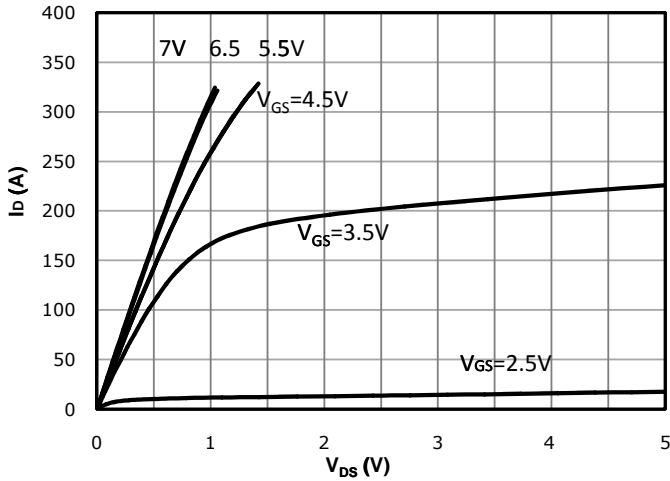


Fig 2: Transfer Characteristics

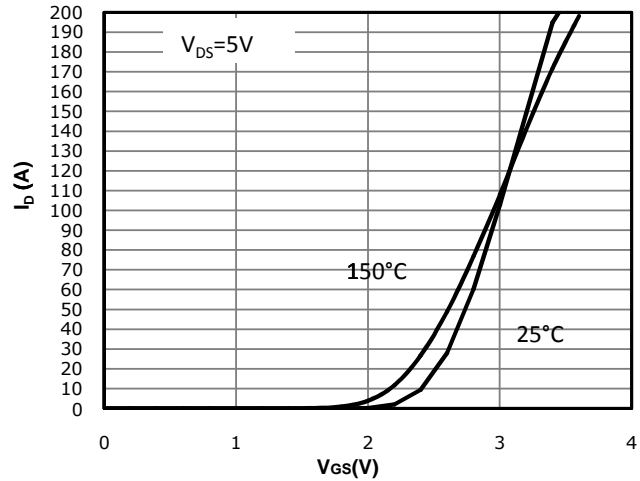


Fig 3:  $R_{DS(on)}$  vs Drain Current and Gate Voltage

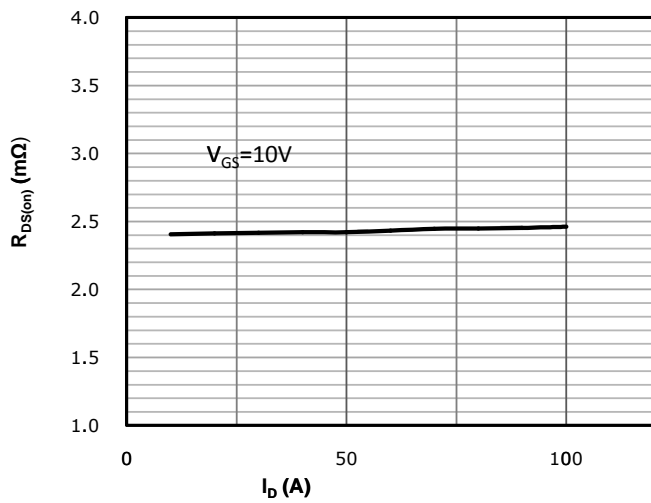


Fig 4:  $R_{DS(on)}$  vs Gate Voltage

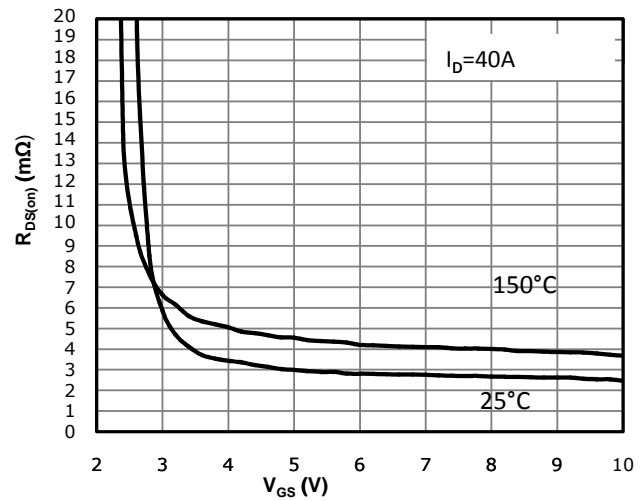


Fig 5:  $R_{DS(on)}$  vs. Temperature

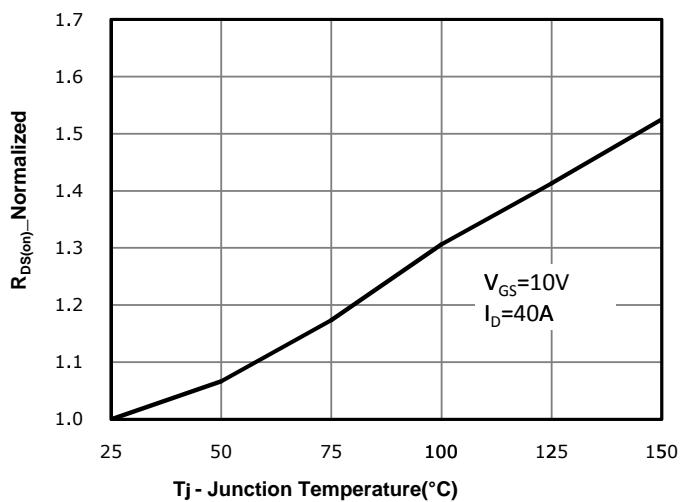


Fig 6: Capacitance Characteristics

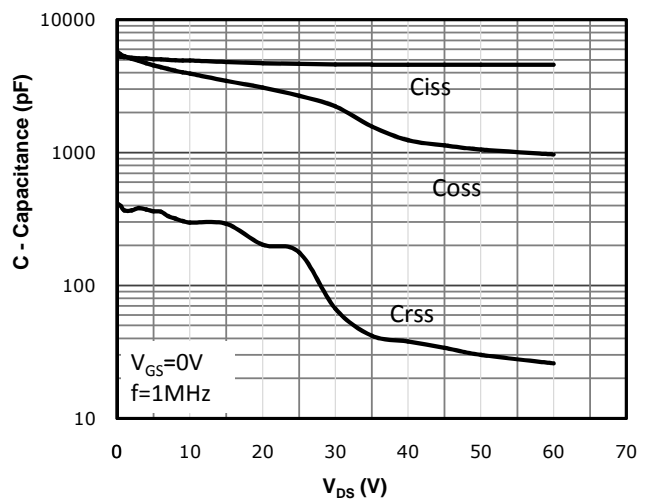




Fig 7: Gate Charge Characteristics

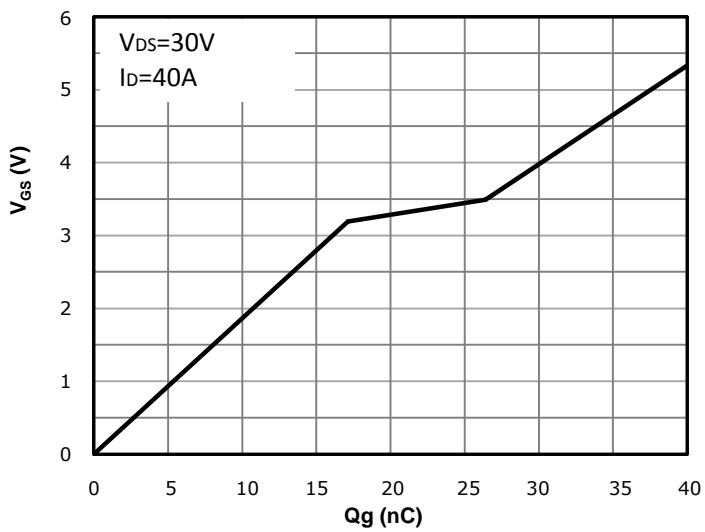


Fig 8: Body-diode Forward Characteristics

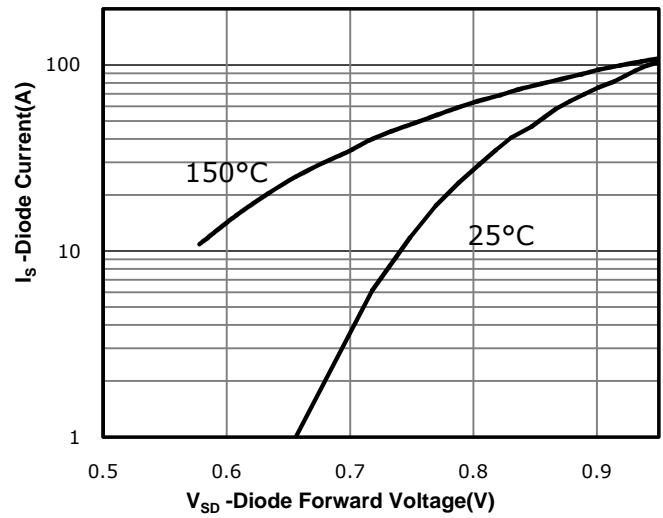


Fig 9: Power Dissipation

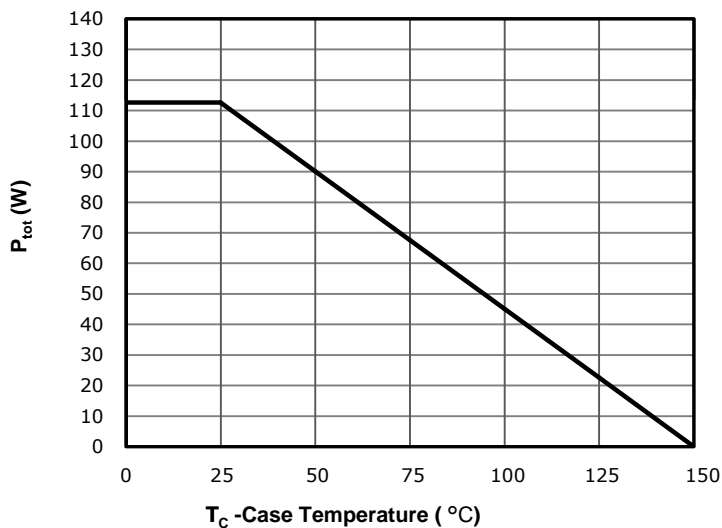


Fig 10: Drain Current Derating

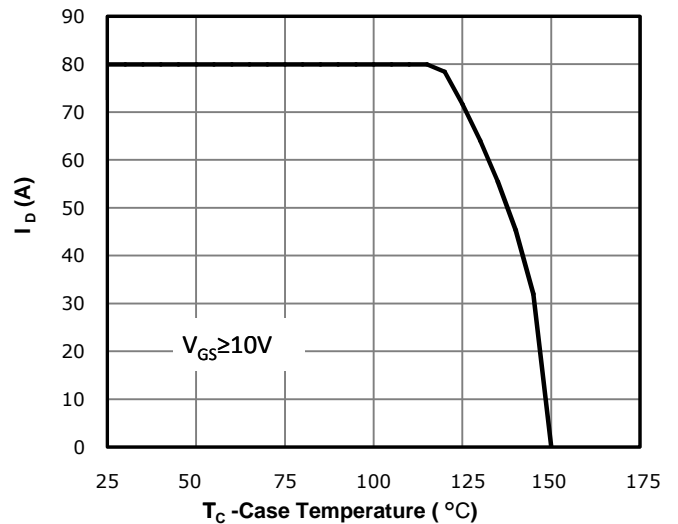


Fig 11: Safe Operating Area

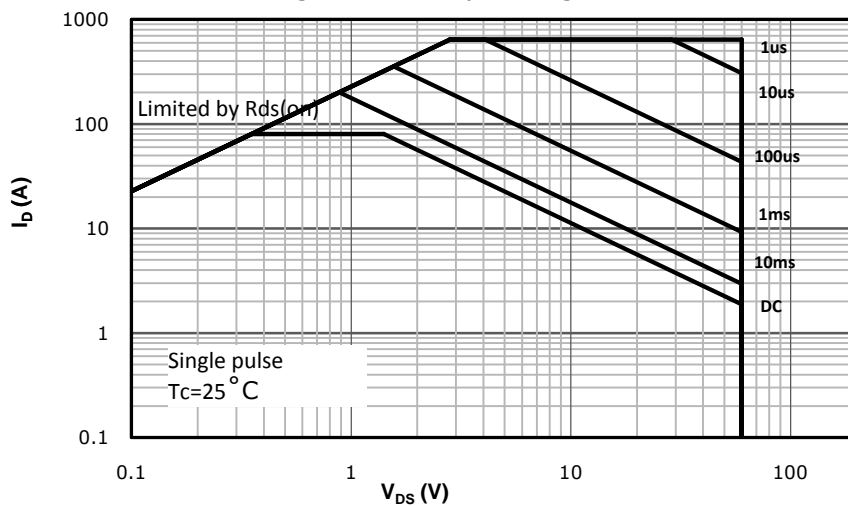
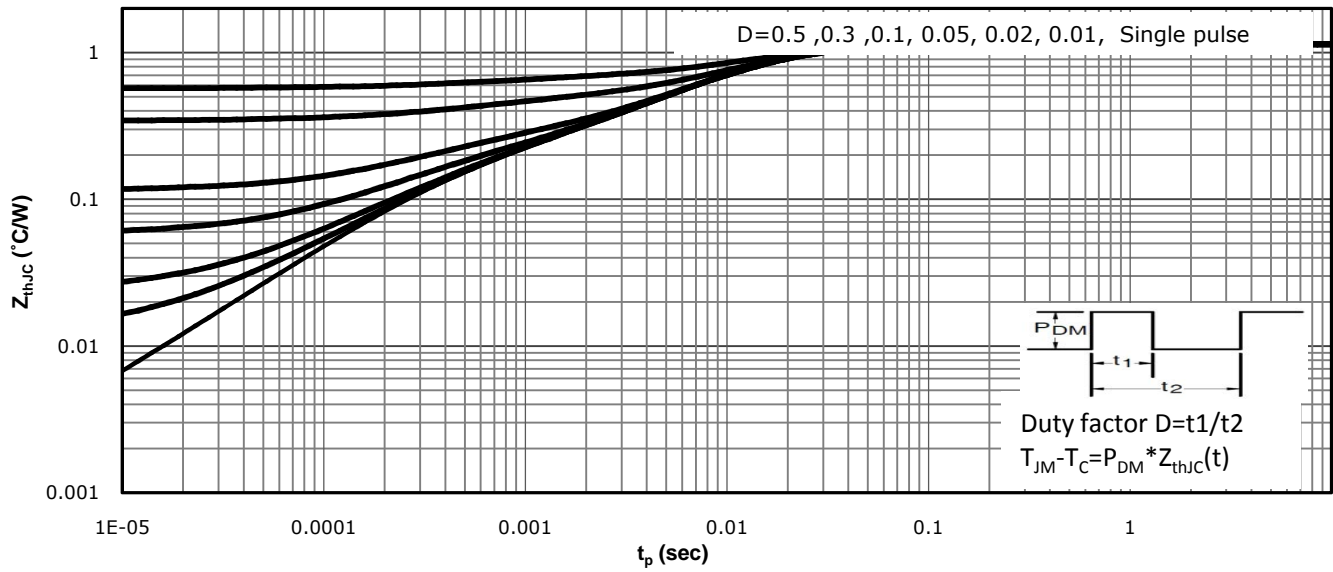


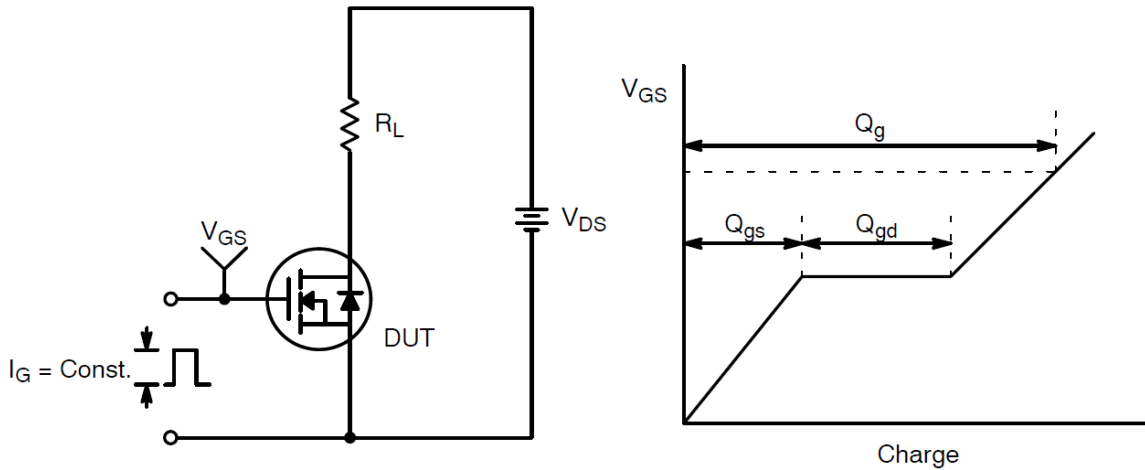


Fig 12: Max. Transient Thermal Impedance

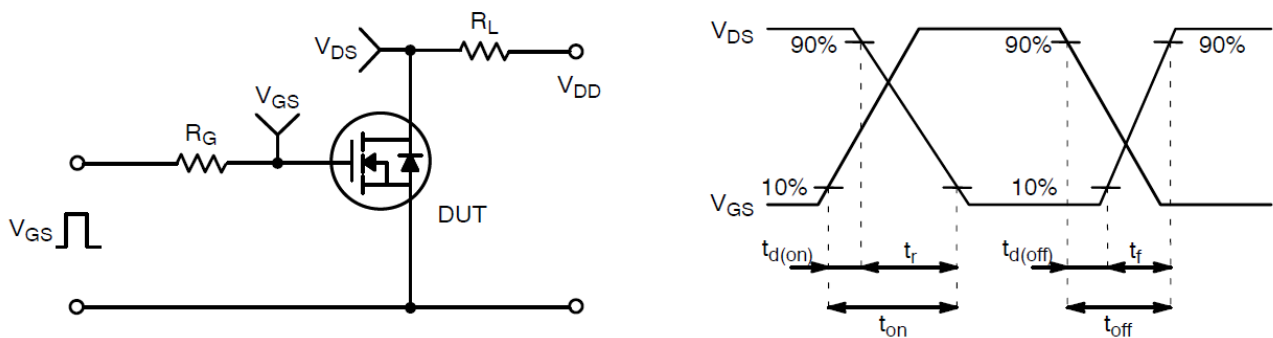




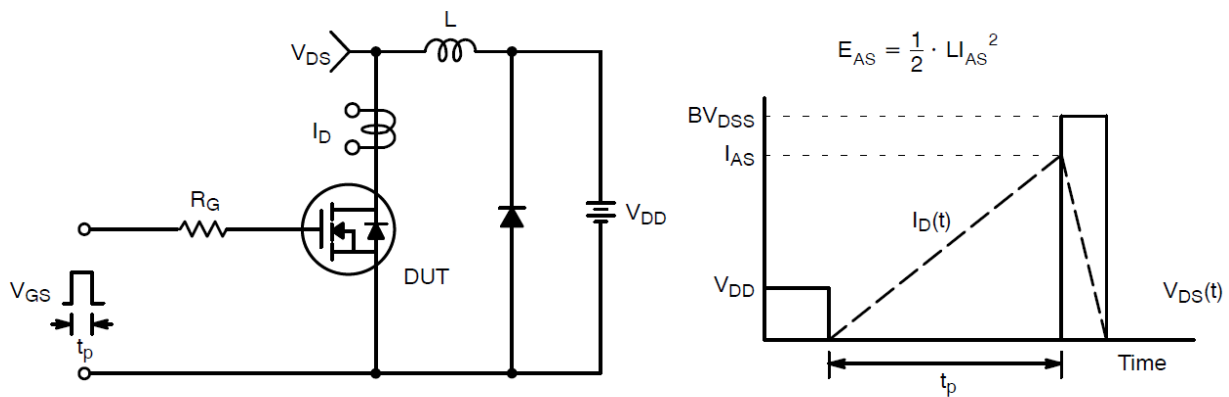
### Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform



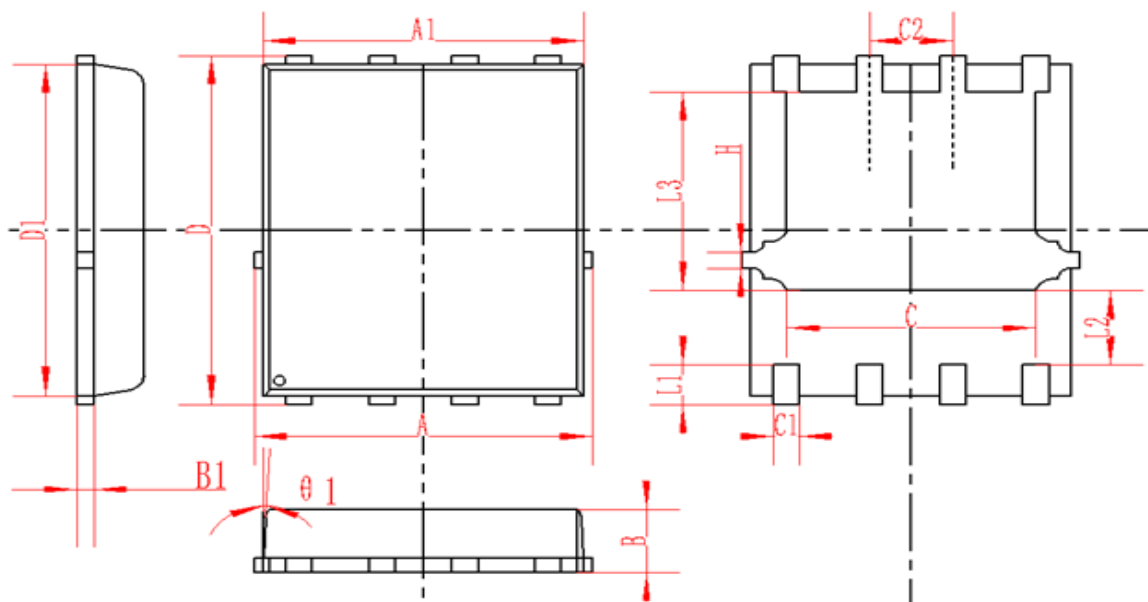
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



## DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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