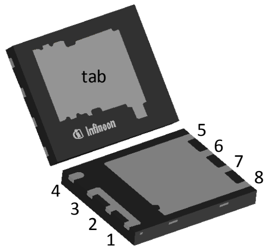
MOSFET

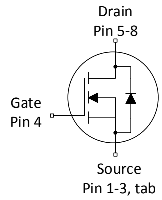
OptiMOS™ Power-MOSFET, 60 V

Features

- Double side cooled package-with lowest Juntion-top thermal resistance
- 175°C rated
- Optimized for synchronous rectification
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection

PG-WSON-8-2





Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.6	mΩ
I_D	234	A
Q_{OSS}	81	nC
Q_G(0V..10V)	71	nC

Type / Ordering Code	Package	Marking	Related Links
BSC016N06NSSC	PG-WSON-8-2	016N06SC	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	234 165 31	A	V_{GS}=10 V, T_C=25 °C[1)] V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2)]
Pulsed drain current[3)]	$I_{D,pulse}$	-	-	936	A	T_C=25 °C
Avalanche energy, single pulse[4)]	E_{AS}	-	-	380	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	167 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	0.4	0.86	K/W	-
Device on PCB, 6 cm² cooling area[2)]	R_{thJA}	-	-	50	K/W	-

[1)] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher Tcase please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3)] See Diagram 3 for more detailed information
[4)] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	V_{DS}=V_{GS}, I_D=95 µA
Zero gate voltage drain current	I_{DSS}	- -	0.5 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.4 1.8	1.6 2.4	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=6 V, I_D=12.5 A
Gate resistance	R_G	-	1.9	2.9	Ω	-
Transconductance	g_{fs}	70	140	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	3900	5200	6500	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	900	1200	1500	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	14	48	96	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	19	38	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	9	18	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	34	70	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	9	18	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	16	22	30	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	10	14	19	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	8.8	13	20	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	14	21	30	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	58	71	95	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	3.7	4.3	4.9	V	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	49	62	86	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	60	81	102	nC	V_{DD}=30 V, V_{GS}=0 V

1) Defined by design. Not subject to production test
2) See figure 16 for gate charge parameter definition. Defined by design, not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	119	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	936	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.84	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	24	61	98	ns	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	39	78	156	nC	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test

4 Electrical characteristics diagrams

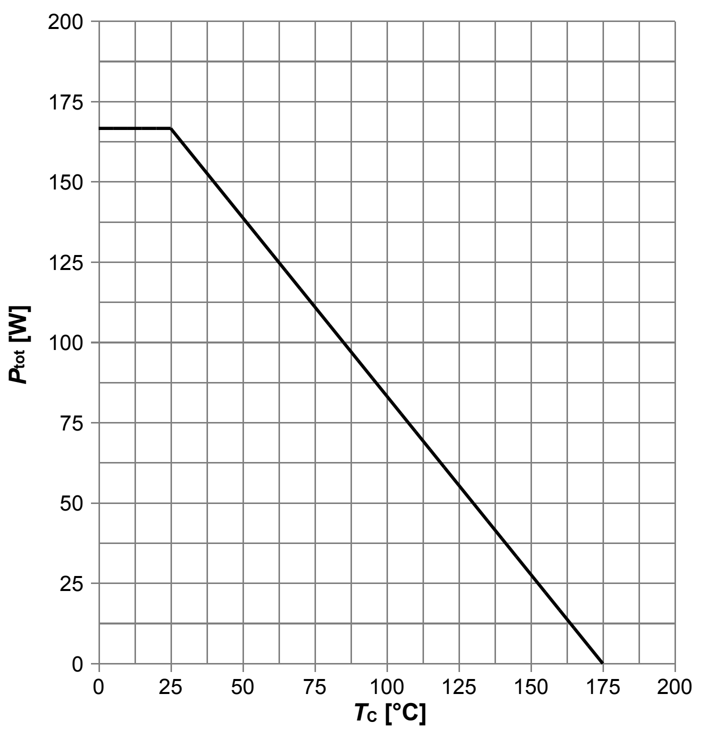
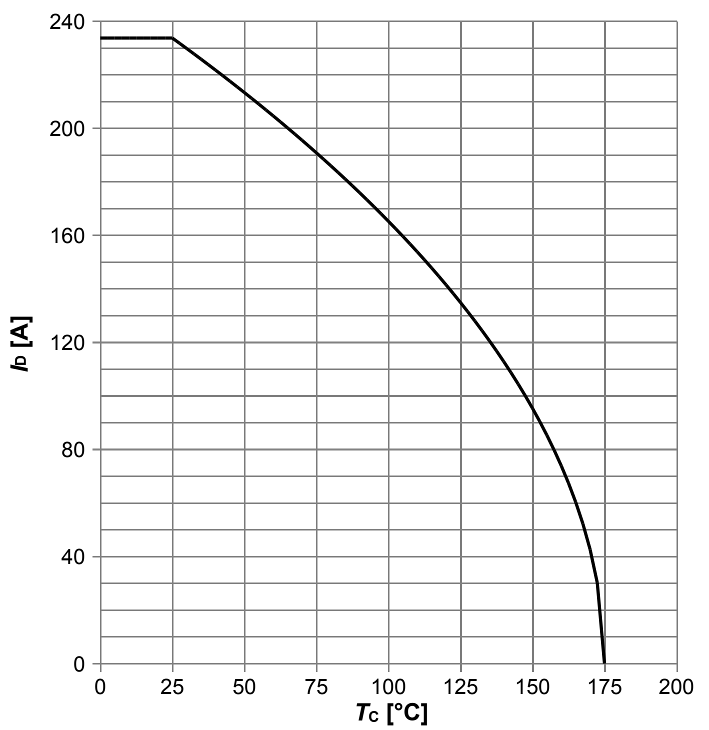
Diagram 1: Power dissipation	Diagram 2: Drain current
	
P_{tot}=f(T_C)	I_D=f(T_C); V_{GS}≥10 V

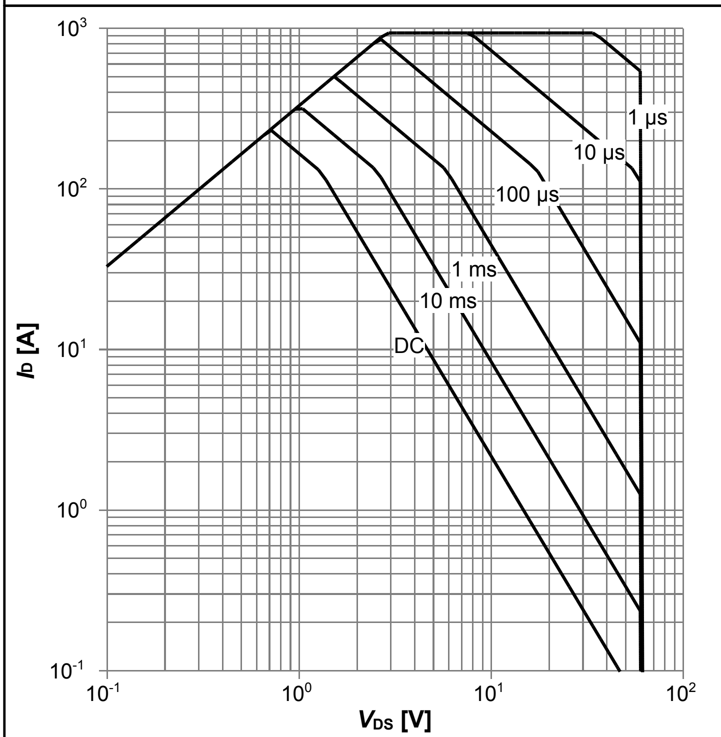
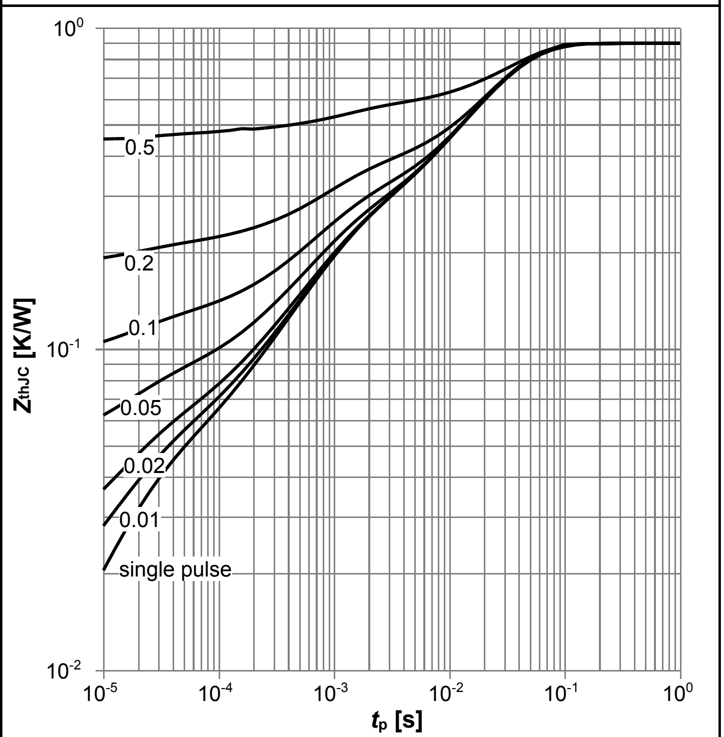
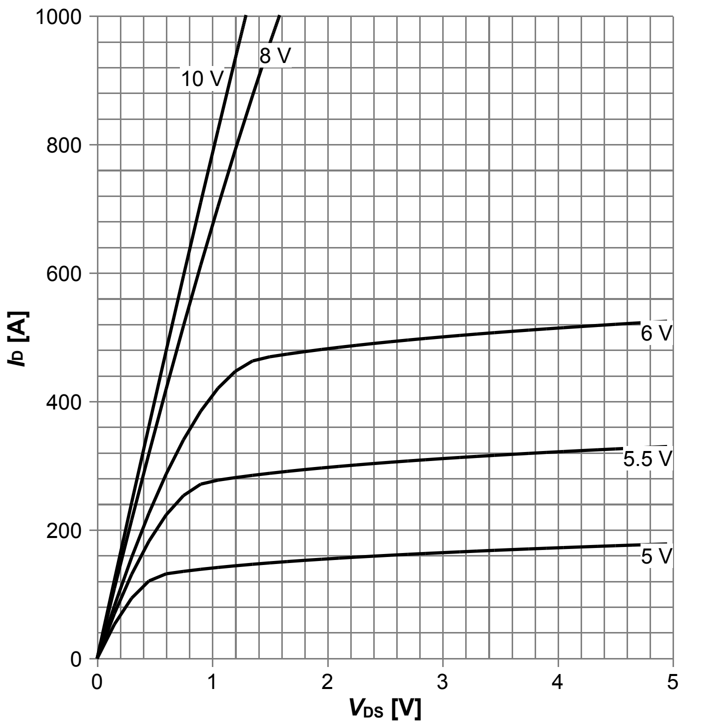
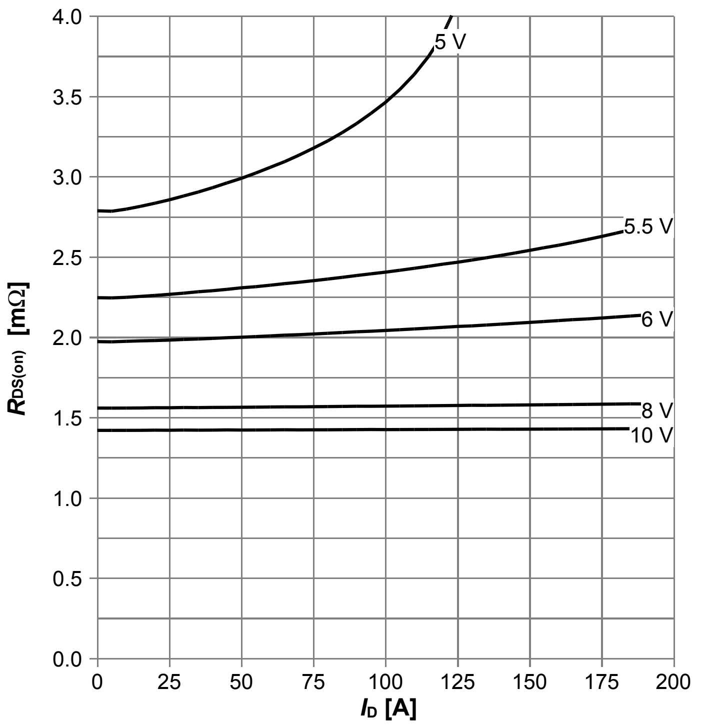
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p	Z_{thJC}=f(t_p); parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



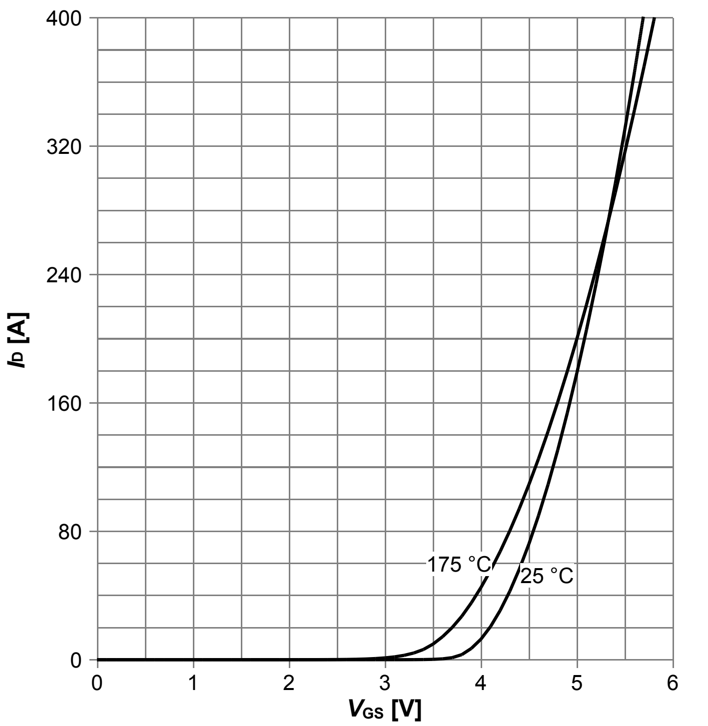
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



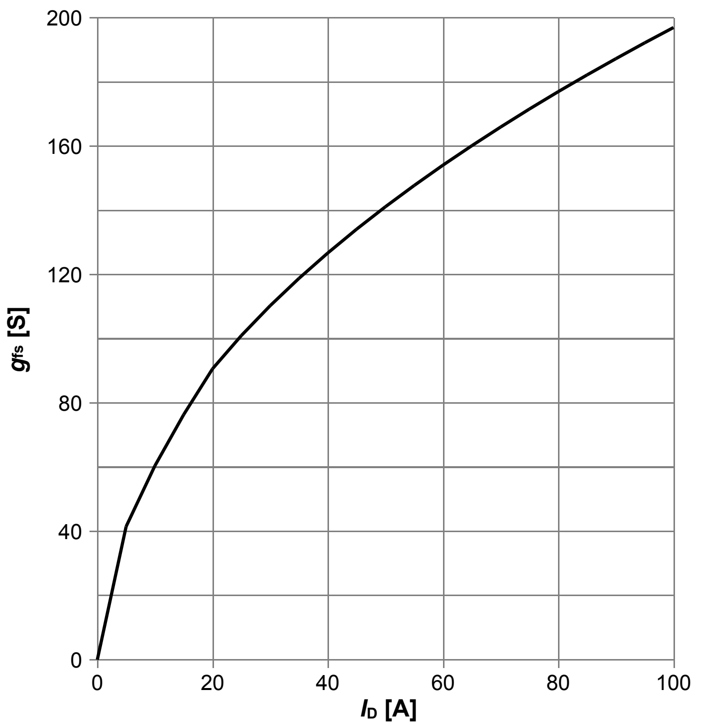
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



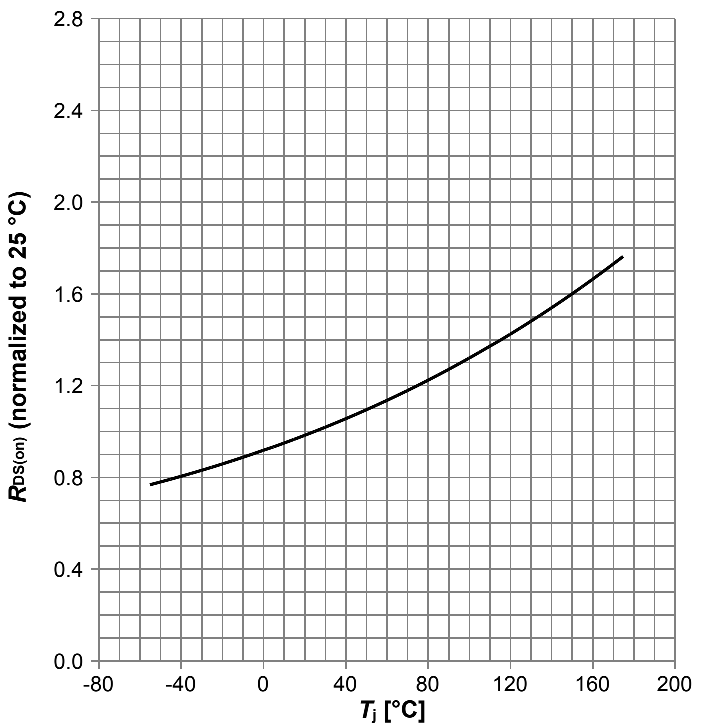
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



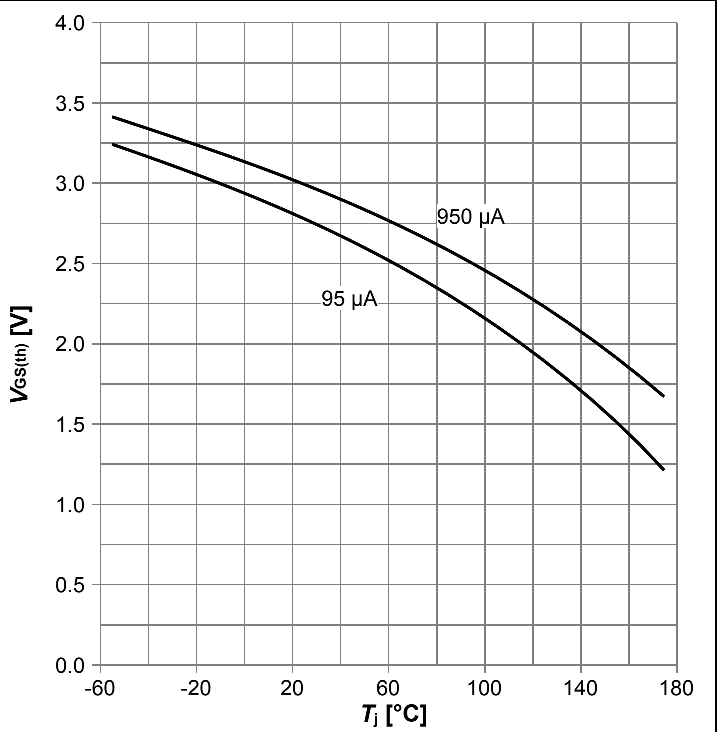
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



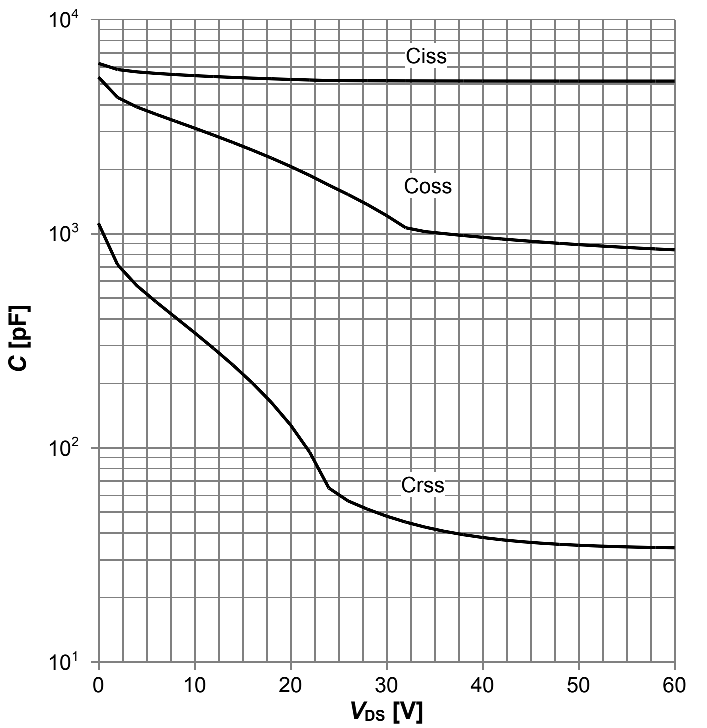
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



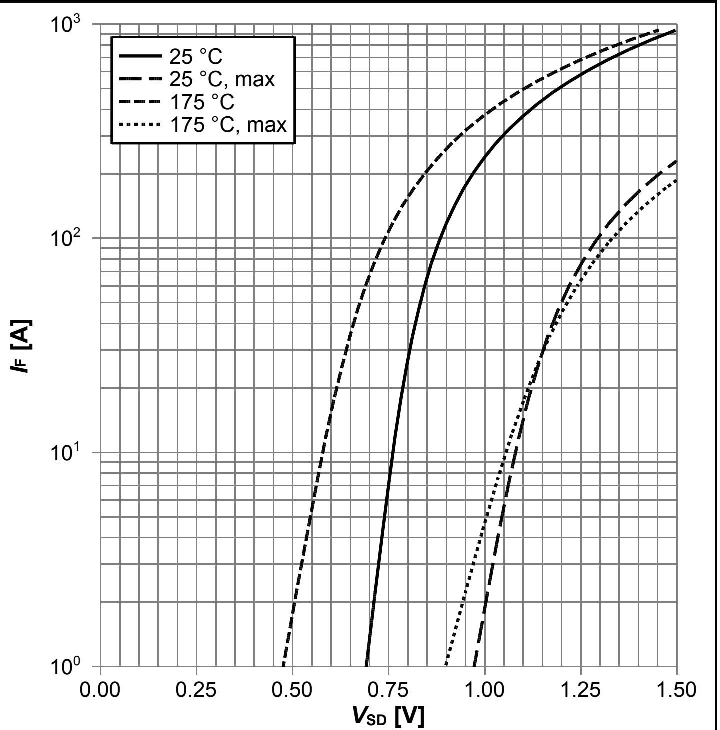
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

Diagram 11: Typ. capacitances



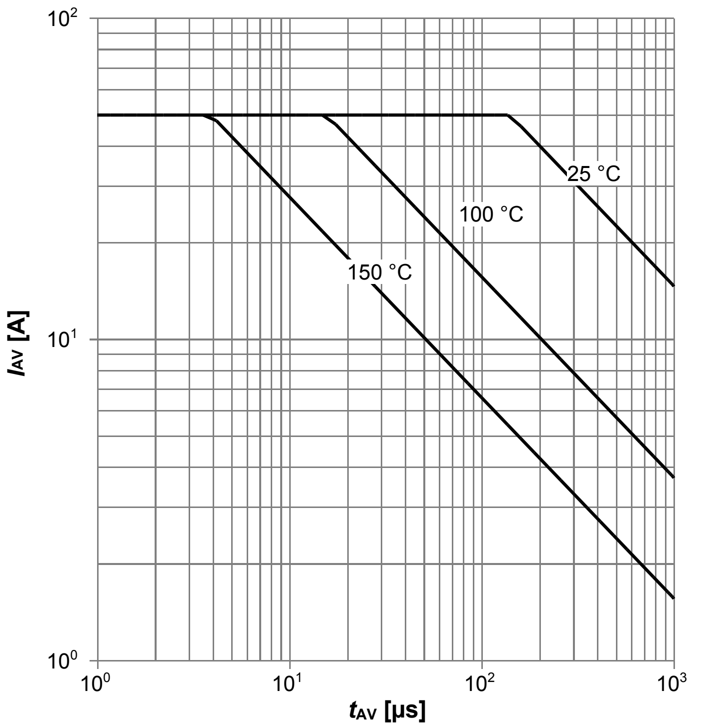
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



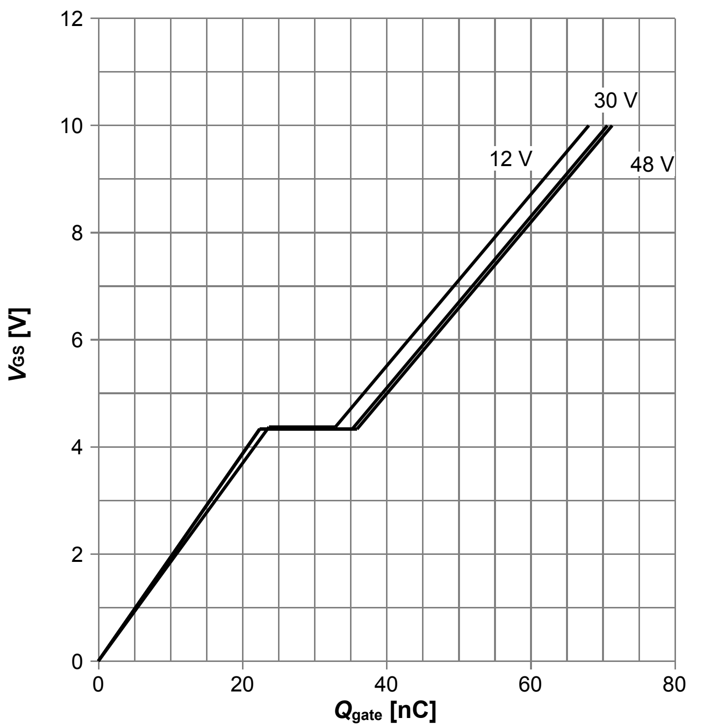
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



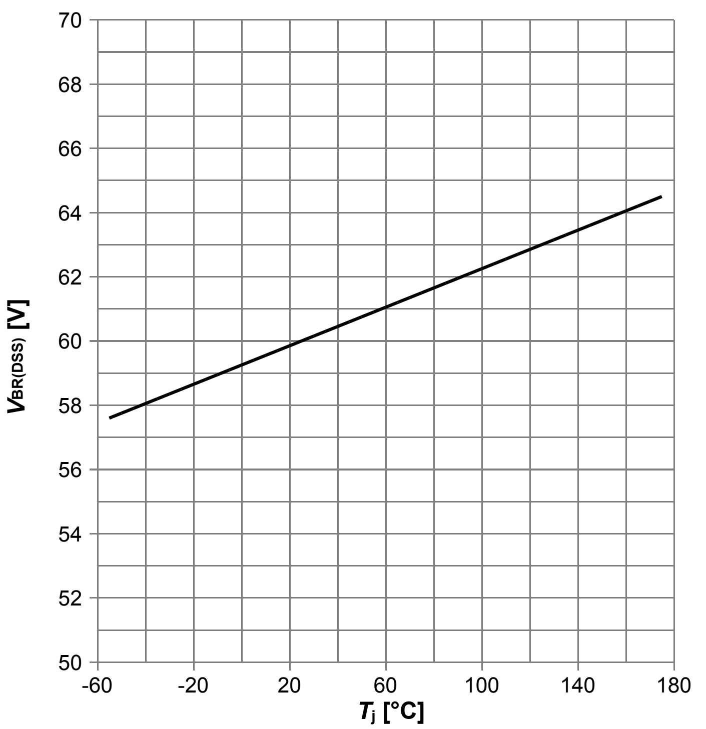
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



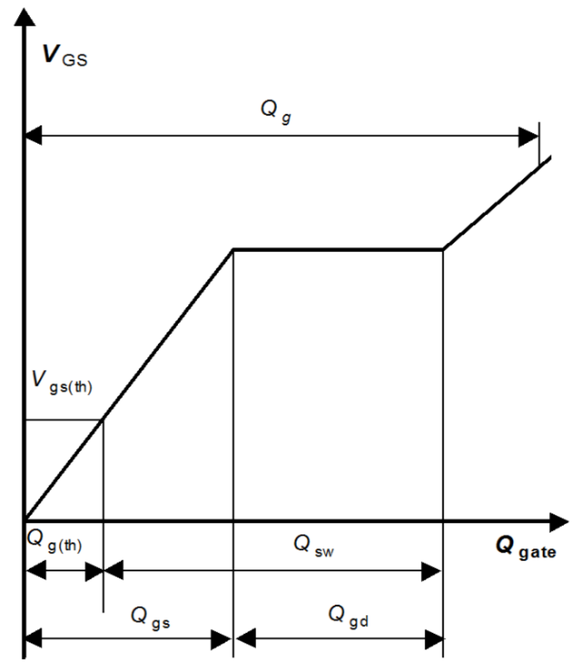
V_{GS}=f(Q_{gate}); I_D=50 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

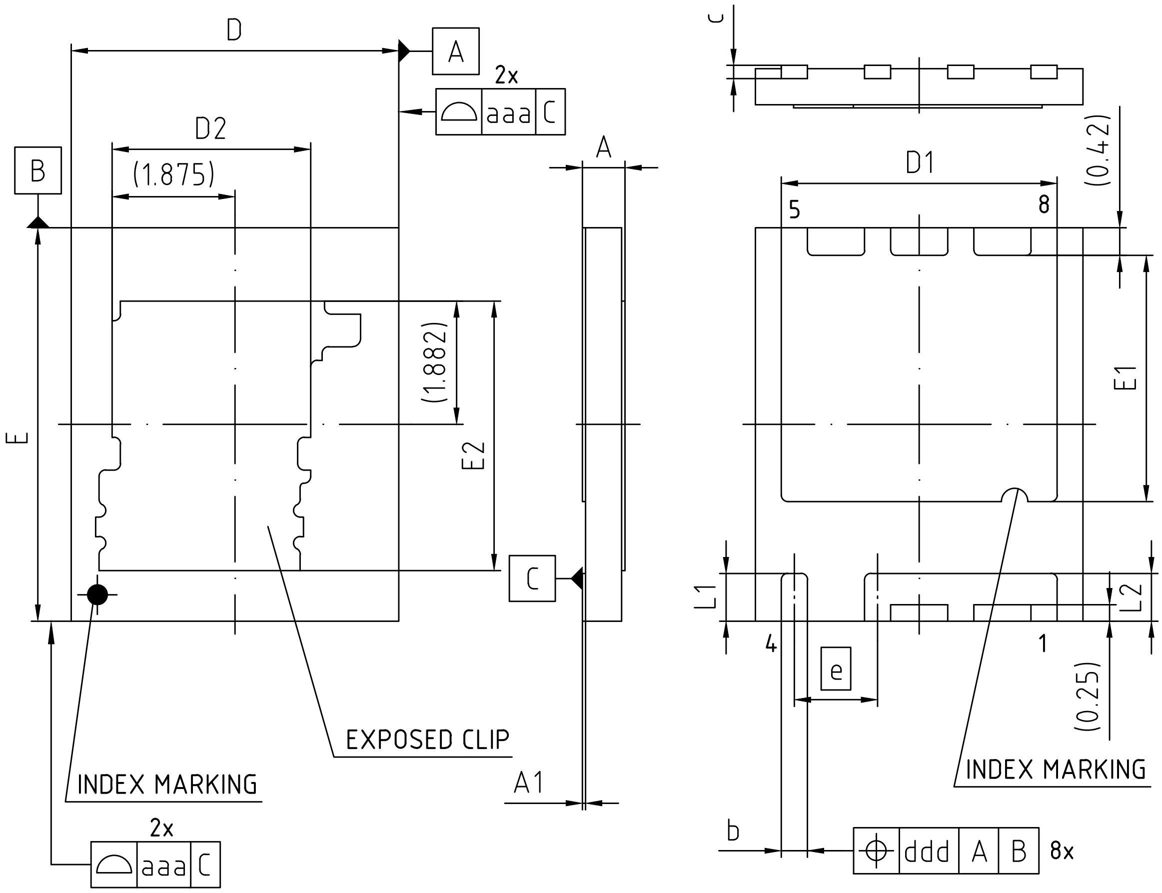


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR MOLD PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	-	0.75
A1	-	0.05
b	0.35	0.45
c	0.203	
D	4.95	5.05
D1	4.11	4.31
D2	3.03	
E	5.95	6.05
E1	3.66	3.86
E2	4.11	
e	1.27	
L1	0.675	0.775
L2	0.625	0.825
aaa	0.05	
ddd	0.10	

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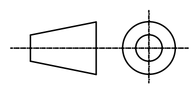
REVISION
03

SCALE 10:1

EUROPEAN PROJECTION



ISSUE DATE
03.06.2019

Figure 1 Outline PG-WSON-8-2, dimensions in mm

Revision History

BSC016N06NSSC

Revision: 2019-10-10, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-10-10	Release of final version

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