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March 2016

# FDB0190N807L

## N-Channel PowerTrench<sup>®</sup> MOSFET

80 V, 270 A, 1.7 m $\Omega$

### Features

- Max  $r_{DS(on)}$  = 1.7 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 34 A
- Max  $r_{DS(on)}$  = 2 m $\Omega$  at  $V_{GS}$  = 8 V,  $I_D$  = 31 A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

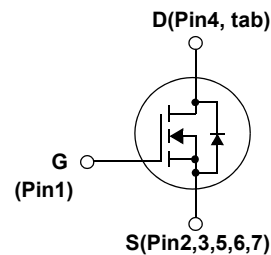
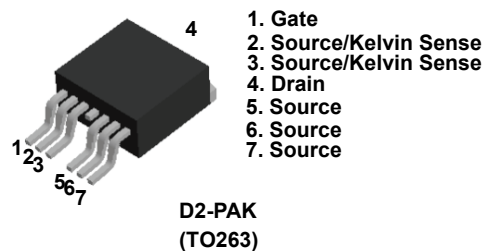


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance while maintaining superior ruggedness and switching performance for industrial applications.

### Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 5)	270	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	190	
	-Pulsed (Note 4)	1440	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	777	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	250	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB0190N807L	FDB0190N807L	D2-PAK-7L	330 mm	24 mm	800 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		34		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		-13		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 34\text{ A}$		1.3	1.7	m $\Omega$
		$V_{GS} = 8\text{ V}$ , $I_D = 31\text{ A}$		1.5	2	
		$V_{GS} = 10\text{ V}$ , $I_D = 34\text{ A}$ , $T_J = 150\text{ }^{\circ}\text{C}$		2.3	4.3	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 34\text{ A}$		133		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		13650	19110	pF
$C_{oss}$	Output Capacitance			1990	2790	pF
$C_{rss}$	Reverse Transfer Capacitance			235	330	pF
$R_g$	Gate Resistance			2.9		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$ , $I_D = 34\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		60	96	ns
$t_r$	Rise Time			78	125	ns
$t_{d(off)}$	Turn-Off Delay Time			98	157	ns
$t_f$	Fall Time			50	80	ns
$Q_g$	Total Gate Charge	$V_{DD} = 40\text{ V}$ , $I_D = 34\text{ A}$ , $V_{GS} = 10\text{ V}$		178	249	nC
$Q_{gs}$	Gate to Source Gate Charge			60		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			32		nC

**Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current				270	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current				1440	A
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 34 A (Note 2)		0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 34 A, di/dt = 100 A/μs		89	142	ns
Q <sub>rr</sub>	Reverse Recovery Charge			103	165	nC

Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

a)  $40\text{ }^{\circ}\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz. copper.

b)  $62.5\text{ }^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz. copper.

2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3.  $E_{AS}$  of 777 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 72\text{ A}$ ,  $V_{DD} = 72\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 104\text{ A}$ .

4. Pulsed  $I_D$  please refer to Figure "Forward Bias Safe Operating Area" for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

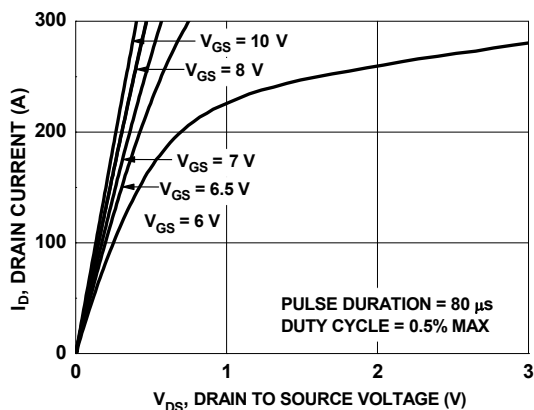


Figure 1. On Region Characteristics

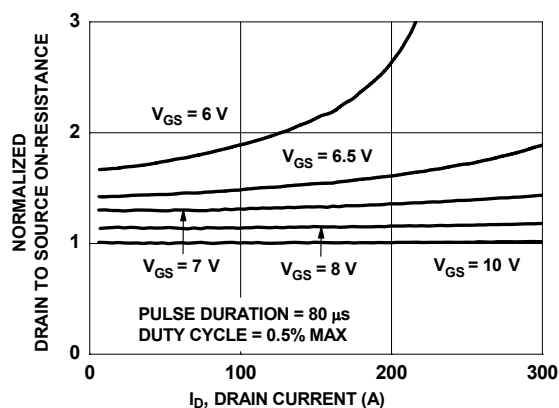


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

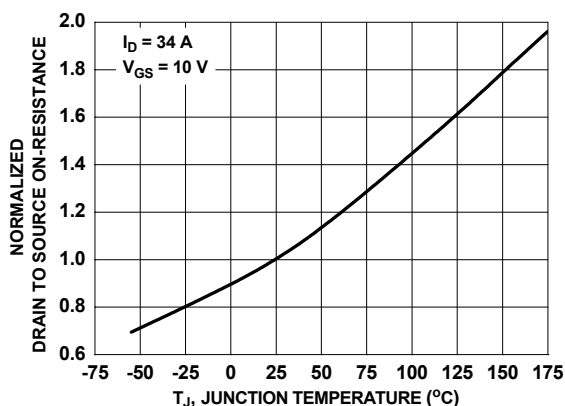


Figure 3. Normalized On Resistance vs. Junction Temperature

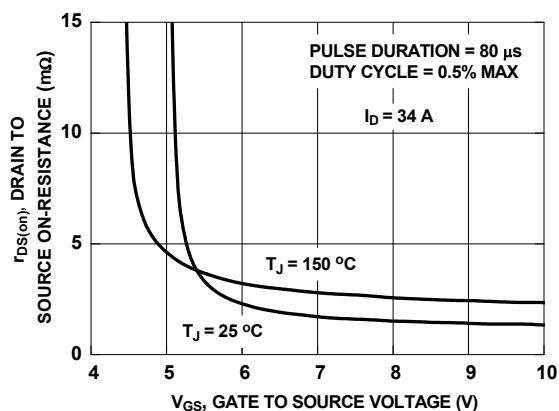


Figure 4. On-Resistance vs. Gate to Source Voltage

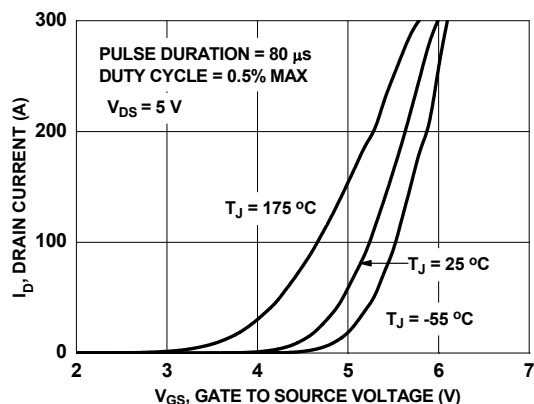


Figure 5. Transfer Characteristics

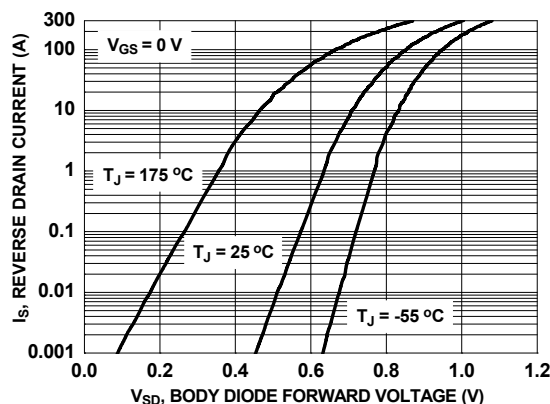


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

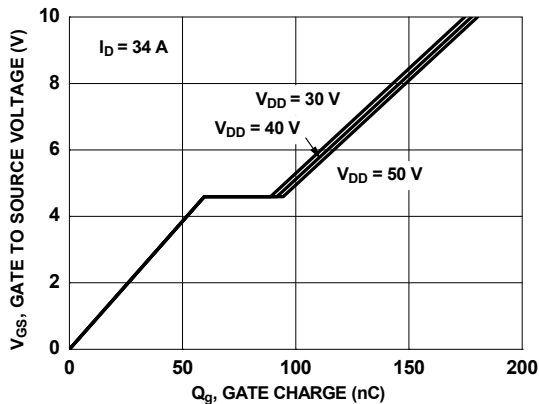


Figure 7. Gate Charge Characteristics

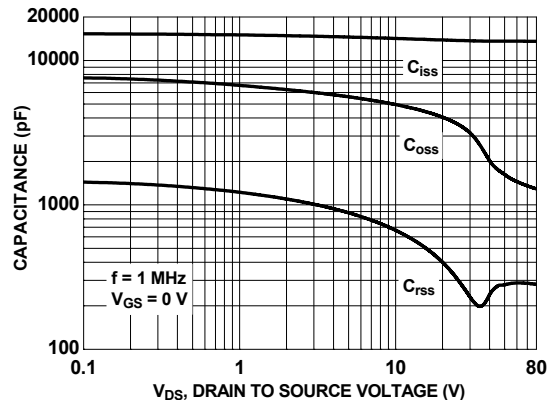


Figure 8. Capacitance vs. Drain to Source Voltage

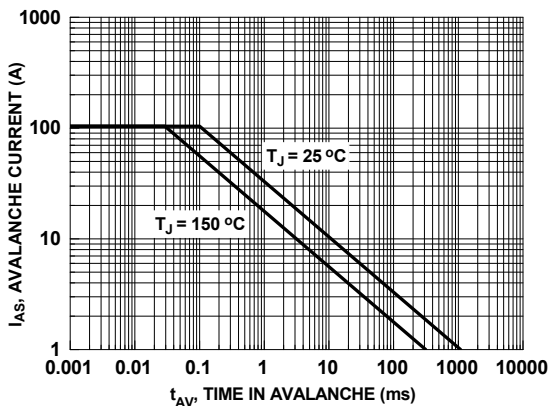


Figure 9. Unclamped Inductive Switching Capability

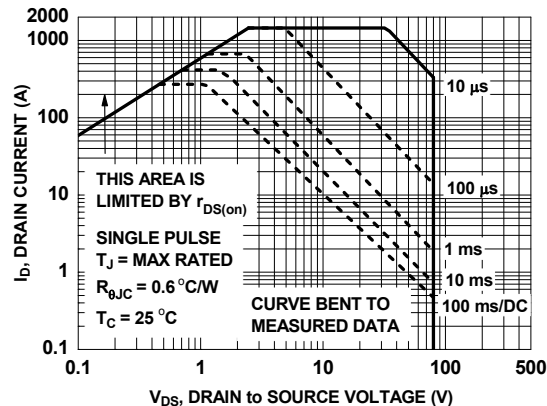


Figure 10. Forward Bias Safe Operating Area

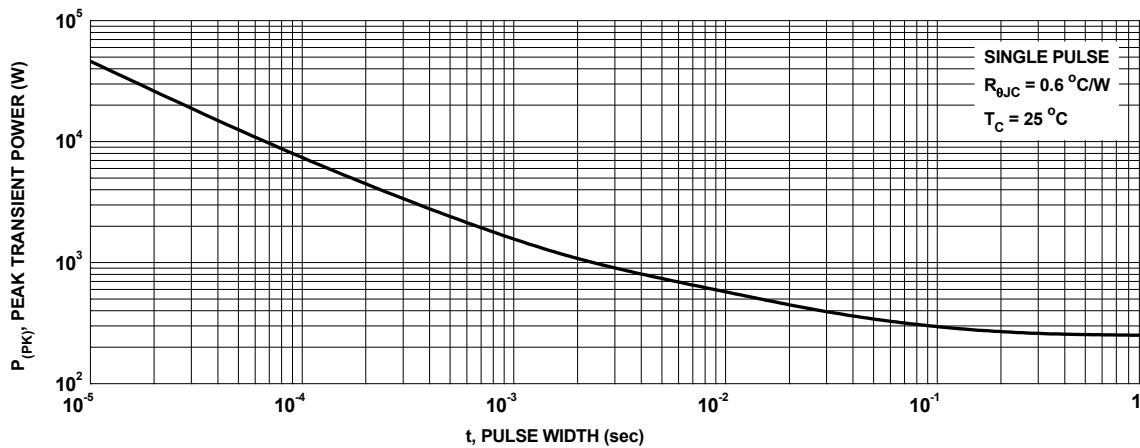


Figure 11. Single Pulse Maximum Power Dissipation

# Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

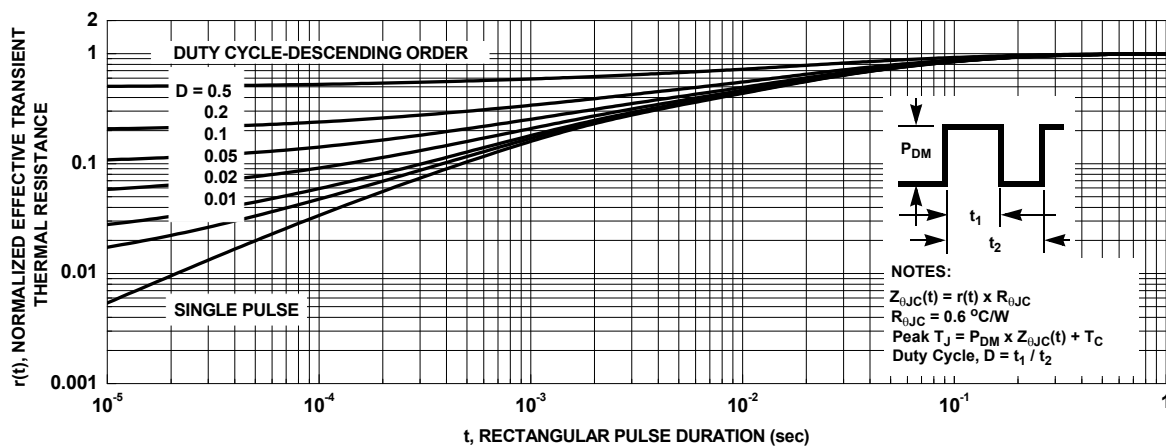
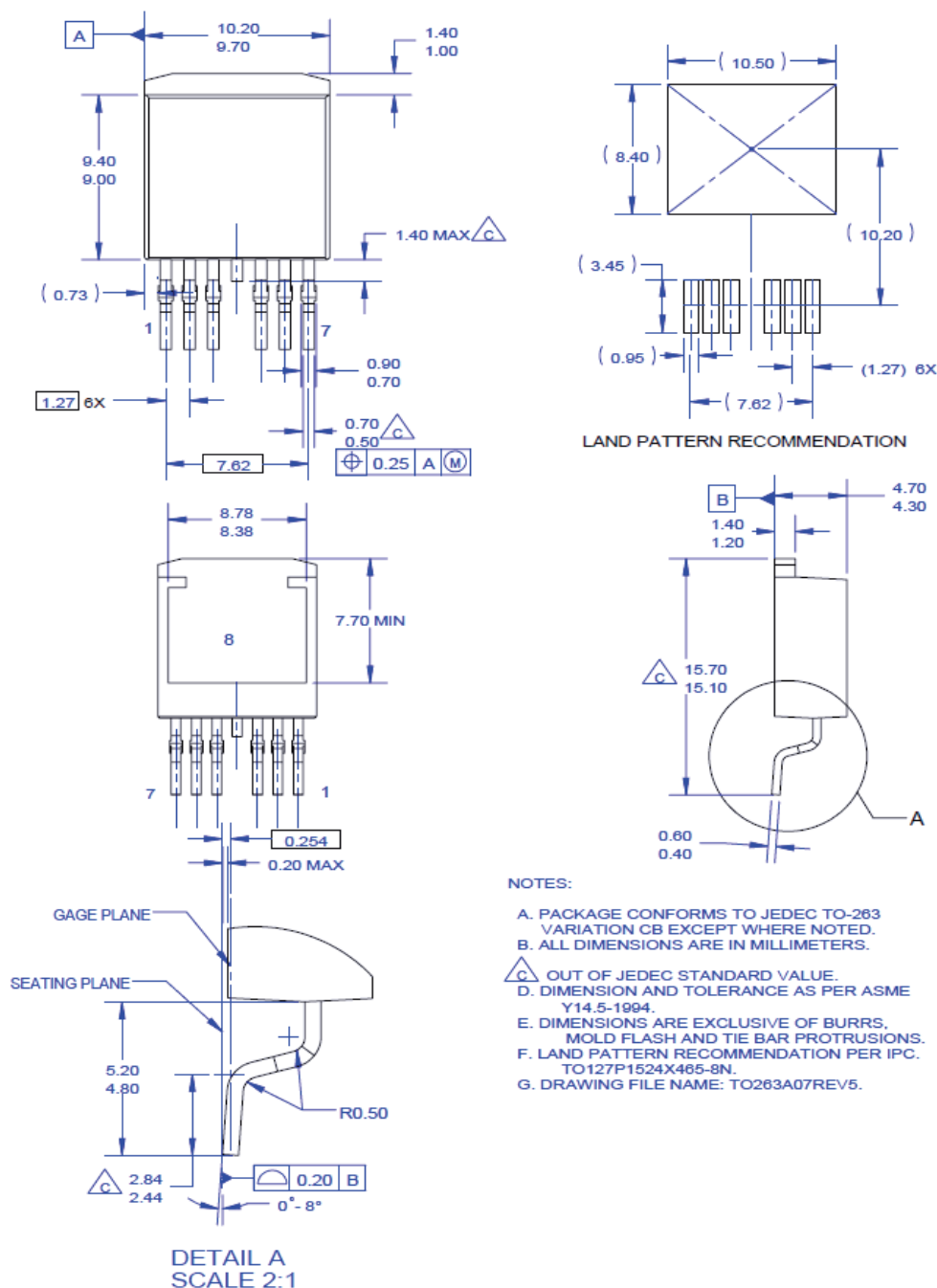


Figure 12. Junction-to-Case Transient Thermal Response Curve

# Dimensional Outline and Pad Layout



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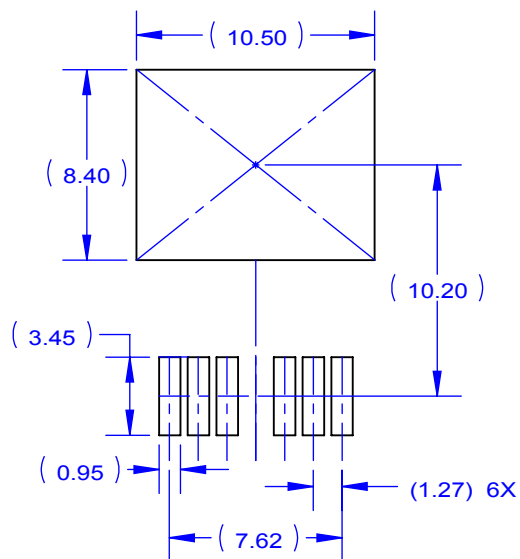
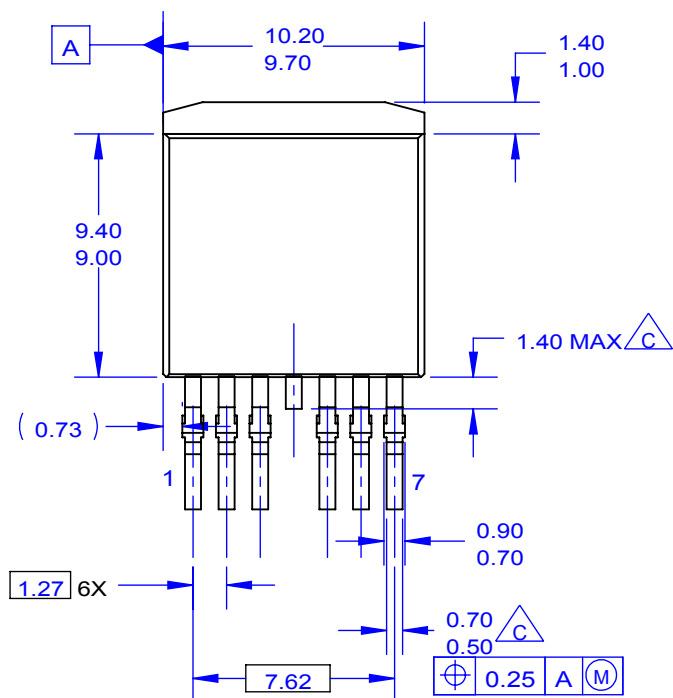
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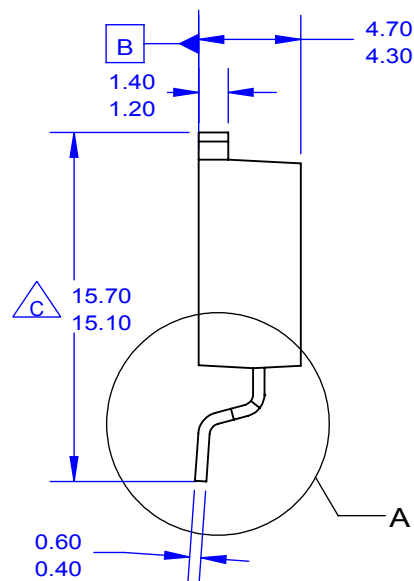
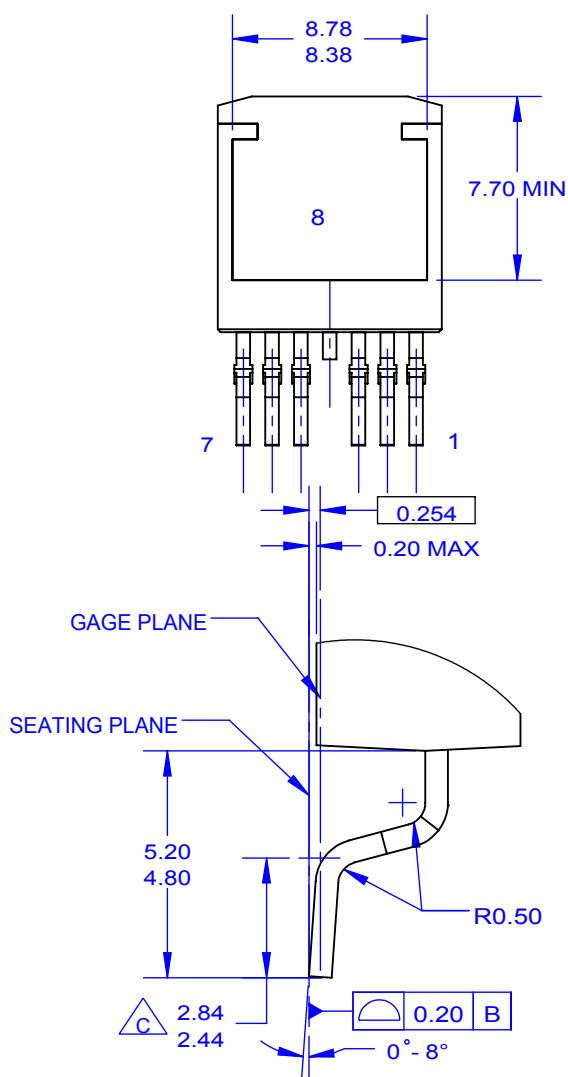
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