

OptiMOS®-T Power-Transistor





Product Summary

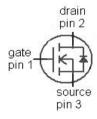
V_{DS}	120	V
R _{DS(on),max} (SMD version)	15.4	mΩ
I _D	50	Α

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

PG-TO263-3-2	PG-TO262-3-1	PG-TO220-3-1
2 (tab)	123	12,3

Туре	Package	Marking
IPB50N12S3L-15	PG-TO263-3-2	3N12L15
IPI50N12S3L-15	PG-TO262-3-1	3N12L15
IPP50N12S3L-15	PG-TO220-3-1	3N12L15



Maximum ratings, at T_i =25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I _D	T _C =25 °C, V _{GS} =10 V	50	А
		T _C =100 °C, V _{GS} =10 V ¹⁾	37	
Pulsed drain current ¹⁾	I _{D,pulse}	T _C =25 °C	200	
Avalanche energy, single pulse ¹⁾	E _{AS}	I _D =25A	330	mJ
Avalanche current, single pulse	IAS	-	50	А
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T _C =25 °C	100	W
Operating and storage temperature	$T_{\rm j}$, $T_{\rm stg}$	-	-55 +175	°C

IPB50N12S3L-15 IPI50N12S3L-15, IPP50N12S3L-15

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics ¹⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ²⁾	-	-	40	

Electrical characteristics, at T_j =25 °C, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	V _{(BR)DSS}	V_{GS} =0V, I_D = 1mA	120	-	-	V
Gate threshold voltage	$V_{\rm GS(th)}$	$V_{\rm DS}=V_{\rm GS}, I_{\rm D}=60\mu{\rm A}$	1.2	1.7	2.4	
Zero gate voltage drain current	I _{DSS}	$V_{\rm DS}$ =120V, $V_{\rm GS}$ =0V, $T_{\rm j}$ =25°C	1	0.01	0.1	μA
		$V_{\rm DS}$ =120V, $V_{\rm GS}$ =0V, $T_{\rm j}$ =125°C ²⁾	1	1	10	
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V	1	1	100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =50A	1	16.1	20.9	mΩ
		$V_{\rm GS}$ =4.5V, $I_{\rm D}$ =50A, SMD version	-	15.8	20.6	
		V _{GS} =10V, I _D =50A	-	13.1	15.7	
		$V_{\rm GS}$ =10V, $I_{\rm D}$ =50A, SMD version	-	12.8	15.4	



Parameter	Symbol	mbol Conditions		Values		
			min.	typ.	max.	
Dynamic characteristics ¹⁾						
Input capacitance	Ciss		-	3215	4180	pF
Output capacitance	Coss	$V_{\rm GS}$ =0V, $V_{\rm DS}$ =25V, f =1MHz	-	730	949	1
Reverse transfer capacitance	C _{rss}		-	63	95	
Turn-on delay time	$t_{d(on)}$		-	10	-	ns
Rise time	$t_{\rm r}$	V_{DD} =20 V, V_{GS} =10 V,	-	5	-	
Turn-off delay time	$t_{d(off)}$	I_{D} =50 A, R_{G} =3.5 Ω	-	28	-	1
Fall time	t_{f}		-	5	-	
Gate Charge Characteristics ¹⁾						_
Gate to source charge	Q _{gs}		-	11	14	nC
Gate to drain charge	Q_{gd}	$V_{\rm DD} = 96 \text{V}, I_{\rm D} = 70 \text{A},$ $V_{\rm GS} = 0 \text{ to } 10 \text{V}$	-	8	12	
Gate charge total	Qg		-	44	57	
Gate plateau voltage	$V_{ m plateau}$		-	3.7	-	V
Reverse Diode						
Diode continous forward current ¹⁾	Is	- T _C =25°C	-	-	50	А
Diode pulse current ¹⁾	I _{S,pulse}	7 _C =25 C	-	-	200	
Diode forward voltage	V_{SD}	V _{GS} =0 V, I _F =50 A, T _j =25 °C	0.6	1	1.2	V
Reverse recovery time ¹⁾	t _{rr}	V_{R} =50V, I_{F} = I_{S} , di_{F}/dt =100A/ μ s	-	80	-	ns
Reverse recovery charge ¹⁾	Q _{rr}		-	185	-	nC

¹⁾ Defined by design. Not subject to production test.

 $^{^{2)}}$ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air



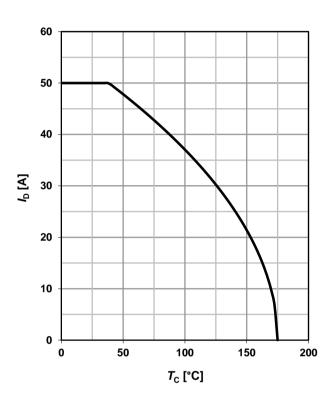
1 Power dissipation

$$P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} = 10 \text{ V}$$

120 100 80 40 20 0 0 50 100 150 200 T_C [°C]

2 Drain current

$$I_{\rm D} = f(T_{\rm C}); \ V_{\rm GS} = 10 \ \rm V; \ SMD$$



3 Safe operating area

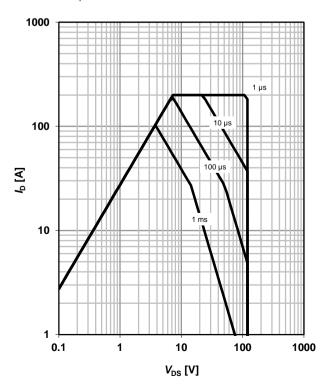
$$I_D = f(V_{DS}); T_C = 25 \,^{\circ}C; D = 0; SMD$$

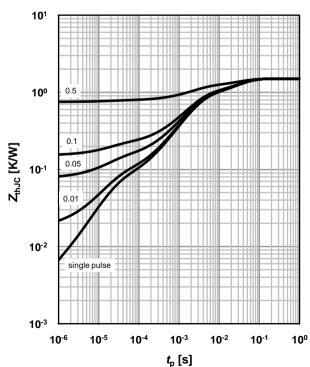
parameter: t_p

4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

parameter: $D=t_p/T$







5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25 \text{ °C}; SMD$

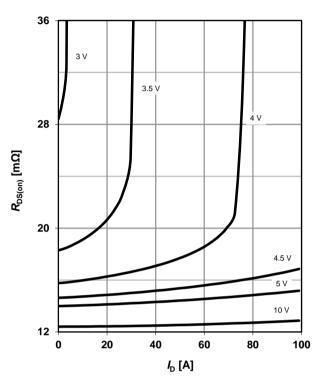
parameter: V_{GS}

200 180 160 4.5 V 140 120 **₹** 100 80 60 3.5 V 40 20 3 V 0 3 $V_{\rm DS}$ [V]

6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_i = 25 \text{ °C}; SMD$

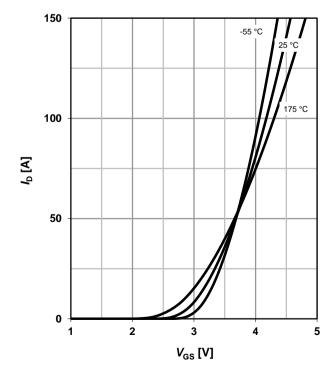
parameter: V_{GS}



7 Typ. transfer characteristics

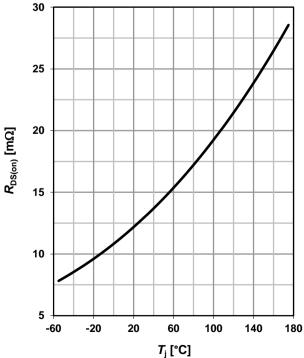
 $I_D = f(V_{GS}); V_{DS} = 6V$

parameter: $T_{\rm j}$



8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}; SMD$





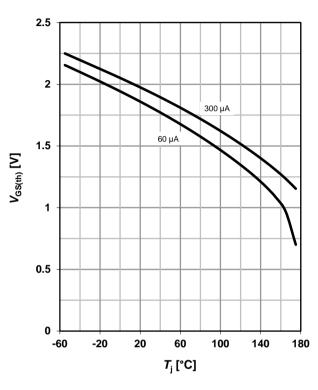
9 Typ. gate threshold voltage

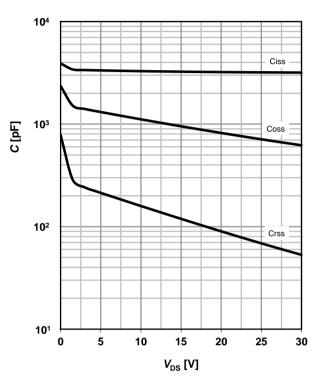
 $V_{GS(th)} = f(T_i); V_{GS} = V_{DS}$

parameter: I_D

10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$





11 Typical forward diode characteristics

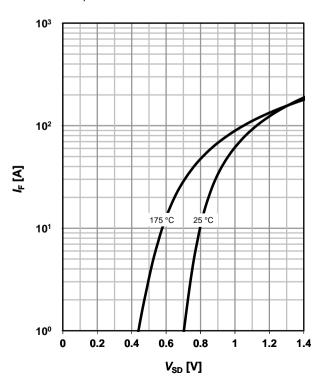
 $IF = f(V_{SD})$

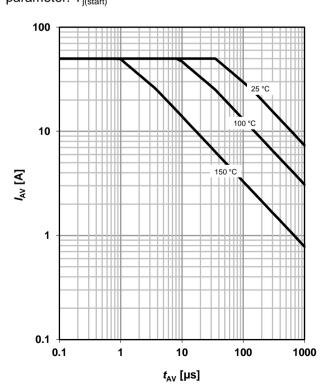
parameter: T_i

12 Typ. avalanche characteristics

 $I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$







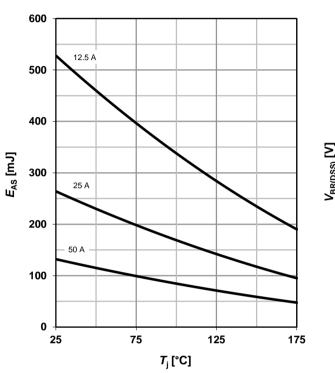
13 Typical avalanche energy

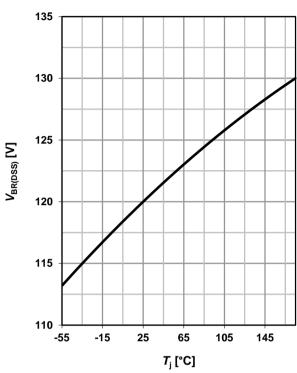
$E_{AS} = f(T_i)$

parameter: I_D

14 Typ. drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_i); I_D = 1 \text{ mA}$$

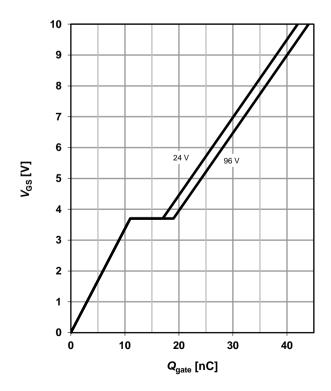




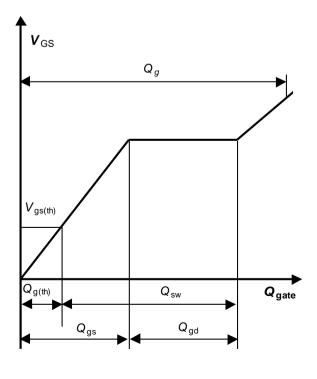
15 Typ. gate charge

 $V_{GS} = f(Q_{gate}); I_D = 50 A pulsed$

parameter: V_{DD}



16 Gate charge waveforms





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Revision History

Version	Date	Changes
Revision 1.0	20.06.2016	Final Data Sheet