eGaN® FET DATASHEET EPC2052

# **EPC2052 – Enhancement Mode Power Transistor**

 $V_{DS}$  , 100 V  $R_{DS(on)}$  , 13.5 m $\Omega$   $I_{D}$  , 8.2 A









Revised September 26, 2022

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



	Maximum Ratings				
	PARAMETER	VALUE	UNIT		
\ \ \	Drain-to-Source Voltage (Continuous)	100	V		
V <sub>DS</sub>	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120			
	Continuous (T <sub>A</sub> = 25°C)	8.2	Α		
I <sub>D</sub>	Pulsed (25°C, $T_{PULSE} = 300 \mu s$ )	74			
V	Gate-to-Source Voltage	6			
V <sub>GS</sub>	Gate-to-Source Voltage	-4	V		
TJ	Operating Temperature -40 to 150		°C		
T <sub>STG</sub>	Storage Temperature	-40 to 150			

	Thermal Characteristics				
	PARAMETER	TYP	UNIT		
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2			
R <sub>OJB</sub> Thermal Resistance, Junction-to-Board 15 °C/		°C/W			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	74			

Note 1:  $R_{\theta,A}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote\_Thermal\_Performance\_of\_eGaN\_FETs.pdf for details.

	Static Characteristics ( $T_j = 25^{\circ}$ C unless otherwise stated)						
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
BV <sub>DSS</sub>	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V, I}_{D} = 0.2 \text{ mA}$	100			V	
I <sub>DSS</sub>	Drain-Source Leakage	$V_{DS} = 80 \text{ V}, \ V_{GS} = 0 \text{ V}, T_{J}$ = 25°C		0.02	0.15	mA	
	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V, T}_{J} = 25^{\circ}\text{C}$		0.01	1.8	mA	
I <sub>GSS</sub>		$V_{GS} = 5 \text{ V}, T_J = 125^{\circ}\text{C}$		0.2	4	mA	
	Gate-to-Source Reverse Leakage#	$V_{GS} = -4 \text{ V}, T_J = 25^{\circ}\text{C}$		0.01	0.18	mA	
V <sub>GS(TH)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 3 \text{ mA}$	0.8	1.4	2.5	V	
R <sub>DS(on)</sub>	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}, I_D = 11 \text{ A}$		10	13.5	mΩ	
V <sub>SD</sub>	Source-Drain Forward Voltage#	$I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}$		2.0		V	

<sup>#</sup> Defined by design. Not subject to production test.



Die Size: 1.5 x 1.5 mm

**EPC2052** eGaN® FETs are supplied in passivated die form with solder bumps.

### **Applications**

- 48 V Servers
- · Lidar/Pulsed Power
- · Isolated Power Supplies
- Point of Load Converters
- Class D Audio
- · LED Lighting
- Low Inductance Motor Drive

## **Benefits**

- Higher Switching Frequency Lower switching losses and lower drive power
- Higher Efficiency Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



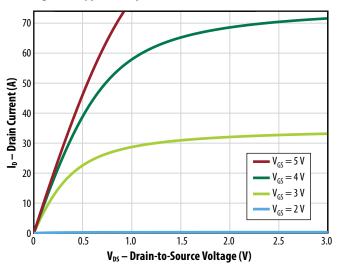
https://l.ead.me/EPC2052

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	Dynamic Characteristics <sup>#</sup> (T <sub>1</sub> = 25°C unless otherwise stated)					
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance			441	584	
$C_{RSS}$	Reverse Transfer Capacitance	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0 \text{ V}$		3.2		
Coss	Output Capacitance			195	293	pF
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 2)	V 0+- F0VVV 0V		227		
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 3)	$V_{DS} = 0 \text{ to } 50 \text{ V}, V_{GS} = 0 \text{ V}$		274		
$R_{G}$	Gate Resistance			0.7		Ω
Q <sub>G</sub>	Total Gate Charge	$V_{DS} = 50 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 11 \text{ A}$		3.5	4.5	
Q <sub>GS</sub>	Gate to Source Charge			1.5		
$Q_{GD}$	Gate to Drain Charge	$V_{DS} = 50 \text{ V}, I_D = 11 \text{ A}$		0.5		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			1.0		nC
Qoss	Output Charge	$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}$		13	20	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

<sup>#</sup> Defined by design. Not subject to production test.

Figure 1: Typical Output Characteristics at 25°C



**Figure 2: Typical Transfer Characteristics** 

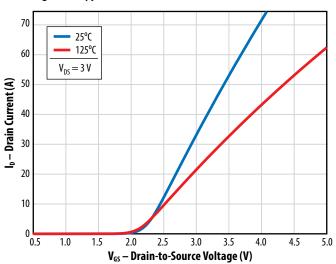


Figure 3: Typical  $\mathbf{R}_{\mathrm{DS(on)}}$  vs.  $\mathbf{V}_{\mathrm{GS}}$  for Various Currents

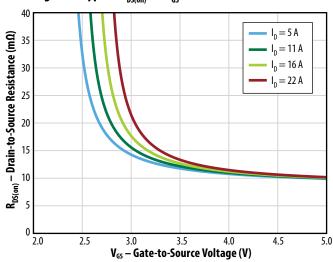
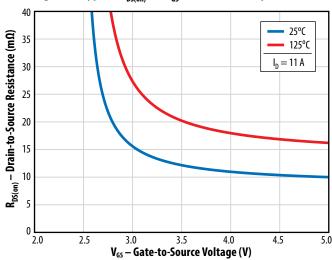


Figure 4: Typical  $\mathbf{R}_{\mathrm{DS(on)}}$  vs.  $\mathbf{V}_{\mathrm{GS}}$  for Various Temperatures

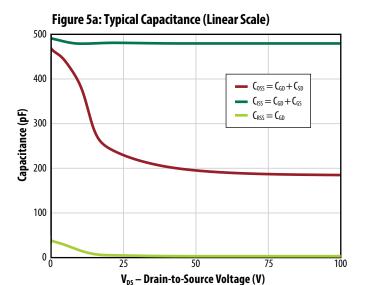


All measurements were done with substrate connected to source.

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50% BV<sub>DSS</sub>.

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50% BV<sub>DSS</sub>.

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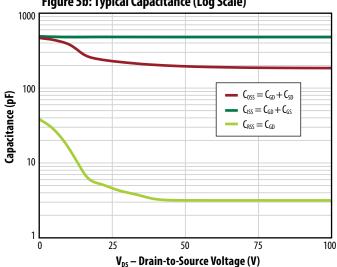


Figure 6: Typical Output Charge and Coss Stored Energy

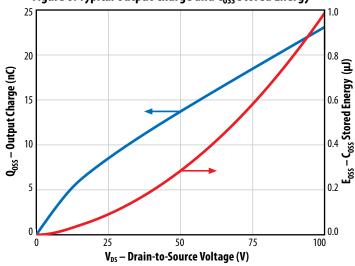
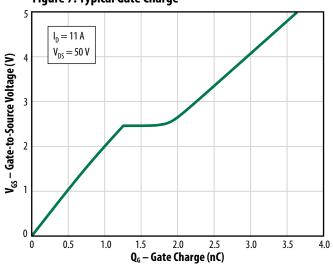


Figure 7: Typical Gate Charge



**Figure 8: Typical Reverse Drain-Source Characteristics** 

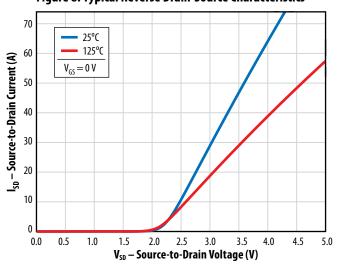
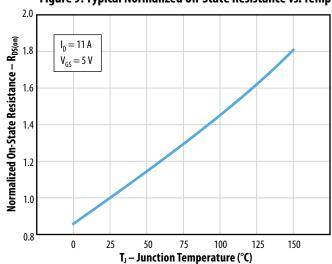
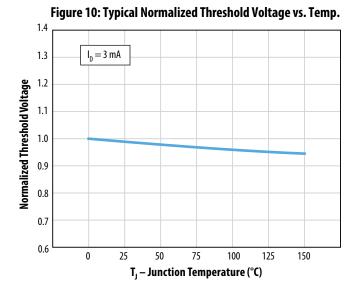


Figure 9: Typical Normalized On-State Resistance vs. Temp.

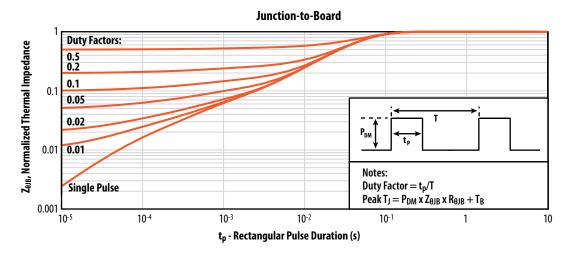


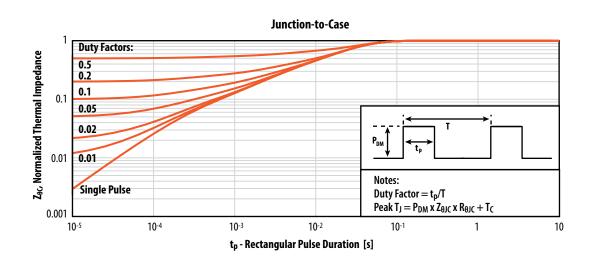
Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF

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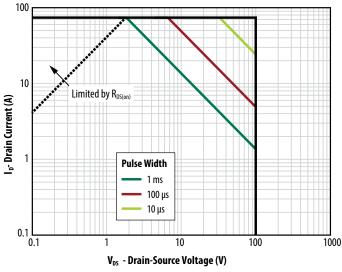
**Figure 11: Typical Transient Thermal Response Curves** 





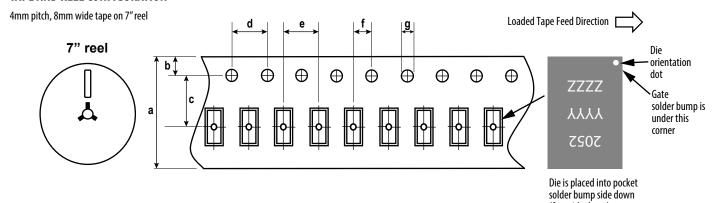
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Figure 12: Safe Operating Area



 $T_J = Max Rated$ ,  $T_C = +25$ °C, Single Pulse

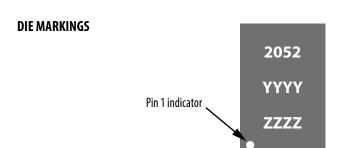
## TAPE AND REEL CONFIGURATION



	EPC2052 (note 1)		
Dimension (mm)	target	min	max
а	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
е	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard. Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

(face side down)

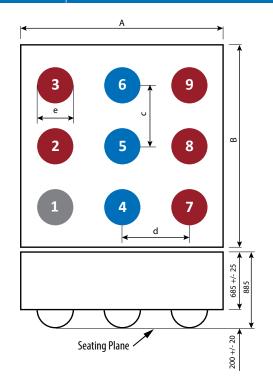


Part		Laser Markings			
Number	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3		
EPC2052	2052	YYYY	ZZZZ		

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### **DIE OUTLINE**

**Solder Bump View** 



DIM	MICROMETERS				
DIM	MIN	Nominal	MAX		
A	1470	1500	1530		
В	1470	1500	1530		
C		450			
d		500			
е	238	264	290		

Pad 1 is Gate;

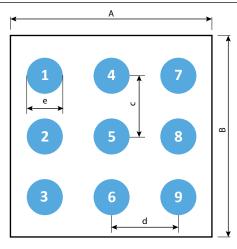
Pads 2, 3, 7, 8, 9 are Source;

Pads 4, 5, 6 are Drain.

# **RECOMMENDED LAND PATTERN**

Side View

(units in  $\mu$ m)



DIM	MICROMETERS
A	1500
В	1500
C	450
d	500
e	230

Pad 1 is Gate;

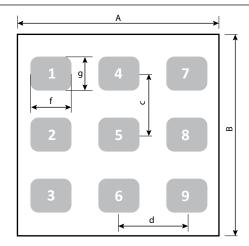
Pads 2, 3, 7, 8, 9 are Source;

Pads 4, 5, 6 are Drain.

# **RECOMMENDED** STENCIL DRAWING

(measurements in µm)

Additional assembly resources available at https://epc-co.com/epc/design-support



DIM	MICROMETERS
A	1500
В	1500
c	450
d	500
f	300
q	250

Pad 1 is Gate;

Pads 2, 3, 7, 8, 9 are Source;

Pads 4, 5, 6 are Drain.

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, opening per drawing. The corner has a radius of R60. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

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