MOSFET - Power, Single P-Channel, WDFN6 -30 V

Product Preview

NTLJS17D0P03P8Z

ON Semiconductor®

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Features

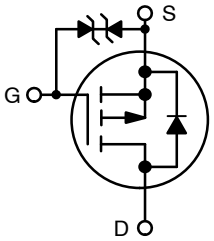
- Small Footprint (4 mm^2) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS Compliant

Applications

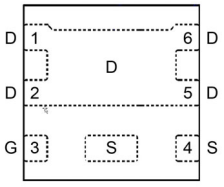
- Battery Management
- Protection
- Power Load Switch

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−30 V	11.3 mΩ @ −10 V	−11.7 A
	21.3 mΩ @ −4.5 V	

ELECTRICAL CONNECTION



P−CHANNEL MOSFET



(Top View)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±25	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	−11.7	A
		T_A = 85°C		−8.4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.40	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	−7.0	A
		T_A = 85°C		−5.1	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	0.86	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	47	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

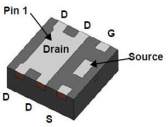
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	52	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	145	

1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz. Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



WDFN6 (2.05x2.05)
CASE 483AV

MARKING DIAGRAM

YW = Date Code
ZZ = Assembly Lot Code
A = Assembly Site Code
17D = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			12.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25°C			−1	μA
			T_J = 125°C			−10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V				±10	μA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.0		−3.0	V
Threshold Temperature Coefficient	V_{GS}/T_J	I_D = −250 μA, ref to 25°C			−5.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −10 A			8.6	11.3	mΩ
		V_{GS} = −4.5 V, I_D = −10 A			14.3	21.3	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −10 A			34		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −15 V, f = 1.0 MHz			1600		pF
Output Capacitance	C_{oss}				550		
Reverse Transfer Capacitance	C_{rss}				530		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −10 A			23		nC
Threshold Gate Charge	$Q_{G(TH)}$				3.0		nC
Gate−to−Source Charge	Q_{GS}				4.6		
Gate−to−Drain Charge	Q_{GD}				14.2		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −10 A			38		nC
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω			18		ns
Rise Time	t_r				106		
Turn−Off Delay Time	$t_{d(off)}$				40		
Fall Time	t_f				72		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω			9		ns
Rise Time	t_r				18		
Turn−Off Delay Time	$t_{d(off)}$				85		
Fall Time	t_f				70		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −10 A	T_J = 25°C		0.83	1.3	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = −100 A/μs, I_S = −10 A			32		ns
Reverse Recovery Charge	Q_{RR}				10		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

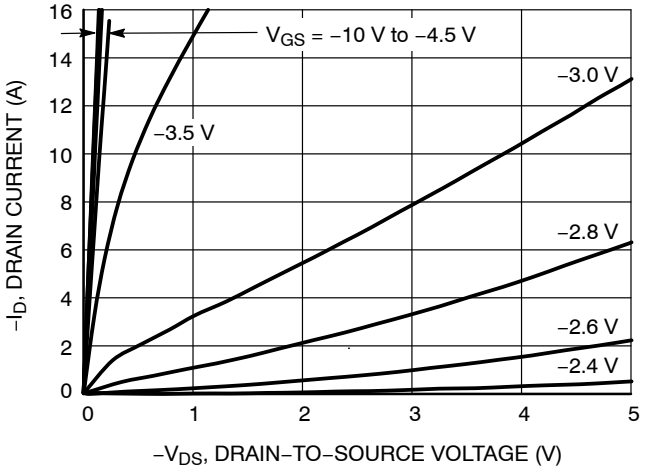


Figure 1. On−Region Characteristics

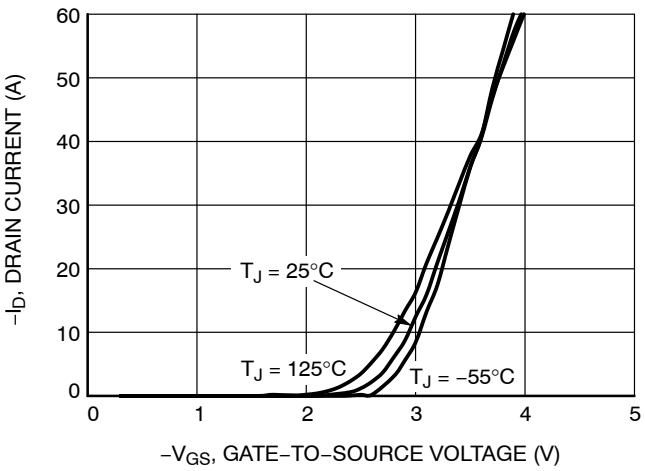


Figure 2. Transfer Characteristics

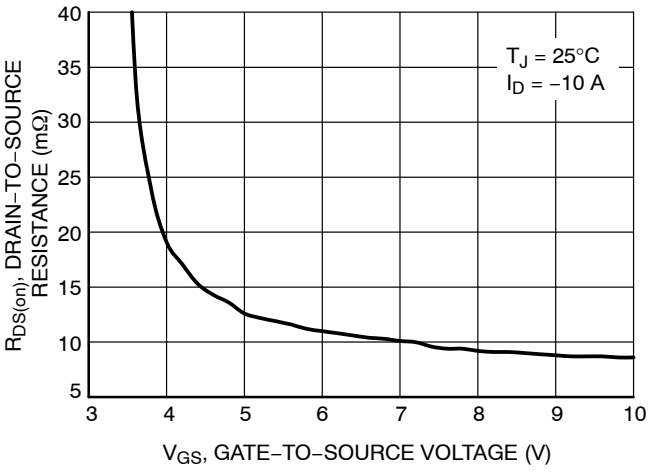


Figure 3. On−Resistance vs. Gate−to−Source Voltage (V)

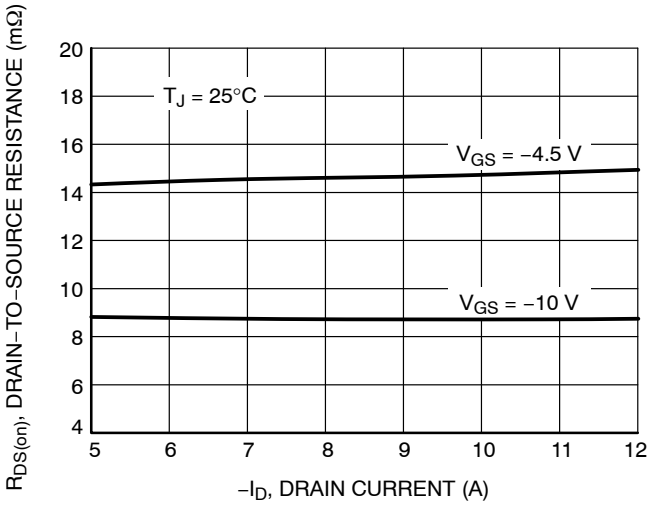


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

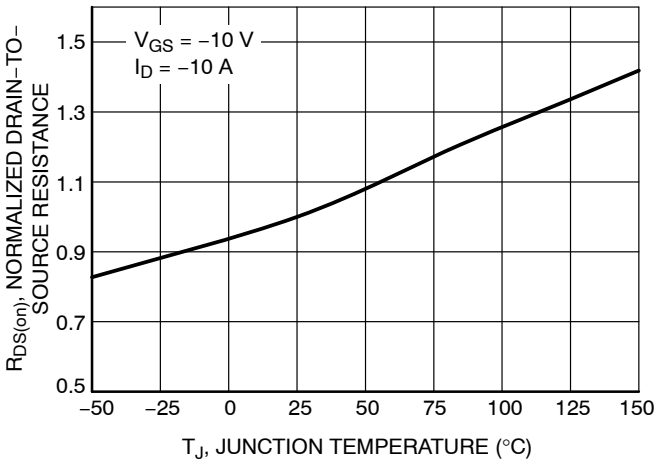


Figure 5. On−Resistance Variation with Temperature

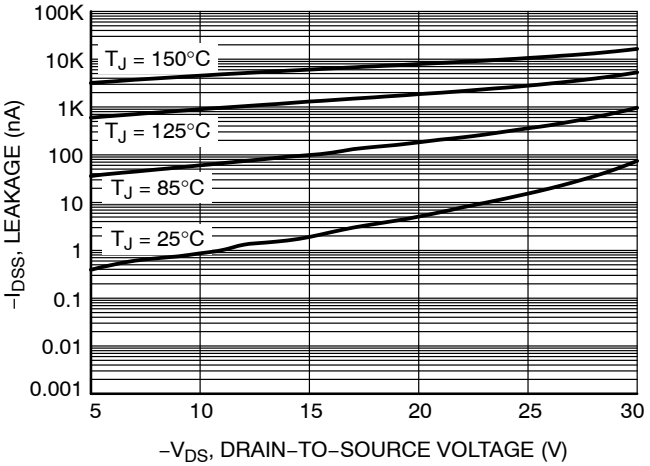


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

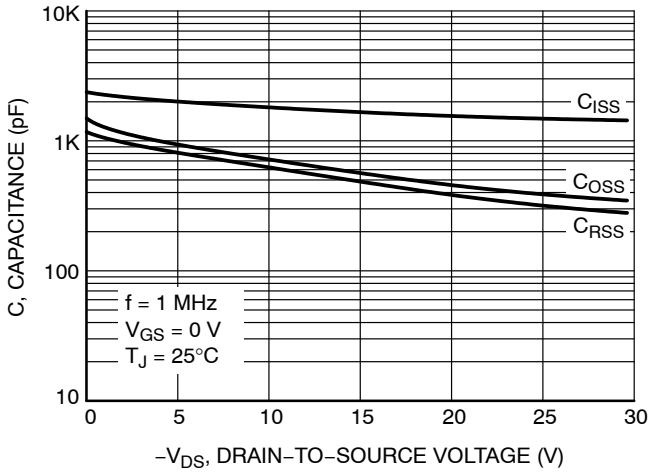


Figure 7. Capacitance Variation

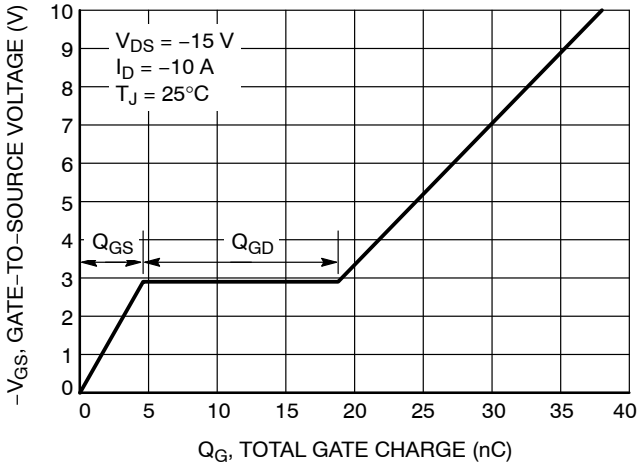


Figure 8. Gate–to–Source vs. Total Charge

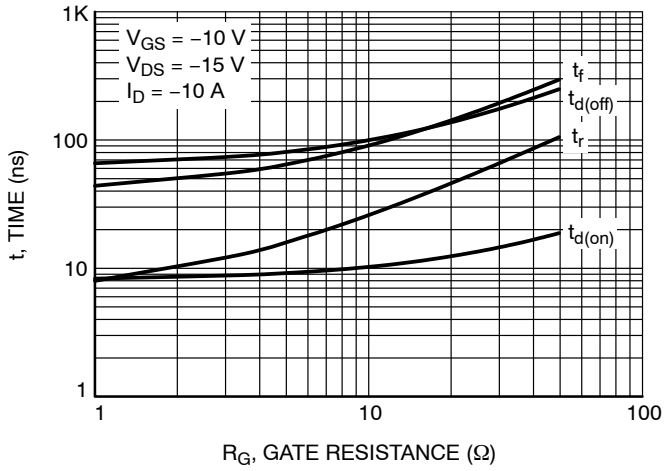


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

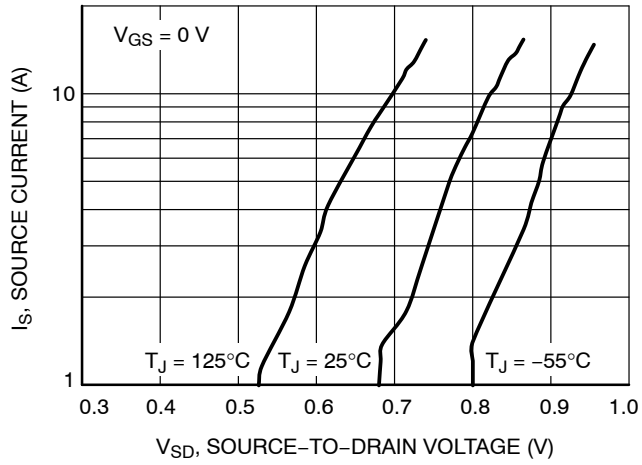
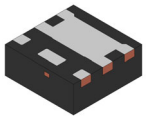


Figure 10. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

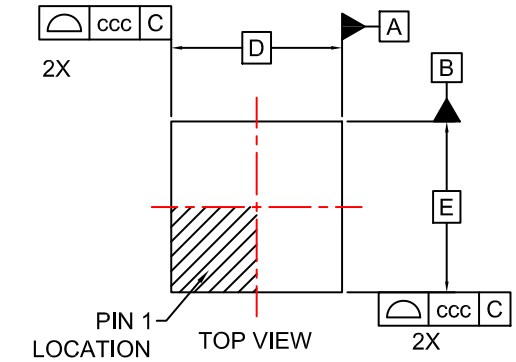
Device	Package	Shipping†
NTLJS17D0P03P8ZTAG	WDFN6 (Pb–Free)	3000 / Tape & Reel

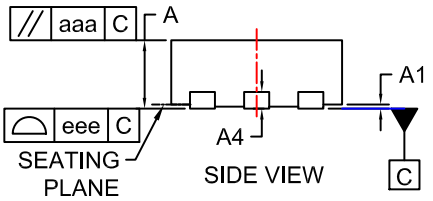
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

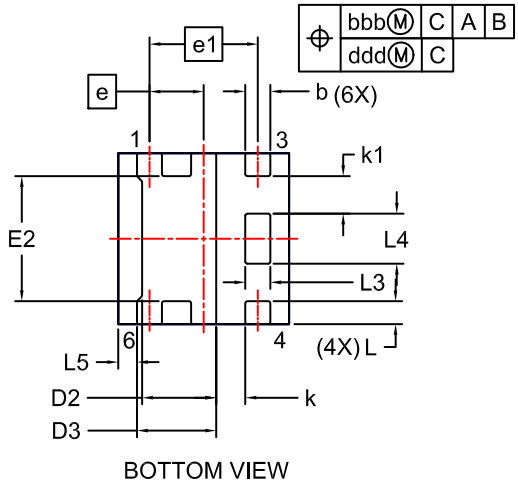


WDFN6 2.05X2.05, 0.65P
CASE 483AV
ISSUE A

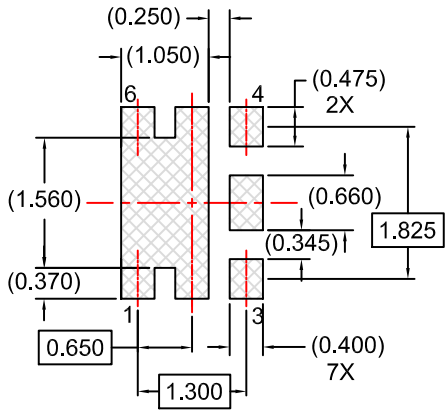
DATE 02 APR 2019







LAND PATTERN
RECOMMENDATION



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4		(0.20)	
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3		(0.95)	
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e		0.65 BSC	
e1		1.30 BSC	
k		(0.35)	
k1		(0.45)	
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5		(0.23)	
aaa		0.10	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.05	

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