

OptiMOS[™]-5 Power Transistor





Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel Enhancement mode Logic Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

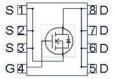
Product Summary

V_{DS}	80	٧
$R_{\mathrm{DS(on),max}}$	14	mΩ
I_{D}	40	Α

PG-TDSON-8-33



Туре	Package	Marking
IAUC40N08S5L140	PG-TDSON-8-33	5N08L140



Maximum ratings, at T_j =25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I _D	$T_{\rm C}$ =25 °C, $V_{\rm GS}$ =10 V, DC ^{1,2)}	40	А
		T _C =100 °C, V _{GS} =10 V, DC ^{1,2)}	28	
Pulsed drain current ²⁾	I _{D,pulse}	T _C =25 °C	160	
Avalanche energy, single pulse ²⁾	E _{AS}	I _D =18 A	32	mJ
Avalanche current, single pulse	IAS	-	18	А
Gate source voltage	V _{GS}	-	±20	V
Power dissipation	P _{tot}	T _C =25 °C	56	w
Operating and storage temperature	$T_{\rm j},T_{\rm stg}$	-	-55 + 175	°C



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics ²⁾						
Thermal resistance, junction - case	R _{thJC}	-	-	-	2.7	K/W
Thermal resistance, junction - ambient ⁴⁾	R _{thJA}	-	-	28.5	-	
Electrical characteristics, at T_j =25	°C, unless	otherwise specified	1	•	•	•
Static characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =1mA	80	-	-	V
Gate threshold voltage	V _{GS(th)}	$V_{\rm DS}=V_{\rm GS}, I_{\rm D}=15~\mu{\rm A}$	1.2	1.6	2.0	
Zero gate voltage drain current	I _{DSS}	V _{DS} =80V, V _{GS} =0V, T _j =25°C	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V, T _j =85°C ²⁾	-	-	20	
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V	-	-	100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =20A	-	16.5	20	mΩ
		V _{GS} =10V, I _D =20A	-	12.5	14	
Gate resistance ²⁾	R _G	-	-	1.2	-	Ω



Parameter	Symbol Conditions	Values			Unit	
			min.	typ.	max.	
Dynamic characteristics ²⁾						
Input capacitance	C iss	V _{GS} =0V, V _{DS} =40V, f=1MHz	-	829	1078	pF
Output capacitance	C oss		-	146	190	
Reverse transfer capacitance	C _{rss}		-	11	17	
Turn-on delay time	t _{d(on)}	$V_{\rm DD}$ =40V, $V_{\rm GS}$ =10V, $I_{\rm D}$ =20A, $R_{\rm G,ext}$ =3.5 Ω	-	2	-	ns
Turn-off delay time	t _{d(off)}		-	9	-	
Rise time	t _r		-	1	-	
Fall time	t _f		-	4	-	
Gate Charge Characteristics ²⁾ Gate to source charge	Q _{gs}	V _{DD} =40V, I _D =20A, V _{GS} =0 to 10V	-	2.7	3.5	nC
Gate to drain charge	Q _{gd}		-	3.2	4.8	
Gate charge total	Qg		-	14.3	18.6	
Gate plateau voltage	V _{plateau}		-	3.2	-	V
Reverse Diode						
Diode continous forward current ²⁾	Is	T _C =25°C	-	-	40	А
Diode pulse current ²⁾	I _{S,pulse}	T _C =25 °C	-	-	160	
Diode forward voltage	V _{SD}	V _{GS} =0V, I _F =20 A, T _j =25°C	-	0.9	1.2	V
Reverse recovery time ²⁾	t _{rr}	V _R =40V, I _F =40A,	-	31	-	ns
	1	d <i>i</i> _F /d <i>t</i> =100A/μs		1		1

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

³⁾ Device on a 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

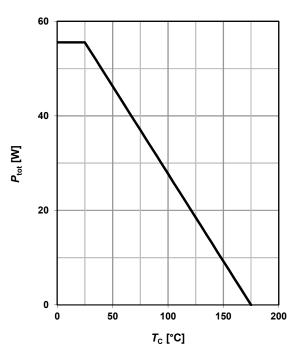


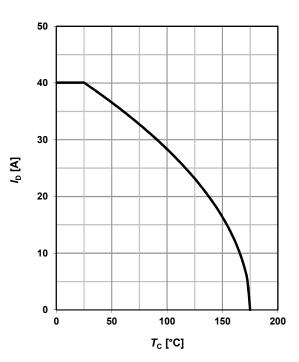
1 Power dissipation

$$P_{\text{tot}} = f(T_{\text{C}}); V_{\text{GS}} = 10 \text{ V}$$

2 Drain current

$$I_{\rm D} = f(T_{\rm C}); V_{\rm GS} = 10 \text{ V}$$





3 Safe operating area

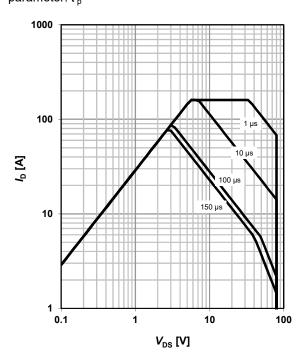
$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

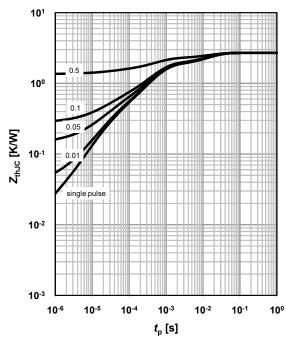
parameter: t_{p}

4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

parameter: $D = t_p/T$







5 Typ. output characteristics

 $I_D = f(V_{DS}); T_i = 25 °C$

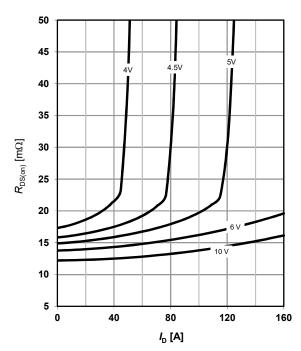
parameter: V_{GS}

120 120 40 40 40 120 40 40 V_{DS} [V]

6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25 °C$

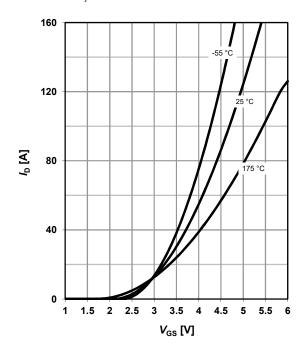
parameter: $V_{\rm GS}$



7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6V$

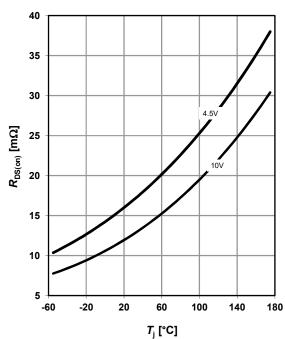
parameter: T_i



8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 20A$

parameter: V_{GS}





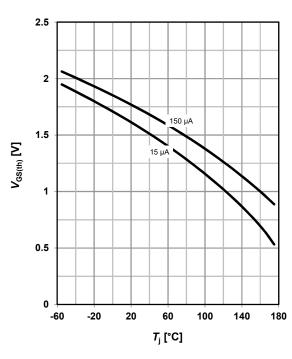
9 Typ. gate threshold voltage

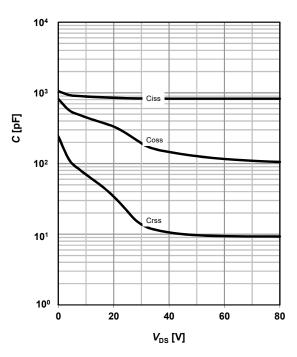
 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D

10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$





11 Typical forward diode characteristics

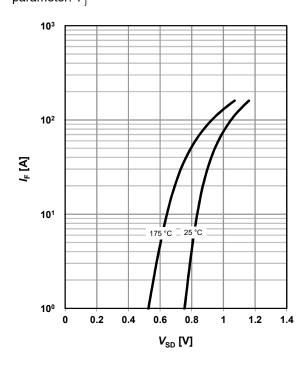
 $I_F = f(V_{SD})$

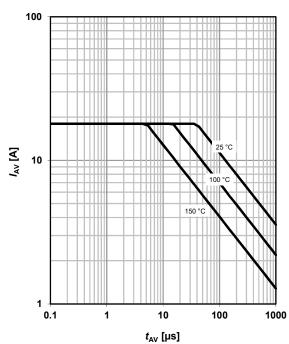
parameter: T_i

12 Avalanche characteristics

 $I_{AS} = f(t_{AV})$

parameter: T_{j(start)}







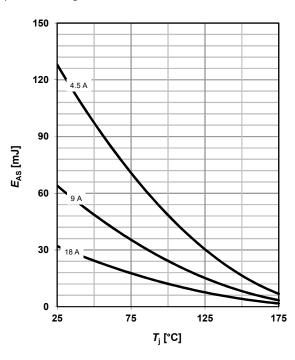
13 Avalanche energy

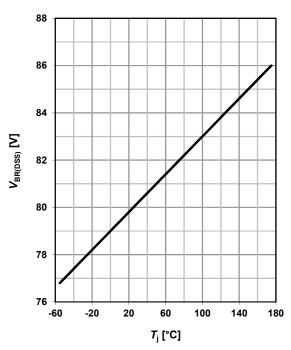
$E_{AS} = f(T_i)$

parameter: I_D

14 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

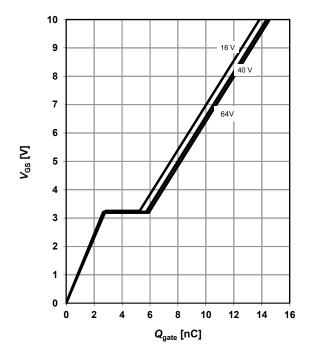




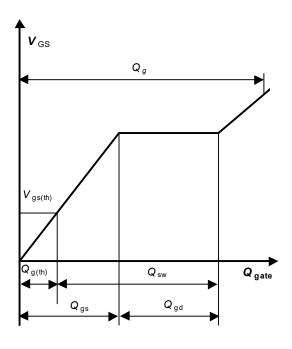
15 Typ. gate charge

 V_{GS} = f(Q_{gate}); I_D = 20 A pulsed

parameter: $V_{\rm DD}$

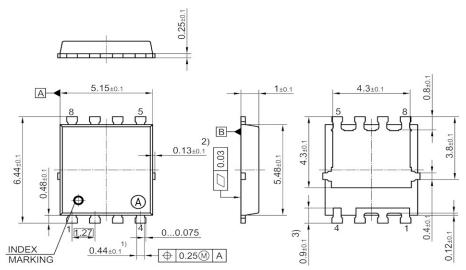


16 Gate charge waveforms



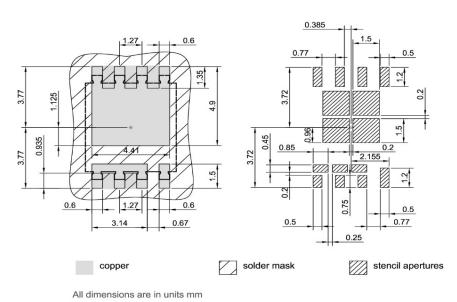


Package Outline

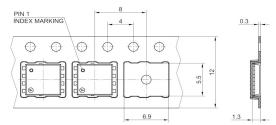


- 1) EXCLUDE MOLD FLASH
 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 3) LEAD LENGTH UP TO ANTI FLASH LINE
 4)ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
 ALL DIMENSIONS ARE IN UNITS MM
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [

Footprint



Packaging





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Revision History

Version	Date	Changes		
Revision 1.0	2021-01-19	Final Data Sheet		