

### **Description**

The DMN3069L-7 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

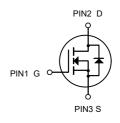
# D S G

# **SOT-23**

## **General Features**

 $V_{DS} = 30V I_{D} = 5.8A$ 

 $R_{DS(ON)}$  < 28m $\Omega$  @  $V_{GS}$ =10V



# **Application**

Battery protection

Load switch

Uninterruptible power supply

#### N-Channel MOSFET

# **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
DMN3069L-7	SOT-23	HXY MOSFET	3000

# Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwisenoted)

Symbol	Parameter	Limit	Unit
VDS	Drain-Source Voltage	30	V
Vgs	Gate-Source Voltage	±20	V
lο	Drain Current-Continuous	5.8	А
Ідм	Drain Current-Pulsed (Note 1)	18.4	Α
P <sub>D</sub>	Maximum Power Dissipation	1	W
Т,,Тѕтс	Operating Junction and Storage Temperature Range	-55 To 150	°C
Reja	Thermal Resistance,Junction-to-Ambient (Note 2)	125	°C/W

# Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30			V	
$\triangle BV_{DSS}/\triangle T$	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.023		V/°C	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =4A		22	28	mΩ	
	Static Drain-Source On-Nesistance	V <sub>GS</sub> =4.5V , I <sub>D</sub> =3A	s=4.5V , I <sub>D</sub> =3A 26		32	1115.2	
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.5	2.5	V	
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	VGS-VDS , ID -230UA		-4.2		mV/°C	
lana	Drain-Source Leakage Current	$V_{DS}$ =24V , $V_{GS}$ =0V , $T_J$ =25 $^{\circ}$ C			1	uA	
I <sub>DSS</sub>		V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5		
Igss	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =4A		7		S	
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.3	4.6	Ω	
Qg	Total Gate Charge (4.5V)			5.0	6.9		
Qgs	Gate-Source Charge	V <sub>DS</sub> =15V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =4A		1.1	2.2	nC	
Q <sub>gd</sub>	Gate-Drain Charge			2.6	2.8		
T <sub>d(on)</sub>	Turn-On Delay Time			2	4		
Tr	Rise Time	$V_{DD}$ =15V , $V_{GS}$ =10V , $R_{G}$ =3.3 $\Omega$		34.4	62	ns	
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =4A		13.2	26		
Tf	Fall Time			4.8	9.6		
Ciss	Input Capacitance			420	582		
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		60	87	pF	
Crss	Reverse Transfer Capacitance			53	71		
ls	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			5.8	Α	
Ism	Pulsed Source Current <sup>2,4</sup>	vg-vb-ov , Force Current			18.4	Α	
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V	
t <sub>rr</sub>	Reverse Recovery Time		1	8.7		nS	
$Q_{rr}$	Reverse Recovery Charge	I <sub>F</sub> =4A , dI/dt=100A/μs , T <sub>J</sub> =25°C		2.3		nC	

#### Note:

<sup>1.</sup> The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

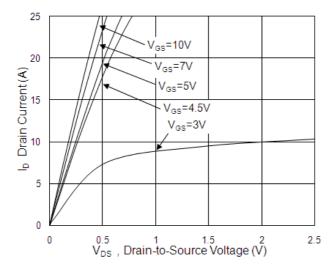
<sup>2.</sup>The data tested by pulsed , pulse width  $\leq 300 \text{us}$  , duty cycle  $\leq 2\%$ 

<sup>3.</sup> The power dissipation is limited by 150°C junction temperature

<sup>4.</sup> The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



# **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

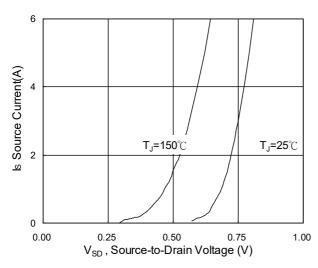


Fig.3 Forward Characteristics Of Reverse

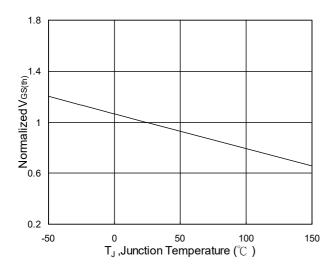


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

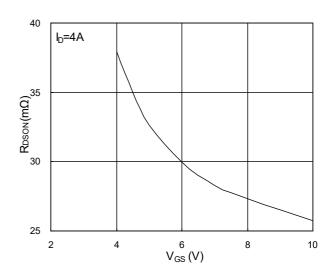


Fig.2 On-Resistance vs. Gate-Source

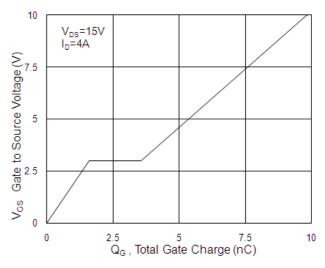


Fig.4 Gate-Charge Characteristics

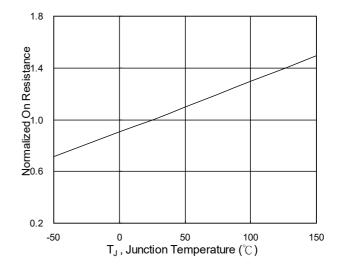
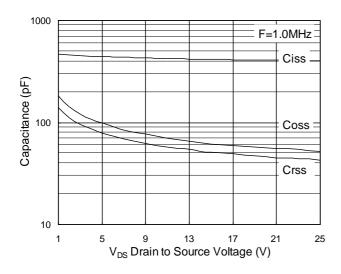


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>





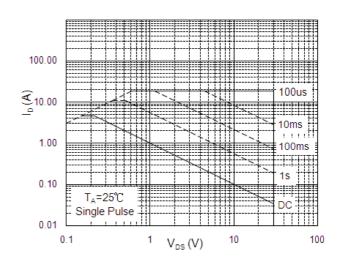


Fig.7 Capacitance

Fig.8 Safe Operating Area

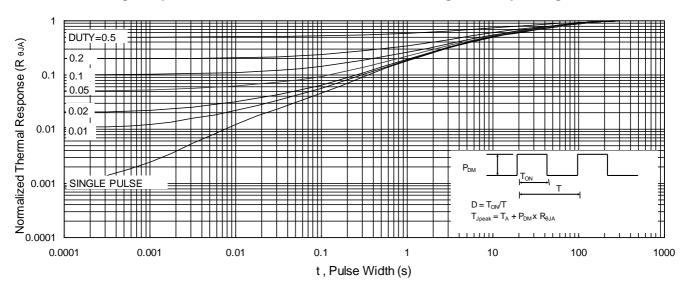


Fig.9 Normalized Maximum Transient Thermal Impedance

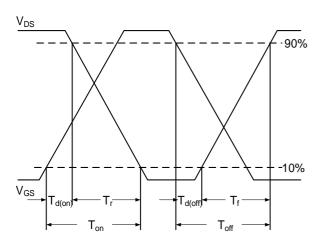


Fig.10 Switching Time Waveform

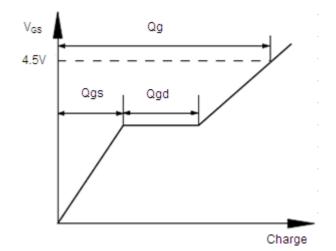
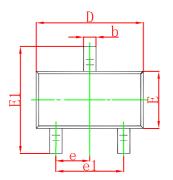
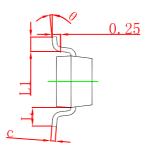


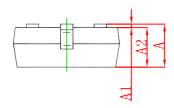
Fig.11 Gate Charge Waveform



# **SOT-23 Package Outline Dimensions**

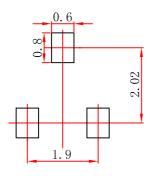






Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
Е	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF		0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

# **SOT-23 Suggested Pad Layout**



- Note:
  1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.



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