			Implementation		
mnemonic	Name	PVECLIB	P7	P8	P9
bcdadd	Decimal Add Modulo	Vec_bcdadd	1	1	1
bcdsub	Decimal Subtract Modulo	vec_bcdsub	1	1	1
mfvsrd	Move From VSR Doubleword				
mfvsrwz	Move From VSR Word and Zero				
mtvsrd	Move To VSR Doubleword				
mtvsrwa	Move To VSR Word Algebraic				
mtvsrwz	Move To VSR Word and Zero				
vaddcuq	Vector Add & write Carry Unsigned Quadword	Vec_addcuq	1	1	1
vaddecuq	Vector Add Extended & write Carry Unsigned Quadword	vec_addecuq	1	1	1
vaddeuqm	Vector Add Extended Unsigned Quadword Modulo	vec_addeuqm	1	1	1
vaddudm	Vector Add Unsigned Doubleword Modulo	vec_addudm	1	1	1
vadduqm	Vector Add Unsigned Quadword Modulo	vec_adduqm	1	1	1
vbpermq	Vector Bit Permute Quadword				
vcipher	Vector AES Cipher				
vcipherlast	Vector AES Cipher Last				
vclzb	Vector Count Leading Zeros Byte	vec_clzb	1	1	1
vclzd	Vector Count Leading Zeros Doubleword	vec_clzd	1	1	1
vclzh	Vector Count Leading Zeros Halfword	vec_clzh	1	1	1
vclzw	Vector Count Leading Zeros Word	vec_clzw	1	1	1
vcmpequd	Vector Compare Equal To Unsigned Doubleword	vec_cmpequd	1	1	1
vcmpgtsd	Vector Compare Greater Than Signed Doubleword	vec_cmpgtsd	1	1	1
vcmpgtud	Vector Compare Greater Than Unsigned Doubleword	vec_cmpgtud	1	1	1
veqv	Vector Equivalence				
vgbbd	Vector Gather Bits by Byte by Doubleword				
vmaxsd	Vector Maximum Signed Doubleword	vec_maxsd	1	1	1
vmaxud	Vector Maximum Unsigned Doubleword	vec_maxud	1	1	1
vminsd	Vector Minimum Signed Doubleword	vec_minsd	1	1	1
vminud	Vector Minimum Unsigned Doubleword	vec_minud	1	1	1
vmrgew	Vector Merge Even Word	Vec_mrgew	1	1	1
vmrgow	Vector Merge Odd Word	vec_mrgow	1	1	1
vmulesw	Vector Multiply Even Signed Word	vec_mulesw	1	1	1
vmuleuw	Vector Multiply Even Unsigned Word	vec_muleuw	1	1	1
vmulosw	Vector Multiply Odd Signed Word	vec_mulosw	1	1	1
vmulouw	Vector Multiply Odd Unsigned Word	vec_mulouw	1	1	1
vmuluwm	Vector Multiply Unsigned Word Modulo	vec_muluwm	1	1	1
vnand	Vector NAND				
vncipher	Vector AES Inverse Cipher				
vncipherlast	Vector AES Inverse Cipher Last				
vorc	Vector OR with Complement				

vpermxor	Vector Permute and Exclusive-OR				
vpksdss	Vector Pack Signed Doubleword Signed Saturate				
vpksdus	Vector Pack Signed Doubleword Unsigned Saturate				
vpkudum	Vector Pack Unsigned Doubleword Unsigned Modulo				
vpkudus	Vector Pack Unsigned Doubleword Unsigned Saturate				
vpmsumb	Vector Polynomial Multiply-Sum Byte				
vpmsumd	Vector Polynomial Multiply-Sum Doubleword				
vpmsumh	Vector Polynomial Multiply-Sum Halfword				
vpmsumw	Vector Polynomial Multiply-Sum Word				
vpopcntb	Vector Population Count Byte	vec_popcntb	1	1	1
vpopcntd	Vector Population Count Doubleword	vec_popcntd	1	1	1
vpopcnth	Vector Population Count Halfword	vec_popcnth	1	1	1
vpopcntw	Vector Population Count Word	vec_popcntw	1	1	1
vrld	Vector Rotate Left Doubleword	vec_vrld	1	1	1
vsbox	Vector AES S-Box				
vshasigmad	Vector SHA-512 Sigma Doubleword				
vshasigmaw	Vector SHA-256 Sigma Word				
vsld	Vector Shift Left Doubleword	vec_vsld	1	1	1
vsrad	Vector Shift Right Algebraic Doubleword	vec_vsrad	1	1	1
vsrd	Vector Shift Right Doubleword	vec_vsrd	1	1	1
vsubcuq	Vector Subtract & write Carry Unsigned Quadword	vec_subcuq	1	1	1
vsubecuq	Vector Subtract Extended & write Carry Unsigned Quadword	vec_subecuq	1	1	1
vsubeuqm	Vector Subtract Extended Unsigned Quadword Modulo	vec_subeuqm	1	1	1
vsubudm	Vector Subtract Unsigned Doubleword Modulo	vec_subudm	1	1	1
vsubuqm	Vector Subtract Unsigned Quadword Modulo	vec_subuqm	1	1	1
vupkhsw	Vector Unpack High Signed Word				
vupklsw	Vector Unpack Low Signed Word				
xxleqv	VSX Logical Equivalence				
xxlnand	VSX Logical NAND				
xxlorc	VSX Logical OR with Complement				

Link
vec_bcdaddcsq ...
vec_bcdsubscq ...
vec_cmpud_all_eq
vec_cmpgesdvec_cmpltsd
vec_cmpgeudvec_cmpltud
vec_mulhsw
vec_mulhsw
vec_mulhuw
vec_mulhuw

vec_rldi

vec_sldi
vec_sradi
vec_srdi

mnemonic	Name	PVECLIB	Implement P8	P9
bcdcfn.	Decimal Convert From National & record			
bcdcfsq.	Decimal Convert From Signed Quadword & record	vec_bcdcfsq	1	1
bcdcfz.	Decimal Convert From Zoned & record	vec_bcdcxfz	1	1
bcdcpsgn.	Decimal CopySign & record	vec_bcdcpsgn	1	1
bcdctn.	Decimal Convert To National & record			
bcdctsq.	Decimal Convert To Signed Quadword & record	vec_bcdctsq	1	1
bcdctz.	Decimal Convert To Zoned & record	vec_bcdctz	1	1
bcds.	Decimal Shift & record	vec_bcds	1	1
bcdsetsgn.	Decimal Set Sign & record	vec_bcdsetsgn	1	1
bcdsr.	Decimal Shift & Round & record	vec_bcdsr	1	1
bcdtrunc.	Decimal Truncate & record	vec_bcdtrunc	1	1
bcdus.	Decimal Unsigned Shift & record	vec_bcdus	1	1
bcdutrunc.	Decimal Unsigned Truncate & record	vec_bcdutrunc	1	1
vabsdub	Vector Absolute Difference Unsigned Byte	vec_absdub	1	1
vabsduh	Vector Absolute Difference Unsigned Halfword	vec_absduh	1	1
vabsduw	Vector Absolute Difference Unsigned Word	vec_absduw	1	1
vbpermd	Vector Bit Permute Doubleword			
vcfsx	Vector Convert with round to nearest Signed Word format to FP			
vcfux	Vector Convert with round to nearest Unsigned Word format to FP			
vclzlsbb	Vector Count Leading Zero Least-Significant Bits Byte			
vcmpneb[.]	Vector Compare Not Equal Byte			
vcmpneh[.]	Vector Compare Not Equal Halfword			
vcmpnew[.]	Vector Compare Not Equal Word			
vcmpnezb[.]	Vector Compare Not Equal or Zero Byte			
vcmpnezh[.]	Vector Compare Not Equal or Zero Halfword			
vcmpnezw[.]	Vector Compare Not Equal or Zero Word			
vctsxs	Vector Convert with round to zero FP To Signed Word format saturate			
vctuxs	Vector Convert with round to zero FP To Unsigned Word format saturate			
vctzb	Vector Count Trailing Zeros Byte			
vctzd	Vector Count Trailing Zeros Doubleword			
vctzh	Vector Count Trailing Zeros Halfword			
vctzw	Vector Count Trailing Zeros Word			
vextractd	Vector Extract Doubleword			
vextractub	Vector Extract Unsigned Byte			
vextractuh	Vector Extract Unsigned Halfword			
vextractuw	Vector Extract Unsigned Word			

vextsb2d	Vector Extend Sign Byte to Doubleword			
vextsb2w	Vector Extend Sign Byte to Word			
vextsh2d	Vector Extend Sign Halfword to Doubleword			
vextsh2w	Vector Extend Sign Halfword to Word			
vextsw2d	Vector Extend Sign Word to Doubleword			
vextublx	Vector Extract Unsigned Byte Left-Indexed			
vextubrx	Vector Extract Unsigned Byte Right-Indexed			
vextuhlx	Vector Extract Unsigned Halfword Left-Indexed			
vextuhrx	Vector Extract Unsigned Halfword Right-Indexed			
vextuwlx	Vector Extract Unsigned Word Left-Indexed			
vextuwrx	Vector Extract Unsigned Word Right-Indexed			
vinsertb	Vector Insert Byte			
vinsertd	Vector Insert Doubleword			
vinserth	Vector Insert Halfword			
vinsertw	Vector Insert Word			
vmsumudm	Vector Multiply-Sum Unsigned Doubleword Modulo	vec_muludm	1	1
vmul10cuq	Vector Multiply-by-10 & write Carry Unsigned Quadword	vec_mul10cuq	1	1
vmul10ecuq	Vector Multiply-by-10 Extended & write Carry Unsigned Quadword	vec_mul10ecuq	1	1
vmul10euq	Vector Multiply-by-10 Extended Unsigned Quadword	vec_mul10euq	1	1
vmul10uq	Vector Multiply-by-10 Unsigned Quadword	vec_mul10uq	1	1
vnegd	Vector Negate Doubleword			
vnegw	Vector Negate Word			
vpermr	Vector Permute Right-indexed			
vprtybd	Vector Parity Byte Doubleword			
vprtybq	Vector Parity Byte Quadword			
vprtybw	Vector Parity Byte Word			
vrldmi	Vector Rotate Left Doubleword then Mask Insert			
vrldnm	Vector Rotate Left Doubleword then AND with Mask			
vrlwmi	Vector Rotate Left Word then Mask Insert			
vrlwnm	Vector Rotate Left Word then AND with Mask			
vslv	Vector Shift Left Variable			
vsrv	Vector Shift Right Variable			
xvcvhpsp	VSX Vector Convert Half-Precision to Single-Precision format			
xvcvsphp	VSX Vector Convert with round Single-Precision to Half-Precision format			
xviexpdp	VSX Vector Insert Exponent Double-Precision			
xviexpsp	VSX Vector Insert Exponent Single-Precision			
xvtstdcdp	VSX Vector Test Data Class Double-Precision		1	1
xvtstdcsp	VSX Vector Test Data Class Single-Precision		1	1
xvxexpdp	VSX Vector Extract Exponent Double-Precision			
xvxexpsp	VSX Vector Extract Exponent Single-Precision			
xvxsigdp	VSX Vector Extract Significand Double-Precision			
xvxsigsp	VSX Vector Extract Significand Single-Precision			
xxbrd	VSX Vector Byte-Reverse Doubleword	vec_revbd	1	1
xxbrh	VSX Vector Byte-Reverse Halfword	vec_revbh	1	1
xxbrq	VSX Vector Byte-Reverse Quadword	vec_revbq	1	1
xxbrw	VSX Vector Byte-Reverse Word	vec_revbw	1	1
xxextractuw	VSX Vector Extract Unsigned Word			

xxinsertw	VSX Vector Insert Word
xxperm	VSX Vector Permute
xxpermr	VSX Vector Permute Right-indexed
xxspltib	VSX Vector Splat Immediate Byte

tation
P10 Link

vec_is*f64
vec_is*f32

mnemonic	Name	PVECLIB	Implemer P8	P9
vcmpgtuq[	Vector Compare Greater Than Unsigned Quadword	vec_cmpgtuq	1	1
vcmpsq	Vector Compare Signed Quadword	vec_cmpsq_all	1	1
vcmpuq	Vector Compare Unsigned Quadword	vec_cmpuq_all	1	1
vcntmbb	Vector Count Mask Bits Byte			
vcntmbd	Vector Count Mask Bits Doubleword			
vcntmbh	Vector Count Mask Bits Halfword			
vcntmbw	Vector Count Mask Bits Word			
vctzdm	Vector Count Trailing Zeros Doubleword under bit Mask			
vdivesd	Vector Divide Extended Signed Doubleword			
vdivesq	Vector Divide Extended Signed Quadword			
vdivesw	Vector Divide Extended Signed Word			
vdiveud	Vector Divide Extended Unsigned Doubleword			
vdiveuq	Vector Divide Extended Unsigned Quadword			
vdiveuw	Vector Divide Unsigned Word			
vexpandbm	Vector Expand Byte Mask			
vexpanddm	Vector Expand Doubleword Mask			
vexpandhm	Vector Expand Halfword Mask			
vexpandqm	Vector Expand Quadword Mask	vec_setb_sq	1	1
vexpandwm	Vector Expand Word Mask			
vextddvlx	Vector Extract Double Doubleword to VSR using GPR Left Index			
vextddvrx	Vector Extract Double Doubleword to VSR using GPR Right Index			
vextdubvlx	Vector Extract Double Unsigned Byte to VSR using GPR Left Index			
vextdubvrx	Vector Extract Double Unsigned Byte to VSR using GPR Right Index			
vextduhvlx	Vector Extract Double Unsigned Halfword to VSR using GPR Left Index			
vextduhvrx	Vector Extract Double Unsigned Halfword to VSR using GPR Right Index			
vextduwvlx	Vector Extract Double Unsigned Word to VSR using GPR Left Index			
vextduwvrx	Vector Extract Double Unsigned Word to VSR using GPR Right Index			
vextractbm	Vector Extract Byte Mask (to GPR)			
vextractdm	Vector Extract Doubleword Mask			
vextracthm	Vector Extract Halfword Mask			
vextractqm	Vector Extract Quadword Mask			
vextractwm	Vector Extract Word Mask			
vextsd2q	Vector Extend Sign Doubleword to Quadword			
vgnb	Vector Gather every Nth Bit (to GPR)			
vinsblx	Vector Insert Byte from GPR using GPR-specified Left-Index			
vinsbrx	Vector Insert Byte from GPR using GPR-specified Right-Index			

vinsbvlx	Vector Insert Byte from VSR using GPR-specified Left-Index			
vinsbvrx	Vector Insert Byte from VSR using GPR-specified Right-Index			
vinsd	Vector Insert Doubleword from GPR using mmediate-specified index			
vinsdlx	Vector Insert Doubleword from GPR using GPR-specified Left-Index			
vinsdrx	Vector Insert Doubleword from GPR using GPR-specified Right-Index			
vinshlx	Vector Insert Halfword from GPR using GPR-specified Left-Index			
vinshrx	Vector Insert Halfword from GPR using GPR-specified Right-Index			
vinshvlx	Vector Insert Halfword from VSR using GPR-specified Left-Index			
vinshvrx	Vector Insert Halfword from VSR using GPR-specified Right-Index			
vinswlx	Vector Insert Word from GPR using GPR-specified Left-Index			
vinswrx	Vector Insert Word from GPR using GPR-specified Right-Index			
vinswvlx	Vector Insert Word from VSR using GPR-specified Left-Index			
vinswvrx	Vector Insert Word from VSR using GPR-specified Right-Index			
vmodsd	ector Modulo Signed Doubleword			
vmodsq	Vector Modulo Signed Quadword			
vmodsw	Vector Modulo Signed Word			
vmodud	ector Modulo Unsigned Doubleword			
vmoduq	Vector Modulo Unsigned Quadword			
vmoduw	Vector Modulo Unsigned Word			
vmsumcud	Vector Multiply-Sum & write Carry-out Unsigned Doubleword			
vmulesd	Vector Multiply Even Signed Doubleword			
vmuleud	Vector Multiply Even Unsigned Doubleword	Vec_vmuleud	1	1
vmulhsd	Vector Multiply High Signed Doubleword			
vmulhsw	Vector Multiply High Signed Word	vec_mulhsw	1	1
vmulhud	Vector Multiply High Unsigned Doubleword	Vec_mulhud	1	1
vmulhuw	Vector Multiply High Unsigned Word	vec_mulhuw	1	1
vmulld	Vector Multiply Low Doubleword	vec_muludm	1	1
vmulosd	Vector Multiply Odd Signed Doubleword			
vpdepd	Vector Parallel Bits Deposit Doubleword			
vpextd	Vector Parallel Bits Extract Doubleword			
vrlq	Vector Rotate Left Quadword	Vec_rlq	1	1
vrlqmi	Vector Rotate Left Quadword then Mask Insert			
vrlqnm	Vector Rotate Left Quadword then AND with Mask			
vsldbi	Vector Shift Left Double by Bit Immediate	vec_sldqi	1	1
vslq	Vector Shift Left Quadword	vec_slq	1	1
vsraq	Vector Shift Right Algebraic Quadword	Vec_sraq	1	1
vsrdbi	Vector Shift Right Double by Bit Immediate			
vsrq	Vector Shift Right Quadword	vec_srq	1	1
vstribl	Vector String Isolate Byte Left-justified			
vstribr	Vector String Isolate Byte Right-justified			
vstrihl	Vector String Isolate Halfword Left-justified			
vstrihr	Vector String Isolate Halfword Right-justifie			
xscmpeqqp	VSX Scalar Compare Equal Quad-Precision			
xscmpgeqp	VSX Scalar Compare Greater Than or Equal Quad-Precision			
xscmpgtqp	VSX Scalar Compare Greater Than Quad-Precision			
xscvqpsqz	VSX Scalar Convert with round to zero Quad-Precision to Signed Quadword			

xscvqpuqz	VSX Scalar Convert with round to zero Quad-Precision to Unsigned Quadword
xscvsqqp	VSX Scalar Convert with round Signed Quadword to Quad-Precision
xscvuqqp	VSX Scalar Convert with round Unsigned Quadword to Quad-Precision
xsmaxcqp	VSX Scalar Maximum Type-C Quad-Precision
xsmincqp	VSX Scalar Minimum Type-C Quad-Precision
xvbf16ger2	VSX Vector bfloat16 GER (Rank-2 Update)
xvbf16ger2nn	VSX Vector bfloat16 GER (Rank-2 Update) Negative multiply, Negative accumulate
xvbf16ger2np	VSX Vector bfloat16 GER (Rank-2 Update) Negative multiply, Positive accumulate
xvbf16ger2pn	VSX Vector bfloat16 GER (Rank-2 Update) Positive multiply, Negative accumulate
xvbf16ger2pp	VSX Vector bfloat16 GER (Rank-2 Update) Positive multiply, Positive accumulate
xvcvbf16sp	VSX Vector Convert bfloat16 to Single-Precision format
xvcvspbf16	VSX Vector Convert with round Single-Precision to bfloat16 format
xvf16ger2	VSX Vector 16-bit Floating-Point GER (rank-2 update)
xvf16ger2nn	VSX Vector 16-bit Floating-Point GER (rank-2 update) Negative multiply, Negative accumulate
xvf16ger2np	VSX Vector 16-bit Floating-Point GER (rank-2 update) Negative multiply, Positive accumulate
xvf16ger2pn	VSX Vector 16-bit Floating-Point GER (rank-2 update) Positive multiply, Negative accumulate
xvf16ger2pp	VSX Vector 16-bit Floating-Point GER (rank-2 update) Positive multiply, Positive accumulate
xvf32ger	VSX Vector 32-bit Floating-Point GER (rank-1 update)
xvf32gernn	VSX Vector 32-bit Floating-Point GER (rank-1 update) Negative multiply, Negative accumulate
xvf32gernp	VSX Vector 32-bit Floating-Point GER (rank-1 update) Negative multiply, Positive accumulate
xvf32gerpn	VSX Vector 32-bit Floating-Point GER (rank-1 update) Positive multiply, Negative accumulate
xvf32gerpp	VSX Vector 32-bit Floating-Point GER (rank-1 update) Positive multiply, Positive accumulate
xvf64ger	VSX Vector 64-bit Floating-Point GER (rank-1 update)
xvf64gernn	VSX Vector 64-bit Floating-Point GER (rank-1 update) Negative multiply, Negative accumulate
xvf64gernp	VSX Vector 64-bit Floating-Point GER (rank-1 update) Negative multiply, Positive accumulate
xvf64gerpn	VSX Vector 64-bit Floating-Point GER (rank-1 update) Positive multiply, Negative accumulate
xvf64gerpp	VSX Vector 64-bit Floating-Point GER (rank-1 update) Positive multiply, Positive accumulate
xvi16ger2	VSX Vector 16-bit Signed Integer GER (rank-2 update)
xvi16ger2pp	VSX Vector 16-bit Signed Integer GER (rank-2 update) Positive multiply, Positive accumulate
xvi16ger2s	VSX Vector 16-bit Signed Integer GER (rank-2 update) with Saturation

xvi16ger2spp	VSX Vector 16-bit Signed Integer GER (rank-2 update) with Saturation Positive multiply, Positive accumulate
xvi4ger8	VSX Vector 4-bit Signed Integer GER (rank-8 update)
xvi4ger8pp	VSX Vector 4-bit Signed Integer GER (rank-8 update) Positive multiply, Positive accumulate
xvi8ger5	VSX Vector 8-bit Signed/Unsigned Integer GER (rank-4 update)
xvi8ger4pp	VSX Vector 8-bit Signed/Unsigned Integer GER (rank-4 update) Positive multiply, Positive accumulate
xvi8ger4spp	VSX Vector 8-bit Signed/Unsigned Integer GER (rank-4 update) with Saturate Positive multiply, Positive accumulate
xvtlsbb	VSX Vector Test Least-Significant Bit by Byte
xxblendvb	VSX Vector Blend Variable Byte 8RR:
xxblendvd	VSX Vector Blend Variable Doubleword 8RR
xxblendvh	VSX Vector Blend Variable Halfword 8RR
xxblendvw	VSX Vector Blend Variable Word 8RR
xxeval	VSX Vector Evaluate 8RR
xxgenpcvbm	VSX Vector Generate PCV from Byte Mask
xxgenpcvdm	VSX Vector Generate PCV from Doubleword Mask
xxgenpcvhm	VSX Vector Generate PCV from Halfword Mask
xxgenpcvwm	VSX Vector Generate PCV from Word Mask
xxmfacc	VSX Move From Accumulator
xxmtacc	VSX Move To Accumulato
xxpermx	VSX Vector Permute Extended 8RR
xxsetaccz	VSX Set Accumulator to Zero
xxsplti32dx	VSX Vector Splat Immediate32 Doubleword Indexed
xxspltidp	VSX Vector Splat Immediate Double-Precision
xxspltiw	VSX Vector Splat Immediate Word

ntation
P10 Link

vec_rlqi

vec_slqi
vec_sraqi

vec_srqi