







Open3DBench: 3D-IC Backend Implementation Flow

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github:



arXiv:



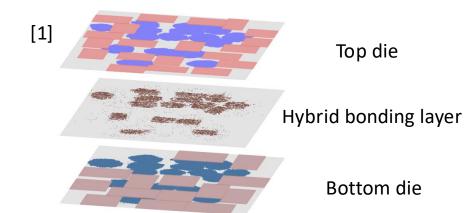
Why Open3DBench?

- 3D-IC physical design research has attracted tremendous attention these years.
- We want to test our 3D algorithms in a **standardized** and **reliable** way.

Taking 3D placement as an example:

Contest benchmarks:

- 3D Placement with D2D Vertical Connections @ ICCAD'22 Contest
- 3D Placement with Macros @ ICCAD'23 Contest



• Such contest benchmarks provide standardized comparison. But the host did not provide any implementation details (including valid PDK or design RTLs), narrowing the use of test cases.

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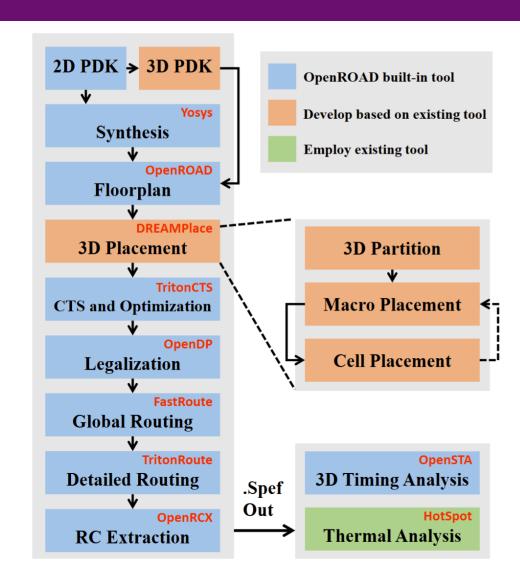
Taking 3D placement as an example:

Workaround by 2D backend flow:

- Macro-3D [1], Pin-3D [2], 3D Net-to-Pad Assignment [3] use Innovus to perform 3D backend flow.
- TA-3D [4] builds a 3D timing model using 2D tool OpenSTA.
- Commercial tools and commercial PDKs prevent replicable comparisons due to license issue.
- Building our own workaround flow may be time consuming and sometimes not reliable enough.
- [1] Bamberg, Lennart, et al. "Macro-3D: A physical design methodology for face-to-face-stacked heterogeneous 3D ICs." DATE 2020.
- [2] Pentapati, Sai Surya Kiran, et al. "Pin-3D: A physical synthesis and post-layout optimization flow for heterogeneous monolithic 3D ICs." ICCAD 2020.
- [3] Vanna-iampikul, Pruek, et al. "Placement-Aware 3D Net-to-Pad Assignment for Array-Style Hybrid Bonding 3D ICs." ISPD 2025.
- [4] Kim, Donggyu, et al. "TA3D: Timing-Aware 3D IC Partitioning and Placement by Optimizing the Critical Path." MLCAD 2024

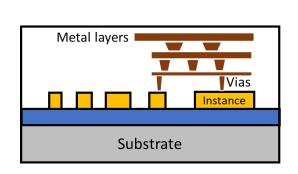
Main purpose:

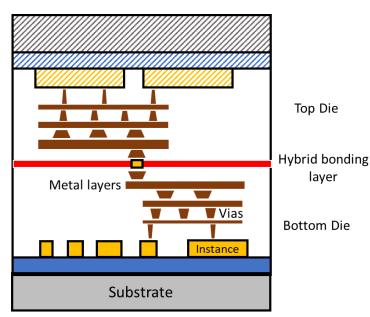
Benchmarking everything in 3D backend flow

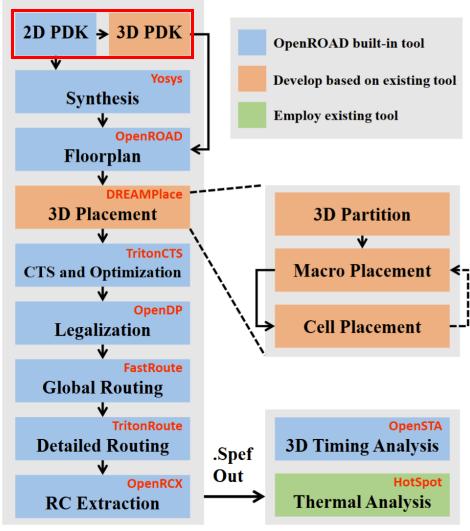


Key idea:

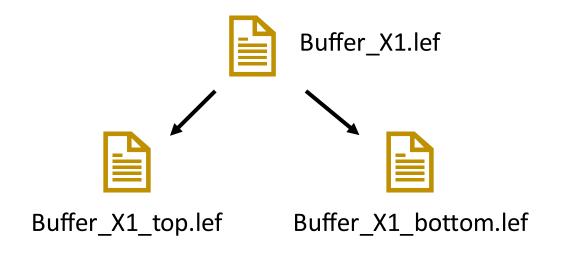
Double the original 2D metal layers and implement the 3D design on one die (like Macro-3D [1]).

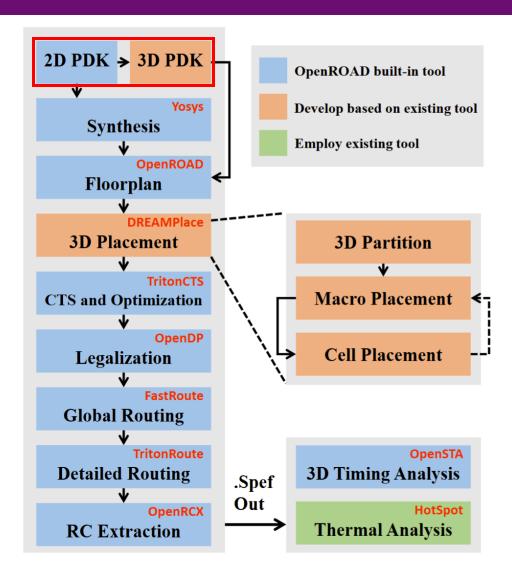






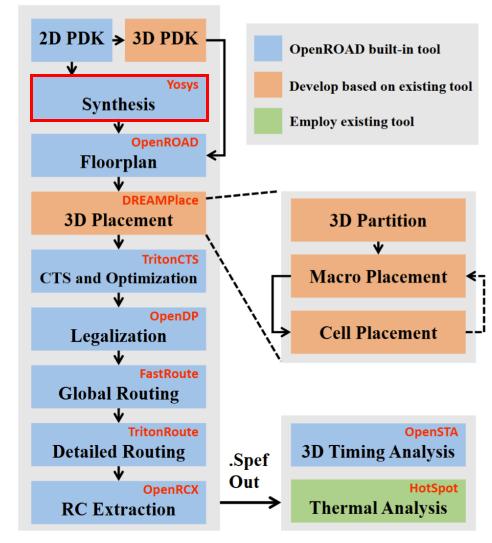
- PDK preparation: Modify NG45 to NG45_3D
 - Duplicate the metal layer in *techlef*
 - Duplicate the instance lef and lib to distinguish top and bottom die





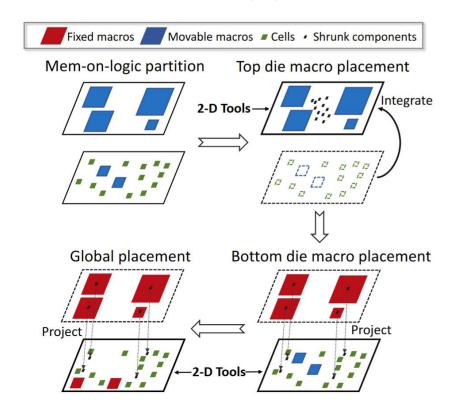
Design preparation:

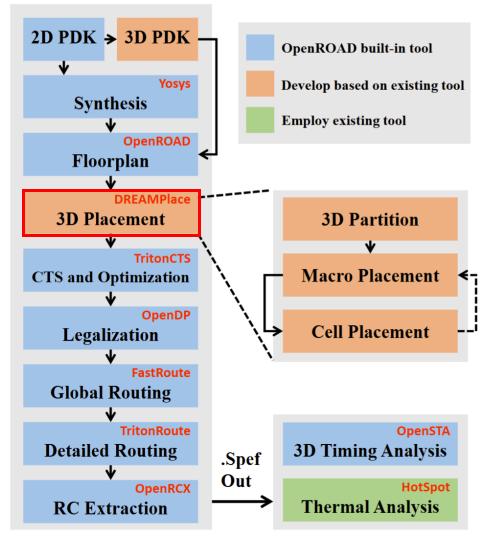
Any 2D design (RTL / netlist) supported by OpenROAD-flow-scripts



3D Placement:

Adopt 2D DREAMPlace [1] for workaround





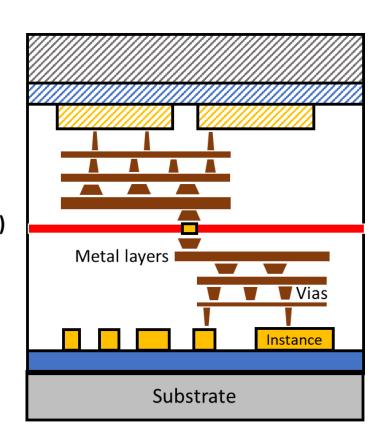
[1] Lin, Yibo, et al. "DREAMPlace: Deep learning toolkit-enabled GPU acceleration for modern VLSI placement." DAC 2019.

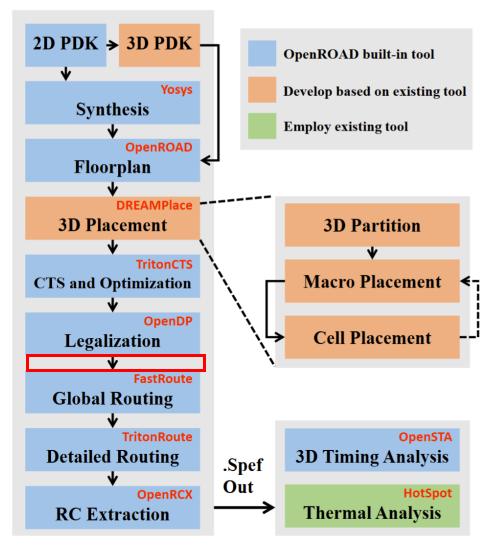
Hybrid Bonding Terminal (HBT)

Top Die

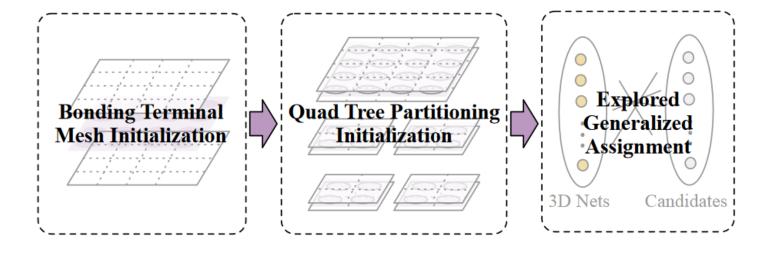
HBT layer (metal layer, resource = 0) Insert a buffer pin serving HBT

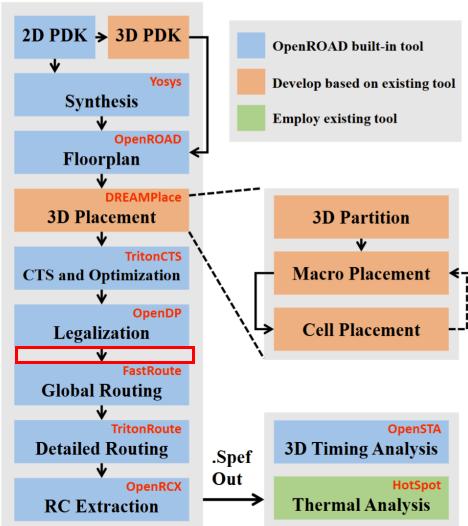
Bottom Die





Hybrid Bonding Terminal (HBT)

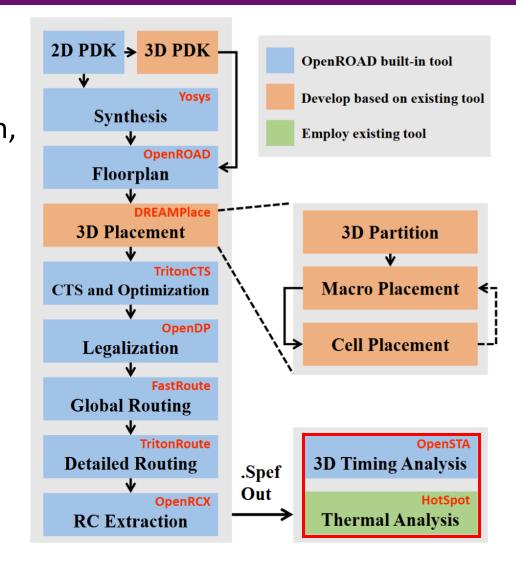




PPA evaluation

Since we establish the whole design on a 2D vision, and have defined the 3D connections properly, the original 2D OpenSTA [1] can serve 3D timing analysis.

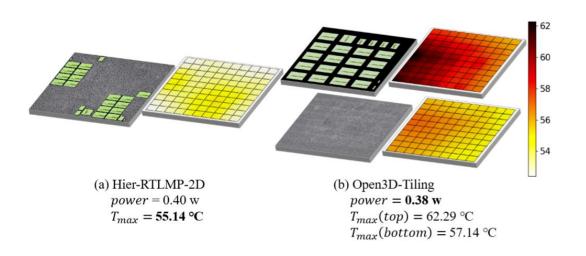
HotSpot [2] supports 3D inherently.



^[1] https://github.com/The-OpenROAD-Project/OpenSTA

^[2] https://github.com/uvahotspot/HotSpot

Some evaluations

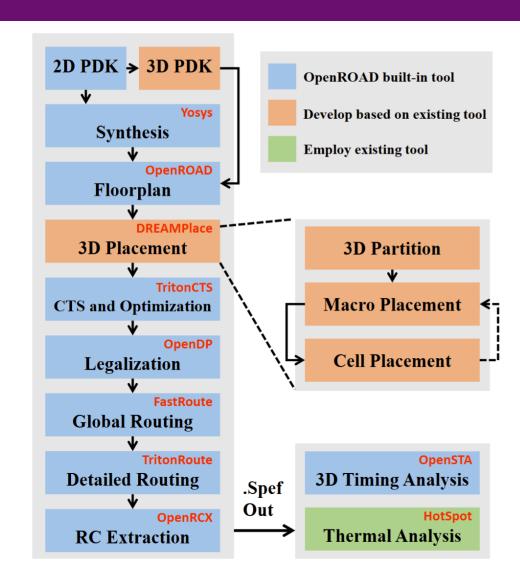


Designs	Methods	Area	rWL	Overflow	WNS	TNS	Power	T_{max}	Runtime
		(mm^2)	(m)	(#)	(ns)	(ns)	(W)	(°C)	(s)
ariane133	Hier-RTLMP-2D	2.25	8.20	132	-2.18	-5766.41	0.393	58.84	3667
	DREAMPlace-2D	2.25	7.18	112	-1.69	-4098.04	0.389	58.69	1556
	Open3D-Tiling	1.00	6.21	0	-1.40	-3049.41	0.360	58.35	1743
	Open3D-DMP	1.00	5.59	0	-1.34	-2648.76	0.360	58.21	1739
ariane136	Hier-RTLMP-2D	2.25	8.63	127	-2.51	-7072.67	0.514	63.40	1779
	DREAMPlace-2D	2.25	7.80	148	-2.71	-7561.23	0.508	61.14	1720
	Open3D-Tiling	1.00	6.32	0	-2.38	-6125.24	0.471	60.93	1791
	Open3D-DMP	1.00	6.05	0	-2.45	-6603.91	0.471	62.27	1870
black_parrot	Hier-RTLMP-2D	1.76	12.41	68	-6.96	-6289.17	0.398	55.14	1819
	DREAMPlace-2D	1.76	12.23	334	-6.57	-5268.85	0.399	55.26	1728
	Open3D-Tiling	0.81	8.08	0	-5.76	-2251.30	0.376	62.29	1895
	Open3D-DMP	0.81	7.79	0	-5.67	-4067.11	0.374	60.97	1920
bp_be	Hier-RTLMP-2D	0.56	3.00	30	-1.88	-523.27	0.152	52.63	1063
	DREAMPlace-2D	0.56	2.89	36	-1.30	-246.99	0.153	53.08	916
	Open3D-Tiling	0.30	2.40	0	-1.21	-188.86	0.144	61.17	998
	Open3D-DMP	0.30	2.42	0	-0.89	-108.89	0.144	59.11	1053
bp_fe	Hier-RTLMP-2D	0.48	1.81	6	-1.40	-942.36	0.302	64.09	449
	DREAMPlace-2D	0.48	1.73	30	-1.51	-978.59	0.305	63.62	239
	Open3D-Tiling	0.24	1.38	0	-1.53	-729.42	0.284	87.33	398
	Open3D-DMP	0.24	1.30	0	-1.37	-814.64	0.283	82.32	388
bp_multi	Hier-RTLMP-2D	1.21	6.20	36	-7.97	-12072.10	1.143	86.18	868
	DREAMPlace-2D	1.21	5.63	9	-8.30	-10946.20	1.126	85.50	760
	Open3D-Tiling	0.64	4.06	0	-7.01	-9246.70	1.062	112.09	883
	Open3D-DMP	0.64	4.03	0	-8.03	-9812.57	1.050	98.09	935
bp_quad	Hier-RTLMP-2D	12.96	46.63	3429	-3.66	-39020.00	1.822	66.05	8010
	DREAMPlace-2D	12.96	41.99	3968	-2.05	-31231.90	1.848	68.17	6336
	Open3D-Tiling	6.25	50.19	0	-2.62	-31124.70	1.840	69.78	7973
	Open3D-DMP	6.25	40.39	0	-1.83	-26966.20	1.832	66.96	7981
swerv_wrapper	Hier-RTLMP-2D	1.10	5.62	14428	-2.14	-1975.79	0.250	54.86	1175
	DREAMPlace-2D	1.10	5.54	9540	-1.86	-1429.90	0.254	53.48	1092
	Open3D-Tiling	0.56	3.63	0	-1.26	-972.80	0.232	62.17	2085
	Open3D-DMP	0.56	3.46	0	-1.23	-958.01	0.234	60.49	1744
3D improvements over 2D†		51.19%↑	24.06%	100%↑	16.24%	30.84%↑	5.72%↑	-10.04%↓	-24.82%↓
3D-DMP improvements over 3D-Tiling		Equal	5.96%↑	Equal	7.22%↑	-4.49%↓	1.98%	3.56%	0.23%

Limitations

- Heterogeneous
- TSV consideration
- 3D power distribution network
- 3D buffering & sizing

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Thank you!

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github:



arXiv:

