Open Tools for Advanced Packaging STCO

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THE CHIPS TO SYSTEMS CONFERENCE

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YAP: <u>Y</u>ield Modeling for <u>A</u>dvanced <u>P</u>ackaging

*Github: https://github.com/nanocad-lab/YAP | GUI: http://nanocad.ee.ucla.edu:8081/yap_gui/ | - Zhichao Chen*
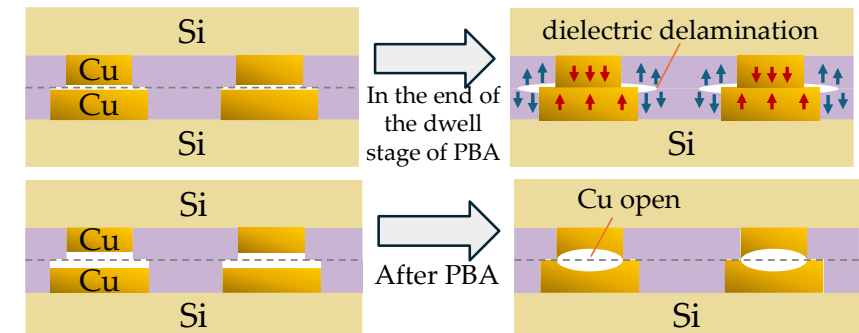
- Traditional yield models are inadequate for addressing the complexities inherent in hybrid bonding technology.
- The **first** published yield model for hybrid bonding technology accounting for multiple failure mechanisms:
  - Overlay errors, particle defects, Cu recess variations
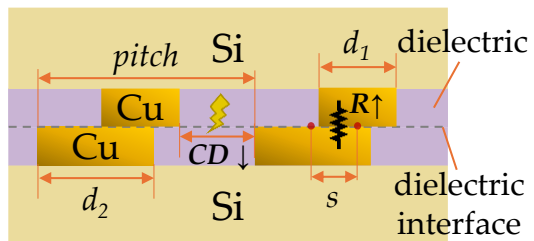
Misalignment caused by overlay errors
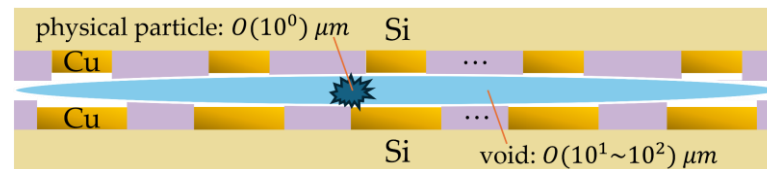
Voids caused by particle defects

Delamination/Open caused by too high/low Cu recess

YAP: <u>Y</u>ield Modeling for <u>A</u>dvanced <u>P</u>ackaging
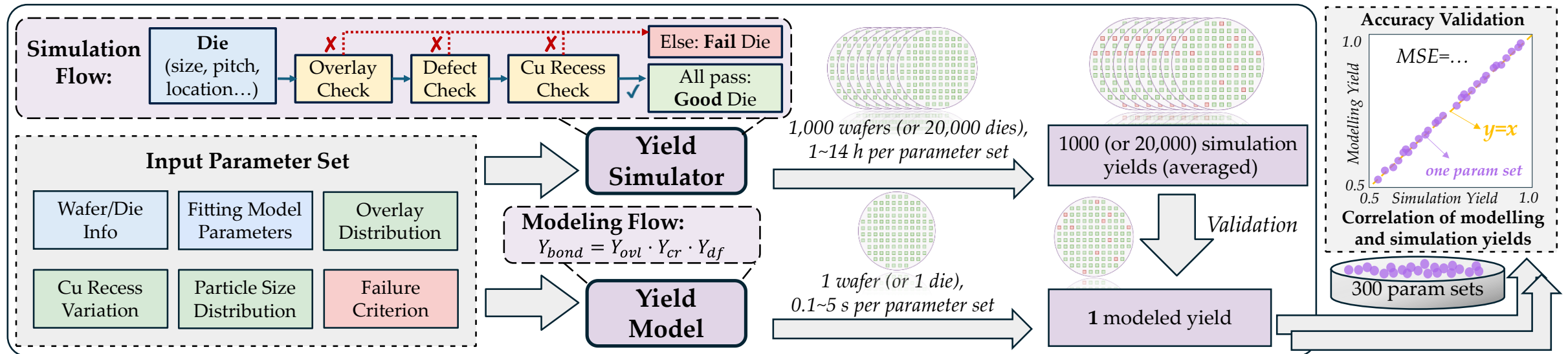
Github: *https://github.com/nanocad-lab/YAP* | *GUI:* *http://nanocad.ee.ucla.edu:8081/yap_gui/* | *- Zhichao Chen*

- YAP achieves virtually identical accuracy while offering over **10,000x** faster runtime.
- Perform case studies to:
  - Show impacts of each input parameter (chiplet size, pitch, particle density, …...).
  - Compare W2W & D2W hybrid bonding.

Simulation Flow: Die (size, pitch, location…) → Overlay Check ✗ → Defect Check ✗ → Cu Recess Check ✗ → Else: **Fail** Die / All pass: **Good** Die ✓

Input Parameter Set
- Wafer/Die Info
- Fitting Model Parameters
- Overlay Distribution
- Cu Recess Variation
- Particle Size Distribution
- Failure Criterion

Yield Simulator

Modeling Flow: $Y_{bond} = Y_{ovl} \cdot Y_{cr} \cdot Y_{df}$

Yield Model

1,000 wafers (or 20,000 dies), 1~14 h per parameter set

1 wafer (or 1 die), 0.1~5 s per parameter set

1000 (or 20,000) simulation yields (averaged)

Validation

1 modeled yield

Accuracy Validation
$MSE=...$
$y=x$
one param set
Modelling Yield (0.5 – 1.0) vs Simulation Yield (0.5 – 1.0)

Correlation of modelling and simulation yields

300 param sets

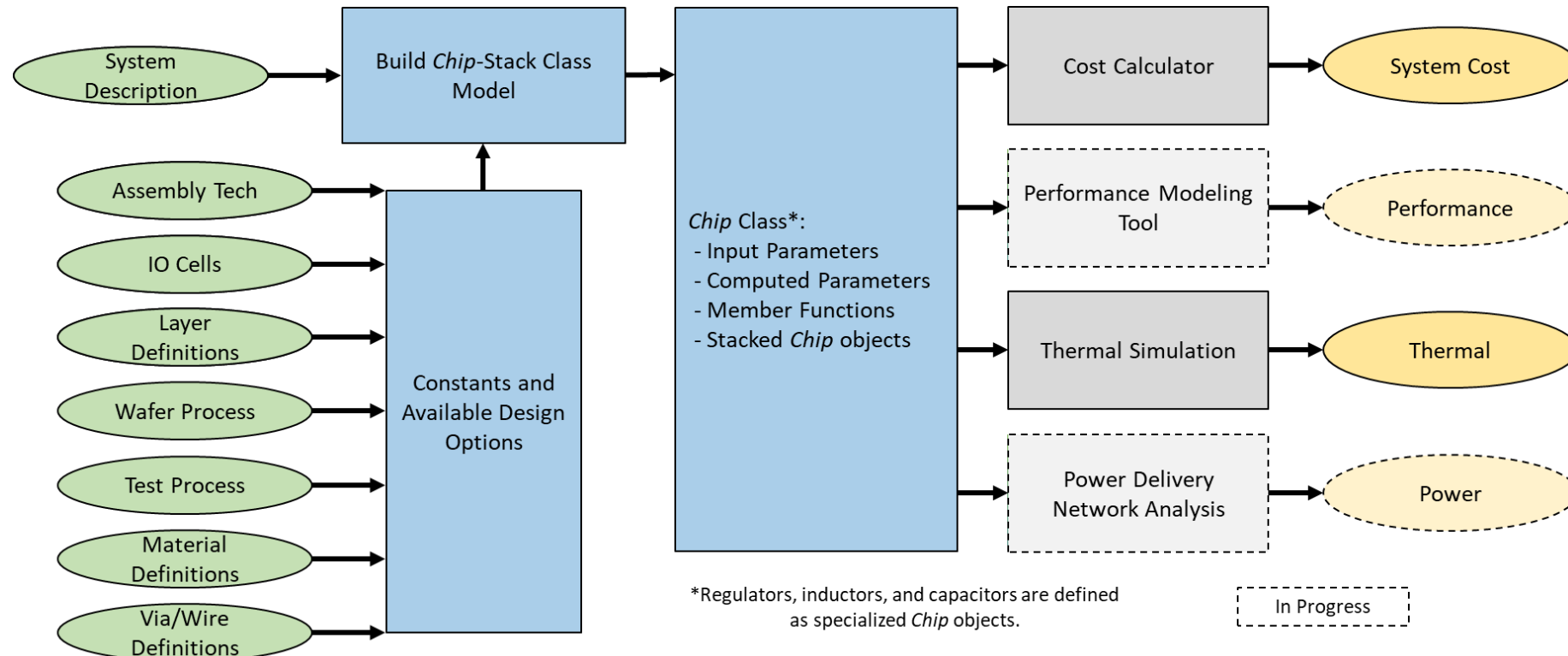**Date:** Wednesday, June 25, 11:15am - 11:30am PDT
Site: 3003, Level 3
Session: Welcome to the Silicon Rodeo: Wrangling Transistors, Taming Yield, and Riding the 3D Packaging Frontier

CATCH: Cost Model for Stacks of Chiplets

Github: *https://github.com/nanocad-lab/CATCH* | *- Alexander Graening*

- Fully parameterized with system definition plus "library files" defining various processes.
- Case studies to show impacts of each parameter.
- Deployed at IMEC and Analog Devices for their internal use.


*Regulators, inductors, and capacitors are defined as specialized *Chip* objects.*

In Progress

CATCH: Cost Model for Stacks of Chiplets

Github: *https://github.com/nanocad-lab/CATCH* | *- Alexander Graening*

File Structure:

- **System definition:**
  - Structured around a Chip object definition.
  - Each *Chip* contains *Chip* specific parameters and library references.
  - *Chips* may be stacked on top or bottom of the root *Chip*.
  - XML file format.

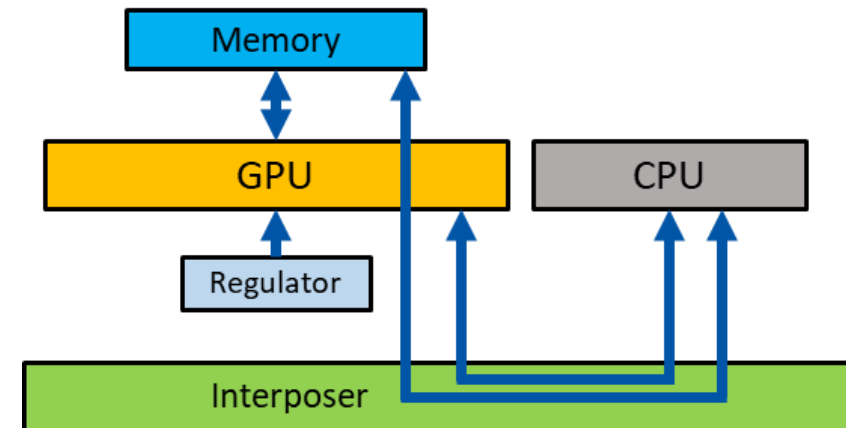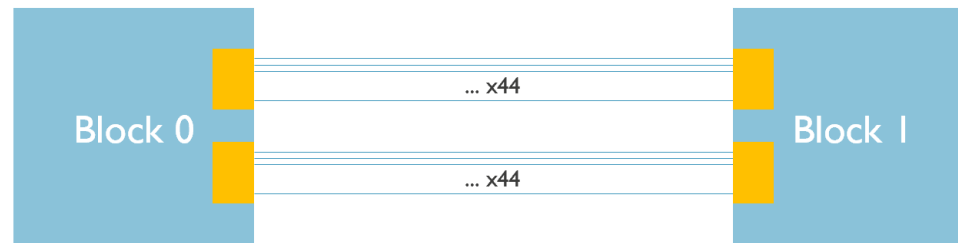# CATCH: Cost Model for Stacks of Chiplets
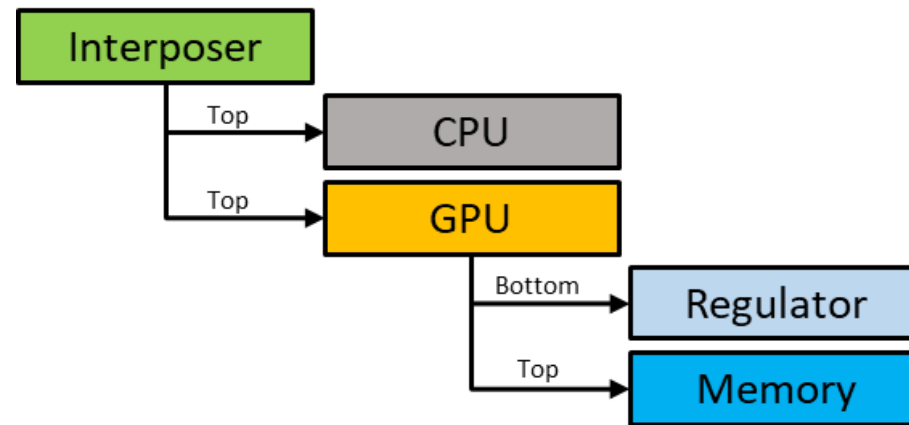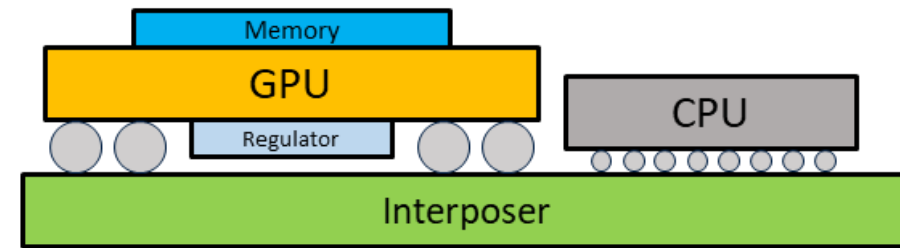
Github: *https://github.com/nanocad-lab/CATCH* | *- Alexander Graening*

File Structure:

- **Netlist definition:**
  - Netlist is defined as connections between Chip objects with a defined IO type.
  - Connections are defined by a bandwidth or a count.
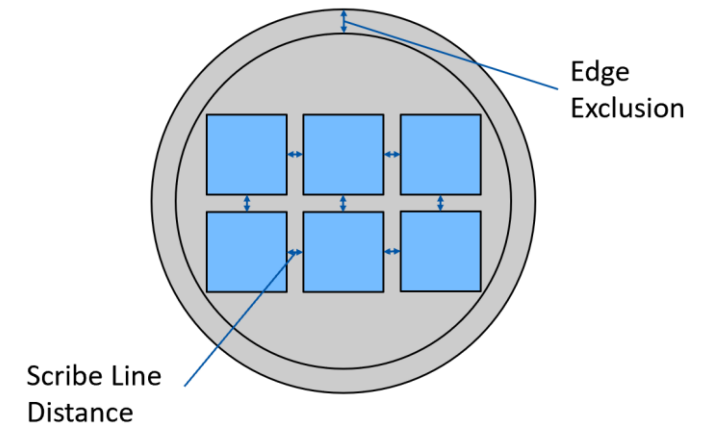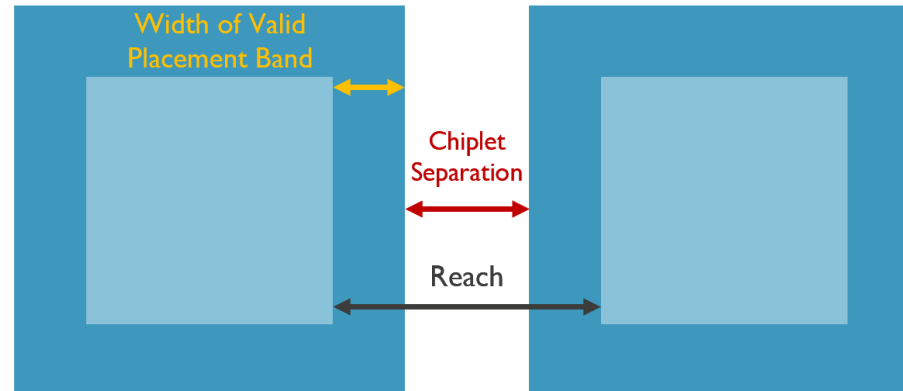 - The IO area is added to die area.

CATCH: Cost Model for Stacks of Chiplets

Github: https://github.com/nanocad-lab/CATCH | - Alexander Graening

File Structure:

- **Library Files**
  - Assembly process
  - IO Type
  - Wafer process
  - Test process
  - Layer definitions
  - Via/Wire definitions
  - Material definitions
  - …

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