Yosys-slang: Fast open-source SystemVerilog frontend for Yosys

DAC 2025: Open-Source EDA Birds-of-a-Feather Session

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Yosys: Logic synthesis tool

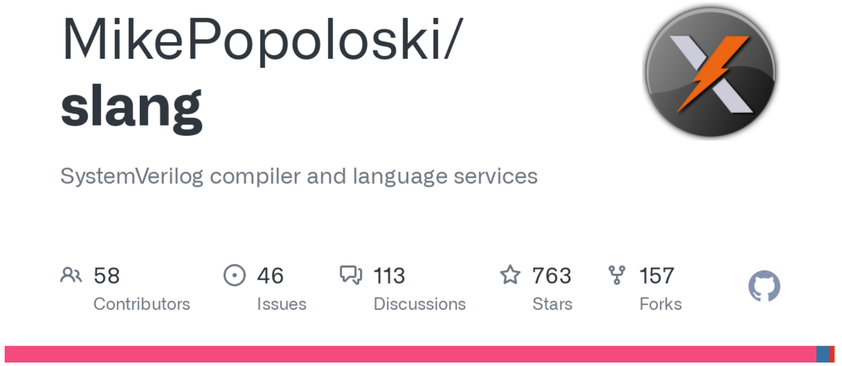
Very popular and fully open-source

- Synthesis tool for Verilog-2005
  - Little native support for SystemVerilog
- Has a powerful intermediate representation: RTLIL
  - Allows *custom passes* to manipulate RTLIL
    - For optimizations, analysis, etc.
- Developed by Claire Wolf (clairexen) circa 2013, now maintained by YosysHQ
- Available under ISC license; compatible with FPGA/ASIC flows

Slang: C++ frontend for SystemVerilog

Fully-compliant and blazing fast

- Hand-written parser and resolver for SystemVerilog
  - No lexer/parser generators involved!
- Developed by Mike Popoloski (MikePopoloski)
- Fully compliant with latest IEEE 1800-2023
- Only open-source tool that can fully parse 3033/3033 sv-tests
- Written in C++, also has a Python frontend (pyslang)
- Available under MIT license since 2015



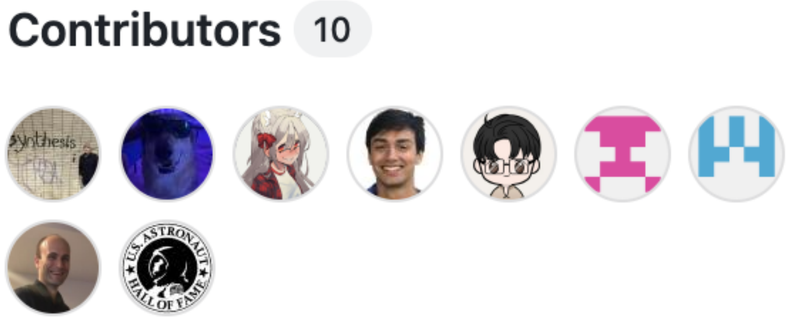
Yosys-slang: SystemVerilog plugin for Yosys

The marriage between Yosys and Slang

- **Key idea:** Slang elaborates hierarchy, resolves constants, types, and name references; yosys-slang performs symbolic execution, emits word-level RTLIL
- Developed by Martin Povišer (povik), formerly YosysHQ, now at Precision Inno
  - Inspired by svase by Paul Scheffler (paulsc96) of PULP group
  - Conceived at Yosys User's Group in 2024; available under ISC license
- Supporters/contributors:

ETH zürich SILIMATE

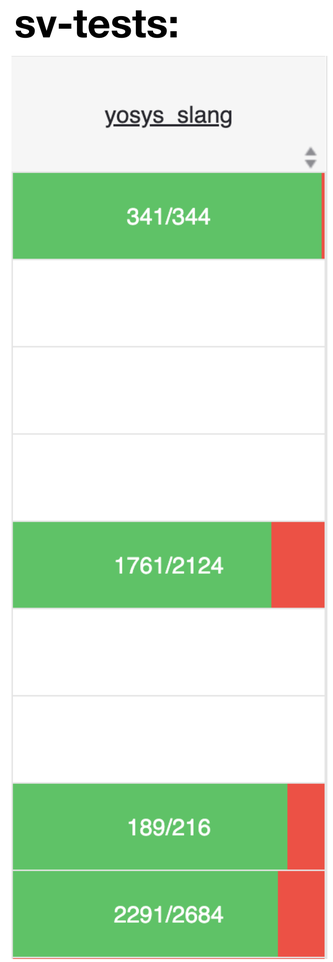
YosysHQ



Current status

Ready for use in ~99% of real-world designs!

- Passing most of synthesizable sv-tests
  - Few known exceptions for uncommon language features
- Able to correctly elaborate large designs
  - Black Parrot
  - BSC Core Tile
  - OpenHW Group's CV32E40P
  - Ibex RISC-V Core
  - OpenTitan
  - RSD RISC-V Processor



Benchmarking (preliminary)

Yosys-slang is on par with (slightly faster than) Tabby CAD Suite

- CPU: Apple M1 Pro
- OS: macOS
- Reduced runtimes
- Reduced memory usage
- With instance caching enabled
  - Without instance caching, a bit worse
- Synlig: not able to compile these

	Yosys-slang Runtime	Tabby CAD Runtime	Yosys-slang Peak RAM	Tabby CAD Peak RAM
OpenTitan Earlgrey	12.4 s	16.3 s	1.7 GB	2.6 GB
CVA6	3.1 s	7.2 s	0.5 GB	1.5 GB
Black Parrot	4.5 s	4.5 s	0.4 GB	0.8 GB

Comparison with alternatives

Verific, Synlig, sv2v, bsg_sv2v

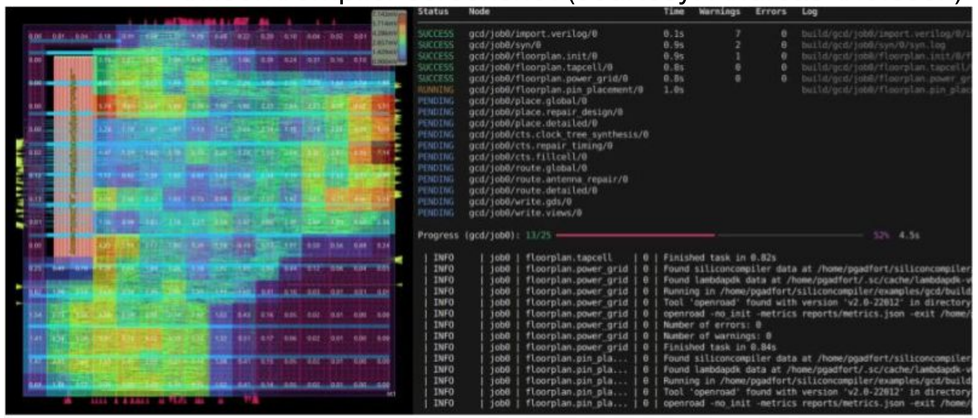
- Use Verific frontend for Yosys (not open-source)
  - Fast and fully compliant with IEEE 1800-2023 SystemVerilog standard
  - Available for no cost via Tabby CAD Suite for academic use, but not for professional use
- Use Synlig frontend for Yosys (open-source: Apache-2.0)
  - Uses Surelog to elaborate, UHDM as IR, dumps to Yosys AST
- Use sv2v to convert SystemVerilog to Verilog, then use Yosys as usual (open-source: BSD-3)
  - Almost fully compliant, but missing thorough validation
- Use bsg_sv2v (open-source: BSD-3, but also requires Synopsys DesignCompiler...)

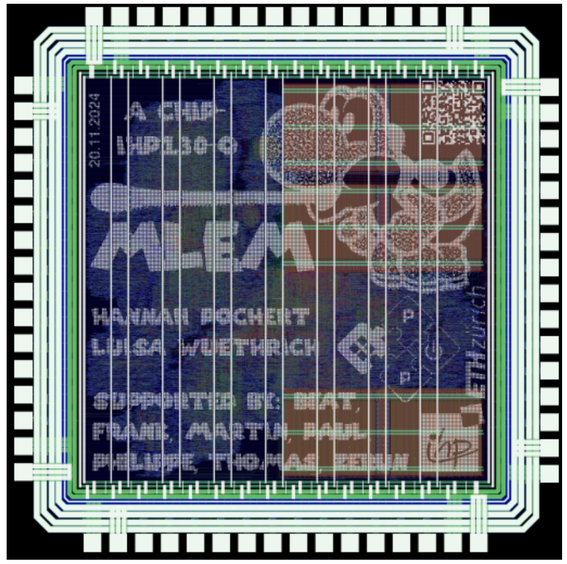
Real-world adoption

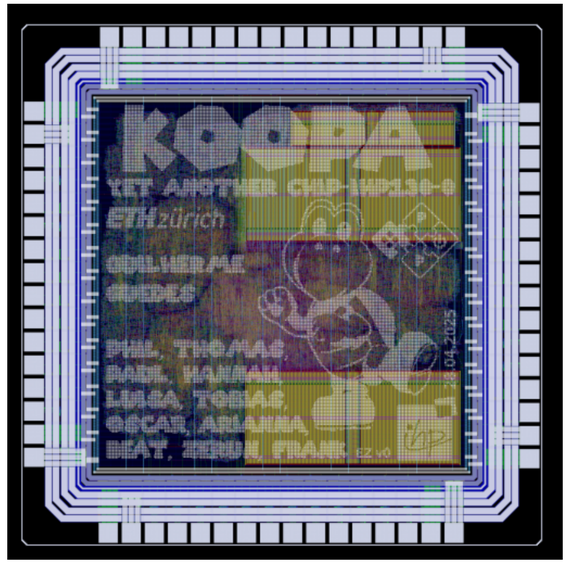
Where is yosys-slang being used?

- PULP Tapeouts: MLEM, KOOPA
- YosysHQ's OSS CAD Suite
- Zero ASIC's SiliconCompiler
- JKU's IIC-OSIC-TOOLS
- OpenROAD Flow Scripts

SiliconCompiler screenshot (courtesy: Andreas Olofsson)



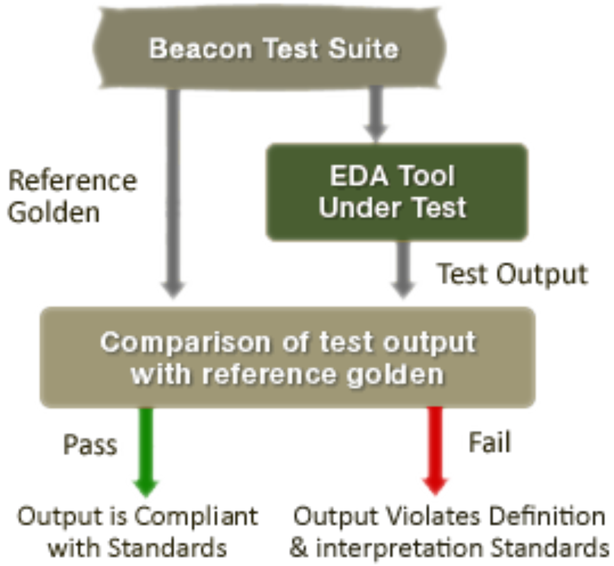




Future Plans

What's next for yosys-slang?

- Add support for last few synthesizable language features
- Formal equivalence checks against other tools
- Simulated equivalence checks with Interra Beacon
- Testing on more and larger (>1M gate) designs
- Generalize to act as frontend for other tools



Thank you!

Silimate is hiring: https://www.silimate.com

- Building the co-pilot for chip designers
- We love, use, and support open-source EDA (OpenSTA, Yosys, etc.)
- Well-funded and backed by Y Combinator
- Used by companies like SiFive, Tenstorrent
  - And more companies we can't disclose yet...
- Come chat with me!
  - Also, my email is akash@silimate.com

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BACKUP: Current feature/issue status

Beta features, todo features, known bugs

- BETA: Non-uniquified hierarchy
- FEATURE: Support `celldefine
- FEATURE: Break down structs
- FEATURE: Support SR latches/FFs
- FEATURE: Support foreach loops
- FEATURE: Support .prev, .next
- FEATURE: Better loop unrolling
- FEATURE: Support inout without keep hierarchy
- FEATURE: Graceful handling of non-synthesizable constructs
- FEATURE: Support initial
- BUG: Write addressing with latches
- BUG: Unpacked unions
- BUG: Large case statement timeout