Pacific Northwest
NATIONAL LABORATORY

SODA Toolchain & DeCoDe

Open-Source EDA, Data, and Collaboration BoF
DAC 2025
June 24, 2025

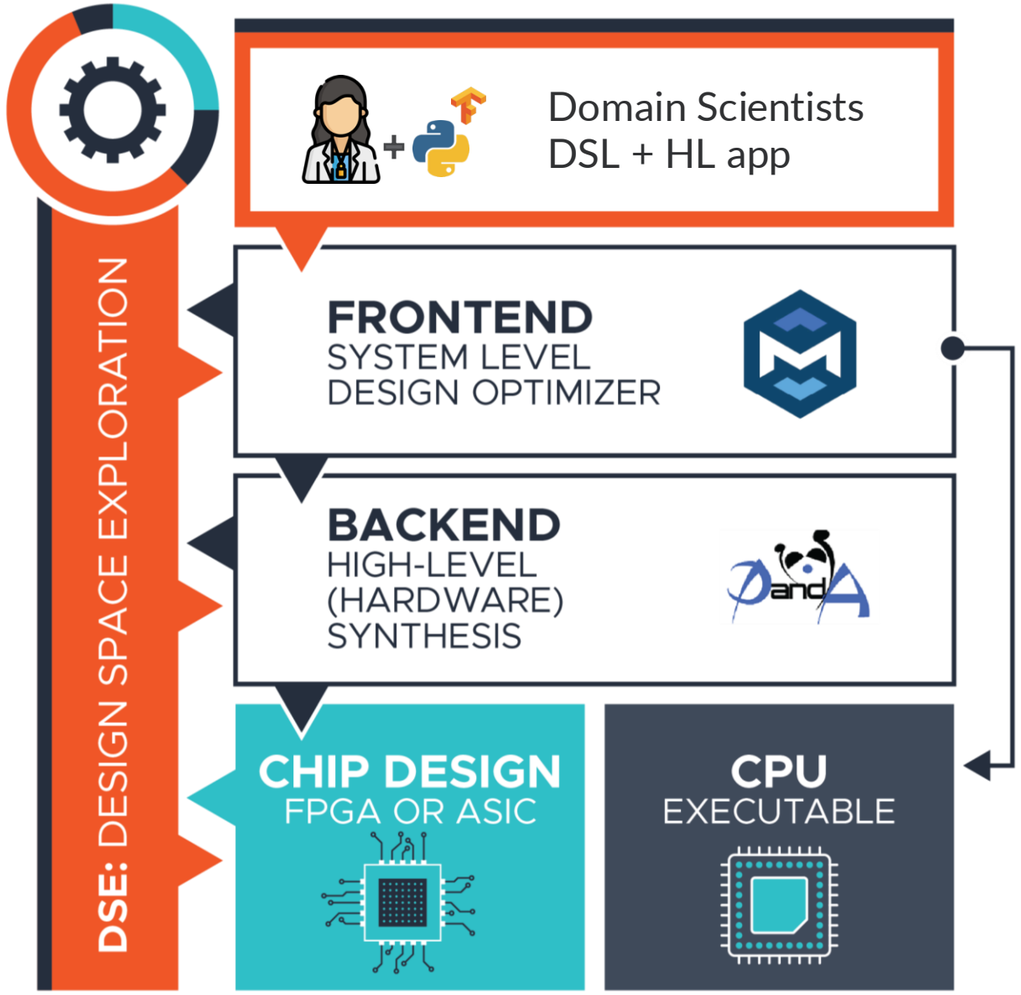
Ankur Limaye
Pacific Northwest National Laboratory

U.S. DEPARTMENT OF ENERGY BATTELLE

PNNL is operated by Battelle for the U.S. Department of Energy

SODA Toolchain to design custom accelerators

- SODA: Software-defined Architectures
  - Open-source, multi-level compiler toolchain to automatically generate hardware designs from high-level programming frameworks
- Compiler-based frontend, SODA-OPT: Search, Outline, Dispatch, Accelerate frontend optimizer generates the "soda" High-Level IR
  - Interfaces with high-level ML frameworks leveraging MLIR bridges (e.g., libraries, rewriters)
  - Compiler optimization passes to identify dataflow segments, perform high-level optimizations, and generate host/runtime calls
- Compiler-based backend, Bambu HLS: generates hardware designs
  - Targets FPGAs and ASICs
- Supports automated design space exploration



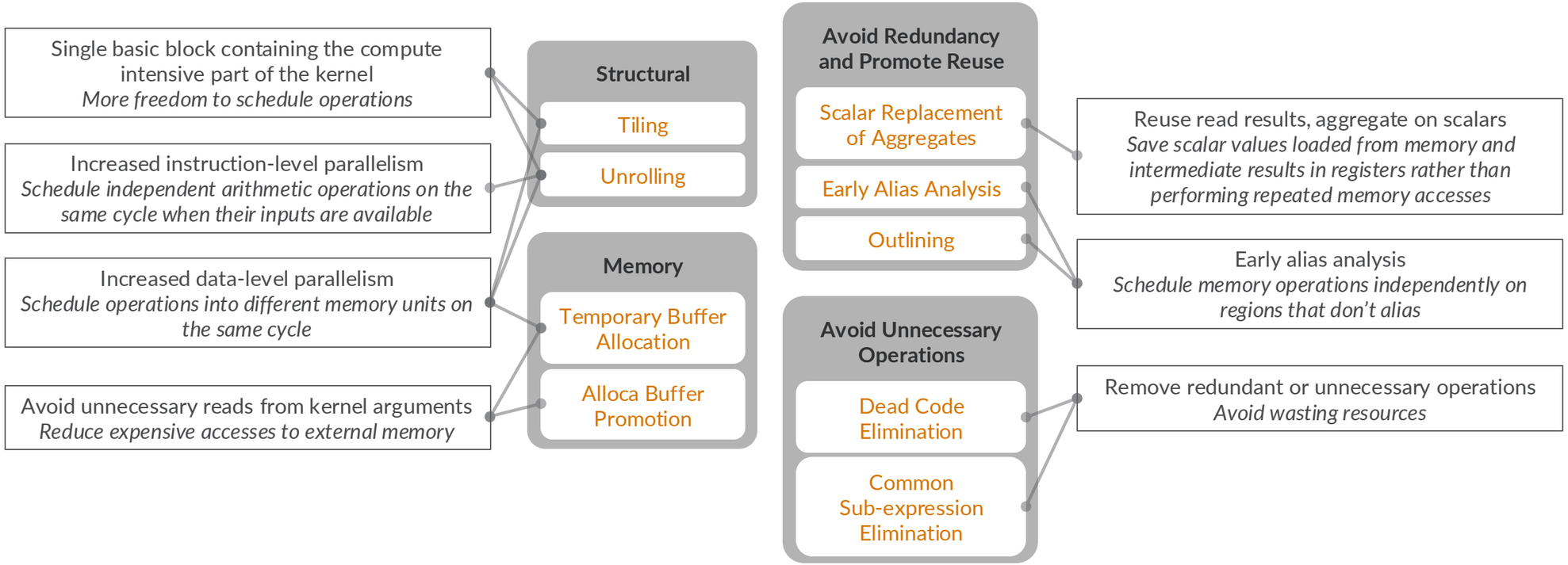
[V. G. Castellana, *et al.*: Software-defined Architectures for Data Analytics. *ASP-DAC 2019*]
[N. Bohm Agostini, *et al.*: Bridging Python to Silicon: The SODA Toolchain. IEEE Micro *2022* (***Best Paper***)]
[F. Ferrandi, *et al.* : Bambu: an Open-Source Research Framework for the High-Level Synthesis of Complex Applications. *DAC 2021*]

SODA-OPT & Bambu HLS

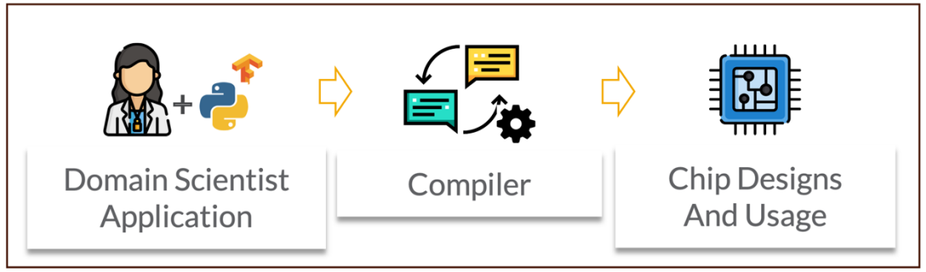
SODA-OPT

Bambu HLS

- SODA-OPT optimization passes:



DeCoDe: Democratizing Co-Design for Energy-efficient Scientific Computing



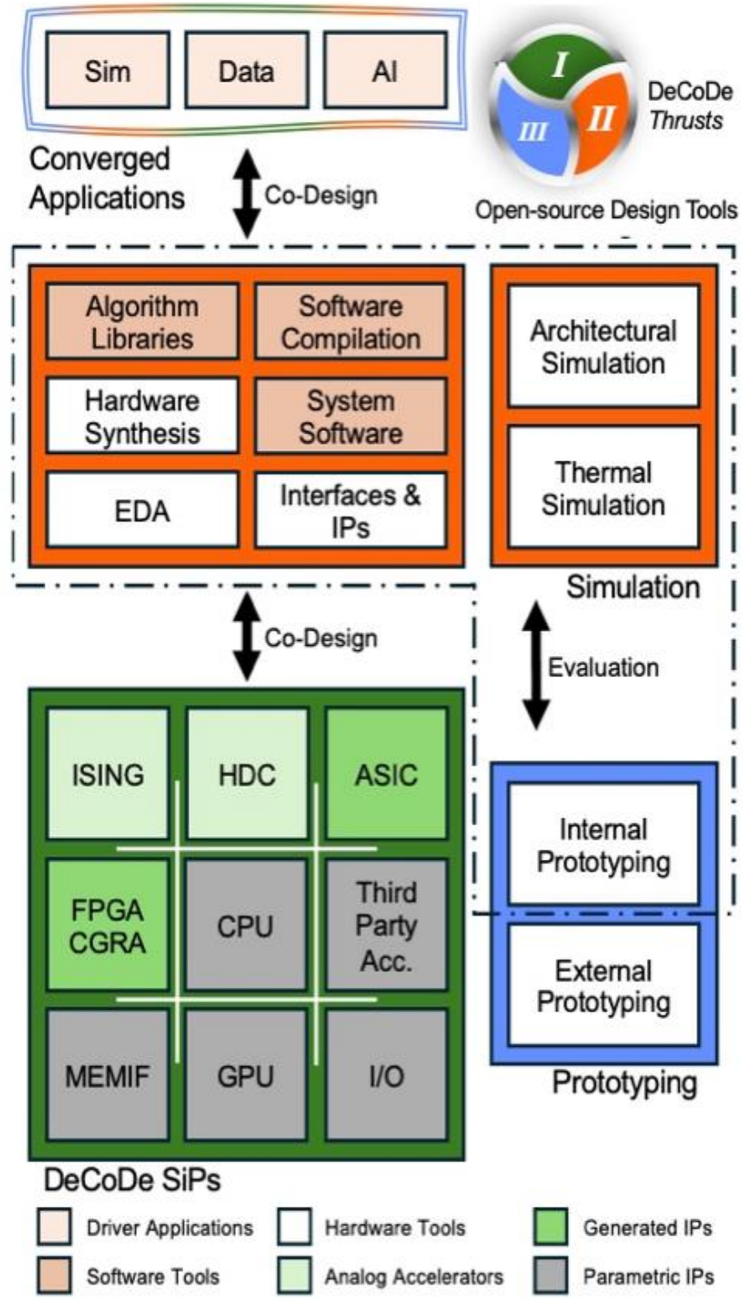
- Focuses on lowering the cost of developing and deploying open-source, optimized hardware designs
- Support PCAST CHIPS Act advice on computing innovations:
  - Target goals for energy-efficient computing
  - Drive the co-design of heterogeneous processors.
- Democratizing hardware prototyping through open-source co-design tools:
  - Energy-efficient accelerators and software
  - Hardware analysis, hardware design, and hardware generators with software stack
  - Pursue open chiplet ecosystem standards
- Integrate energy efficient analog accelerator concepts into heterogeneous architectures:
  - Hyperdimensional Compute, Resistively-coupled Dynamical System Unit accelerators
  - Address DOE's Energy-Efficient Computing (EEC) objectives while retaining general-purpose for diverse scientific workloads

DeCoDe Team Capabilities

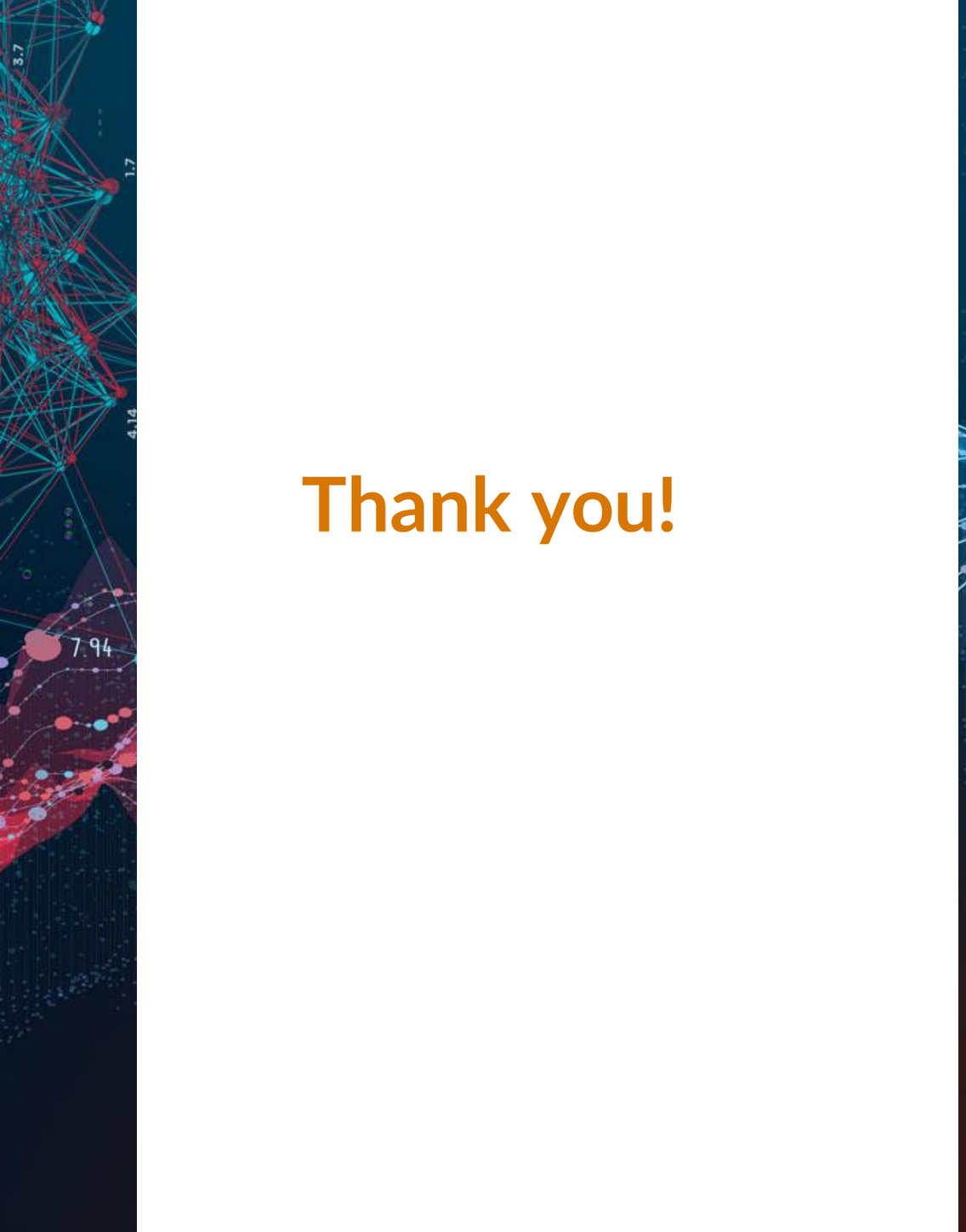
	PNNL	UCSD	Zero ASIC	TCL	Harvard	Columbia	WSU	UMN	Rochester
PI's and SKP	James Ang, Antonino Tumeo	Andrew Kahng, Tajana Rosing	Andreas Olofsson, Peter Gadfort	John Leidel, David Donofrio	David Brooks, Gu-Yeon Wei	Luca Carloni	Partha Pande, Jana Doppa	Yu (Kevin) Cao	Tong (Tony) Geng
Novel Analog Accelerators		X							X
Algorithm Libraries	X	X							X
Compilers for Heterogeneous Systems	X			X					
EDA Tools		X	X						
HLS Tools	X								
Hardware Generators	X		X	X					
Architectural Simulation Frameworks	X			X	X				
Thermal Simulation Models							X	X	
Chiplet Ecosystem Standards			X						
Prototyping Platforms	X		X			X			
Tapeout Experience		X	X		X	X		X	X

DeCoDe Approach

- Approach to generating Proof-of-Concept System Testbeds
- Thrust 1: Co-designing Energy-Efficient SiPs
  - Develop robust, versatile hardware for DOE scientific computing needs, integrating:
    - ✓ Analog accelerators (Hyperdimensional Computing & Resistively-coupled Dynamical System Machines), and
    - ✓ Conventional accelerators (CPUs, GPUs, Domain-specific accelerators)
- Thrust 2: Expanding our Open-Source Co-Design Tools
  - Build an integrated, interoperable toolchain including:
    - ✓ Energy-efficient algorithms for analog accelerators
    - ✓ Compiler framework & accelerator generators
    - ✓ Architectural and thermal simulators for heterogeneous SiPs
    - ✓ Chiplet packaging, 2.5D integration, and Interface Generator
- Thrust 3: Prototyping and Chiplet Integration
  - Establish in-house prototyping and tapeout capabilities, leveraging CHIPS Act resources



Thank you!


121.5
7.2
9.3
6.1
7.8
0.38
17.9
1.4
5.2
3.7
1.7
6.184
6.96
4.14
4.59
7.31
4.70
8.58
5.47
10.06
5.52
6.14
7.94