Federal Ministry
of Research, Technology
and Space

German Microelectronics Design Initiative Federal Ministry of Research, Technology and Space (BMFTR)

Design Automation Conference 2025, San Francisco

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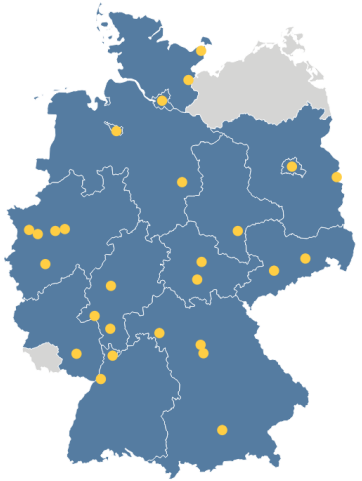
Funding program: Design instruments for sovereign chip development with open source (DE:Sign)

- Design tools, methods, and chip designs with focus on open source
- Significant development work on the open source toolchain
- Participation of young researchers and talents
- 15 projects launched with 62 partners by May 1, 2024
- Close collaboration of the projects with Chip Design Germany



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DE:Sign R&D projects on open source EDA tools

Talents: Student competition „Open source chip design challenge“ (**OCDCpro**)

Analog design

- ✓ Text based design (**ORDeC**)
- ✓ High frequency chips (**DEMICO**)

Hardware security

- ✓ HW architecture (**ExViPaS**)
- ✓ HW security module (**SIGN-HEP**)

Digital design

- ✓ eFPGAs (**OWAS**)
- ✓ FPGAs (**FEntWumS**)
- ✓ RISC-V (**GATE-V**)
- ✓ Verification (**OSVISE**)
- ✓ DRAM (**DERAMSys**)
- ✓ AI hardware (**EDAI**)

Novel technologies

- ✓ RFETs (**ReDesign**)
- ✓ MEMS/ASIC (**Meta-X**)
- ✓ Packaging/SiP (**PASSIONATE**)
- ✓ Radiation hardened HW (**Flowspace**)

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Student competition „Open source chip design challenge“ (OCDCpro)

- Development of a learning and competition platform for young students and talents
- Annual competition rounds with evolving topics
- Development of a tailored student-specific 130 nm open-source PDK
- Specification and verification of the open-source toolchain based on a demonstrator chip
- Development of teaching/learning concepts for digital design with open-source tools

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Open source design tools for sovereign chip design – research study on status and perspectives (QDISC)

- Advantages and disadvantages, innovation mechanisms
- Framework conditions for usage, compliance with industry requirements, business perspectives
- Potential for specific application industries, recommendations for action
- Start: August 1, 2024, funding period until September 30, 2025
- Tight collaboration with Chip Design Germany, science, industry and industry networks

acatech
NATIONAL ACADEMY OF SCIENCE AND ENGINEERING

Funding program: Closing gaps in design tools for sovereign chip development with open source (DE:Sign Challenge)

- R&D to bridge remaining critical points in open-source EDA toolchains
- Focus on analog/RF/mixed-signal design, data formats and interfaces, verification and testing, as well as education and training programs
- 60 project ideas submitted by March 31, 2025, currently in review
- Start: January 1, 2026, funding period until 2028
- Close collaboration with Chip Design Germany and DE:Sign projects

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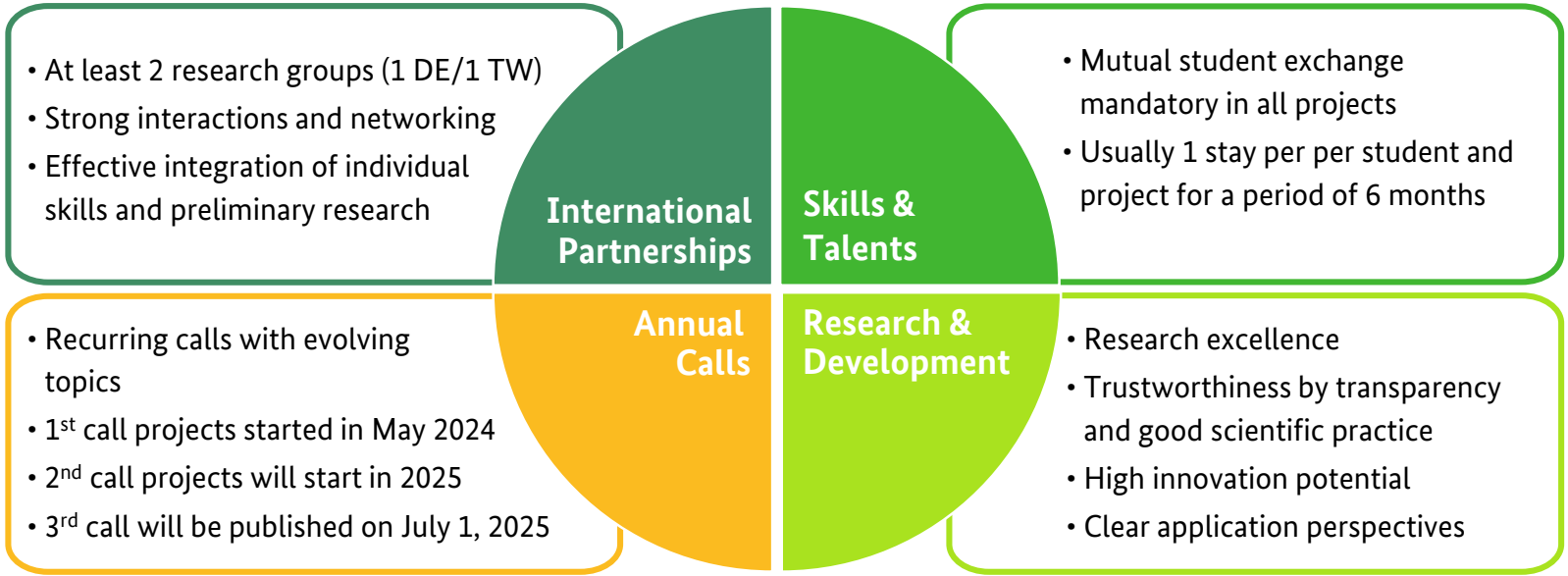
NSTC 國家科學及技術委員會
National Science and Technology Council

BMFTR/NSTC joint funding program: Research collaboration in microelectronics with Taiwan



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NSTC 國家科學及技術委員會
National Science and Technology Council

1st call R&D projects

NeuroMemSense Neuromemristive circuits as hardware accelerators for edge training and computing towards ultra-security of bio-sensors	• Prof. Choubey (Uni Siegen) • Prof. Chao – 趙昌博 (NYCU)
ATTRACTS D-Band Multipurpose Transmitter and Receiver with DDS	• Prof. Weigel (FAU Erlangen-Nürnberg) • Prof. Huang – 黃天偉 (NTU)
PNN AI Edge Applications Using PNN with High-speed and Low-power E-O Conversion Interfacing Circuits	• Prof. Gerfers (TU Berlin) • Prof. C.-C. Wang – 王朝欽 (NSYSU)
PI3D Reliability-Aware Task Deployment of Photonic Interconnected 2.5D/3D Integrated Systems	• Prof. Schlichtmann, Dr. Tsun-Ming Tseng (TU München) • Prof. Lin – 林英超 (NCKU)
TEdgeAI Ensuring Trustworthiness of Edge AI Chip	• Prof. Berekovic (Uni Lübeck) • Prof. Wu – 吳安宇 (NTU), Prof. Huang – 黃世旭 (CYCU)
FeEdge Computing-in-Memory with Ferroelectric Field Effect Transistors Featuring Normally-off Operation	• Dr. Kämpfe (FhG IPMS) • Prof. Lu – 盧達生 (NCKU)

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Federal Ministry of Research, Technology and Space
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Karlsruher Institut für Technologie

Rheinland-Pfälzische Technische Universität Kaiserslautern Landau

OPEN-SOURCE DESIGN TOOLS FOR CO-DEVELOPMENT OF AI ALGORITHMS AND AI CHIPS (DE-EDAI)

emmtrix Technologies

CREONIC ip cores & system solutions

Dream CHIP

LUBIS EDA

SMEs

SYNOPSYS®

NXP

Infineon

Large Industries (Design and EDA)

BMW GROUP

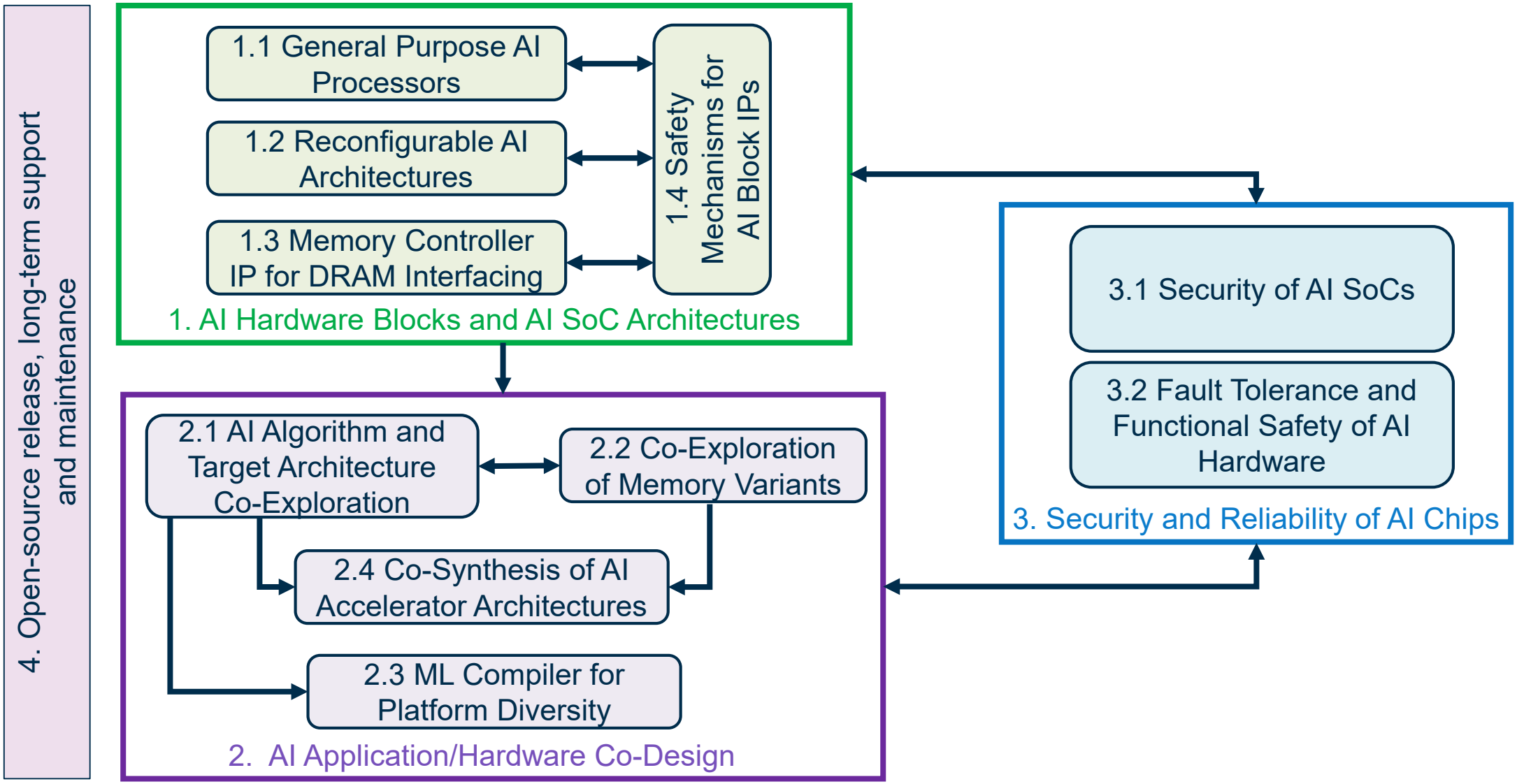
SCHAEFFLER

End Users

With funding from the:

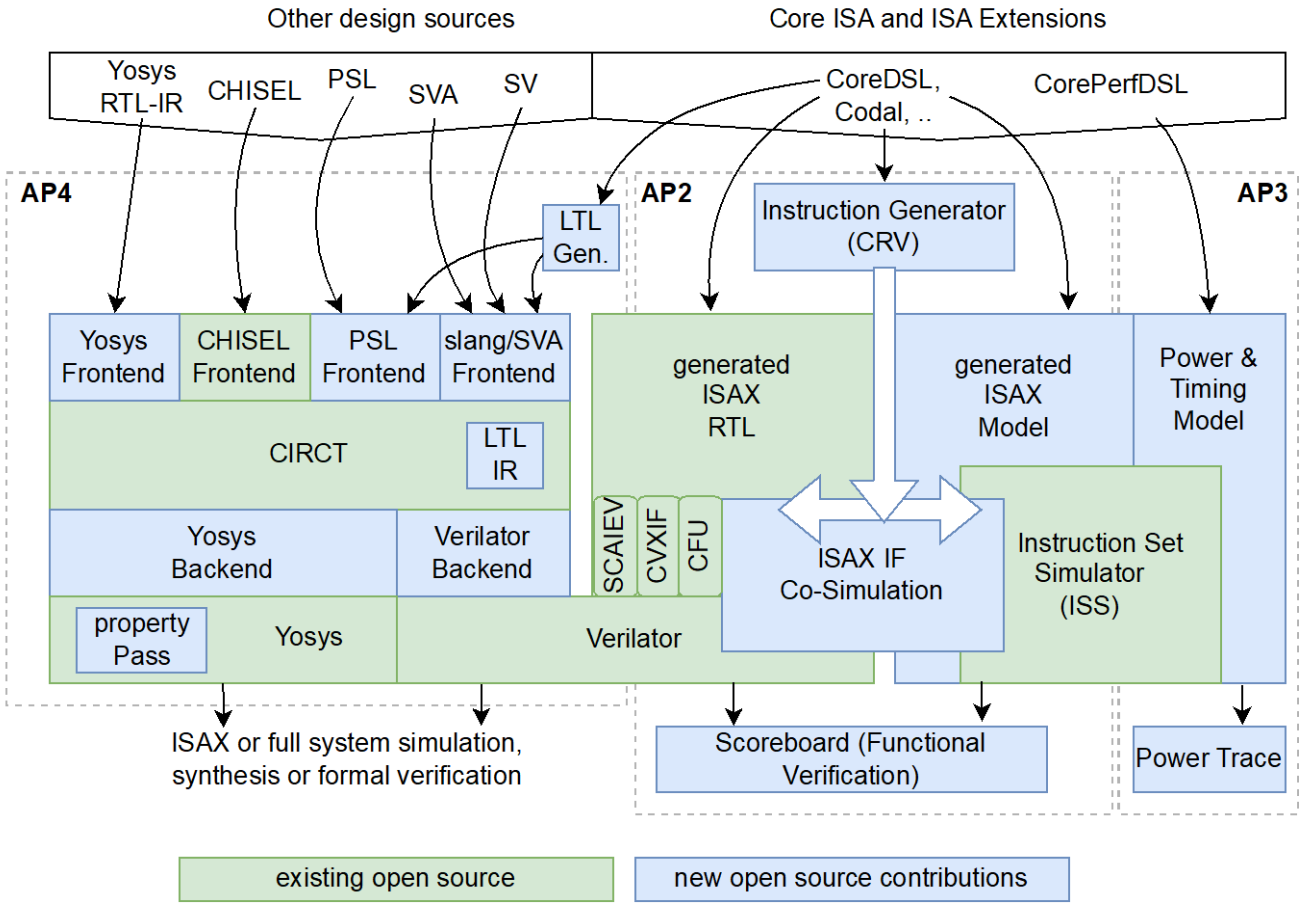
Federal Ministry of Research, Technology and Space

The work packages of EDAI and their interactions



Contributions

- From design capture to simulation/verification
- Open-source tools
  - Extend existing wherever possible
  - Interoperability and integration of tools



DI-OSVISE

Partners

Hochschule München University of Applied Sciences

Coordination

TECHNISCHE UNIVERSITÄT DARMSTADT

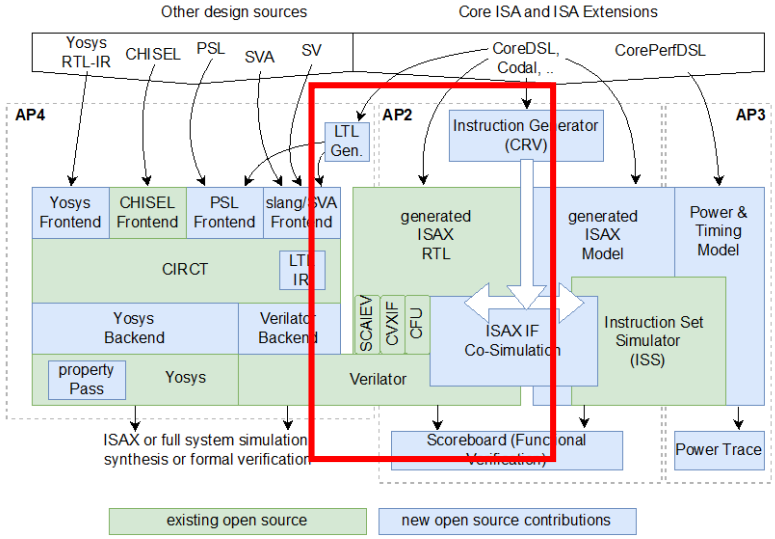
UNIVERSITÄT ZU LÜBECK

TECHNISCHE UNIVERSITÄT WIEN

Subcontractors

Associated

WP2: ISA extension verification with open-source tools



- Verify correctness of ISA extensions
- Combine generated RTL (CoreDSL) and Instruction Set Simulators
- Abstract functionality for standard instructions in ISS
- Constrained random generated instruction stream
- Complete Verilator support for UVM

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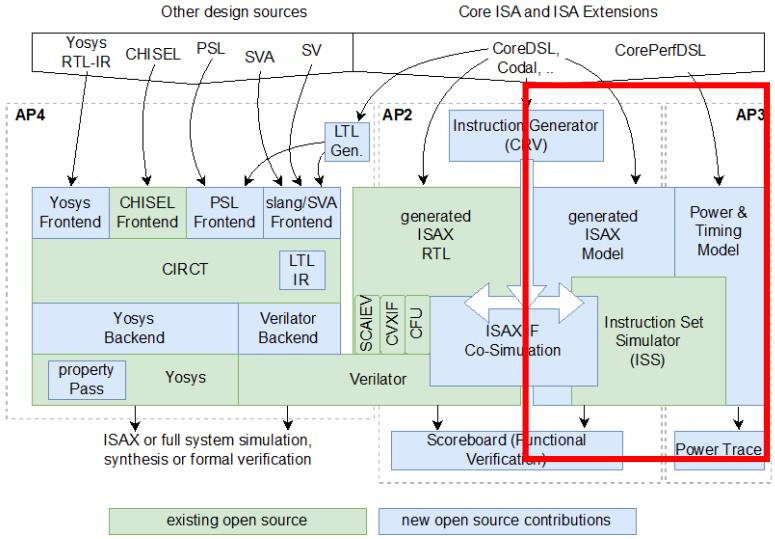
WP3: Verification of non-functional properties



- Validate non-functional properties
- Timing and power behavior
- Extend CorePerfDSL to describe behavior
- Extend ETISS open-source instruction set simulator
- Power estimation on RTL and netlist

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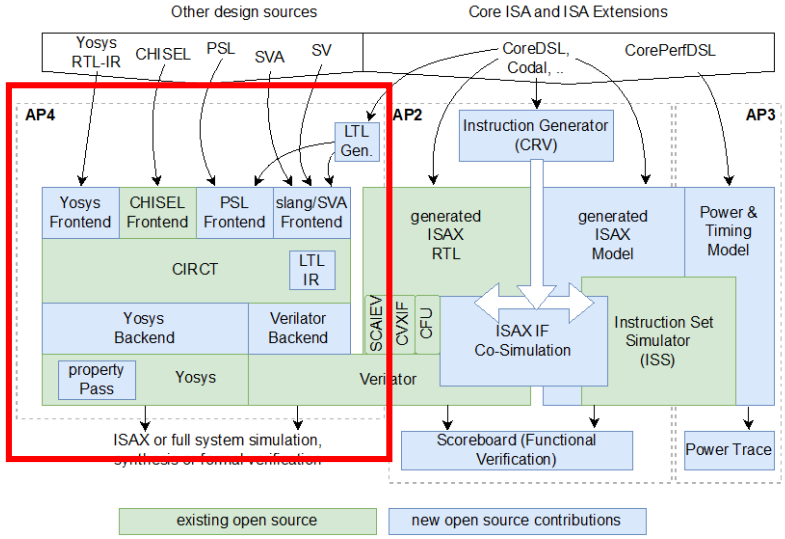
WP4: Better support for formal verification



- CIRCT and Yosys integration (switch between)
- Intermediate representation for LTL (and SVA properties) in CIRCT and Yosys
- CIRCT integration with Verilator
- Seamless flow from Properties to dynamic verification in Verilator and formal verification in Yosys/SBY

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