ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Open-Source From Ideas to Silicon: PULP Teaching & Research with Open IPs, EDAs, PDKs

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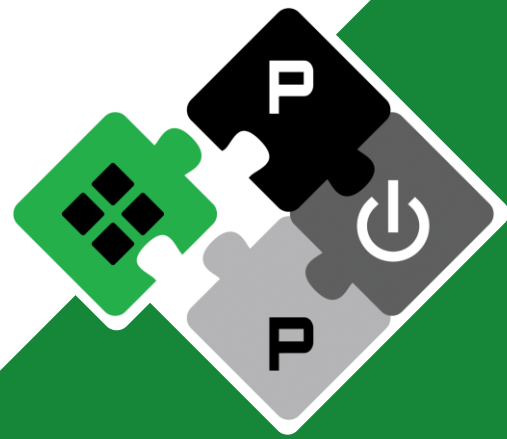
PULP Platform
Open Source Hardware, the way it should be!



pulp-platform.org
@pulp_platform
company/pulp-platform
youtube.com/pulp_platform

Parallel Ultra Low Power (PULP) Platform

- **Lead by Luca Benini involves >100 people**

We have designed over 60 ASICs using open-source HW

All our designs are based on open-source HW published on our GitHub page

- All using a permissive open source license (SolderPad)

`github.com/pulp-platform`

Most of our chips so far used open-designs, closed-tools&PDKs

The «Trinity» of open source HW

Design (RTL/HDL/Physical Design)

- RTL, HDL, Physical Design Scripts

Tools (EDA)

- Synthesis, P&R, Simulation/Verification

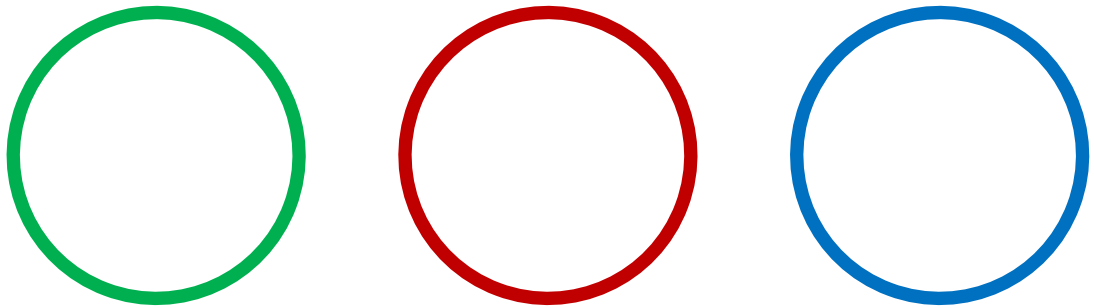
Manufacturing (PDK)

- Design Rules, Parasitics, Device Models

Open **RTL** can use **commercial EDAs** and **closed PDKs**

Open EDAs are mostly agnostic of the process technology

Open PDKs can be used with **commercial EDAs**



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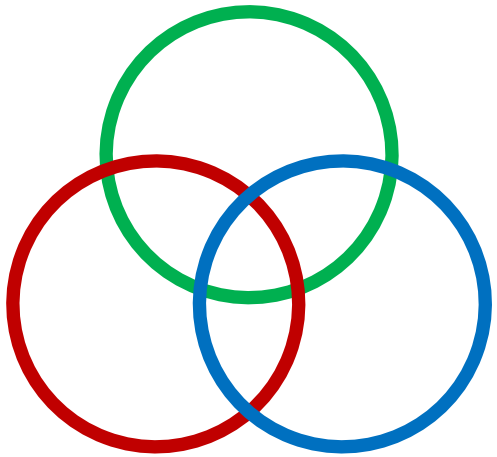

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We need all three aspects together for end-to-end open-source ICs

End-to-end Open-Source Digital IC Design is possible today! But …

Design: from PULP

`github.com/pulp-platform`

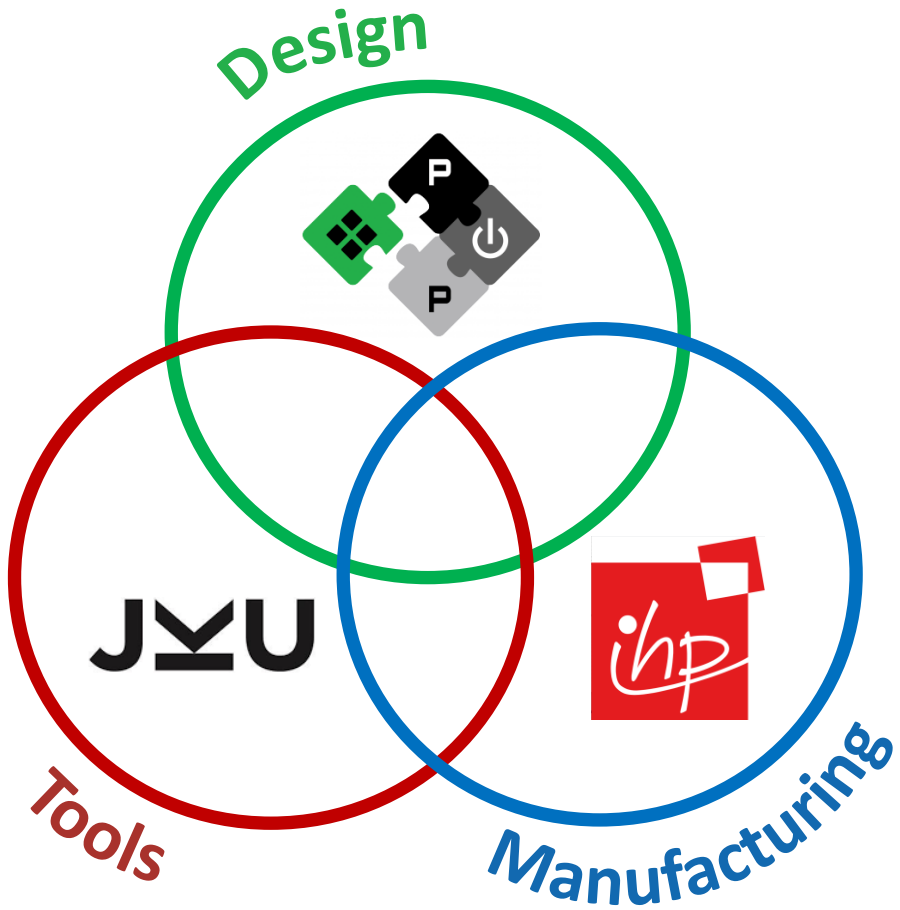
Tools: from Johannes Kepler University (JKU)

Reliable VM with large collection of open-source tools

`github.com/iic-jku/IIC-OSIC-TOOLS`

Manufacturing: IHP130nm

`github.com/IHP-GmbH/IHP-Open-PDK`



… a bit of craftsmanship & design-iterations are needed

- **Custom IHP130 standard cells:** workshop + VLSI5 course @ETHZ

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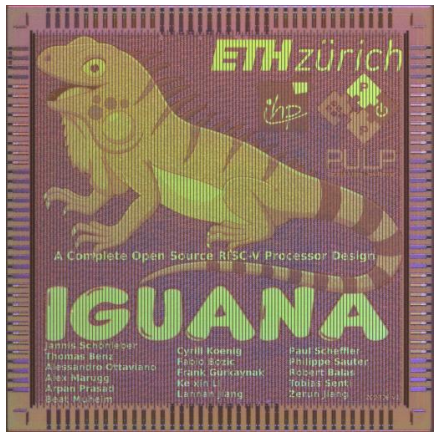
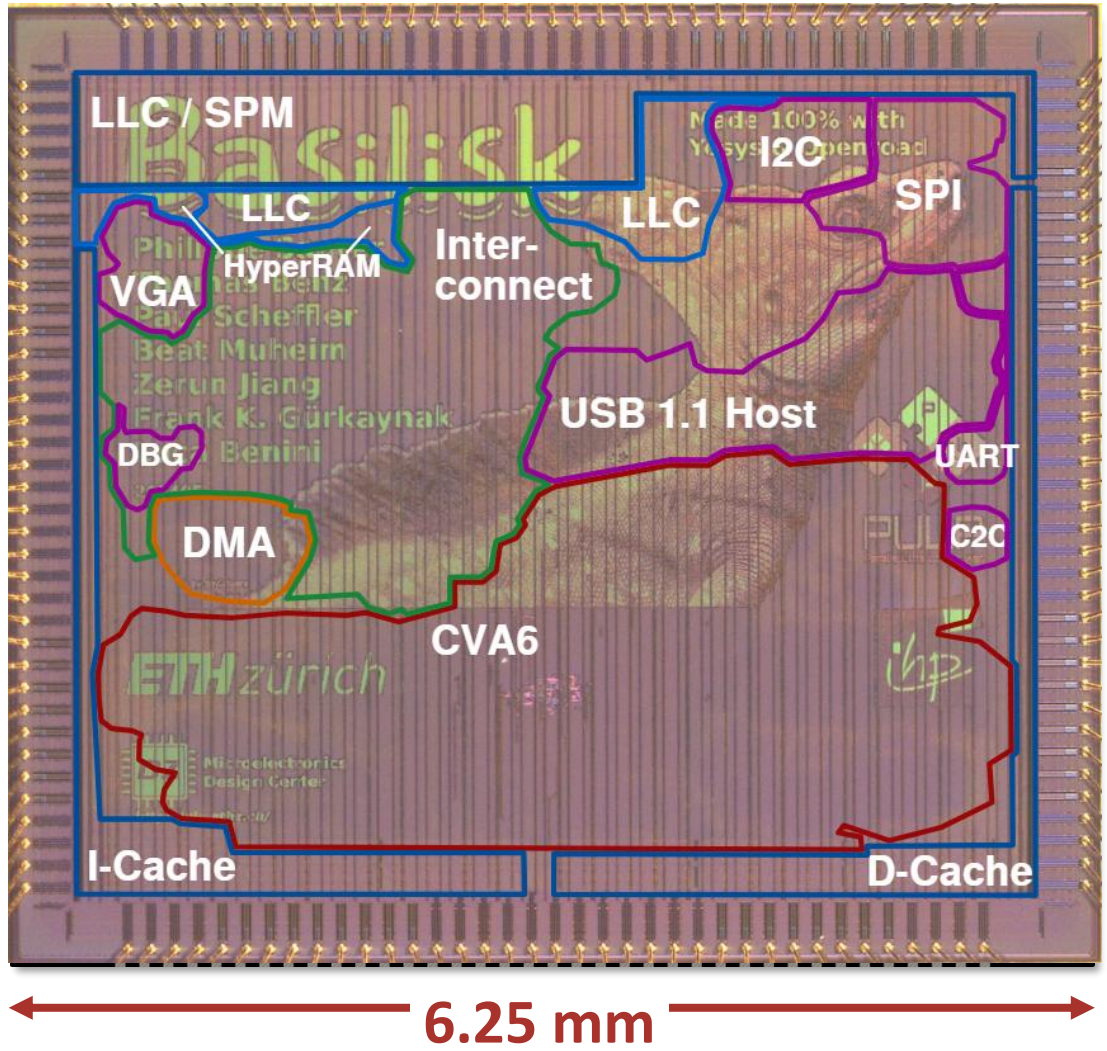
- **Custom IHP130 standard cells:** workshop + VLSI5 course @ETHZ
- **First Attempt in July 2023: Iguana SoC**, open-PDK, proprietary Synth. P&R Verification
- **From industry-grade SV to V understandable for Yosys (yosys-slang) →**

  Iguana can be synthesized Open-Source!
- **Improvement in Synthesis:**
  1. Part-select synthesis with block multiplexer trees (Yosys0.34)
  2. Overhaul to ABC flow for Lazy-Man synthesis
  3. Optimized Library of Arithmetic Units
- **P&R optimizations in OpenROAD**



arxiv.org/html/2406.15107v1

Basilisk: Open **RTL**, Open **EDA**, Open **PDK**

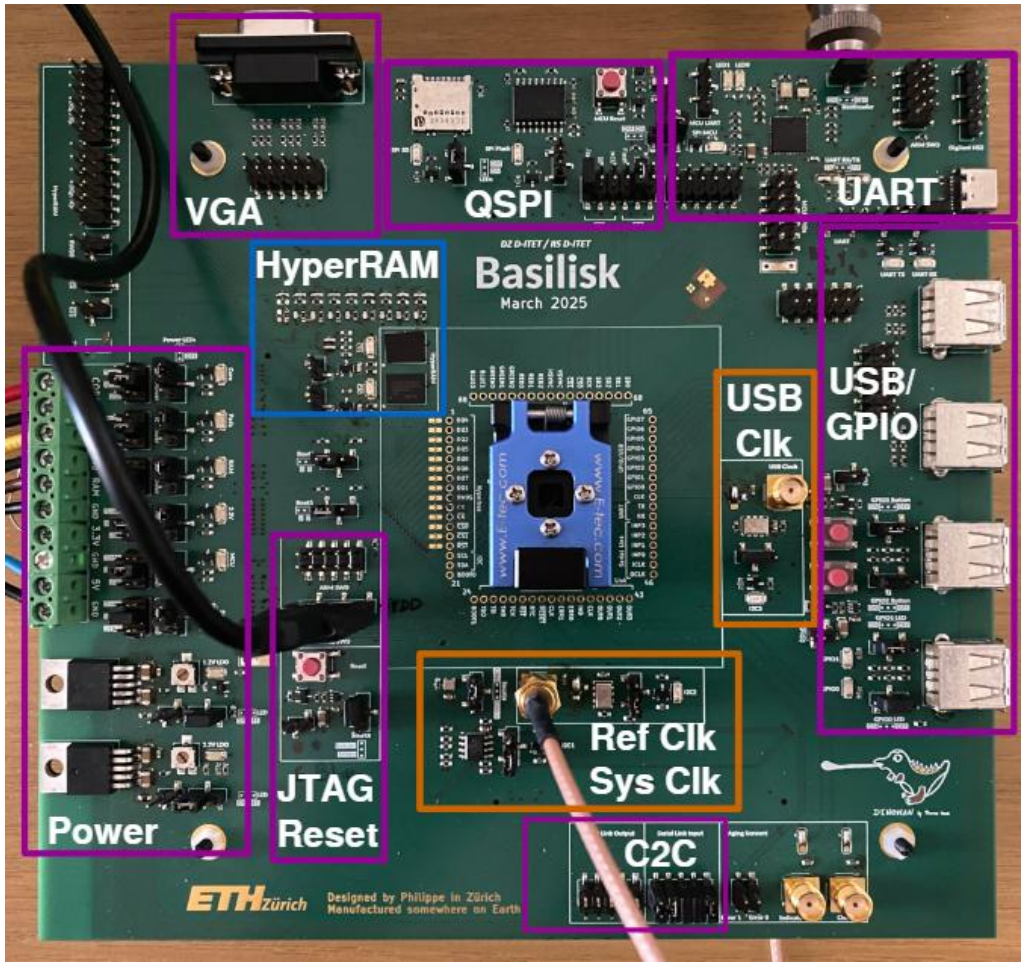


- **Designed in IHP 130nm OpenPDK with Yosys, OpenROAD, KiCAD (board)**
  - SV-to-Verilog chain @ **<2min** runtime
  - Yosys synthesis:
    → **1.1 MGE** (**1.6×**) @ **77 MHz** (**2.3×**)
    → **1.4×** less runtime, **2.4×** less peak RAM
  - OpenROAD P&R tuning:
    → **-12%** die area, **+10%** core utilization

PULP

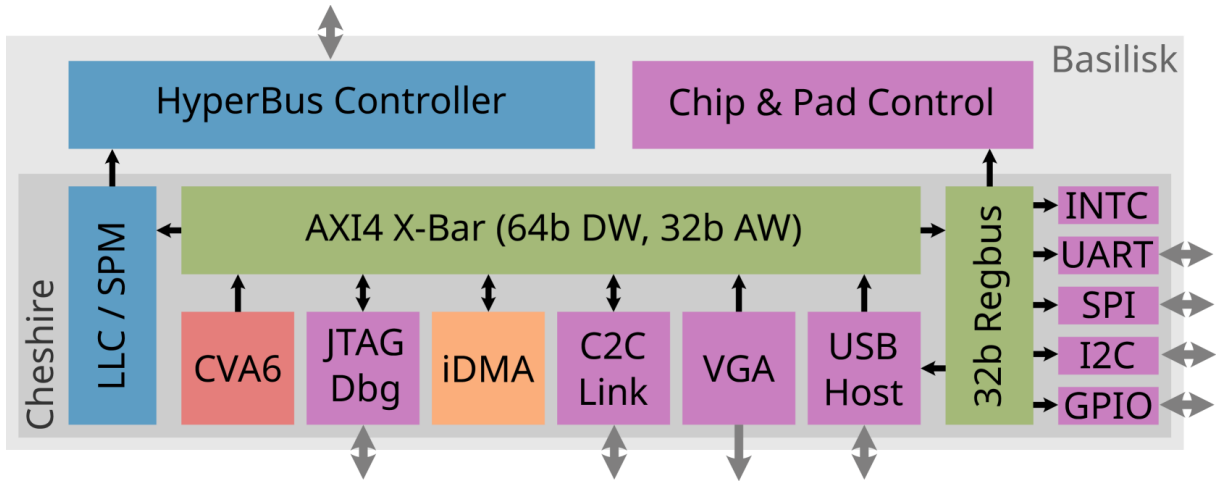
github.com/pulp-platform/cheshire-ihp130-o

A Complete Linux-Capable SoC



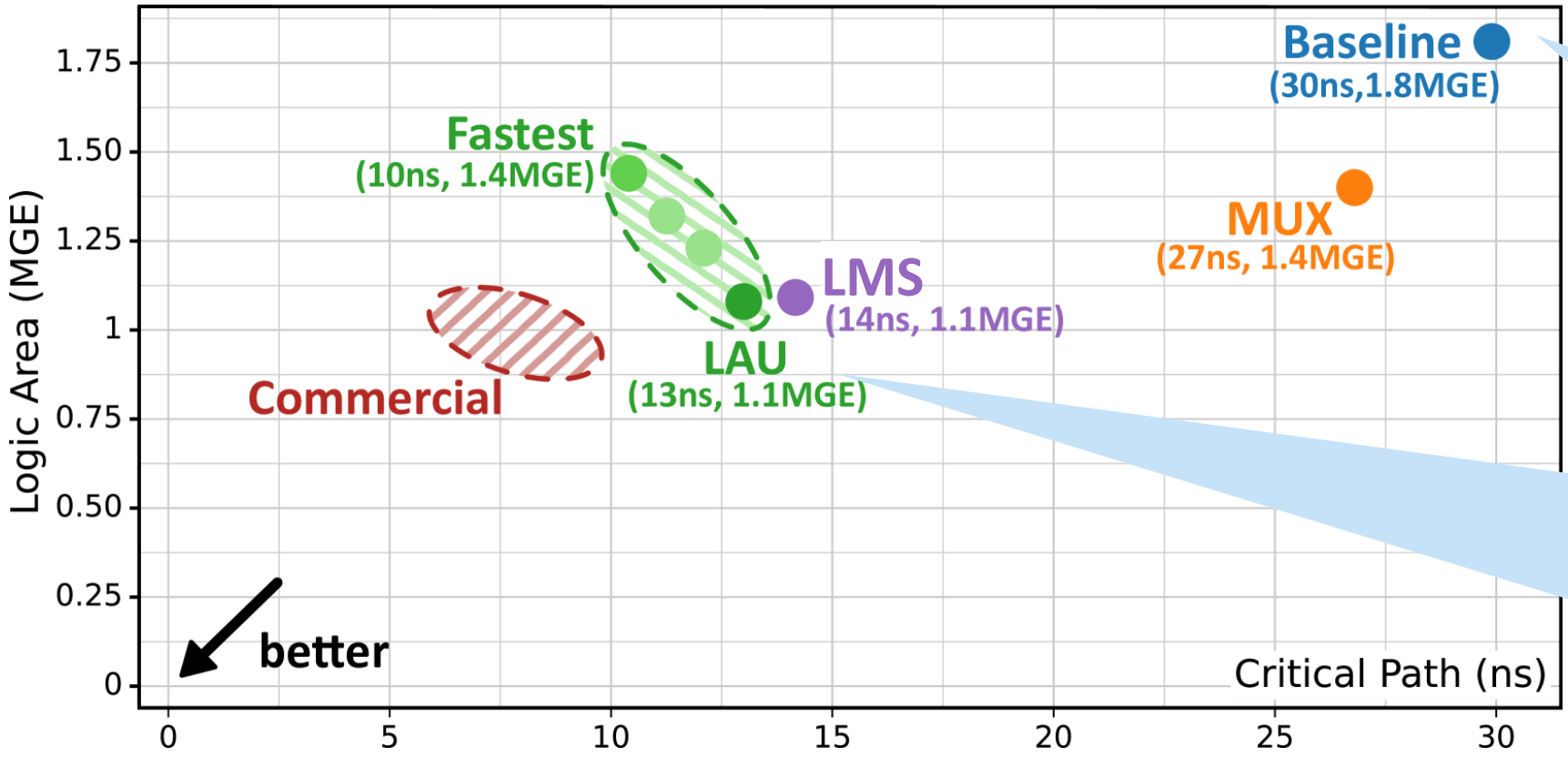
- **64-bit RISC-V core**
- **Rich peripherals:**
  - HyperRAM controller **@154MB/s**
  - C2C AXI-Link **@77MB/s**
- **Autonomous boot from SD-Card**

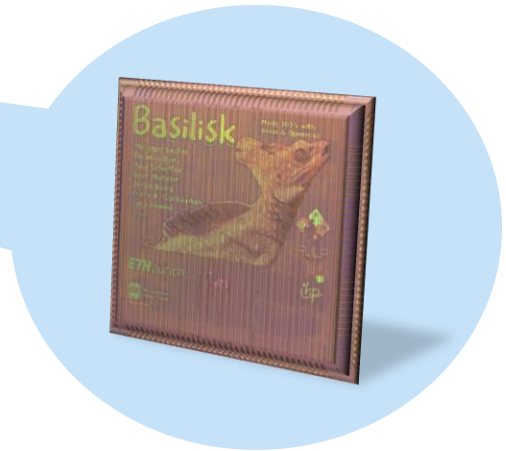
Watch the video



arxiv.org/pdf/2505.10060

Closing the PPA gap to commercial EDA





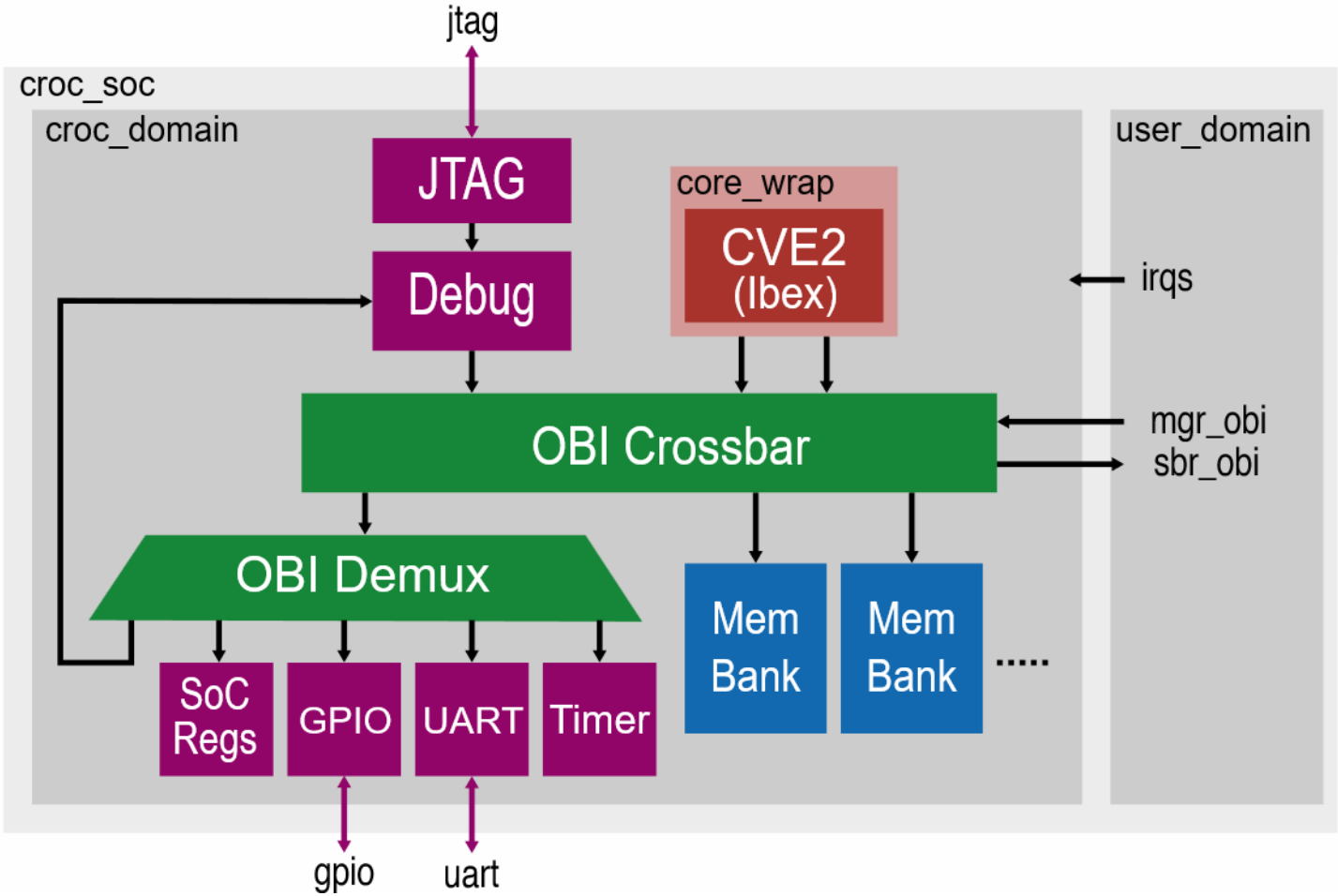
We can get there!

(timing-aware synth., elaboration+optimizations, pre-optimized blocks libs, physically aware synthesis...)

Croc: a simple SoC for education with PULP IPs

- **32-bit RISC-V core**
- **User-Domain ready for custom extensions**
- **Reference design for the VLSI2 lecture @ETHZ**

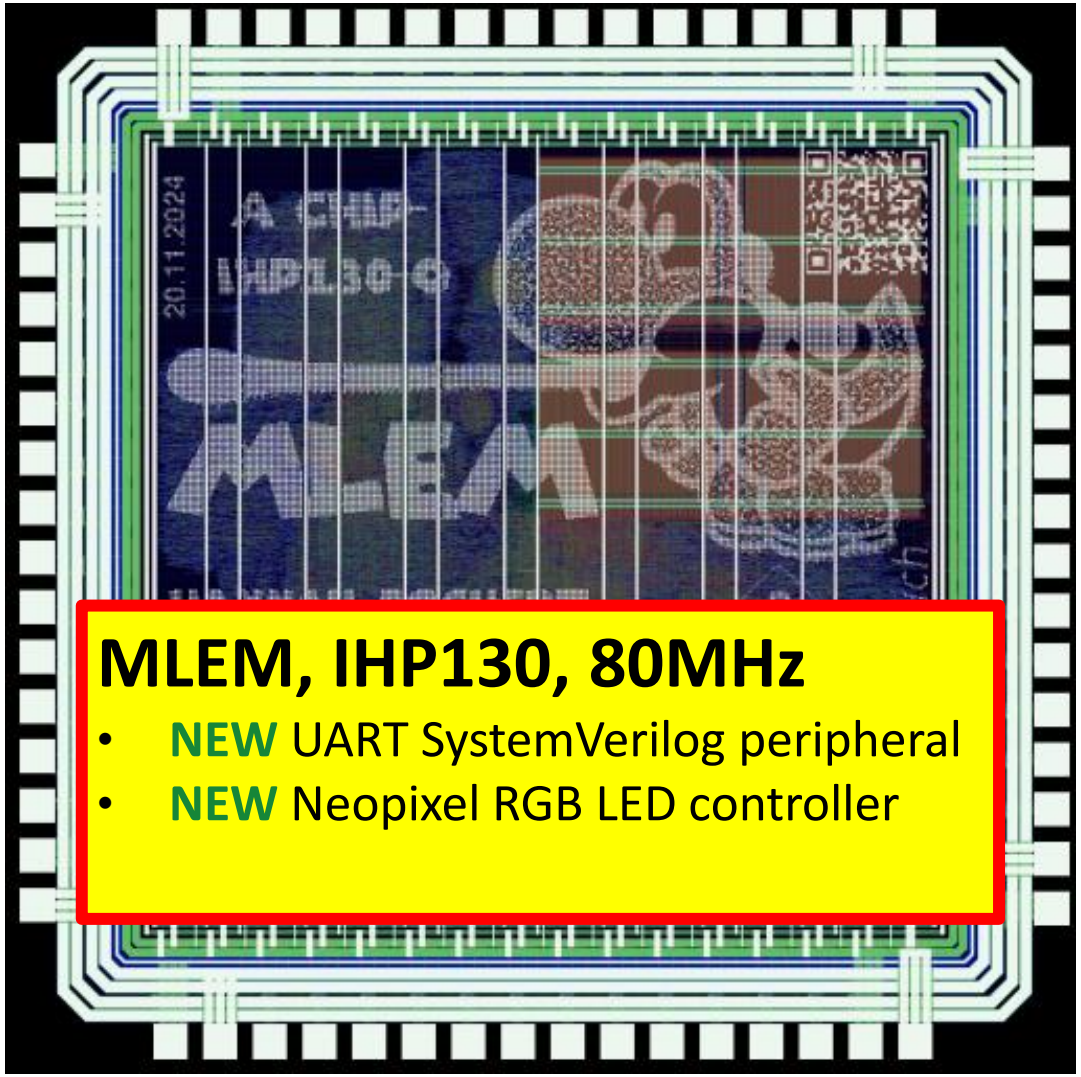
  (72 students enrolled 5 tape-outs planned)



vlsi.ethz.ch

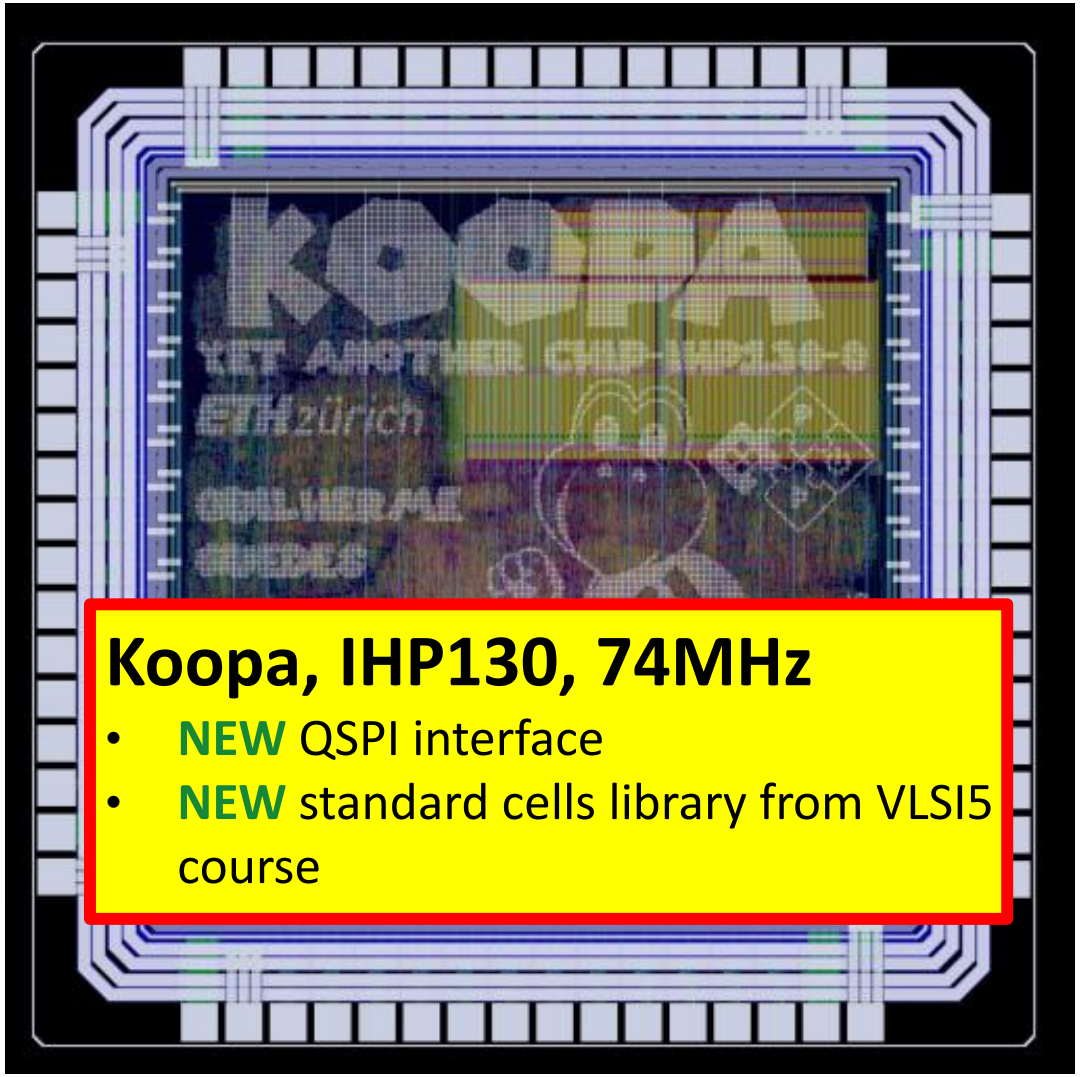
github.com/pulp-platform/croc

Projects on end-to-end open SoCs **Mlem, Koopa, …**



MLEM, IHP130, 80MHz

- **NEW** UART SystemVerilog peripheral
- **NEW** Neopixel RGB LED controller



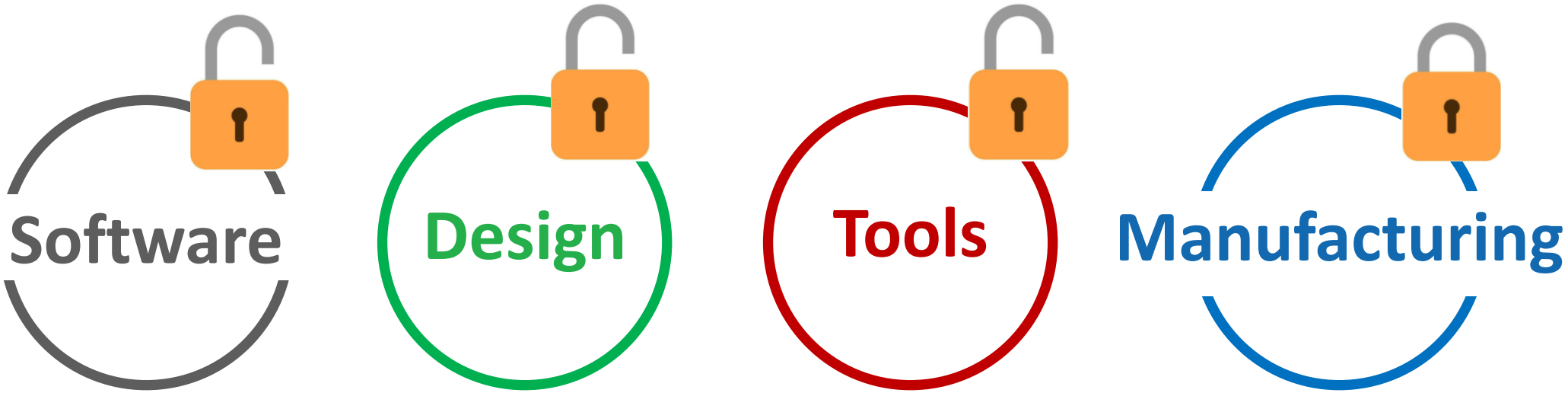
Koopa, IHP130, 74MHz

- **NEW** QSPI interface
- **NEW** standard cells library from VLSI5 course

Open EDAs for more advanced technologies?

Low-Power, IoT, Automotive, ECUs, Wearables = Edge AI

Performance + Energy Efficiency is required!



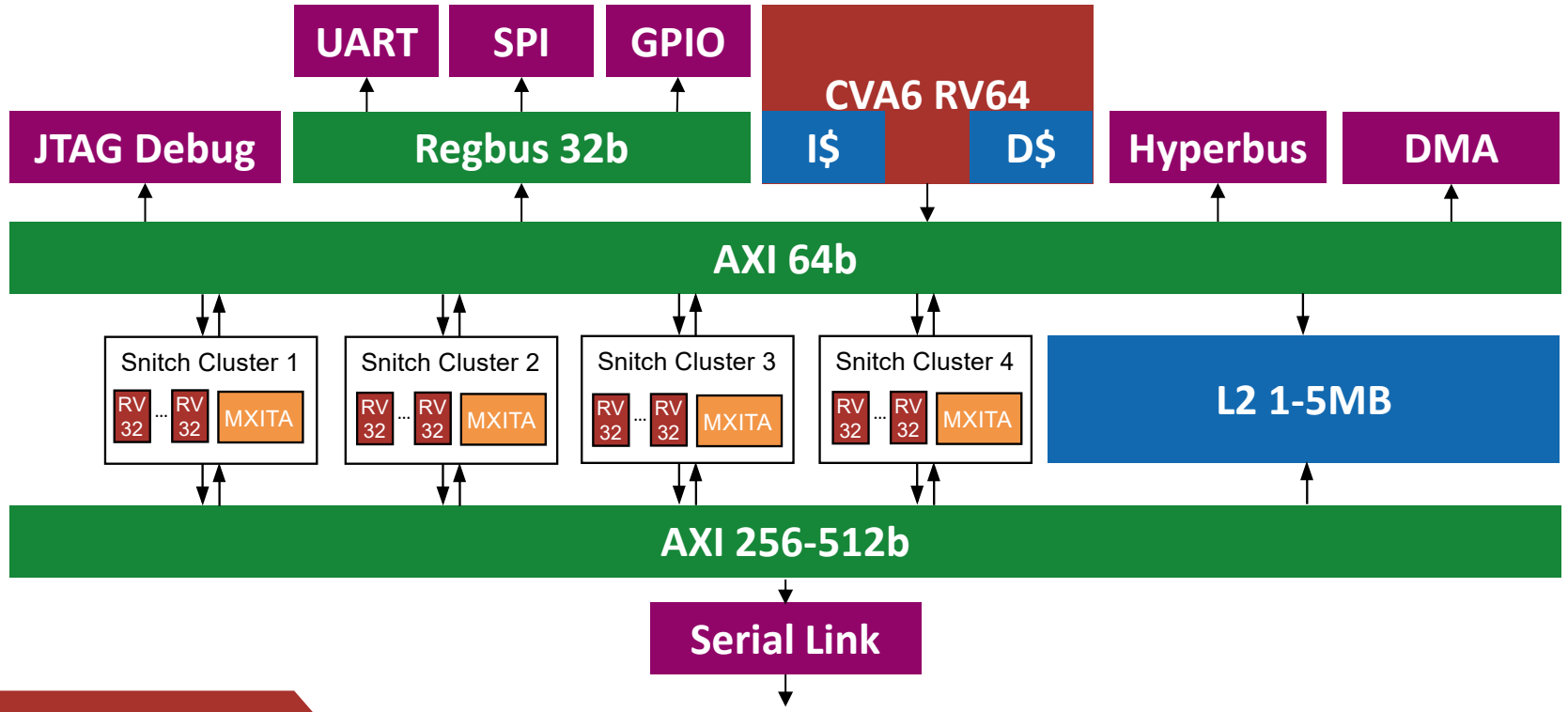
HW-SW Co-Design

HW-SW & Tools Co-Optimization

Get the best from advanced nodes!

SeyrITA: the open-source SoC for Embodied-AI

- **GF22 technology, open-flow with Yosys & OpenROAD**
- **(1 MX-ITA accelerator = 512 FLOP/s) x 2/4 clusters = 1/2 TFLOP/s @500MHz**
- **Target applications:** transformer models (DeiT, MobileBERT, …), microscaling quantization

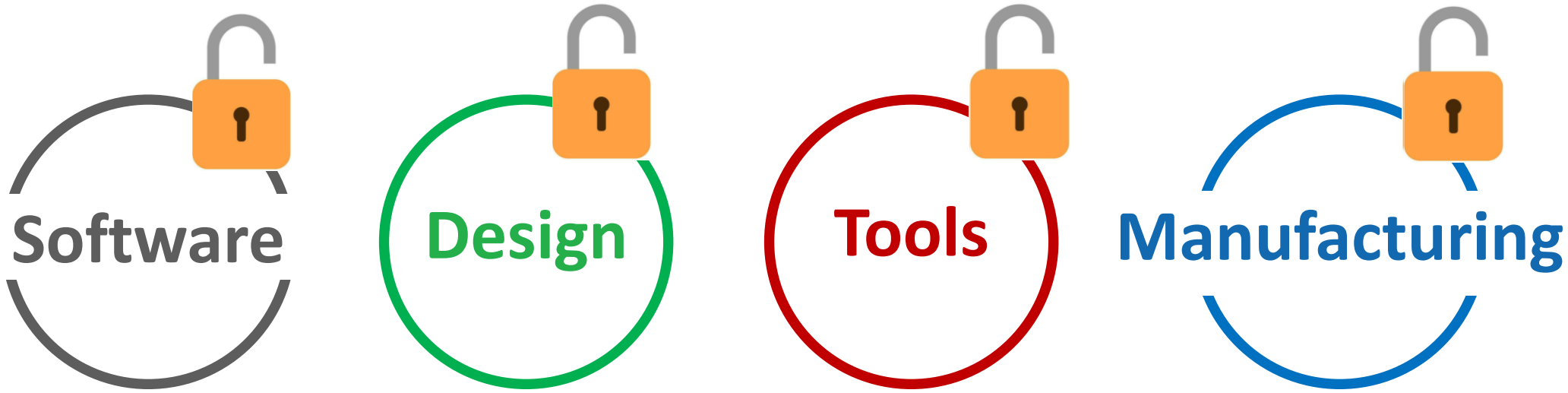


Tape-out by end 2025

Next step to make end-to-end open-source HW success

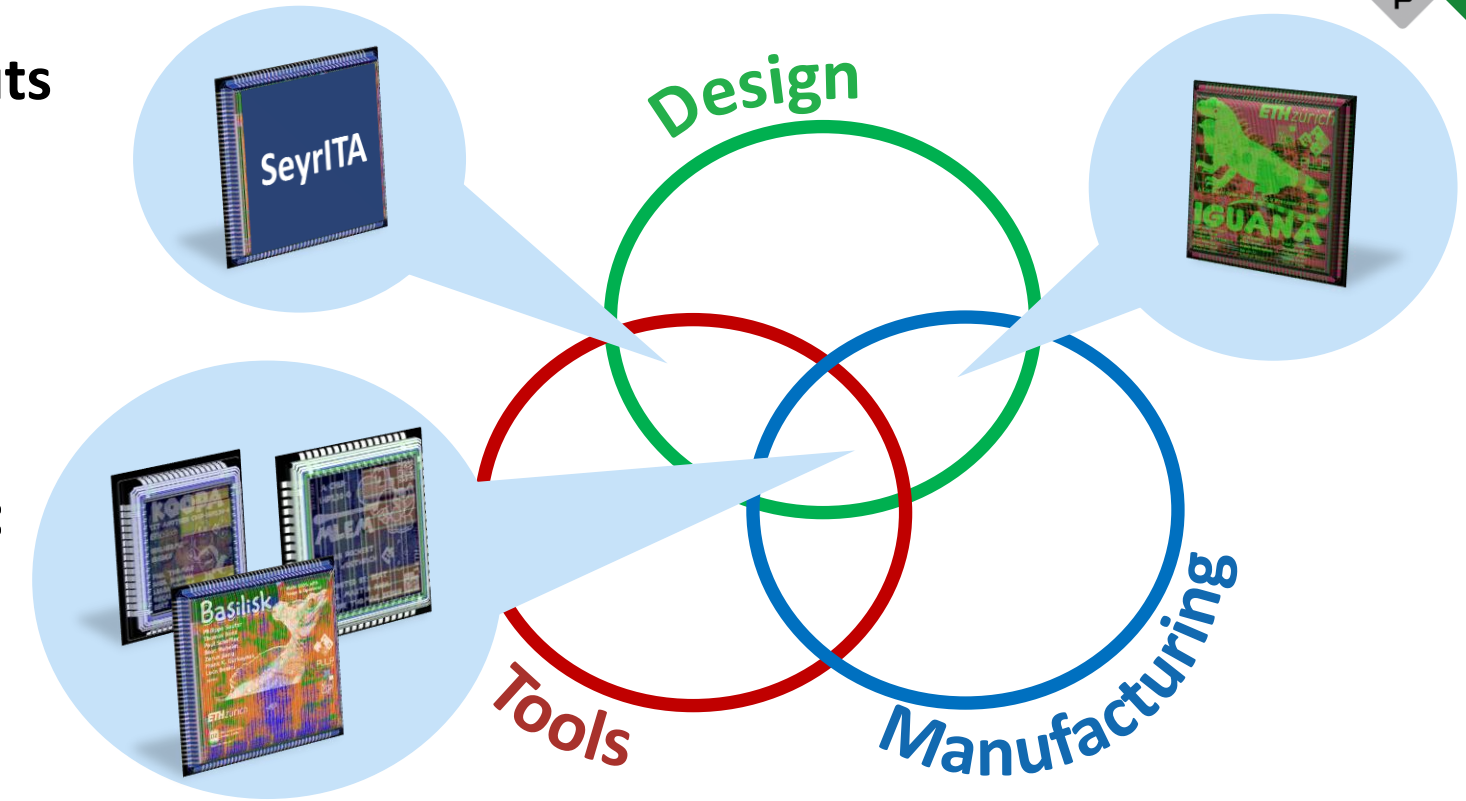
Get access to more open PDKs

- Something in the 65nm – 28nm range would be a game changer
- Discussion on going
- But it is a long game…



Freedom on **Tools** & **Process** According to **Design** Goals

- **4 open-EDAs & PDKs tape-outs with different design choices**
  (+many more coming)
- **Active contribution to open-EDA community**
- **Successful educational goals:**
  - Open-EDA based courses
  - Open-source tape-out student projects



Open-Source Design&Flow for Reproducible SoA Innovations!