



# SW Toolchain for RISC-V Vector Extensions

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# **Acknowledgements**





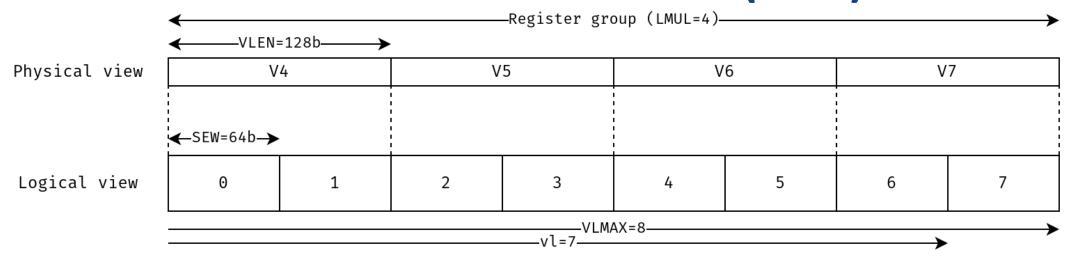
Pilot using Independent Local & Open Technologies

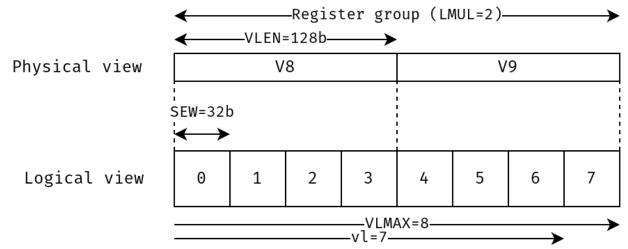






#### RISC-V Vector Extension (RVV)





vtype = <SEW, LMUL, policy>



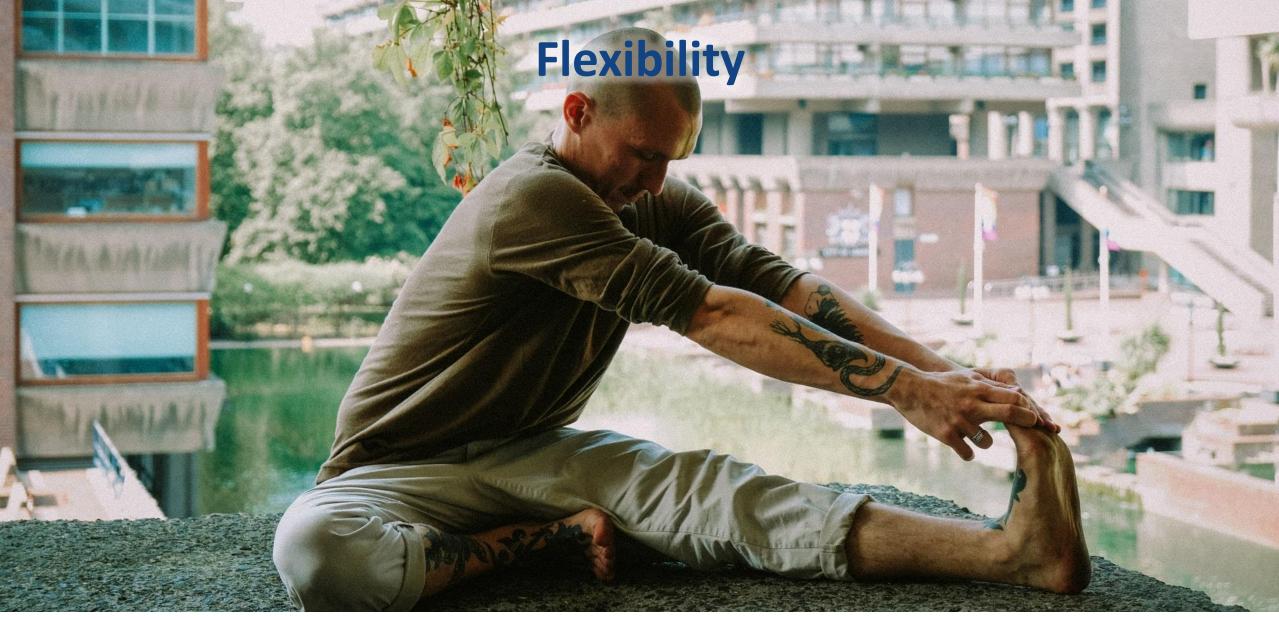




Photo by Benn McGuinness on Unsplash

# Challenges in code generation



#### **RVV Architectural State and Instructions**

```
%dc = fadd <2 x double> %da, %db

%sc = fadd <4 x float> %sa, %sb

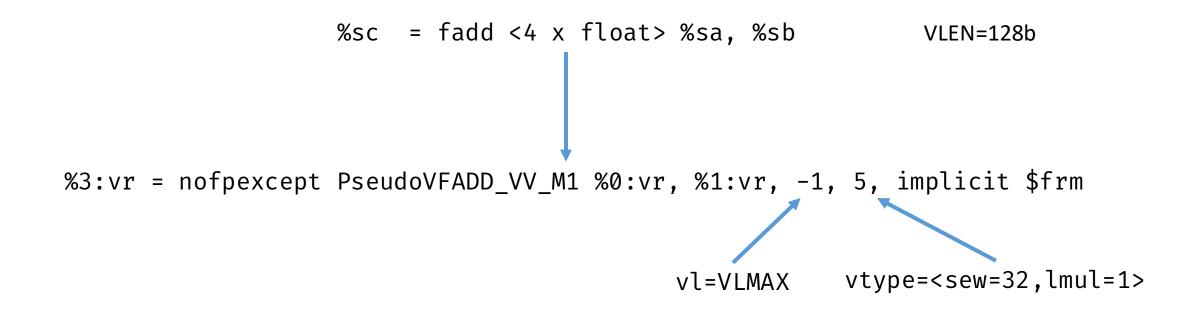
%sc2 = fadd <8 x float> %sa2, %sb2

%sch = fadd <2 x float> %sah, %sbh

∨fadd.vv
```



# **Current approach**



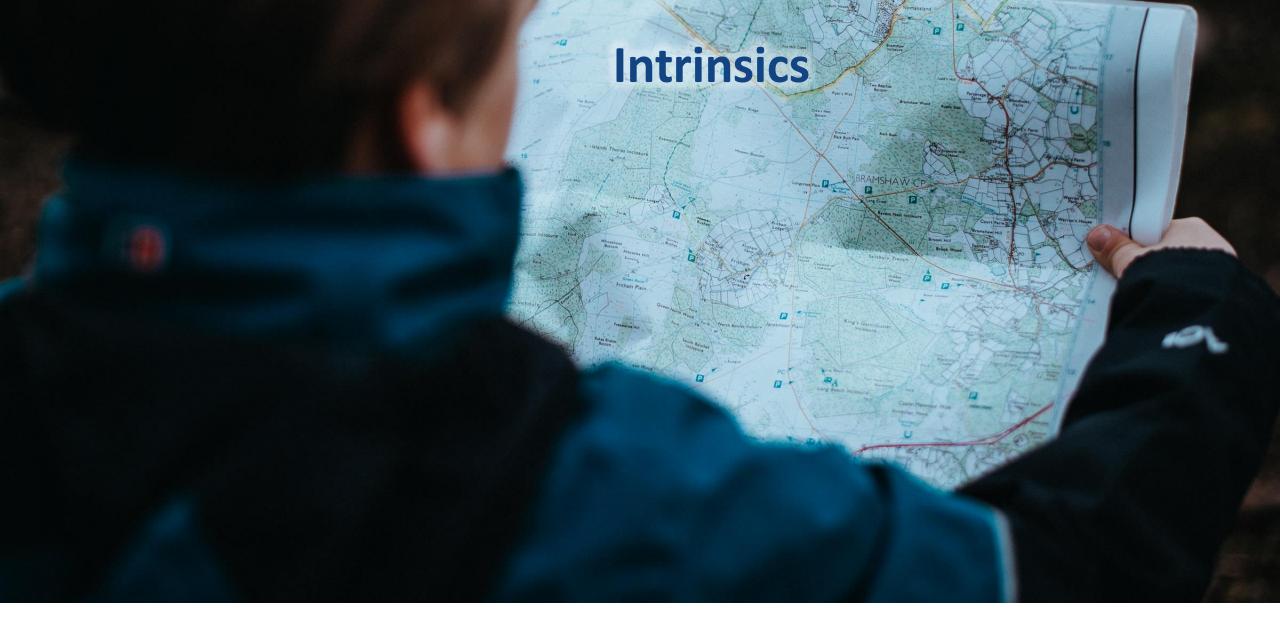


# What about setting the context



# Challenges that impact the user of RVV







# Vectorization







# **LLVM** and predication





Image by **AxxLC** from **Pixabay** 

#### **Vector Predication**

Scalar operation (add two double precision values)

```
%sc = fadd double %sa, %sb
```

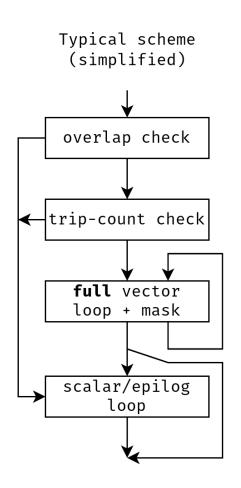
Element-wise extension to whole vectors (add two double precision vector values)

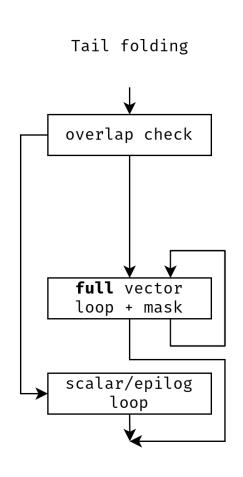
```
%vc = fadd <8 x double> %va, %vb
%vla.c = fadd <vscale x 1 x double> %vla.a, %vla.b
```

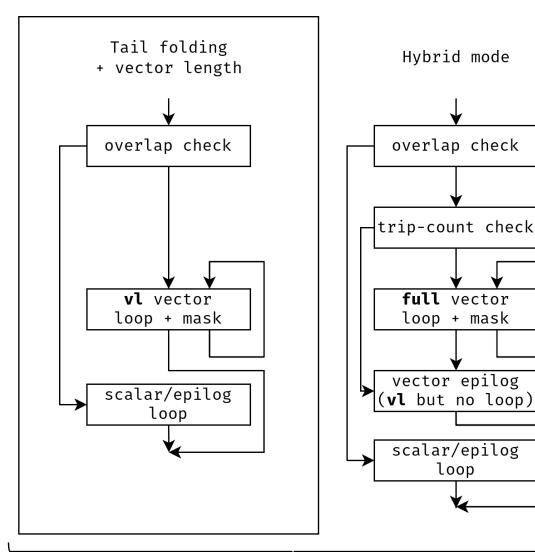
Vector Predication allows us to specify mask and vector length operands



# **Loop Vectorisation at EPI**









#### **Example DAXPY kernel**

ret

You can try it at

https://repo.hca.bsc.es/epic/z/iBdt4p

```
Tail folding
                                             + vector length
daxpy:
       blez
               a2, .LBB0 3
       li
               a3, 0
                                             overlap check
       slli
             a2, a2, 32
       srli
             a6, a2, 32
.LBB0 2:
       slli a4, a3, 3
       add a5, a0, a4
       sub a2, a6, a3
       vsetvli a2, a2, e64, m1, ta, mu
                                               vl vector
       vle64.v v8, (a5)
                                              loop + mask
       add a4, a4, a1
       vle64.v v9, (a4)
       vfmacc.vf v9, fa0, v8
                                              scalar/epilog
       add a3, a3, a2
                                                 loop
       vse64.v v9, (a4)
       bne a3, a6, .LBB0 2
.LBB0 3:
```







# Thank you!

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