Automatic RISC-V Processor Synthesis using Speculative Pipelining

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The Internet of Things raises many challenges for computer designers: devices are expected to handle larger computational workloads (e.g., AI-based) while enforcing stringent cost and energy efficiency. One way to answer those expectations is to use specialized Instruction Set Processors. The RISC-V initiative enables third parties to freely implement their own customized microarchitecture, allowing them to deviate from a standardized ISA. However, the design of these complex hardware pieces is costly and very error-prone. In this work, we propose to bridge part of the gap between Instruction Set Processor design flows and High-Level Synthesis tools. More specifically, we aim at taking advantage of speculative loop pipelining to automatically synthesize in-order pipelined micro-architectures directly from RISC-V Instruction Set Simulators written in C.