Alternative languages for safe and secure RISC-V programming

Fabien Chouteau

Embedded Software Engineer at AdaCore

Twitter : @DesChips

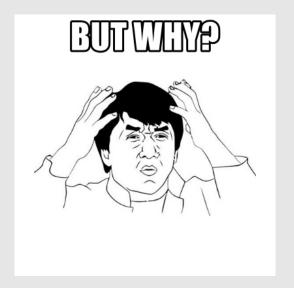
GitHub : Fabien-Chouteau

Hackaday.io: Fabien.C

What do I mean by "alternative"?

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Functional Safety

Specifications

```
type Servo_Angle is new Float range -90.0 .. 90.0
-- Servo rotation angle in degree

procedure Set_Angle (Angle : Servo_Angle);
-- Set desired angle for the servo motor
```



Contracts

```
type Stack is tagged private;
function Empty (S : Stack) return Boolean;
function Full (S : Stack) return Boolean;
procedure Push (S : in out Stack; Val : Integer)
 with Pre => not S.Full,
      Post => not S.Empty;
procedure Pop (S : in out Stack; Val : out Integer)
 with Pre => not S.Empty,
      Post => not S.Full;
```

Checks

- At run-time
 - Checks inserted in the code
 - For debug or testing
- At Compile time
 - Compiler
 - Static analyzer
 - Formal verification (SPARK)



```
-- High level view of the Sense field
type Pin_Sense is
  (Disabled,
   High,
  Low)
  with Size => 2;
    Hardware representation of the Sense field
for Pin_Sense use
  (Disabled \Rightarrow 0,
   High \Rightarrow 2,
   Low \Rightarrow 3);
```

```
-- High level view of the register
type IO_Register is record
  Reserved_A : UInt4;
  SENSE : Pin Sense;
  Reserved B : UInt2;
end record with Size => 32;
   Hardware representation of the register
for IO_Register use record
  Reserved_A at 0 range 0 .. 3;
  SENSE at 0 range 4 .. 5;
  Reserved_B at 0 range 6 .. 7;
end record;
```

```
#define SENSE_MASK
#define SENSE_POS
                     (4)
#define SENSE_DISABLED (0)
#define SENSE_HIGH (2)
#define SENSE_LOW (3)
uint8_t *register = 0x80000100;
// Clear Sense field
*register &= ~SENSE_MASK;
// Set sense value
*register |= SENSE_DISABLED << SENSE_POS;
```

```
Register : IO_Register
with Address => 16#8000_0100#;
```

```
Register.SENSE := Disabled;
```

SVD -> Ada

```
<field>
  <name>SENSE</name>
  <description>Pin sensing mechanism.</description>
  <lsb>16</lsb> <msb>17</msb>
  <enumeratedValues>
    <enumeratedValue>
      <name>Disabled</name>
      <description>Disabled.</description>
      <value>0x00</value>
    </enumeratedValue>
 [...]
```

github.com/AdaCore/svd2ada



Interfacing with C / Assembly

```
with Interfaces.C; use Interfaces.C;
[...]
function My_C_Function (A : int) return int
  with Pre \Rightarrow A /= 0;
pragma Import (C, My_C_Function, "my_c_function");
function My_Ada_Function (A : int) return int;
pragma Export (C, My_Ada_Function, "my_ada_function");
```

Getting started on RISC-V

Hardware



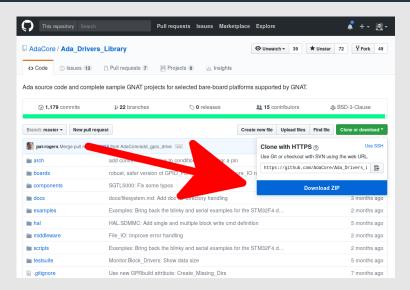


Download and install the tools: adacore.com/community





Download Ada Drivers Library





MAKE Ada

- Embedded programming competition
- Open to everyone
- \$8000 in prizes

Keep the door open

What as already been done

- Open specs and documentation
- RISC-V support in open-source tools:
 - Compilers (GCC, LLVM)
 - Debuggers (Gdb, openocd)
 - Simulators (QEMU)

Challenges

- Complexity of extension combinations
 RV(32|64|128) I M A C B [F|D|Q] ...
- Deviation from the standard
- Custom/proprietary extensions



Hardware description

Do we need to go beyond SVD?

- Registers √
- Interrupts √
- CPU specs ?
- RAM and ROM banks?
- Modular representation ?
- A mix between Device Tree and SVD?
- Tools that generate SVD from custom design ?



Resources

- learn.adacore.com : interactive learning website
- Competition: makewithada.org
- Twitter: @AdaProgrammers
- Reddit : r/ada

