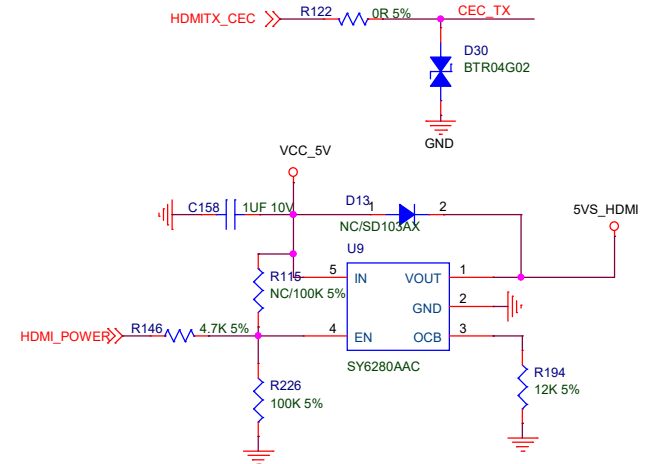
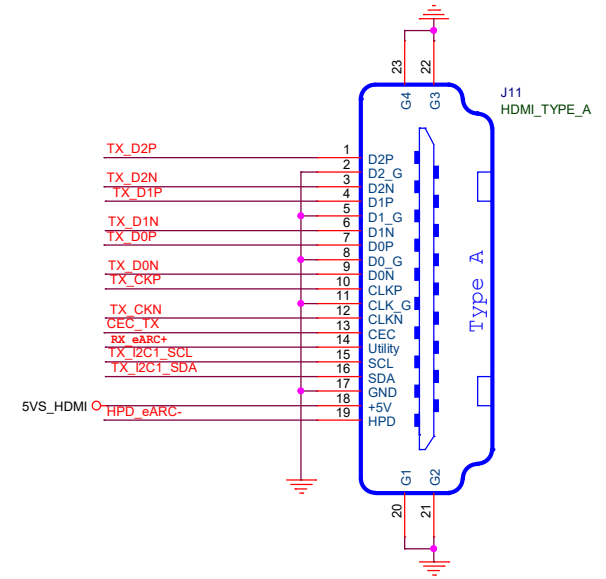
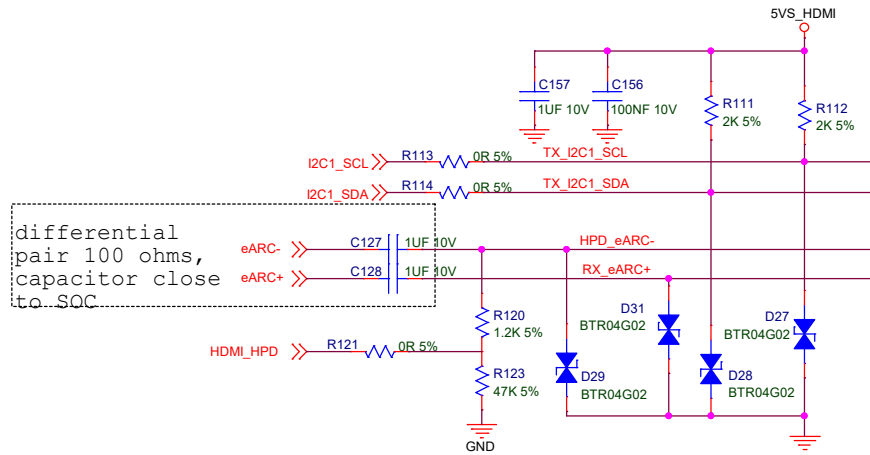
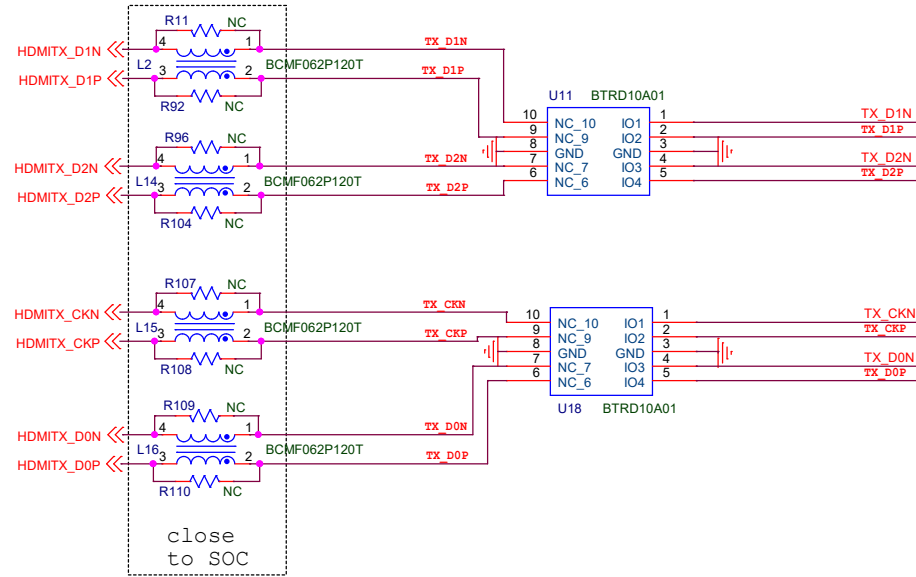
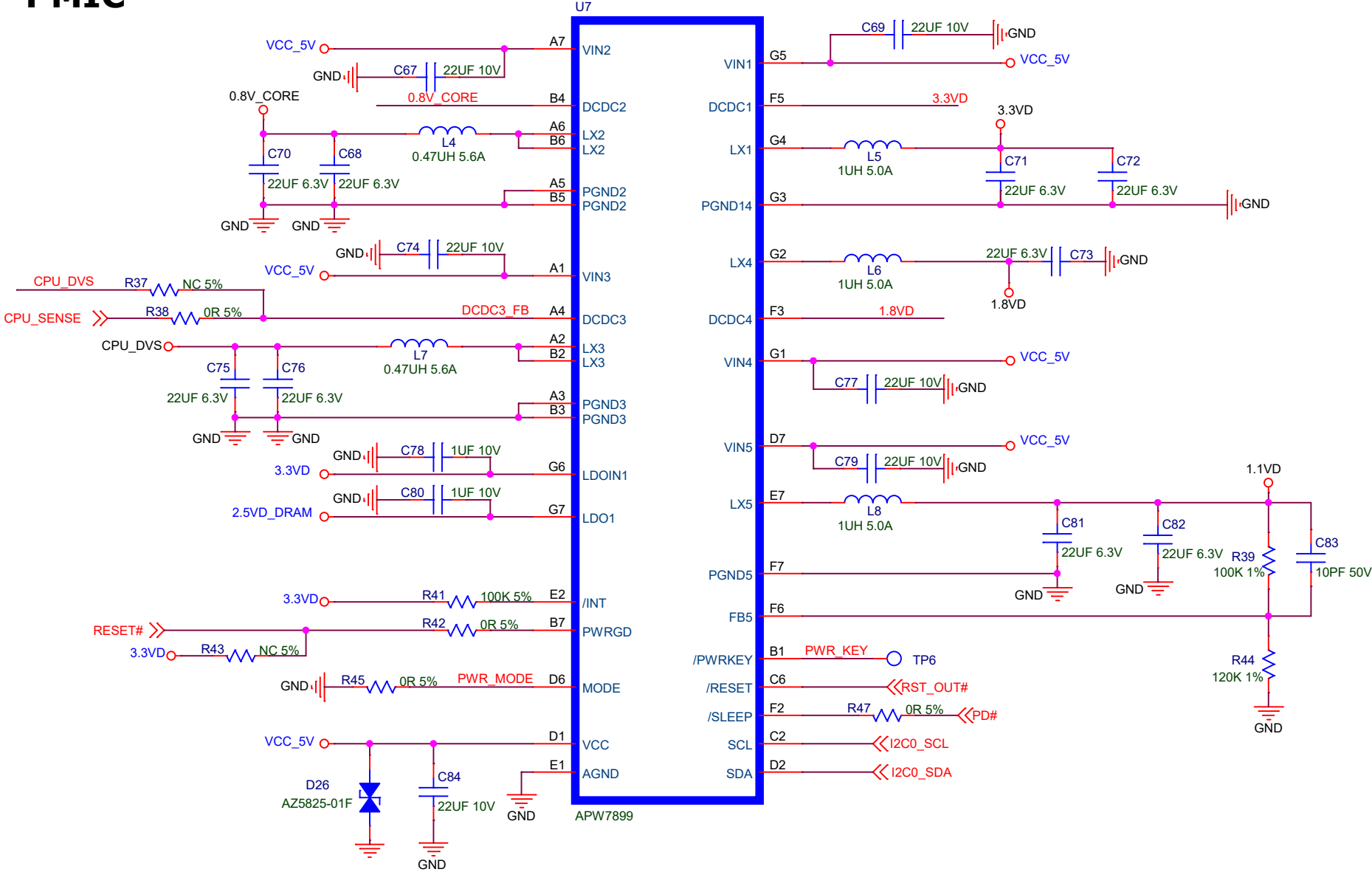


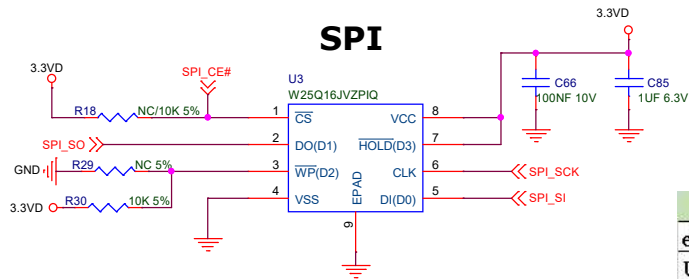
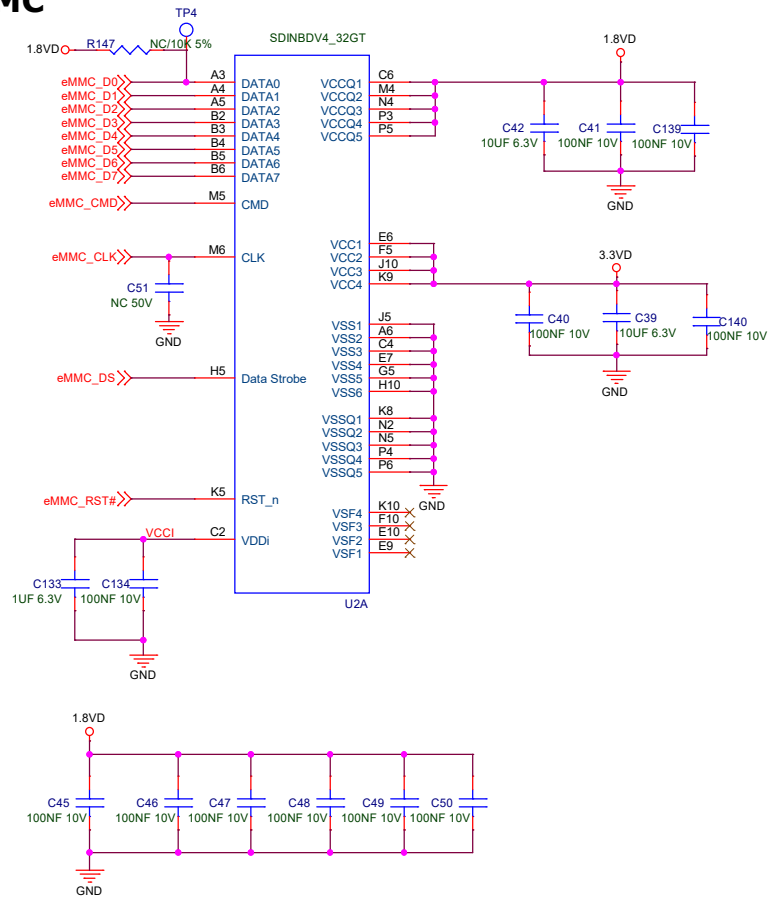
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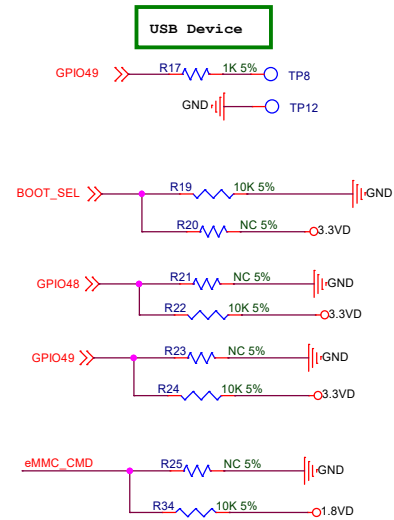
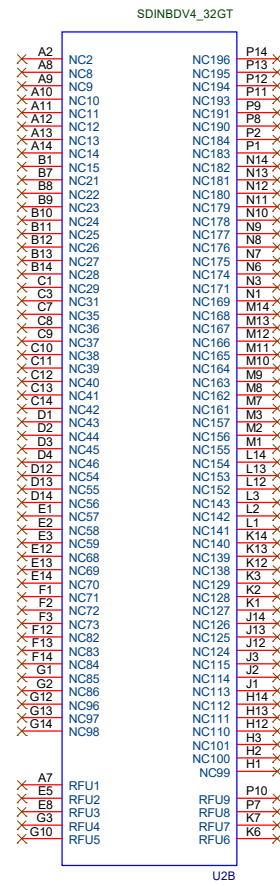
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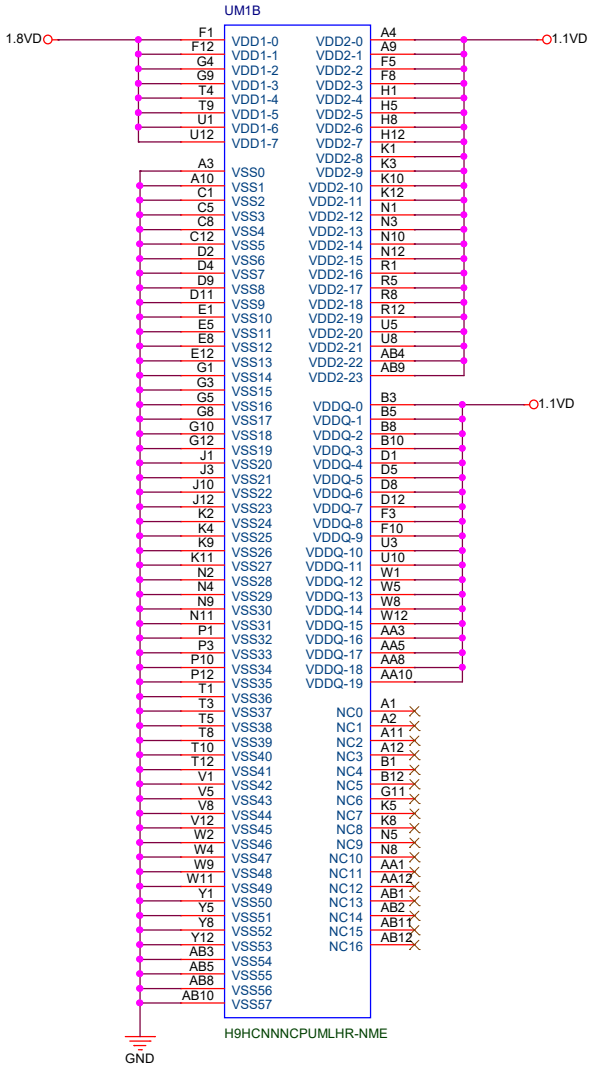
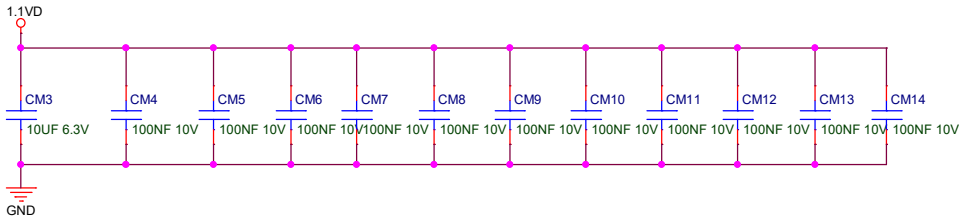
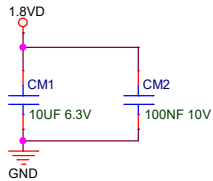
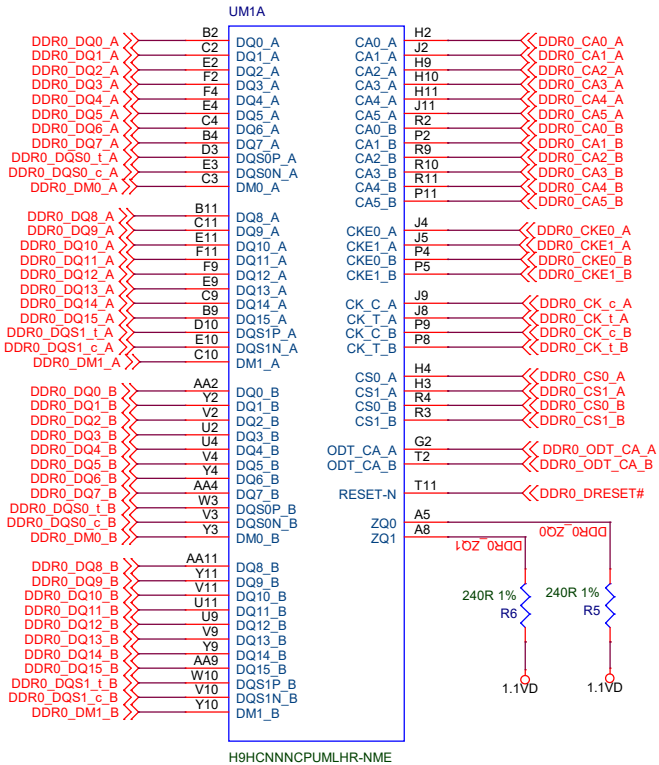
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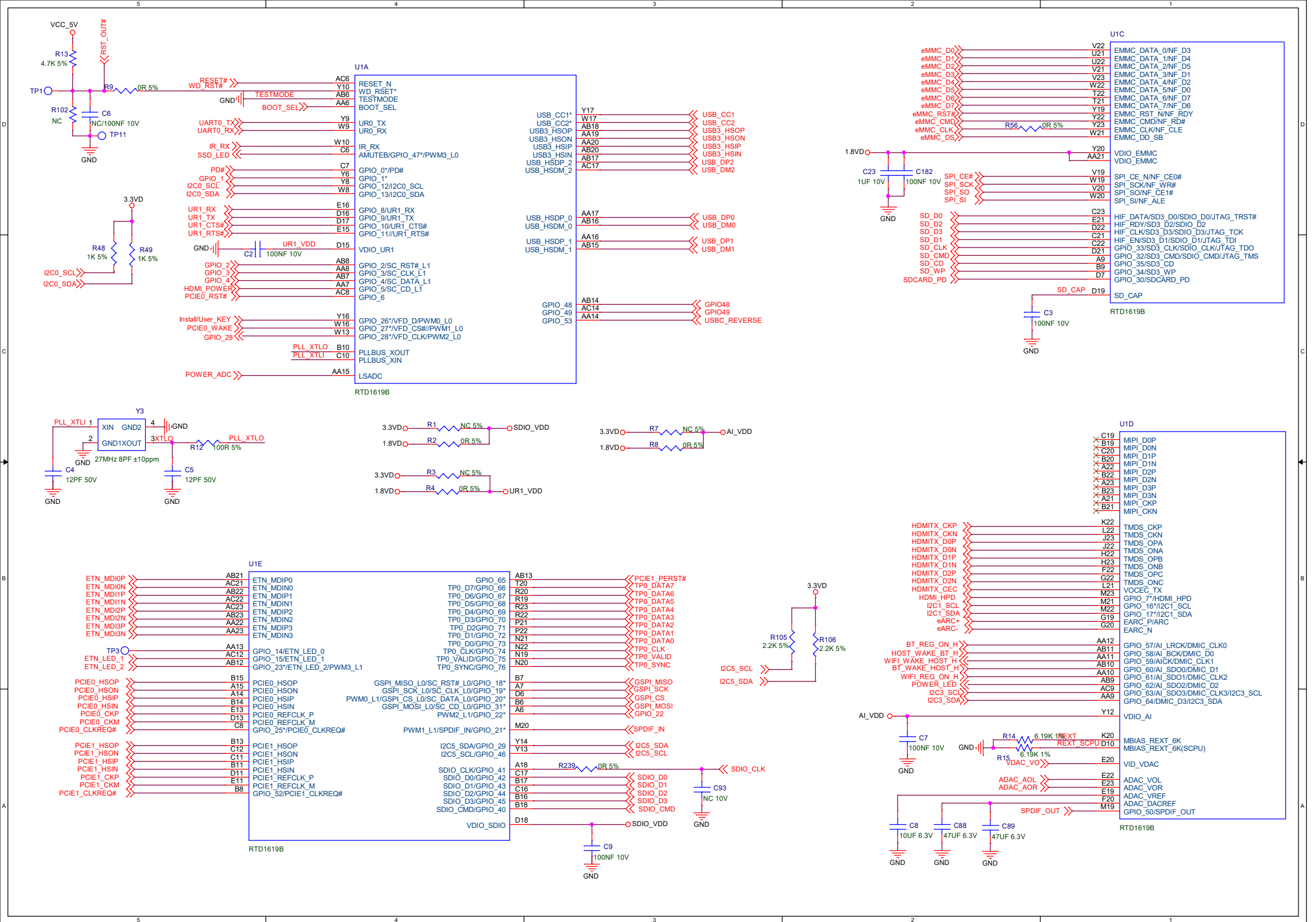


	Boot_sel	GPIO_48	GPIO_49	eMMC_CMD
eMMC	0	1	1	X
USB Device	0	1	0	X
NOR	0	0	1	0
NAND Parallel	0	0	1	1



LPDDR4





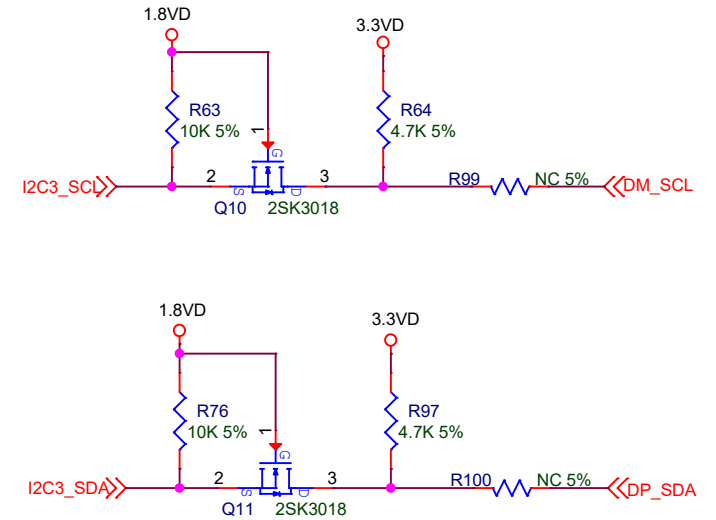
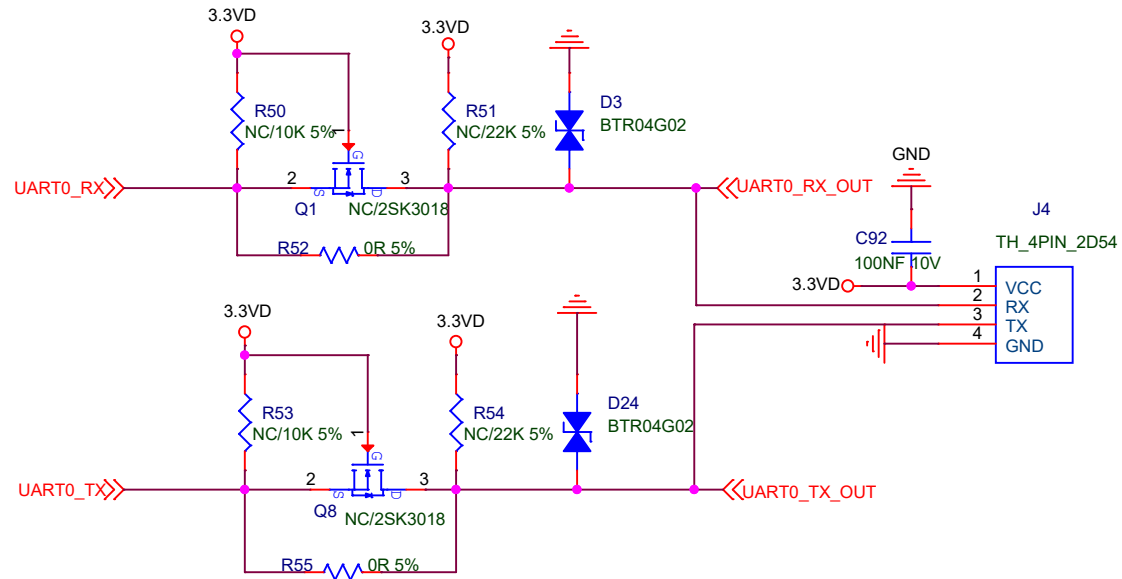
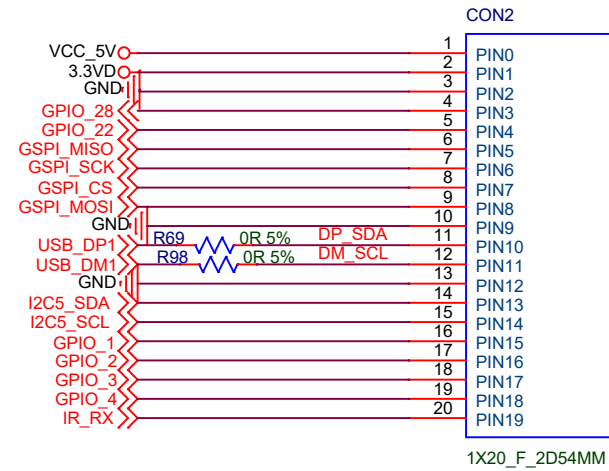
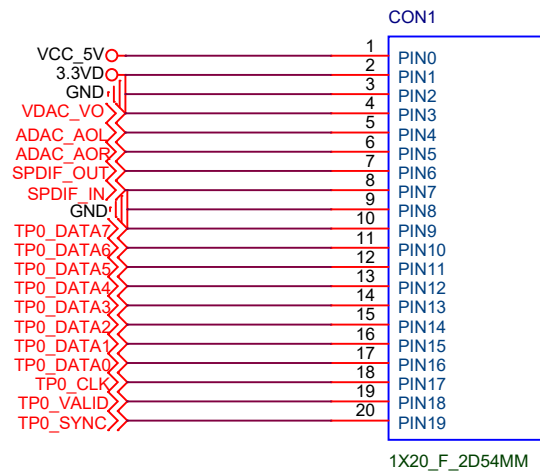
5

4

3

2

1



Version	Date	Author	Description
0.1	2021/01/05	Suluclac	Internal test
0.1A	2021/01/13	Suluclac	Modify bom, C12 & C13 from 10u to 0.1u, C184 & C185 from 10u to 1u, C33 from 100p to 0.1u, C34 from 220p to 0.1u, C35 from 470p to 0.1u.
0.1B	2021/03/23	Suluclac	1. Modify bom, R13 from NC to 4.7K, R206 & R213 change to 61.9K/F, R205 & R212 change to 36.5K/F, R204&R211change to 14K/F, C163 from NC to 100uF/16V.
0.2	2021/05/28	Suluclac	1. @Page12, Modify TX_I2C1_SCL & TX_I2C1_SDA pull high connection from 5VD to 5VS_HDMI. 2. @Page15, Modify LSADC pull high connection form 3.3VD to UR1_VDD and modify bom, R169 from NC to 9.1K, R172 from 4.7K to 11K. 3. @Page9, Modify bom, C169 & C175 from 1u to 4.7u, C172 & C180 from 15p/10V to NC, R207 from 49.9K/F to NC, R208 form 1K to NC, R209 from 3K to NC, C176 from 1u to NC. 4. @Page10, Modify bom, R77~R83 from 22 to 0. 5. @Page06, Modify bom, R16 from 22 to 0. 6. HDK release
0.3	2021/06/28	Suluclac	1. Modify PartU1, remove SNF_SLA & SNF_MA function 2. @Page09, Modify VDAC VO connection, add L11 to GND after R55. 3. @Page03, Modify UART0 connecton, add U33, U34, R217, R218,C581~C584 to prevent leakage from unknow UART debug board. 4. HDK release
0.4	2021/07/30	Suluclac	1. Modify Part U1, change Ball V13 from 0.8V_U2 to NC and remove Ball Y6 SPDIF_IN_COAXIAL function. 2. @Page04, remove R214. 3. @Page07, Change U6 EN pin connection from 5VD to 3.3VD. 4. HDK release
0.5	2021/08/24	Suluclac	1. @Page12, Change HDMI common mode choke from U10 & U11 to CM800~ CM803. 2. HDK release
0.5A	2022/07/19	Suluclac	1. @Page10, Modify BOM, change R91 & R92 from NC to 10K. 2. HDK release
0.5B	2022/08/23	Suluclac	1. @Page03, Modify BOM, change U33 & U34 to NC, C581~C584 from 0.1u to NC, R217 & R218 from NC to 0 ohm. 2. @Page04, Modify BOM, change C10 from 0.1u to 10u/6.3V. 3. @Page10, Modify BOM, change U30 & U31 to NC, R200 & R201 from NC to 0 ohm, R91 & R92 from 10K to 47K ohm. 4. HDK release

GPI00	O/L	PD#	default I/H
GPI01	<div>L 3.3V H 5V</div>	SC_PWR_SEL	default I/H
GPI02	I/L	BT_WAKE#	default I/H
GPI03	O/L	WiFi_DIS#	default I/H
GPI04	I/L	WiFi_WAKE#	default I/H
GPI05	O/H	HDMI_TX_OFF	default O/L
GPI06	O/L	BT_DIS#	default I/H
GPI07	I/H	HDMI_HPD	default I/L
GPI022	O/L	SC_CMDVCC#	default I/H
GPI025	I/L	PCIE0_CLKREQ#	default I/H
GPI026	I/L	Install	default I/H
GPI027	O/H	LED	default I/H
GPI030	O/L	SDCARD_PWR#	default I/H
GPI047	O/L	Audio Mute	default I/L
GPI048	O/L	USB0_PWR/GPIO48	Boot Option
GPI049	O/L	USB1_PWR/GPIO49	Boot Option
GPI052	I/L	PCIE1_CLKREQ#	default I/H
GPI053	O/L	USBC_REVERSE	default I/H
GPI080	O/L	PCIE1_RST#	default I/H
GPI081	O/L	PCIE2_RST#	default I/H

Realtek Semiconductor Corp.

Engineer: HW Wang

Title

Note

Size Custom

Project Name

BleedingEdge

Rev V0.5B

Date:

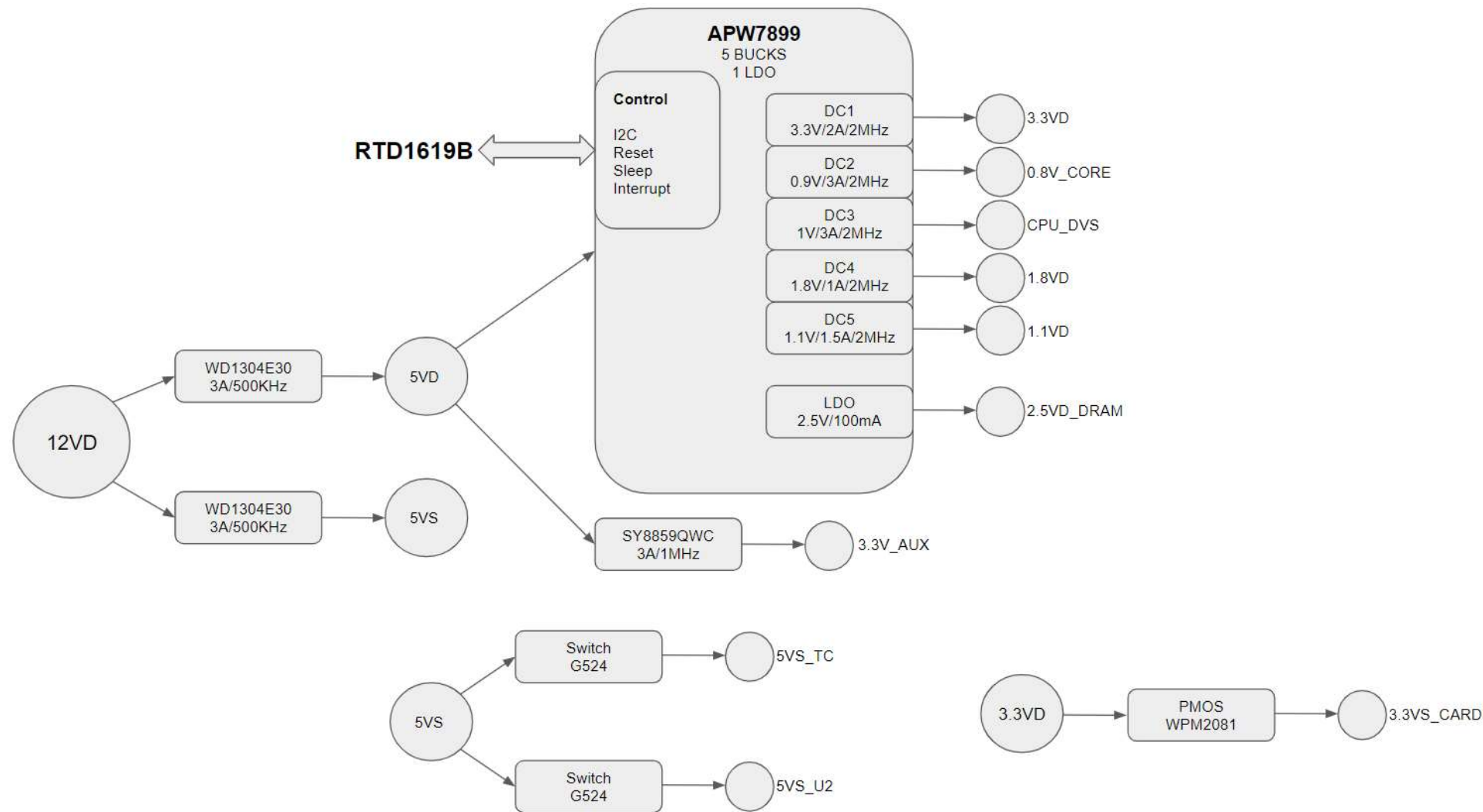
Tuesday, November 12, 2024

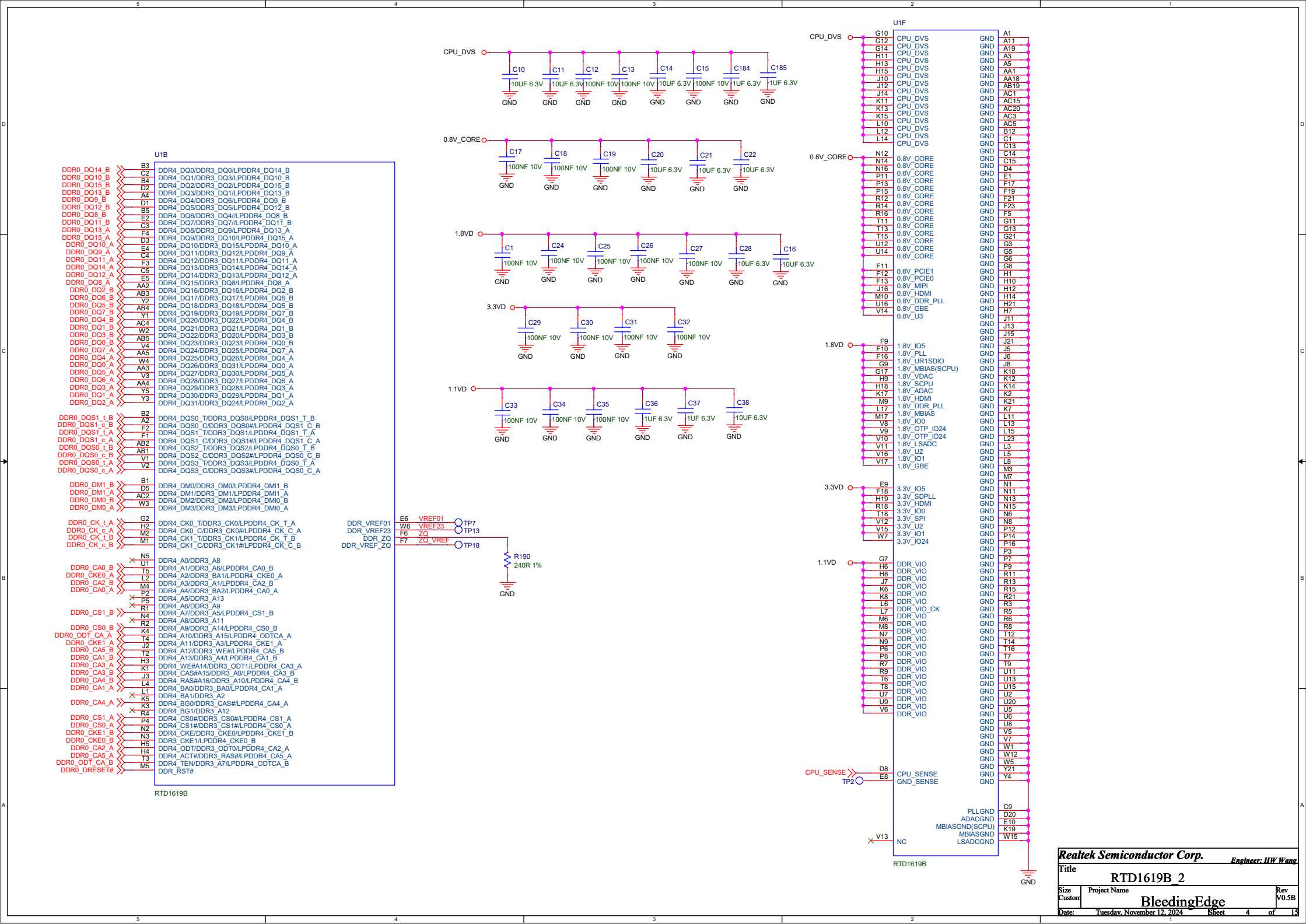
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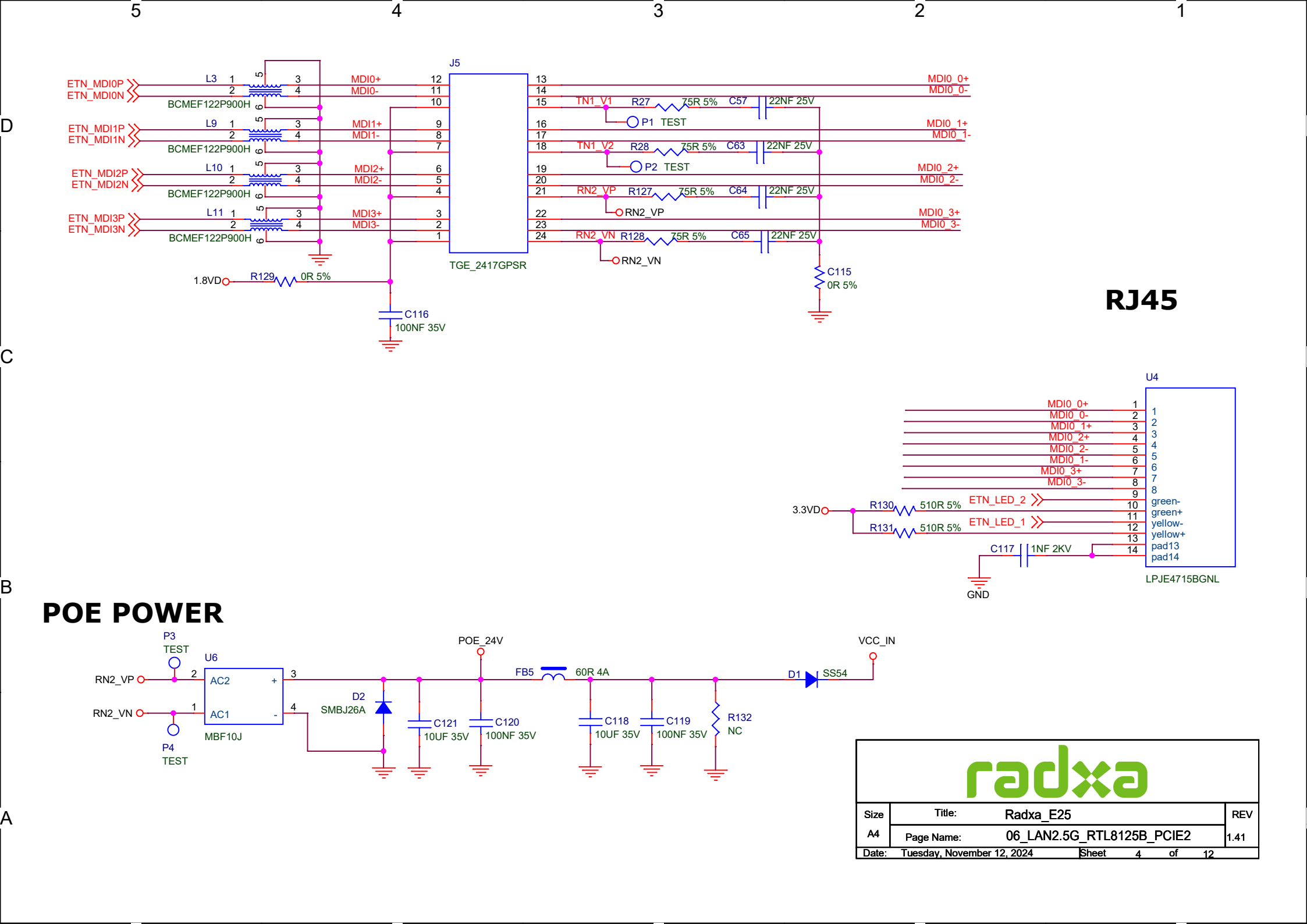
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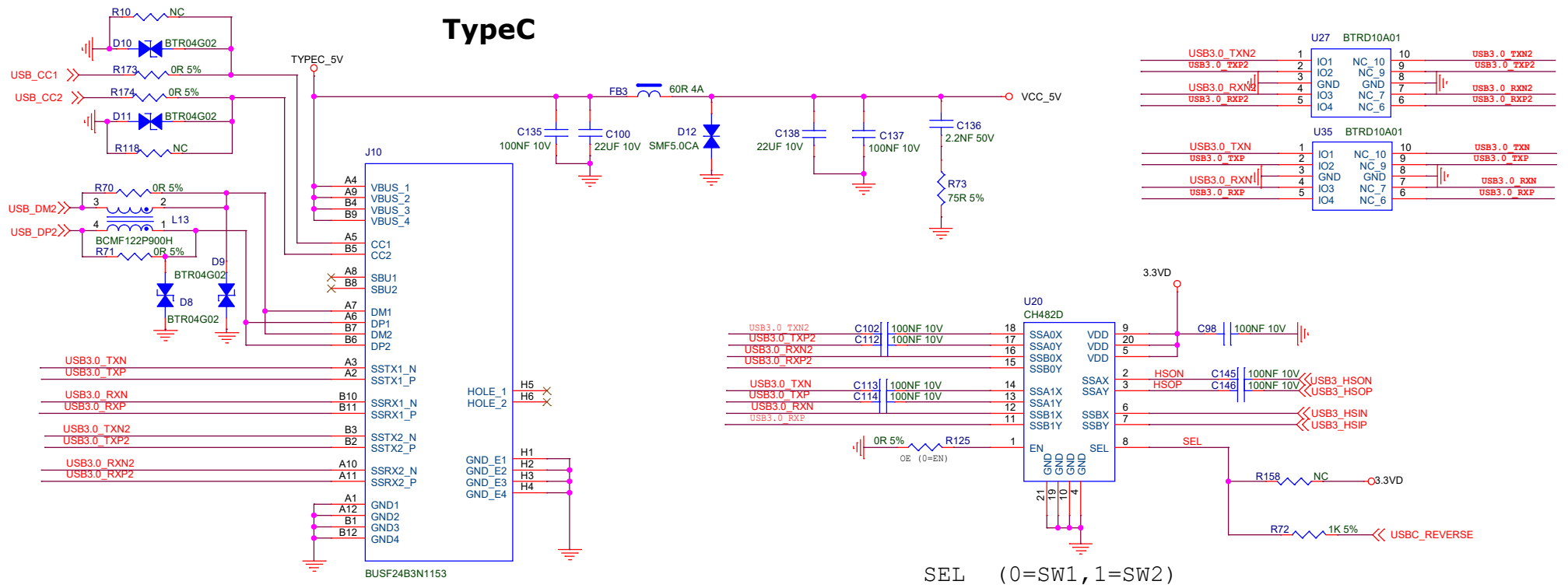
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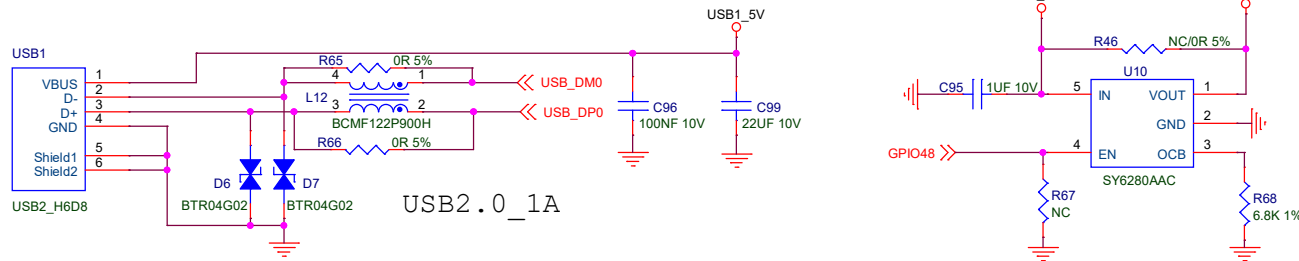




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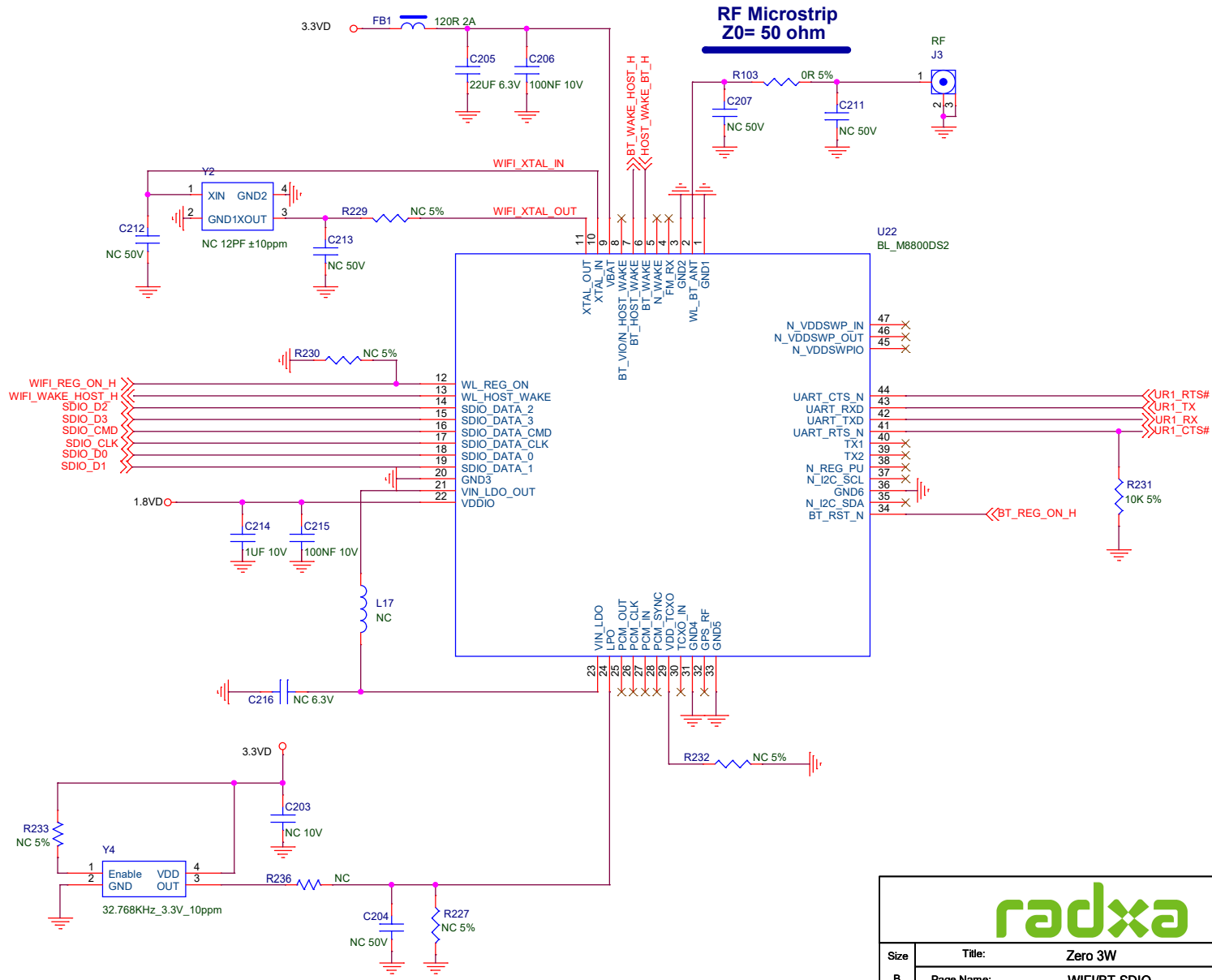



USB2.0



radxa		
Size	Title: Zero 3W	REV
B	Page Name: USB Port	V1.11
Date:	Tuesday, November 12, 2024	Sheet 17 of 22

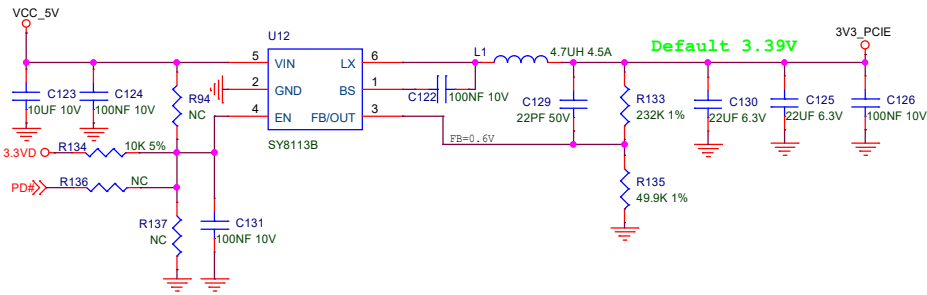
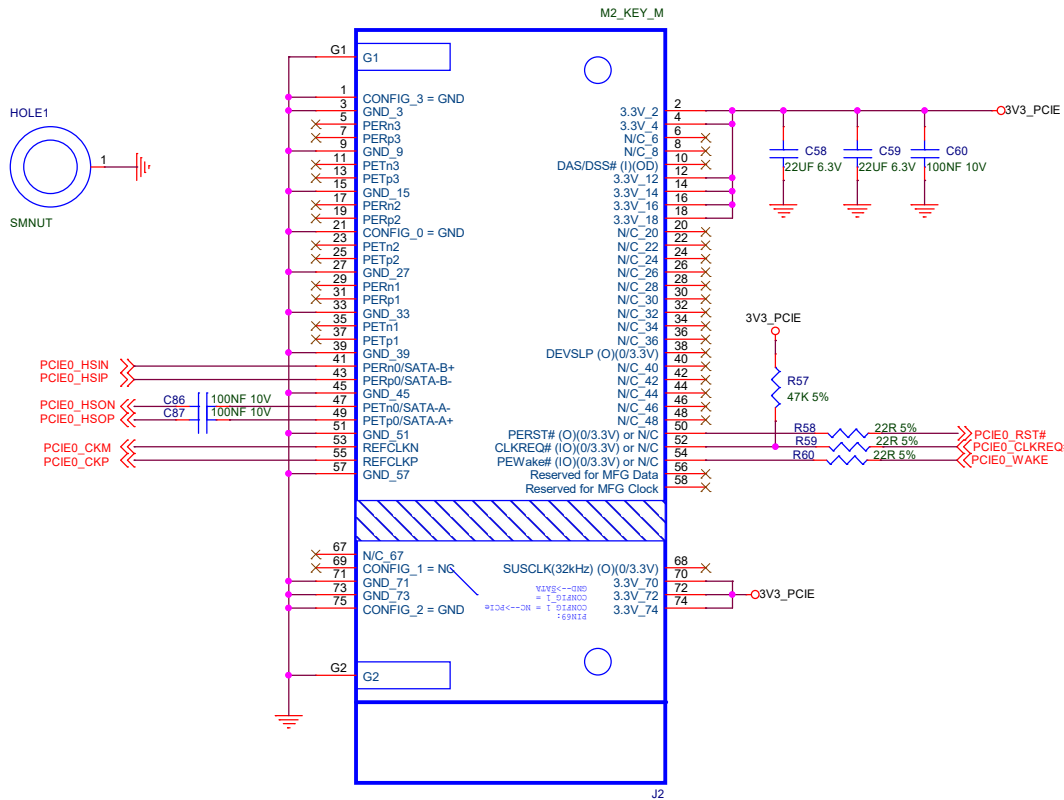
SDIO WIFI/BT



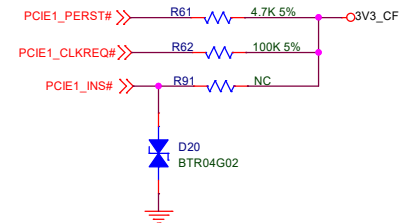
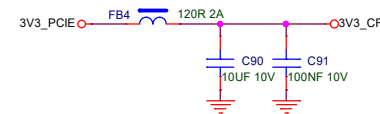
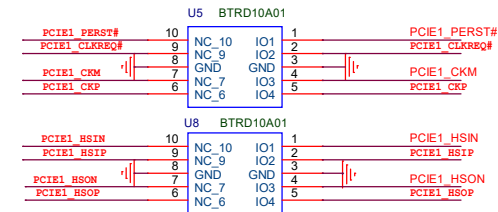
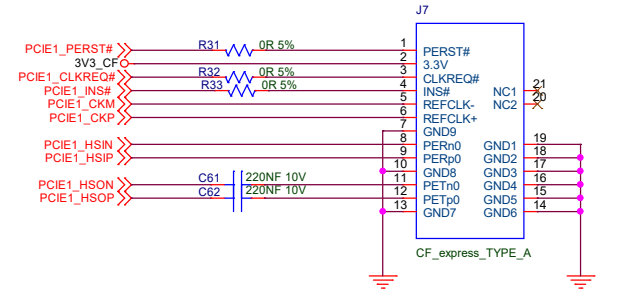


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B	Page Name: WIFI/BT-SDIO	V1.11
Date: Tuesday, November 12, 2024 Sheet 19 of 22		

PCIE



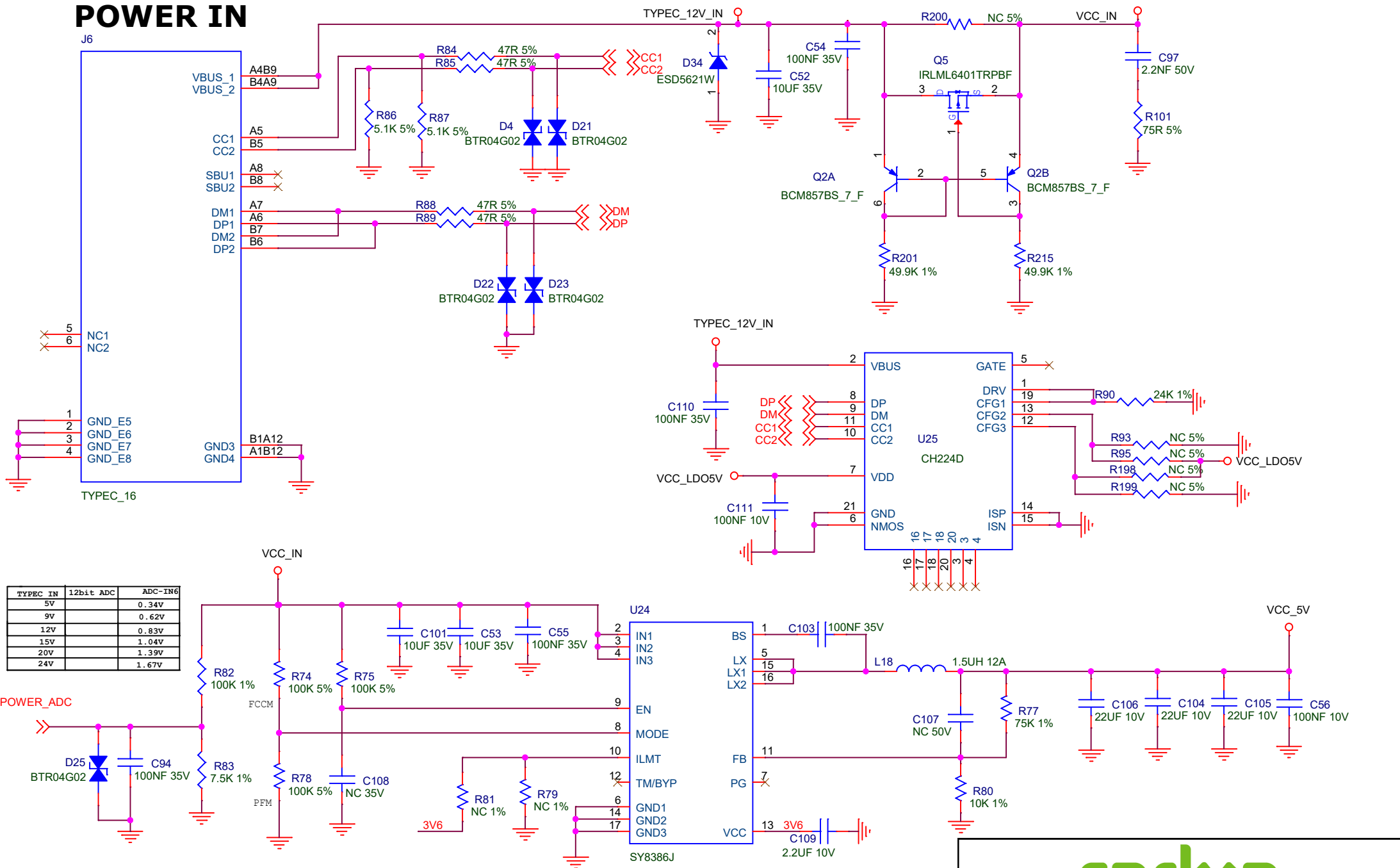
CF express TYPE A



radxa

Size	Title:	ROCK 5A	REV
A3	Page Name:	M.2 E Key	1.1
Date:	Wednesday, November 13, 2024	Sheet	21 of 26

POWER IN



TYPEC IN	12bit ADC	ADC-IN6
5V		0.34V
9V		0.62V
12V		0.83V
15V		1.04V
20V		1.39V
24V		1.67V

