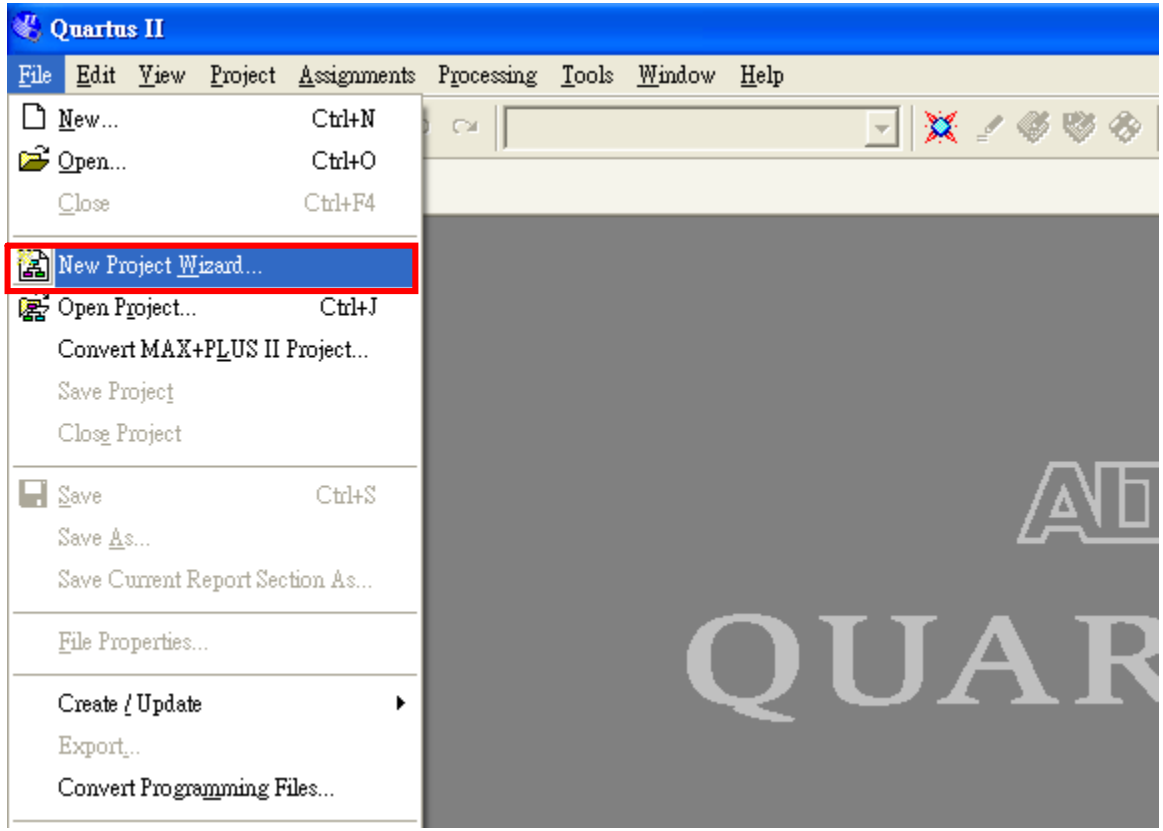
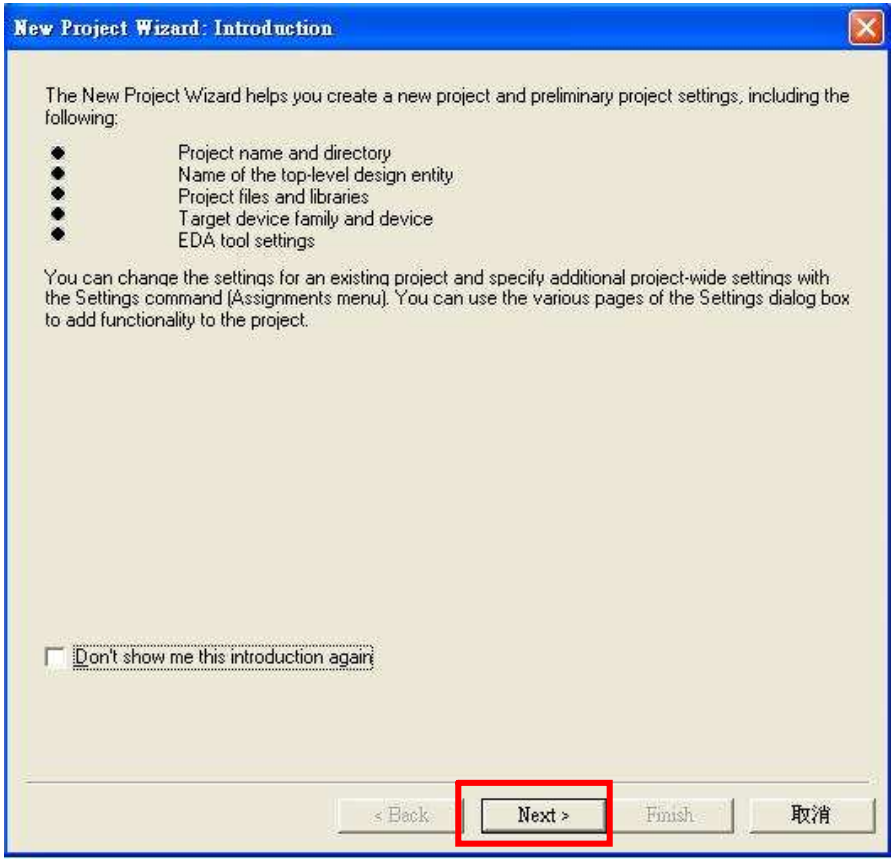
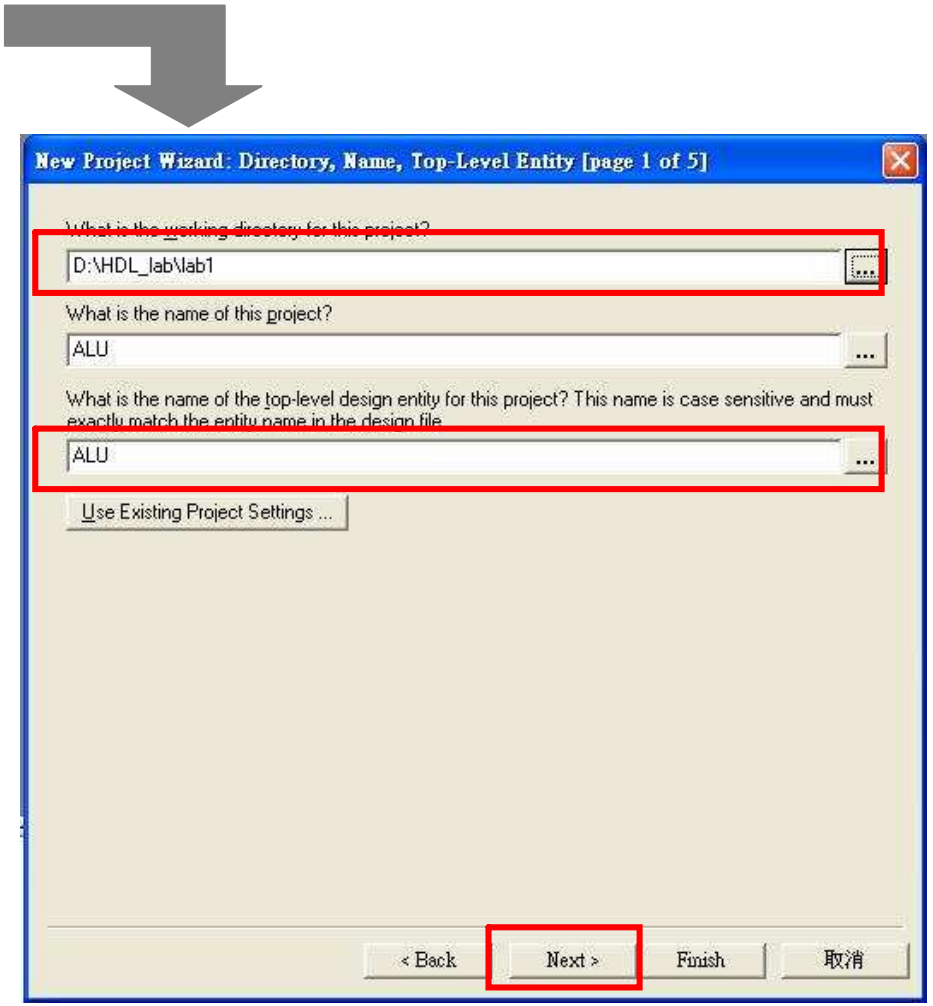
Using Quartus II 7.0

➢Open new project wizard.

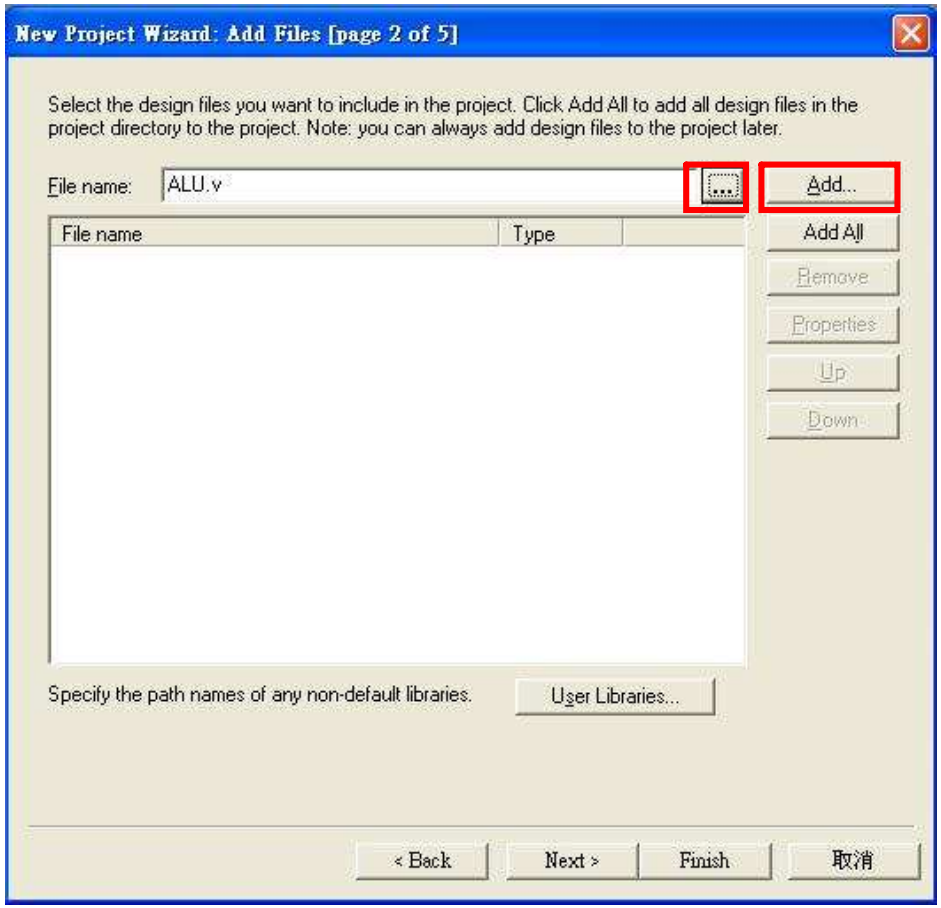


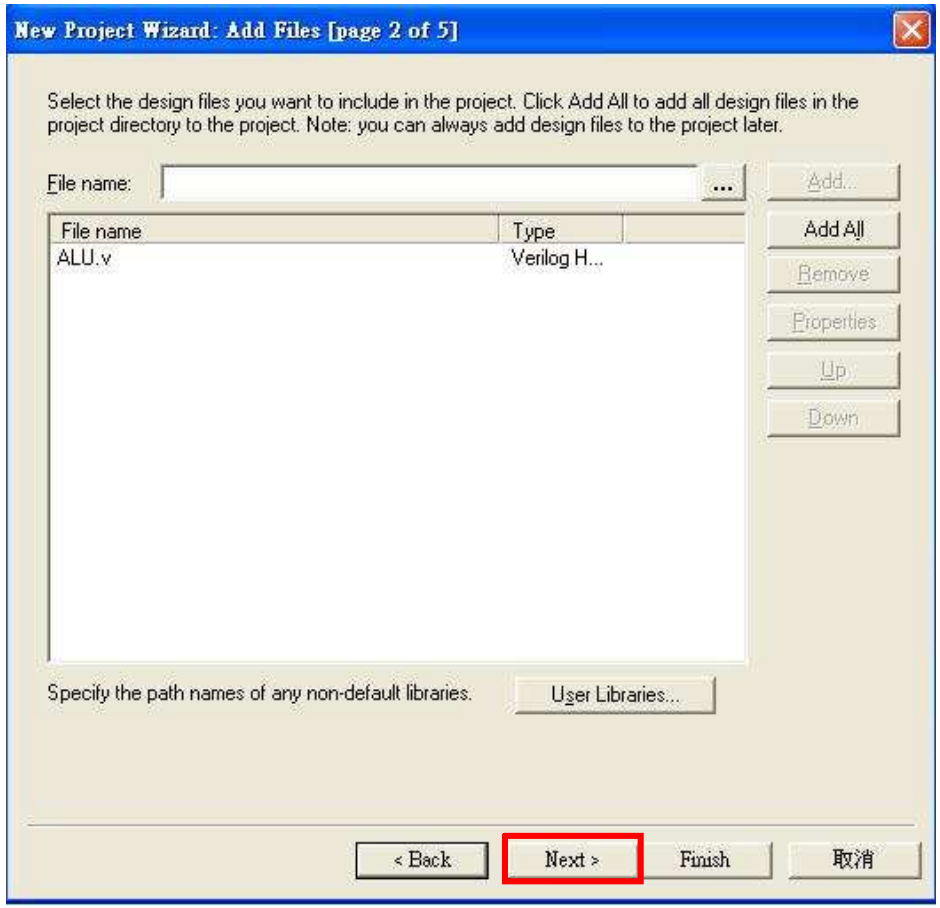
➢Specify the directory and the name of the project.



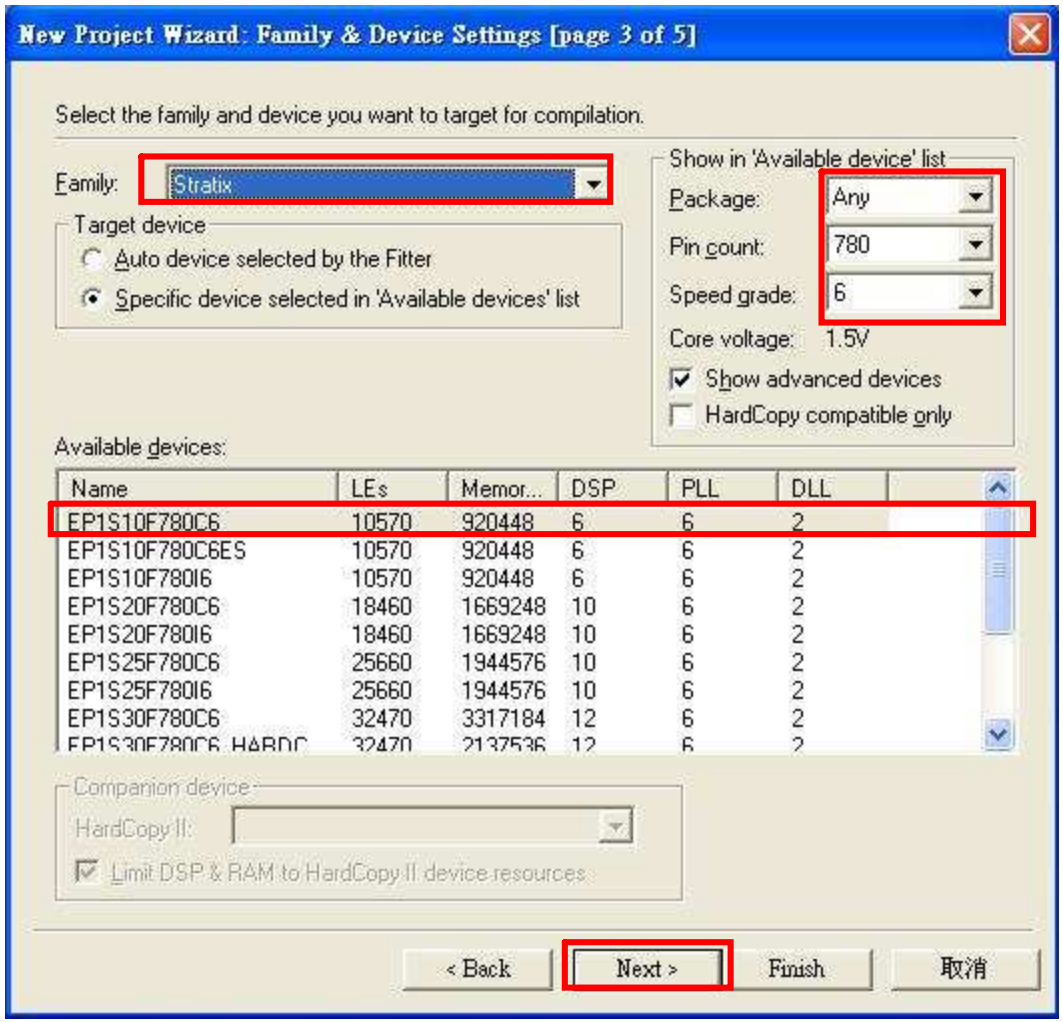


➢**Select design files and source files. Or click “Next” to skip this step.**

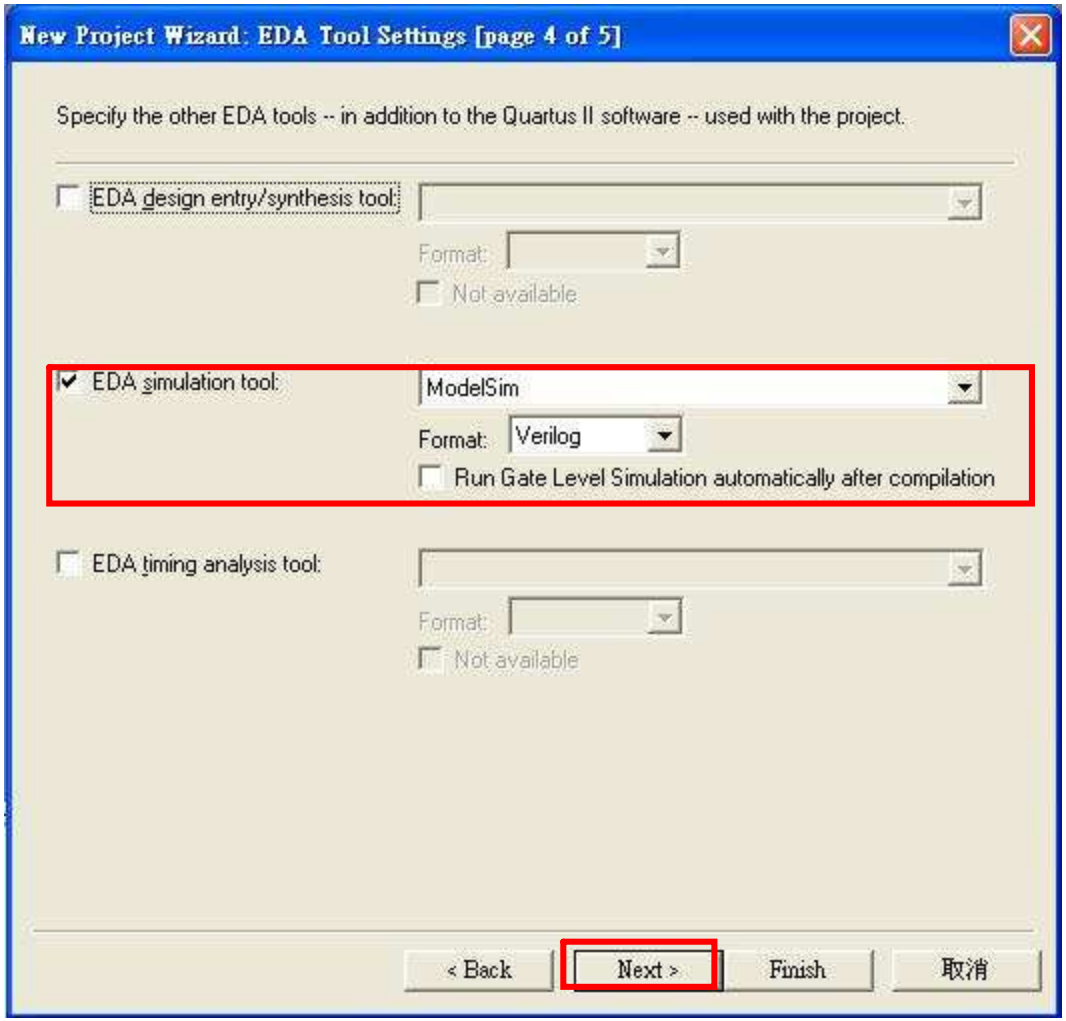




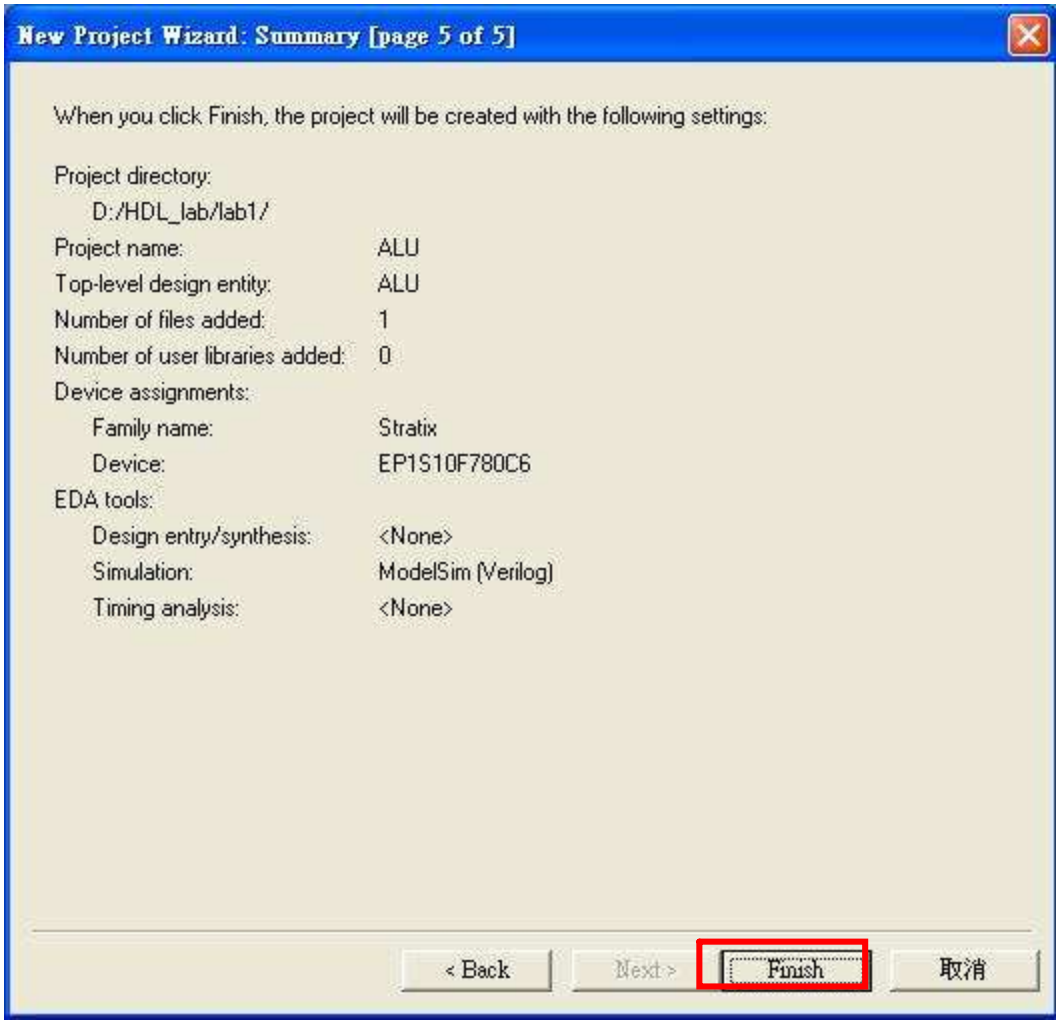
➢Specify device settings.



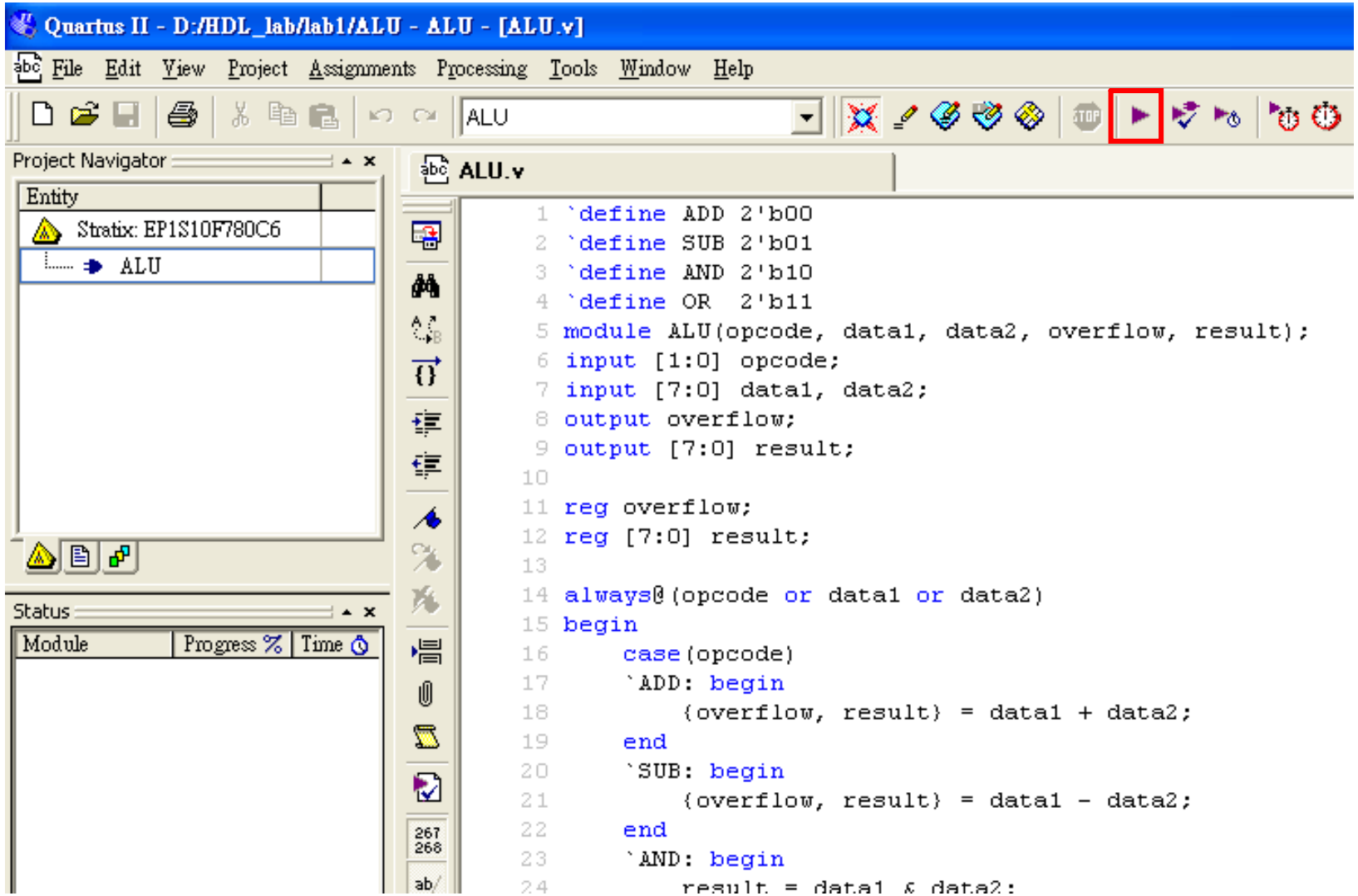
➢**Specify other EDA tools. Here you can click “Next” to skip this step since we don’t use other EDA tools.**



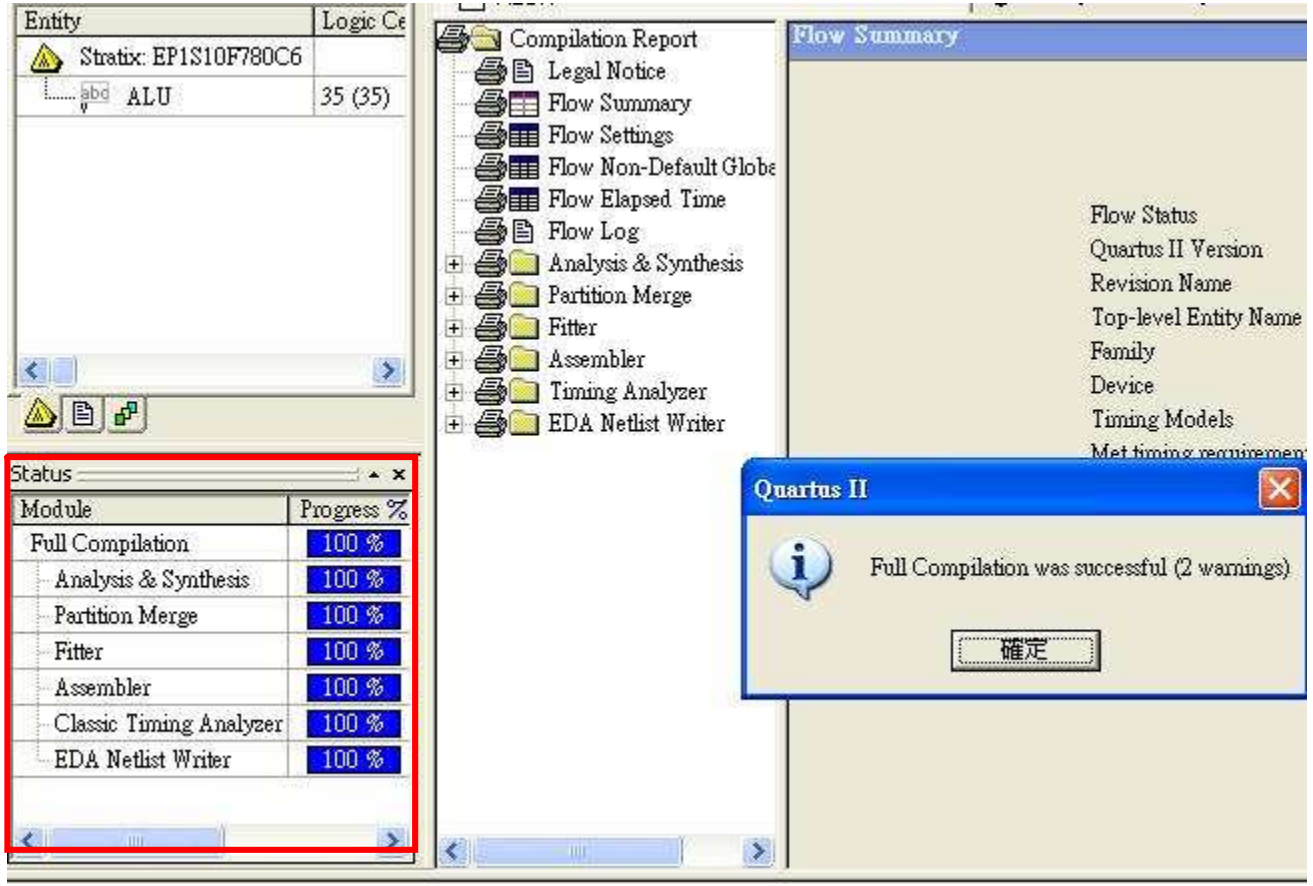
➢**Click “Finish”, and the new project will be created with the specified settings.**



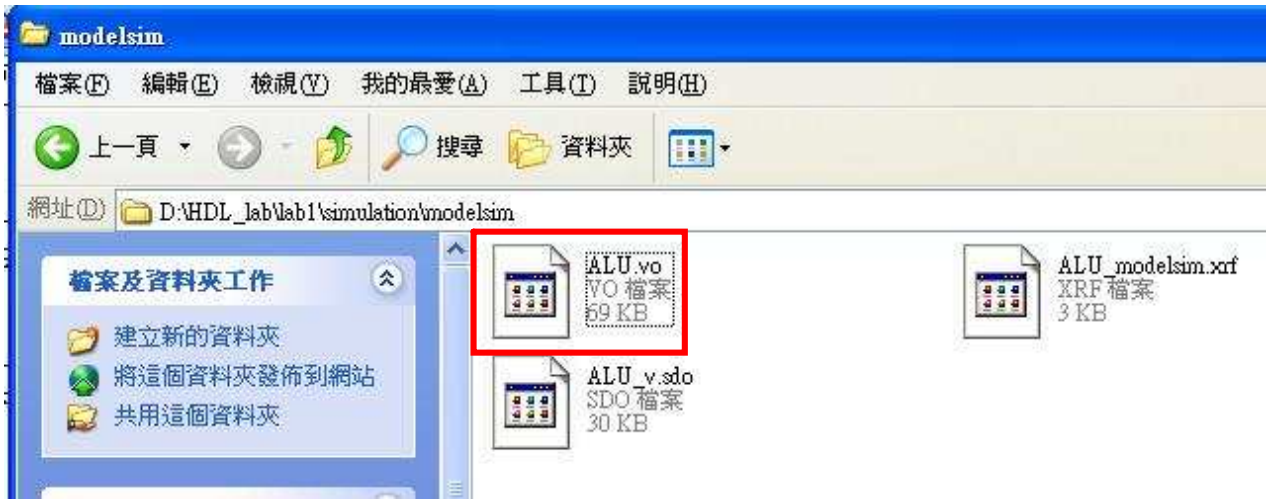
➢Start compilation.



➢Compilation result.

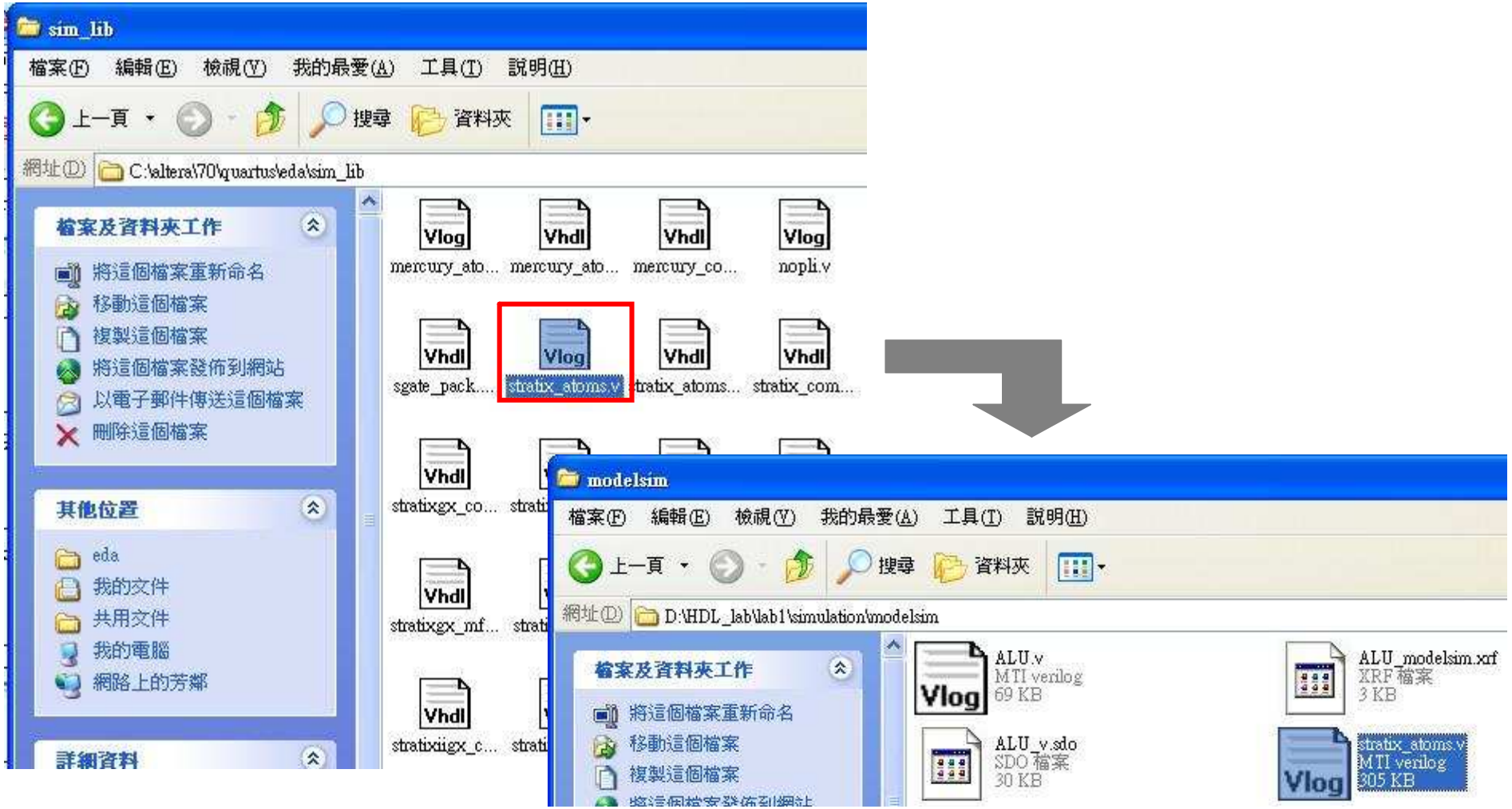


➢**Get the post-layout gate-level netlist. Rename your_design.vo to your_design.v for simulation.**



➢**Prepare to post-layout simulation.**

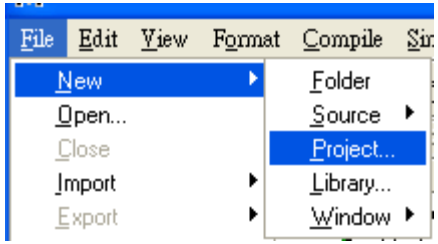
Copy file (\%your_quartus_dir\eda\sim_lib\stratix_atoms.v) to your project directory

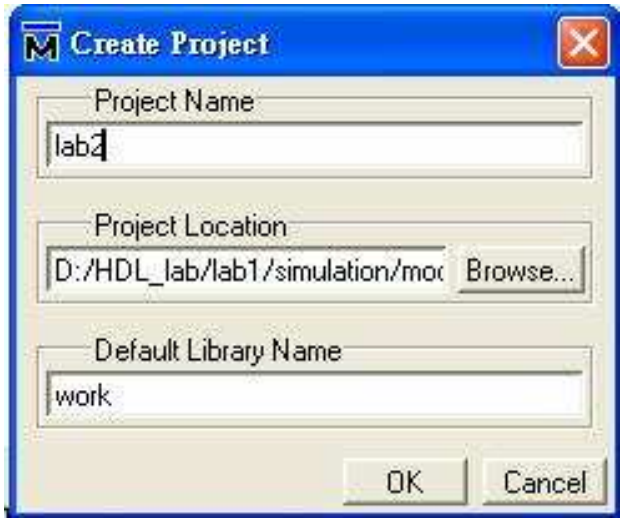


➢**Copy your testbench and testing data to your project directory.**

Using ModelSim

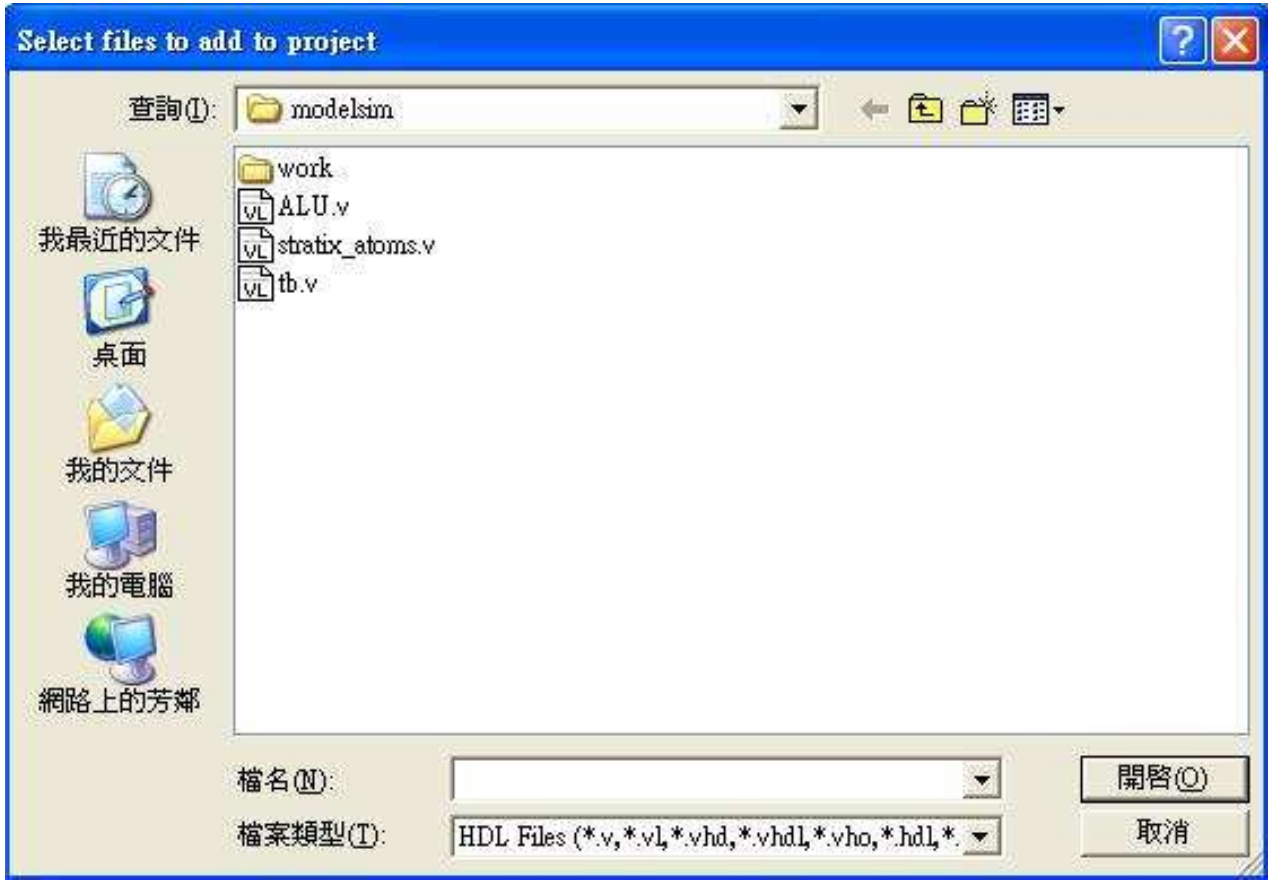
➢Open modelSim and create a project.



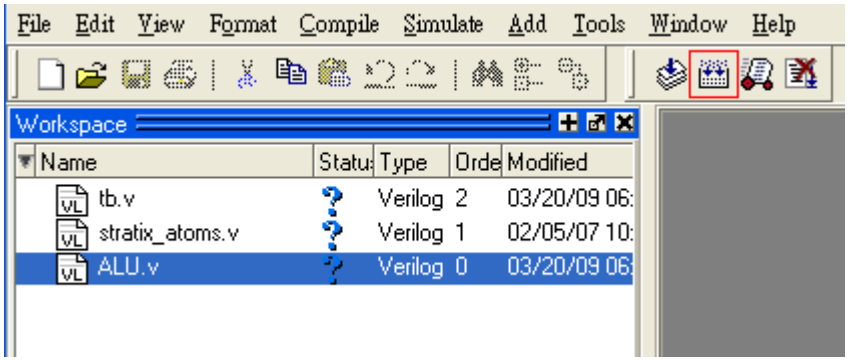


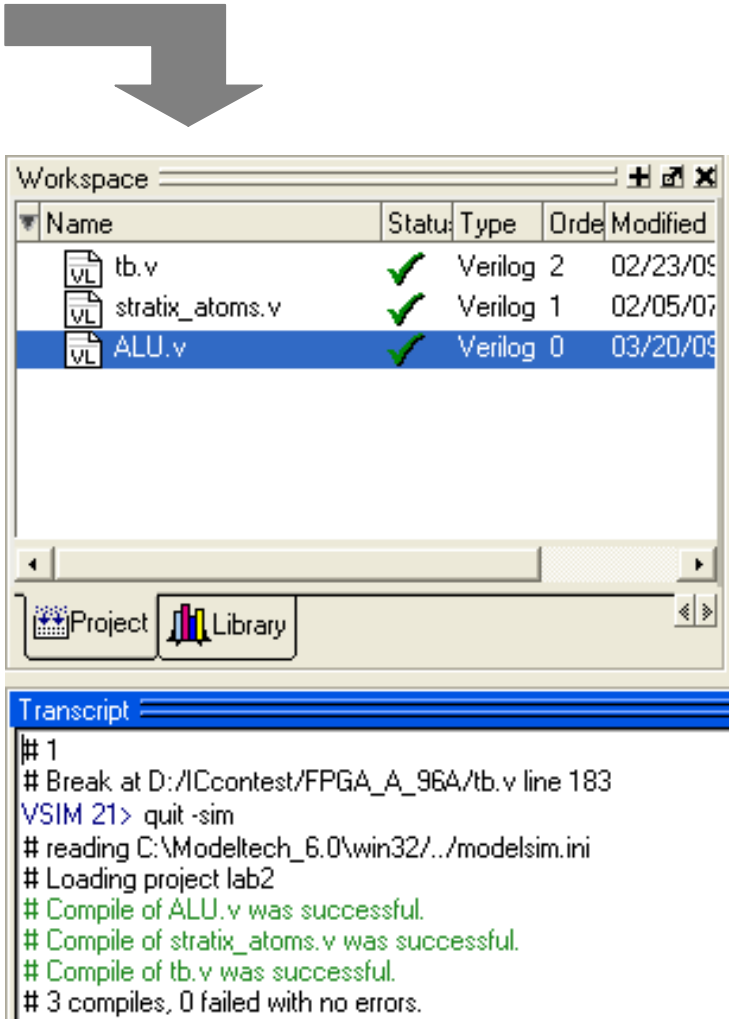
➢Add files to project.

Pre-simulation: before synthesis
Post-simulation: after synthesis

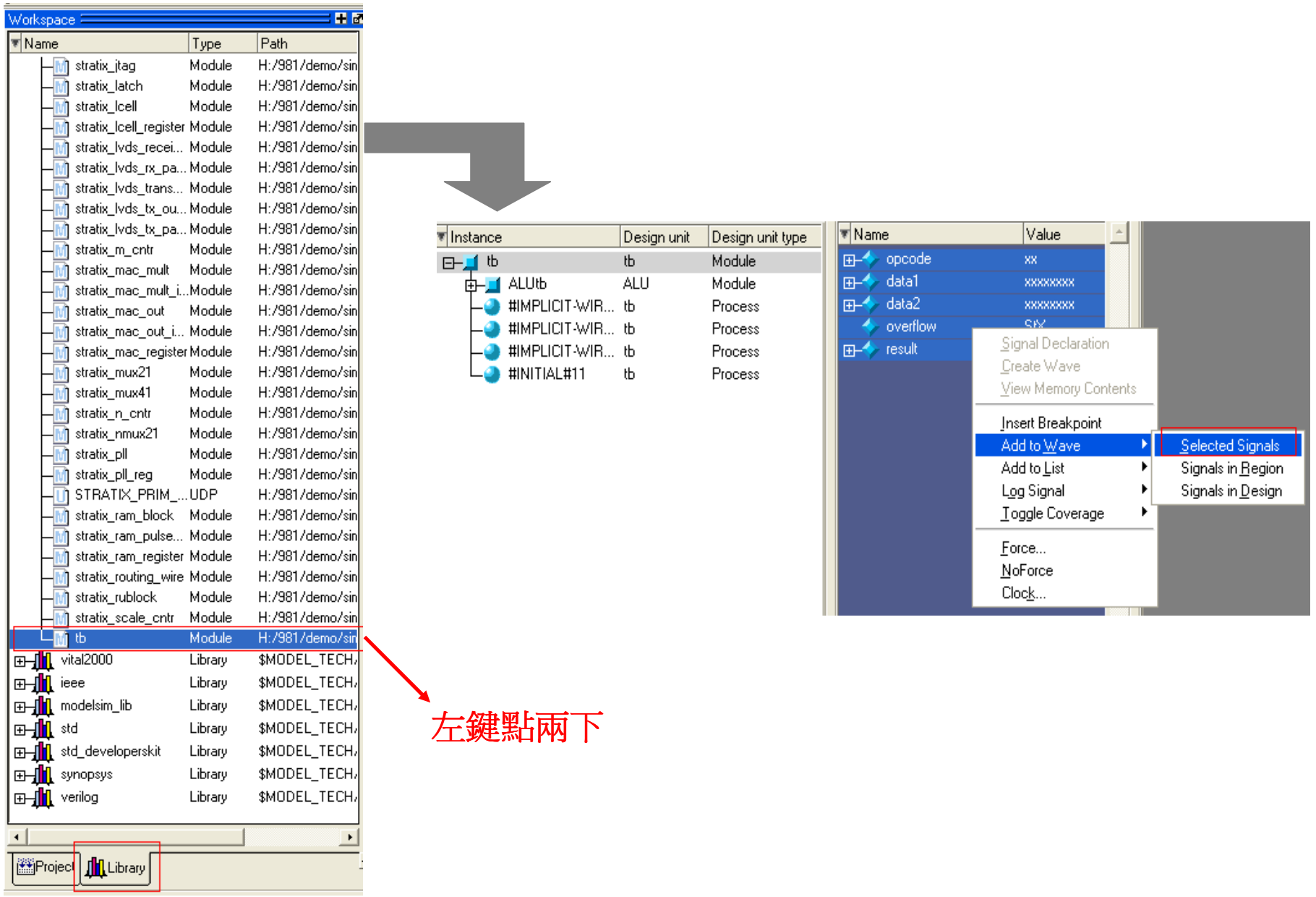


➢**Compilation. And the following simulation steps is the same with RTL simulation.**

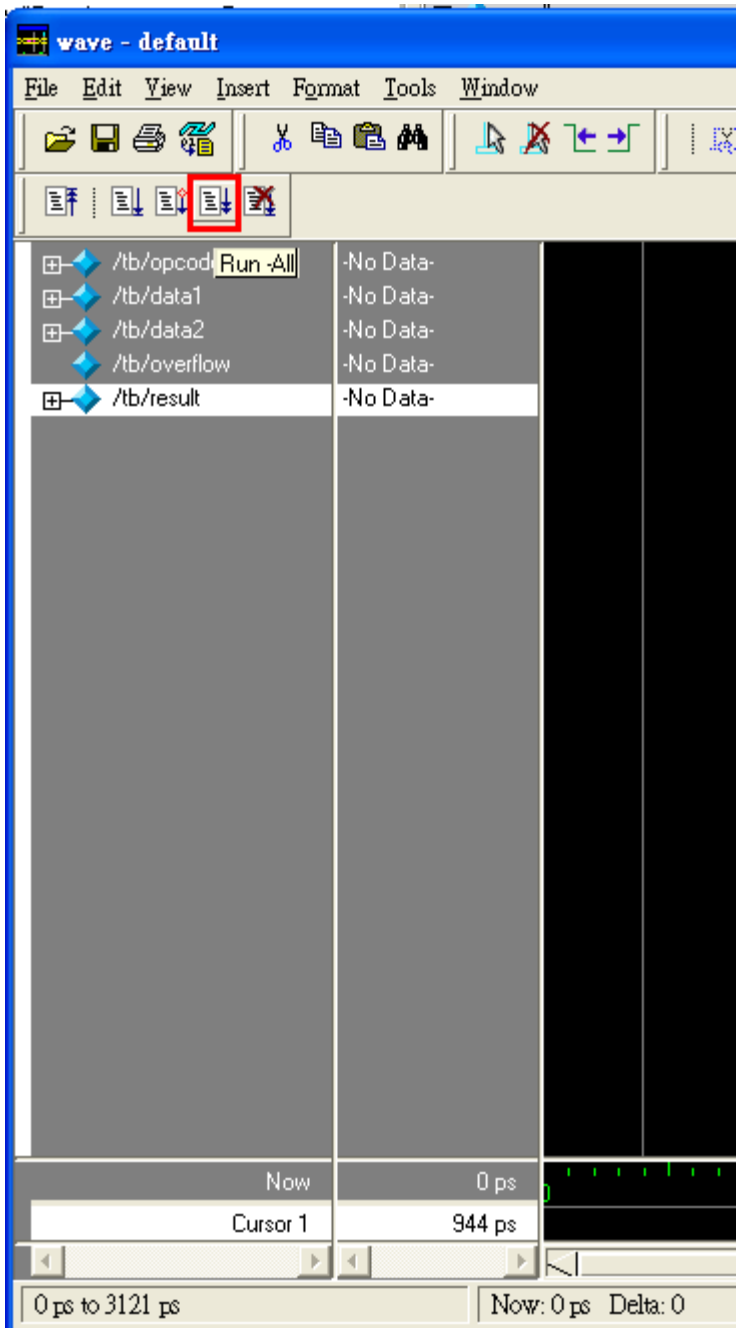




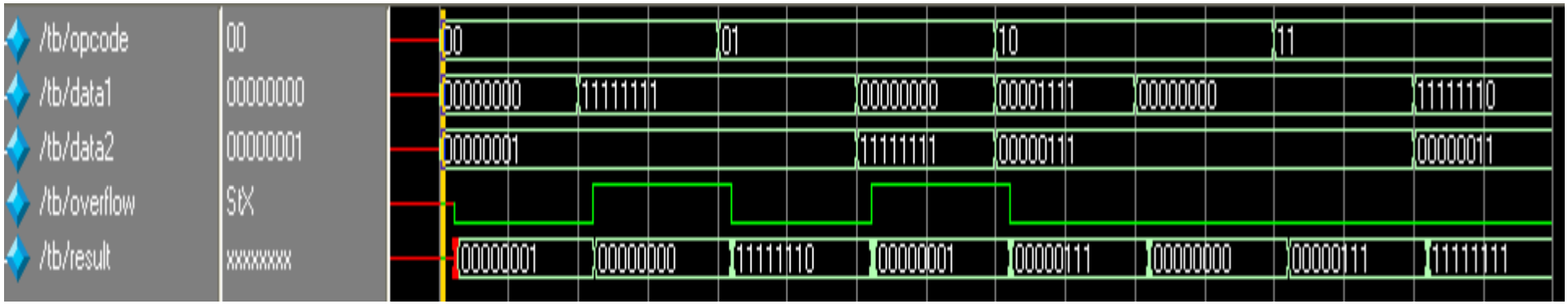
➢Simulation.


Workspace
Name
Type
Path
stratix_jtag Module H:/981/demo/sin
stratix_latch Module H:/981/demo/sin
stratix_lcell Module H:/981/demo/sin
stratix_lcell_register Module H:/981/demo/sin
stratix_lvds_recei... Module H:/981/demo/sin
stratix_lvds_rx_pa... Module H:/981/demo/sin
stratix_lvds_trans... Module H:/981/demo/sin
stratix_lvds_tx_ou... Module H:/981/demo/sin
stratix_lvds_tx_pa... Module H:/981/demo/sin
stratix_m_cntr Module H:/981/demo/sin
stratix_mac_mult Module H:/981/demo/sin
stratix_mac_mult_i... Module H:/981/demo/sin
stratix_mac_out Module H:/981/demo/sin
stratix_mac_out_i... Module H:/981/demo/sin
stratix_mac_register Module H:/981/demo/sin
stratix_mux21 Module H:/981/demo/sin
stratix_mux41 Module H:/981/demo/sin
stratix_n_cntr Module H:/981/demo/sin
stratix_nmux21 Module H:/981/demo/sin
stratix_pll Module H:/981/demo/sin
stratix_pll_reg Module H:/981/demo/sin
STRATIX_PRIM_... UDP H:/981/demo/sin
stratix_ram_block Module H:/981/demo/sin
stratix_ram_pulse... Module H:/981/demo/sin
stratix_ram_register Module H:/981/demo/sin
stratix_routing_wire Module H:/981/demo/sin
stratix_rublock Module H:/981/demo/sin
stratix_scale_cntr Module H:/981/demo/sin
tb Module H:/981/demo/sin
vital2000 Library $MODEL_TECH/
ieee Library $MODEL_TECH/
modelsim_lib Library $MODEL_TECH/
std Library $MODEL_TECH/
std_developerskit Library $MODEL_TECH/
synopsys Library $MODEL_TECH/
verilog Library $MODEL_TECH/
Project
Library
Instance
Design unit
Design unit type
tb tb Module
ALUtb ALU Module
#IMPLICIT-WIR... tb Process
#IMPLICIT-WIR... tb Process
#IMPLICIT-WIR... tb Process
#INITIAL#11 tb Process
Name
Value
opcode xx
data1 xxxxxxxx
data2 xxxxxxxx
overflow
result
Signal Declaration
Create Wave
View Memory Contents
Insert Breakpoint
Add to Wave
Add to List
Log Signal
Toggle Coverage
Force...
NoForce
Clock...
Selected Signals
Signals in Region
Signals in Design
左鍵點兩下

➢Simulation.

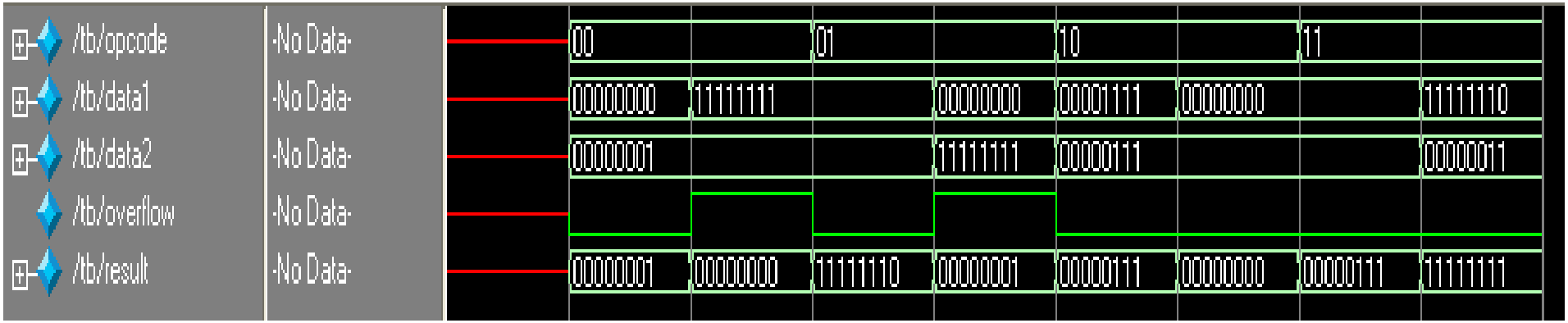

wave - default
File Edit View Insert Format Tools Window
Run -All
/tb/opcod
/tb/data1
/tb/data2
/tb/overflow
/tb/result
-No Data-
-No Data-
-No Data-
-No Data-
-No Data-
Now
0 ps
Cursor 1
944 ps
0 ps to 3121 ps
Now: 0 ps Delta: 0

➢The Post-simulation waveform

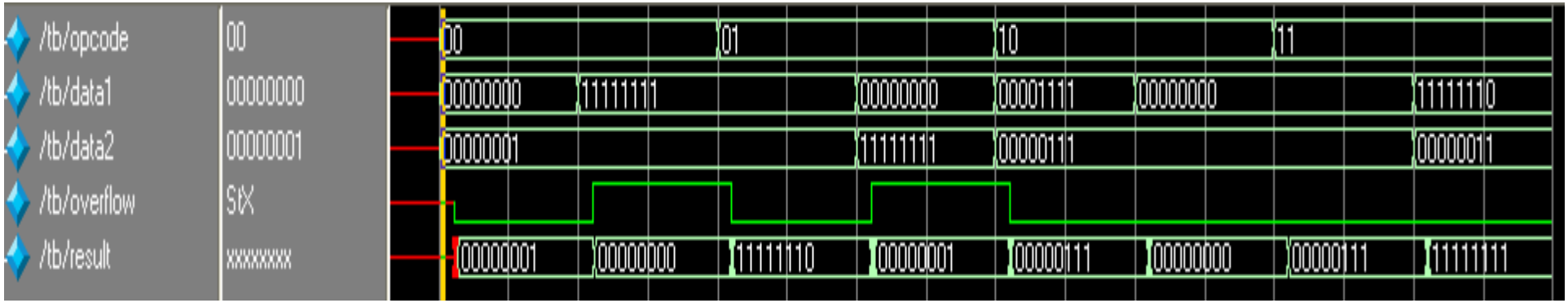


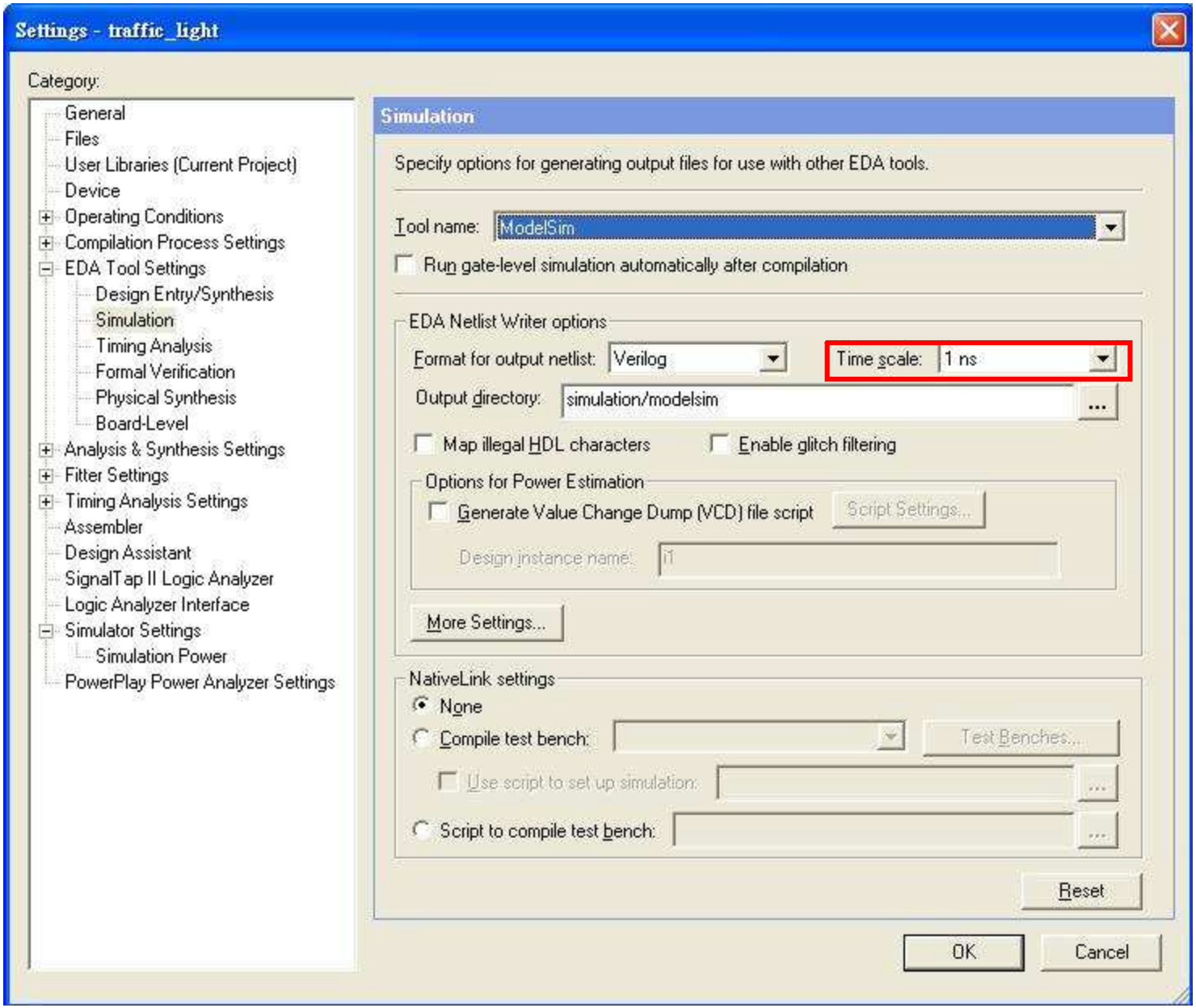
➢Compare with the waveform of RTL simulation

RTL simulation



Post-layout gate-level simulation




Settings - traffic_light
Category:
General
Files
User Libraries (Current Project)
Device
Operating Conditions
Compilation Process Settings
EDA Tool Settings
Design Entry/Synthesis
Simulation
Timing Analysis
Formal Verification
Physical Synthesis
Board-Level
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
Simulation Power
PowerPlay Power Analyzer Settings
Simulation
Specify options for generating output files for use with other EDA tools.
Tool name: ModelSim
Run gate-level simulation automatically after compilation
EDA Netlist Writer options
Format for output netlist: Verilog
Time scale: 1 ns
Output directory: simulation/modelsim
Map illegal HDL characters
Enable glitch filtering
Options for Power Estimation
Generate Value Change Dump (VCD) file script
Script Settings...
Design instance name: i1
More Settings...
NativeLink settings
None
Compile test bench:
Test Benches...
Use script to set up simulation:
Script to compile test bench:
Reset
OK
Cancel