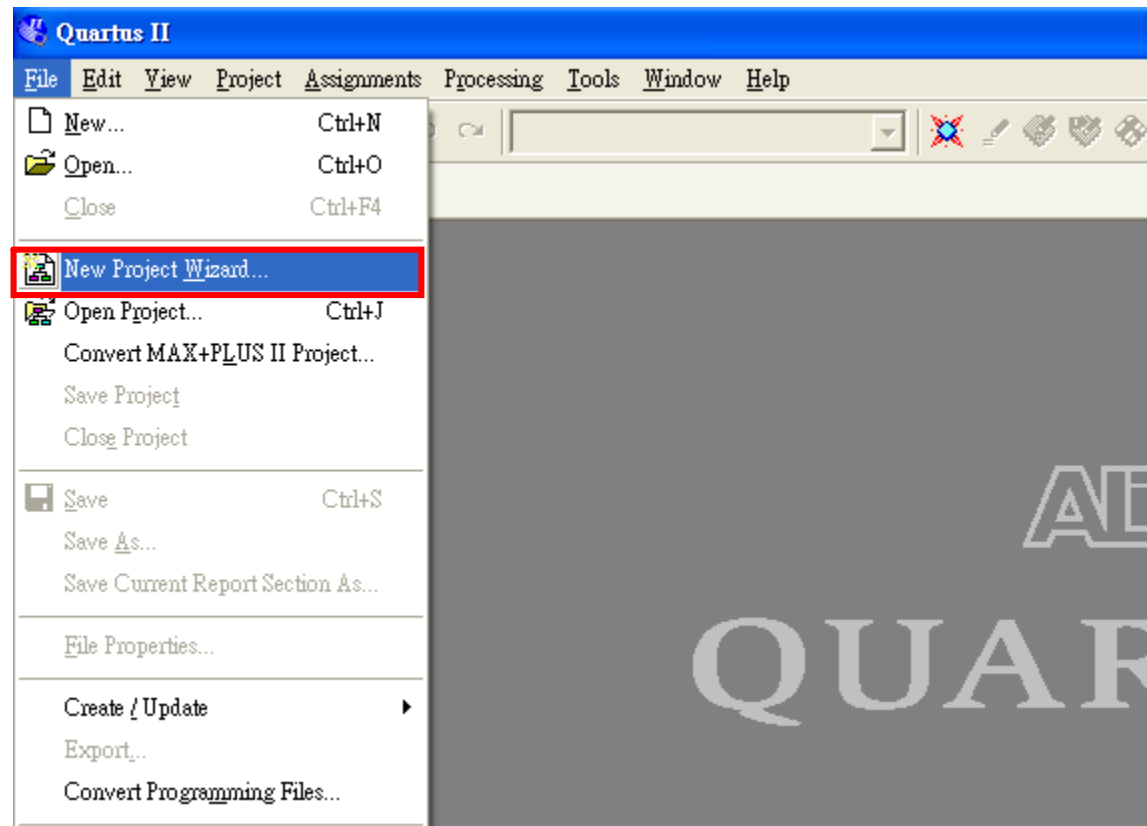
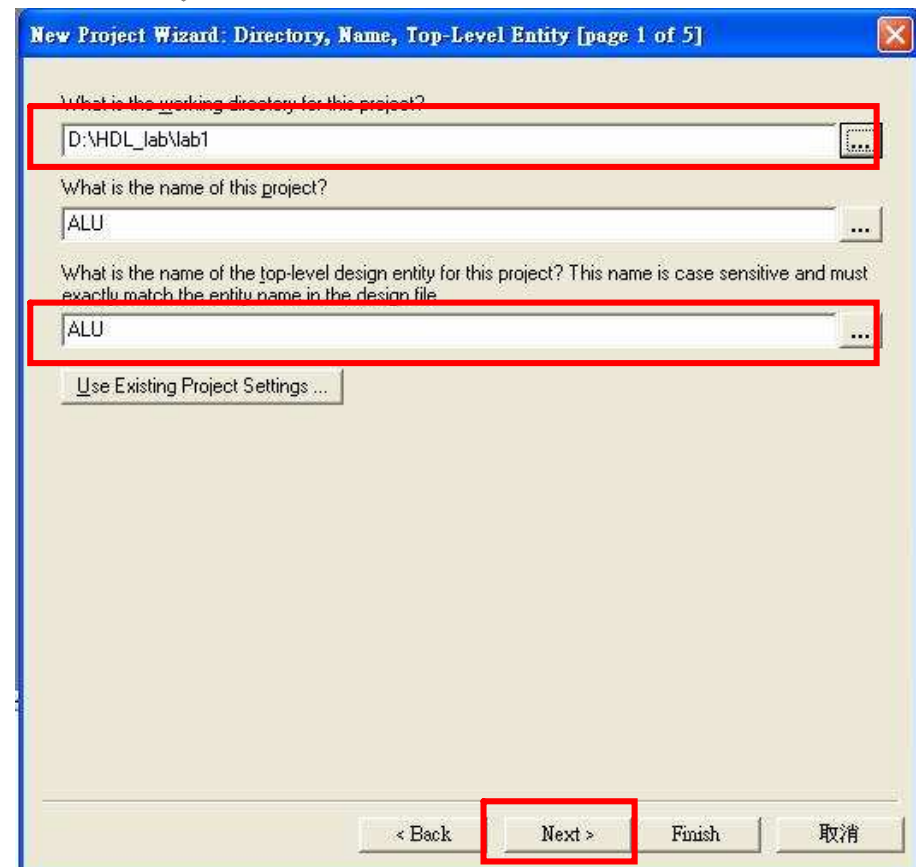
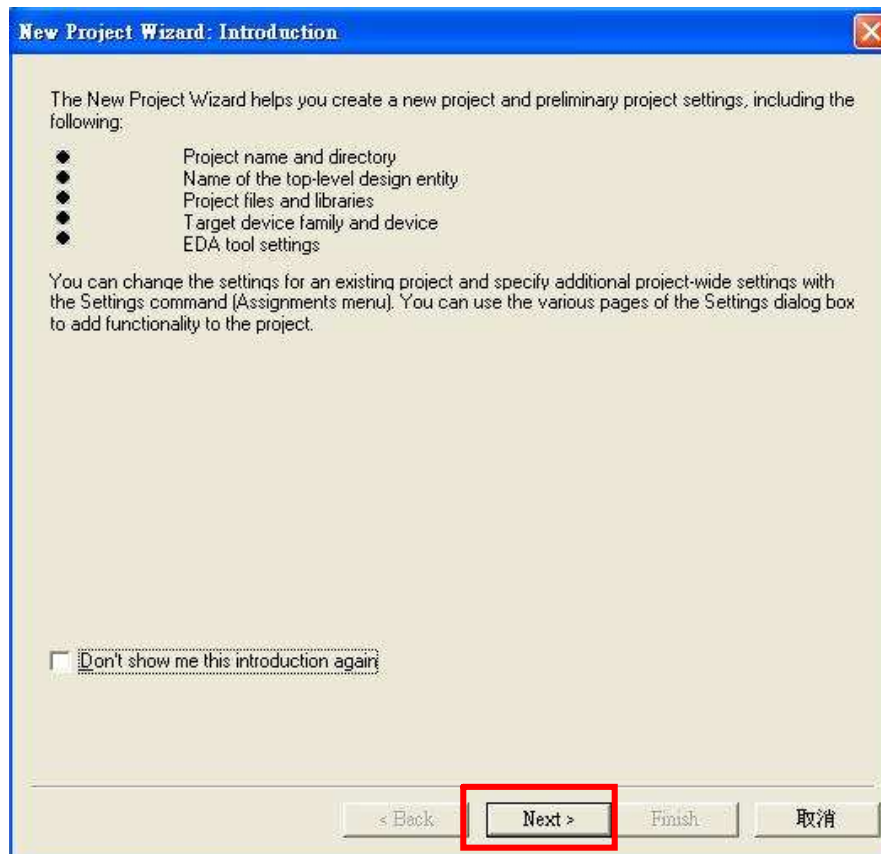


# Using Quartus II 7.0

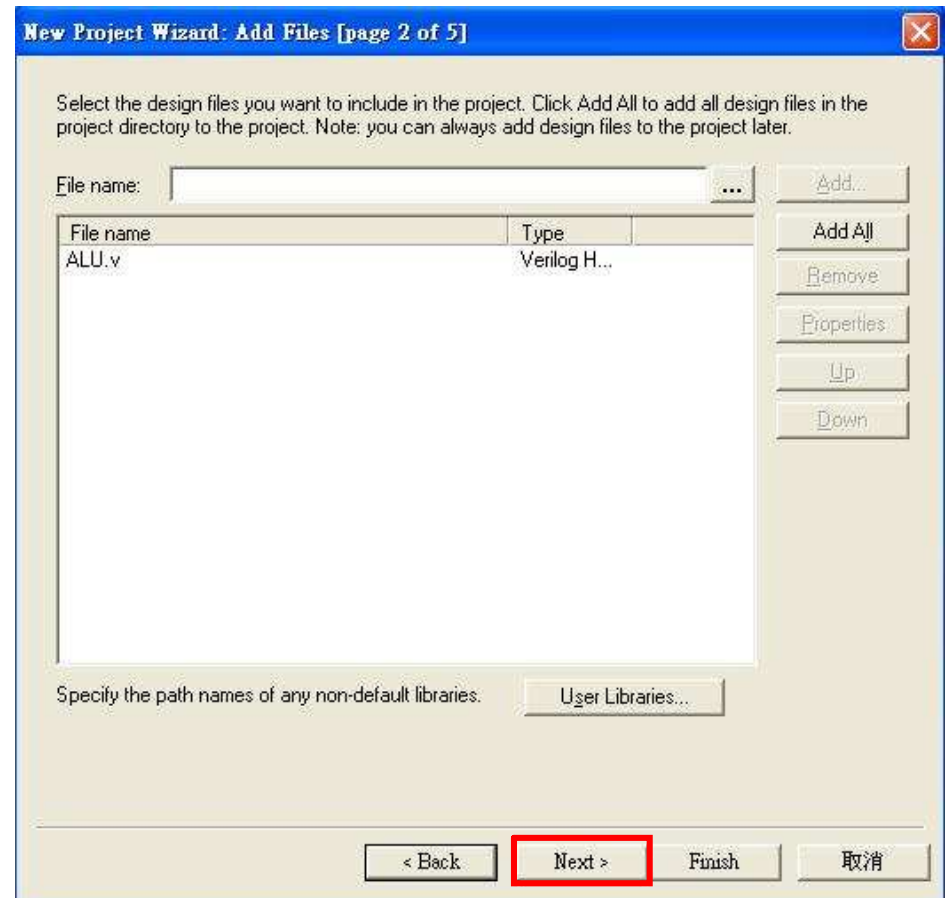
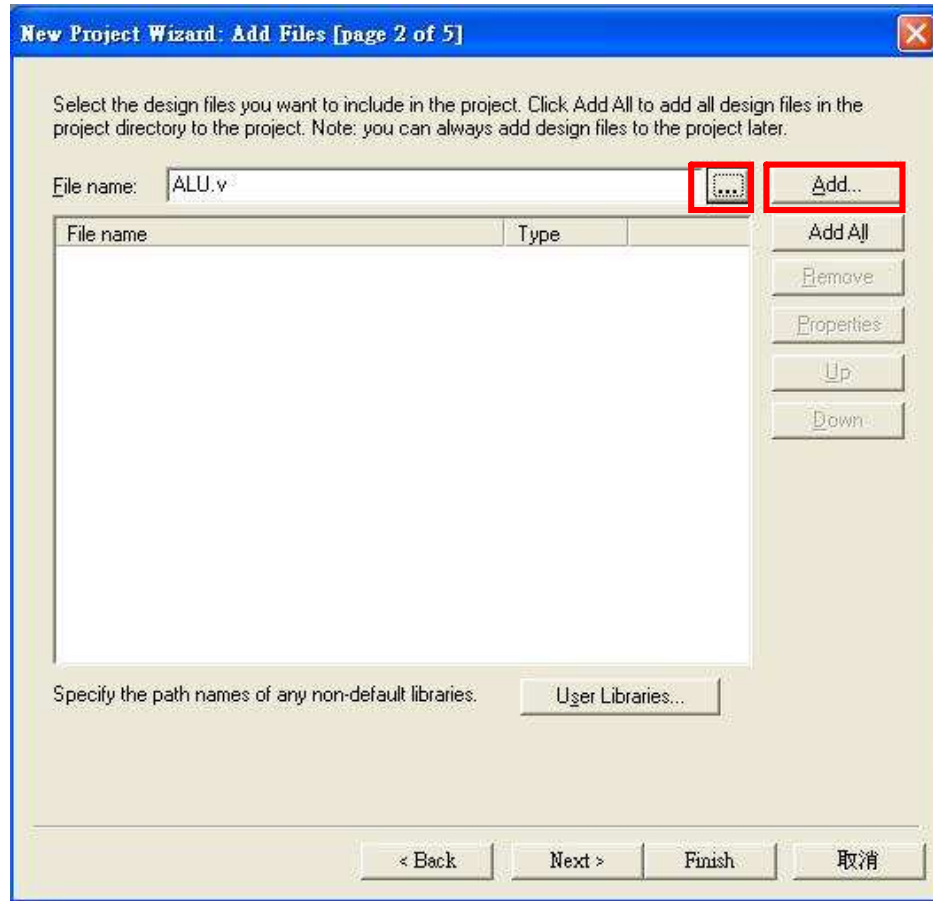
## ➤ Open new project wizard.



## ➤ Specify the directory and the name of the project.



➤ **Select design files and source files. Or click “Next” to skip this step.**



## ➤ Specify device settings.

**New Project Wizard: Family & Device Settings [page 3 of 5]**

Select the family and device you want to target for compilation.

Family: **Stratix**

Target device:

- ☐ Auto device selected by the Filter
- ☒ Specific device selected in 'Available devices' list

Show in 'Available device' list:

Package: **Any**

Pin count: **780**

Speed grade: **6**

Core voltage: 1.5V

☒ Show advanced devices

☐ HardCopy compatible only

Available devices:

Name	LEs	Memor...	DSP	PLL	DLL
<b>EP1S10F780C6</b>	10570	920448	6	6	2
EP1S10F780C6ES	10570	920448	6	6	2
EP1S10F780I6	10570	920448	6	6	2
EP1S20F780C6	18460	1669248	10	6	2
EP1S20F780I6	18460	1669248	10	6	2
EP1S25F780C6	25660	1944576	10	6	2
EP1S25F780I6	25660	1944576	10	6	2
EP1S30F780C6	32470	3317184	12	6	2
EP1S30F780C6 HARD	32470	2137536	12	6	2

Companion device:

HardCopy II:

☒ Limit DSP & RAM to HardCopy II device resources.

< Back **Next >** Finish 取消

➤ Specify other EDA tools. Here you can click “Next” to skip this step since we don’t use other EDA tools.

New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

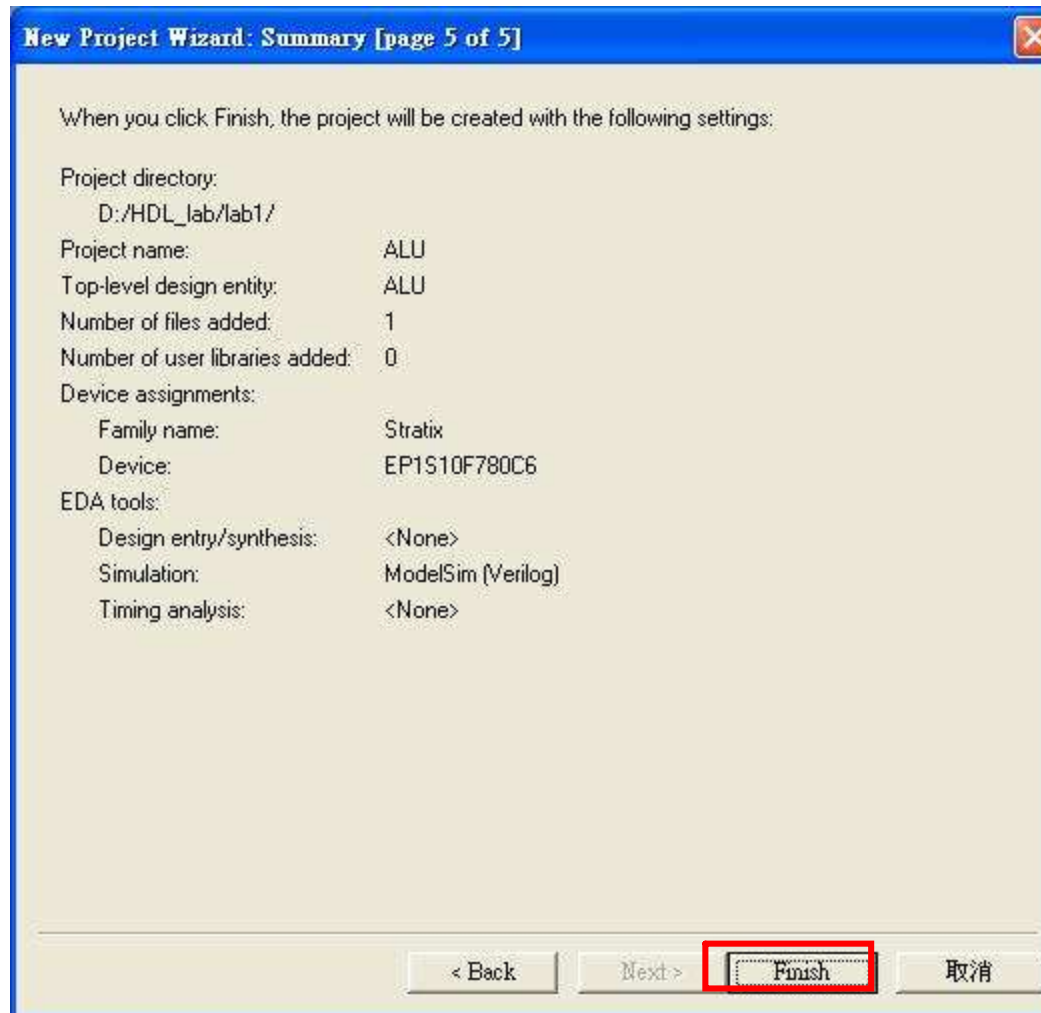
☐ EDA design entry/synthesis tool: [ ]  
Format: [ ]  
☐ Not available

☒ EDA simulation tool: ModelSim  
Format: Verilog  
☐ Run Gate Level Simulation automatically after compilation

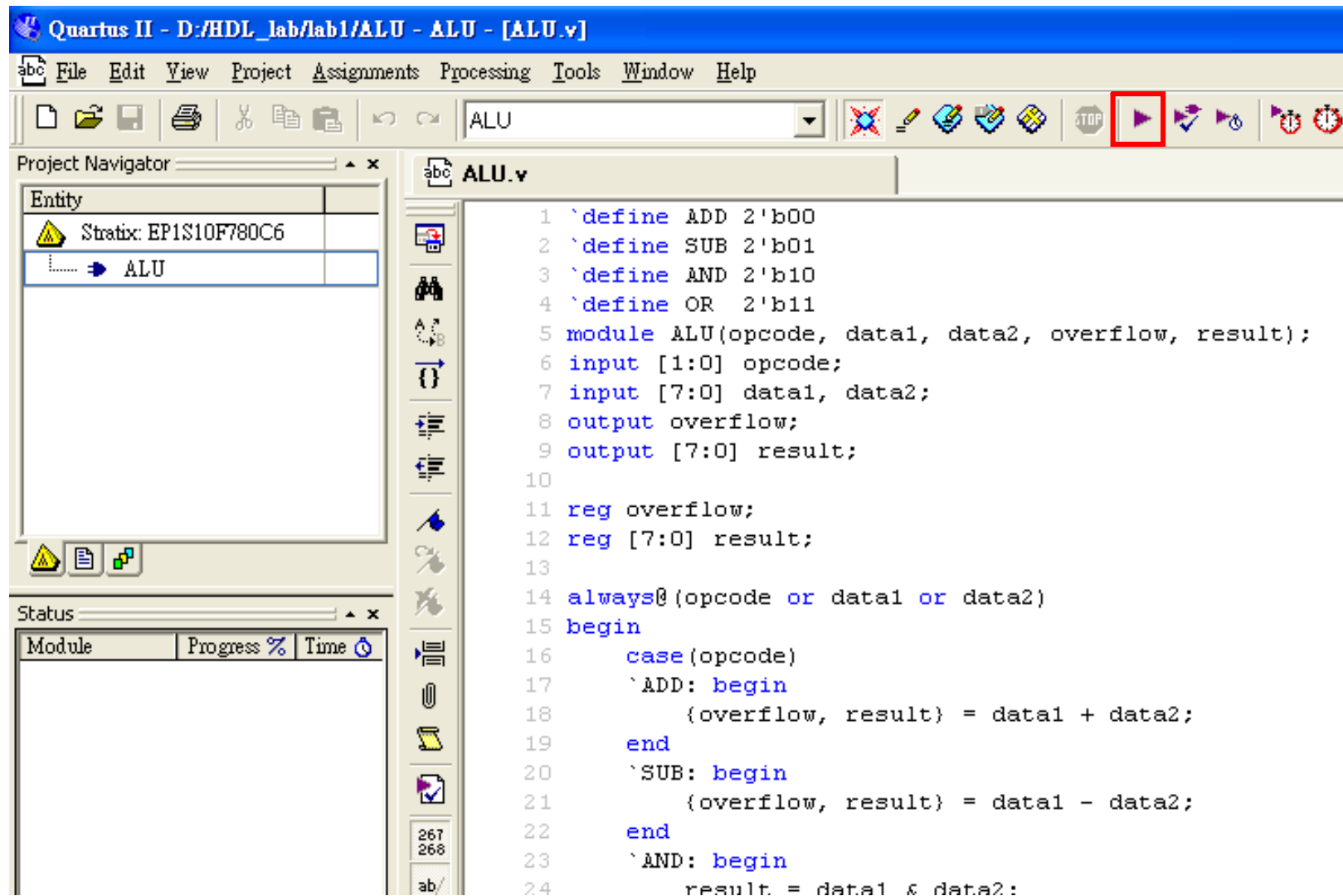
☐ EDA timing analysis tool: [ ]  
Format: [ ]  
☐ Not available

< Back Next > Finish 取消

➤ Click “Finish”, and the new project will be created with the specified settings.



## ➤ Start compilation.





## ➤ Compilation result.

The screenshot displays the Quartus II compilation results. The main window shows the 'Flow Summary' tab, which lists the compilation steps and their progress. A red box highlights the 'Status' window, which shows the progress of each module. The 'Status' window is a table with two columns: 'Module' and 'Progress %'. The 'Flow Summary' window is a list of compilation steps, including 'Compilation Report', 'Legal Notice', 'Flow Summary', 'Flow Settings', 'Flow Non-Default Global Settings', 'Flow Elapsed Time', 'Flow Log', 'Analysis & Synthesis', 'Partition Merge', 'Fitter', 'Assembler', 'Timing Analyzer', and 'EDA Netlist Writer'. The 'Status' window shows that all modules have reached 100% progress.

Module	Progress %
Full Compilation	100 %
Analysis & Synthesis	100 %
Partition Merge	100 %
Fitter	100 %
Assembler	100 %
Classic Timing Analyzer	100 %
EDA Netlist Writer	100 %

The 'Flow Summary' window shows the following steps:

- Compilation Report
- Legal Notice
- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow Log
- Analysis & Synthesis
- Partition Merge
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer

The 'Status' window shows the following progress:

Module	Progress %
Full Compilation	100 %
Analysis & Synthesis	100 %
Partition Merge	100 %
Fitter	100 %
Assembler	100 %
Classic Timing Analyzer	100 %
EDA Netlist Writer	100 %

The 'Flow Summary' window also displays the following information:

- Flow Status
- Quartus II Version
- Revision Name
- Top-level Entity Name
- Family
- Device
- Timing Models
- Met timing requirements

A message box titled 'Quartus II' displays the following text:

Full Compilation was successful (2 warnings)

The message box includes a '確定' (OK) button.

➤ Get the post-layout gate-level netlist. Rename your\_design.vo to your\_design.v for simulation.

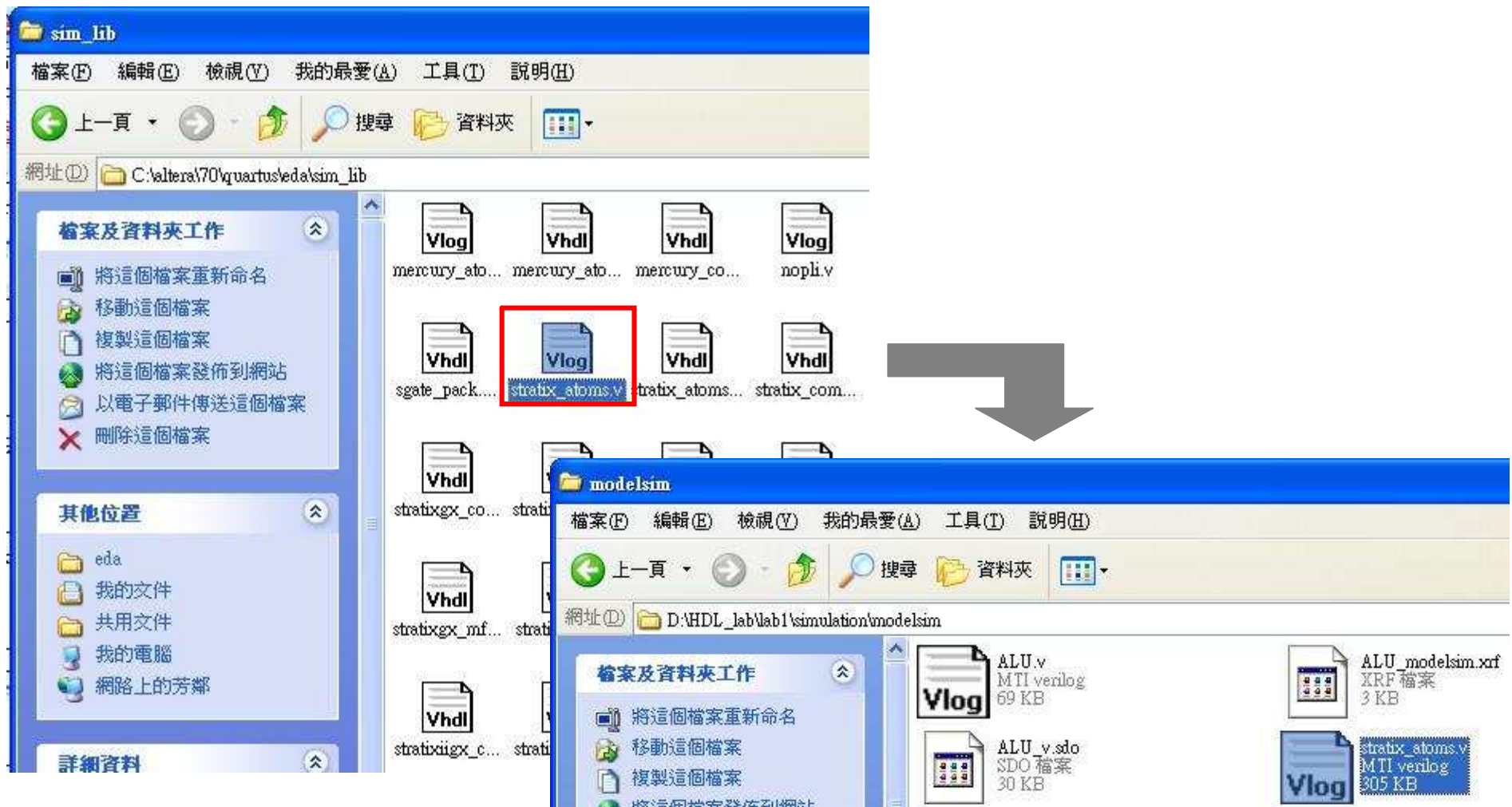


➤ Prepare to post-layout simulation.

Copy file

(\\%your\_quartus\_dir\eda\sim\_lib\stratix\_atoms.v)

to your project directory

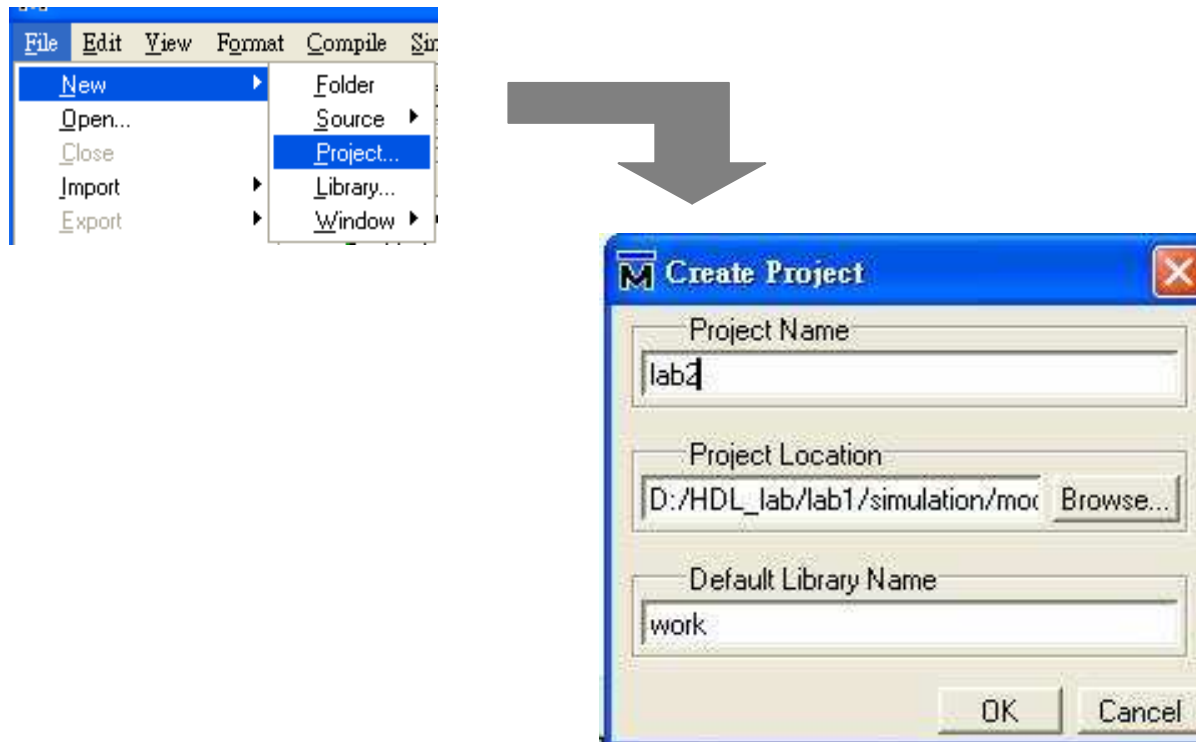


➤ Copy your testbench and testing data to your project directory.



Using ModelSim

## ➤ Open modelSim and create a project.

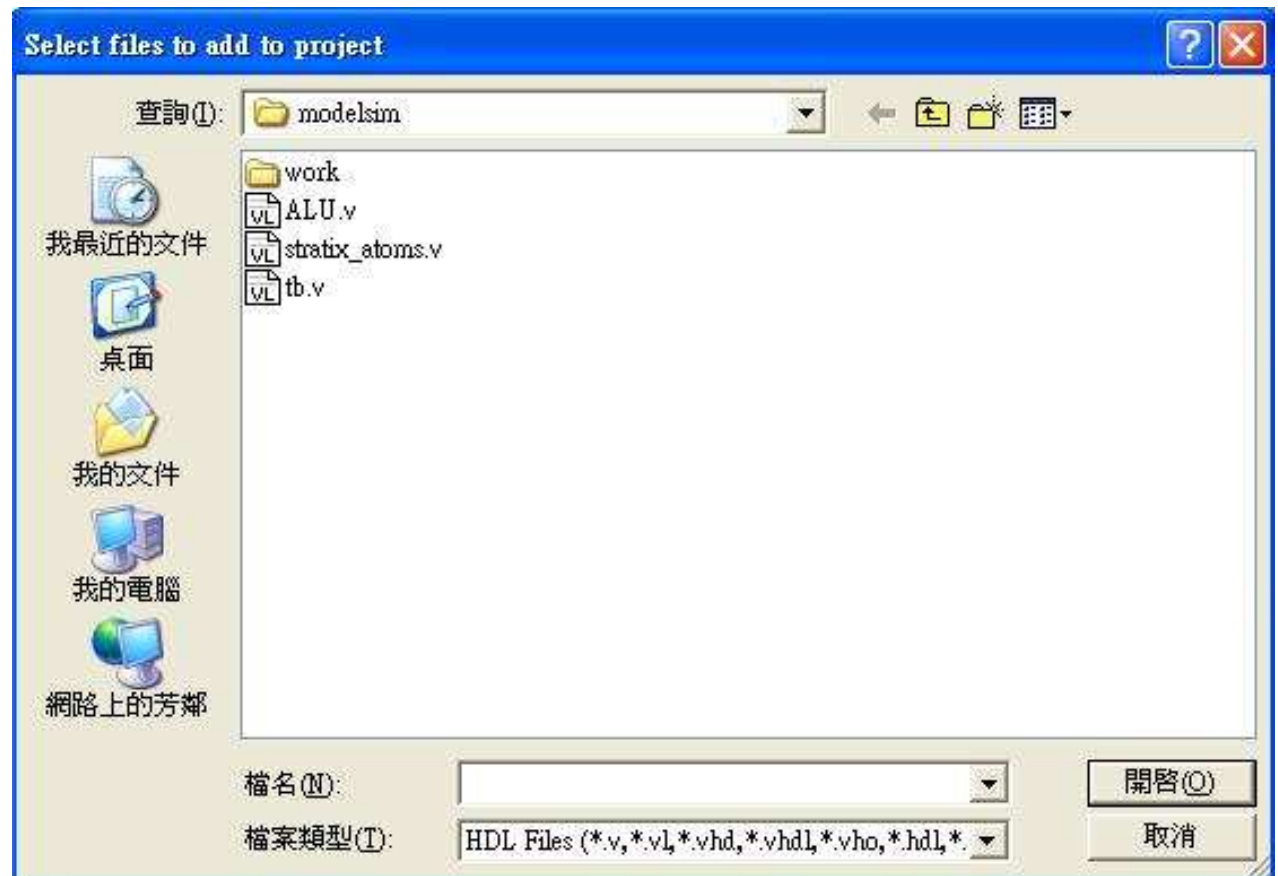


## ➤ Add files to project.



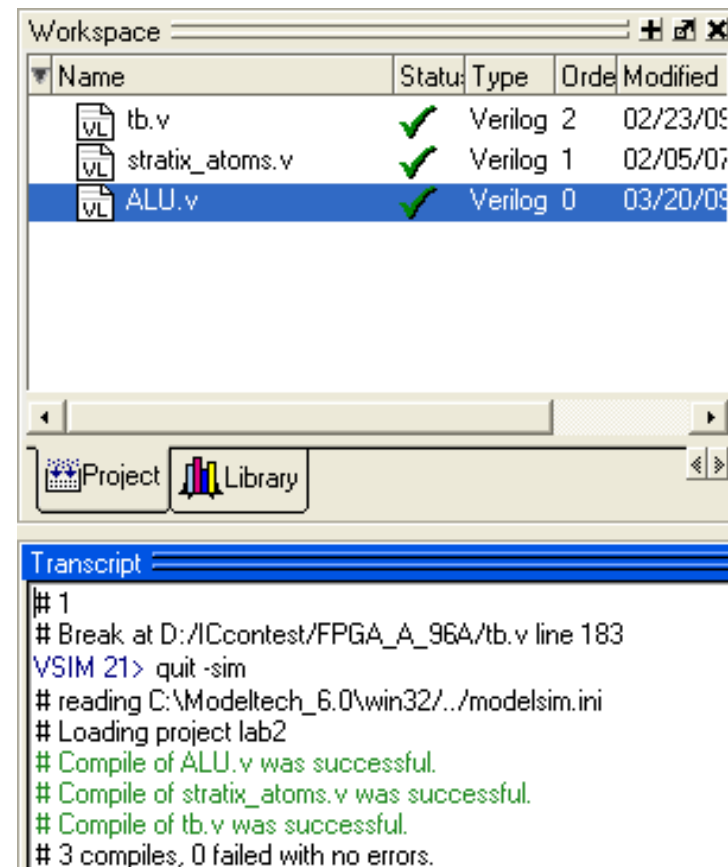
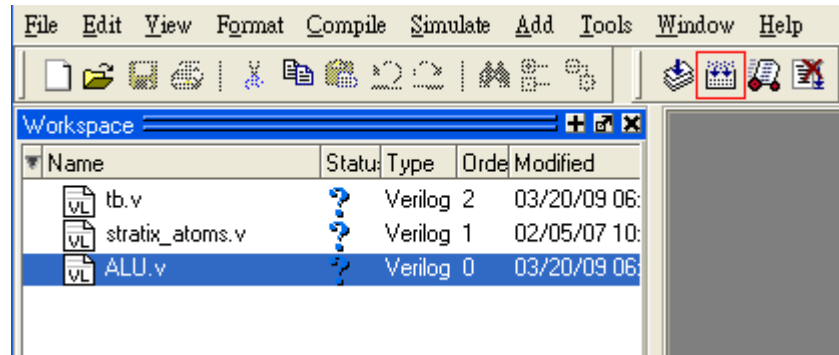
Pre-simulation: before synthesis

Post-simulation: after synthesis



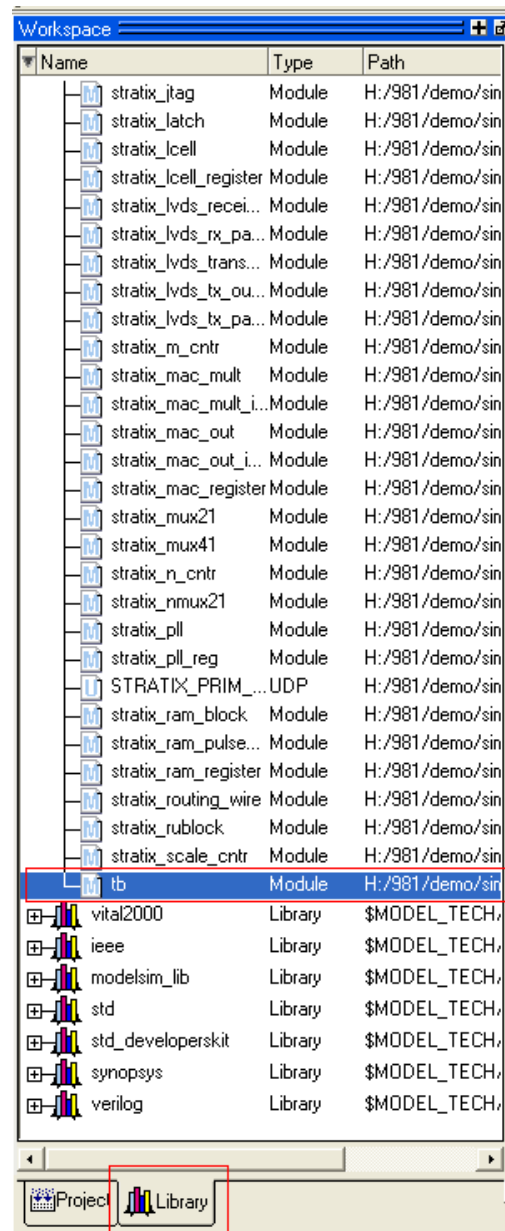


➤ **Compilation.** And the following simulation steps is the same with RTL simulation.



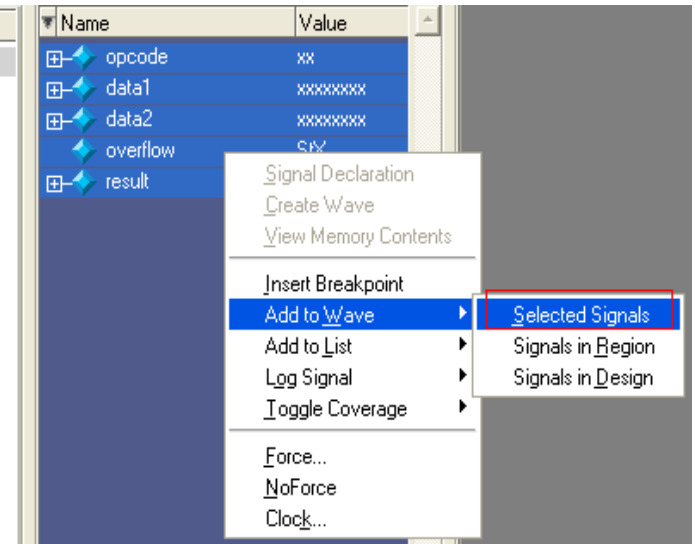


# ➤ Simulation.

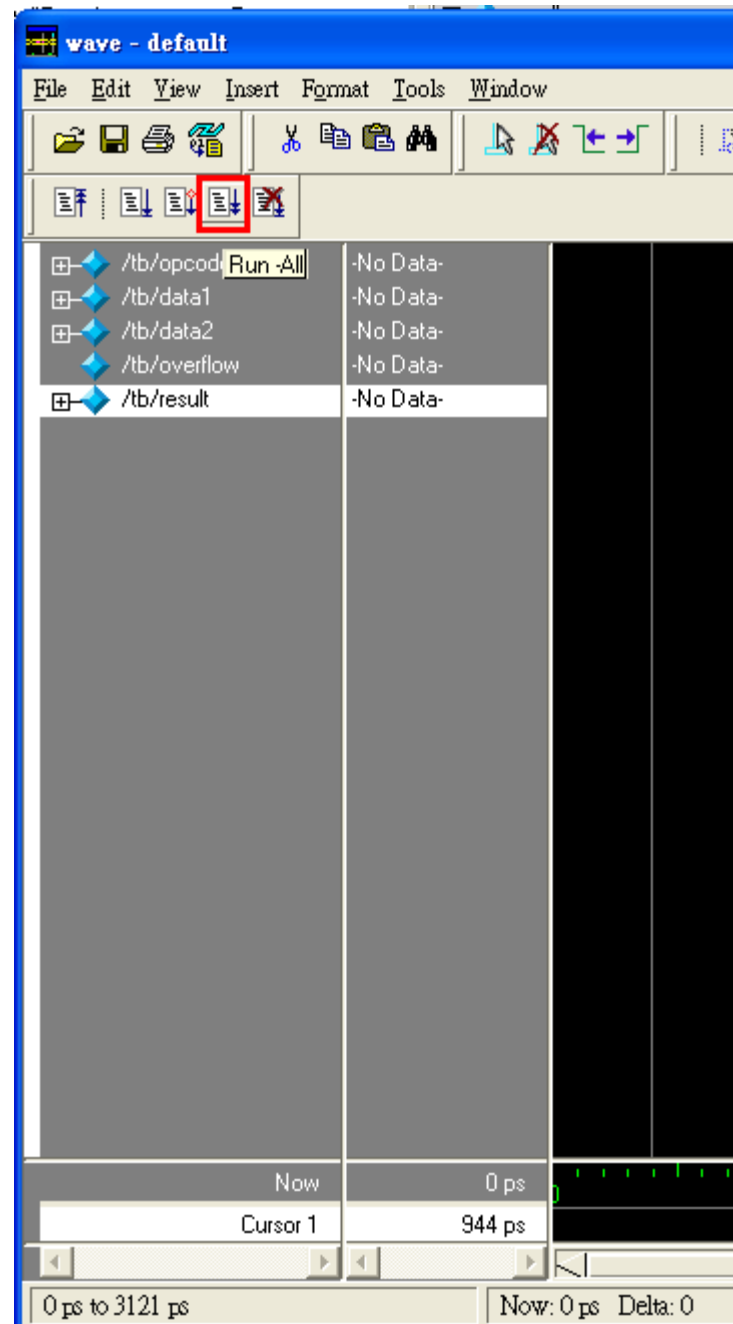


左鍵點兩下

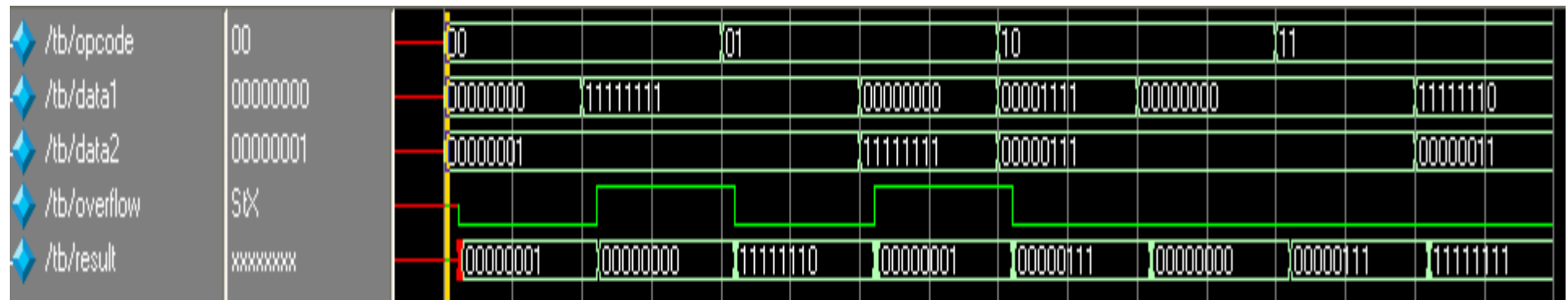
Instance	Design unit	Design unit type
tb	tb	Module
ALUtb	ALU	Module
#IMPLICIT-WIR...	tb	Process
#IMPLICIT-WIR...	tb	Process
#IMPLICIT-WIR...	tb	Process
#INITIAL#11	tb	Process



## ➤ Simulation.












## ➤ The Post-simulation waveform








## ➤ Compare with the waveform of RTL simulation

RTL simulation

  /b/opcode	-No Data-		00		01		10		11	
  /b/data1	-No Data-		00000000	11111111		00000000	00001111	00000000		11111110
  /b/data2	-No Data-		00000001			11111111	00000111			00000011
 /b/overflow	-No Data-									
  /b/result	-No Data-		00000001	00000000	11111110	00000001	00000111	00000000	00000111	11111111

Post-layout gate-level simulation

 /b/opcode	00		00		01		10		11	
 /b/data1	00000000		00000000	11111111		00000000	00001111	00000000		11111110
 /b/data2	00000001		00000001			11111111	00000111			00000011
 /b/overflow	StX									
 /b/result	xxxxxxx		00000001	00000000	11111110	00000001	00000111	00000000	00000111	11111111

Settings - traffic\_light



Category:

- General
- Files
- User Libraries (Current Project)
- Device
- + Operating Conditions
- + Compilation Process Settings
- EDA Tool Settings
  - Design Entry/Synthesis
  - Simulation
  - Timing Analysis
  - Formal Verification
  - Physical Synthesis
  - Board-Level
- + Analysis & Synthesis Settings
- + Filter Settings
- + Timing Analysis Settings
  - Assembler
  - Design Assistant
  - SignalTap II Logic Analyzer
  - Logic Analyzer Interface
- Simulator Settings
  - Simulation Power
- PowerPlay Power Analyzer Settings

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim

☐ Run gate-level simulation automatically after compilation

EDA Netlist Writer options

Format for output netlist: Verilog

Time scale: 1 ns

Output directory: simulation/modelsim

☐ Map illegal HDL characters

☐ Enable glitch filtering

Options for Power Estimation

☐ Generate Value Change Dump (VCD) file script

Script Settings...

Design instance name: it

More Settings...

NativeLink settings

☒ None

☐ Compile test bench:

Test Benches...

☐ Use script to set up simulation:

☐ Script to compile test bench:

Reset

OK

Cancel