

# Design Compiler

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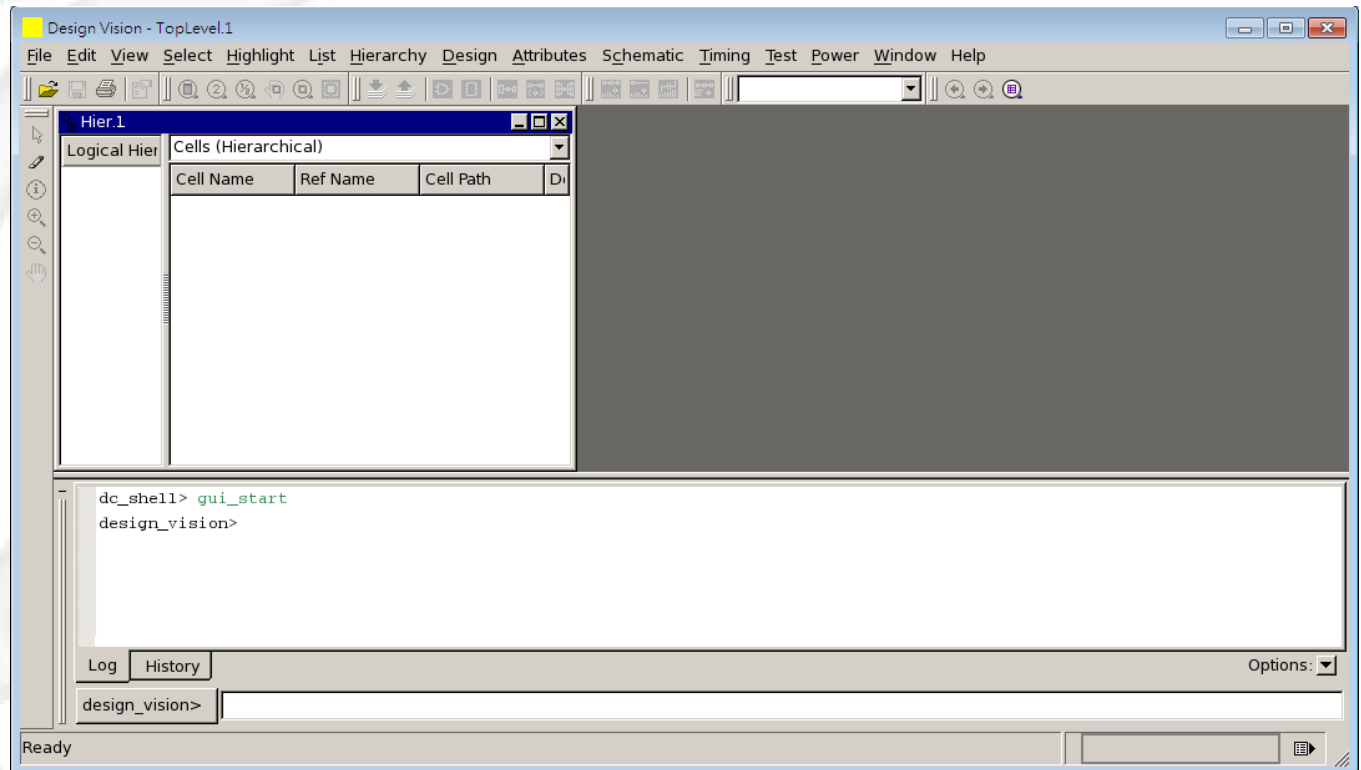
TA : Kiwi, Kevin

Date : 2010/09/16

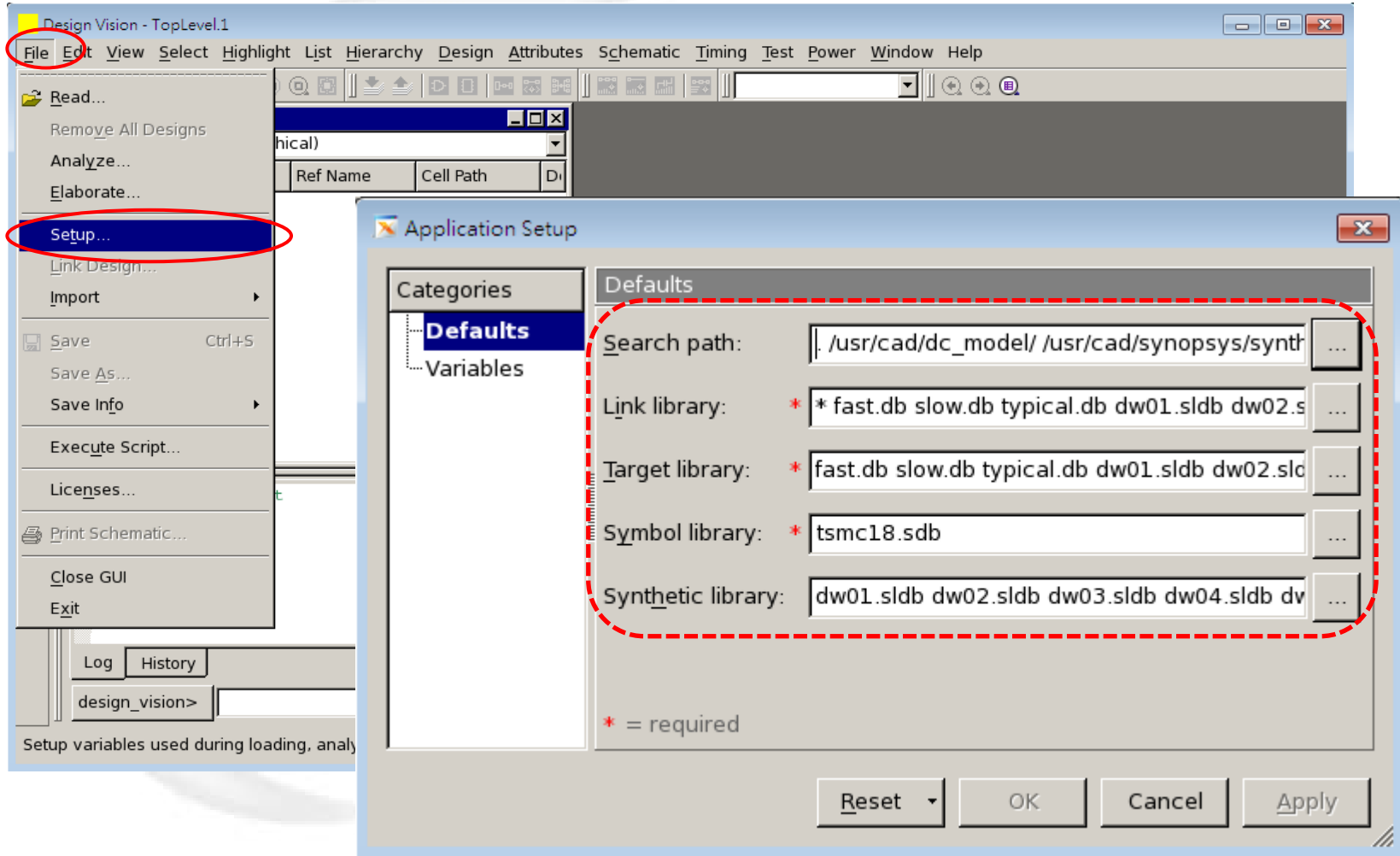


# Start to Design Compiler

□ dv &



# Setup libraries (1/2)





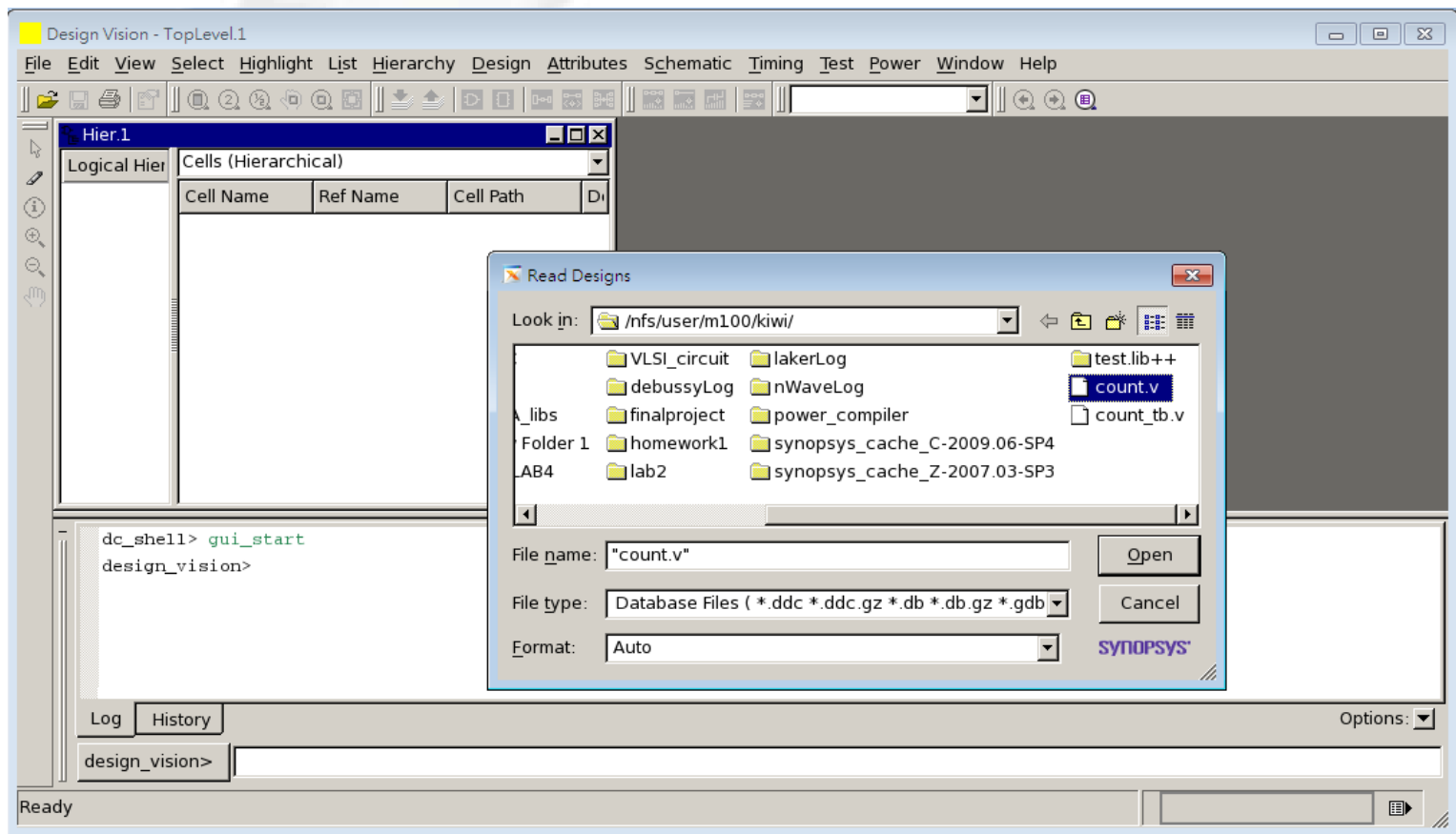
# Setup libraries (2/2)

❑ **.synopsys\_dc.setup** is a setup file when entering Design Vision

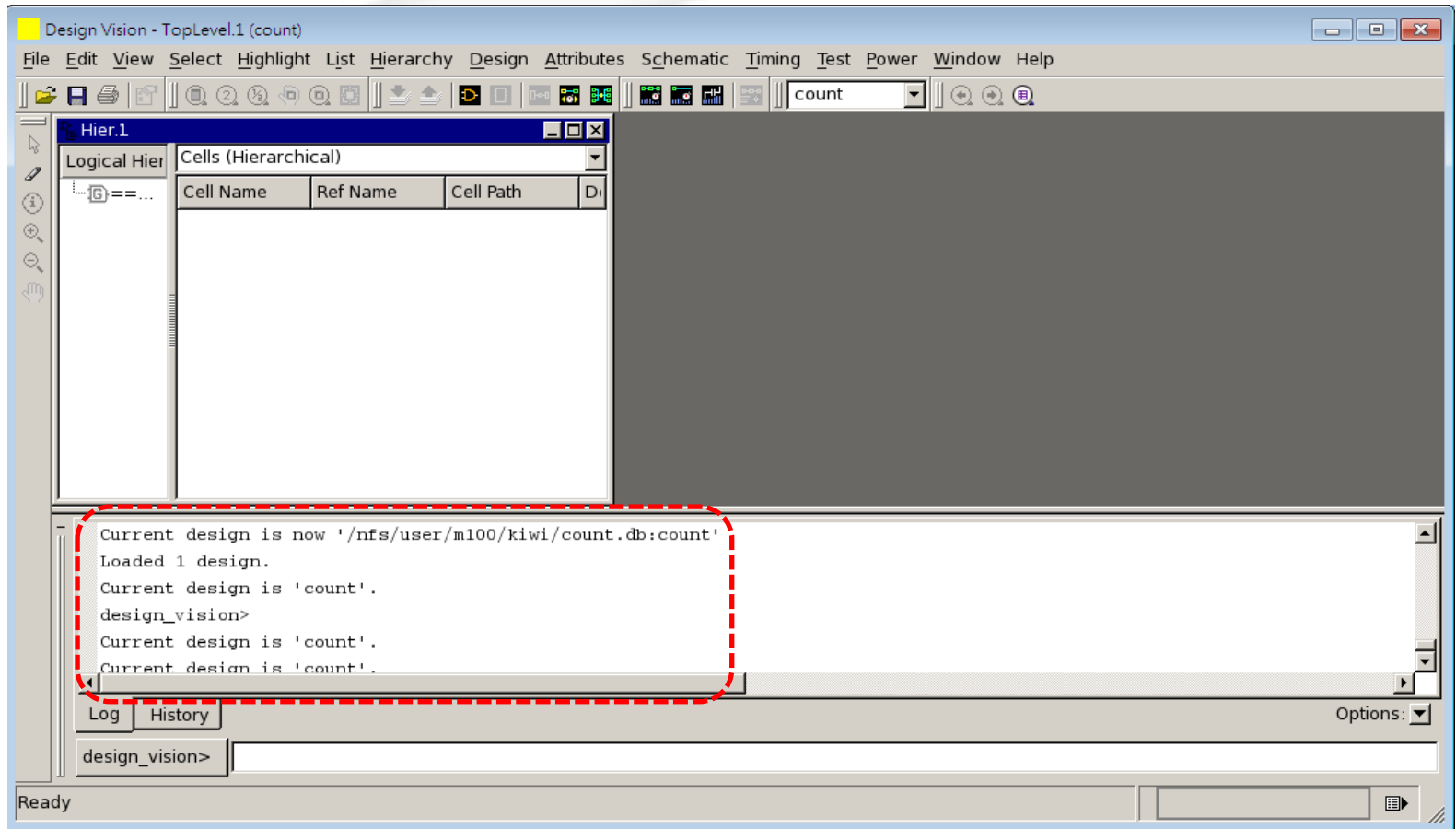
- set company "NCKU"
- set designer "your name"
- set search\_path  
"/usr/cad/CBDK018\_TSMC\_Artisan/CIC/SynopsysDC/db"
- set target\_library "fast.db slow.db"
- set link\_library "\$target\_library"
- set symbol\_library "tsmc18.sdb"
- set\_min\_lib slow.db -min fast.db ;      # for core lib
- set verilogout\_no\_tri true
- set hdlin\_enable\_presto\_for\_vhdl "TRUE"
- set sh\_enable\_line\_editing true
- history keep 100
- alias h history

# Read file

File > Read

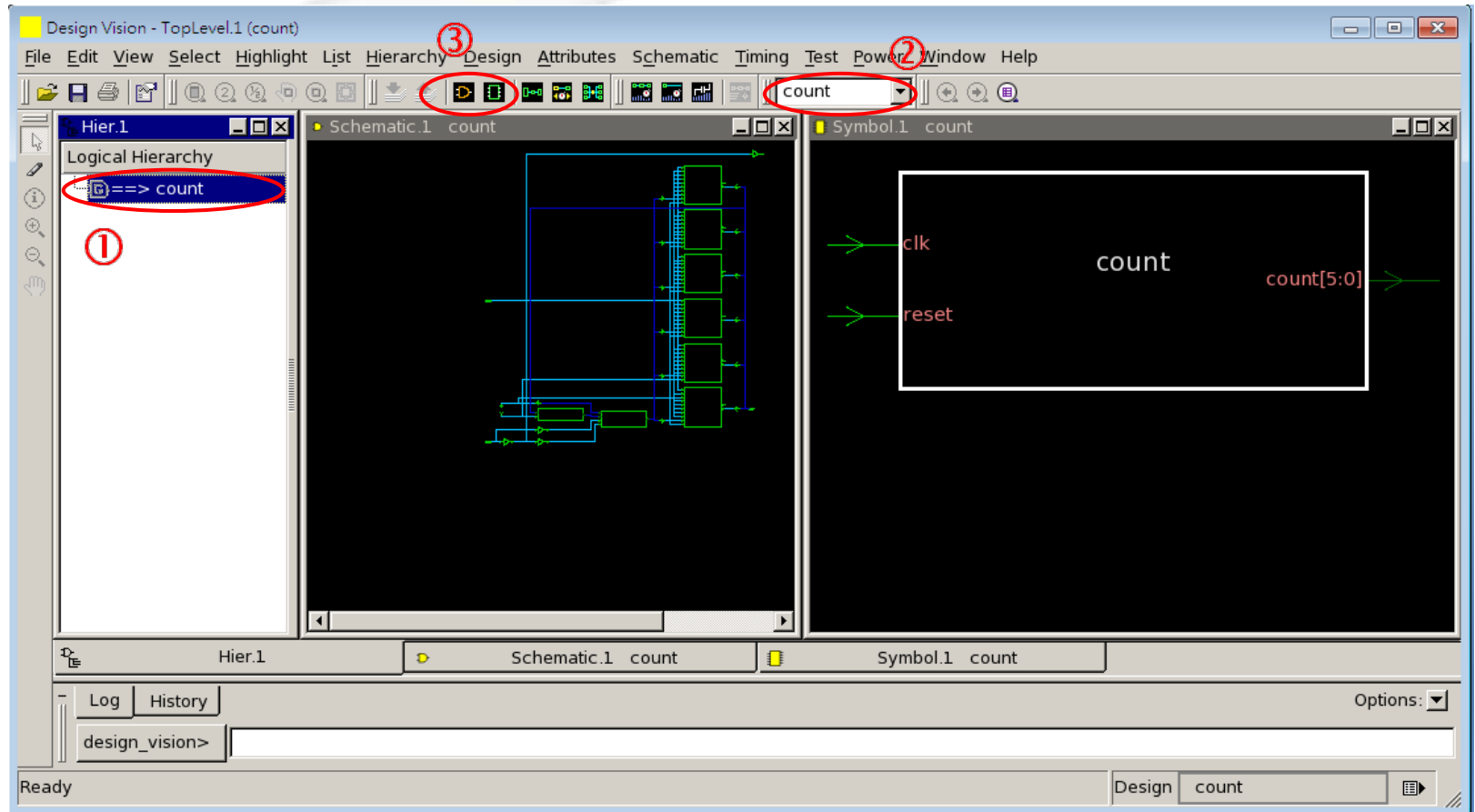


# Read File Check



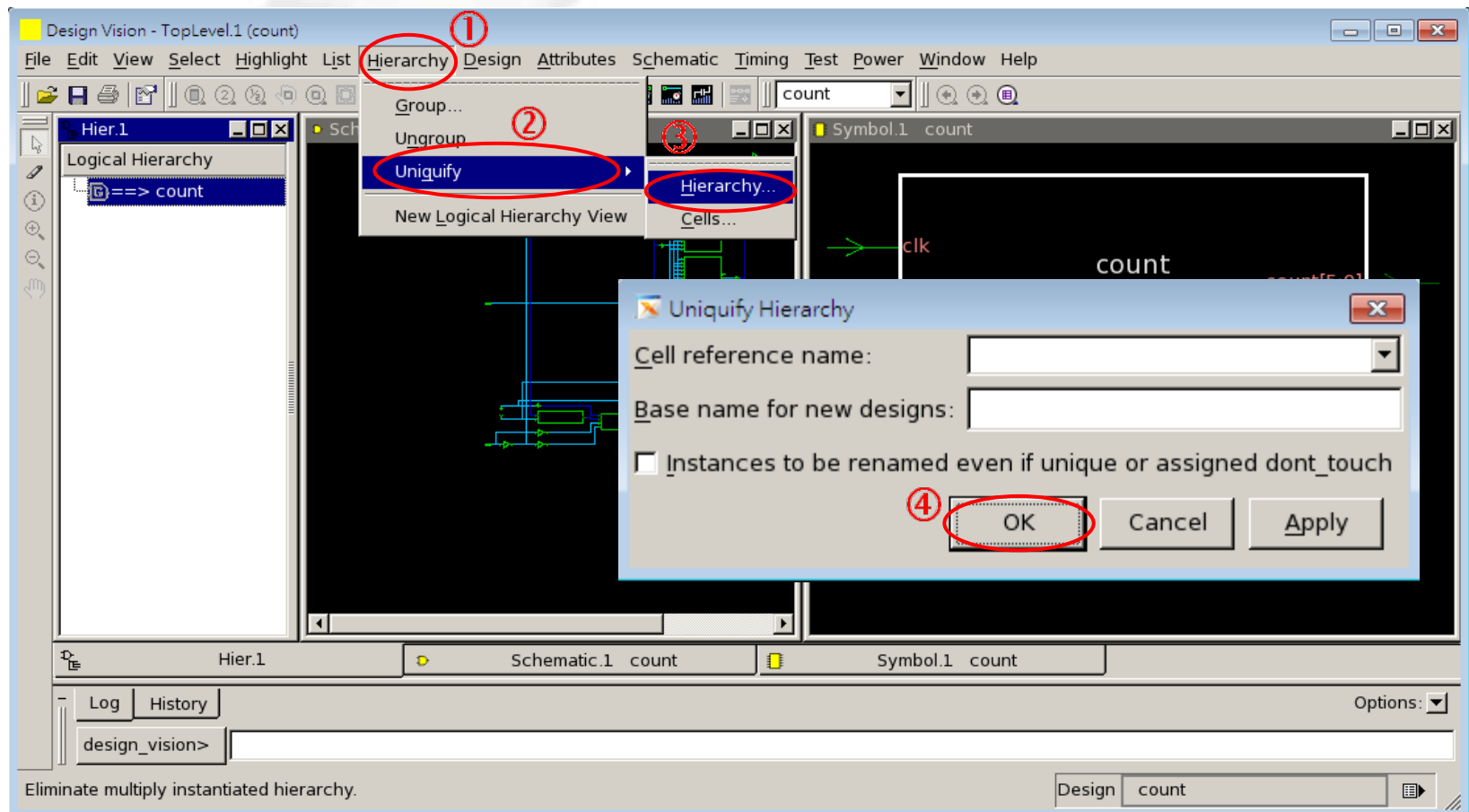
If any errors or warnings exist, you should modify your codes to avoid them.

# Symbol and Schematic View



# Uniquify

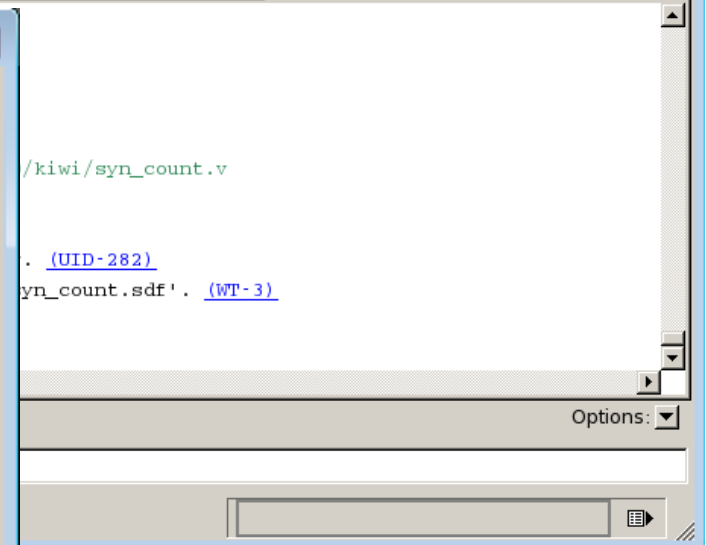
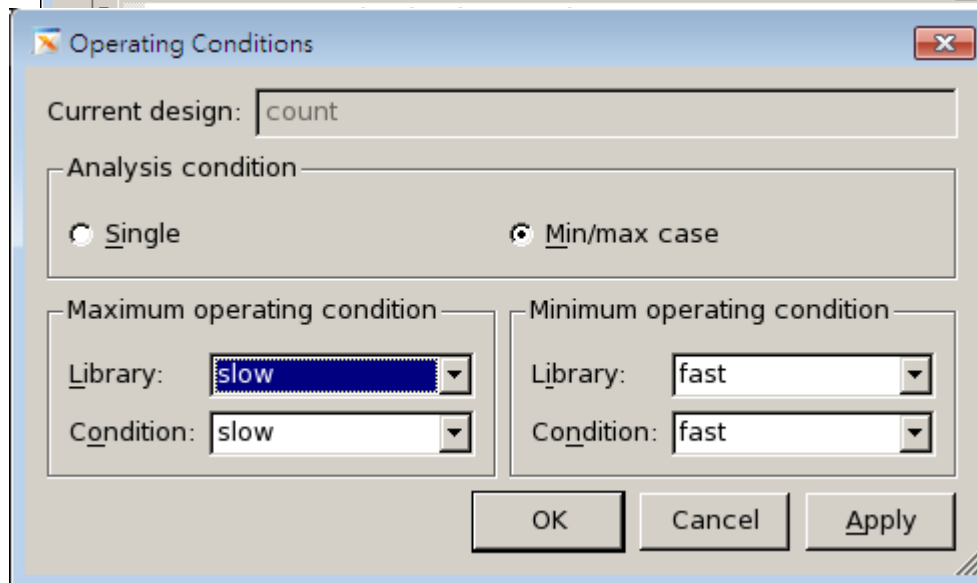
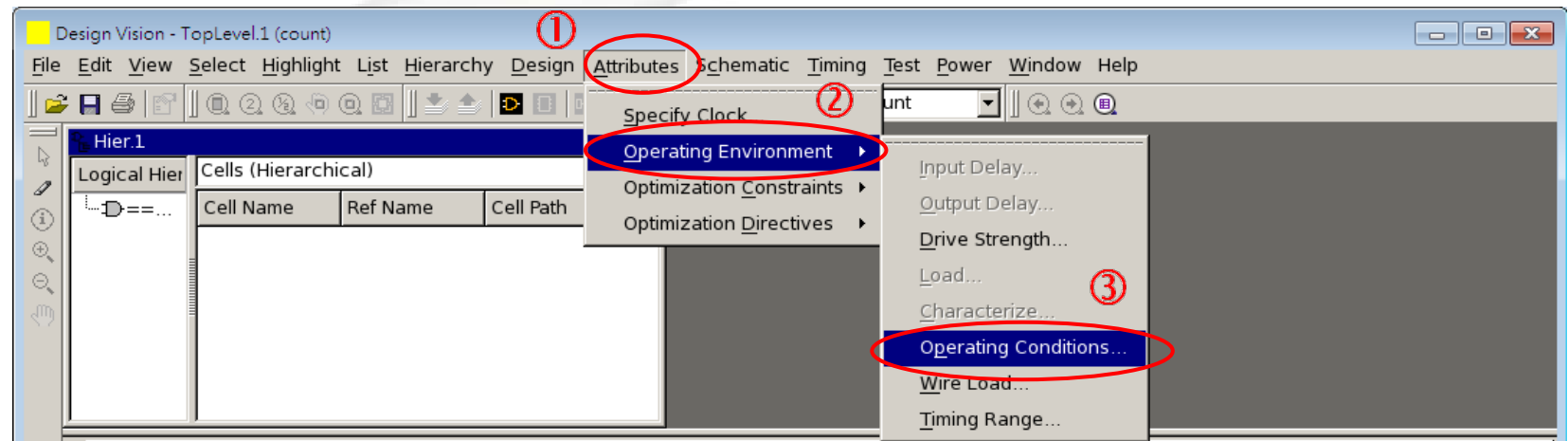
- ❑ Hierarchy > Uniquify > Hierarchy
- ❑ Objective: Solving 『multiple design instance』 problem.





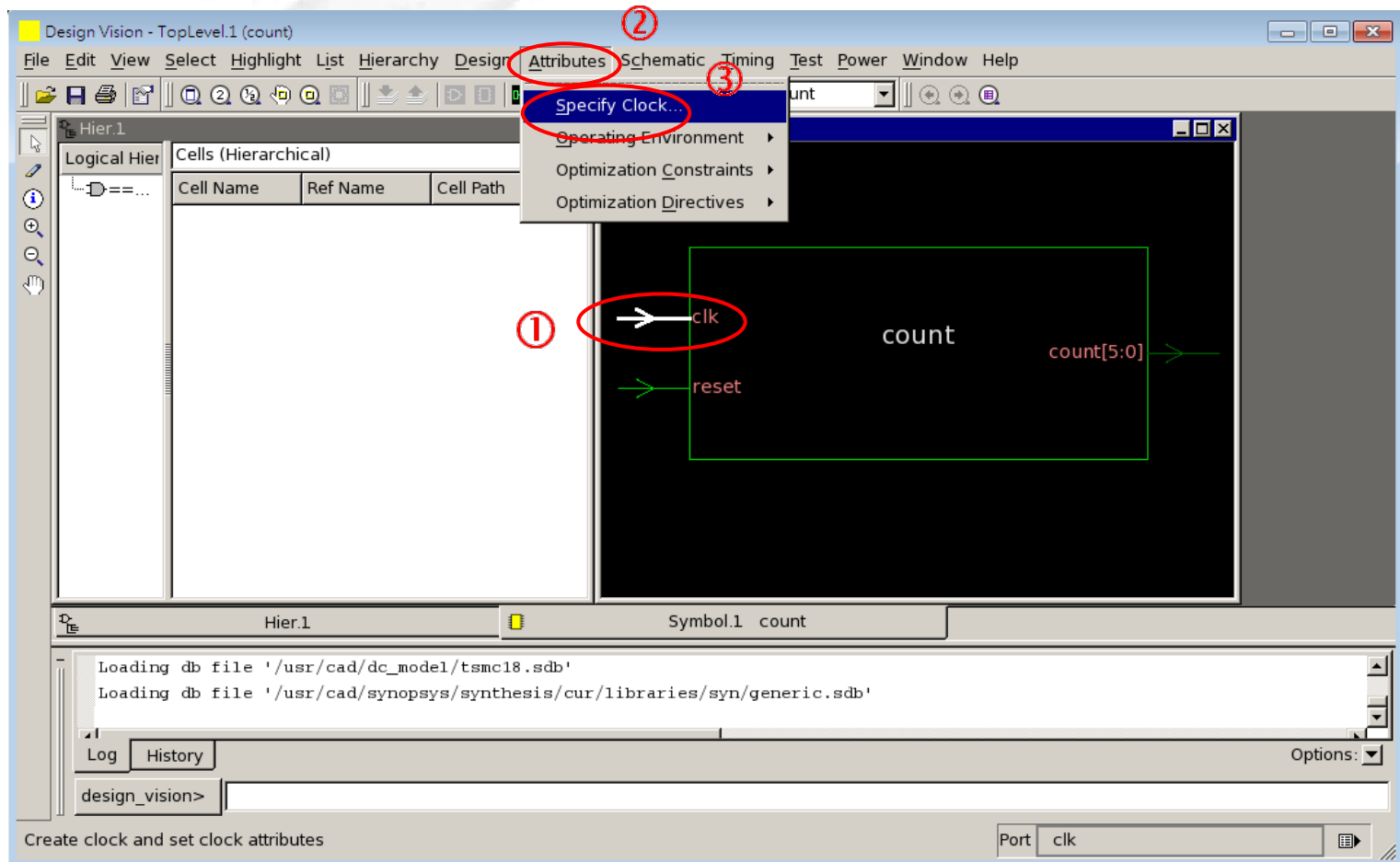
# Operating Environment

## Attributes > Operating Environment > Operation Conditions



# Constraint : Clock (1/2)

1. In the symbol view
2. Choose the clock
3. Attributes > Specify Clock



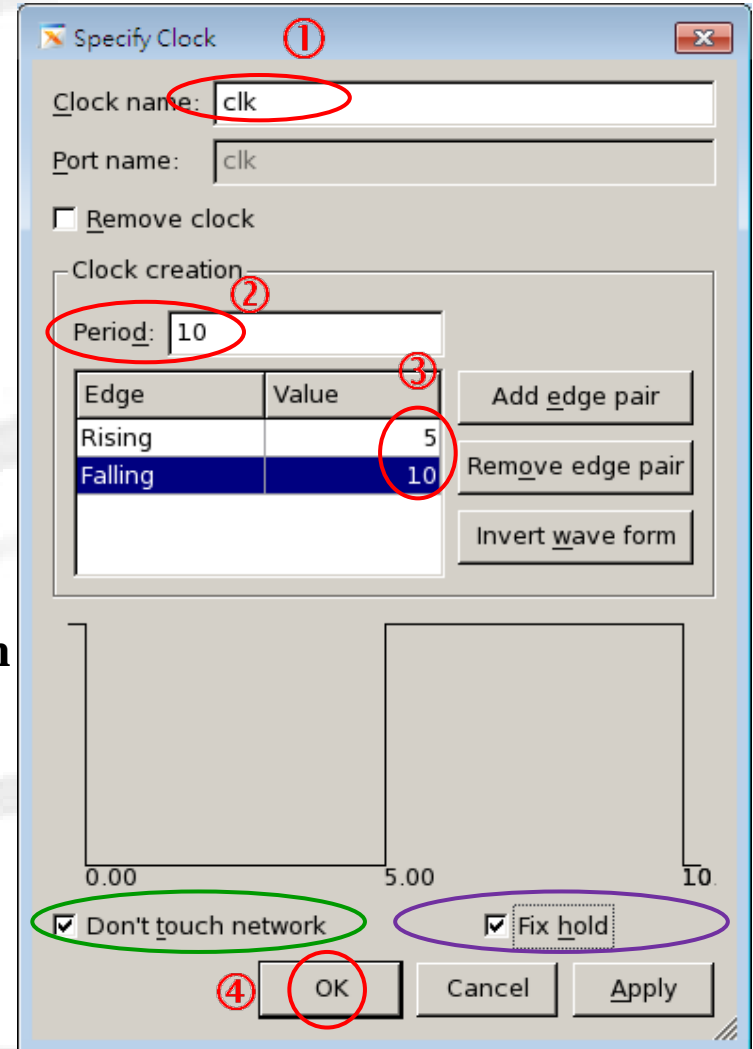
# Constraint : Clock (2/2)

## □ Don't touch network:

The command preserves the nets attached to one or more clock sources during optimization.

## □ Fix hold:

The command directs Design Compiler to insert delay to correct hold(minimum path) violations for timing paths that end at registers fed by this clock.



The image shows the 'Specify Clock' dialog box in a design tool. It contains the following elements:

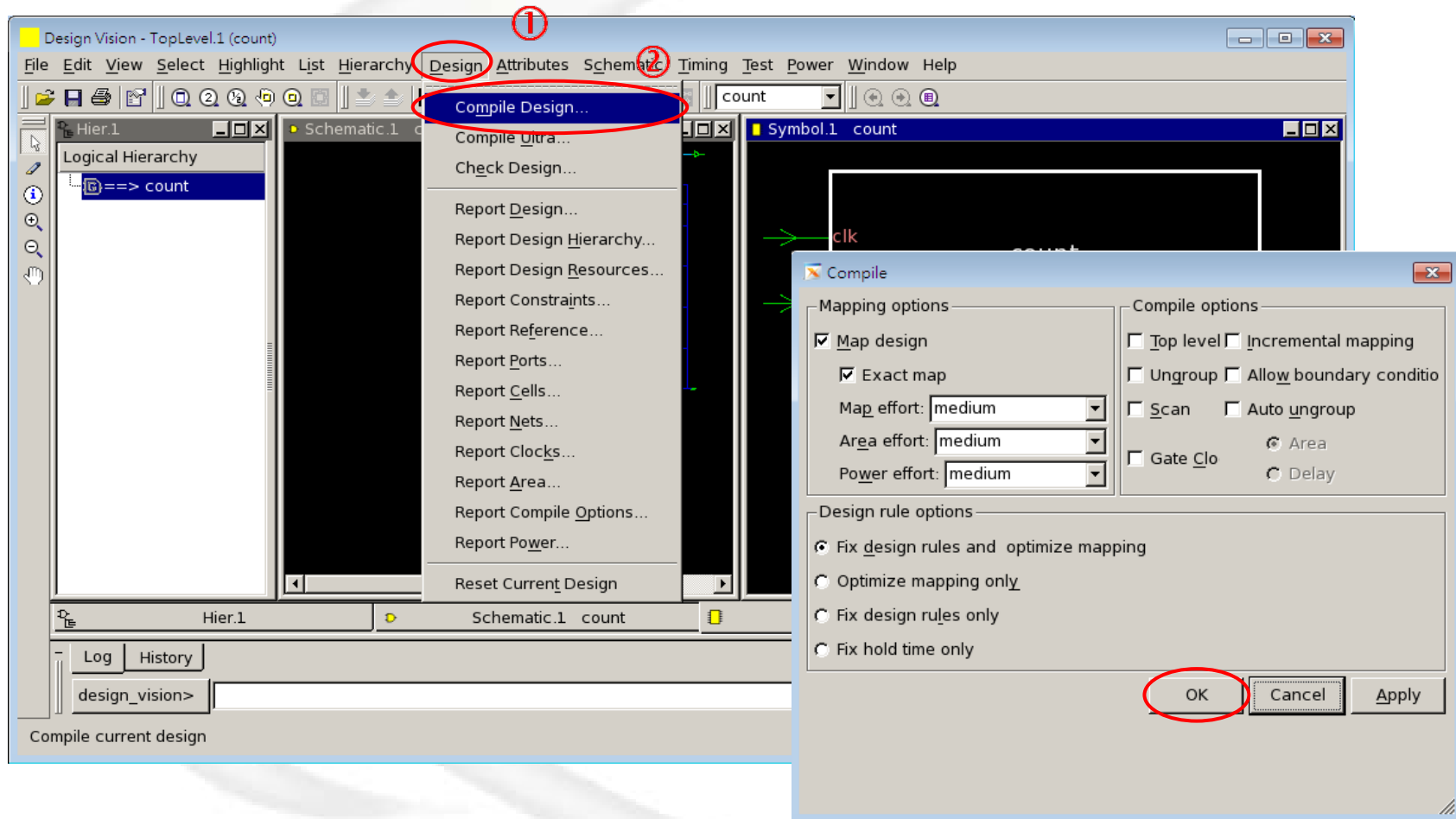
- 1** Clock name: clk
- Port name: clk
- ☐ Remove clock
- 2** Clock creation section:
  - 3** Period: 10
  - Table with 2 columns: Edge, Value

Edge	Value
Rising	5
Falling	10

- Buttons: Add edge pair, Remove edge pair, Invert wave form
- Graph area with x-axis labels: 0.00, 5.00, 10.
- ☒ Don't touch network
- ☒ Fix hold
- 4** OK, Cancel, Apply buttons

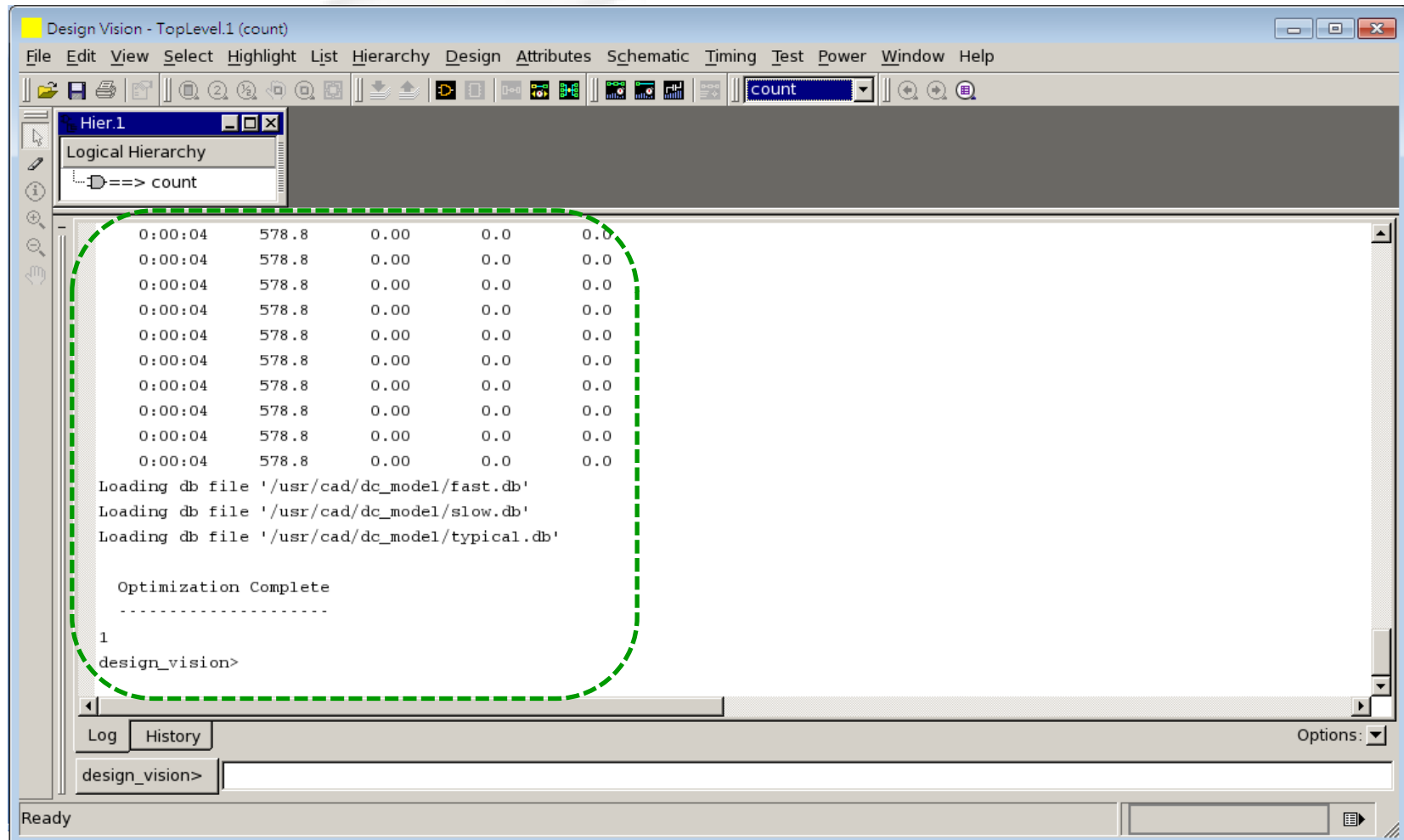
# Compile Your Design

## □ Design > Compile Design



# Check Compile Log

- ❑ If any errors or warnings exist, which be shown in this window.





# Timing Report (1/2)

## □ Timing > Report timing Paths

The screenshot shows the Design Vision software interface. The main window is titled "Design Vision - TopLevel.1 (count)". The menu bar includes File, Edit, View, Select, Highlight, List, Hierarchy, Design, Attributes, Schematic, Timing, Test, Power, Window, and Help. The Timing menu is open, showing options like Path Inspector, Timing Analysis Driver, Path Slack..., Endpoint Slack..., Net Capacitance..., Path Profile View, Check Timing..., Report Timing Path..., Report Timing Requirements..., Report Clock Skew..., Report Clock Tree..., Report Path Group..., and Report Wire Load....

The "Report Timing Paths" dialog box is open, showing the following options:

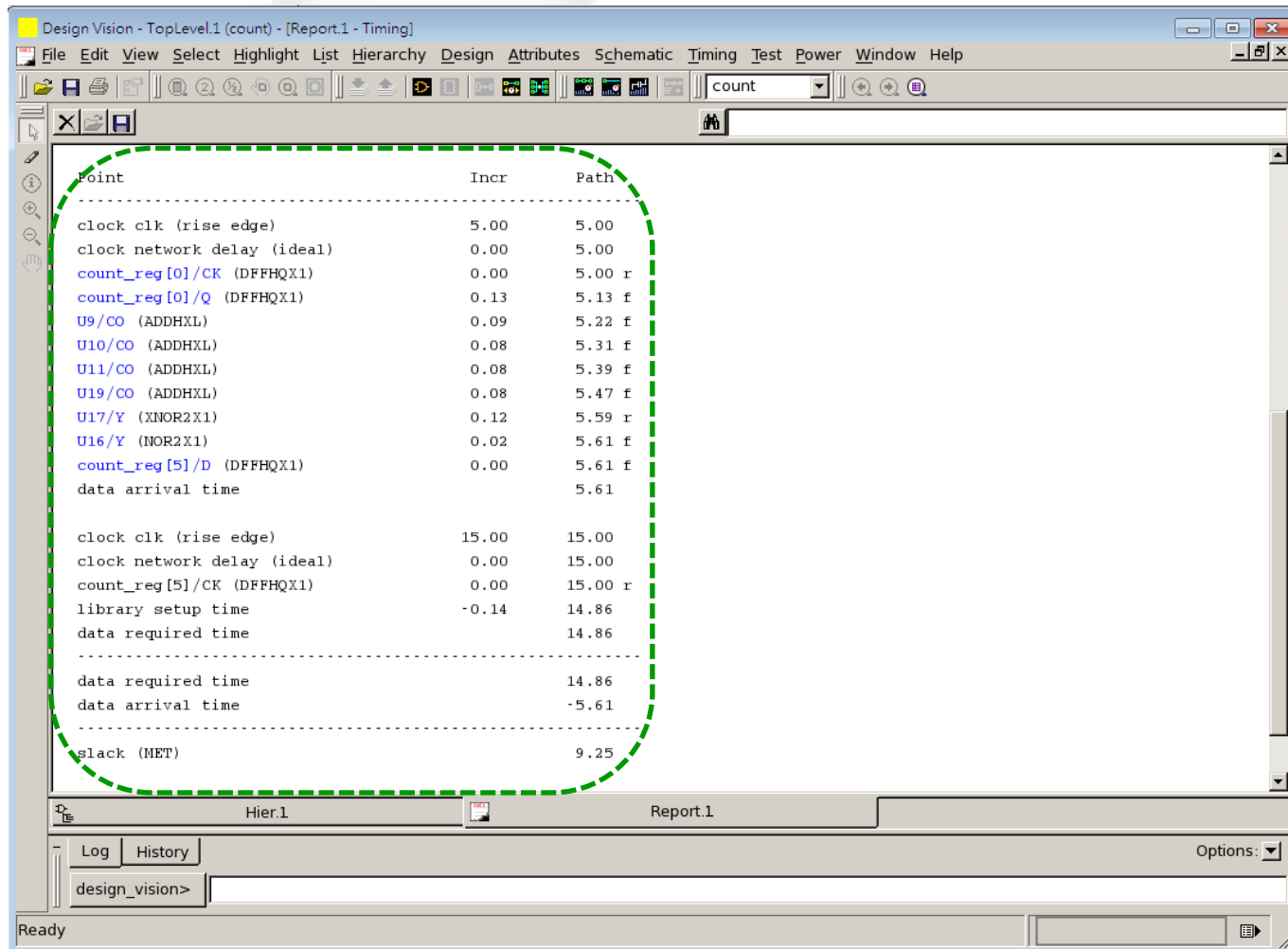
- From: pin (Selection[1])
- Through: pin (Selection[2])
- To: pin (Selection[3])
- Report options:
  - Worst paths per endpoint: 1
  - Maximum path delay: [ ]
  - Max paths per group: 1
  - Minimum path delay: [ ]
  - Path type: full
  - Delay type: max
  - Sort by: group
  - Significant digits: 2
  - Path delay threshold: 0
  - ☐ Report timing loops
  - ☐ Justify paths with input vector
  - ☐ Find true path
  - ☐ No line split
  - ☐ Enable asynchronous arcs
  - ☐ Show nets in combinational path
  - ☐ Show net transition time
  - ☐ Show input pins in combinational path
  - ☐ Show net capacitance
  - ☐ Show dont\_touch, size\_only attributes for nets and cells
- Output options:
  - ☒ To report viewer
  - ☐ To file: Report.txt (Browse...)
  - ☒ Append to file

The OK button is highlighted with a red circle.

Red circles and numbers are used to highlight specific elements: 1 points to the Timing menu, 2 points to the Check Timing... option, and 3 points to the OK button.

# Timing Report (2/2)

- ❑ The `report_timing` command reports the most critical maximum path (the path with the worst slack).



Design Vision - TopLevel1 (count) - [Report.1 - Timing]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

count

Point	Incr	Path
-----		
clock clk (rise edge)	5.00	5.00
clock network delay (ideal)	0.00	5.00
count_reg [0]/CK (DFFHQX1)	0.00	5.00 r
count_reg [0]/Q (DFFHQX1)	0.13	5.13 f
U9/CO (ADHXL)	0.09	5.22 f
U10/CO (ADHXL)	0.08	5.31 f
U11/CO (ADHXL)	0.08	5.39 f
U19/CO (ADHXL)	0.08	5.47 f
U17/Y (XNOR2X1)	0.12	5.59 r
U16/Y (NOR2X1)	0.02	5.61 f
count_reg [5]/D (DFFHQX1)	0.00	5.61 f
data arrival time		5.61
-----		
clock clk (rise edge)	15.00	15.00
clock network delay (ideal)	0.00	15.00
count_reg [5]/CK (DFFHQX1)	0.00	15.00 r
library setup time	-0.14	14.86
data required time		14.86
-----		
data required time		14.86
data arrival time		-5.61
-----		
slack (MET)		9.25

Hier.1 Report.1

Log History Options: ▾

design\_vision>

Ready

# Report cells (1/2)

## Design > Report cells

The screenshot shows the Design Vision software interface. The 'Design' menu is open, and the 'Report Cells...' option is highlighted. The 'Report Cells' dialog box is also open, showing the 'Report for' section with 'count' selected, and the 'Report options' section with 'No line split' and 'Verbose' checked. The 'Output options' section shows 'To report viewer' checked and 'To file' unchecked. The 'OK' button is highlighted.

Design Vision - TopLevel.1 (count) - [Report.1 - Timing]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Count

Report Cells

Report for

Cells: count Selection

Report options

☐ No line split ☒ Verbose

☐ Show cell connections Significant digits: 2

Output options

☒ To report viewer

☐ To file: Report.txt Browse...

☒ Append to file

OK Cancel Apply

Point

clock clk (rise edge)

clock network delay (ideal)

count\_reg [0] /CK (DFFHQX1)

count\_reg [0] /Q (DFFHQX1)

U9/CO (ADDHXL)

U10/CO (ADDHXL)

U11/CO (ADDHXL)

U19/CO (ADDHXL)

U17/Y (XNOR2X1)

U16/Y (NOR2X1)

count\_reg [5] /D (DFFHQX1)

data arrival time

clock clk (rise edge)

clock network delay (ideal)

count\_reg [5] /CK (DFFHQX1)

library setup time -0.14 14.86

data required time 14.86

data required time 14.86

data arrival time -5.61

slack (MET) 9.25

Hier.1 Report

Log History

design\_vision>

Report cells

# Report cells (2/2)

Design Vision - TopLevel1 (count) - [Report.2 - Cell]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

count

n - noncombinational  
r - removable  
u - contains unmapped logic

Cell	Reference	Library	Area	Attributes
U9	ADDHXL	fast	36.590401	mo, r
U10	ADDHXL	fast	36.590401	mo, r
U11	ADDHXL	fast	36.590401	mo, r
U12	NOR2BX1	fast	13.305600	
U13	NOR2BX1	fast	13.305600	
U14	NOR2BX1	fast	13.305600	
U15	NOR2BX1	fast	13.305600	
U16	NOR2X1	fast	9.979200	
U17	XNOR2X1	fast	26.611200	
U18	NOR2X1	fast	9.979200	
U19	ADDHXL	fast	36.590401	mo, r
count_reg [0]	DFFHQX1	fast	53.222401	n
count_reg [1]	DFFHQX1	fast	53.222401	n
count_reg [2]	DFFHQX1	fast	53.222401	n
count_reg [3]	DFFHQX1	fast	53.222401	n
count_reg [4]	DFFHQX1	fast	53.222401	n
count_reg [5]	DFFHQX1	fast	53.222401	n
Total 17 cells			565.488008	

\*\*\*\*\* End Of Report \*\*\*\*\*

Hier.1 Report.1 Report.2

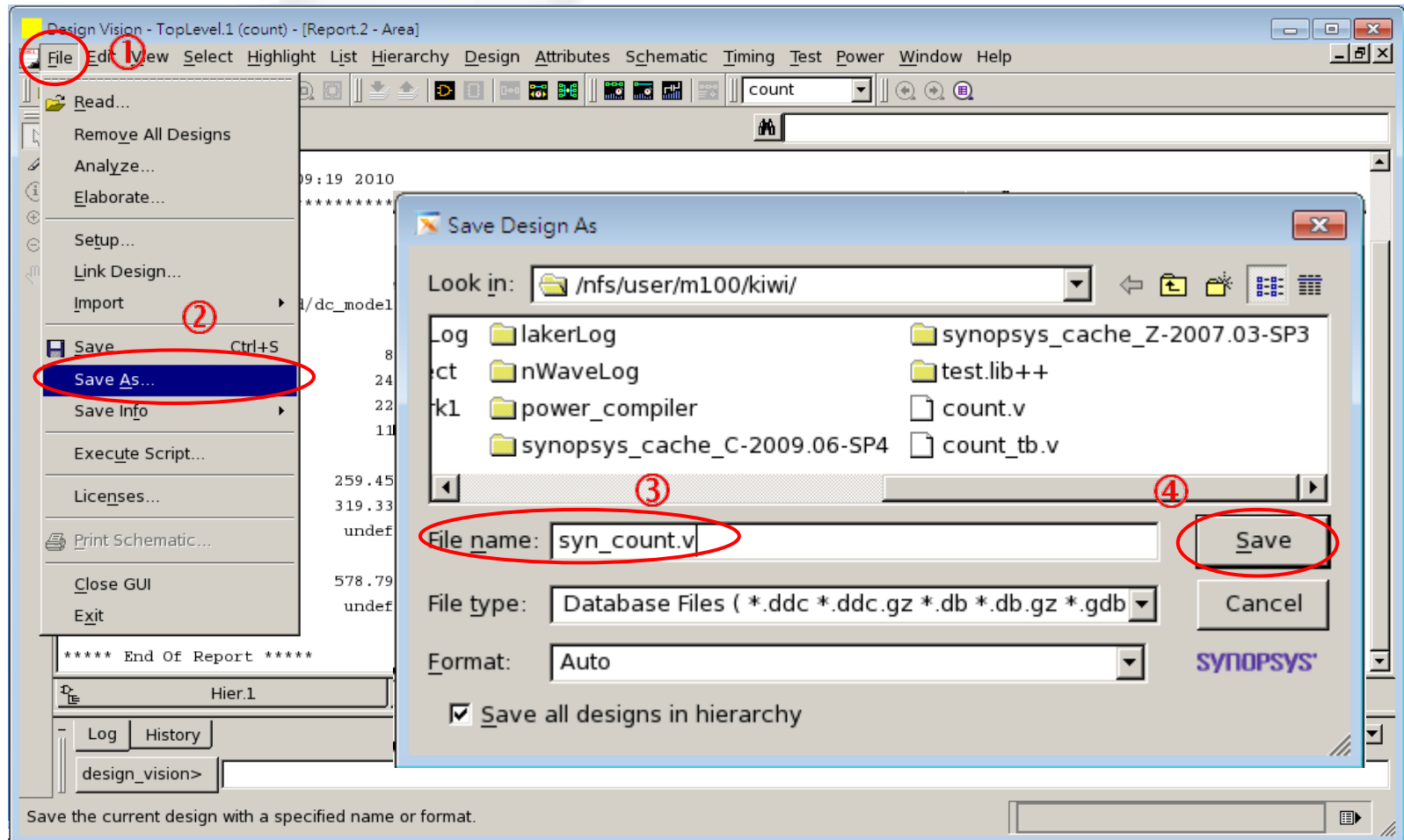
Log History Options: ▾

design\_vision>

Ready

# Save Your Design

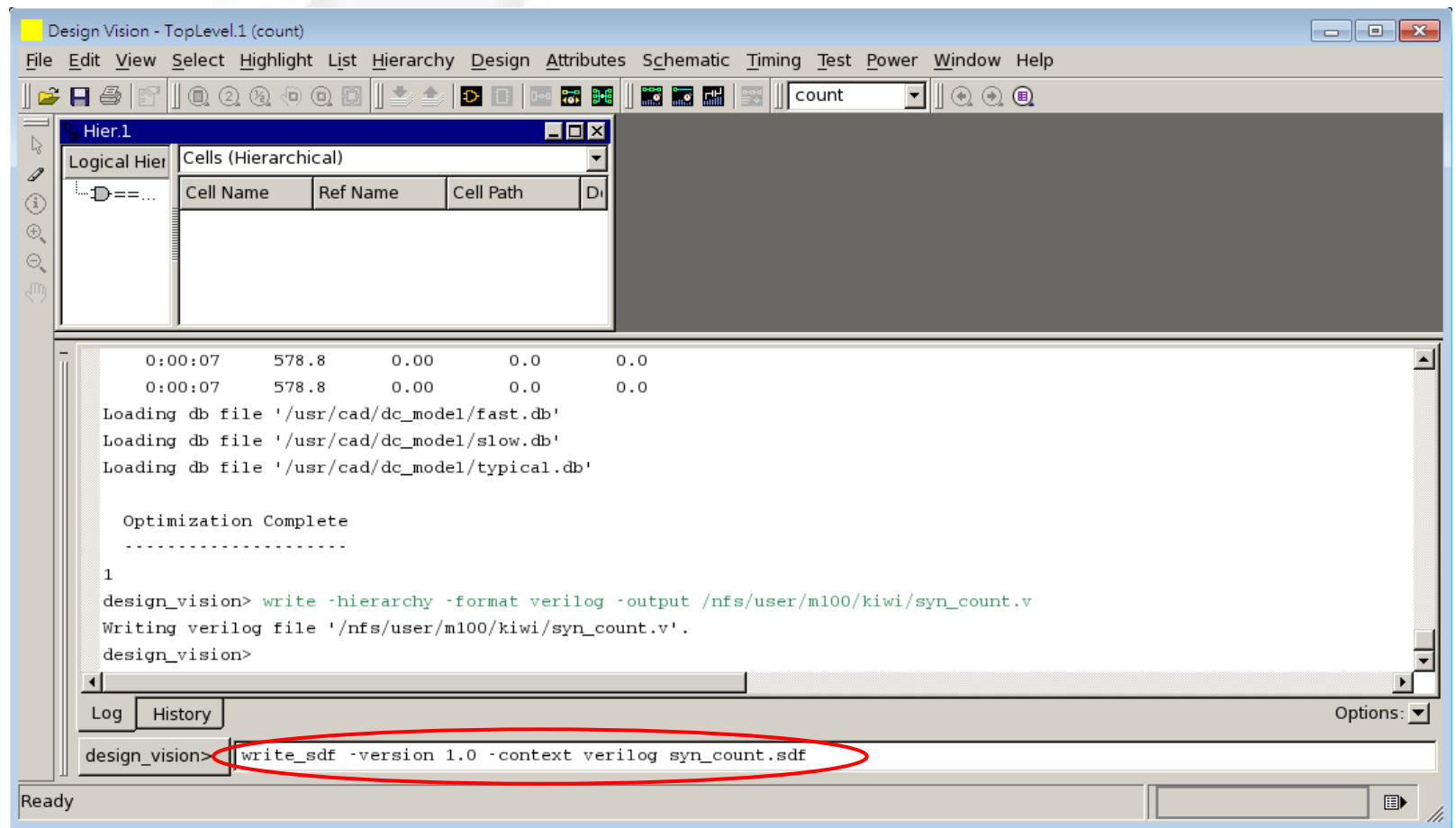
## File > Save as





# Save Timing File

- ❑ `write_sdf -version 1.0 -context verilog syn_count.sdf`
- ❑ **sdf files store timing information for simulation**



# Gate level Simulation (1/3)

- Add 『`timescale 1ns/10ps』 into syn\_file.v

```
`timescale 1ns / 10ps
```

```
module count ( count, clk, reset );  
    output [5:0] count;  
    input clk, reset;  
    wire  N9, N10, N11, N12, N13, N14, n2, n3, n4, n5, n6, n7, n8, n9, n10, n11  
    ;
```

# Gate level Simulation (2/3)

## □ Modify testbench.v:

**initial \$sdf\_annotate("syn\_file.sdf", instance module name);**

```
timescale 1ns / 10ps

define period 4

module count_tb;
  wire [5:0] count;
  reg clk, reset;

  count a1(
    .count(count),
    .clk(clk),
    .reset(reset)
  );

  always #(`period/2) clk=~clk;
  initial begin
    clk=0;
    reset=0;
    #(`period/4) reset=1;
    #(`period) reset=0;
    #(`period*30) $finish;
  end

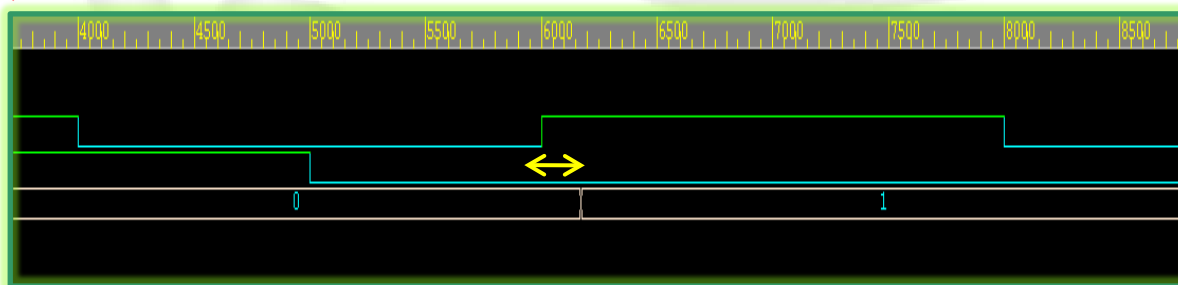
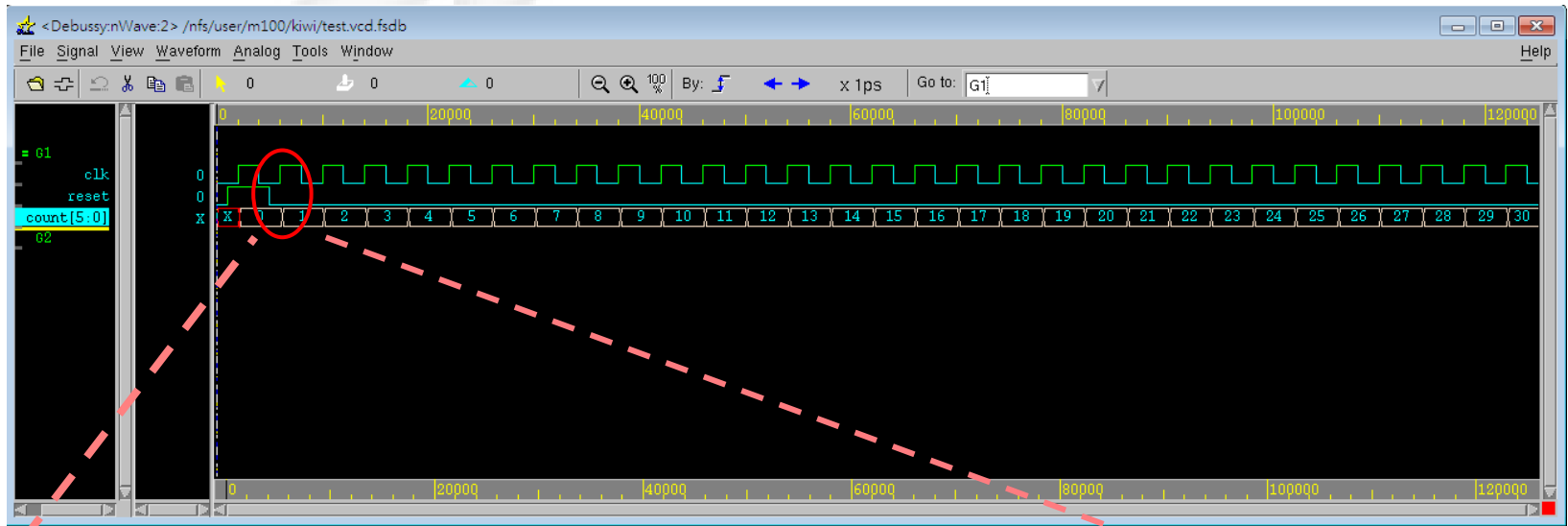
  initial $sdf_annotate("syn_count.sdf", a1);

  initial begin
    $dumpfile("test.vcd");
    $dumpvars();
  end
endmodule
```

# Gate level Simulation (3/3)

❑ `ncverilog testbench.v syn_file.v TechFile.v (ex:tsmc18.v) +access+r`

➤ Please refer to “ncverilog” powerpoint to open waveform !



Delay time !