N26F300
VLSI SYSTEM DESIGN
(GRADUATE LEVEL)

Fall 2010

Instructor & TA

Instructor: **邱瀝毅 (Lih-yih Chiou), Ph.D.**

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Course website: http://moodle.ncku.edu.tw

TA: **蕭育書**/簡才淦/柯柏洲/吳冠麟

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Room: EE95316/EE95604 (奇美樓)

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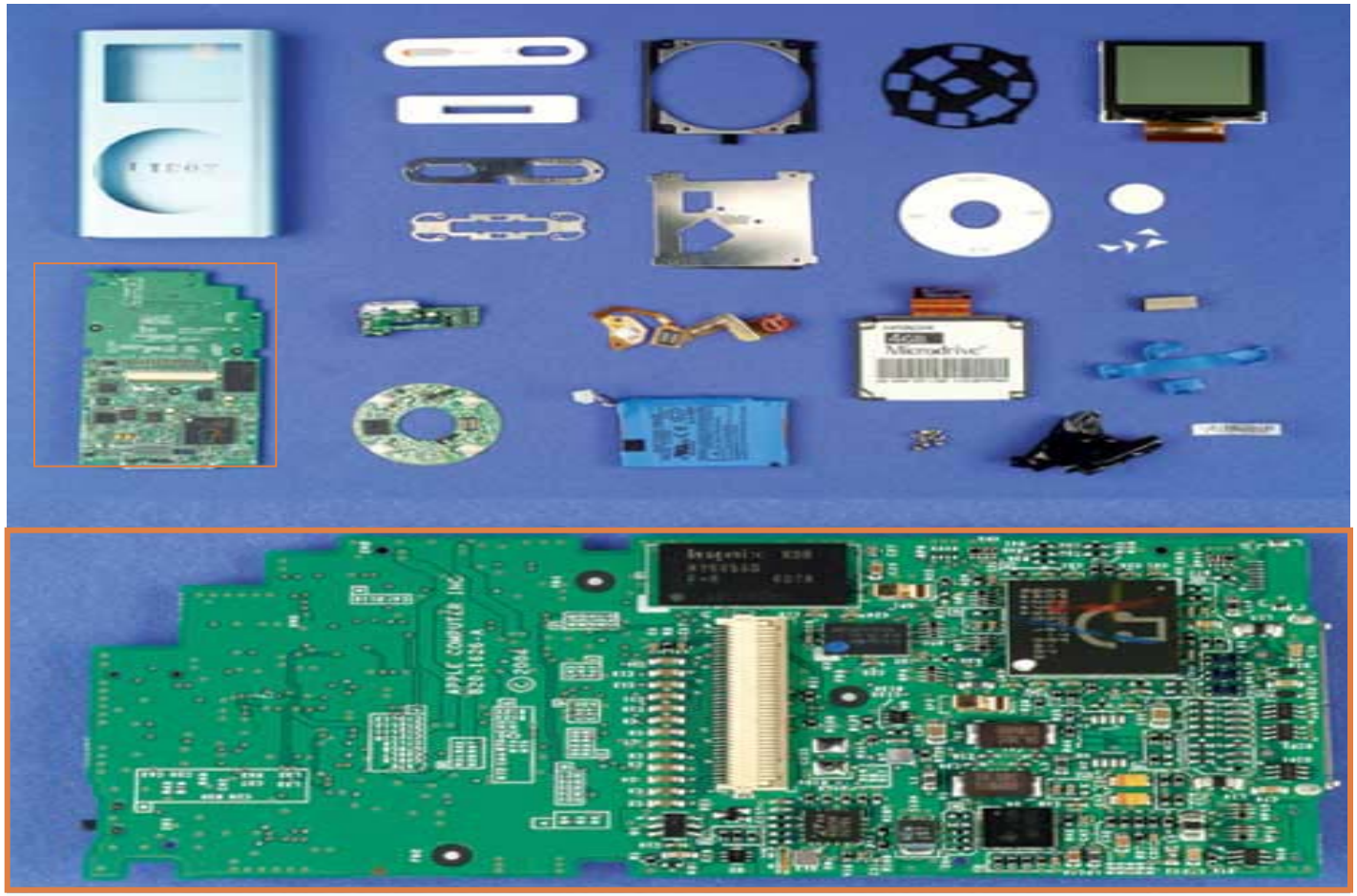
office hour: Tue. 19:00--21:00 EE95316

Electronic Device: iPod

ipod

Source: pc.watch.impress.co.jp

Components Inside iPOD

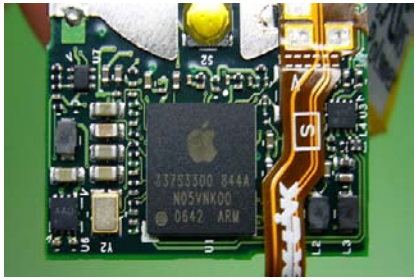


Source: www.elecdesign.com

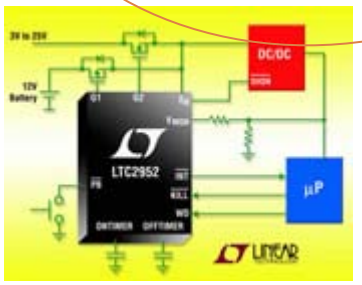
6 Key Components of iPod

Battery/Sony

Processor ?? / ARM ??

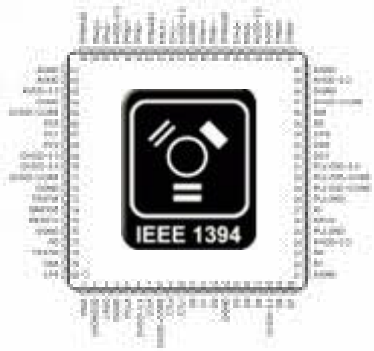


Codec / Wolfson



Power Management /
Linear Technology

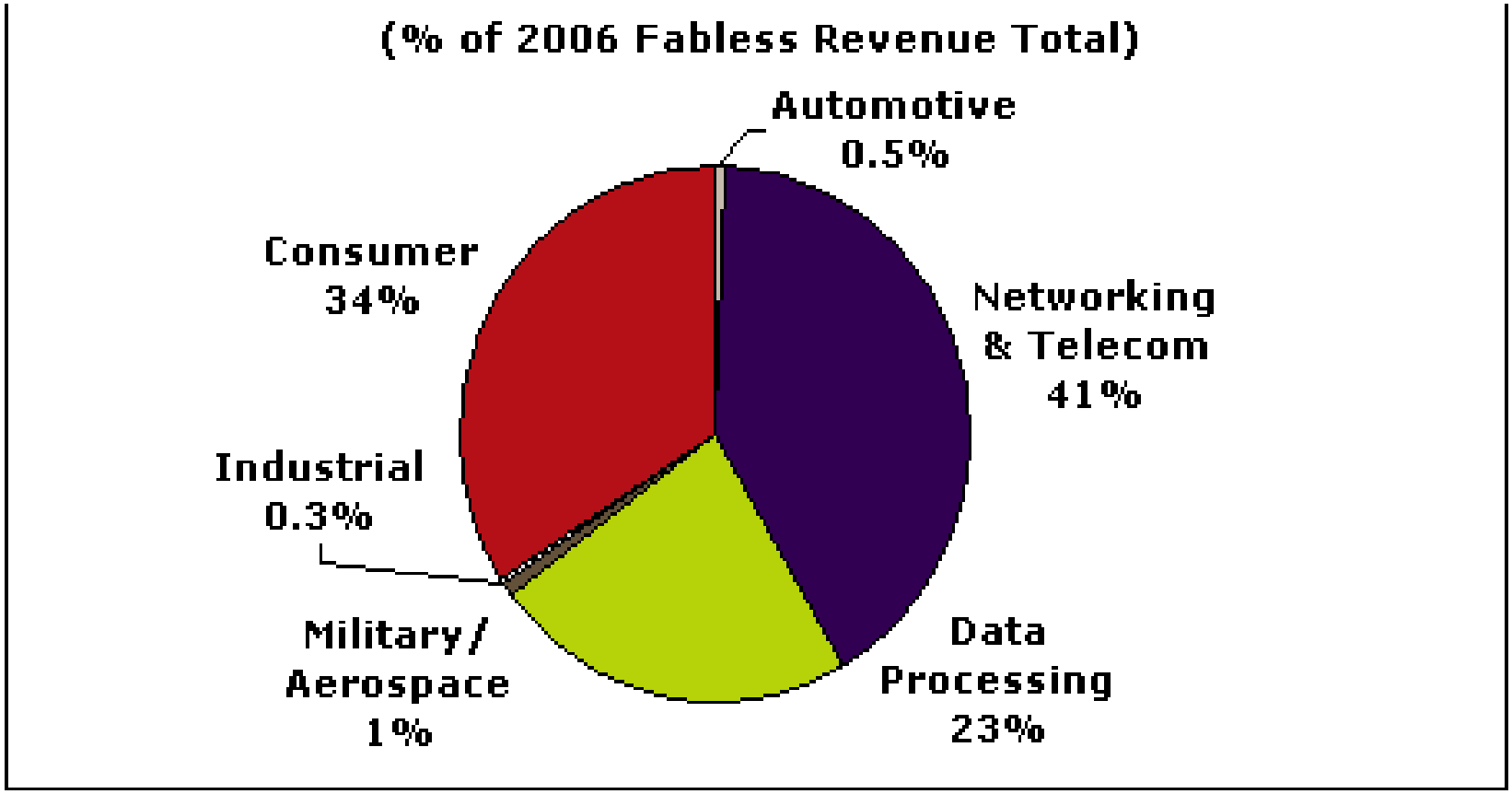
DAC / Wolfson



Firewire / Texas Instrument

Disk Drive / Toshiba

Public Fabless End-Markets Breakdown



Source: www.fsa.org

Top 10 Fabless Companies in 2006

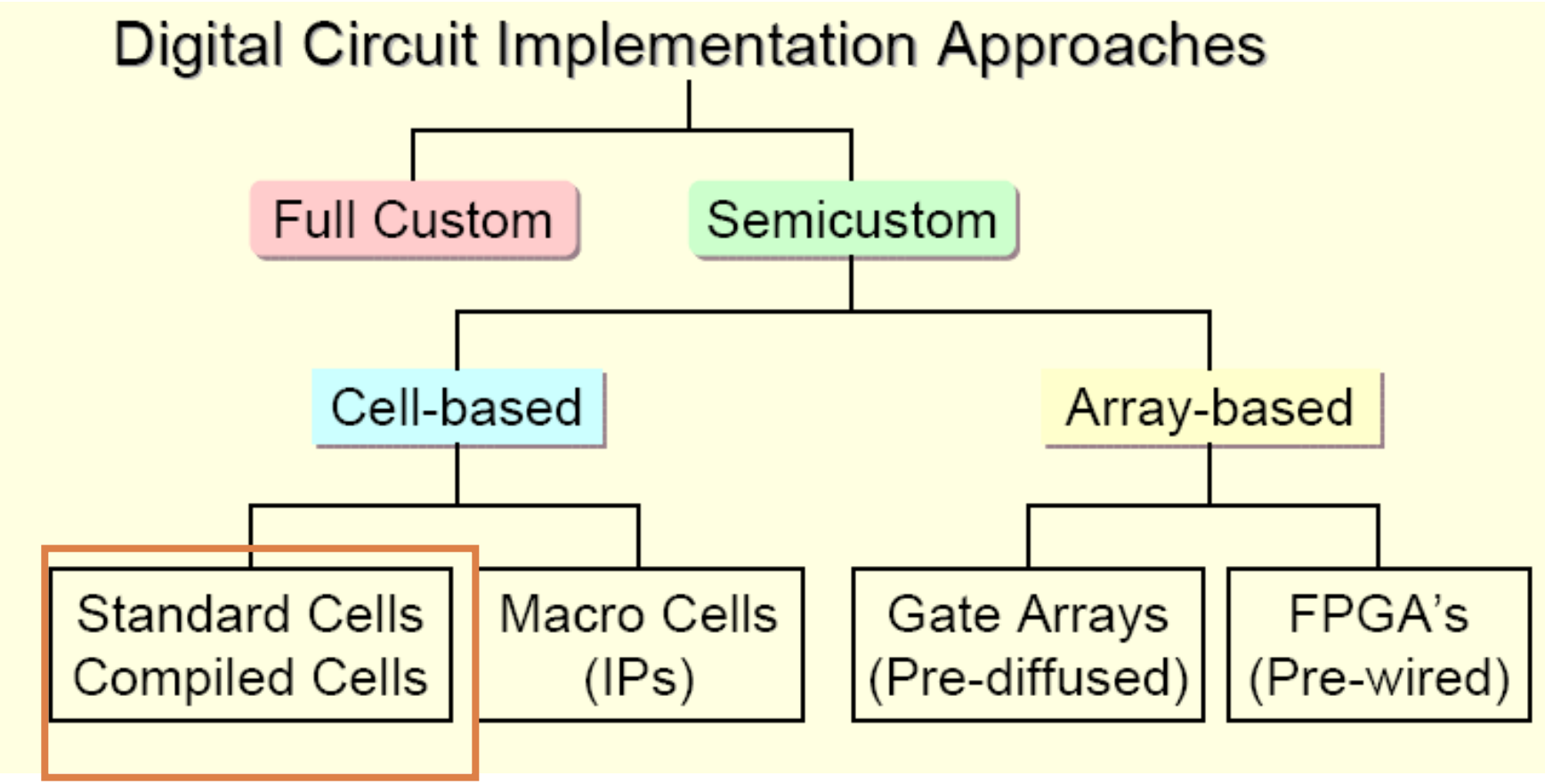
Company		2006 Revenue (US millions)
1	QUALCOMM	$4,331.0
2	Broadcom	$3,667.8
3	ScanDisk Corporation	$3,257.5
4	NVIDIA Corporation	$3,068.8
5	Marvell Technology Group Ltd.	$2,237.6
6	LSI Logic	$1,982.1
7	Xilinx, Inc.	$1,871.6
8	MediaTek Incorporation	$1,624.5
9	Altera	$1,285.5
10	Conexant Systems	$985.6

Source: www.fsa.org

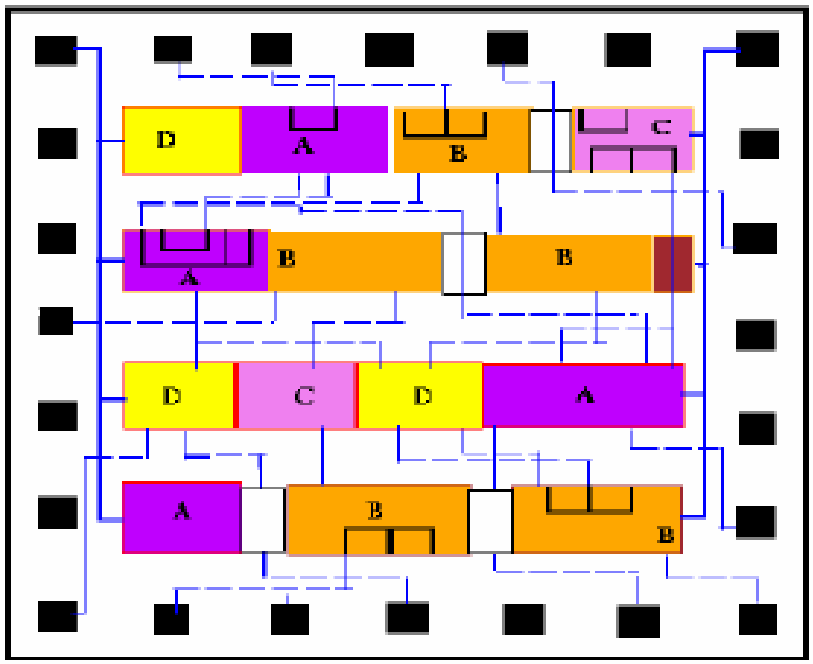
Top 10 Fabless Companies in 2009

2009	2008(2Q)	2007	公司名	2008年 前兩季營收（億美元）	主要產品
1	1	1	Qualcomm (高通)	6.6	手機晶片 、 無線通訊晶片
2			**AMD**	5.3	繪圖晶片、fab to Global Foundries
3	2	4	Broadcomm (博通)	4.2	手機晶片、無線通訊晶片 、數據機與GPS晶片
4	7	7	聯發科	3.5	光儲存晶片、 手機晶片 、數位電視晶片
5	3	2	nVidia	3.1	繪圖晶片
6	4	5	Marvell (邁威爾)	2.7	網路晶片、 手機晶片
7	8	8	Xilinx(智霖)	1.7	可程式邏輯晶片 （主要用於家電及電腦週邊）
8	6	6	LSI	1.4	儲存晶片、 光儲存晶片
9	10	10	Altera (阿爾特拉)	1.2	可程式邏輯晶片
10	9	9	Avago (安華高)	0.87	類比晶片

Target Digital Design Implementation



Standard Cell Design Style

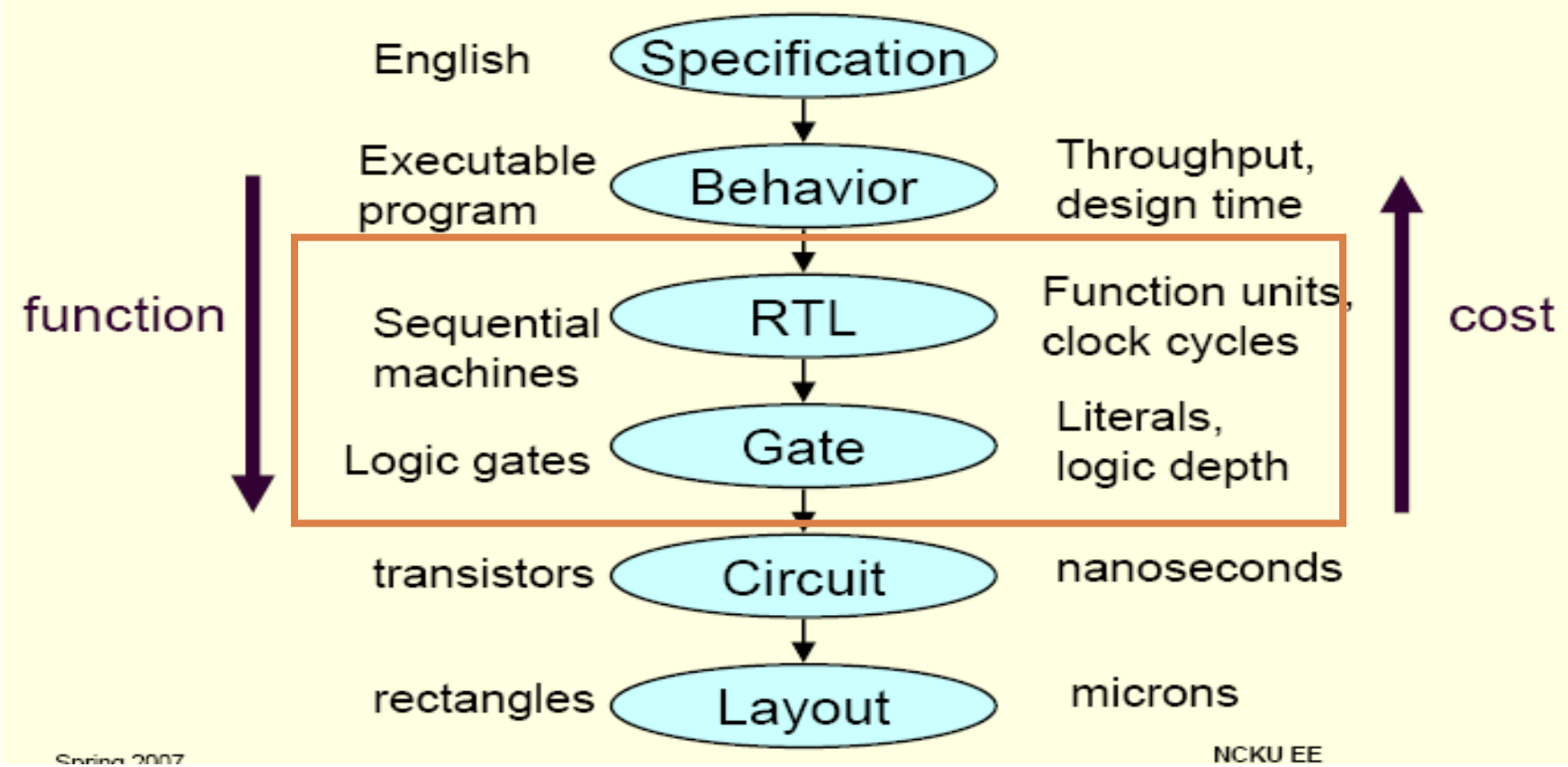


Selects pre-design cells (of the same height) to implement logic

These cells may be

- Logic gates: nand2, NOT, and2, and4, nor2, mux2, decoder etc.
- Latches: latchx1, latchrx2, …
- Flip-flops: pdffx1, pdffx2,…
- Basic blocks: fulladder

Target Levels of Design Abstractions



Course Objectives

- Provide fundamental design concepts
  - Modeling systems using Verilog-HDL
  - Digital IC design flow using modern CAD tools
  - Design of synchronous systems
  - Synthesis of HDL
- Establish design and analysis skills for
  - Multi-cycle architecture
  - Pipelined architectures

Course Prerequisites

- Digital Logic Design (must)
  - Boolean algebra
  - Logic minimization
  - Arithmetic units (+,-,*, AND, OR, …)
  - Finite state machine
- Computer Organization (must)
  - Multi-cycle CPU
  - Pipeline CPU
  - Cache
- Self-motivation in learning CAD tools and Verilog HDL

Outline

- Basic Digital IC System Design (7 weeks)
  - VLSI System Design Flow
  - EDA Tools
  - Digital Design Using Verilog
  - Synthesis of Digital Logic
- Advanced IC System Design (7 weeks)
  - Design of digital processors and periphery
  - Project

Hours Arrangement

- Lecture
  - Time: Thursday 9:10-noon
  - Location: EE 92177
  - Most of the weeks except tutorial sessions
- Laboratory
  - Selected weeks
  - Location: SoC Lab (EE 95312@奇美樓)
  - DO NOT LOCK TERMINALS. Otherwise, your right will be suspended (7 days x number of violations)
- NO FOOD or DRINK in the lecture hall or computer labs

References

References

- "Advanced Digital Design with Verilog HDL," Michael D. Ciletti, Prentice Hall, 2003. ISBN: 0-13-089161-4
- "FSM based Digital Design using Verilog HDL," Peter Minns and Ian Elliott, Wiley, 2008. ISBN: 978-0-470-06070-4
- "Digital Design: An Embedded System Approach Using Verilog," by Peter J. Ashenden. Weste and David Harris, Morgan Kaufmann, 2008. ISBN: 978-0-12-369527-7
- "Computer Organization and Design: The Hardware/Software Interface," 3th ed. by David A. Patterson and John L. Hennessy, Morgan Kaufmann Pub., 2005. ISBN: 981-2592-17-2
- "Verilog HDL: A Guide to Digital Design and Synthesis," 2nd ed. by Samir Palnitkar, Prentice Hall, 2003. ISBN: 0-13-044911-3

Grading Policy

- **Grading will be based on the following items:**
  - Participation
  - Homework assignments
  - Quizzes and Exams
  - Final project report/demo

Homework Assignments

- Principles
  - Help you to learn the materials
  - Promote self-motivated learning capability as a graduate student
  - Focus on your learning and self-evaluation

- Ideas
  - Longer period of time for an HW assignment
  - A series of small labs as homework
  - A contest problem as homework
  - A project-oriented homework

Homework Assignments

- 4~ 6 homework assignments
- Submission electronically through the course website before the specified time and date
- If you fail to do so, your assignment is considered OVERDUE and gets NO credit.
- An EXTRA paper copy needs to be delivered in class

Exams

- Schedule
  - Midterm exam: Thursday, Nov 04, 2010
  - NO final

- There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for make-up exams).

Final Project

- Principles
  - Use learned design skills for your target applications
  - Need team work (4~7 persons/team)
  - Promote self-tracking capability as a graduate student
  - Focus on end results

- Ideas
  - Propose and present your interested project based on requirements
  - Discuss your team project regularly on Moodle
  - Emphasize on verified designs
  - Plan and meet your own schedule

Final Project

- **Schedule**
  - Proposal presentation (11/18, Thu.)

    in class
  - Project submission/Demo (1/20, Tue.)

    09:00 @Moodle ; 10:00 ~ 18:00 @EE95312
  - Project Presentation (1/22, Thu.)

    09:00 ~ 12:00 @ EE95312
- **Topic**
  - **Design a general pipeline processor that can work with a compiler and communicate with external modules (either memory or accelerators) via on-chip buses**

Course Policy

- Encourage you to discuss assigned problems with peers
- Must complete his/her assignment independently or as specified
- Any person/team who is found to be dishonesty in homework assignments, examines/quizzes, or the project, the involved person(s) will receive an ***"0"*** on the evaluated instrument (*paper, exam, project, homework, etc.*)

Notes

- Applying SoC Lab entrance authorization needs to have your department entrance card (門禁卡) number. For details, please check the web http://lpvlsi.ee.ncku.edu.tw
- Submit your head photo in JPEG to course website
- When the photo is received, you will be assigned an SoC Lab account, which all homework and project will be graded based on tools in this lab.

Tutorials on 9/16 & 9/24

- Contents
  - Basics of Unix, Environment in SoC Lab, NC-Verilog, Debussy, Design Vision
- Class hours arrangement
  - 9:10-10:00 Regular session/Tutorial Overview
  - 10:10-noon Hand-on practices @SoC Lab
- Group arrangement (by student ID)
  - Even: 9/16
  - Odd: 9/24
- Suggestion: Watch tutorial video last year first

Tutorials on 10/21 & 10/24

- Contents
  - Advanced Design Vision and AndeSight Basics
- Class hours arrangement
  - 9:10-10:00 Regular session/Tutorial Overview
  - 10:10-noon Hand-on practices @SoC Lab
- Group arrangement (by student ID)
  - Even: 9/16
  - Odd: 9/24
- Suggestion: Watch tutorial video last year first