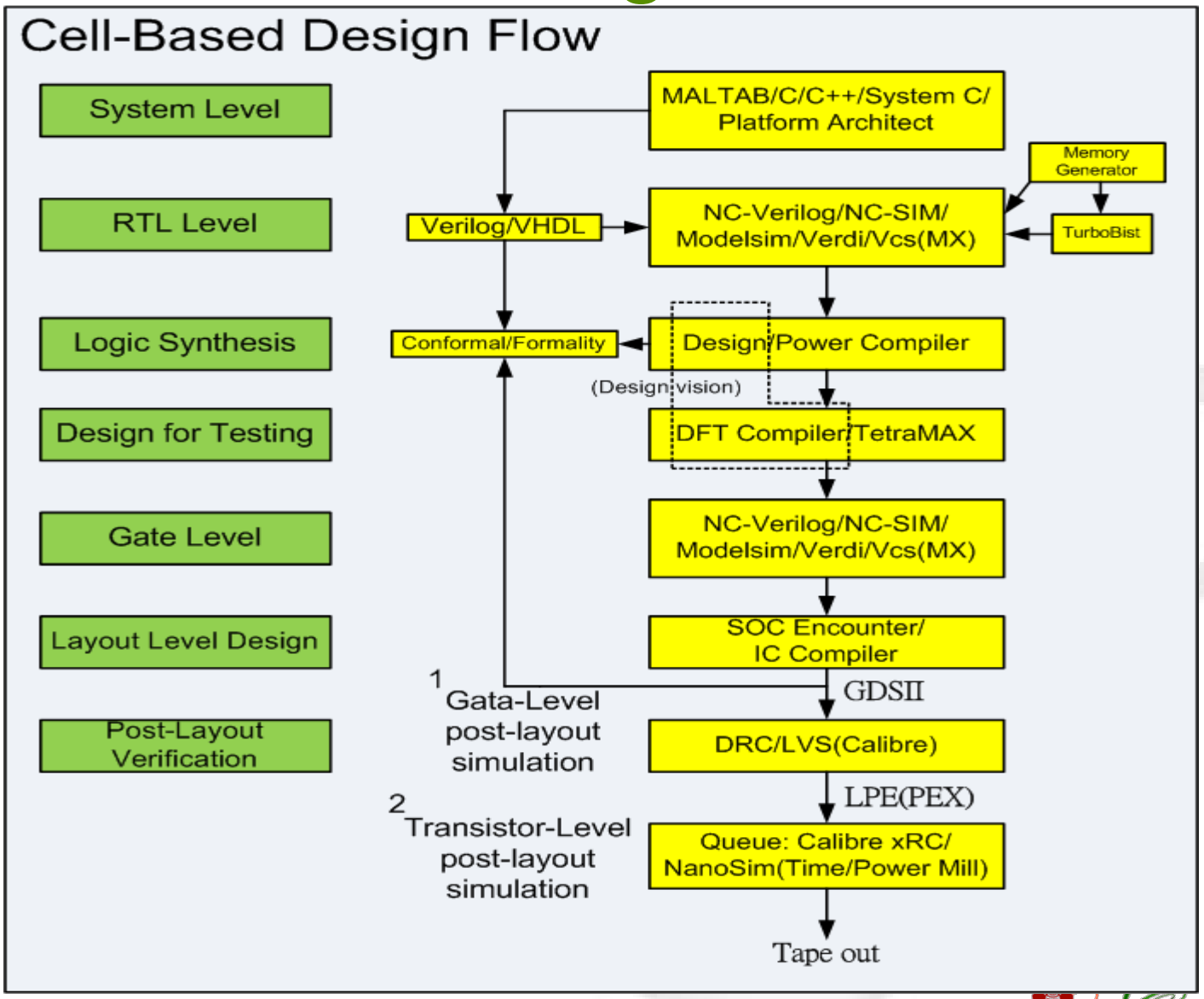
NC-Verilog

Advisor：Lih-Yih Chiou

Speaker :

Date : 2010/09/16

Cell-Based Design Flow

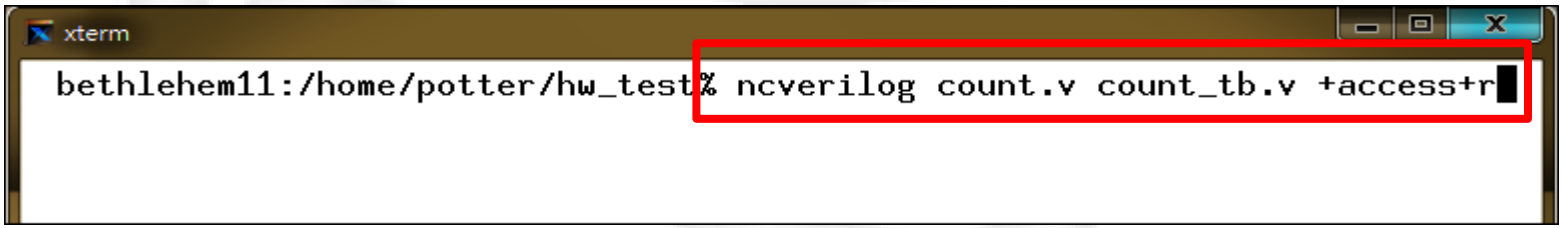


Compiling & Simulating Using NC-Verilog (1/2)

- To dump vcd file (attach to testbench)
  - Initial
    begin
    $dumpfile("test.vcd");
    $dumpvars;
    end
  - Initial
    begin
    $fsdbDumpfile("test.fsdb");
    $fsdbDumpvars;
    end

```
`timescale 1ns / 10ps

`define period 4

module count_tb;
  wire [5:0]count;
  reg clk,reset;

  count      a1(
                .count(count),
                .clk(clk),
                .reset(reset)
               );
  always #(`period/2) clk=~clk;
  initial begin
    clk=0;
    reset=0;
    #(`period/4) reset=1;
    #(`period)   reset=0;
    #(`period*30) $finish;
  end

  initial begin
    $dumpfile("test.vcd");
    $dumpvars();
  end

endmodule
```

- To compile & dump vcd file
  - ncverilog test.v test_tb.v +access+r



Compiling & Simulating Using NC-Verilog (2/2)

Compiling result

```
xterm
                Registers:              3       3
                Scalar wires:           2       -
                Expanded wires:         6       1
                Always blocks:          2       2
                Initial blocks:         2       2
                Simulation timescale:  10ps
        Writing initial simulation snapshot: worklib.count_tb:v
Loading snapshot worklib.count_tb:v ..................... Done
ncsim> source /usr/cad/cadence/IUS/cur/tools/inca/files/ncsimrc
ncsim> run
Simulation complete via $finish(1) at time 125 NS + 0
./count_tb.v:20      #(`period*30) $finish;
ncsim> exit
bethlehem11:/home/potter/hw_test%
```

Check .vcd file

```
xterm
bethlehem11:/home/potter/hw_test% ls
INCA_libs  count.v  count_tb.v  ncverilog.log  test.vcd
bethlehem11:/home/potter/hw_test%
```

Debussy教學

Advisor: Lih-Yih Chiou
Speaker:
Date: 2010/9/16

EE

LPHPLAB
VLSI Design LAB

Outline

1. Introduction
2. nTrace
   - Overview
   - Import Files
   - hierarchy browser and source code
   - nWave

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Introduction

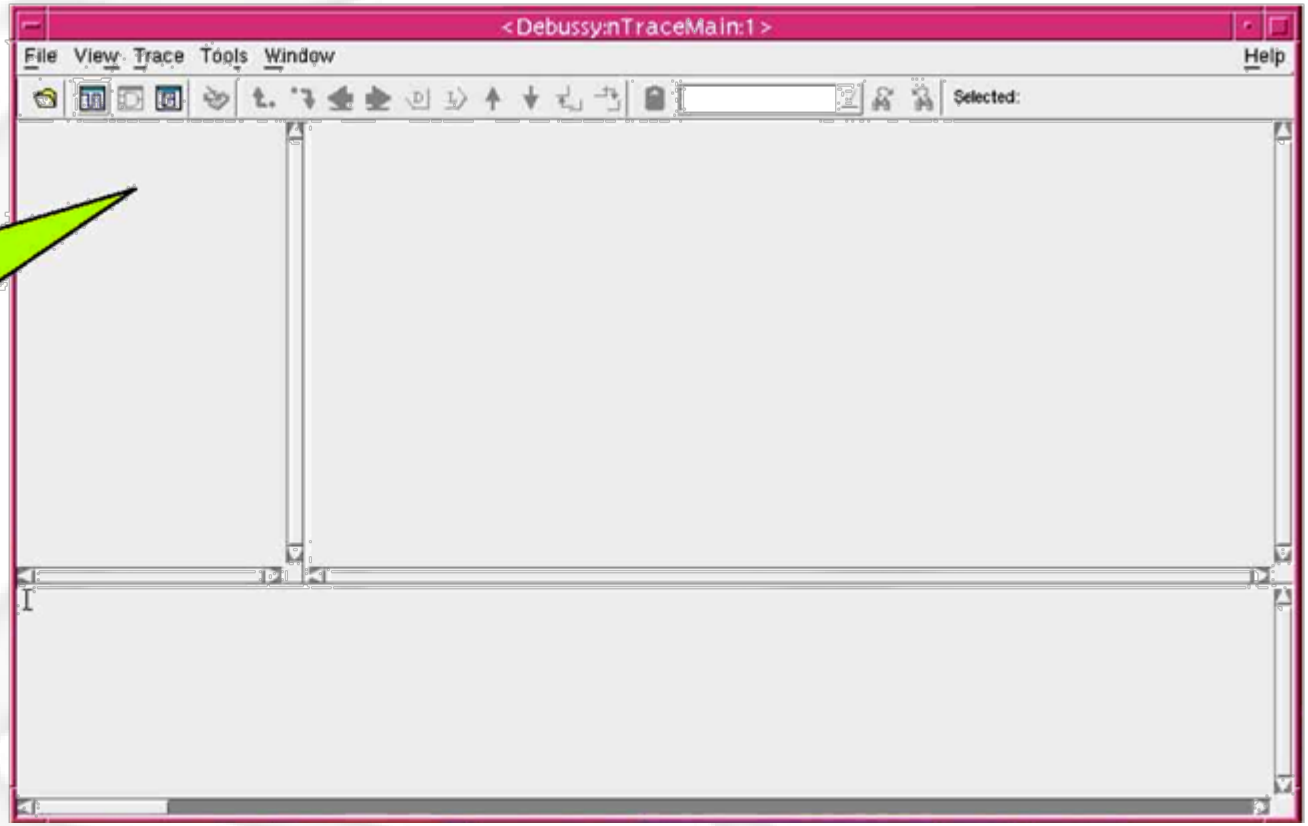
- Debussy是NOVAS Software, Inc(思源科技)發展的HDL Debug & Analysis tool . 現在改名為Verdi.
- 它強大的功能在：能在HDL source code、schematic diagram、 waveform、state bubble diagram做即時的trace.
- Debussy本身沒有模擬器，所以要透過外部來模擬(如NcVerilog, Verilog-XL, ModelSim).

Outline

1. Introduction
2. nTrace
   - Overview
   - Import Files
   - hierarchy browser and source code
   - nWave

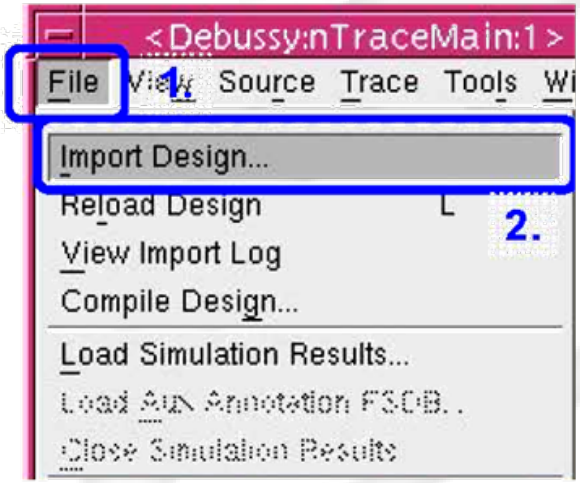
nTrace Overview

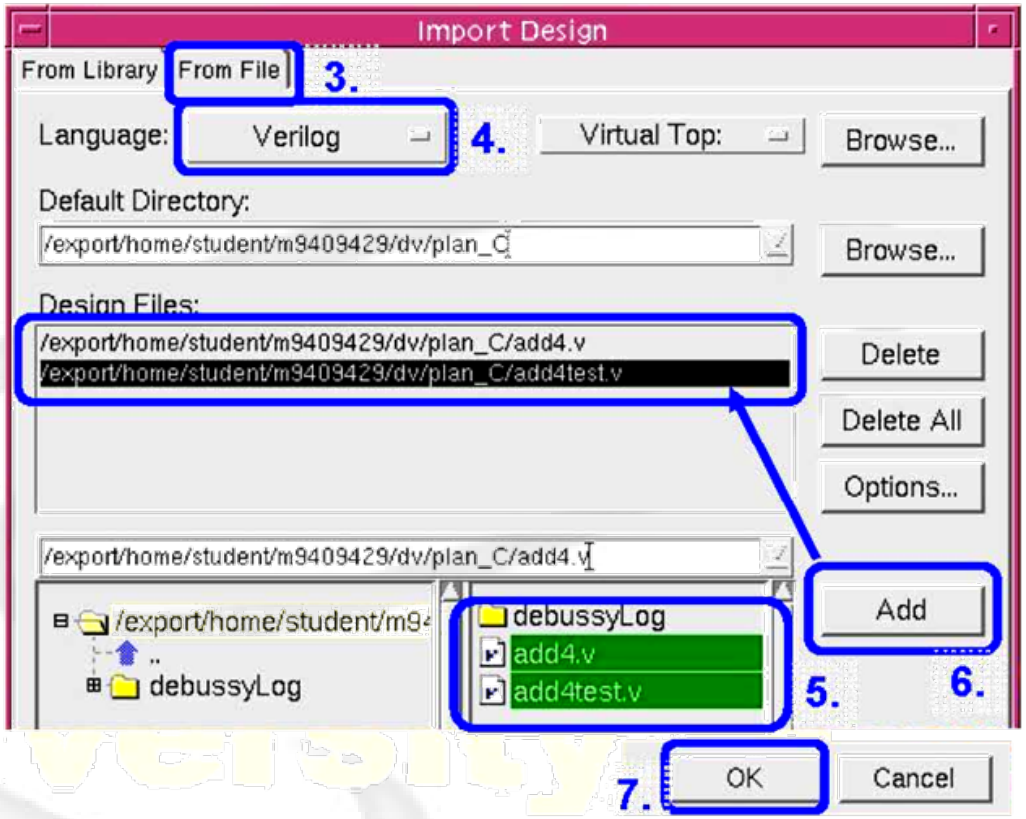
- **Invoke Debussy： Debussy &**
  會開啟nTrace



nTrace :: Import Files

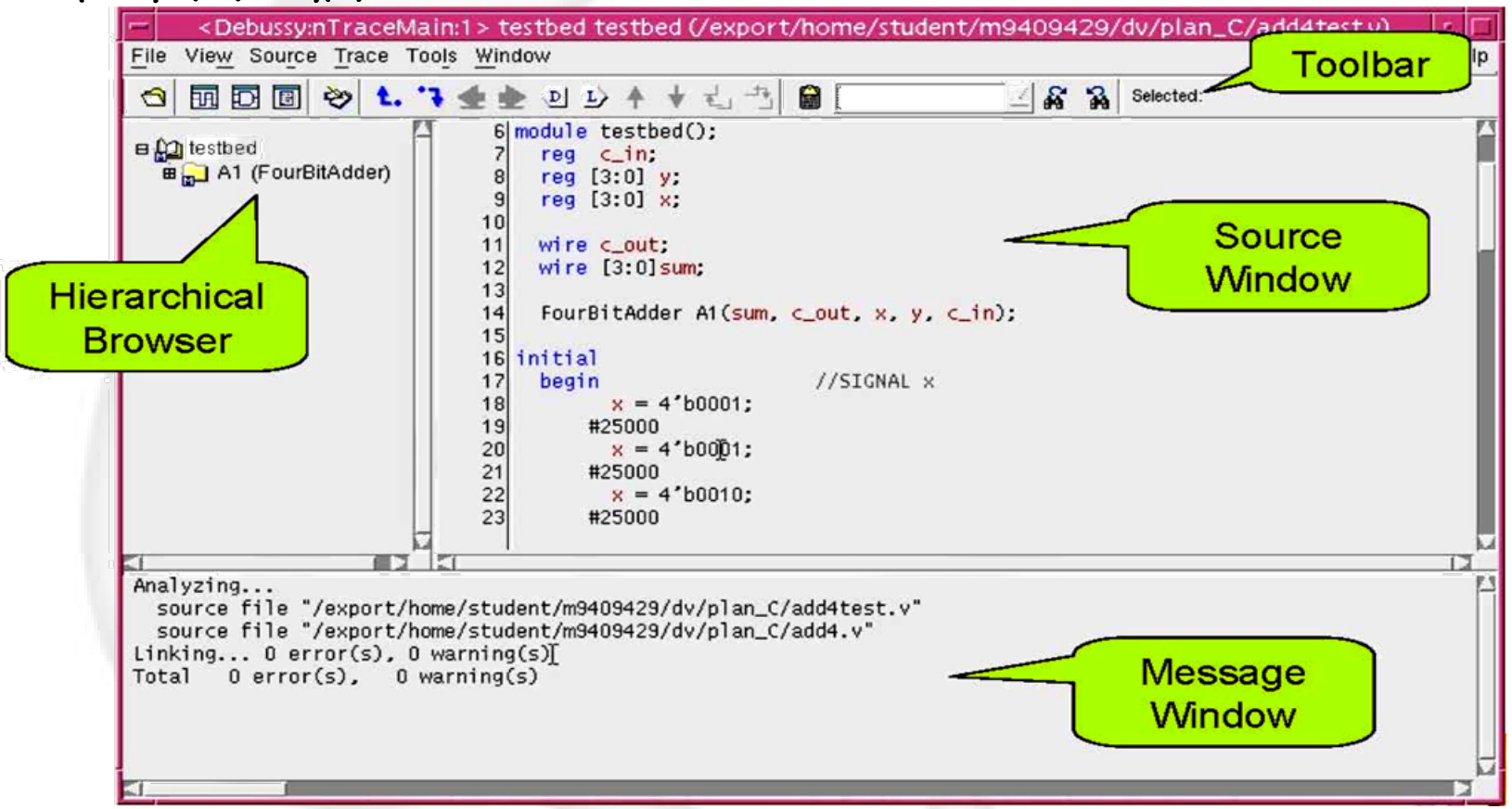
- **Import verilog design**
  - ➔ **By GUI: *File➔Import Design➔From File***





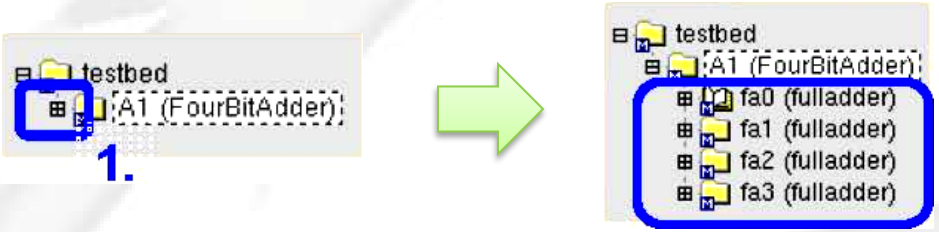
nTrace :: Import Files

- 當打開檔案之後，每個**window**出現的畫面如下，含下面三個**window:**

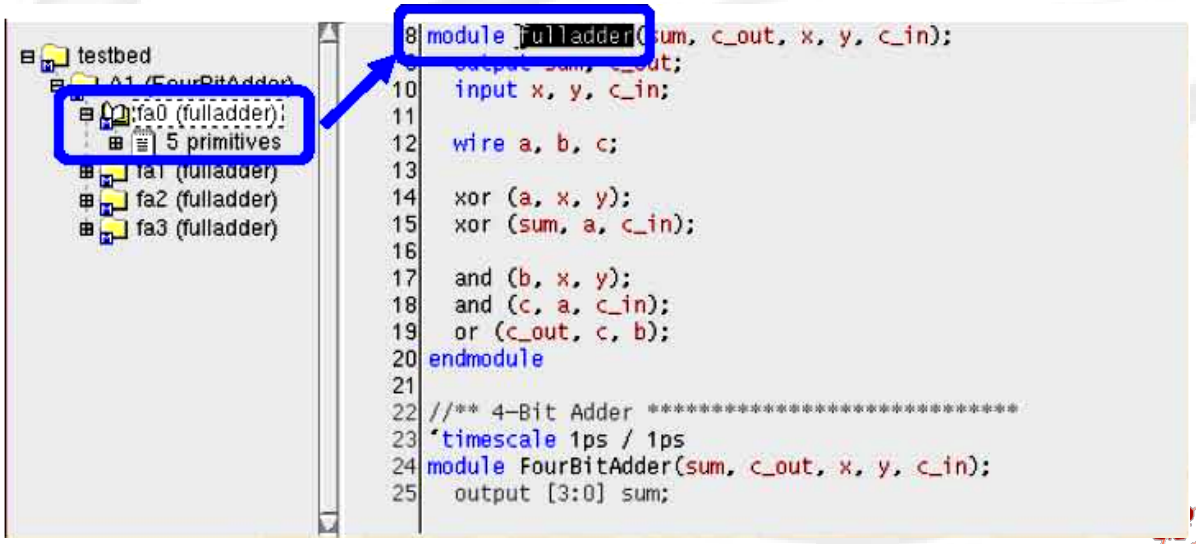


nTrace :: hierarchy browser and source code

- 在Hierarchy browser點擊A1(FourBitAdder)左側的符號“+”，可以展開四個Full A的(fa0, fa1, fa2, fa3)。



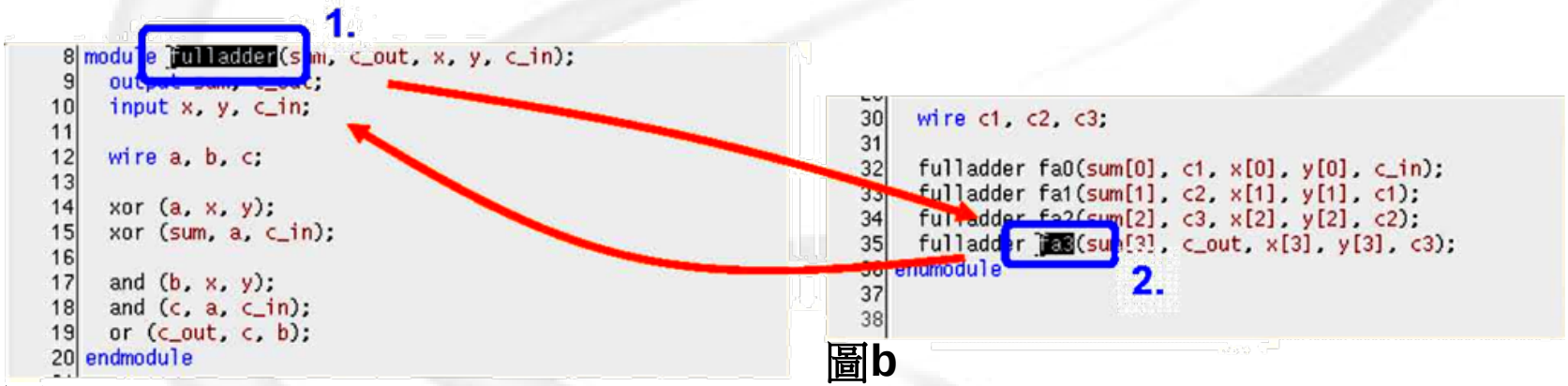
- 雙擊Hierarchy brower內的fa0…，右邊的source code window會立即切換到相對應的module。



nTrace :: hierarchy browser and source code

- 如果你想追蹤**fa3**的話，雙擊**source code window**內的**“fulladder”**，軟體會自動幫你追蹤出引用**fa3**的地方，結果顯示於圖**b – A1(FourBitAdder)**的**fa3**；若再雙擊**fa3**，則又回到**“fulladder”**。

- 你可以藉由這個方法，輕易的追蹤出**project**內的所有**design**彼此之間的關連性。

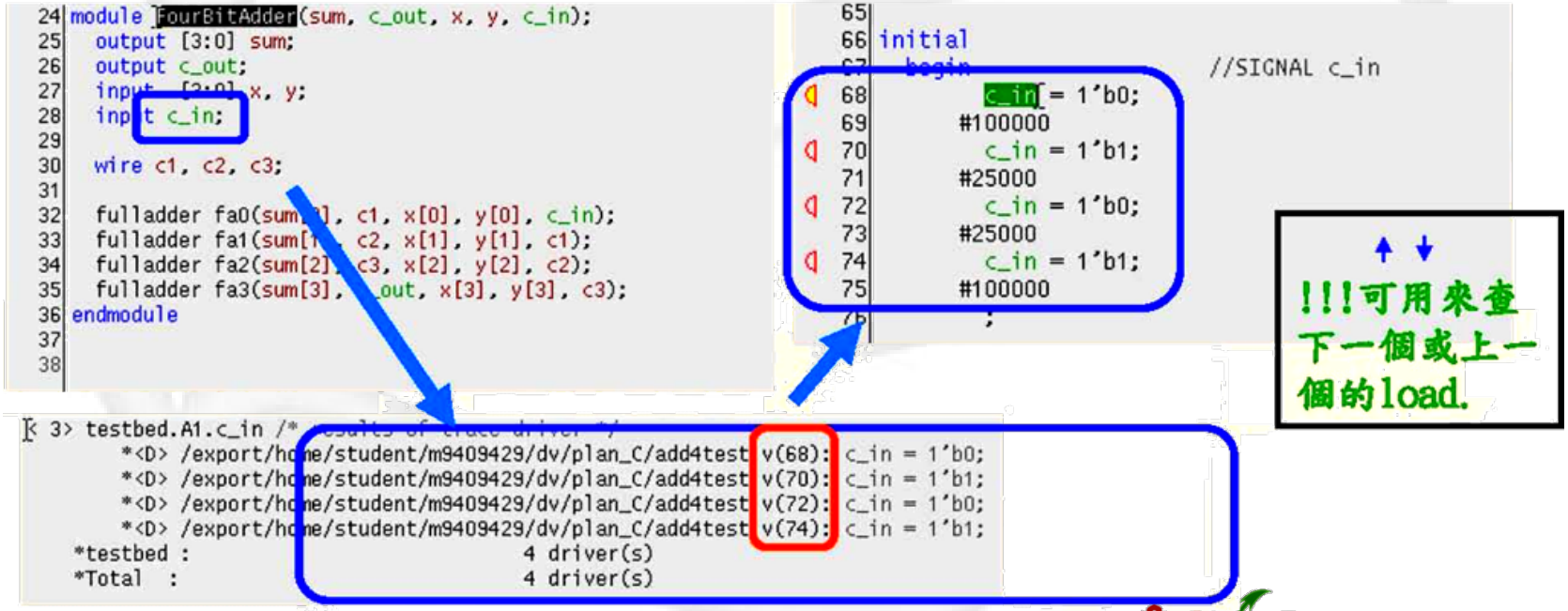


圖a　圖b

nTrace :: hierarchy browser and source code

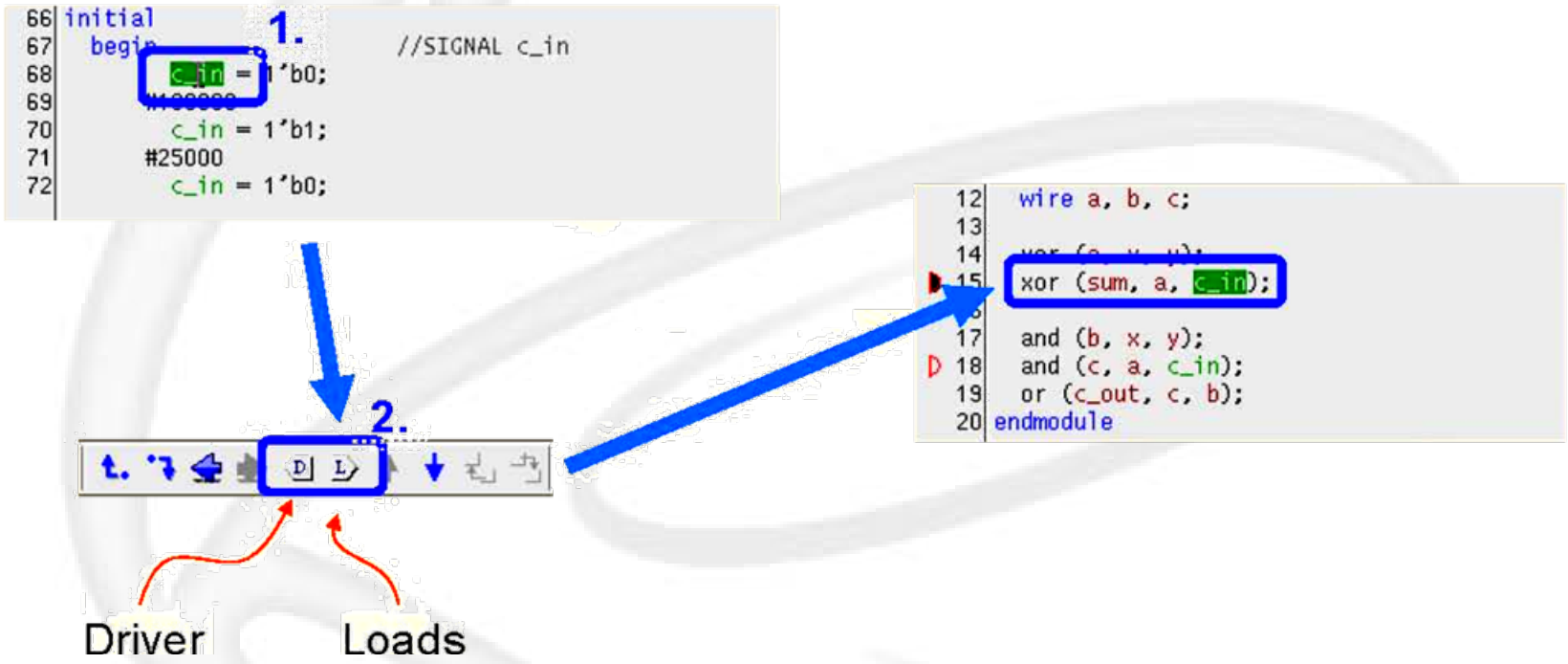
- 除了追蹤各個**module**之間的關連性，也可以用同樣的方法來追蹤出**signal's drivers**和**loads**。

- 若雙擊**FourBitAdder**的訊號**c_in**，將顯示該訊號的所有**drive loads**，結果如**message window**顯示，有**4**處**drive c_in**，分別在**add4test line 69, 71, 73, 74**。



nTrace :: hierarchy browser and source code

- 選定line 69，*Trace➔load*則可用來追蹤該訊號的所有 **“load”**。



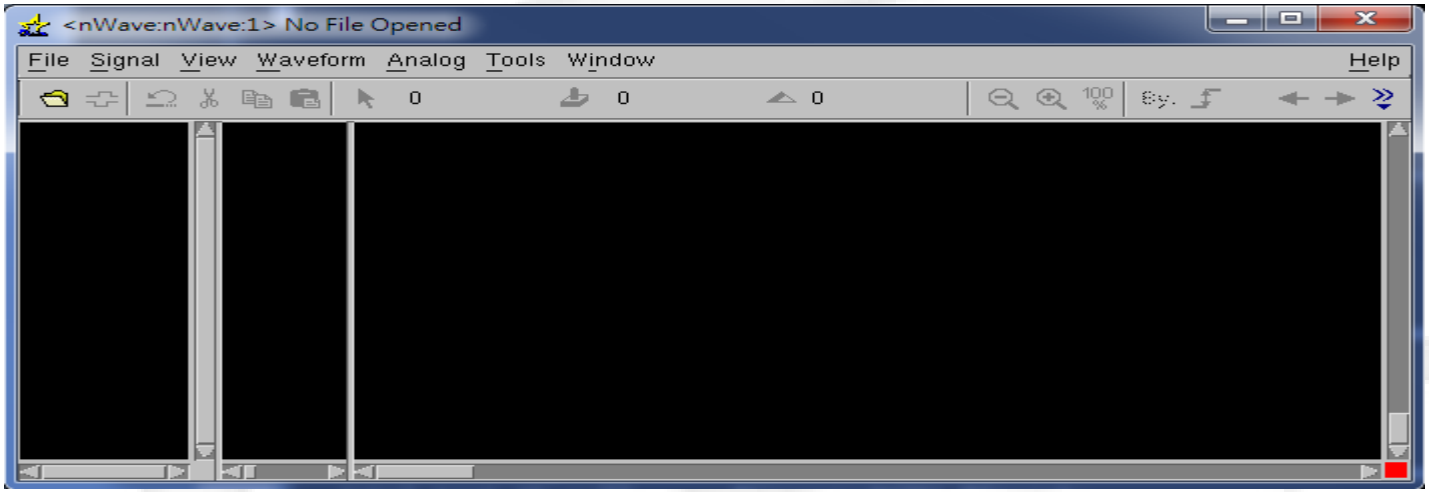
nTrace :: nWave

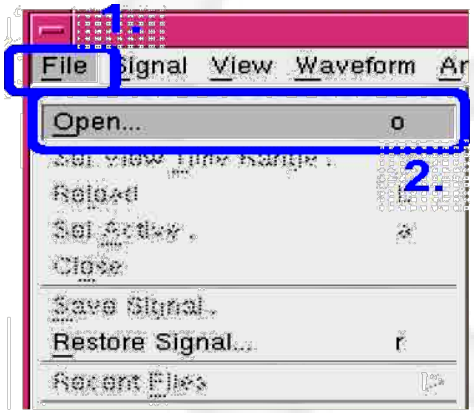
- 接下來的操作，需要利用模擬器所產生的資料(.vcd)，用 “nWave”，來顯示訊號波形。有兩種作法:
  - ➔直接利用nWave來開啟波形，有三種方法打開nWave:
    - ◆按nTrace工具列中的New Waveform Icon.

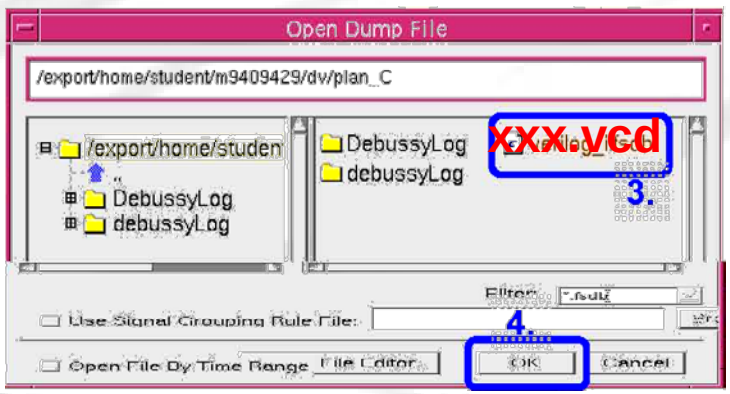
    - ◆(nTrace) *Tools➔New Waveform.*

    - ◆%nWave & (注意大小寫)

nTrace :: nWave

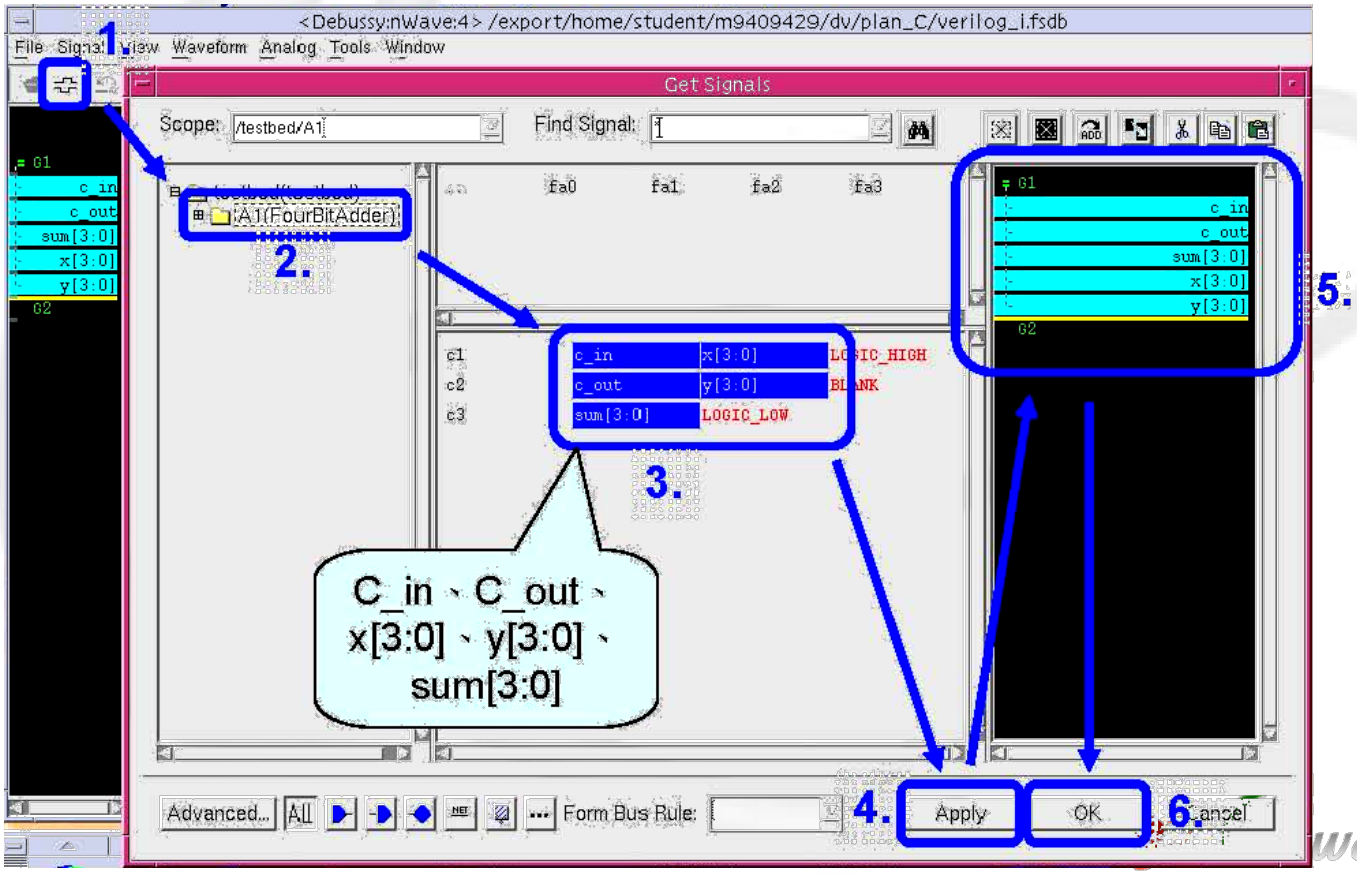






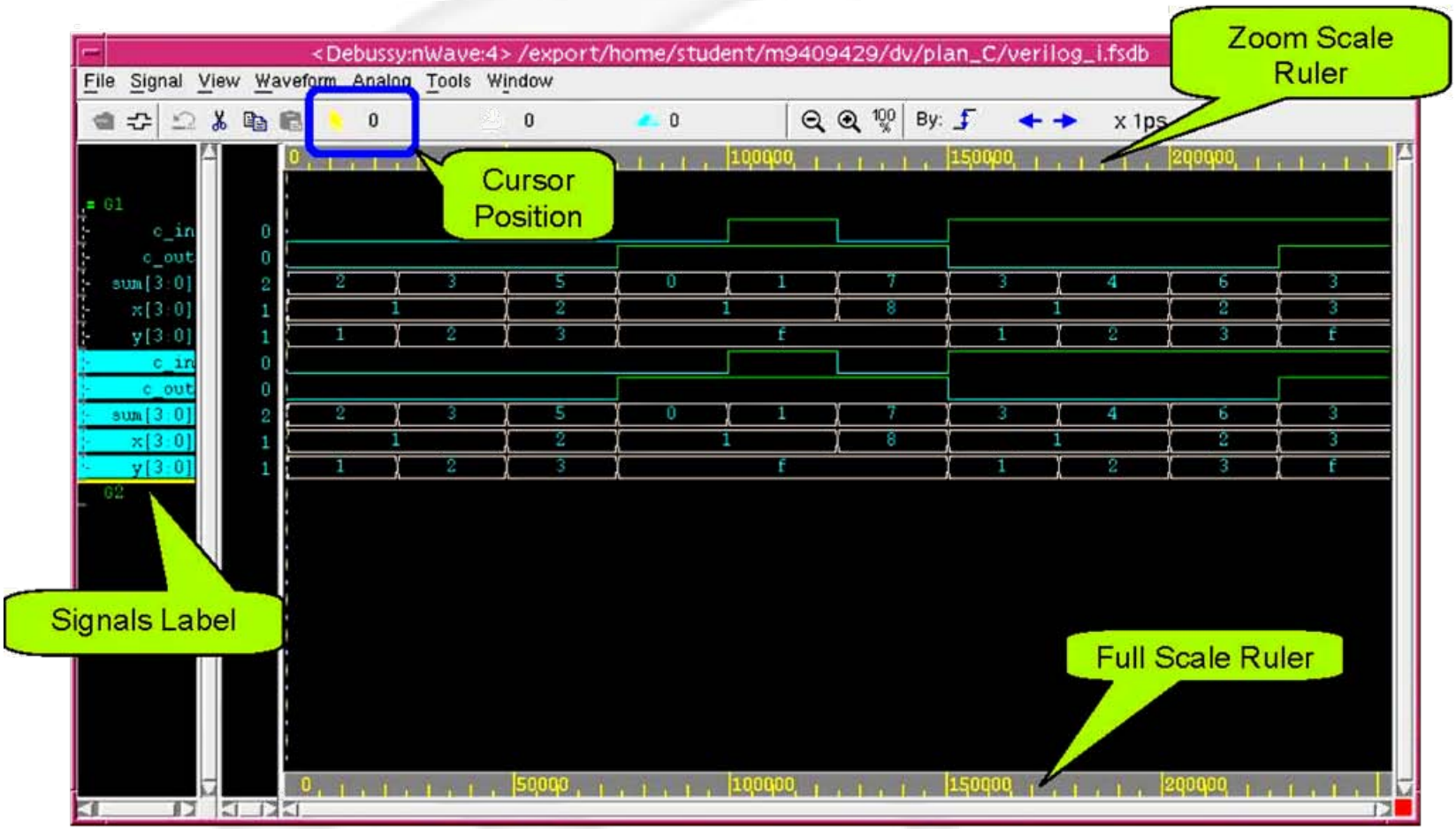
nTrace :: nWave

- 接著按**Get Signals icon**，此時就會看到有訊號可以讓你選擇了。
  - ➔如果你看不到訊號，把想觀察的**design(A1)**，直接從**(nTrace) Hierarchy browser**拖進**nWave**就可以了。



nTrace :: nWave

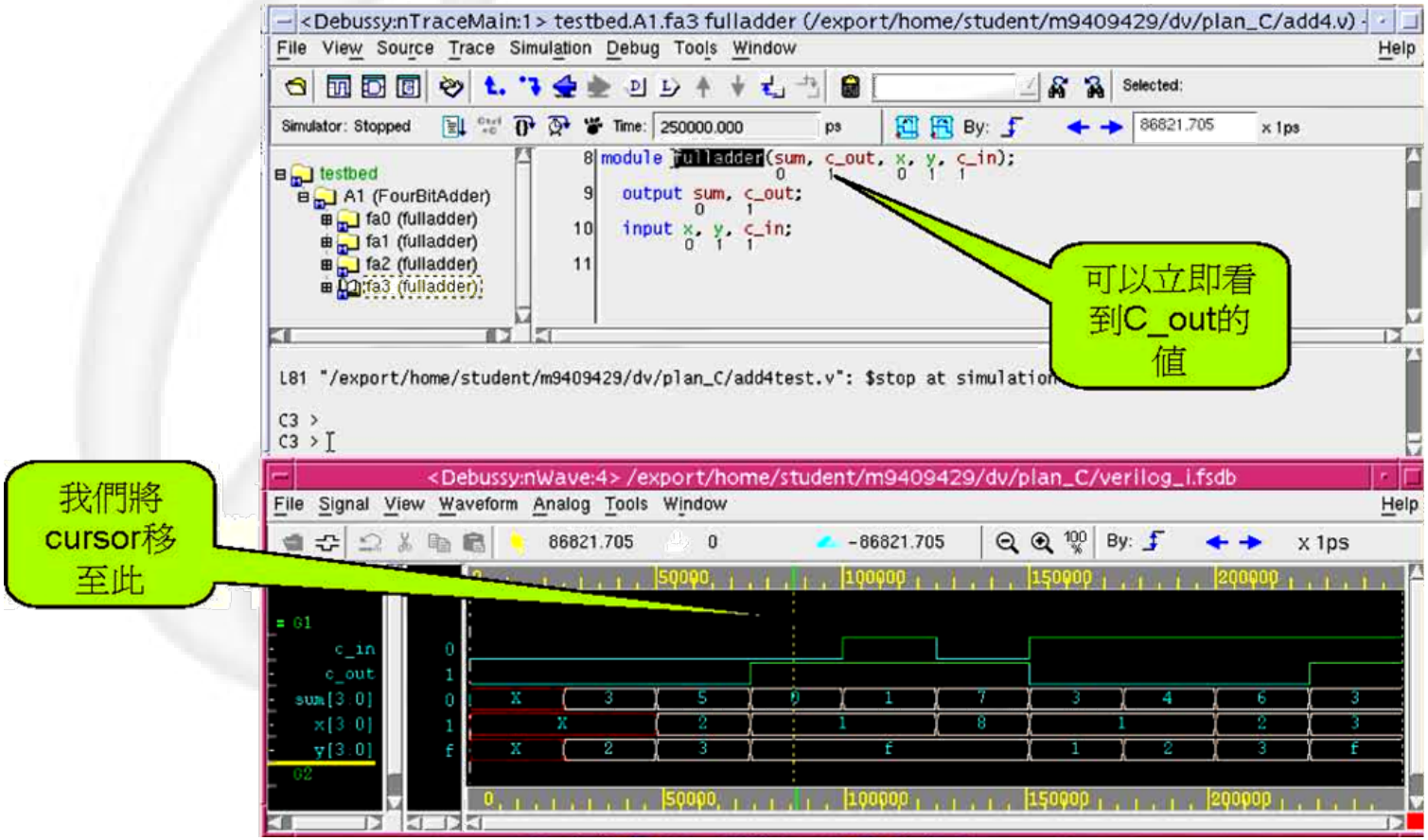
- (nWave) *View➔Zoom➔Zoom All*



nTrace :: nWave

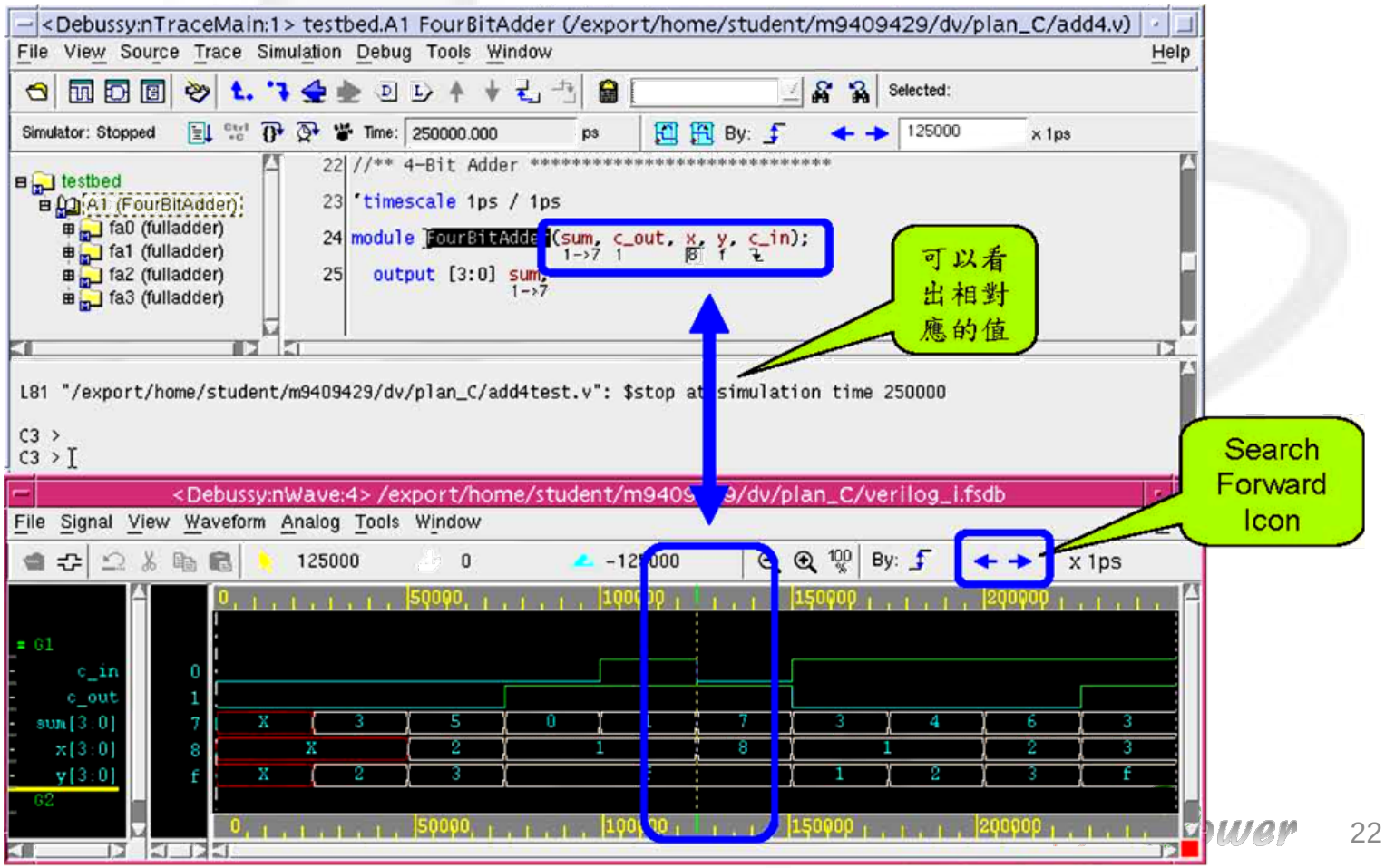
- 啟動**Active Annotation**功能: (nTrace) ***Source*➔*Active Annotation***能夠在**nWave**選擇訊號觸發緣，同時在**nTrace**的**source code**的所有訊號符號下方，直接看到數值得變換。

- 在**nWave**雙擊想觀察其觸發狀況的訊號 (如**c_out**).



nTrace :: nWave

- 從(nTrace) Hierarchy browser雙擊A1(FourBitAdder)，按Search Forward icon，看看在nTrace與nWave的變化。



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Thanks for your participation and attendance ! !