N26F300
VLSI SYSTEM DESIGN
(GRADUATE LEVEL)

Fall 2010

Exams

- Schedule
  - Midterm exam: Thursday, Nov 04, 2010
    - ➔ **Thursday, Nov. 18, 2010**
  - NO final

- There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for make-up exams).

Final Project

- **Schedule**
  - Proposal presentation (11/18, Thu.) → (11/25 , Thu.)

    in class
  - Project submission/Demo (1/20, Tue.)

    Due 09:00 @Moodle ;

    Demo: 10:00 ~ 18:00 @EE95312
  - Project Presentation (1/22, Thu.)

    09:00 ~ 12:00 @ EE95312
- **Topic**
  - **Design a general pipeline processor that can work with a compiler and communicate with external modules (either memory or accelerators) via on-chip buses**

Basic Requirements

- Pipeline and Andes (or equivalent processor) compatible
- ISA must workable with a compiler and a debugger
- >=50 MHz for post-synthesized version
- >=30 instructions
- Non-ideal memory latency (for both data and instruction mem), 4 times of processor speed or >=80ns
- Interrupt-based IO
- Sort 100 numbers and Fibonacci F_{100}
- A sequence of1000 instructions for a specific applications

Advanced Requirements

- Extra 20 instructions
- Stack or mechanisms to facilitate function calls or recursive calls
- Forwarding, Cache, DMA, AHB
- nLint
- Layout, post-layout simulation
- O.S. booting

Tutorials on 10/21-11/04-11/11

- Contents
  - 10/21 AndeSight
  - 11/04 Advanced Design Vision and Basics
  - 11/25 nLint
- Location
  - 9:10-11:20 Regular lecture session
  - 11:20-noon Tutorial