Lab 2 Handout

Objectives:

To design the CPU controller. Refer to the “SMILE_CPU_lab2.ppt”.

Practical:

1) Design a Mealy machine of a sequence recognizer to sample the serial input, D_in, on the falling edge of the clock and assert D_out if a sequence of successive samples of 101 are detected. The machine will have the synchronous reset action and an input control signal to enable the machine to carry out the operation.

2) Design a controller unit that is able to decode an input instruction as shown in Fig. 1 and control the datapath unit designed in Lab 1 practical (3) to carry out the designated operation. Develop a testbench that includes the instructions with the format as shown below to verify the overall system.

```
0011_10__00000_0000_1101__00000_0000_0000 //ADD R0=R0+4'b1101
0011_10__00000_0000_1100__00000_0000_0001 //ADD R1=R1+4'b1100
0011_10__00000_0000_1000__00000_0000_0010 //ADD R2=R2+4'b1000
0011_10__00000_0000_0100__00000_0000_0011 //ADD R3=R3+4'b0100
0011_10__00000_0000_0010__00000_0000_0100 //ADD R4=R4+4'b0010
0011_10__00000_0000_0001__00000_0000_0101 //ADD R5=R5+4'b0001
0011_10__00000_0000_1001__00000_0000_0110 //ADD R6=R6+4'b1001
0011_00__00000_0000_0000__00000_0000_0001 //ADD R1=R1+R0;
0100_00__00000_0000_0000__00000_0000_0001 //SUB R1=R1-R0
0101_00__00000_0000_0000__00000_0000_0001 //AND R1=R0 & R1
```

Fig. 1 Input instruction in binary format, i.e., machine code