N26F300
VLSI System Design
(Graduate Level)

Fall 2008

Instructor & TA

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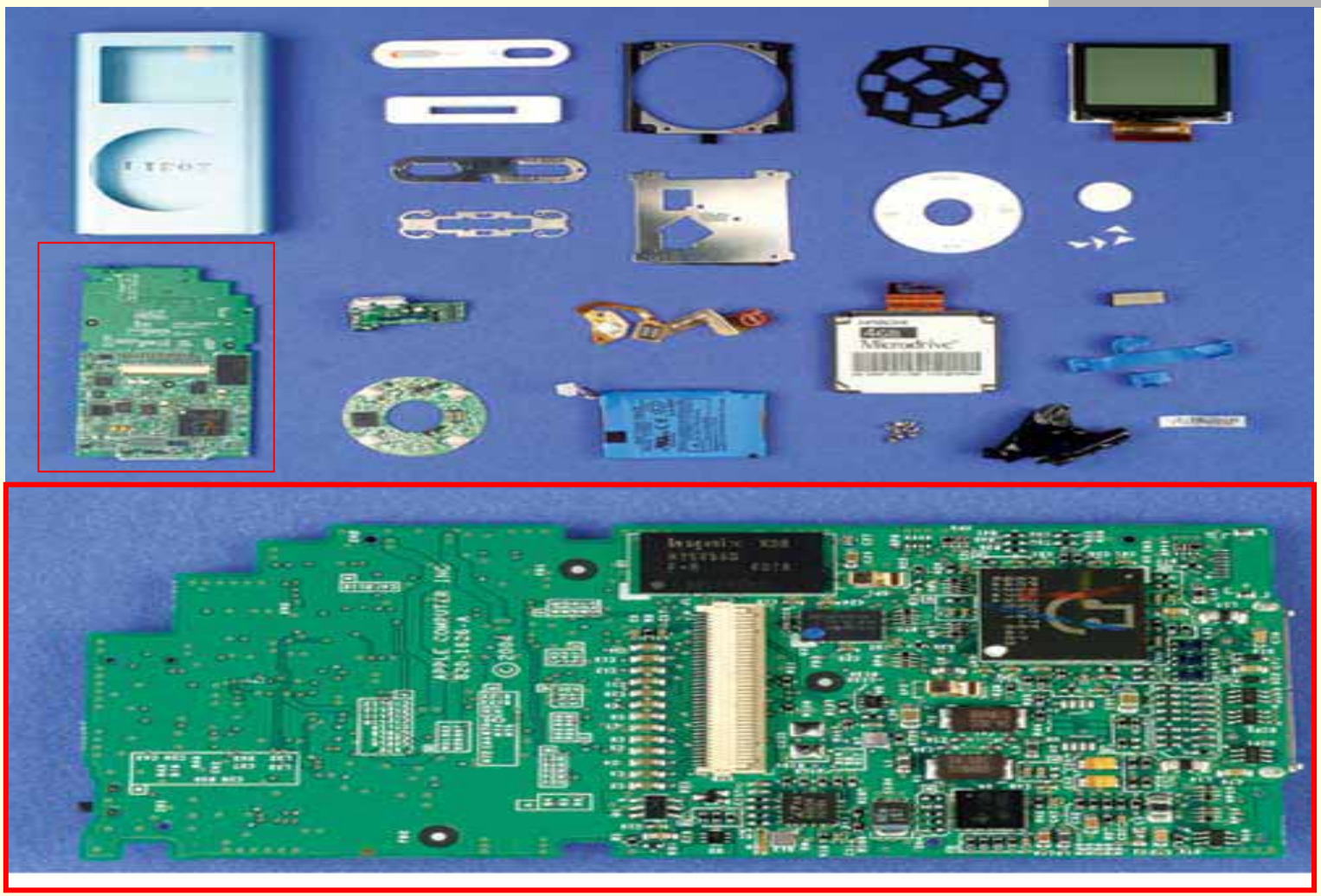
Thur. 20:00--21:00 EE95604

Electronic Device: iPod

ipod

Source: pc.watch.impress.co.jp

Components Inside iPOD



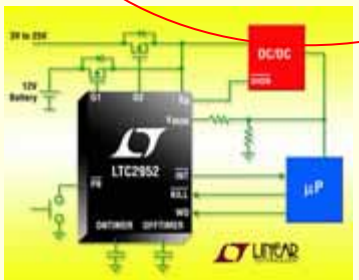
Source: www.elecdesign.com

6 Key Components of iPod

Processor ?? / ARM ??

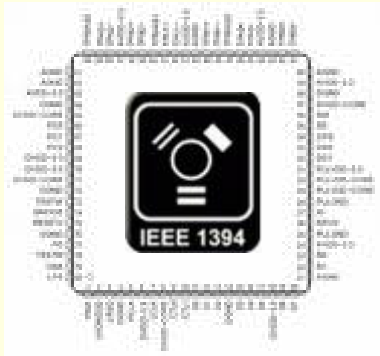
Battery/Sony

Codec / Wolfson



Power Management /
Linear Technology

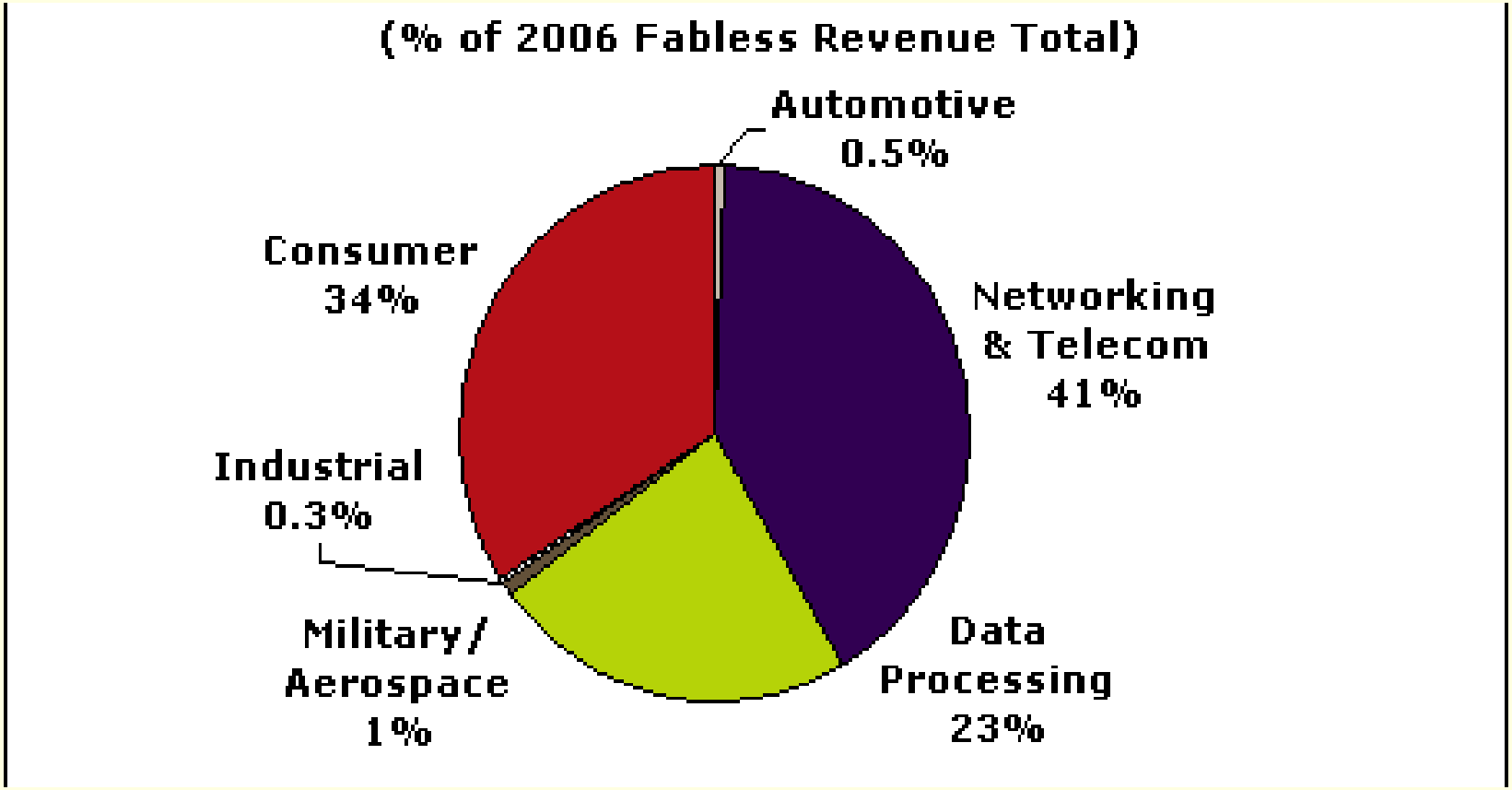
DAC / Wolfson



Firewire / Texas Instrument

Disk Drive / Toshiba

Public Fabless End-Markets Breakdown



Source: www.fsa.org

Top 10 Fabless Companies in 2006

Company		2006 Revenue (US millions)
1	QUALCOMM	$4,331.0
2	Broadcom	$3,667.8
3	ScanDisk Corporation	$3,257.5
4	NVIDIA Corporation	$3,068.8
5	Marvell Technology Group Ltd.	$2,237.6
6	LSI Logic	$1,982.1
7	Xilinx, Inc.	$1,871.6
8	MediaTek Incorporation	$1,624.5
9	Altera	$1,285.5
10	Conexant Systems	$985.6

Source: www.fsa.org

Course Objectives

- Provide fundamental design concepts
  - Modeling systems using Verilog-HDL
  - Digital IC design flow using modern CAD tools
  - Design of synchronous systems
  - Synthesis of HDL
- Establish design and analysis skills for
  - Multi-cycle architecture
  - Pipelined architectures

Course Prerequisites

- Digital Logic Design (must)
  - Boolean algebra
  - Logic minimization
  - Arithmetic units (+,-,*, AND, OR, …)
  - Finite state machine
- Computer Organization (must)
  - Multi-cycle CPU
  - Pipeline CPU
  - Cache
- Self-motivation in learning CAD tools and Verilog HDL

Outline

- Basic IC System Design (7 weeks)
  - VLSI System Design Flow
  - Digital Design Using Verilog
  - Synthesis of Digital Logic
- Advanced IC System Design (7 weeks)
  - Design of digital processors
  - Design of application-specific systems

Hours Arrangement

- Lecture
  - Time: Thursday 9:10-noon
  - Location: EE 92127 藹雲廳
  - Most of the weeks except tutorial sessions
- Laboratory
  - Selected weeks
  - Location: SoC Lab (EE 95312@奇美樓)
    or EE 4F CIC 教室 (for tutorial only)
  - Reserved time slots in SoC Lab: TBA
  - DO NOT LOCK TERMINALS. Otherwise, your right will be suspended (7 days, 14 days, etc.)
- NO FOOD or DRINK in the lecture hall or computer labs

Textbooks & References

- **Textbooks**
  - “Advanced Digital Design with Verilog HDL,” Michael D. Ciletti, Prentice Hall, 2003. ISBN: 0-13-089161-4
- **References**
  - “Computer Organization and Design: The Hardware/Software Interface,” 3th ed. by David A. Patterson and John L. Hennessy, Morgan Kaufmann Pub., 2005. ISBN: 981-2592-17-2
  - “Verilog HDL: A Guide to Digital Design and Synthesis,” 2nd ed. by Samir Palnitkar, Prentice Hall, 2003. ISBN: 0-13-044911-3
  - “Digital Design: An Embedded System Approach Using Verilog,” by Peter J. Ashenden. Weste and David Harris, Morgan Kaufmann, 2008. ISBN: 978-0-12-369527-7

Grading Policy

- **Grading will be based on the following items:**
  - Participation
  - Homework assignments
  - Quizzes and Exams
  - Final project report/demo

Homework Assignments

- Principles
  - Help you to learn the materials
  - Promote self-motivated learning capability as a graduate student
  - Focus on your learning and self-evaluation
- Ideas
  - Longer period of time for an HW assignment
  - A series of small labs as homework
  - A contest problem as homework
  - A project-oriented homework

Homework Assignments

- 2 ~ 4 homework assignments
- Submission electronically through the course website before the specified time and date
- If you fail to do so, your assignment is considered OVERDUE and gets NO credit.
- An EXTRA paper copy needs to be delivered in class

Exams

- Schedule
  - Midterm exam: Thursday, Nov 06, 2007
  - NO final

- There will be no make-up exams (in very special circumstances, written excuse and official proofs are required for make-up exams).

Final Project

- Principles
  - Use learned design skills for your target applications
  - Need team work
  - Promote self-tracking capability as a graduate student
  - Focus on end results

- Ideas
  - Propose and present your interested project based on requirements
  - Discuss your team project regularly
  - Emphasize on verified designs
  - Plan and meet your own schedule

Final Project

- **Schedule**
  - Proposal presentation

    Thu 10/23/2008 in class
  - Final report due day

    09:00, Tue 1/20/2009
  - Demo:

    10:00 ~ 18:00, Tue 1/20/2009
- **Topic**
  - **Design a general pipeline processor or an application-specific accelerator (such as java machine, 3D graphic processor or DSP processor, etc.)**

Course Policy

- Encourage you to discuss assigned problems with peers
- Must complete his/her assignment independently or as specified
- Any person/team who is found to be dishonesty in homework assignments, examines/quizzes, or the project, the involved person(s) will receive an ***"0"*** on the evaluated instrument (*paper, exam, project, homework, etc*.)

Notes

- Please sign your name on the 4th page of course syllabus and give to TAs during break session
- Email your head photo to vsd2008@lpvlsi.ee.ncku.edu.tw.
- When both are submitted, you will be assigned an SoC Lab account, which all homework and project will be graded based on tools in this lab.