Lab 3 Handout

Objectives:

Model the function of memory and integrate them into the SMILE CPU design. Refer to SMILE_CPU_lab 3 slides -- Instruction Memory and Data Memory.

Practical:

Please complete the following exercises.

1. Please add a 32x32bit instruction memory to SMILE designed in Lab2. Load the following machine code into the instruction memory and modify the controller so that the CPU system could read the sequence of the machine codes from the instruction memory and implement the corresponding operations. The machine code is as below:

```
0011_10__00000_0000_1101__00000_0000_0000 //ADD R0=R0+4'b1101
0011_10__00000_0000_1100__00000_0000_0001 //ADD R1=R1+4'b1100
0011_10__00000_0000_1000__00000_0000_0010 //ADD R2=R2+4'b1000
0011_10__00000_0000_0100__00000_0000_0011 //ADD R3=R3+4'b0100
0011_10__00000_0000_0010__00000_0000_0100 //ADD R4=R4+4'b0010
0011_10__00000_0000_0001__00000_0000_0101 //ADD R5=R5+4'b0001
0011_10__00000_0000_1001__00000_0000_0110 //ADD R6=R6+4'b1001
0011_00__00000_0000_0000__00000_0000_0001 //ADD R1=R1+R0;
0100_00__00000_0000_0000__00000_0000_0001 //SUB R1=R1-R0
0101_00__00000_0000_0000__00000_0000_0001 //AND R1=R0 & R1
0110_00__00000_0000_0000__00000_0000_0001 //OR    R1=R0 || R1
0111_00__00000_0000_0001__00000_0000_0000 //XOR R0=R1^R0
0011_10__00000_0000_1101__00000_0000_0000 //ADD R0=R0+4'b1101
0000_00__00000_0000_0000__00000_0000_0000 //NOP
0100_10__00000_0001_0000__00000_0000_0001 //SUB R1=R1-5'b10000
1000_00__00000_0000_0001__00000_0000_0000 //SLL R0=R0 SLL(R1)
1001_00__00000_0000_0001__00000_0000_0000 //SRL R0=R0 SRL(R1)
0000_00__00000_0000_0000__00000_0000_0000 //NOP
1010_00__00000_0000_0001__00000_0000_0000 //RLL R0=R0 RLL(R1)
0011_10__00000_0000_1010__00000_0000_0010 //ADD R2=R2+4'b1010
0000_00__00000_0000_0000__00000_0000_0000 // NOP
```

2. Design a 32x32bit Data Memory unit for SMILE. Please integrate the Data Memory with the controller, register file, ALU and instruction memory that designed previously. Using the machine codes as listed in Practical 1 (with the addition of SW instructions) to verify the overall design.