VLSI System Design (Graduate Level)
Fall 2008

HOMEWORK I

` Due day: midnight Oct. 27 (Monday), 2008

This is a simplified multi-cycle **(SMILE)** CPU with only 11 instructions. It is to let the first-time CPU designer be familiar with the instruction set architecture, dataflow modeling and controller design. This problem is purposely divided into 4 labs that will guide you to complete the design. Lab1- Lab3 are to model the basic modules. Lab4 is to put all modules together and verify your SMILE. It is expected that you may spend more time on Lab4 than others. Therefore, plan your time wisely.

There will be bonus points for doing extra work for those who like challenges. Partial credits will be given based on level of completeness for bonus parts. Points for this homework are depicted as follows.

BAISC (100 points): Complete a working non-synthesizable CPU design

Bonus-I (+100 points): Complete a working synthesized CPU design

Bonus-II (+200 points): Complete a working synthesized CPU with additional branch instruction

General rules for deliverables

- This homework needs to be completed by INDIVIDUAL student.
- Compress all files described in the problem statements into one zip or rar.
- Submit the compress file to the course website before the due day. **Warning!** AVOID submit in the last minute. Late submission is not accepted.

Grading Notes

- **Important!** DO remember to include your Verilog code. NO code, NO grades. Also, if your code can not be recompiled by TA successfully using tools in SoC Lab, you receive NO credit.
- Write your report seriously and professionally. Incomplete description and information will reduce your chances to get more credits.
- If extra works (like synthesis, post-simulation or additional instructions) are done, please describe them in your final report clearly for bonus points.
- Please follow course policy.

Problem description and deliverables are described in the following.

Problem Description

A Simplified MultI-cycLE (SMILE) CPU, will be designed base on the five labs as indicated below. Synthesis is not mandatory. Bonus points will be given for student who performs synthesis successfully using the constraint file "DC.sdc", which already included in the package.

1. The specifications for instruction set are required to be the same as indicated in the labs (page8 of Lab 1).
2. The data flow of multi-cycle CPU is described in the pps file, "data_flow.pps".
3. Labs below describe the design of a multi-cycle CPU in a step-by-step manner. It could be used as a guide to complete this problem. Most the reference codes are only partially completed. You need to complete the unfilled parts for making them work.

	Title	Details	Documents in each directory
Lab1	-CPU Architecture -ALU -Register Files	Introduction to - CPU architecture - Instruction Decoder - Design of ALU - Design of Register Files.	lab1/SMILE_CPU_lab1.ppt lab1/Lab1_handout.doc
Lab2	-FSM -CPU Controller	Introduction to - FSM Design - Design of CPU controller	lab2/SMILE_CPU_lab2.ppt lab2/Lab2_handout.doc
Lab3	-Data Memory -Instruction Memory	Introduction to - Design of Data Memory - Design of Instruction Memory	lab3/SMILE_CPU_lab3.ppt lab3/Lab3_handout.doc
Lab4	CPU Verification	Verification of design by using assembly codes	lab4/SMILE_CPU_lab4.ppt

Deliverables

1. All CPU Verilog codes including components, testbenches and machine code for each lab exercise.
2. A homework report that includes
    a. A summary in the beginning to state what has been done (such as SMILE CPU, synthesis, post-synthesis simulation, additional branch instruction with verification)
    b. Things need to be included for each lab
        Lab-1. Practical (1)(2)(3)
        Lab-2. Practical (2)
        Lab-3. Practical (1)(2)
        Lab-4 Verification (1)(2)(3)
    c. A block diagram for your completed SMILE CPU indicating all necessary components and I/O pins
    d. Simulated waveforms with proper explanation
    e. Report your maximum simulation speed
    f. Synthesis reports (for Bonus-I)
    g. Post-synthesis simulation waveforms (for Bonus-I)
    h. Report your maximum simulation speed (for Bonus-I)
    i. Additional branch instruction with verification (for Bonus-II)
    j. Conclusion

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