Design Compiler

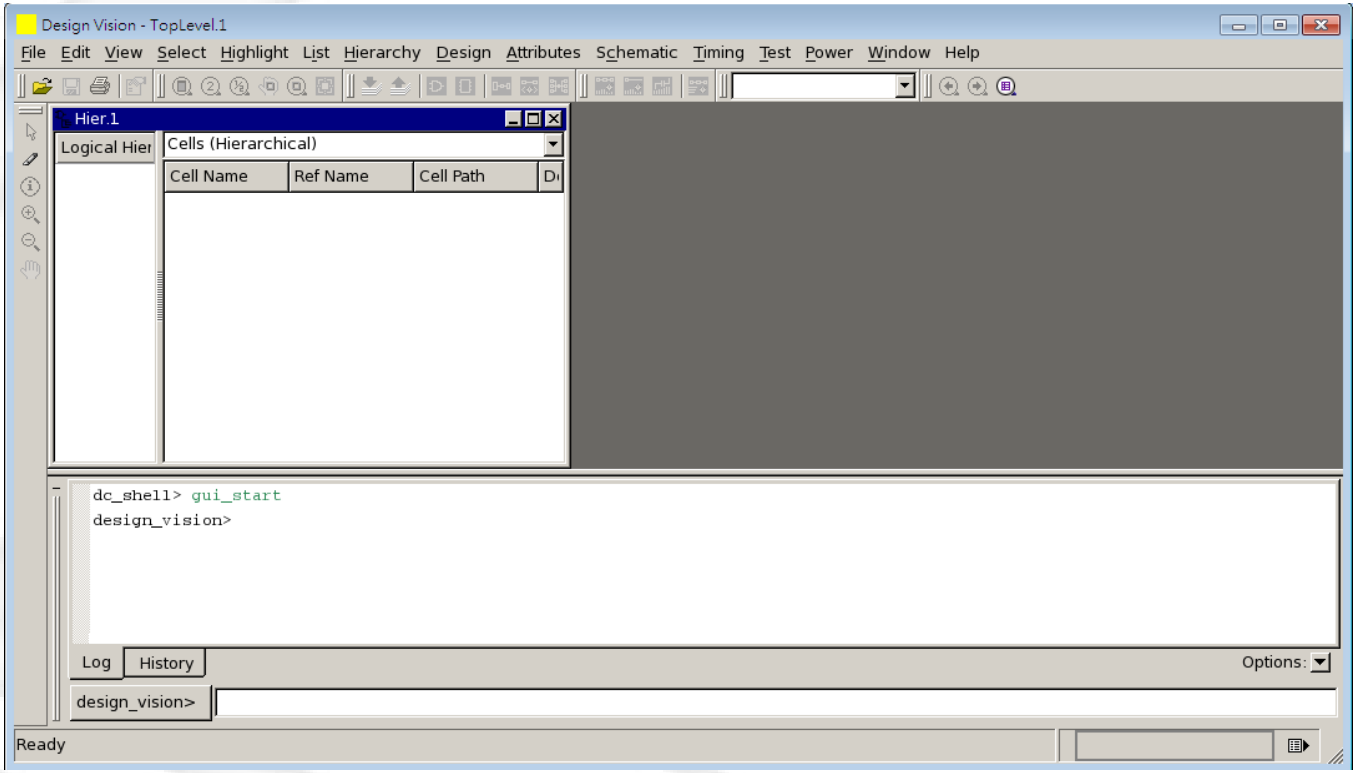
Instructor：Lih-Yih Chiou
TA : Kiwi, Kevin
Date : 2010/09/16

EE

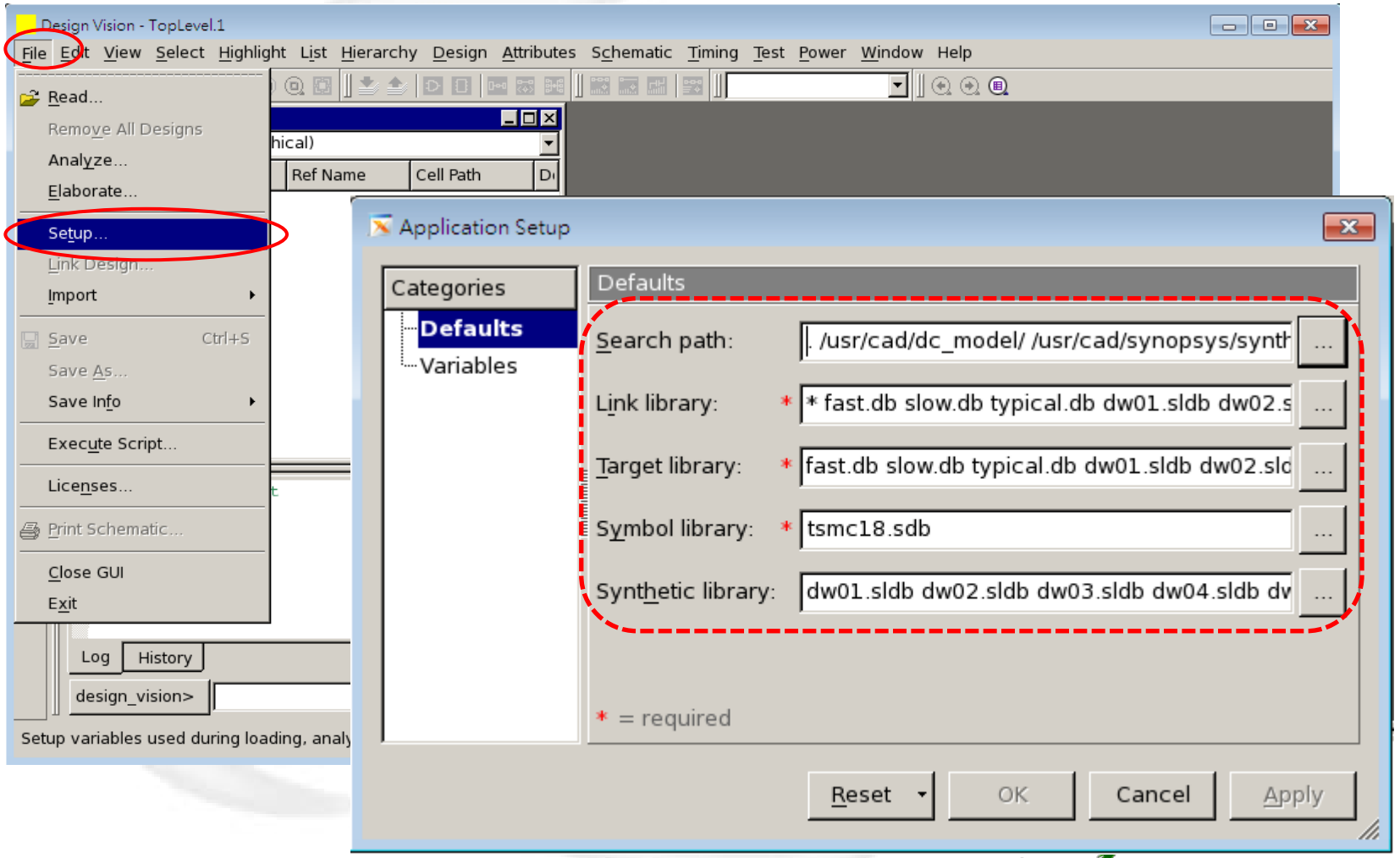
LPHPLAB
VLSI Design LAB

Start to Design Compiler

- **dv &**



Setup libraries (1/2)



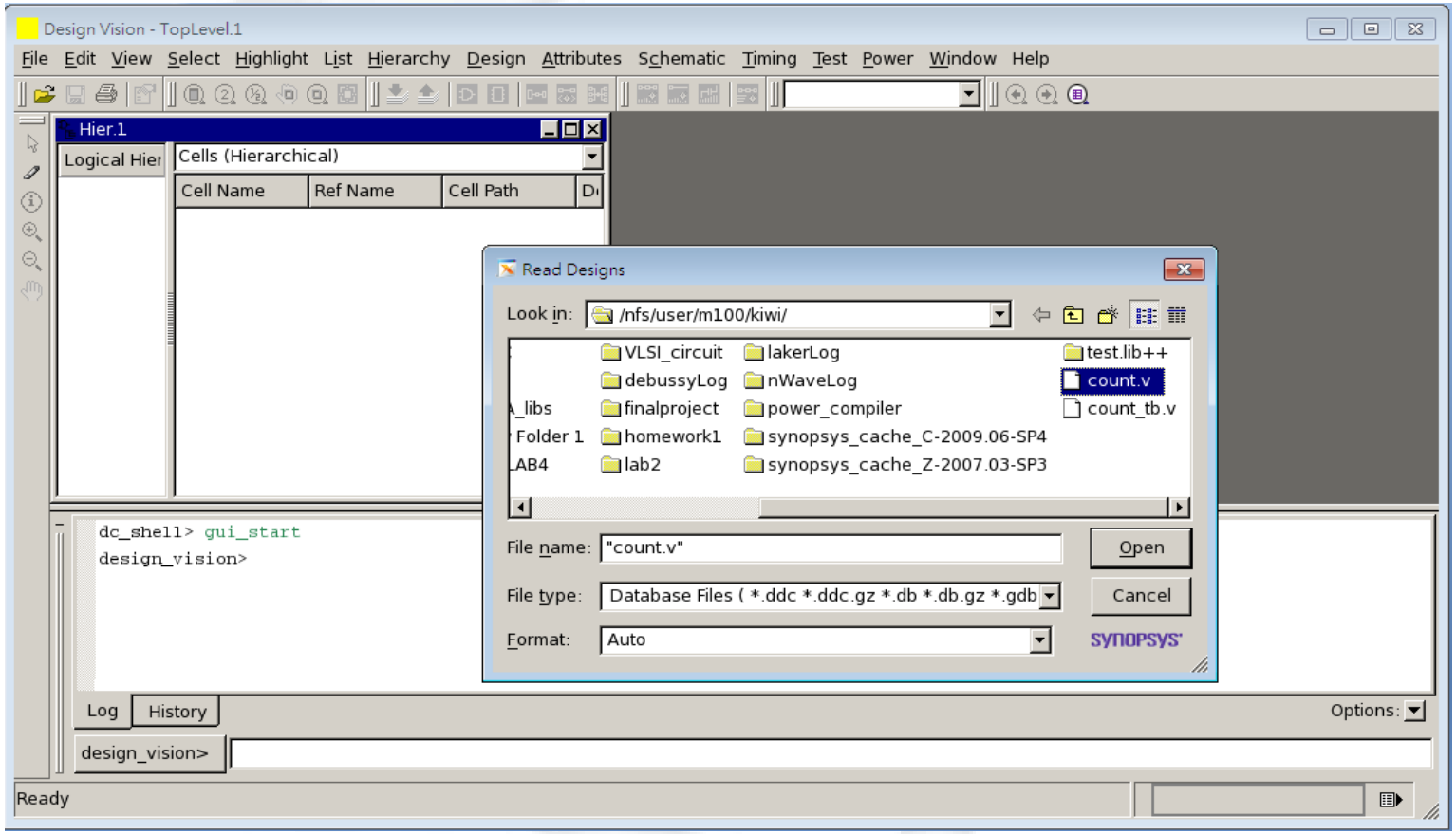
Setup libraries (2/2)

- **.synopsys_dc.setup is a setup file when entering Design Vision**

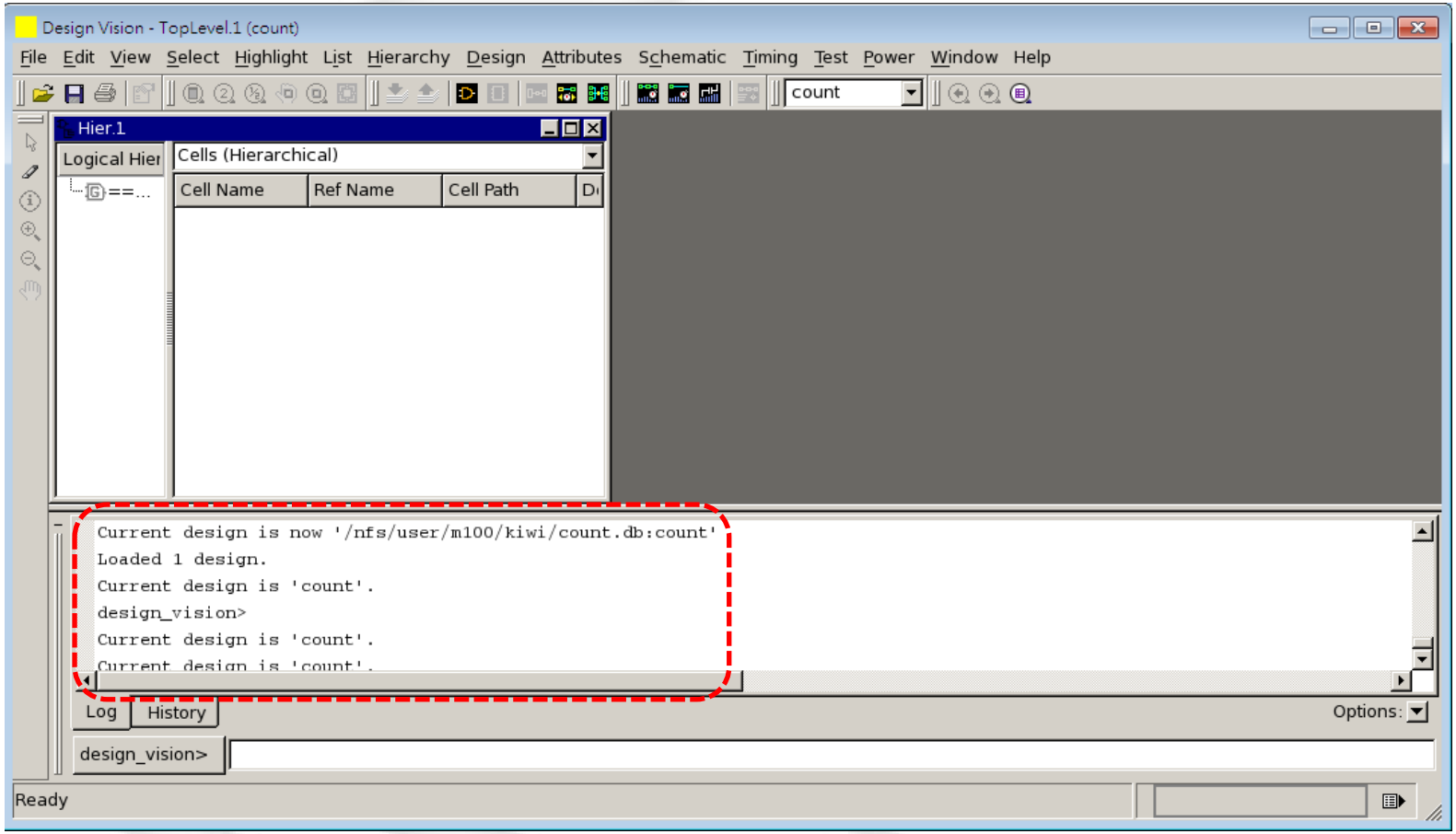
- **set company "NCKU"**
- **set designer "your name“**
- **set search_path "/usr/cad/CBDK018_TSMC_Artisan/CIC/SynopsysDC/db"**
- **set target_library "fast.db slow.db"**
- **set link_library "$target_library"**
- **set symbol_library "tsmc18.sdb“**
- **set_min_lib slow.db -min fast.db ; # for core lib**
- **set verilogout_no_tri true**
- **set hdlin_enable_presto_for_vhdl "TRUE"**
- **set sh_enable_line_editing true**
- **history keep 100**
- **alias h history**

Read file

- **File > Read**

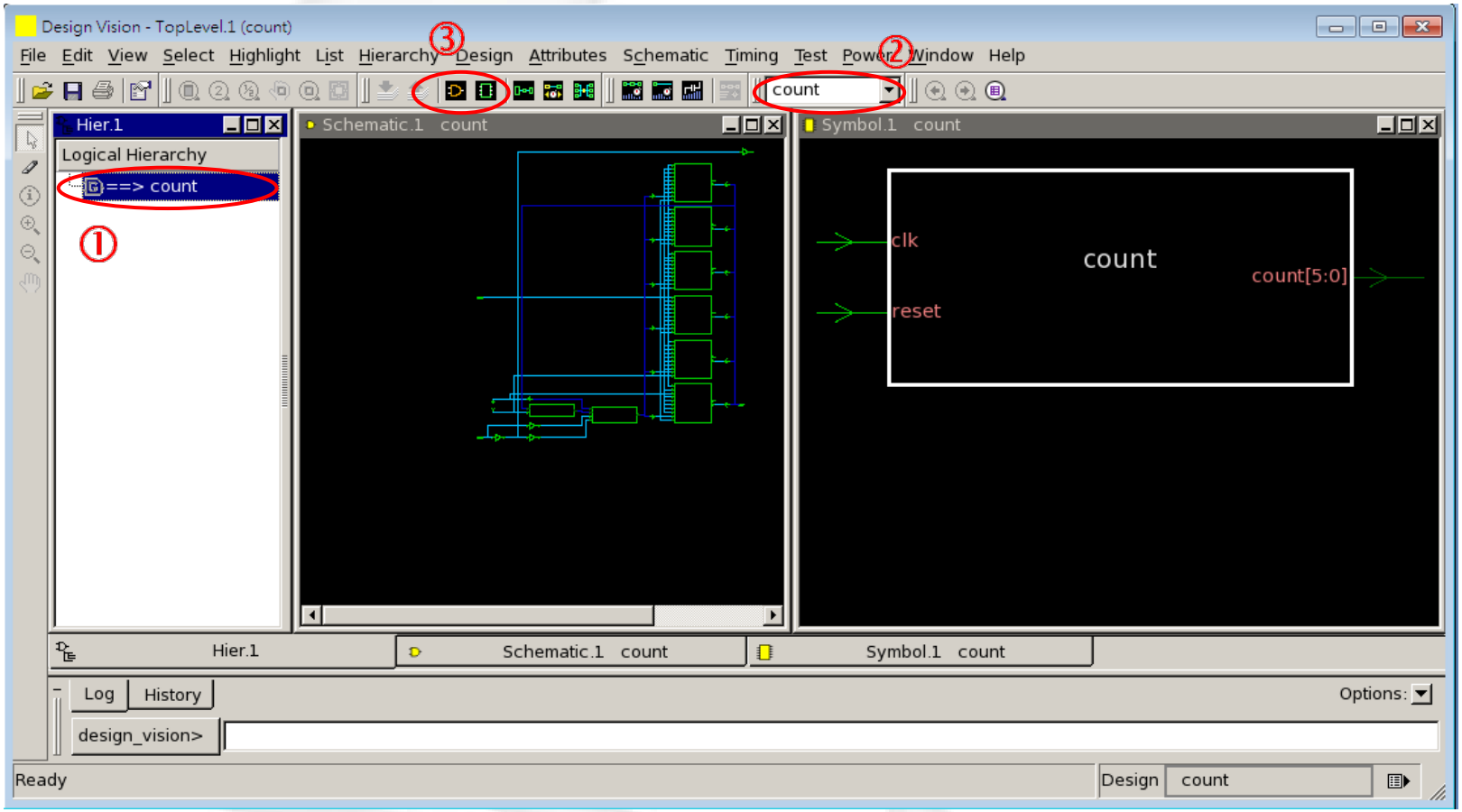


Read File Check



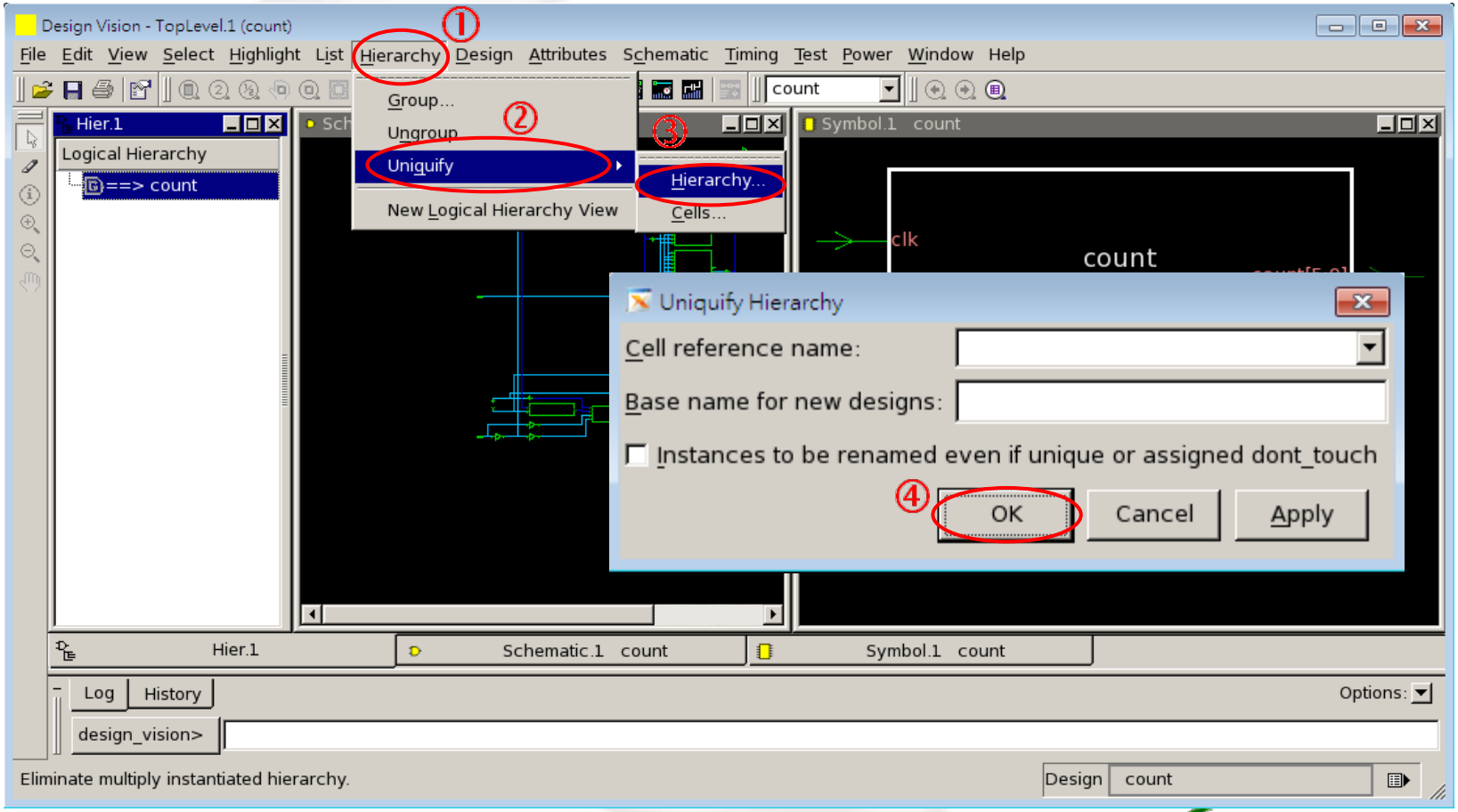
If any errors or warnings exist, you should modify your codes to avoid them.

Symbol and Schematic View



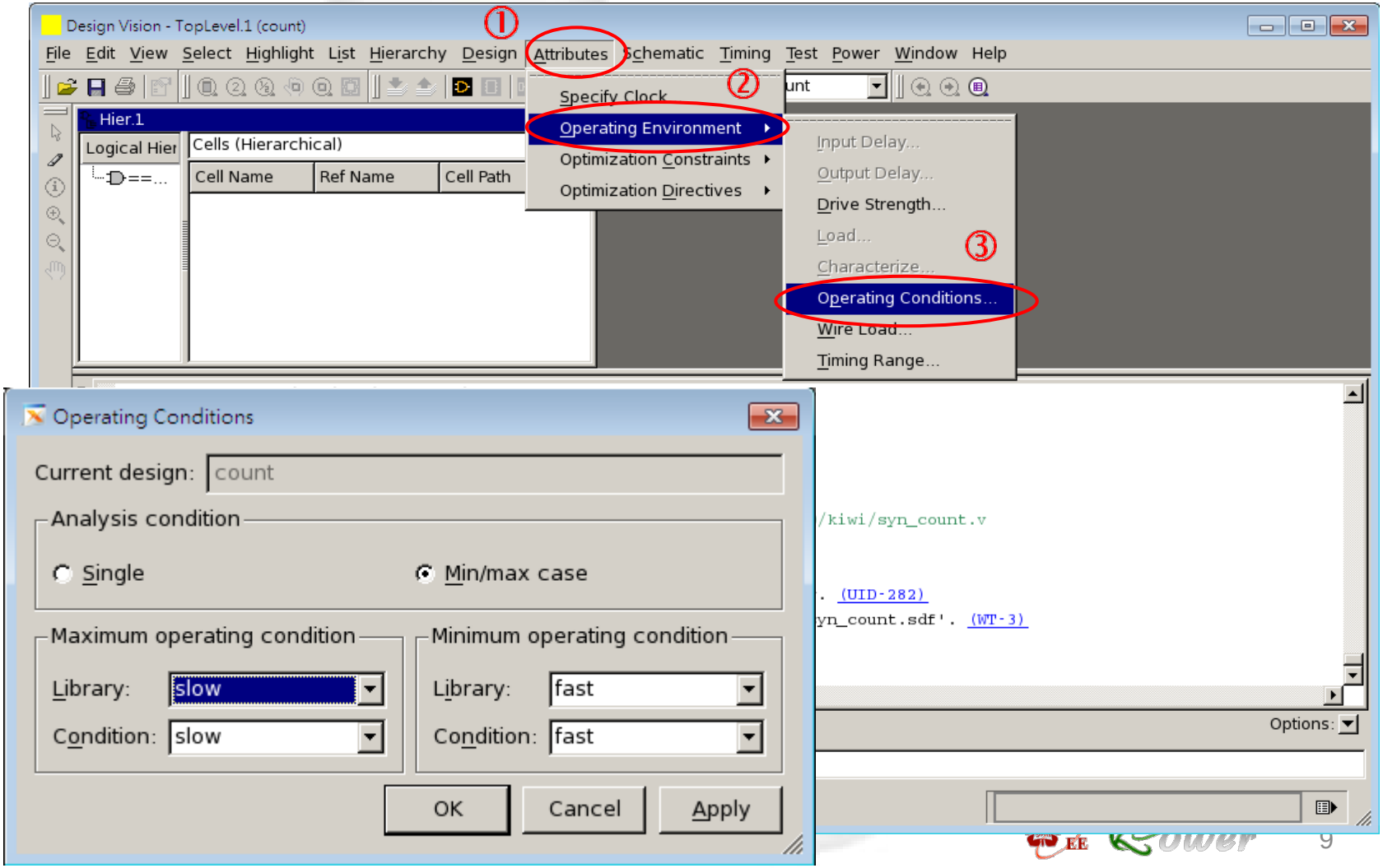
Uniquify

- **Hierarchy > Uniquify > Hierarchy**
- **Objective:** Solving 『multiple design instance』 problem.



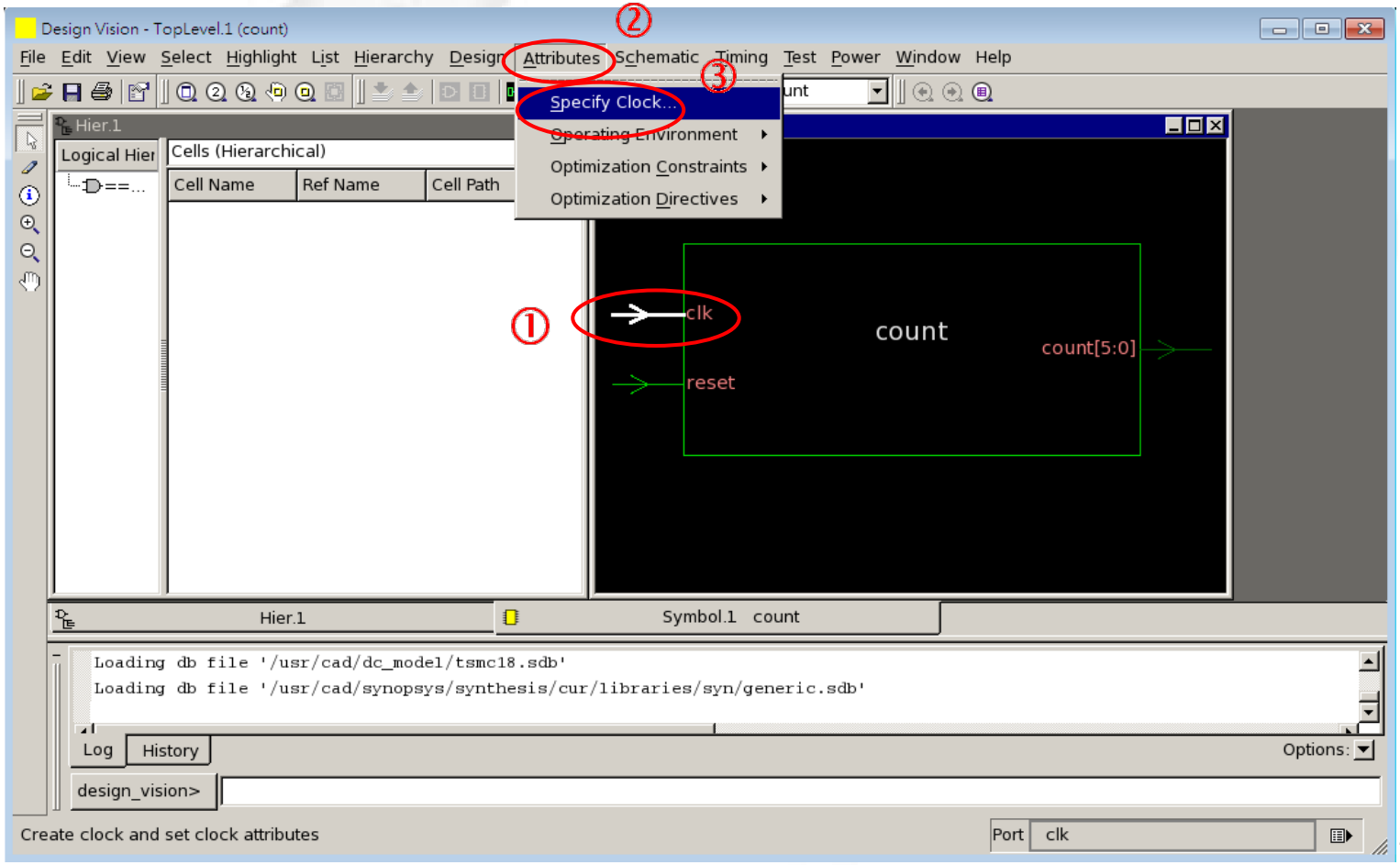
Operating Environment

- **Attributes > Operating Environment > Operation Conditions**



Constraint : Clock (1/2)

1. In the symbol view
2. Choose the clock
3. Attributes > Specify Clock



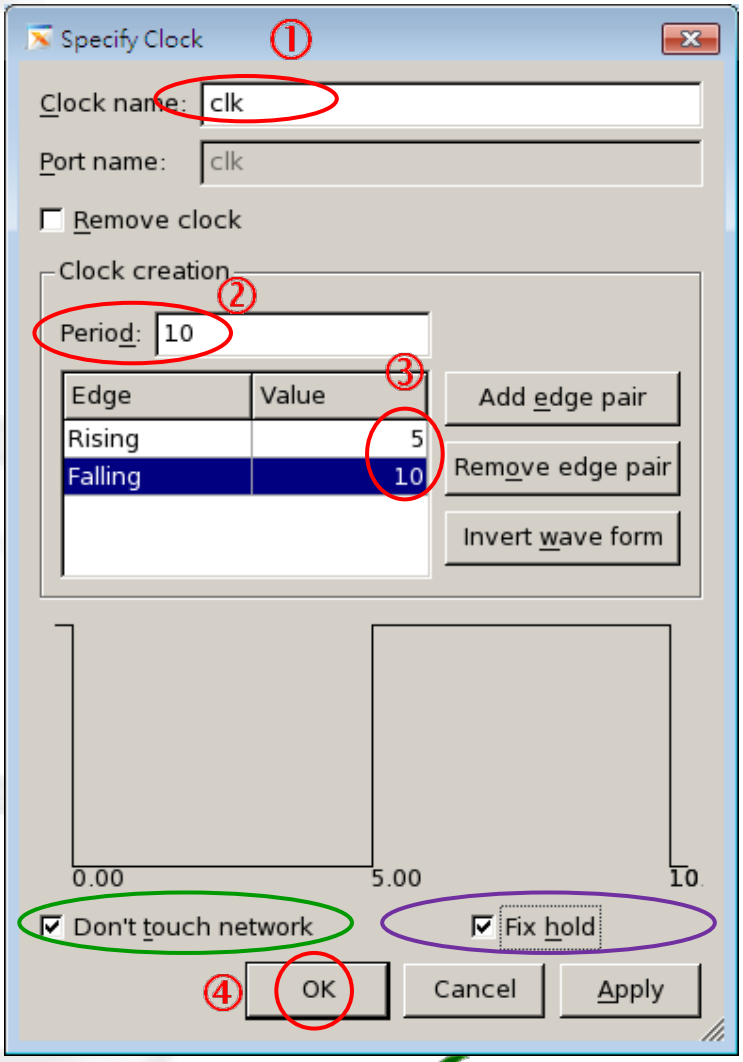
Constraint : Clock (2/2)

- **Don't touch network:**

  The command preserves the nets attached to one or more clock sources during optimization.

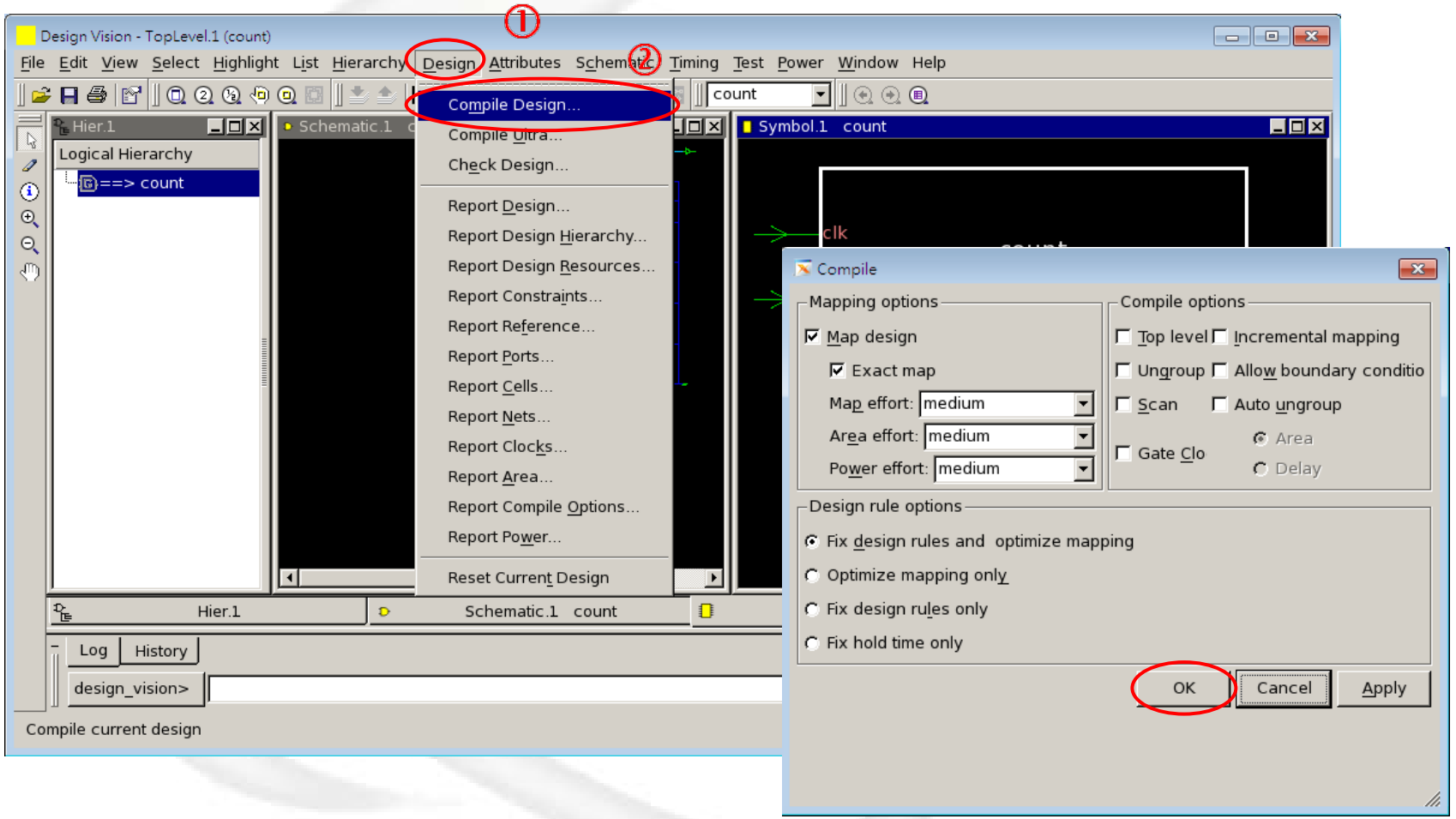
- **Fix hold:**

  The command directs Design Compiler to insert delay to correct hold(minimum path) violations for timing paths that end at registers fed by this clock.



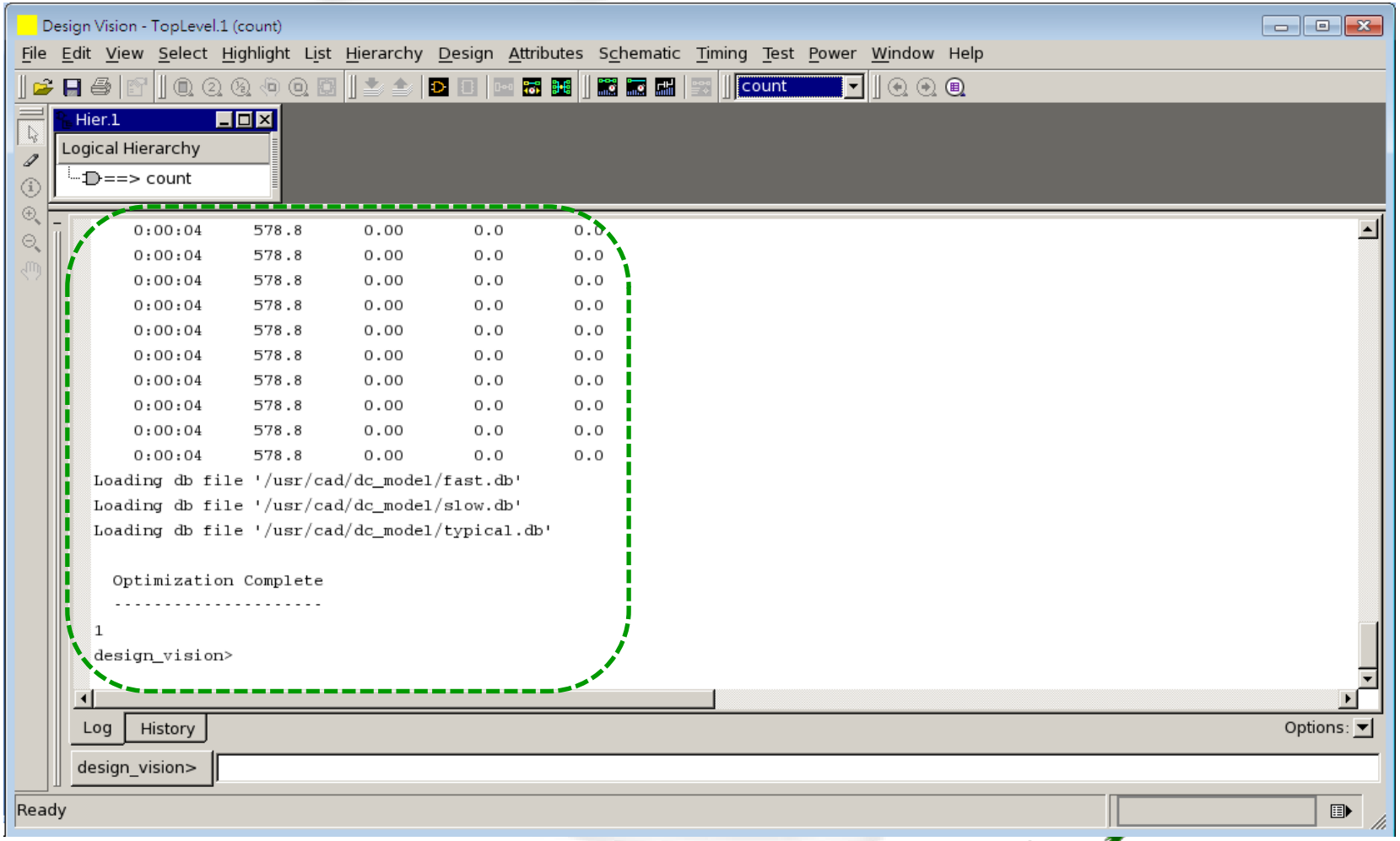
Compile Your Design

- **Design > Compile Design**



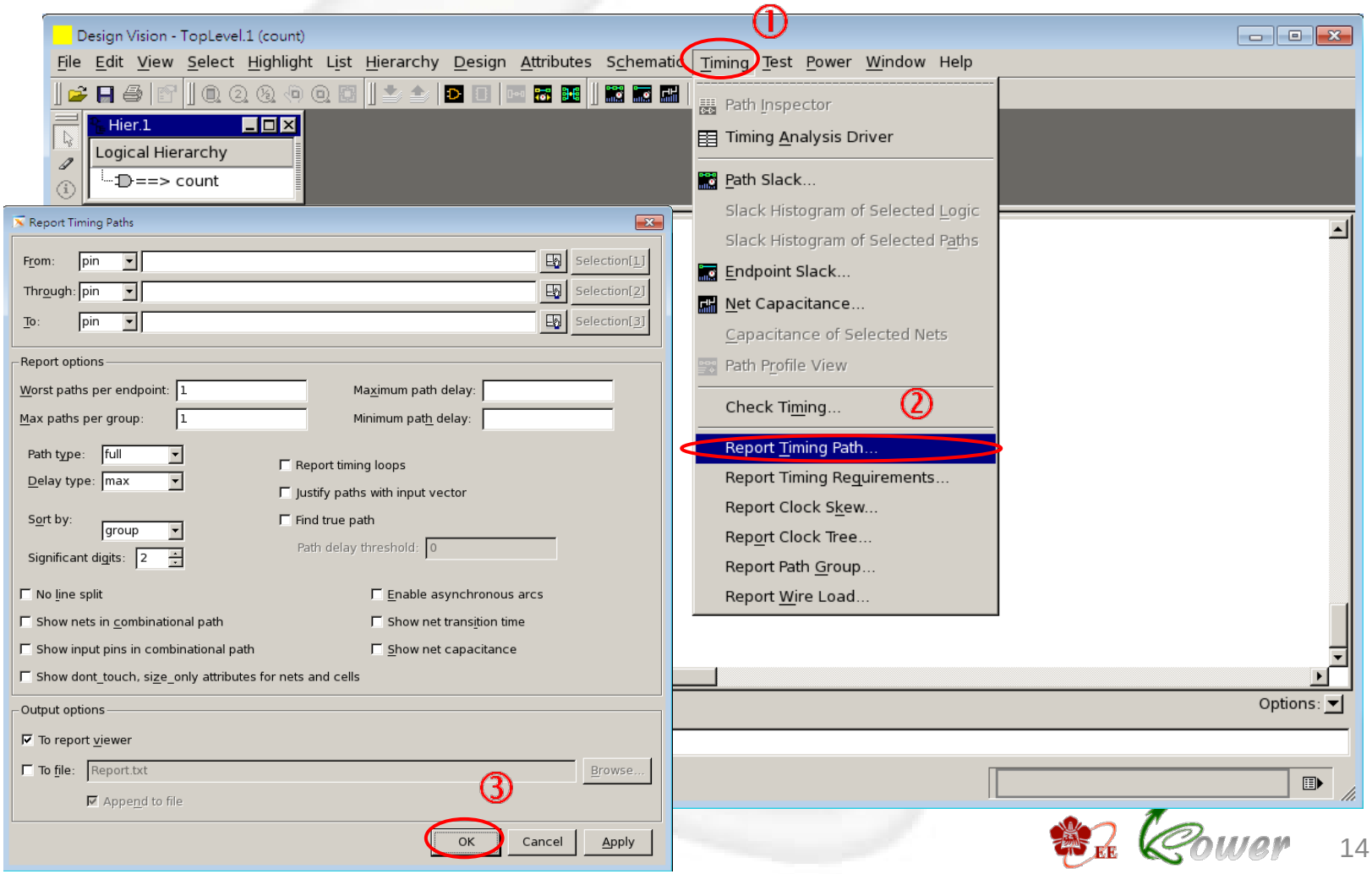
Check Compile Log

- If any errors or warnings exist, which be shown in this window.



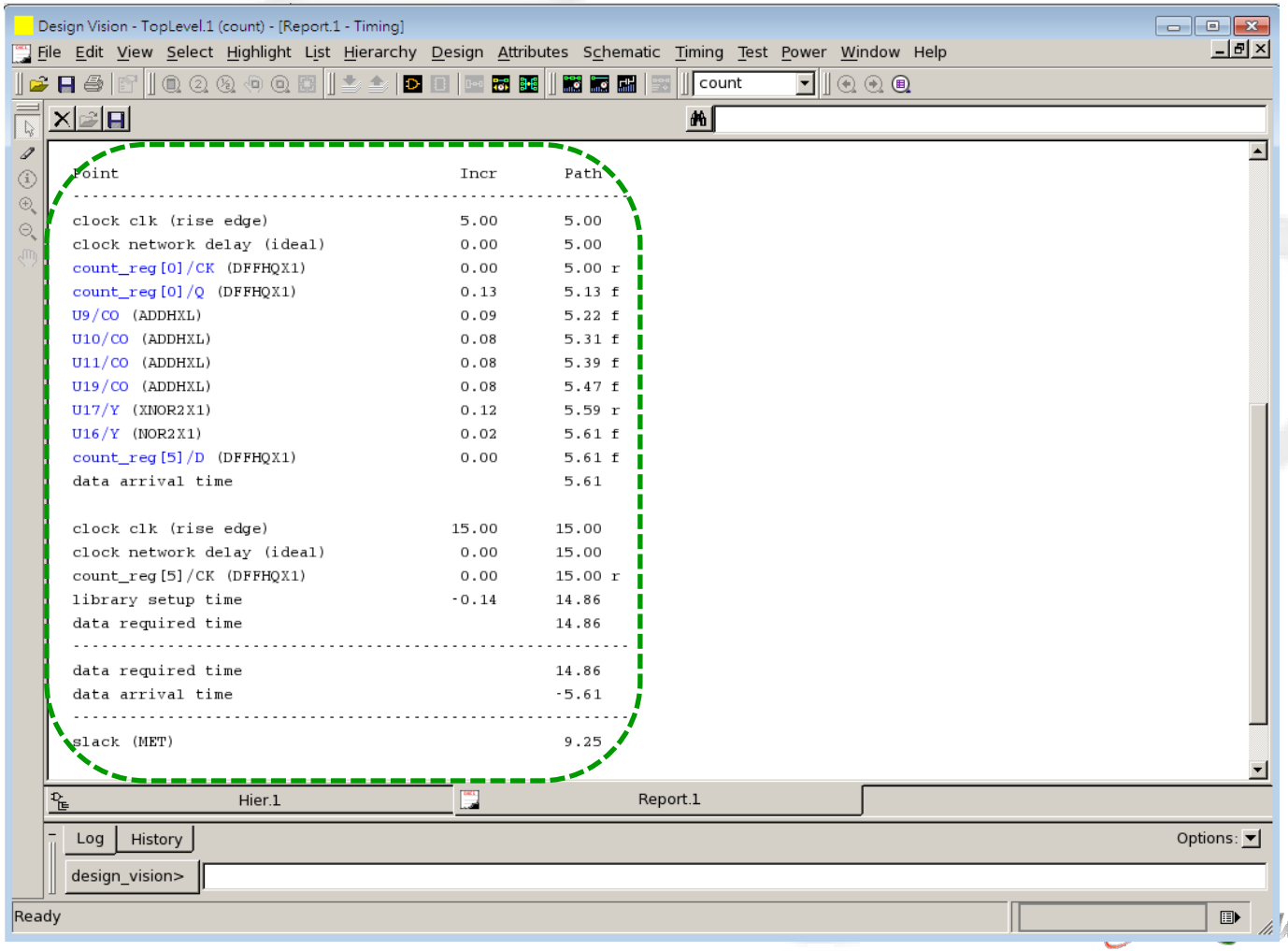
Timing Report (1/2)

- **Timing > Report timing Paths**



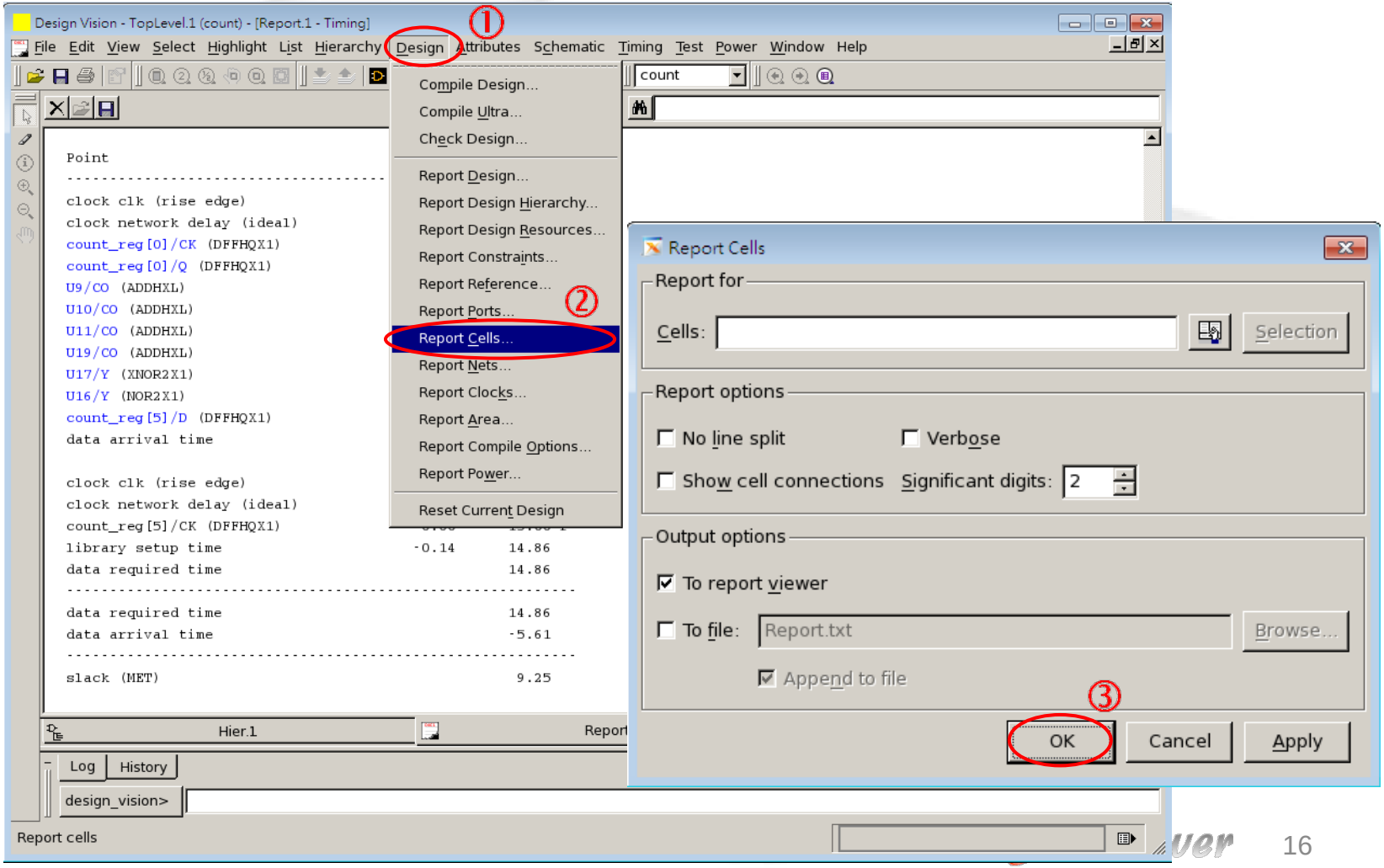
Timing Report (2/2)

- **The report_timing command reports the most critical maximum path (the path with the worst slack).**

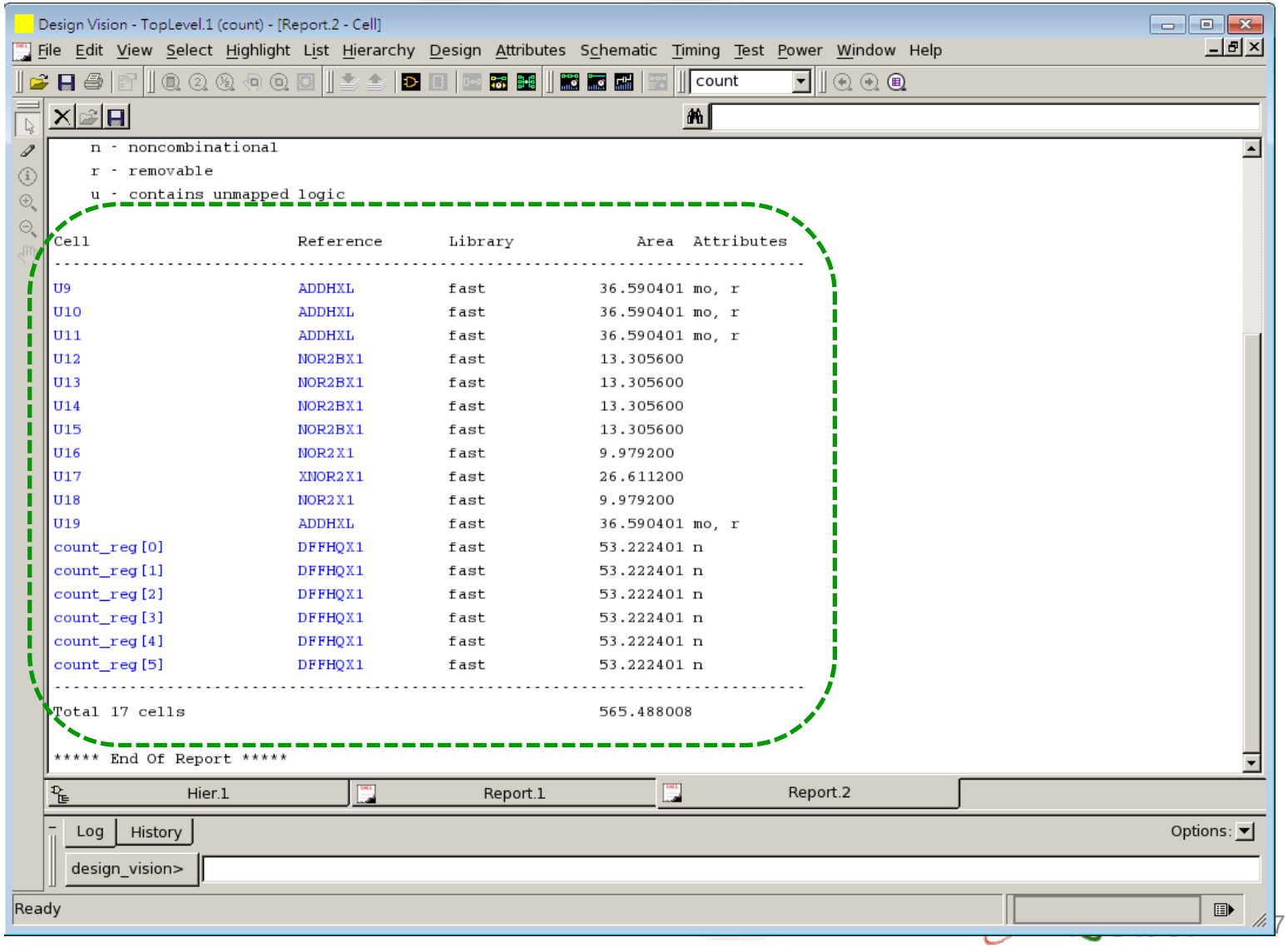


Report cells (1/2)

- **Design > Report cells**

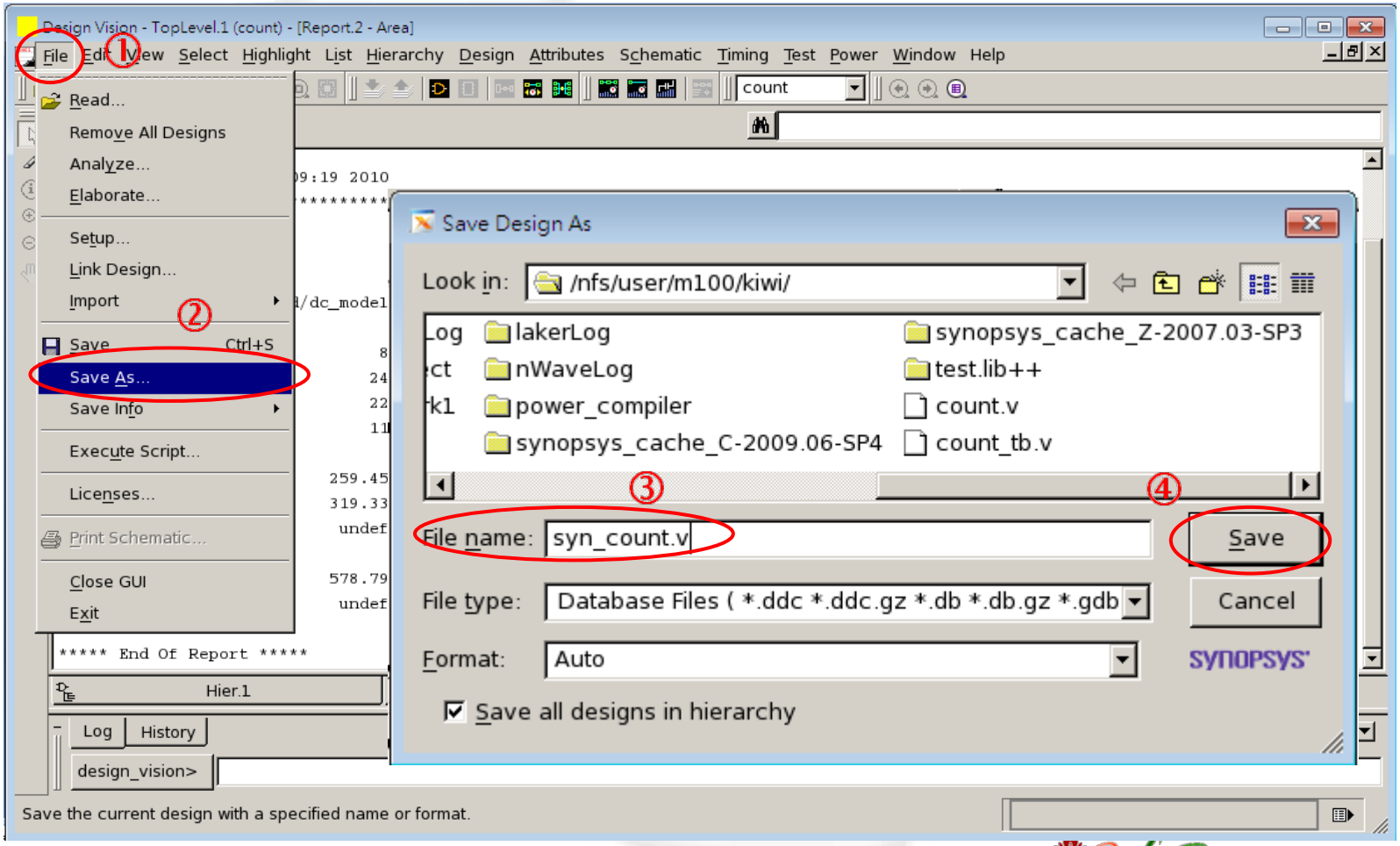


Report cells (2/2)



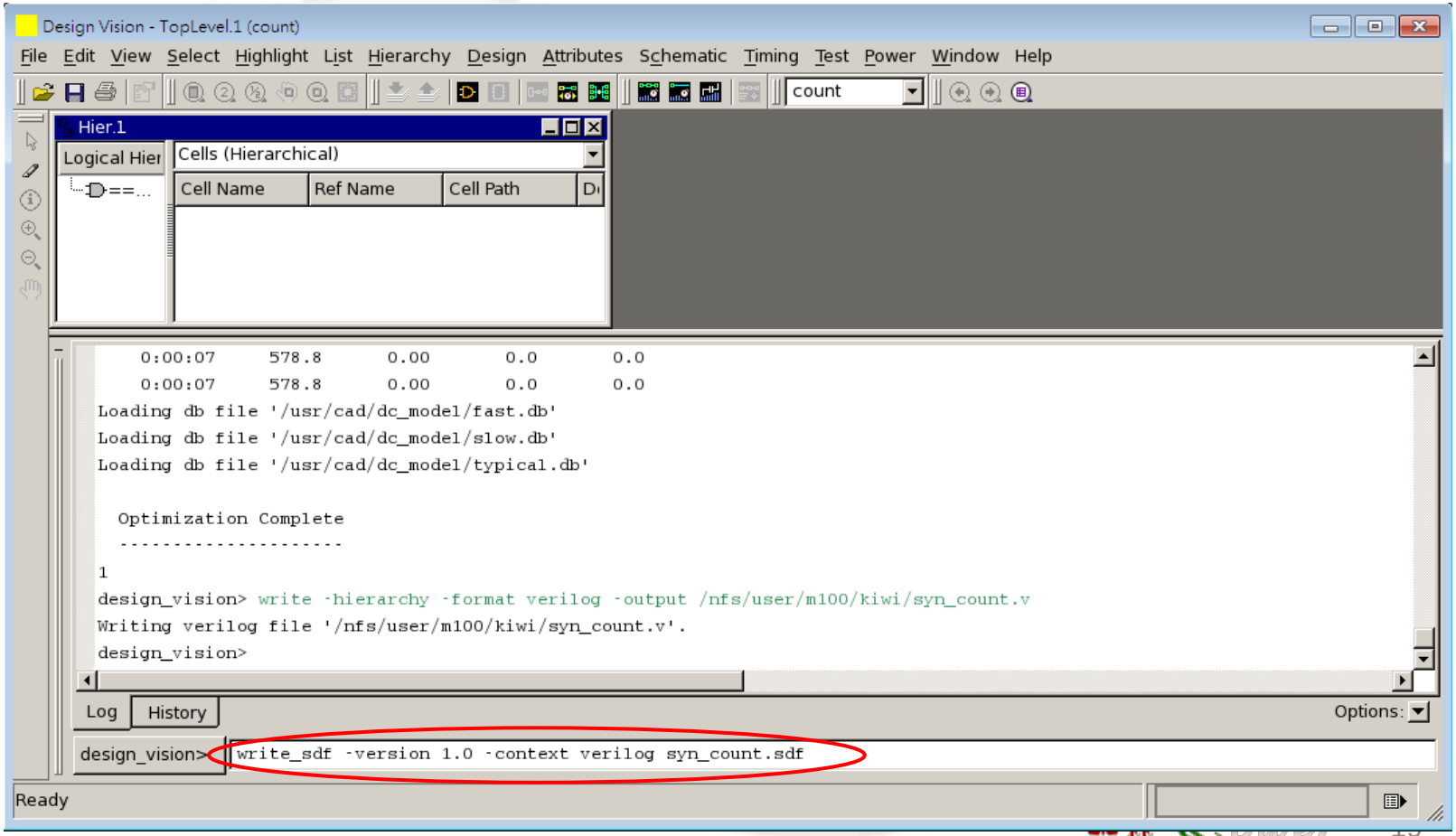
Save Your Design

- **File > Save as**



Save Timing File

- write_sdf -version 1.0 -context verilog syn_count.sdf
- sdf files store timing information for simulation



Gate level Simulation (1/3)

- Add 『`timescale 1ns/10ps』 into syn_file.v

```
`timescale 1ns / 10ps

module count ( count, clk, reset );
  output [5:0] count;
  input clk, reset;
  wire   N9, N10, N11, N12, N13, N14, n2, n3, n4, n5, n6, n7, n8, n9, n10, n11
;
```

Gate level Simulation (2/3)

- **Modify testbench.v:**

  initial $sdf_annotate(“syn_file.sdf”, instance module name);

```
`timescale 1ns / 10ps

`define period 4

module count_tb;
  wire [5:0]count;
  reg clk,reset;

  count     a1(
                .count(count),
                .clk(clk),
                .reset(reset)
              );
  always #(`period/2) clk=~clk;
  initial begin
    clk=0;
    reset=0;
    #(`period/4) reset=1;
    #(`period)   reset=0;
    #(`period*30) $finish;
  end

  initial $sdf_annotate("syn_count.sdf", a1);


  initial begin
    $dumpfile("test.vcd");
    $dumpvars();
  end

endmodule
```

Gate level Simulation (3/3)

- **ncverilog testbench.v syn_file.v TechFile.v (ex:tsmc18.v) +access+r**

- Please refer to “ncverilog” powerpoint to open waveform !