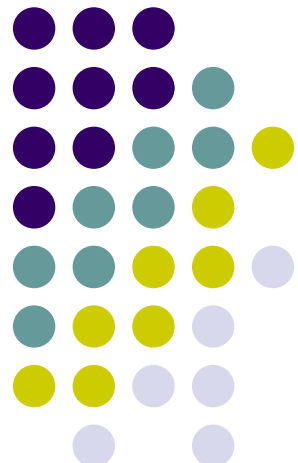
VLSI System Design
(Graduate Level)

Tutorial Overview

Fall 2008

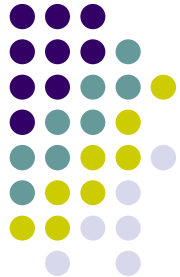


Outline

- Overview
  - General steps using Verilog
  - Tutorial highlights

- Hand-on practices
  - 10:10-noon Hand-on practices @CIC or SoC Lab
    - If your student ID is even, please go to CIC.
    - If odd, go to SoC Lab, please.

Steps Using Verilog (1/2)

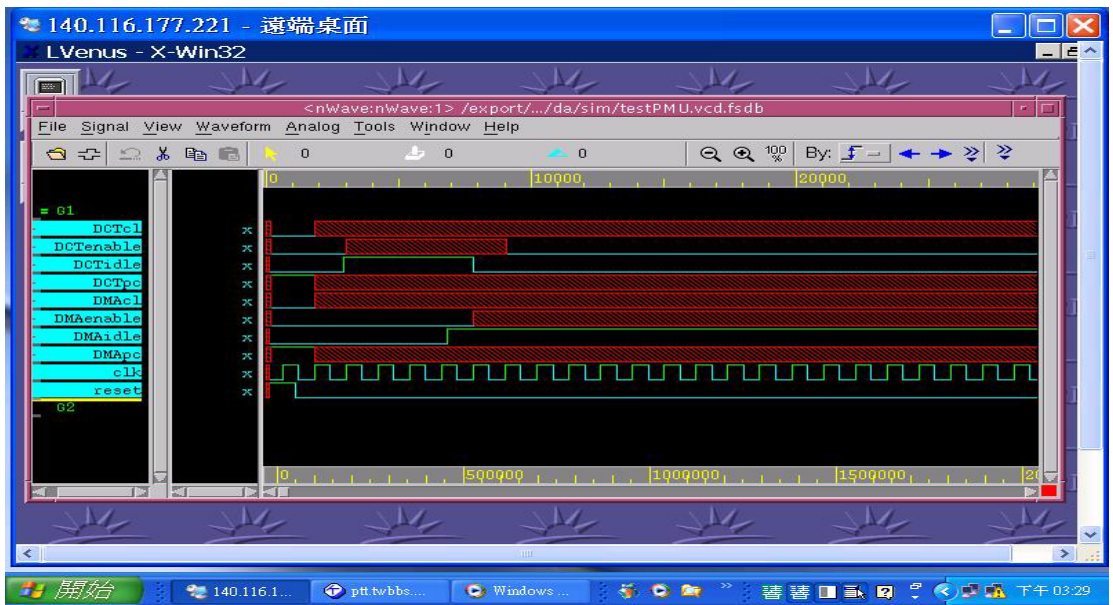


- Write a text-based description of a circuit
  - Use a common text editor,
    - such as vi, vim, ultraedit
- Compile the description to verify its syntax
  - Invoke Verilog compiler from the tool set

```
UNIX> verilog  BitWise.v  test_BitWise.v
```

Steps Using Verilog (2/2)

- Simulate the model and verify functionality
  - Write a ***testbench*** containing stimulus waveforms
  - Simulator displays waveforms
  - Analyze and detect functional errors



Tutorial Contents

- Lab Environment (SoC Lab and CIC)
- Basic Unix commands
- VerilogXL
- Debussy series: nWave, and nSchema
- Design Vision

Tutorial materials: already in course website on iteach

-- /Tutorial/tutorial_SoCLab.rar

-- Please bring those handouts to the class