**Its instruction set shall have at least 30 instructions, including branch and I/O instructions.**

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**There shall be at least 6 addressing modes.**

**Include interrupt mechanism and interrupt service routine for handling requests from other devices, such as sending data and control signals to DMA controller, or receiving data and control signals from DMA controller.**

**Must verify by sorting 100 numbers stored in external memory or any equivalent test bench**

**Must verify by perform Fibonacci series from F0 to F100 stored in external memory**

**Must verify interrupt and interrupt service routine by receiving data from external devices**

**Must verify by running a sequence of instructions (at least 1000 ) that completed a meaningful function based on the target application.**

**Include at least 20 more instructions other than those in basic requirements**

**Implement and verify Cache (either 1 level or 2 levels), Forwarding, or DMA, AHB bus access capability etc. (Note that AHB could be just behavioral model, i.e., not need to synthesize)**

**Complete code analysis by nLint and reach 100%**