

ASM2464PD/PDX PCB Guideline(Mid loss)

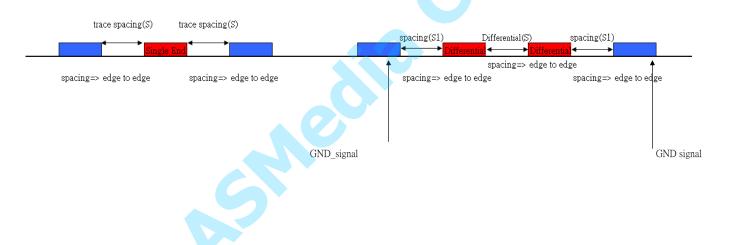
ECN

Date	Revision	Item	Description	Explanation
2023/7/3	1.0		Release	



PCB Stack-up

			Single end	1+/-15%		Differential	+/-10%
Thickness	1.2mm+/-10%		Trace Width	/ impedance		Trace Width_spaci	ng / impedance
Layer	lyr type	Thickness		50ohm	90 ohm	95 ohm	85 ohm
S/M	S/M	0.7					
L1-COMP	0.5oz+plating	1.4		4 / 50.18	4_5 / 89.71	4_7 / 91.59	4_4 / 83.48
	PP 1067(Dk/Df:3.41/0.0059)	2.42					
L2-GND	copper	1.4					
	CORE (TU768:Dk/Df:3.9/0.026)	3					
L3-Signal/Powe	er copper	1.4					
	CORE(TU-768)	27.76					
L4-Signal/Powe	er copper	1.4					
	CORE (TU768:Dk/Df:3.9/0.026)	3					
L5-GND	copper	1.4					
	PP 1067(Dk/Df:3.41/0.0059)	2.42					
L6-SOLD	0.5oz+plating	1.4		4 / 50.18	4_5 / 89.71	4_7 / 91.59	4_4 / 83.48
S/M	S/M	0.7		\			
	Thickness(mil)	48.4	·				
	mm	1.22936			*		









USB4 20Gbps

UTXP/N/0/1, URXP/N/0/1 Differential Pair Guidelines

TXP/N/0/1,URXP/N/0/1 Differential Pair Guidelines				
Parameter	Guidelines	Notes		
Topology	Point to Point			
Signal Reference	Ground			
Laver	Microstrip			
Characteristic Trace Impedance	Difference Pair Impedance = 85 ohm +/- 10 ohm	Shielding is needed for USB 4 differential pairs for signal integrity and EMC performance as below. A radial bend is preferred for 20Gbps.		
Differential(S1:W:S:W:S1)	30:4:4:4:30(S1 > 8 h)	Each distance 40mil with ground via hole for guard trace as below.		
Serpentine Spacing		No Serpentines		
VIA hole Max.	<=2			
Total Length	<1.5" for type C SMT connector, ASAP (prefer 0.5"-1.2") or Maximum insertion loss < 4dB@10GHz.	maintain loss, crosstalk and fiber weave effect. Shielding is needed for USB 4 differential pairs for signal integrity and EMC performance. TXO/TX length match < 1000 mil; RXO/RX1 length match < 1000 mil or lane to lane skew.		
Series Capacity	C_TX=0.22uF (Size 0201 / X7R); C_RX=0.33uF (Size 0201 / X7R)/R_DN=220K ohm(Size 0201)	The Cap close to Connector for UTXP/N; RX AC coupling Cap and resistor pull down for short protection.(Component size should be 0201 on USB4.)		
Differential Pair P/N Length Matching	< 5 mil	Every segment intra pair skew: < 1 mil		

USB2.0 UDP/N Differential Pair Guidelines

Parameter	Guidelines	Notes
Topology	Point to Point	
Signal Reference	Ground	
Characteristic Trace	Difference Pair Impedance = 85 ohm +/- 10%	
Impedance	Difference Fair Impedance = 65 Orini 47- 1076	
Differential (S1:W:S:W:S1)	15:4:4:4:15	
Serpentine Spacing	15 mil	
VIA hole Max.	<=4	
Total Length	< 4"	
Differential Pair Length	< 20 mil	

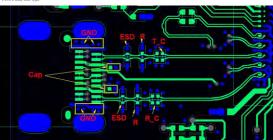
Other

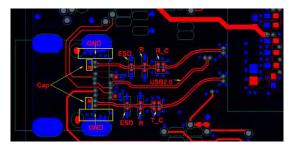
Parameter	Guidelines	Guidelines	Guidelines
Signal Name	UREXT	VBUS	VCC33U.VDD.VCCH
Topology	Point to Point	Point to Point	Point to Point
Single End (W:S)	10:7	5:8	15:8
Total Length	ASAP	10"	ASAP



Refer to USB4 system design guidelines

https://www.usb.org/sites/default/files/D2T2-2%20-%20USB4%20Cable%20anl%20S TYPE C (only SMT type)





Layout Design Considerations/Examples - 5/7





Ensure that layer under the void (surface-2) is not a source of noise, e.g. power plane. It's best to have ground on surface-2 under the void

AC-Caps and Discharge Resistors



Smaller size components (e.g. 0201) will have smaller parasitic and therefore better return loss than larger ones (0402). Consider using 0201 components



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PCIe Gen4 16Gbps

PTXPx/Nx,PRXPx/Nx, Differential Pair Rounting Guidelines

Parameter	Guidelines	Notes
Topology	Point to Point	
Signal Reference	Ground	
Layer	Microstrip	
Characteristic Trace Impedance	TX&RX Impedance Difference Pair = 85 ohm +/- 10%	
Differential (S1:W:S:W:S1)	30:4:4:4:30(S1 > 8 h)	
Serpentine Spacing		
Series Capacity	Cs=0.22uF (Size 0402 / X7R or Size 0201(max. length) ;)	The AC-couple capacitor close to connector for PETXP/N
VIA hole Max.	<= 2 for connector ; <= 4 for down device or chip	
	< 5" for connector, ASAP.	
Total Length	1.5" < Down device(on board device or chip to chip) < 6"	
Differential Pair P/N Length Matching	< 5 mil	

XO/XI

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Parameter	Guidelines
Signal Name	XO /XI
Characteristic Trace	lean-down Difference Dairy OF about 450/
Impedance	Impedance Difference Pair = 85 ohm +/- 15%
Differential	
(S1:W:S:W:S1)	30:4:4:4:30
Total Length	< 0.5" .ASAP

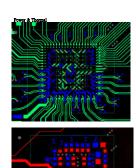
Other

Parameter	Guidelines
Signal Name	VDD/VCCLP/VCCLU/VCCH/VCCx
Topology	Point to Point
Single End (W:S)	15:8
Total Length	ASAP

PECLK

PE_CLKP/N

Parameter	Guidelines	Notes
Signal Reference	Ground	
Signal Name	PECLKP/N	
Layer	Microstrip	
Characteristic Trace	Impedance Difference Pair = 85 ohm +/- 15%	
Impedance	impedance Difference Pail = 65 Onin +/- 15%	
Differential		
(S1:W:S:W:S1)	30:4:4:4:30(S1 > 8 h)	
Total Length	< 7" for connector ,< 8" for chip pad, ASAP.	
Differential Pair P/N	< 5 mil	
Length Matching	< 3 1111	









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SPIDI/SPICK/SPIDO/SPICS/I2C_DATA/I2C_CLK

Parameter	Guidelines	Notes	
Topology	Point to Point		
Signal Reference	Ground		
Characteristic Trace Impedance (Single-Ended)	50 ohm +/- 15%		
Trace Width	5 mils		
Trace Spacing	10 mils		
Total Length	< 10"		

CC1/CC2

Parameter	Guidelines	Notes
Topology	Point to Point	
Signal Reference	Ground	
Trace Width	8 mils	
Trace Spacing	15 mils	
Total Length	< 10"	



GPIO/Strapping/UART_TX/UART_RX

Parameter	Guidelines	Notes
Topology	Point to Point	
Signal Reference	Ground	
Characteristic Trace Impedance (Single-Ended)	50 ohm +/- 15%	
Trace Width	5 mils	
Trace Spacing	8 mils	
Total Length	< 10"	