BoW Statistical Channel Model Simulations

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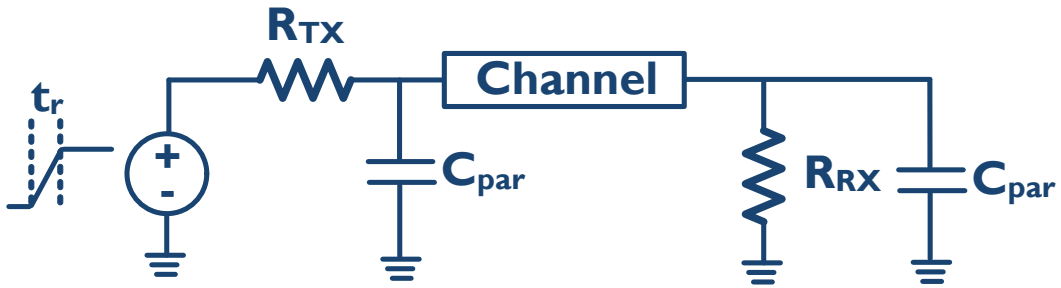
Dec. 3rd, 2021

Global Setup: Channel / TX / RX Models



- **TX/RX simplified models currently use the same parasitic capacitance on both sides**
  - But these can be decoupled; in general we've seen similar SI impact from cap on either side
  - Unterminated signaling modeled by setting R_{RX} to a large value (e.g., ~10KΩ)

- **Note that as of 12-1-201, risetime is <u>before</u> the RC filter, which is pessimistic**
  - Results so far show that risetime does not have a significant impact on margin, but will address this in the future

Global Setup: Analysis

- **All TX ports are excited with data, and responses/statistics on all data RX ports are computed**
  - In channels that include RX ports for the CLK, those are excluded (since they would not carry data)

- **Timing margins are always reported from whatever the worst-case RX data port within a given channel model is**

- **Items not yet included in the analysis (as of 12-1-2021):**
  - Interaction between TX circuit skew and crosstalk statistics
  - Impact of crosstalk on CLK timing relative to data

Available Channel Models

- **Channel models provided by channel modeling team (“Alphawave”)**
  - Include only 5 wires
  - Layers 1 and 7, ~20mm reach
- **Channel models contributed by Namhoon Kim (“Full Slice”)**
  - Representative only – not associated with any real design/project
  - Full 16 data wires + clocks for each slice; slices on layers 2 and 4 are included in a single model
    - Worst-case RX within both slices is found / reported
  - 2mm, 10mm, 25mm reach
- **Channel models developed by ARM**
  - Similar to Alphawave, but with full 16 data wires + clocks
  - Layers 1 and 7, ~20mm reach
- **Channel model from Keysight**
  - Includes only 5 wires
  - 6mm

Summary of Results

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Channel / Rate / Term	Scenario	Alphawave Layer 1	Alphawave Layer 7	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	Default	44.8%	47.2%	68%	61.6%	60.8%	25.6%	47.2%	68%
	C = 200fF	55.4%	58.4%	72.8%	71.2%	69.6%	41.6%	56%	73.6%
	tr = 23%					63.4%			
	C = 200fF, tr = 23%	60%	60.8%			72.8%			
16 Gb/s, Source Terminated	C = 200fF			56%					
	C = 200fF, V_{sen} = 75mV			62.4%					
8 Gb/s, Doubly Terminated	Default				73.6%				
8 Gb/s, Source Terminated	Default			57.6%	40.8%				
	C = 500fF			68.8%					
	C = 400fF			77.6%	59.2%				
	C = 400fF, V_{sen} = 75mV				67.2%				
4 Gb/s, Source Terminated	Default			27.2%	41.6%				0%
	V_{sen} = 150mV			63.2%	59.2%				68.8%
	C = 800fF			58.6%					56.8%
	C = 800fF, V_{sen} = 150mV			76%					76%
	C = 800fF								60.8%
	C = 800fF, V_{sen} = 150mV								80%

Setup: 16Gb/s Doubly Terminated

- **By default, parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):**
  - 20% - 80% rise time of 0.32UI
  - $R_{TX} = R_{RX} = 50\Omega$
  - 300fF lumped capacitance on TX/RX
  - VDDIO = 750mV
  - 75mV peak-to-peak RX sensitivity

Alphawave Layer1

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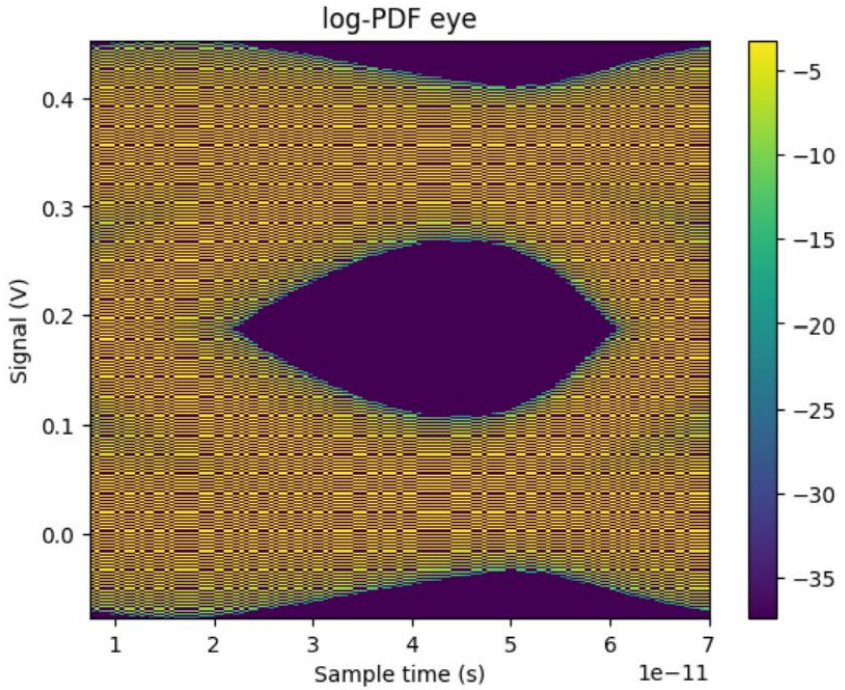
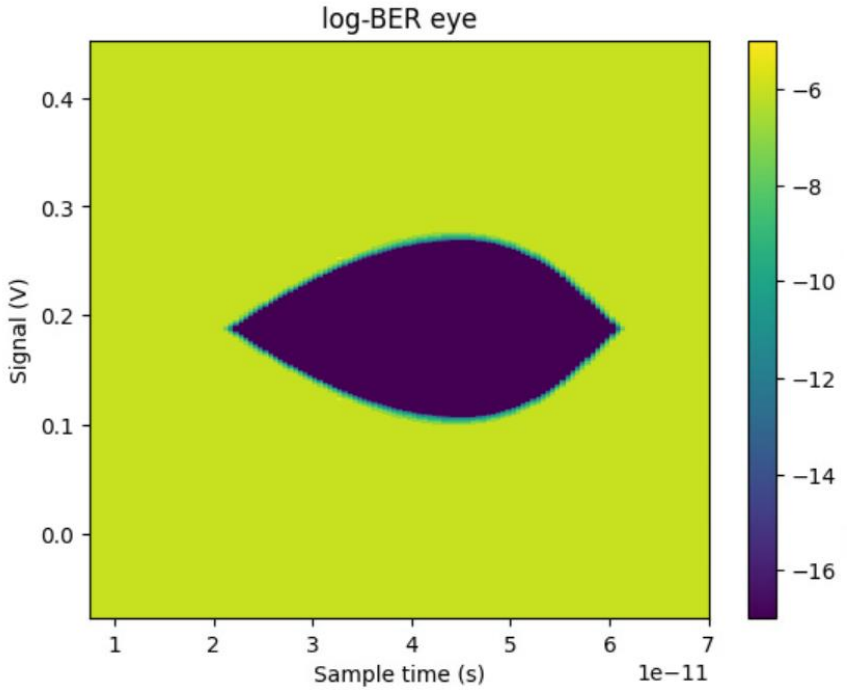
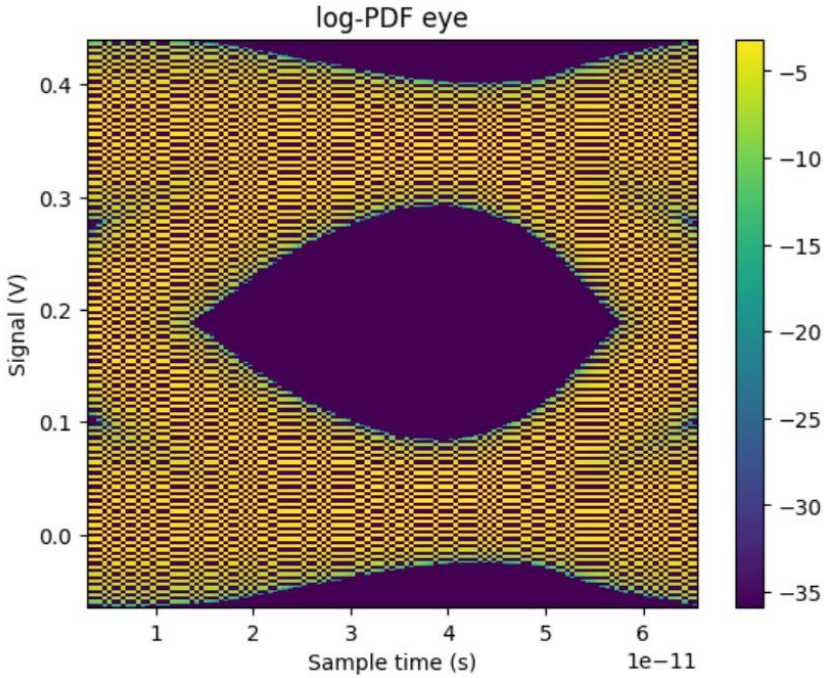
Alphawave Layer1 Results

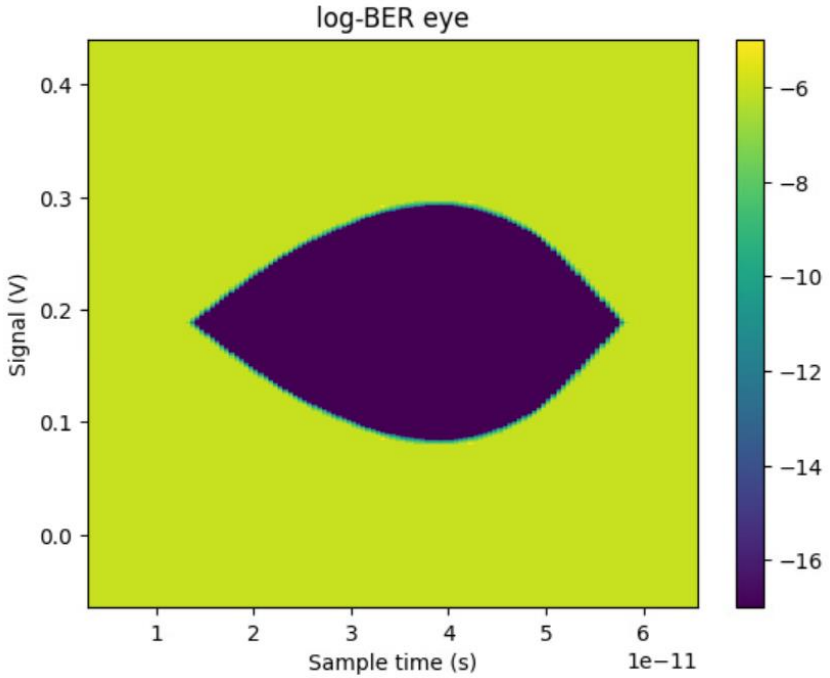




- **Worst line timing margin @ 1e-15 BER: 44.8%**

Alphawave Layer1 Results: Cpar = 200fF

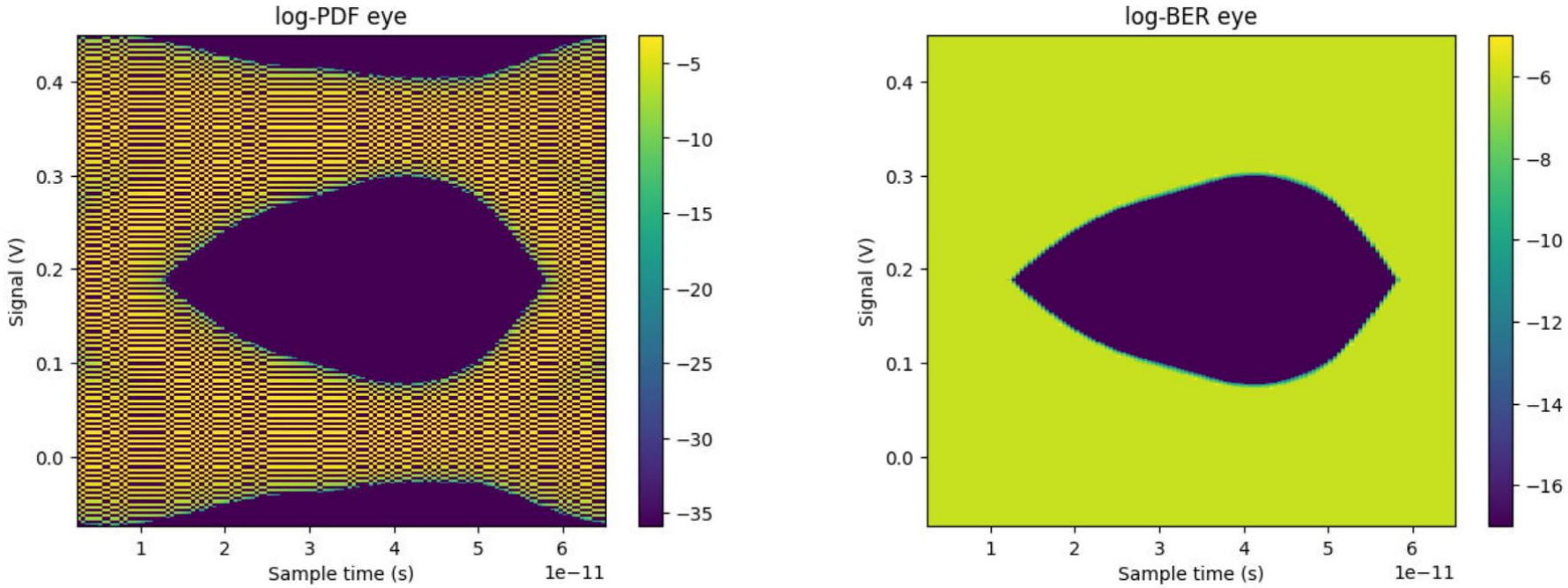




- **Worst line timing margin @ 1e-15 BER: 55.4%**

Alphawave Layer1 Results:

20%-80% risetime = 23% UI, Cpar = 200fF



- **Worst line timing margin @ 1e-15 BER: 60%**

Alphawave Layer7

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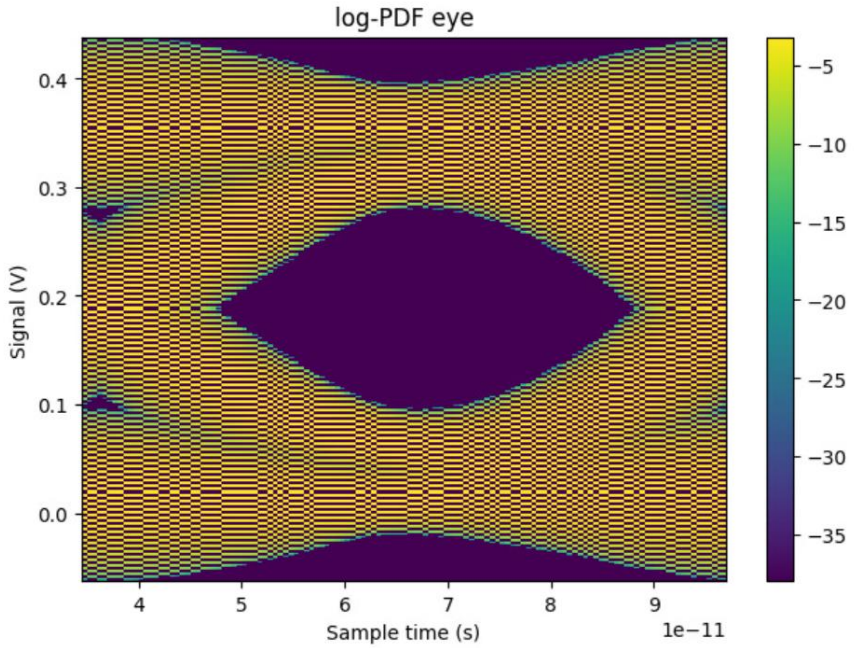
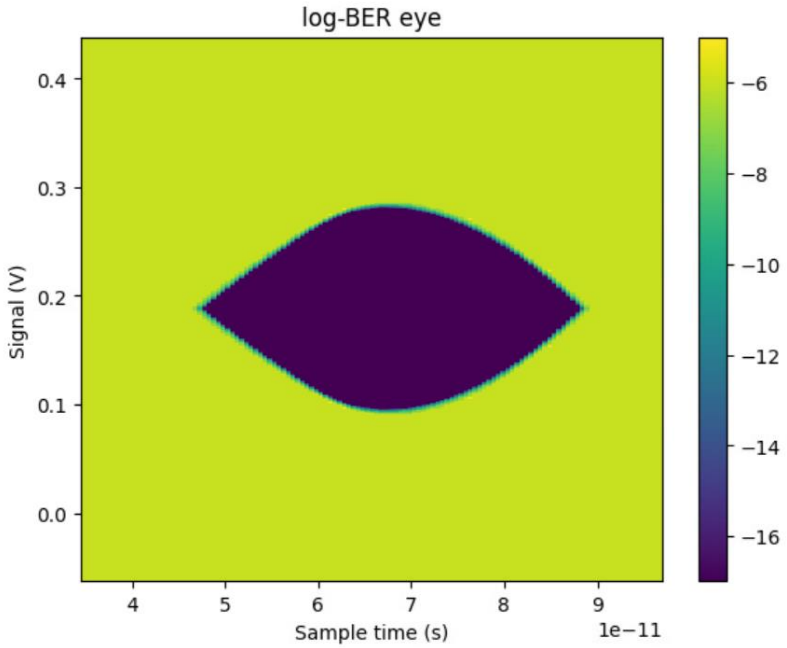
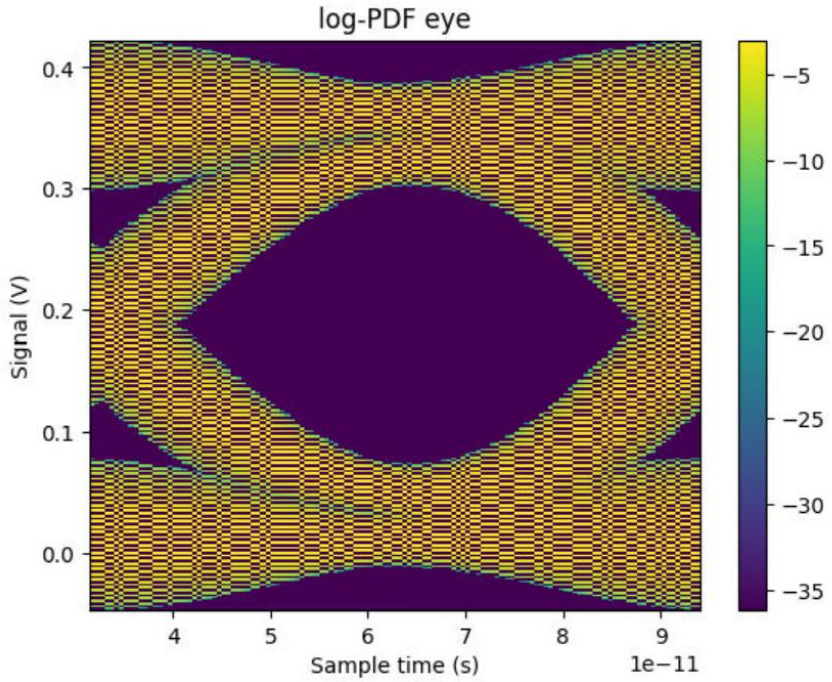
Alphawave Layer7 Results

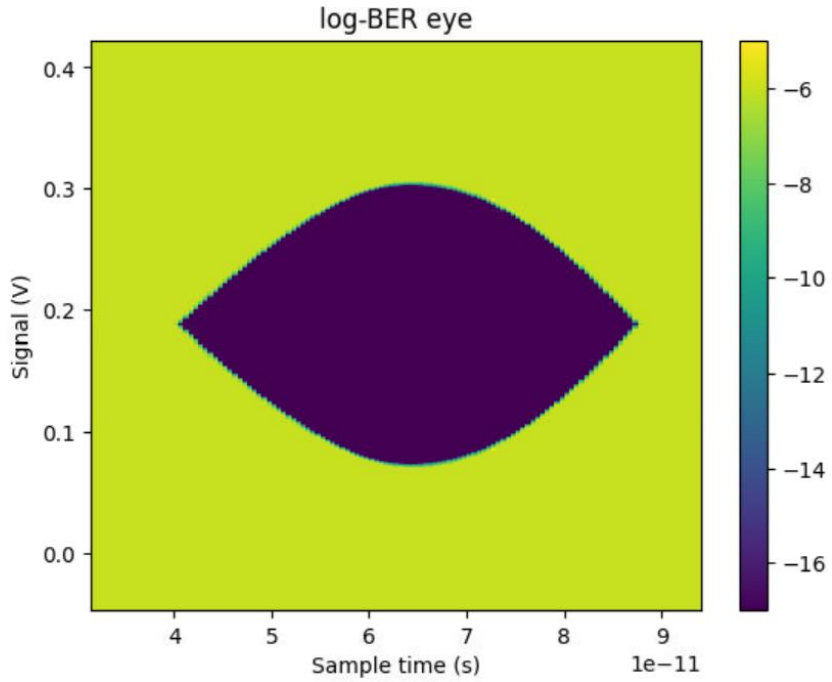




- **Worst line timing margin @ 1e-15 BER: 47.2%**

Alphawave Layer7 Results: Cpar = 200fF

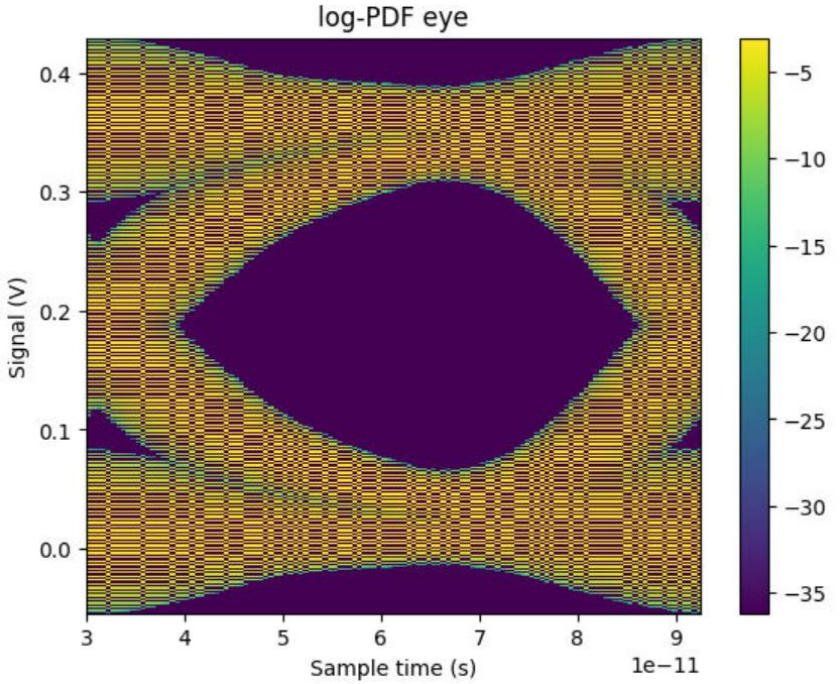


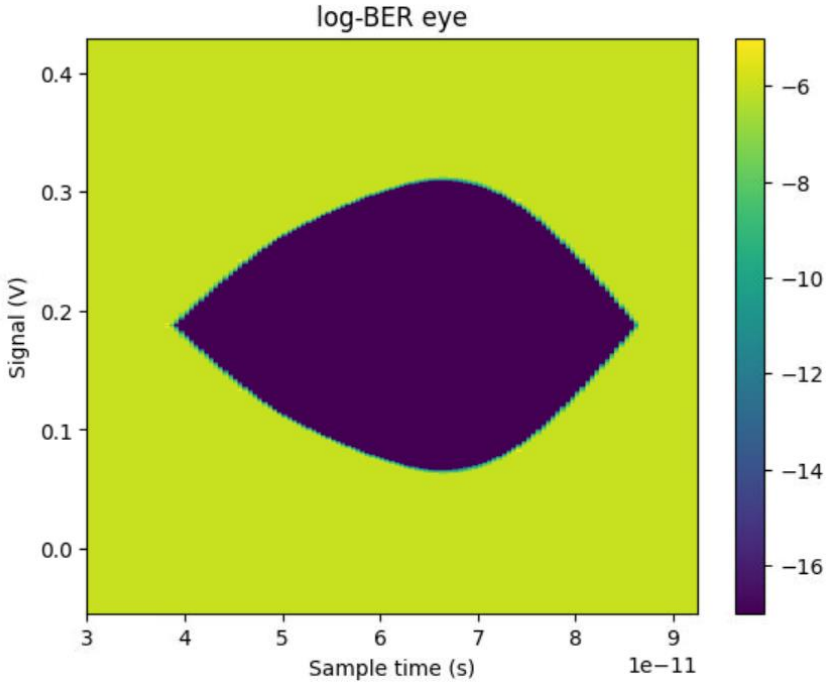


- **Worst line timing margin @ 1e-15 BER: 58.4%**

Alphawave Layer7 Results:

20%-80% risetime = 23% UI, Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 60.8%**

Full Slice 25mm

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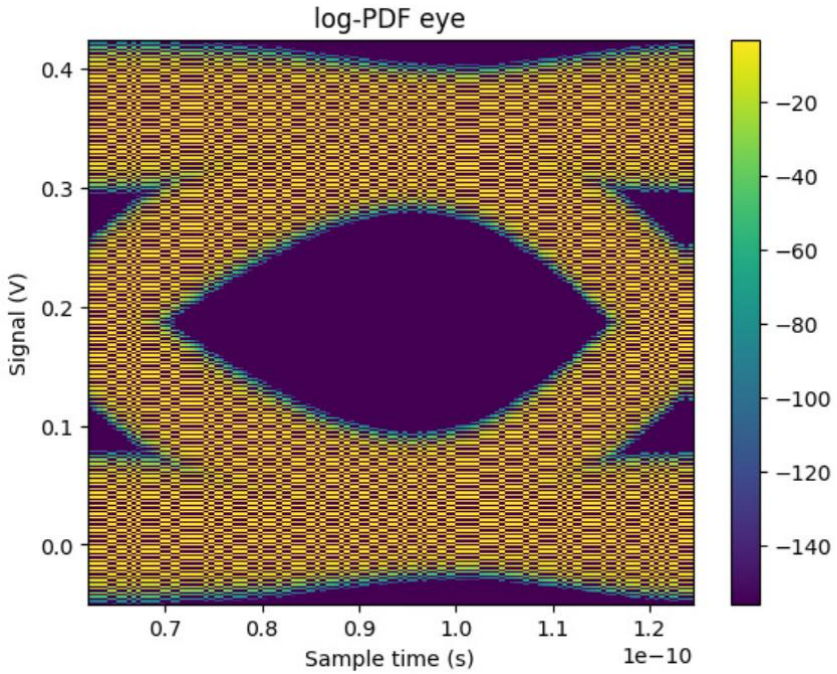
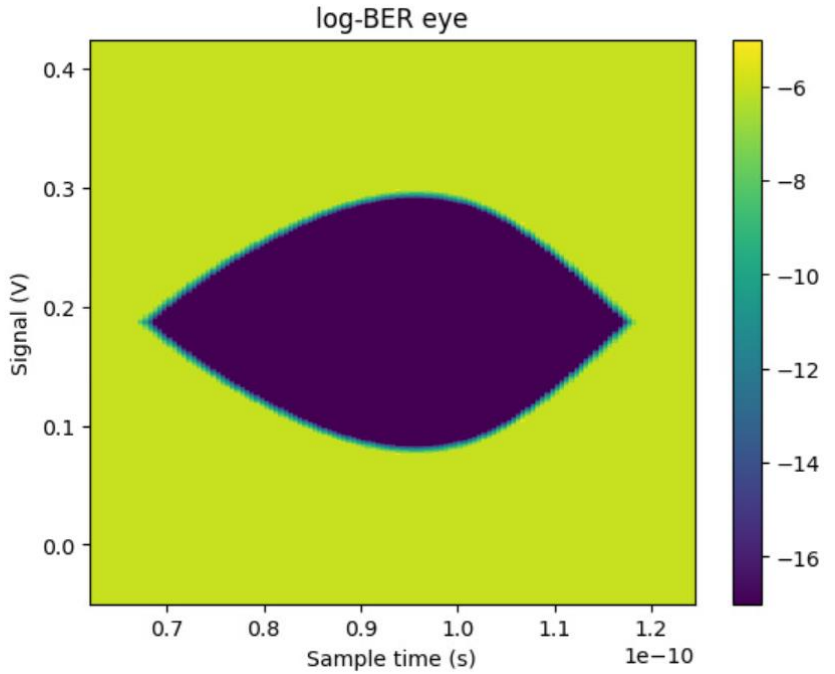
Full Slice 25mm Results

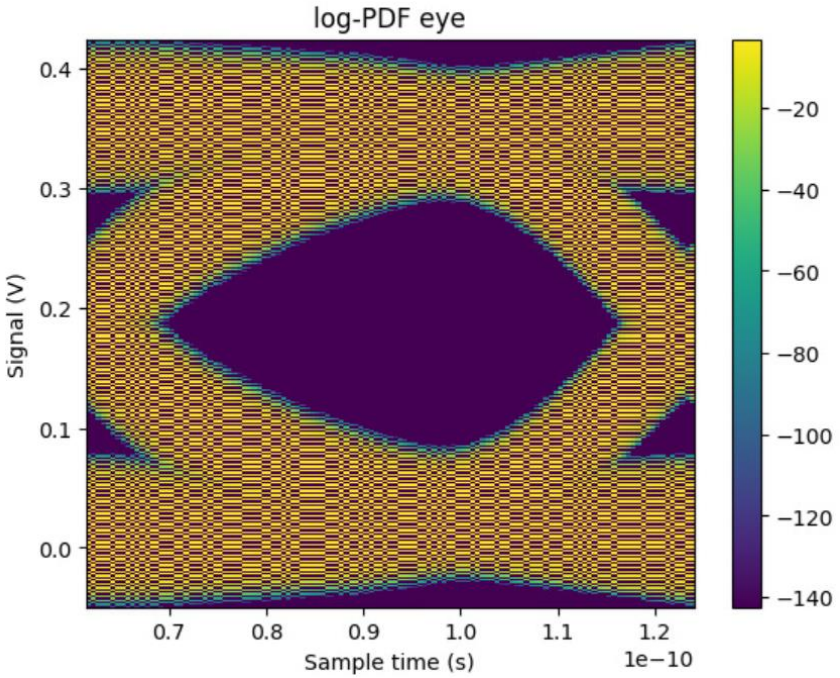


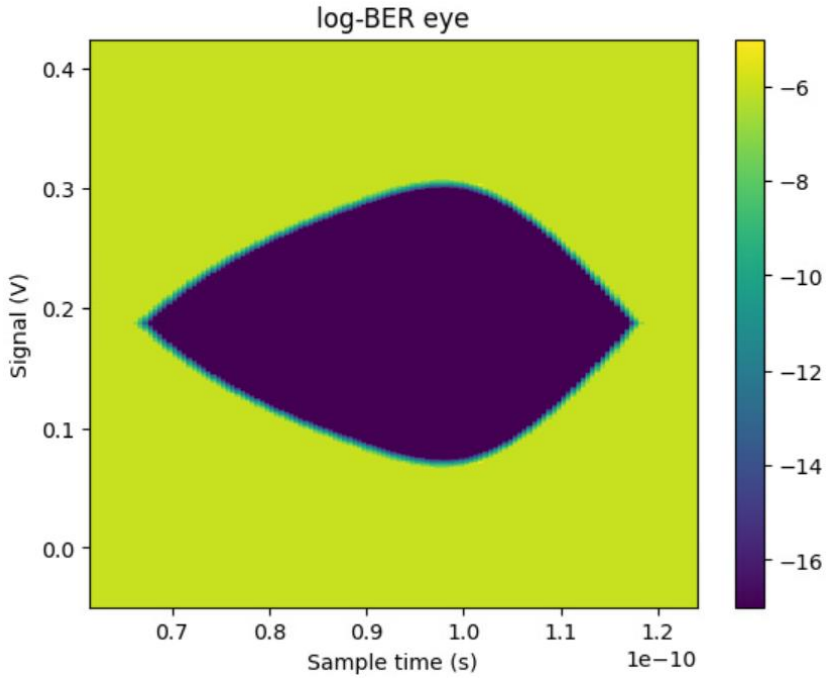


- **Worst line timing margin @ 1e-15 BER: 60.8%**

Full Slice 25mm Results:

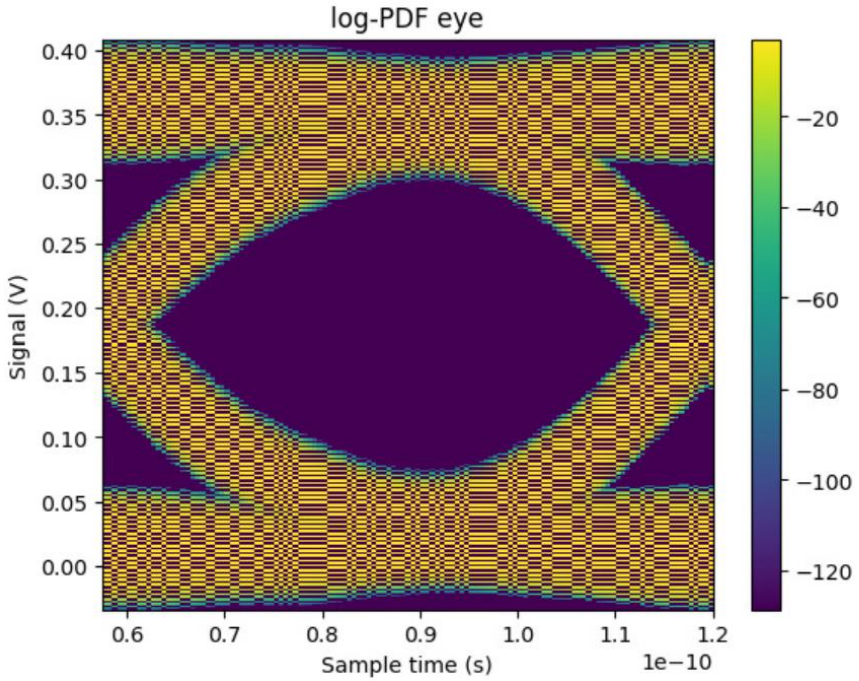
20%-80% risetime = 23% UI

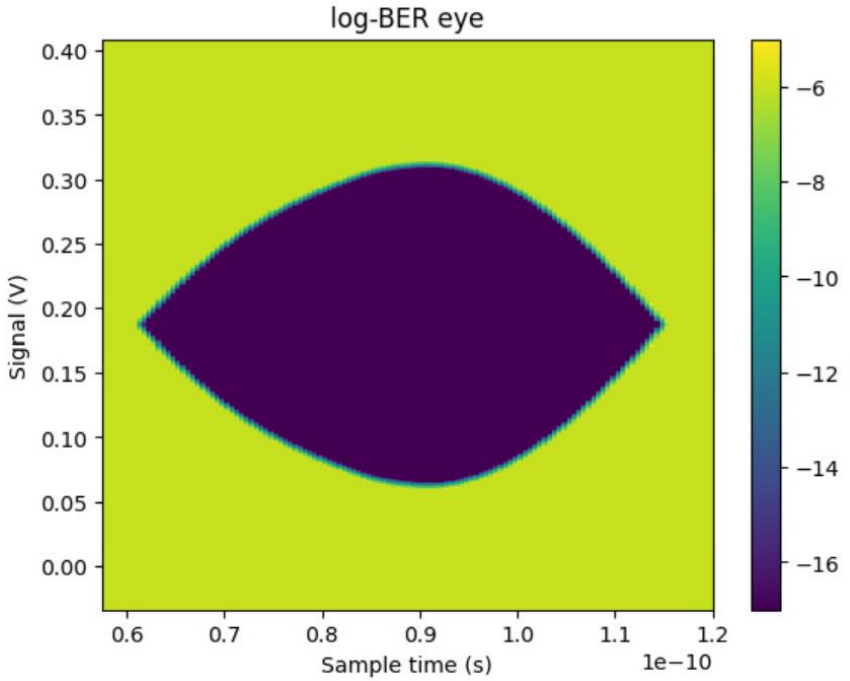




- **Worst line timing margin @ 1e-15 BER: 63.4%**

Full Slice 25mm Results: Cpar = 200fF

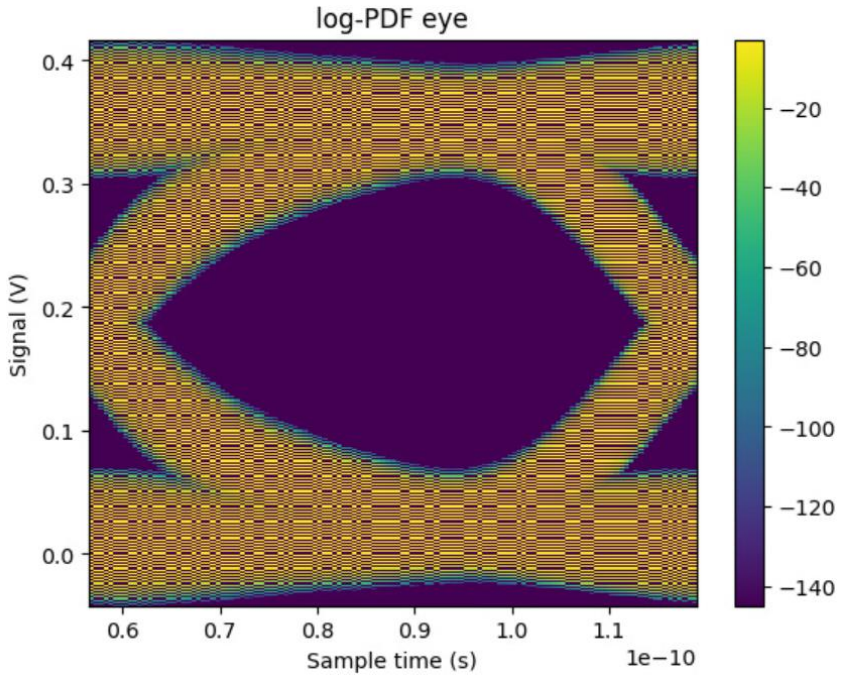


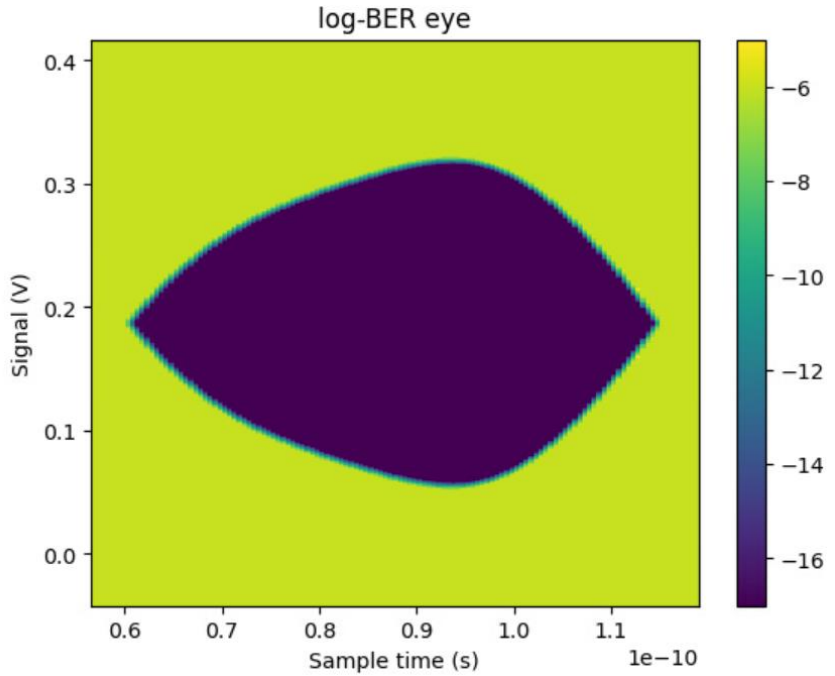


- **Worst line timing margin @ 1e-15 BER: 69.6%**

Full Slice 25mm Results:

20%-80% risetime = 23% UI, Cpar = 200fF

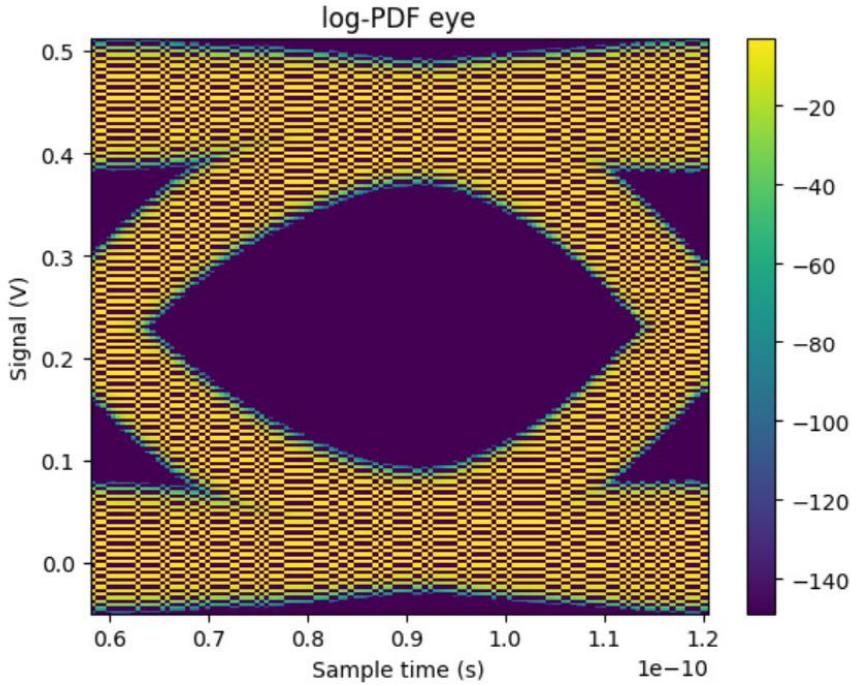


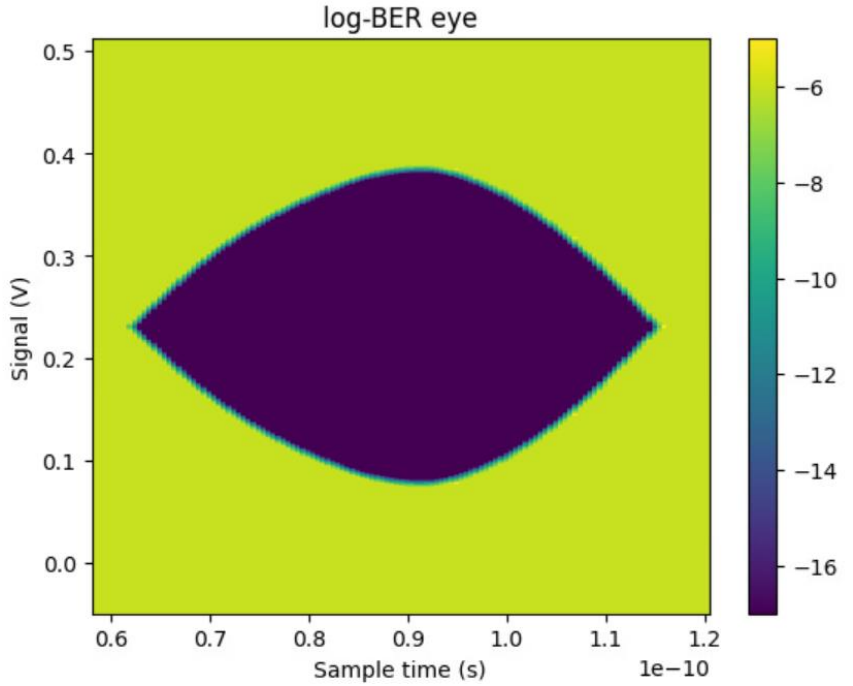


- **Worst line timing margin @ 1e-15 BER: 72.8%**

Full Slice 25mm Results:

Rtx = 43Ω, Rrx = 69Ω, Cpar = 200fF

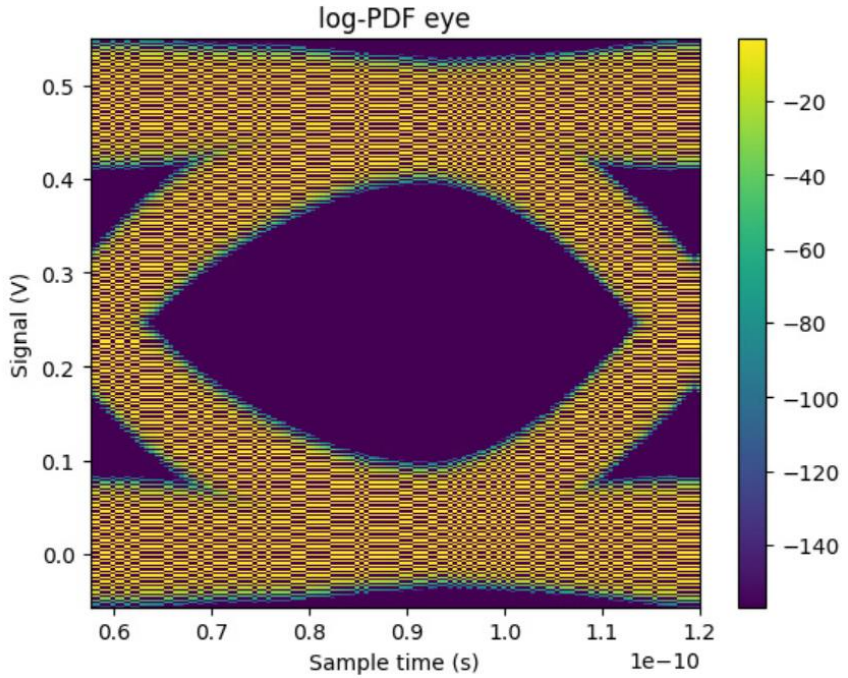


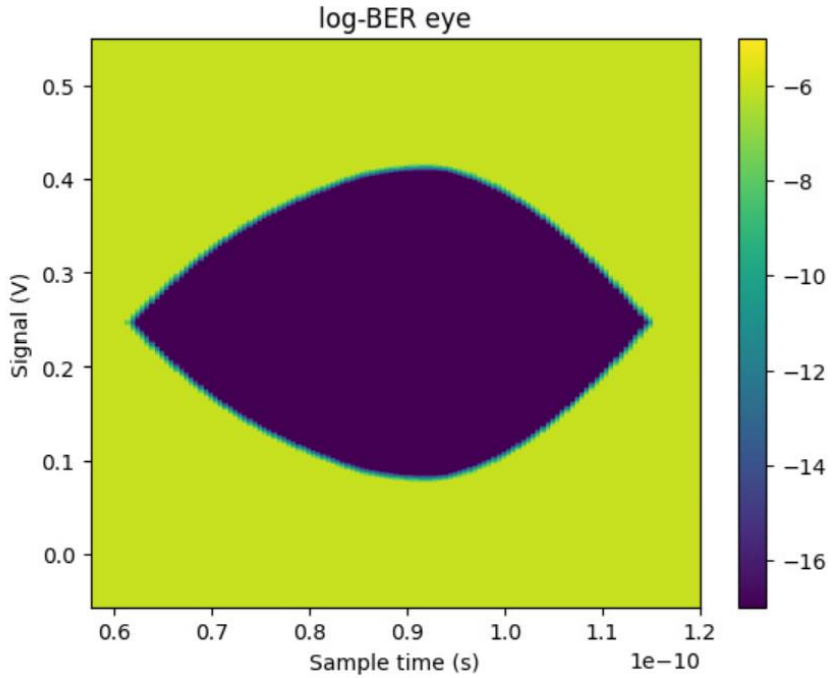


- **Worst line timing margin @ 1e-15 BER: 71.2%**

Full Slice 25mm Results:

Rtx = 36Ω, Rrx = 69Ω, Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 72.8%**

Full Slice 10mm

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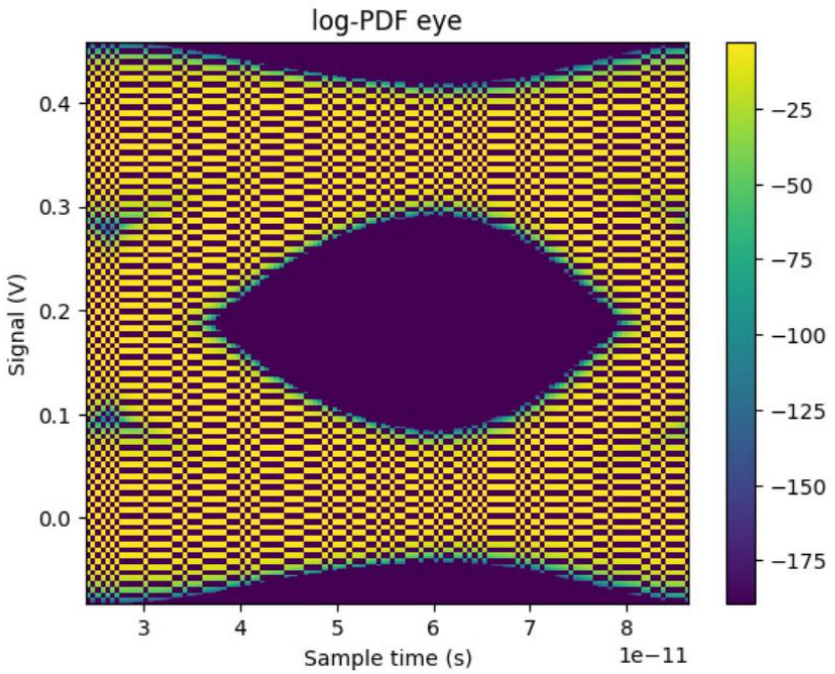
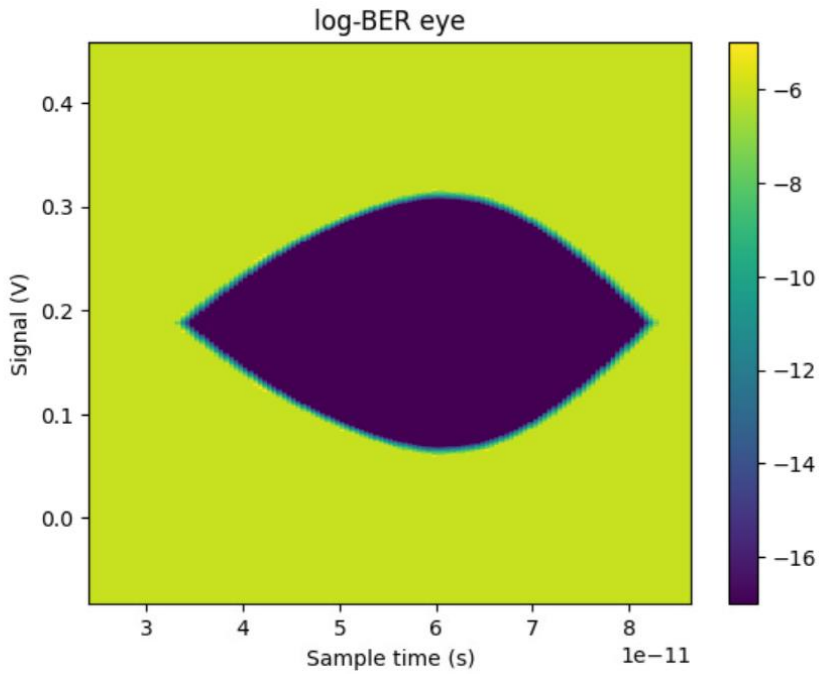
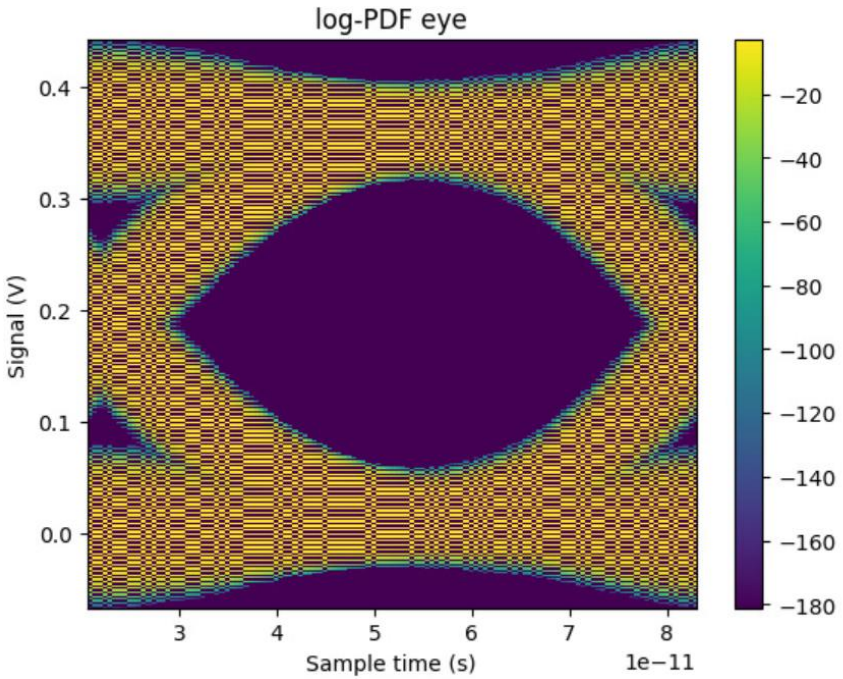
Full Slice 10mm Results

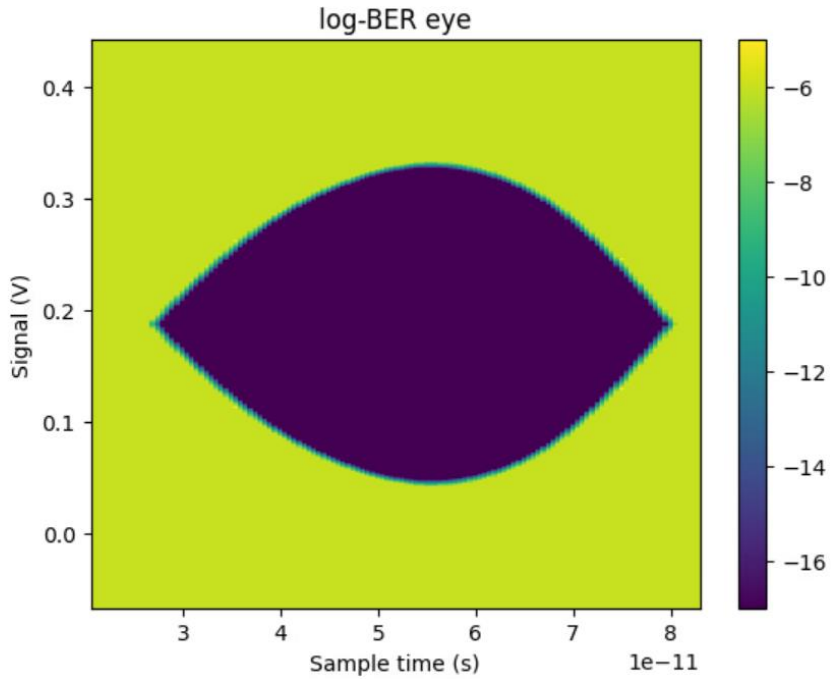




- **Worst line timing margin @ 1e-15 BER: 61.6%**

Full Slice 10mm Results: Cpar = 200fF

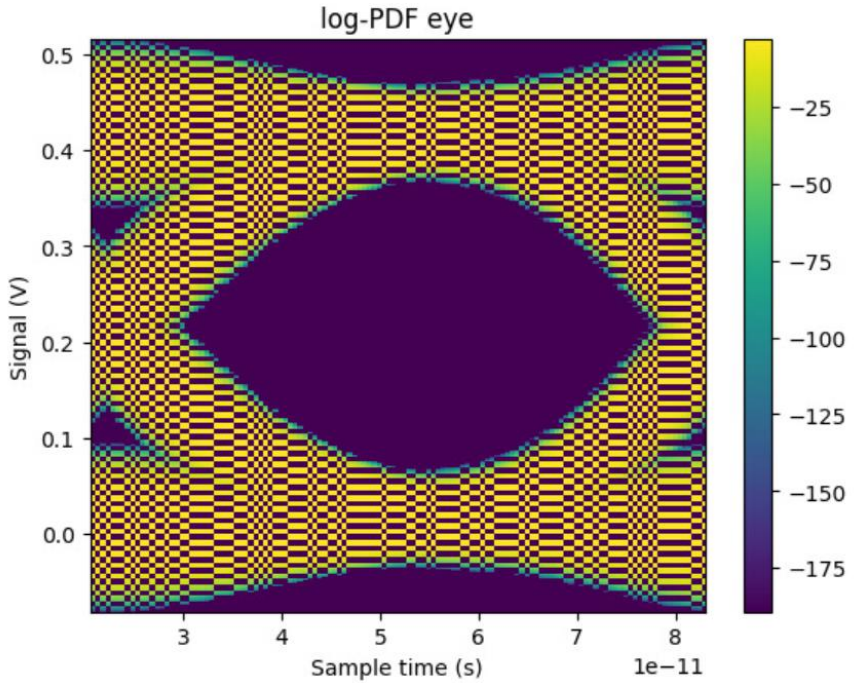


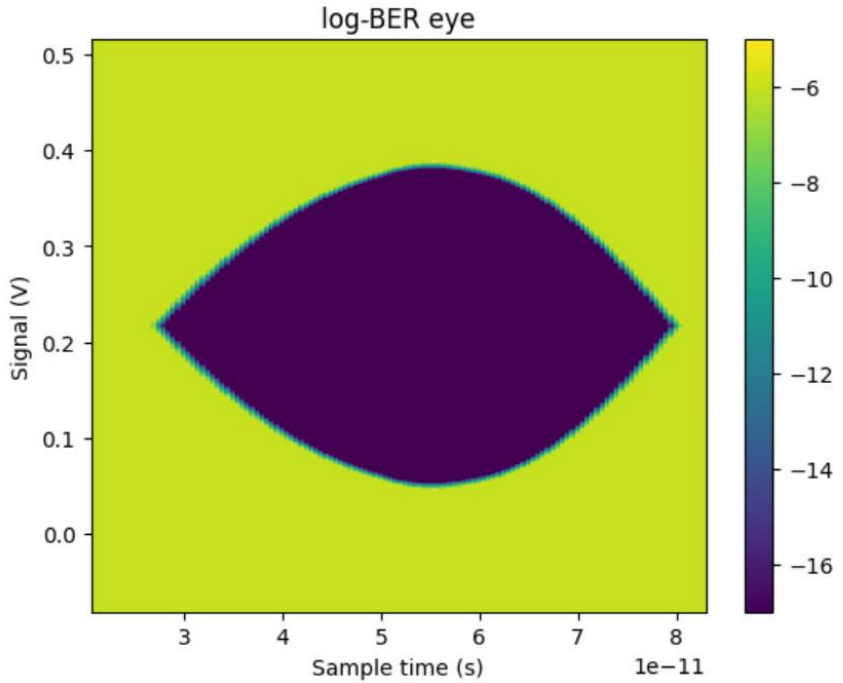


- **Worst line timing margin @ 1e-15 BER: 71.2%**

Full Slice 10mm Results:

Rtx = 43Ω, Rrx = 59Ω, Cpar = 200fF

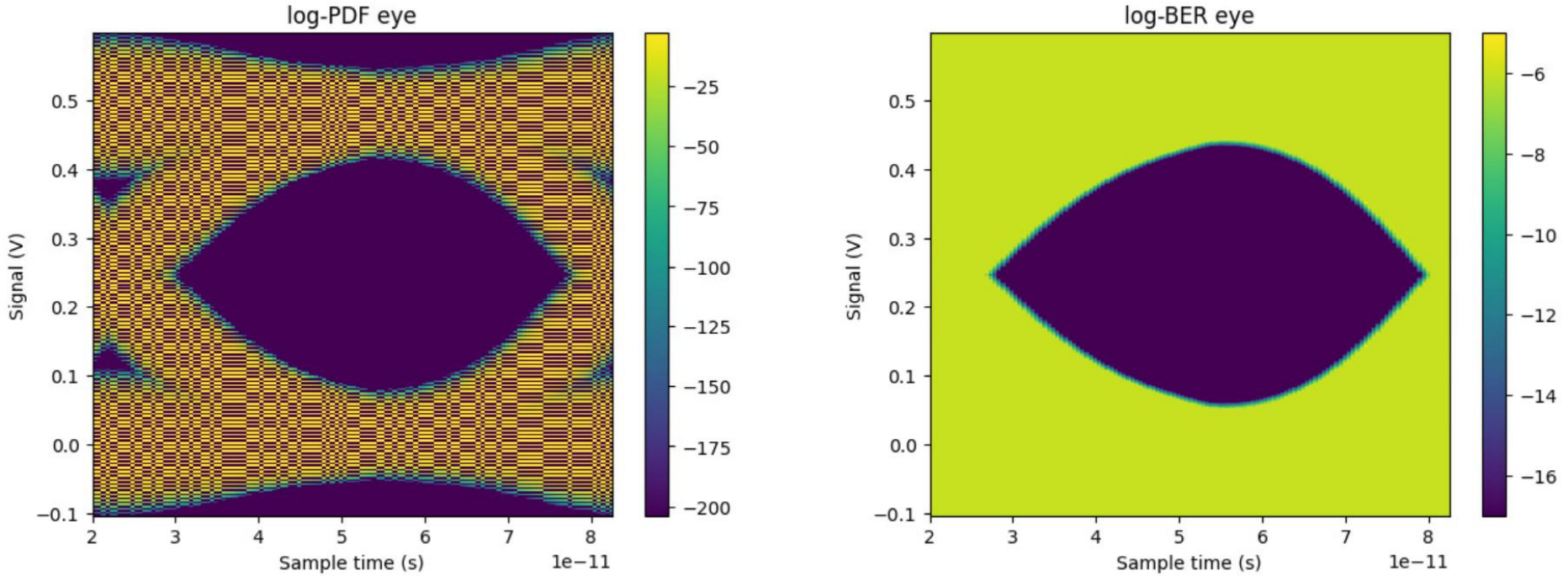




- **Worst line timing margin @ 1e-15 BER: 72%**

Full Slice 10mm Results:

Rtx = 36Ω, Rrx = 69Ω, Cpar = 200fF



- **Worst line timing margin @ 1e-15 BER: 72.8%**

Full Slice 2mm

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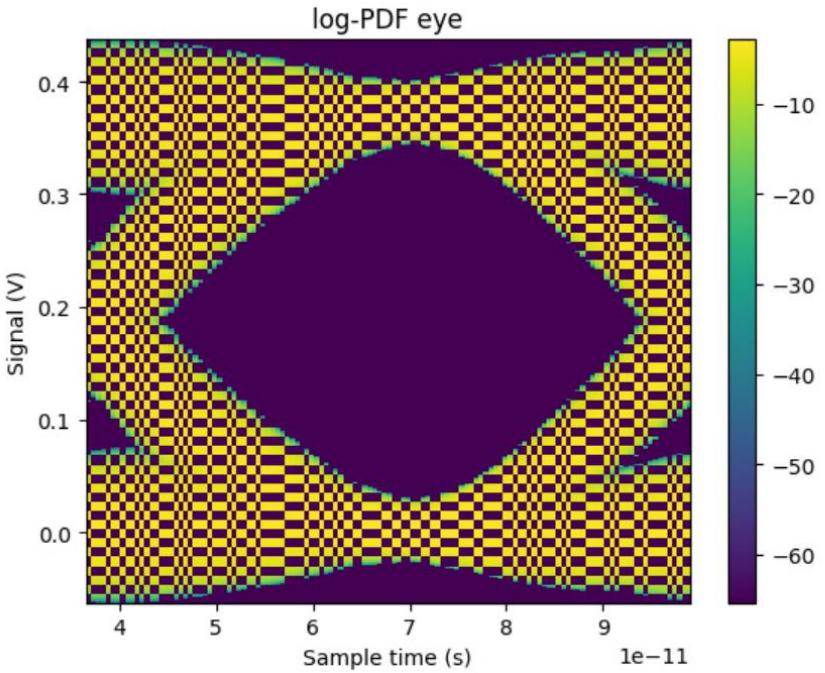
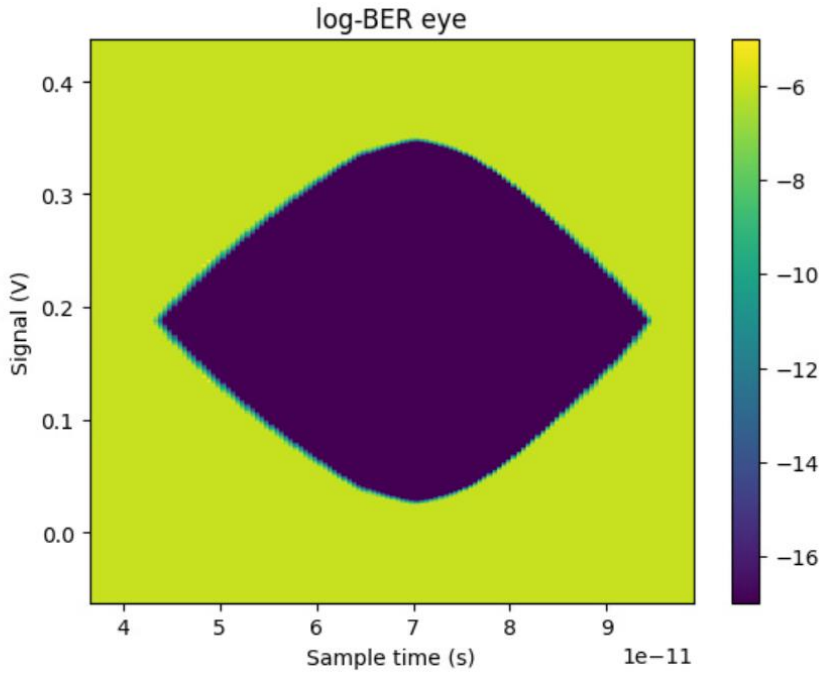
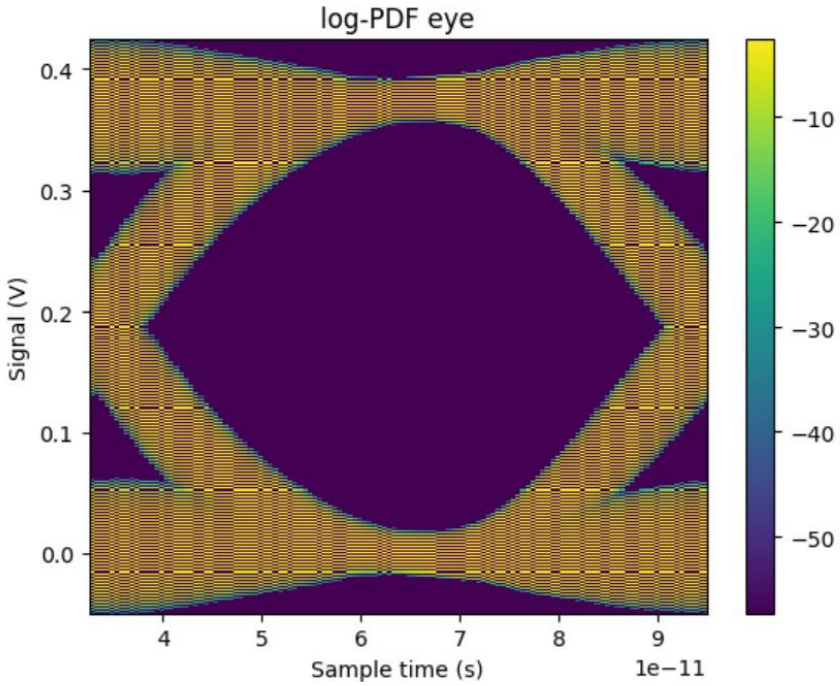
Full Slice 2mm Results

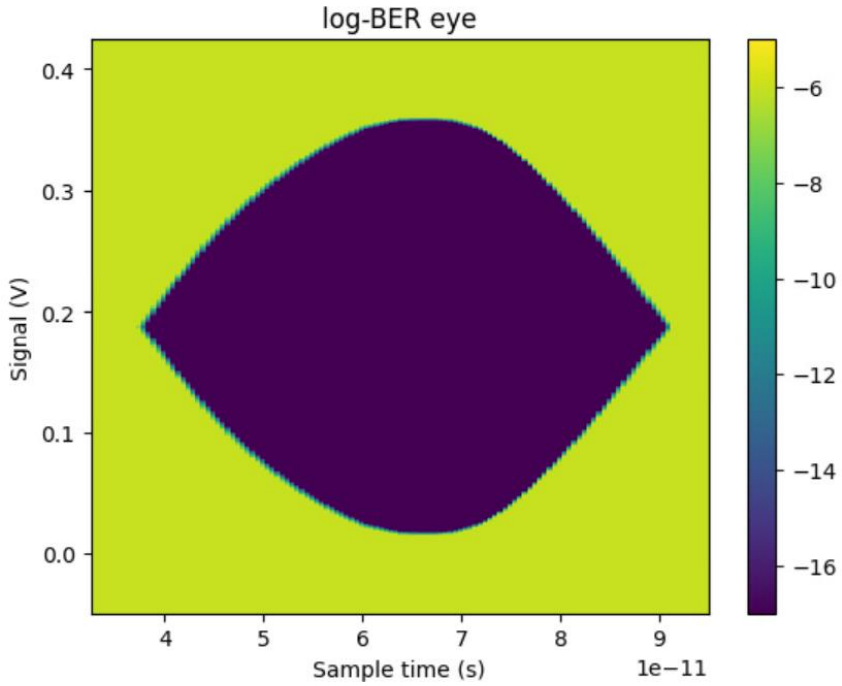




- **Worst line timing margin @ 1e-15 BER: 68%**

Full Slice 2mm Results: Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 72.8%**

ARM Layer A 20mm

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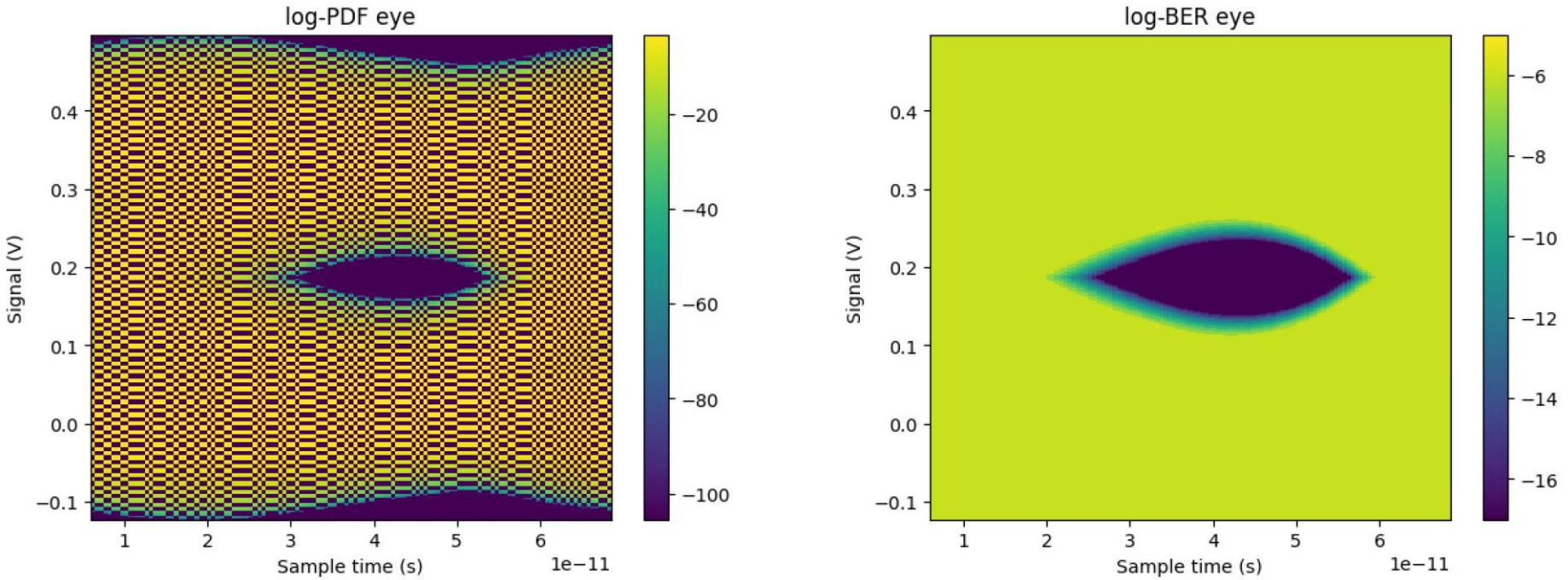
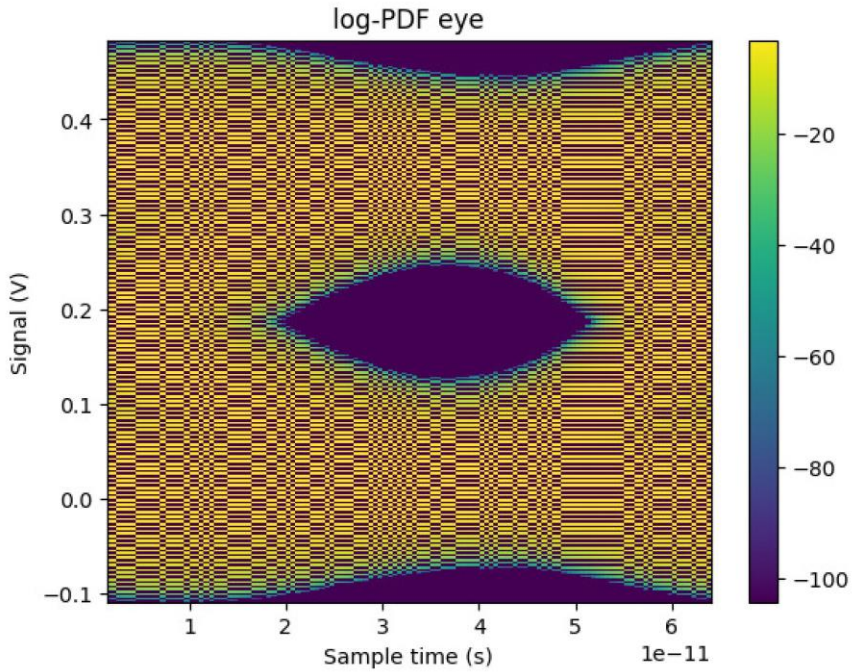
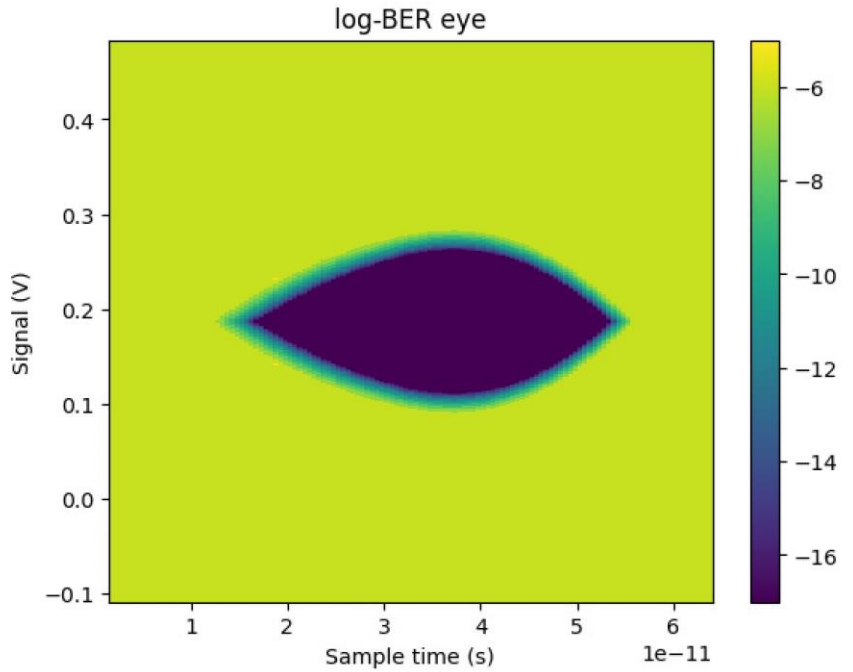
ARM Layer A Results



- **Worst line timing margin @ 1e-15 BER: 25.6%**

ARM Layer A Results: Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 41.6%**

ARM Layer D 20mm

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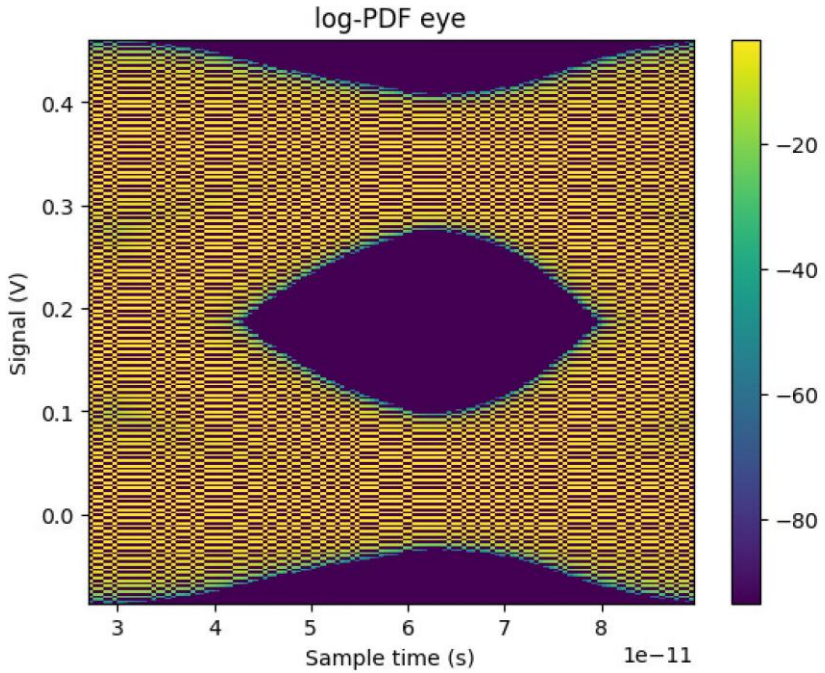
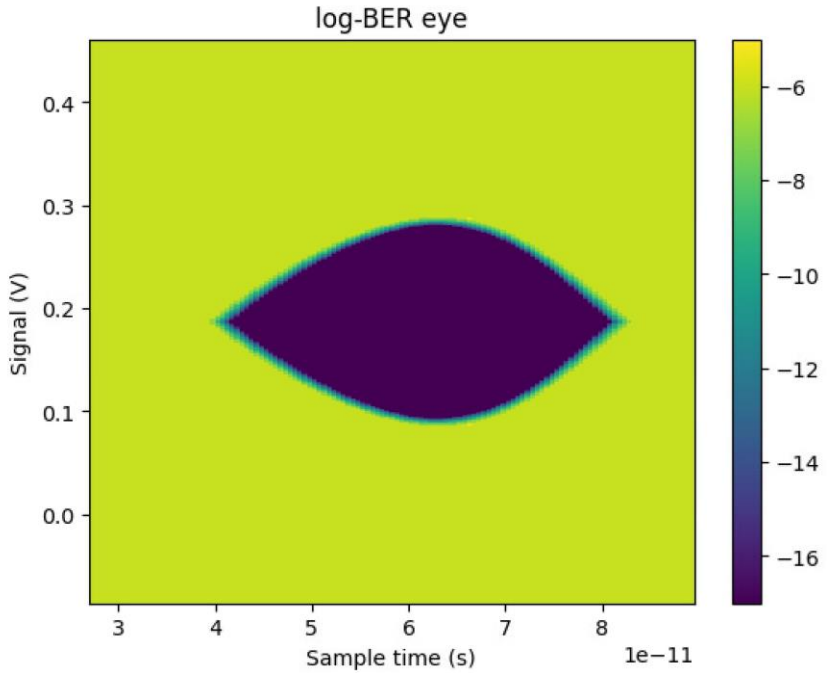
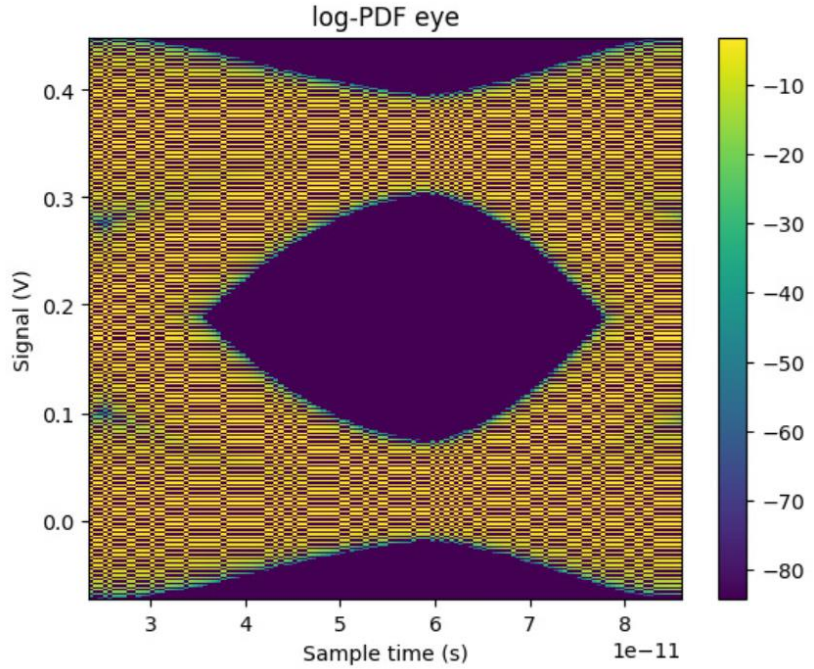
ARM Layer D Results

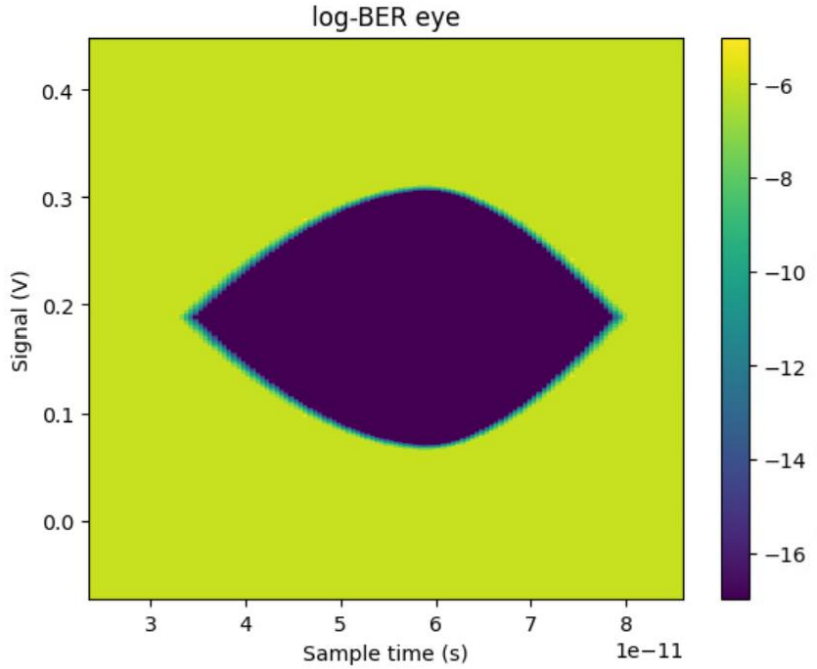




- **Worst line timing margin @ 1e-15 BER: 47.2%**

ARM Layer D Results: Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 56%**

Keysight

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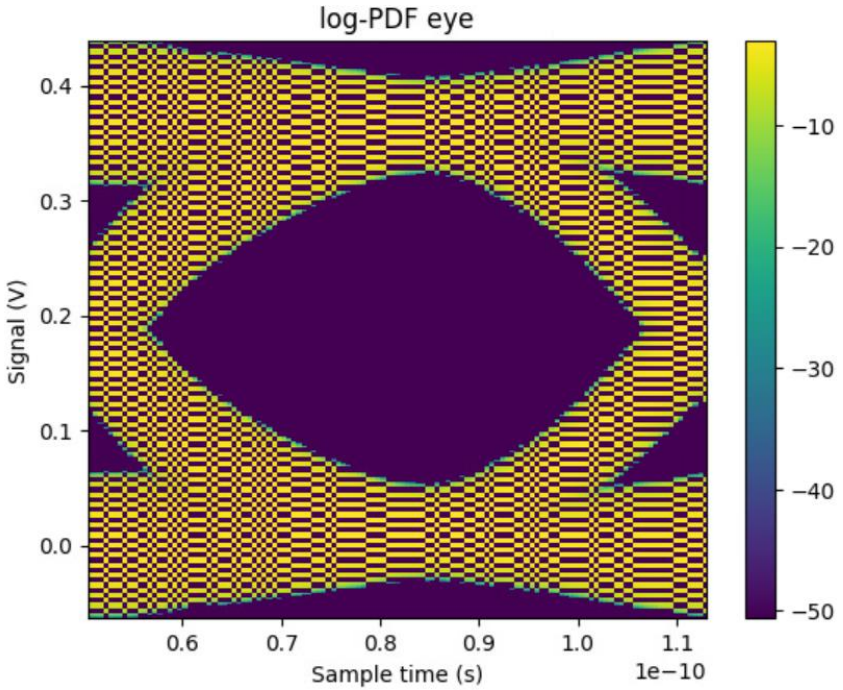
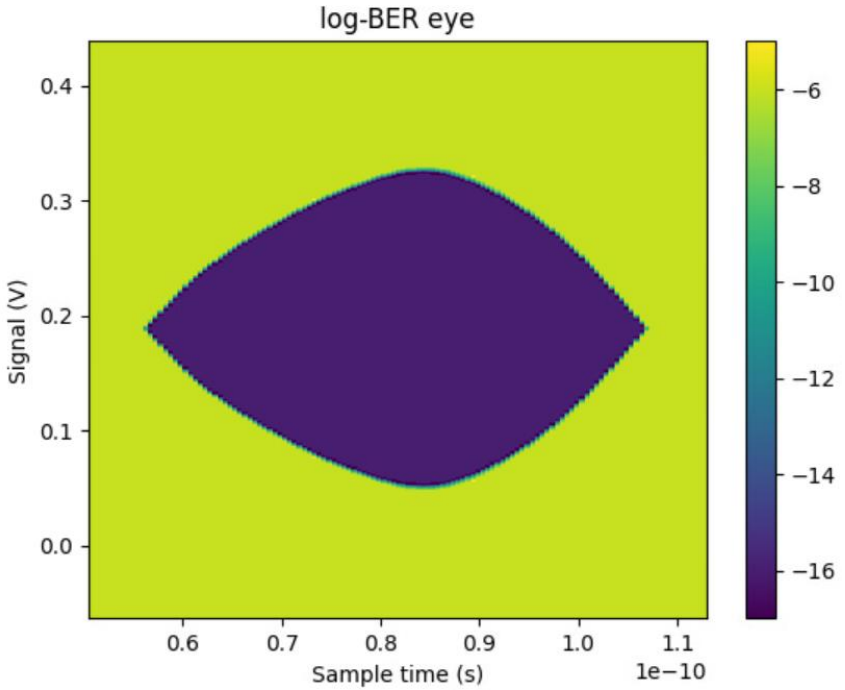
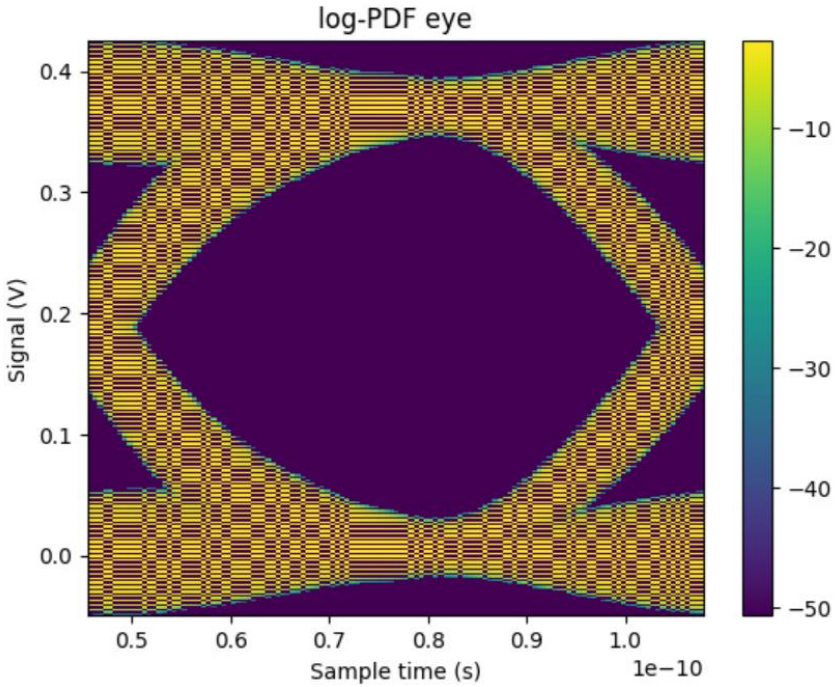
Keysight Results

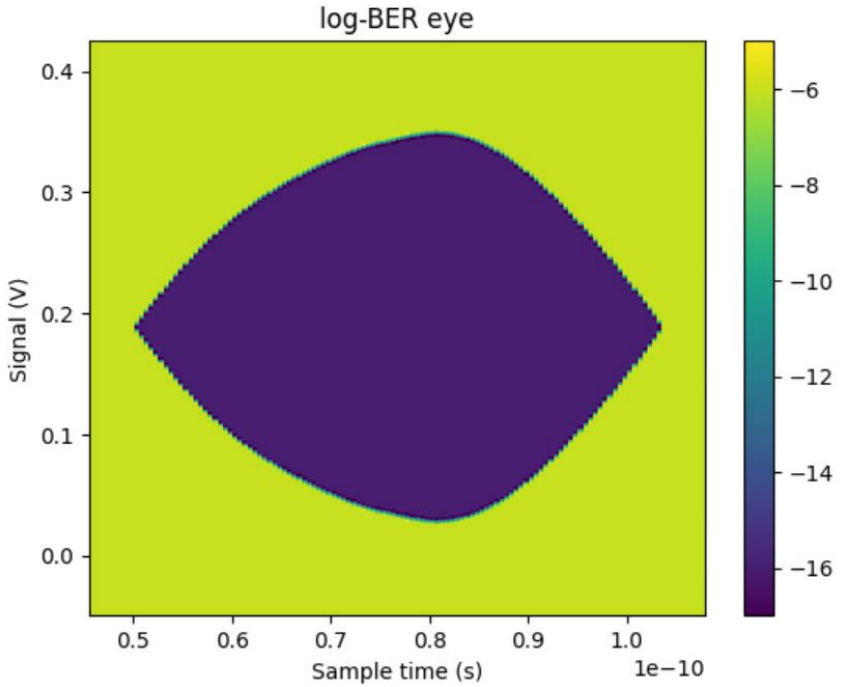




- **Worst line timing margin @ 1e-15 BER: 68%**

Keysight: Cpar = 200fF





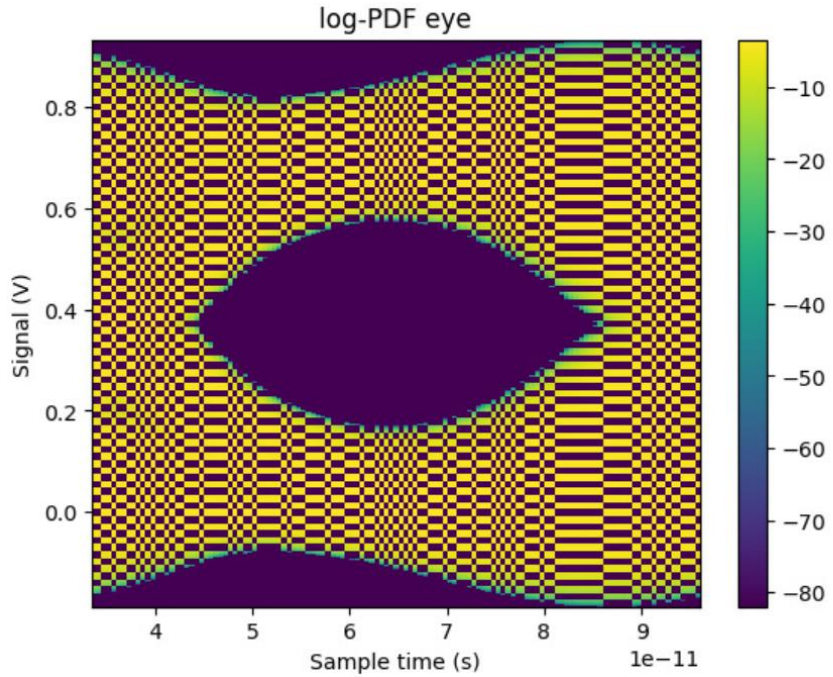
- **Worst line timing margin @ 1e-15 BER: 73.6%**

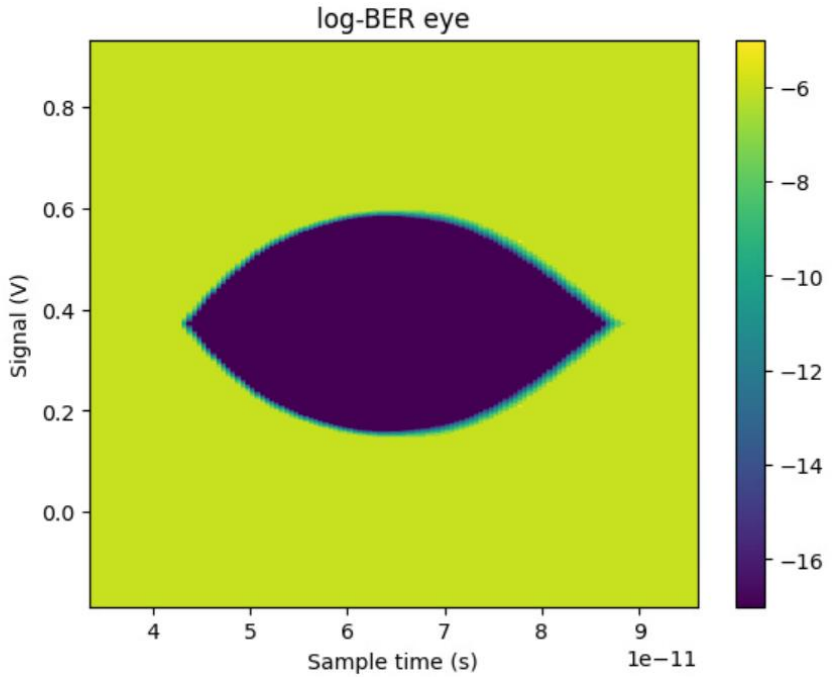
Setup: 16Gb/s Source Terminated

- **Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):**
  - 20% - 80% rise time of 0.32UI
  - R_{TX} = 50Ω (likely worst case; will check other values later)
  - 300fF lumped capacitance on TX/RX
  - VDDIO = 750mV
  - 150mV peak-to-peak RX sensitivity

Full Slice 2mm

Full Slice 2mm Results: Cpar = 200fF





- **Worst line timing margin @ 1e-15 BER: 56%**
- **Worst line timing margin @ 1e-15 BER (75mV sensitivity): 62.4%**

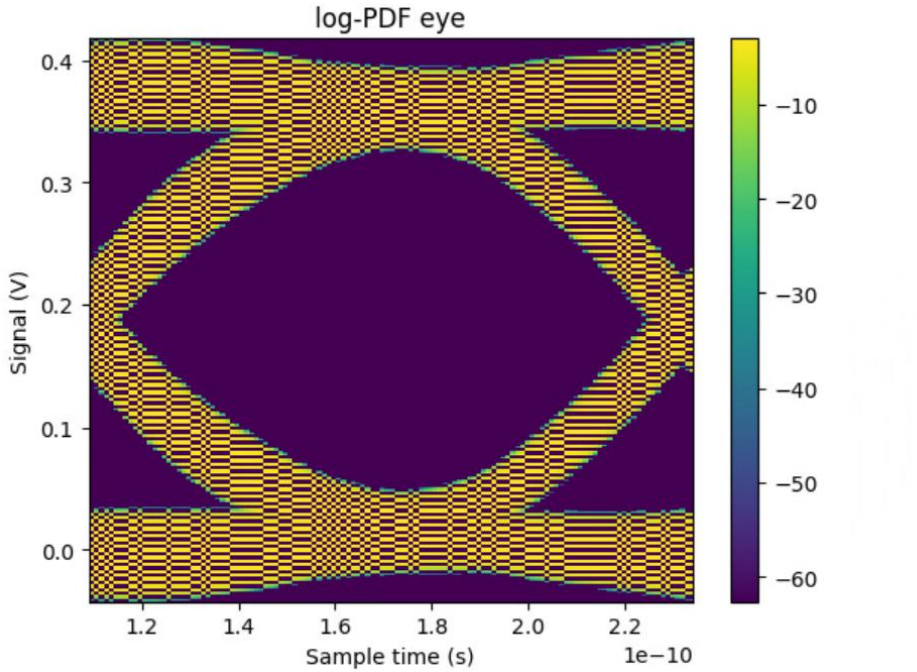
Setup: 8Gb/s Doubly Terminated

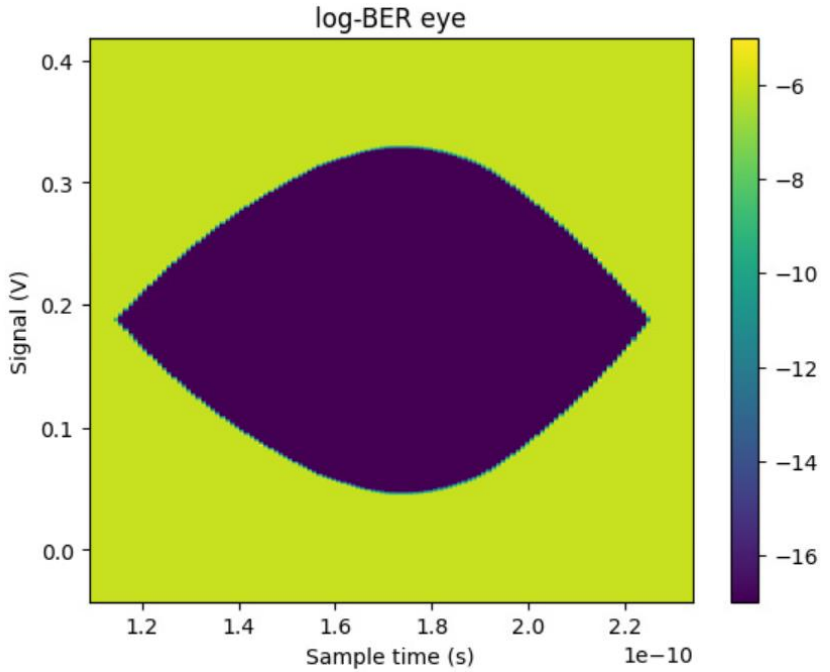
- **Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):**
  - 20% - 80% rise time of 0.32UI
  - $R_{TX} = R_{RX} = 50\Omega$ (likely worst case since this is lowest swing; will check other combinations later)
  - 600fF lumped capacitance on TX/RX
  - VDDIO = 750mV
  - 75mV peak-to-peak RX sensitivity

Full Slice 10mm

BLUE CHEETAH
ANALOG DESIGN

Full Slice 10mm Results





- **Worst line timing margin @ 1e-15 BER: 73.6%**

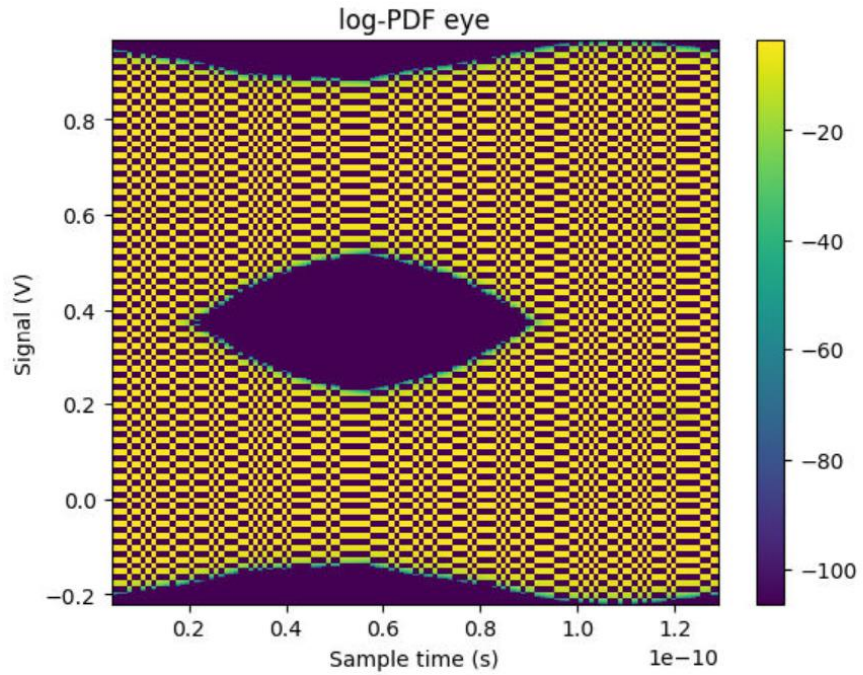
Setup (4): 8Gb/s Source Terminated

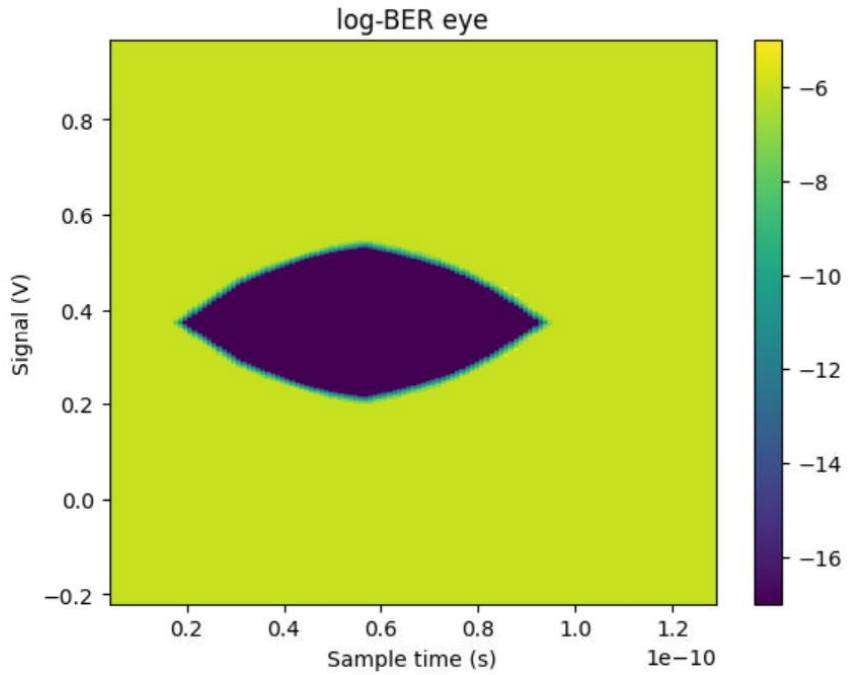
- **Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):**
  - 20% - 80% rise time of 0.32UI
  - R_{TX} = 50Ω (likely worst-case; will check other values later)
  - 600fF lumped capacitance on TX/RX
  - VDDIO = 750mV
  - 150mV peak-to-peak RX sensitivity

Full Slice 10mm

BLUE CHEETAH
ANALOG DESIGN

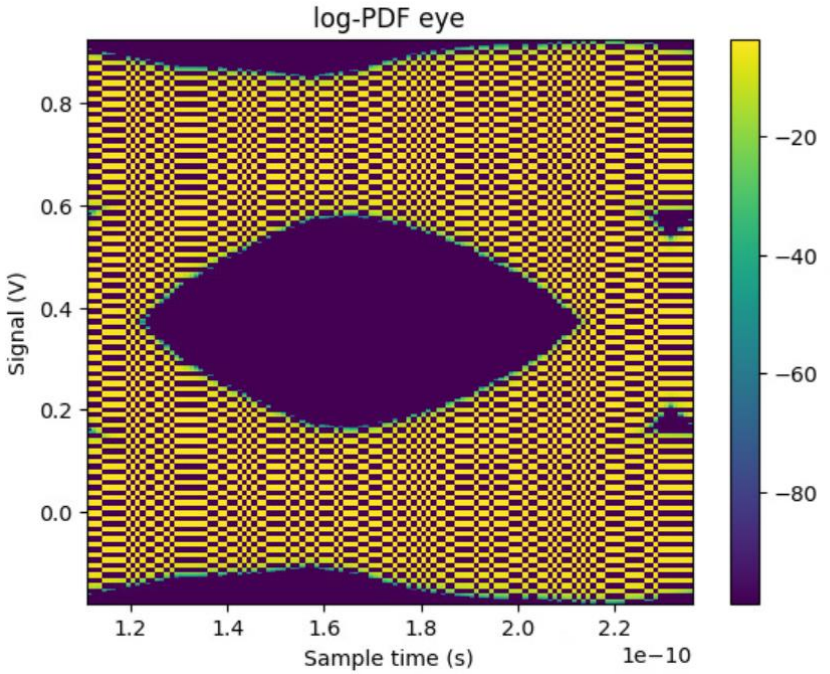
Full Slice 10mm Results

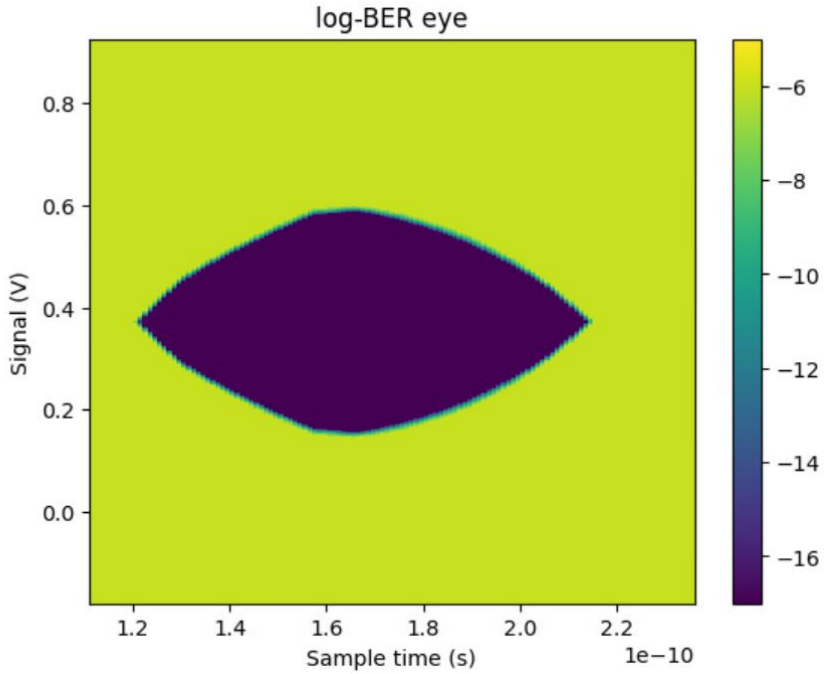




- **Worst line timing margin @ 1e-15 BER: 40.8%**

Full Slice 10mm Results: Cpar = 400fF



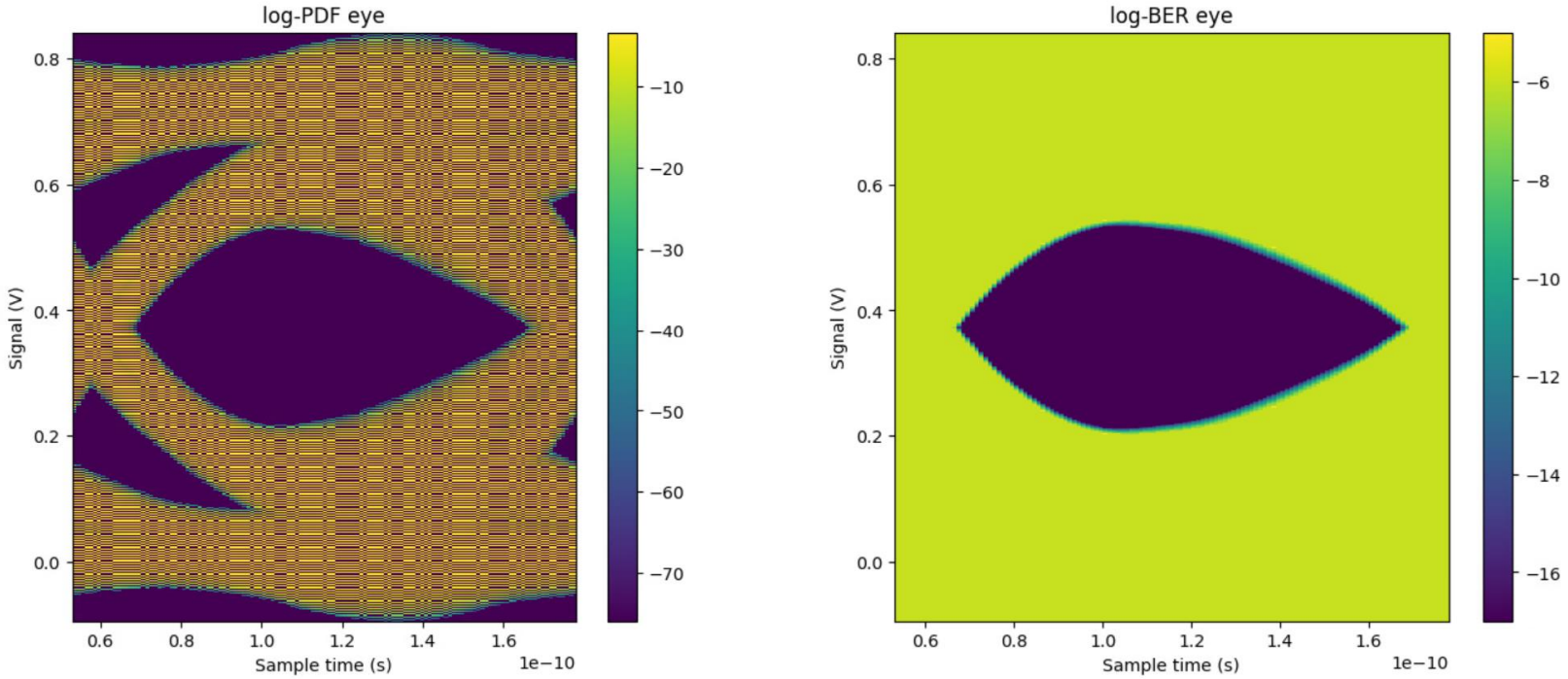


- **Worst line timing margin @ 1e-15 BER: 59.2%**
- **Worst line timing margin @ 1e-15 BER (75mV sensitivity): 67.2%**

Full Slice 2mm

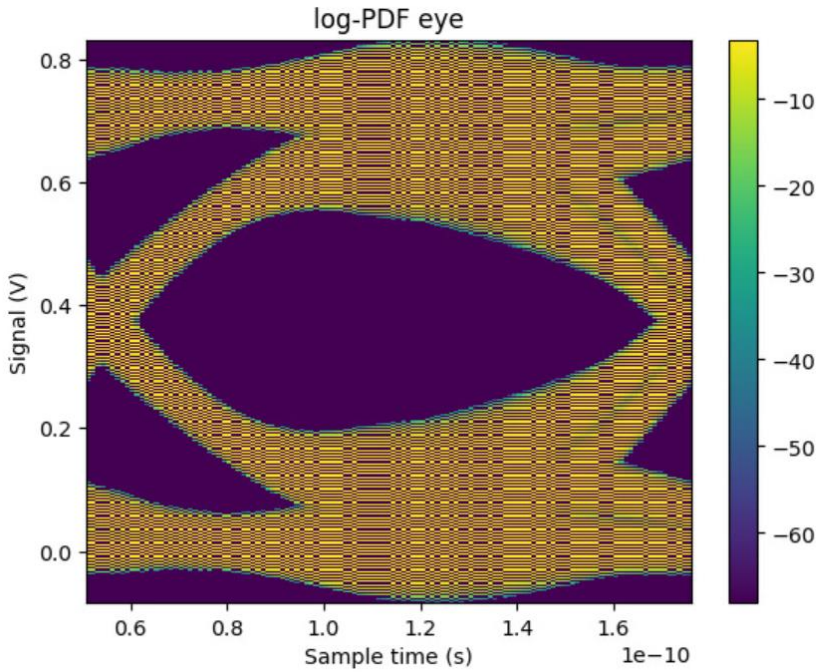
BLUE CHEETAH
ANALOG DESIGN

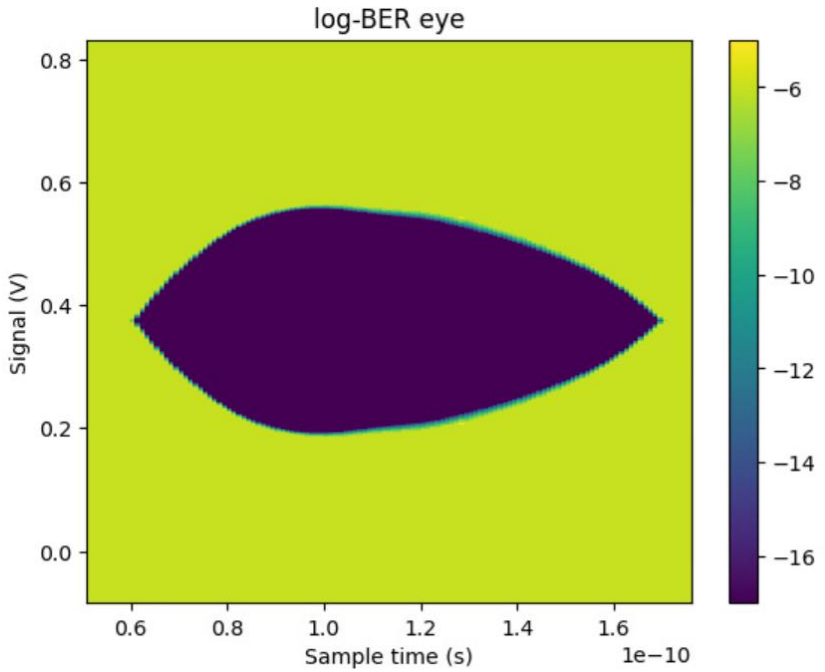
Full Slice 2mm Results



- **Worst line timing margin @ 1e-15 BER: 57.6%**

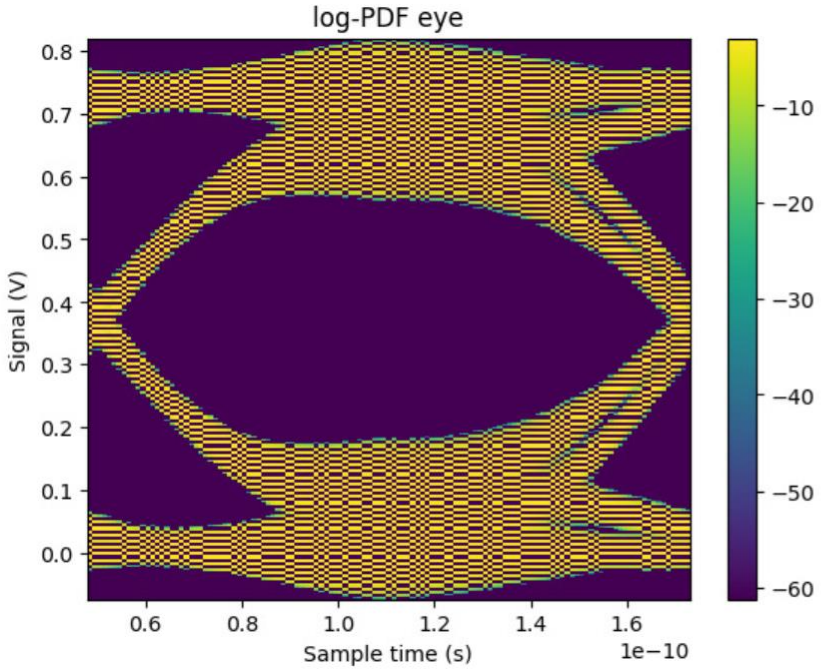
Full Slice 2mm Results: Cpar = 500fF

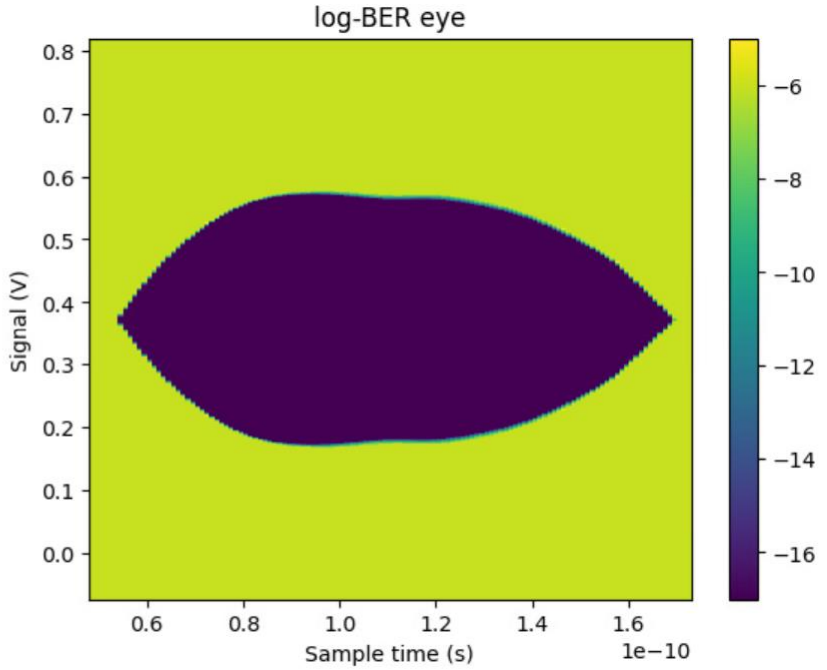




- **Worst line timing margin @ 1e-15 BER: 68.8%**

Full Slice 2mm Results: Cpar = 400fF





- **Worst line timing margin @ 1e-15 BER: 77.6%**

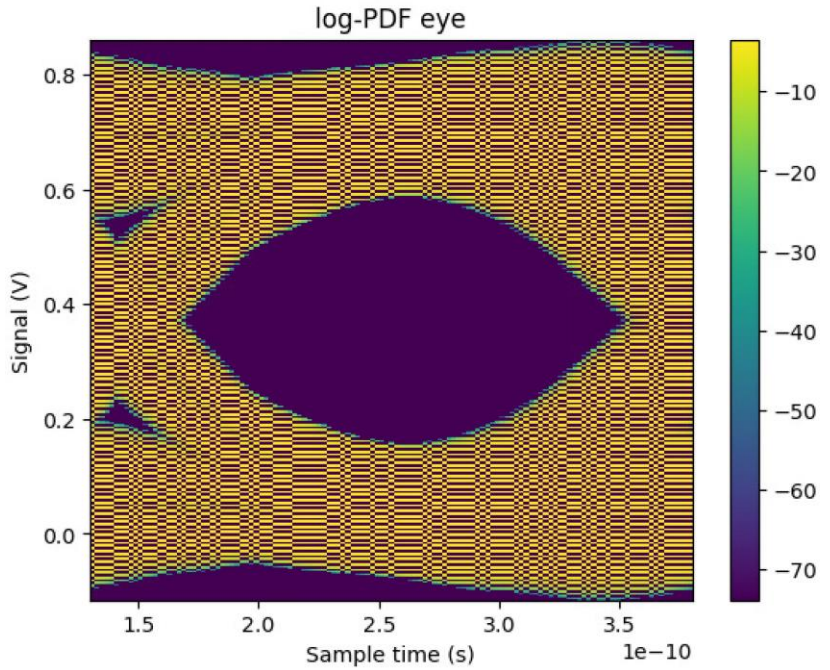
Setup (5): 4Gb/s Source Terminated

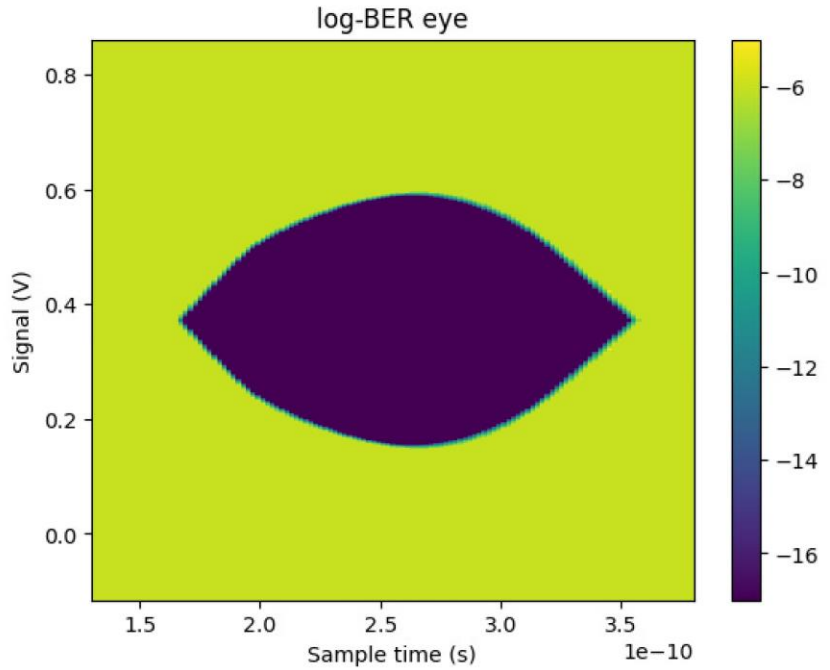
- **Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):**
  - 20% - 80% rise time of 0.32UI
  - R_{TX} = 50Ω (likely worst-case; will check other values later)
  - 1200fF lumped capacitance on TX/RX
  - VDDIO = 750mV
  - 300mV peak-to-peak RX sensitivity

Full Slice 10mm

BLUE CHEETAH
ANALOG DESIGN

Full Slice 10mm Results



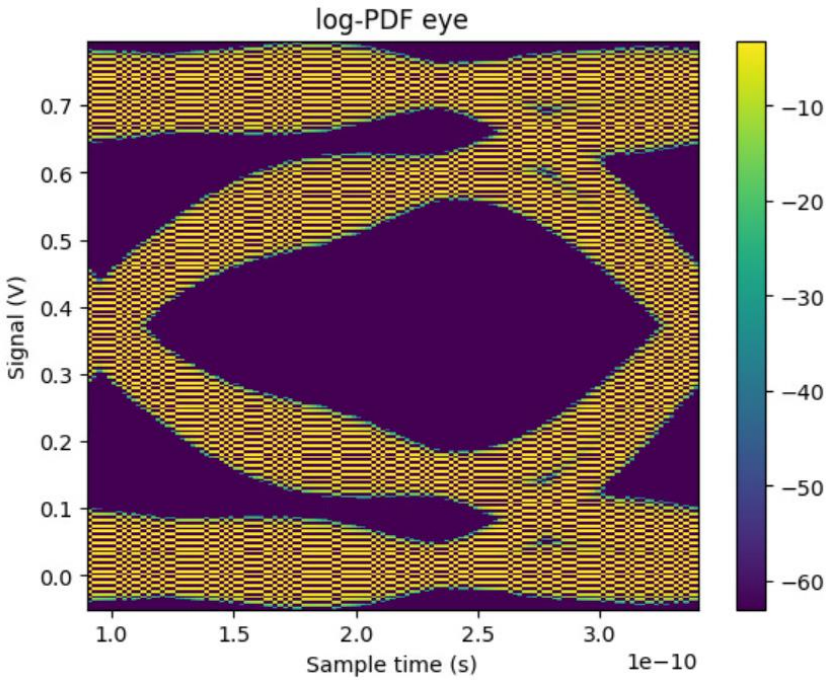


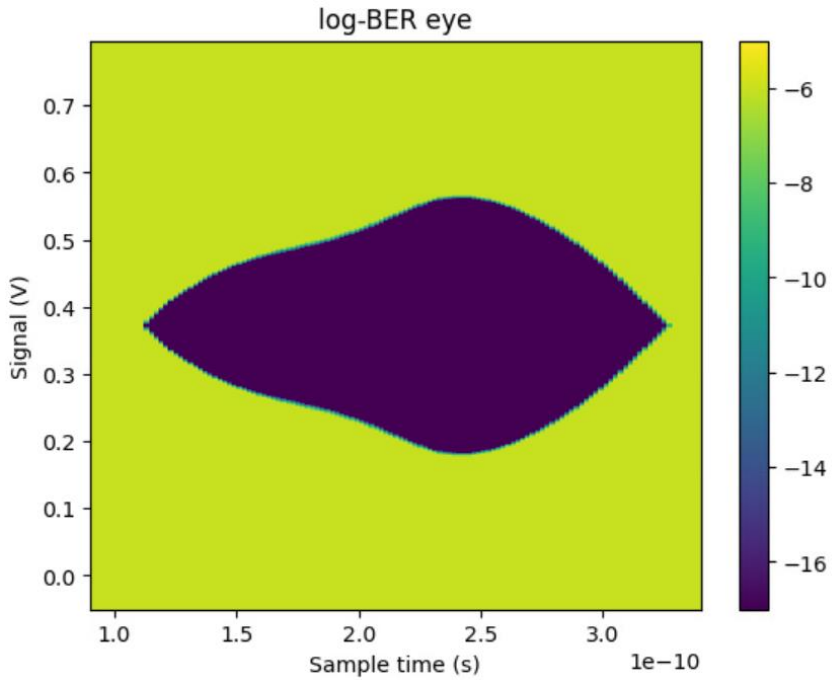
- **Worst line timing margin @ 1e-15 BER: 41.6%**
- **Worst line timing margin @ 1e-15 BER (150mV sensitivity): 59.2%**

Full Slice 2mm

BLUE CHEETAH
ANALOG DESIGN

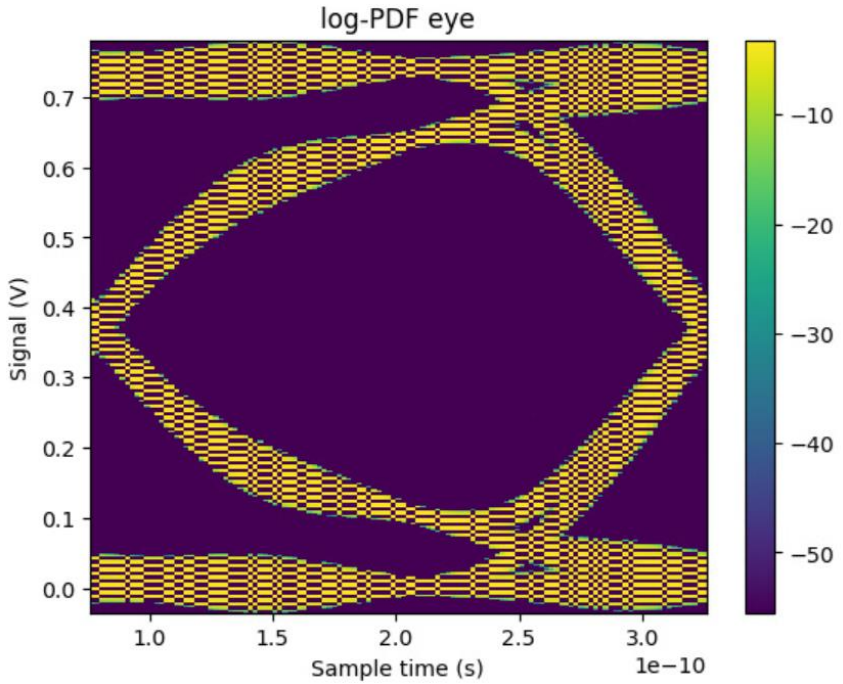
Full Slice 2mm Results

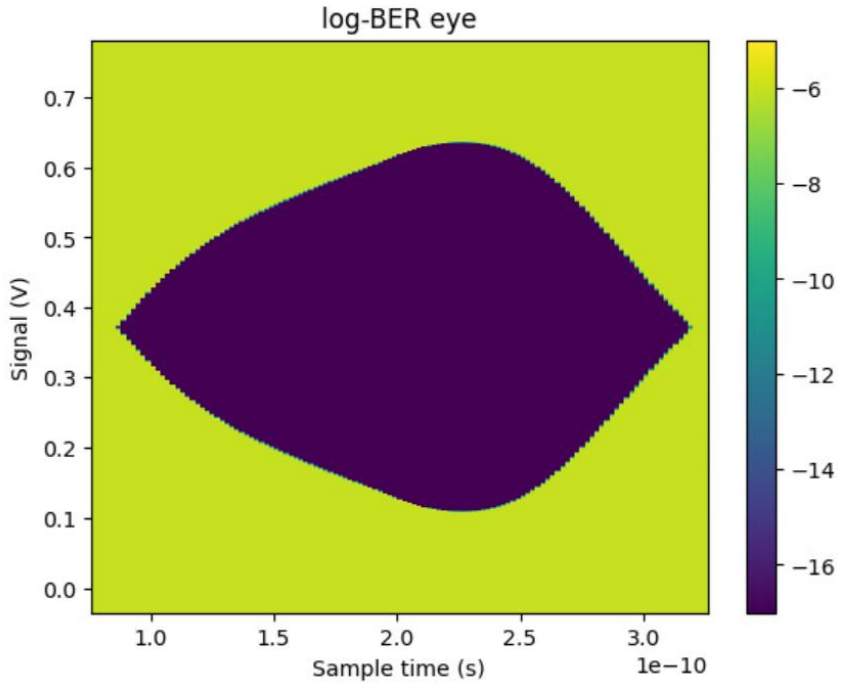




- **Worst line timing margin @ 1e-15 BER: 27.2%**
- **Worst line timing margin @ 1e-15 BER (150mV sensitivity): 63.2%**

Full Slice 2mm Results: Cpar = 800fF



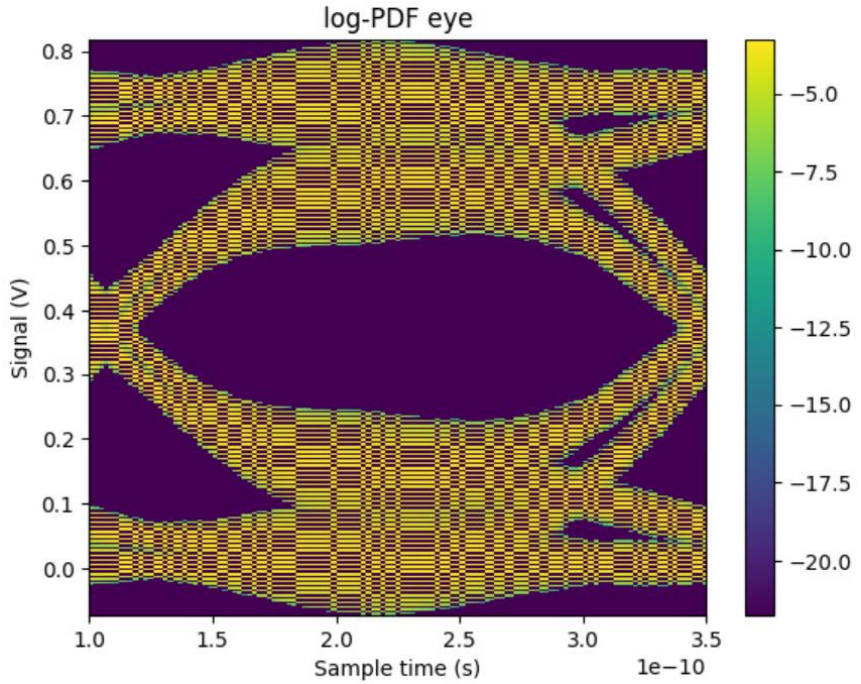


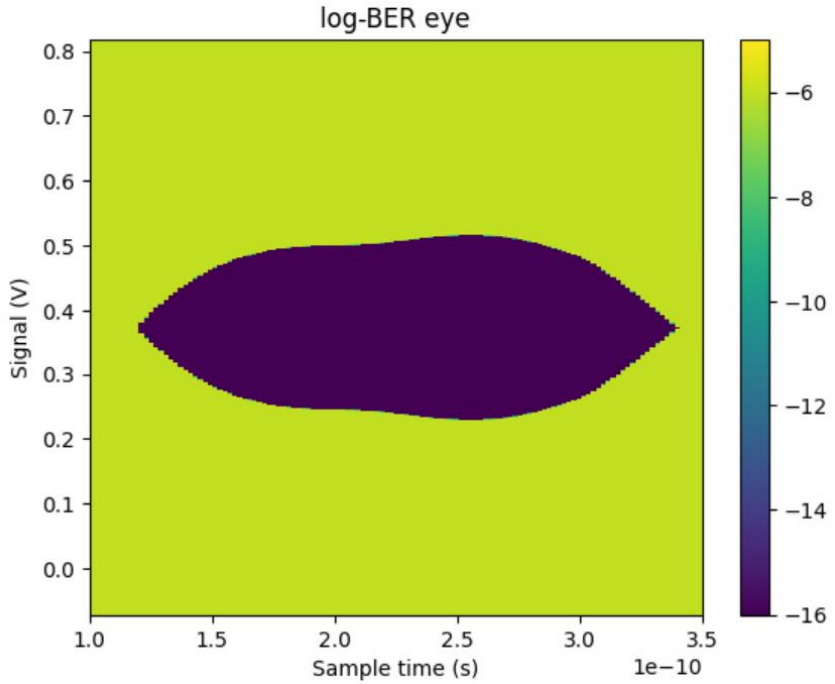
- **Worst line timing margin @ 1e-15 BER: 56.8%**
- **Worst line timing margin @ 1e-15 BER (150mV sensitivity): 76%**

Keysight

BLUE CHEETAH
ANALOG DESIGN

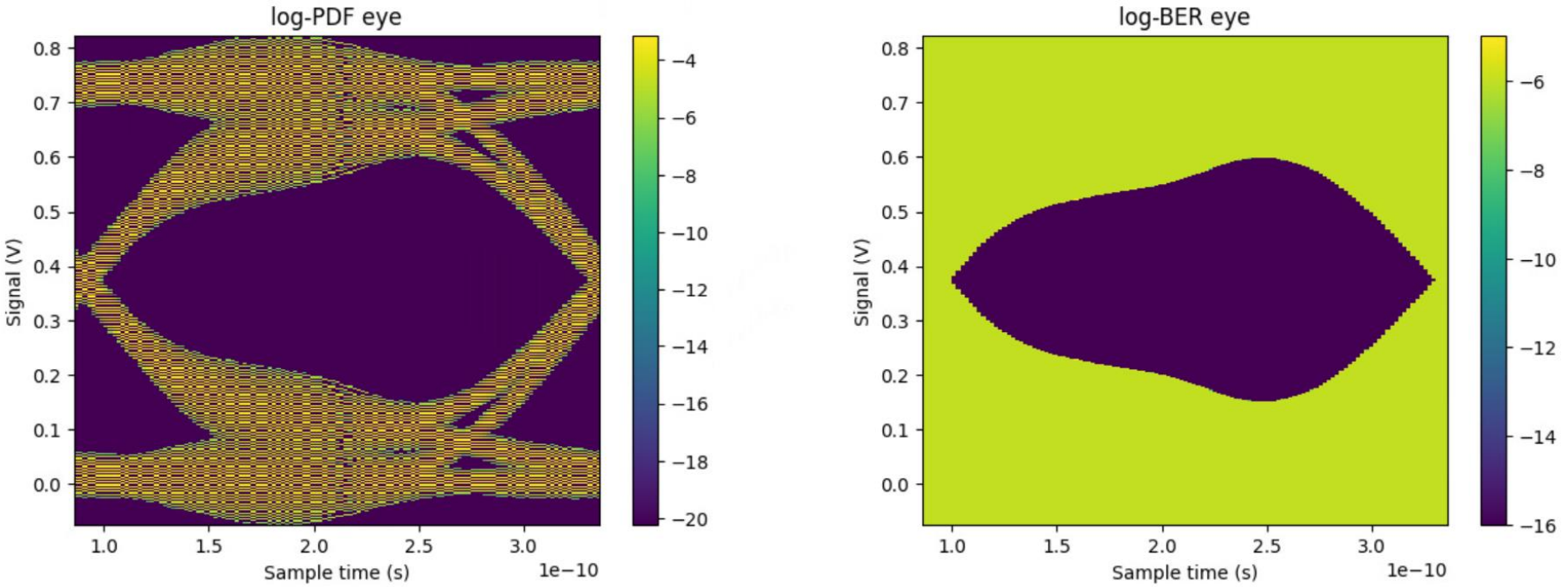
Keysight Results





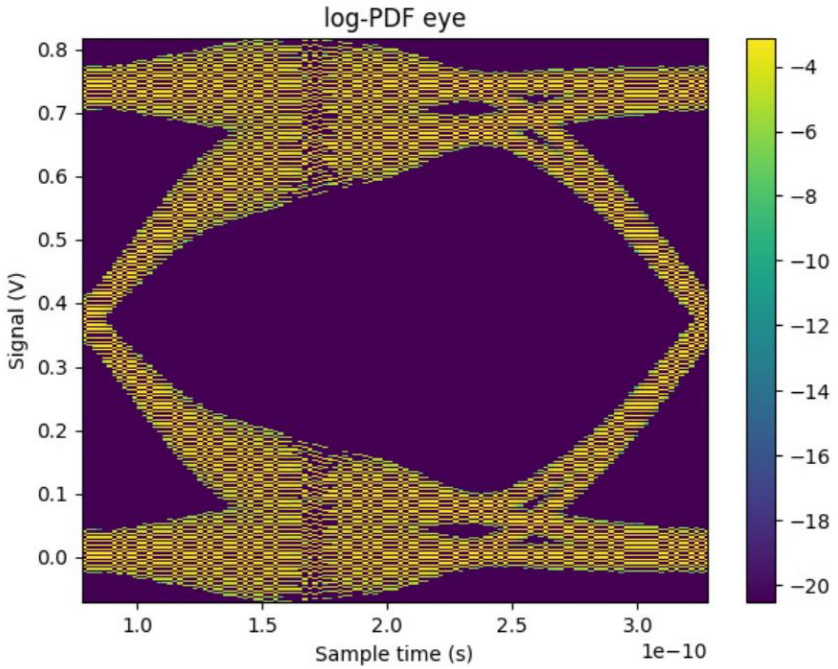
- **Worst line timing margin @ 1e-15 BER: 0%**
- **Worst line timing margin @ 1e-15 BER (150mV sensitivity): 68.8%**

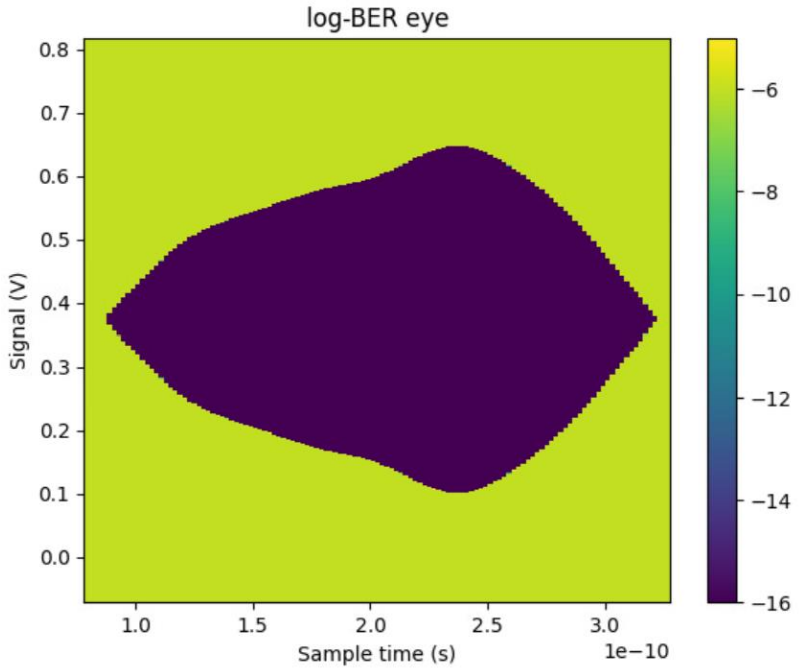
Keysight Results: C_{par} = 800fF



- Worst line timing margin @ 1e-15 BER: **50.4%**
- Worst line timing margin @ 1e-15 BER (150mV sensitivity): **77.6%**

Keysight Results: C_{par} = 600fF





- Worst line timing margin @ 1e-15 BER: 60.8%
- Worst line timing margin @ 1e-15 BER (150mV sensitivity): 80%