

BoW Statistical Channel Model Simulations

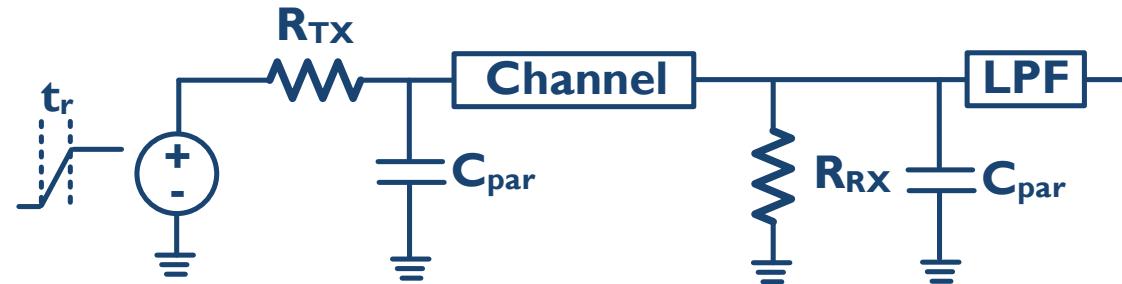


BLUE CHEETAH
ANALOG DESIGN

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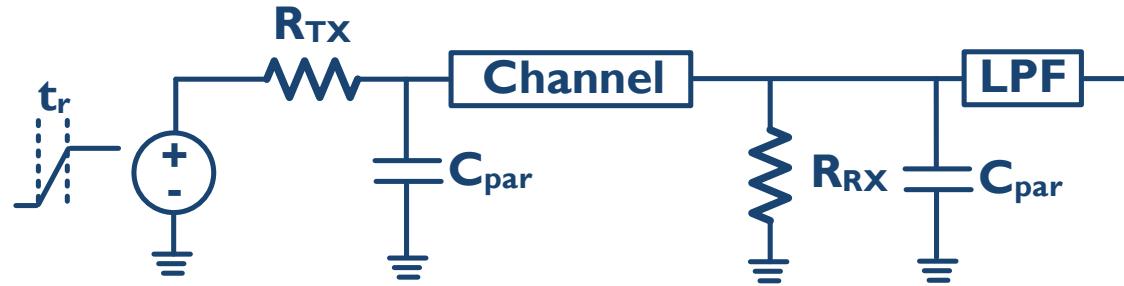
Jan. 18th, 2021

Global Setup: Channel / TX / RX Models



- TX/RX simplified models currently use the same parasitic capacitance on both sides
 - But these can be decoupled; in general we've seen similar SI impact from cap on either side
 - Unterminated signaling modeled by setting R_{RX} to a large value (e.g., $\sim 10K\Omega$)
- Note that as of 12-1-201, risetime is before the RC filter, which is slightly pessimistic
 - Results so far show that risetime does not have a significant impact on margin

Global Setup: Channel / TX / RX Models



- **LPF = Low-Pass Filter**
 - Modeled as a first-order filter
 - Bandwidth of this filter is set to achieve continuous time bandwidth of $2/3/T_{bit}$ (as required in the spec) considering the filtering caused by the channel driving R_{RX} and C_{par}
 - (For reasonable values of R_{RX} and C_{par} , most of the bandwidth is really set by the LPF)

Global Setup: Analysis

- All TX data ports are excited with data, and responses/statistics on all data RX ports are computed
 - In channels that include TX ports for the CLK, those ports are excited with differential clocks
 - In channels that include RX ports for the CLK, those are used to compute jitter due crosstalk
 - Clock RX common-mode to differential voltage conversion gain assumed to be 0.2
- Timing margins are always reported from whatever the worst-case RX data port within a given channel model is
- From BoW spec (as of 12-1-2021), 68% margin is required for a channel to be compliant
 - 50% (eye opening at RX) + 18% (skew / jitter for TX)

Global Setup: Analysis

- **Items not yet included in the analysis (as of 1-3-2022):**
 - Interaction between TX circuit skew and crosstalk statistics
 - Allowed channel skew (all margin numbers assume no skew or perfect per-bit adjustment)

Available Channel Models

- **Channel models contributed by Namhoon Kim (“Full Slice”)**
 - Representative only – not associated with any real design/project
 - Full 16 data wires + clocks for each slice; slices on layers 2 (stripline) and 4 (stripline) are included in a single model
 - Worst-case RX within both slices is found / reported
 - 2mm, 10mm, 25mm reach
- **Channel models developed by ARM**
 - Full 18 data wires + clocks
 - Layers 1 (microstrip), 3 (stripline), and 7 (stripline), ~20mm reach
- **Channel model from Keysight**
 - Includes only 5 wires
 - For clock jitter, run a separate sim with two of the middle lines chosen as CLK+/CLK-
 - 6mm reach

Summary of Results (16 Gb/s)

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	Default	60% (64.8% / 4.8%)	53.6% (56.8% / 3.2%)	53.5% (56.8% / 3.2%)	4.8% (17.6% / 12.8%)		36.8% (42.4% / 5.6%)	60% (64.8% / 4.8%)
	C = 200fF	68% (70.4% / 2.4%)	62.4% (64.8% / 2.4%)	60% (63.2% / 3.2%)	21.6% (34.4% / 12.8%)	62.4% (64.8% / 2.4%)	45.6% (50.4% / 4.8%)	67.2% (70.4% / 3.2%)
	t _r = 23%							
	C = 250fF, t _r = 23%	64.8% (68.8% / 4%)	60.8% (63.2% / 2.4%)	59.2% (62.4% / 3.2%)	21.6% (33.6% / 12%)	60.8% (64% / 3.2%)	43.2% (48.8% / 5.6%)	
	C = 200fF, t _r = 23%			62.4% (65.6% / 3.2%)				
16 Gb/s, Source Terminated	C = 200fF	48% (54.4% / 6.4%)						
	C = 200fF, V _{sen} = 75mV	55.2% (61.6% / 6.4%)						

Summary of Results (8 Gb/s, 4 Gb/s)

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
8 Gb/s, Source Terminated	C = 500fF	67.2% (68.8% / 1.6%)						
	C = 500fF, t _r = 23%	71.2% (72.8% / 1.6%)						52% (55.2% / 3.2%)
	C = 400fF	73.6% (74.4% / 0.8%)	52.4% (56.8% / 6.4%)					57.6% (58.4% / 0.8%)
	C = 400fF, V _{sen} = 75mV		59.2% (65.6% / 6.4%)					68% (68.8% / 0.8%)
4 Gb/s, Source Terminated	C = 1pF, t _r = 23%, V _{sen} = 150mV	65.6% (68% / 2.4%)	62.4% (66.4% / 4%)					72.8% (75.2% / 2.4%)
	C = 800fF	50.4% (51.2% / 0.8%)						39.8% (43.2% / 2.4%)
	C = 800fF, V _{sen} = 150mV	73.6% (74.4% / 0.8%)						70.4% (72.8% / 2.4%)

Updated Global Setup (1-12-2022)

- **Current spec for line-to-line skew on the channel allows for +/-1mm, which without per-bit correct capabilities, requires an additional ~21.3% of UI additional peak-to-peak margin at 16Gb/s**
 - Basically implies that one would have to support per-bit delay correction at 16Gb/s for channels with this kind of skew
 - Or that we need to tighten the length mismatch and recover margin elsewhere
- **All previous sims lumped true random voltage noise at RX into sensitivity figure**
 - This is (intentionally) pessimistic, but may want to revisit this choice to close the overall link budget

Summary of Results (16 Gb/s)

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	C = 200fF $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 40\text{mV}$	71.2% (73.6% / 2.4%)	68% (70.4% / 2.4%)	65.6% (68.8% / 3.2%)	31.2% (44% / 12.8%)	67.2% (69.6% / 2.4%)	52% (56.8% / 4.8%)	69.6% (72.8% / 3.2%)
	C = 250fF, $t_r = 23\%$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 40\text{mV}$	68% (72% / 4%)	65.6% (68% / 2.4%)	64% (67.2% / 3.2%)	29.6% (41.6% / 12%)	64.8% (68% / 3.2%)	48.8% (54.4% / 5.6%)	68% (72% / 4%)
	C = 200fF, $t_r = 23\%$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 40\text{mV}$			66.4% (69.6% / 3.2%)				
	C = 250fF, $t_r = 23\%$ $\sigma_{rx,vn} = 1.57\text{mV}$, $V_{sens,det} = 50\text{mV}$			63.2% (66.4% / 3.2%)				
16 Gb/s, Source Terminated	C = 200fF $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$	52.4% (56.8% / 6.4%)						
	C = 200fF, $V_{sen} = 75\text{mV}$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 40\text{mV}$	58.4% (64.8% / 6.4%)						

Summary of Results (8 Gb/s, 4 Gb/s)

Channel		Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
Rate / Term	Scenario							
8 Gb/s, Source Terminated	C = 500fF $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$	70.4% (72% / 1.6%)						
	C = 500fF, $t_r = 23\%$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$							53.6% (56.8% / 3.2%)
	C = 500fF, $t_r = 23\%$ $\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 100\text{mV}$							54.4% (57.6% / 3.2%)
	C = 400fF $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$	75.2% (76% / 0.8%)	55.6% (60% / 6.4%)					59.2% (60% / 0.8%)
	C = 400fF, $V_{sen} = 75\text{mV}$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 40\text{mV}$		61.6% (68% / 6.4%)					70.4% (71.2% / 0.8%)
4 Gb/s, Source Terminated	C = 1pF, $t_r = 23\%$ $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$	68.8% (71.2% / 2.4%)	64% (68% / 4%)					73.6% (76% / 2.4%)
	C = 800fF $\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 150\text{mV}$	68% (68.8% / 0.8%)						64% (66.4% / 2.4%)
	C = 800fF $\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 115\text{mV}$	75.2% (76% / 0.8%)						71.2% (73.6% / 2.4%)

Proposals from 1-12-2022 Meeting

- (1) Reduce capacitance from 300fF to 250fF for BoW 256 (and scale capacitance for other rates accordingly)
- (2) Tighten 20% - 80% risetime to 23% UI
 - Combination of (1) and (2) improves margin by ~7% UI
- (3) Split TX and RX timing budgets into deterministic and random
 - Reduces pessimism by ~5% UI
- (4) Split RX voltage sensitivity into deterministic and random
 - Reduces pessimism by ~4% UI
- (5) Readjust TX vs. RX total timing budgets to reduce burden on TX
 - Roughly, reduced ~50% eye at RX to ~40%
 - Tighten RX deterministic timing error at lowest rates (BoW 64 and BoW 32) in order to relax RX voltage sensitivity requirements
- (6) Tighten nominal allowed channel skew to 4% UI
 - But will note that implementers may choose to implement per-bit deskew and exceed this
- (7) Tighten RX sensitivity to 112.5mV for BoW 128, 150mV for BoW 64 & BoW 32
 - Original RX sensitivity made even very low rates non-functional due to shape of eye diagram and significant reflections with unterminated signaling

Proposed Timing Budgets

BoW-256, BoW-128

Item	Value	Required Range	Remaining One-Sided Margin
TX Risetime + Channel (ISI + XTALK + CLK DJ) Eye Opening (UI)	64.00%		0.32
Channel Residual Static Clk-Data Skew (UI, p2p)	4.00%		0.3
TX Deterministic Clk-Data + Duty Cycle Error (UI, p2p)	14.00%		0.23
Deterministic Margin at RX (UI)	46.00%		0.23
RX Deterministic Clk-Data Error (UI, p2p)	32.00%		0.07
One-Sided Margin for Jitter (UI)		14.00%	0.07
Random Jitter Subcomponents		Value in ps at 16Gb/s	
TX Random Jitter After RX Delay (σ , UI)	0.69%	0.43	
Total TX Random Jitter @ 1e-15 (UI, p2p)	11.00%	6.875	
RX Random Jitter (σ , UI)	0.54%	0.34	
Total RX Random Jitter @ 1e-15 (UI, p2p)	8.66%	5.41	
Total Random Jitter After RX Delay (σ , UI)	0.88%	0.55	
Total Random Jitter @ 1e-15 (UI, p2p)	14.00%	8.75	

BoW-64, BoW-32

Item	Value	Required Range	Remaining One-Sided Margin
TX Risetime + Channel (ISI + XTALK + CLK DJ) Eye Opening (UI)	60.00%		0.3
Channel Residual Static Clk-Data Skew (UI, p2p)	4.00%		0.28
TX Deterministic Clk-Data + Duty Cycle Error (UI, p2p)	14.00%		0.21
Deterministic Margin at RX (UI)	42.00%		0.21
RX Deterministic Clk-Data Error (UI, p2p)	28.00%		0.07
One-Sided Margin for Jitter (UI)		14.00%	0.07
Random Jitter Subcomponents		Value in ps at 16Gb/s	
TX Random Jitter After RX Delay (σ , UI)	0.69%	0.43	
Total TX Random Jitter @ 1e-15 (UI, p2p)	11.00%	6.875	
RX Random Jitter (σ , UI)	0.54%	0.34	
Total RX Random Jitter @ 1e-15 (UI, p2p)	8.66%	5.41	
Total Random Jitter After RX Delay (σ , UI)	0.88%	0.55	
Total Random Jitter @ 1e-15 (UI, p2p)	14.00%	8.75	

Setup Updates for Final Results

- **Tightened simulation time resolution from 0.8% to 0.4%**
 - To reduce quantization error from subtraction of data margin and crosstalk jitter computations
- **As of 1-15-2022, simulated only channels / conditions at the boundaries of compliance**

Final Results (16 Gb/s)

Channel Rate / Term	Scenario	Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
16 Gb/s, Doubly Terminated	C = 250fF, t _r = 23% $\sigma_{rx,vn} = 2.2\text{mV}$, V _{sens,det} = 40mV			64.4% (67.2% / 2.8%)		64% (67.6% / 3.6%)		
	C = 200fF, t _r = 23% $\sigma_{rx,vn} = 2.2\text{mV}$, V _{sens,det} = 40mV			67.2% (70% / 2.8%)		68.4% (70.8% / 2.4%)		
16 Gb/s, Source Terminated	C = 200fF, V _{sen} = 75mV $\sigma_{rx,vn} = 2.2\text{mV}$, V _{sens,det} = 40mV	59.2% (65.6% / 6.4%)						

Summary of Results (8 Gb/s, 4 Gb/s)

Channel		Full Slice 2mm	Full Slice 10mm	Full Slice 25mm	ARM Layer A	ARM Layer B	ARM Layer D	Keysight
Rate / Term	Scenario							
8 Gb/s, Source Terminated	C = 500fF, t _r = 23% $\sigma_{rx,vn} = 3.14\text{mV}$, V _{sens,det} = 100mV	73.6% (75.6% / 2%)						53.6% (57.2% / 3.6%)
	C = 500fF, t _r = 23% $\sigma_{rx,vn} = 2.2\text{mV}$, V _{sens,det} = 65mV	78% (80% / 2%)						59.2% (62.8% / 3.6%)
	C = 400fF $\sigma_{rx,vn} = 3.14\text{mV}$, V _{sens,det} = 100mV	78% (79.6% / 1.6%)						63.2% (64.8% / 1.6%)
	C = 400fF, t _r = 23% $\sigma_{rx,vn} = 2.2\text{mV}$, V _{sens,det} = 65mV	81.6% (83.2% / 1.6%)						69.6% (70.8% / 1.2%)
4 Gb/s, Source Terminated	C = 1pF, t _r = 23% $\sigma_{rx,vn} = 4.71\text{mV}$, V _{sens,det} = 225mV	42% (44.4% / 2.4%)						29.6% (32% / 2.4%)
	C = 1pF, t _r = 23% $\sigma_{rx,vn} = 3.14\text{mV}$, V _{sens,det} = 150mV	60.8% (63.2% / 2.4%)						68.8% (71.2% / 2.4%)
	C = 800fF $\sigma_{rx,vn} = 4.71\text{mV}$, V _{sens,det} = 225mV	42% (53.2% / 0.8%)						41.2% (43.6% / 2.4%)
	C = 800fF $\sigma_{rx,vn} = 3.14\text{mV}$, V _{sens,det} = 150mV	68% (68.8% / 0.8%)						69.2% (71.6% / 2.4%)

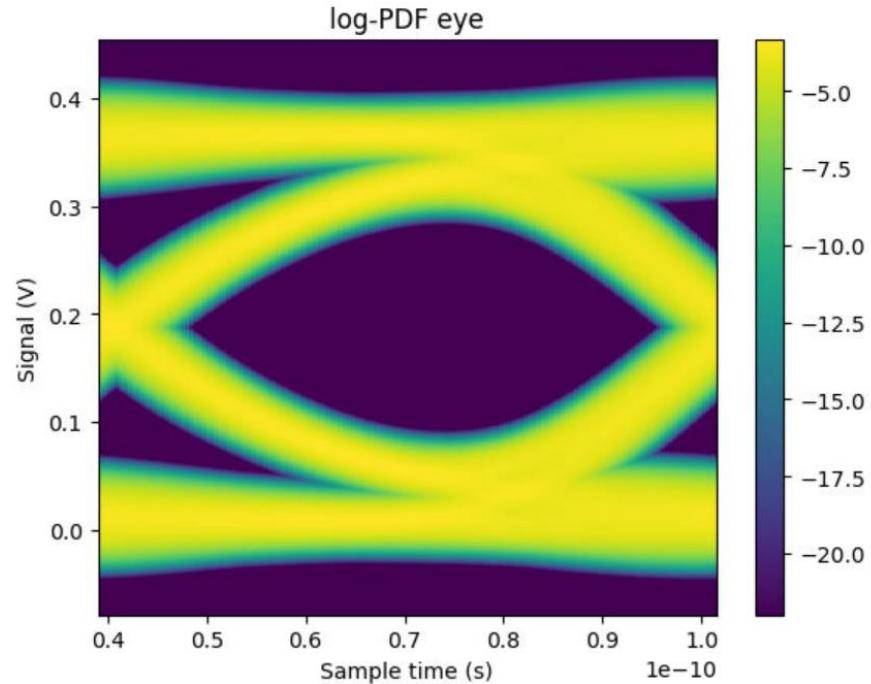
Final Results: 16Gb/s Doubly Terminated

ARM Layer B Results:

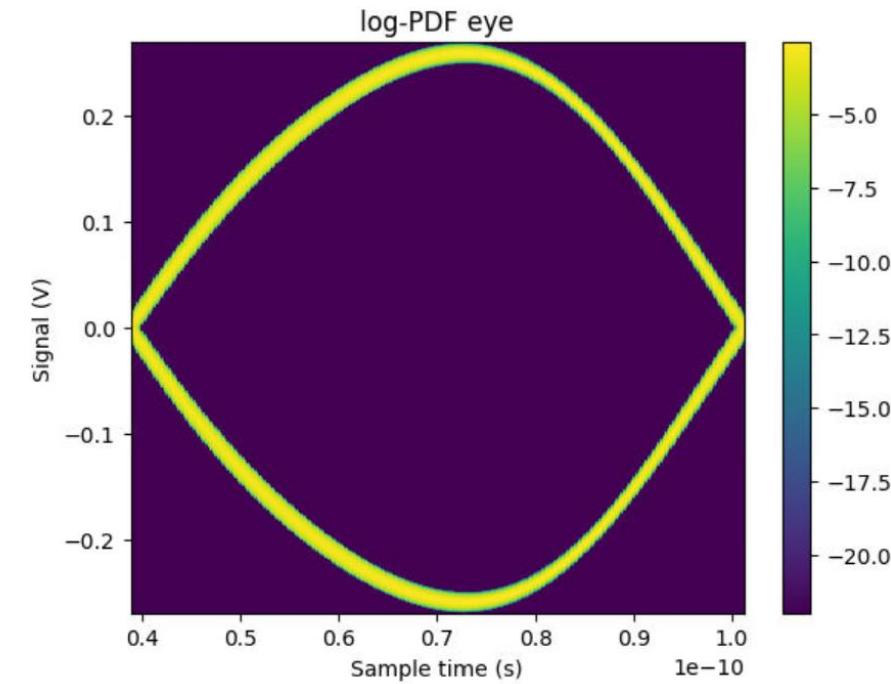
20%-80% risetime = 23% UI, Cpar = 250fF



Worst Data Eye



Diff. Clock



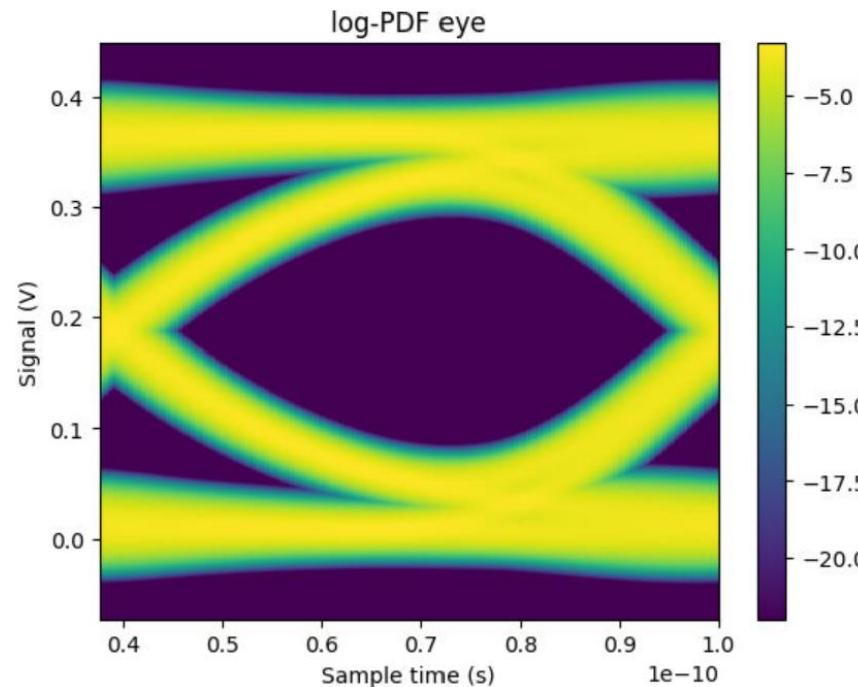
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 67.6% / 3.6%**

ARM Layer B Results:

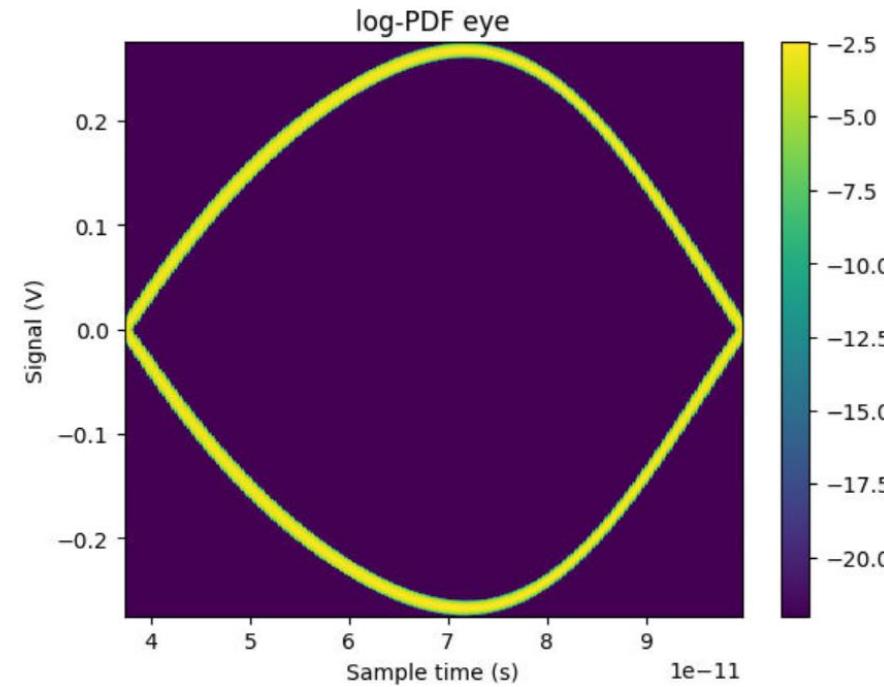
20%-80% risetime = 23% UI, Cpar = 200fF



Worst Data Eye



Diff. Clock



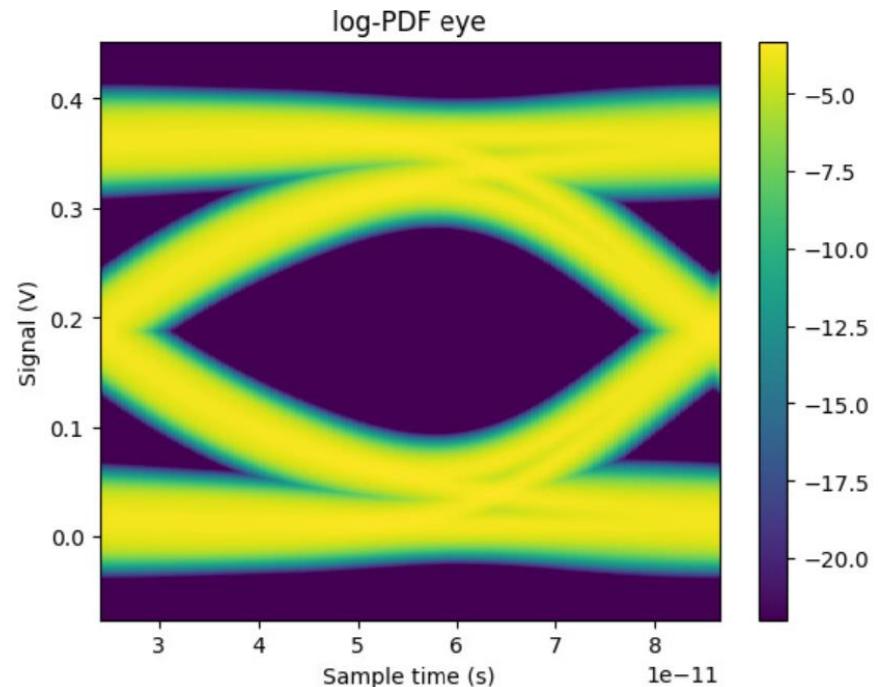
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 70.8% / 2.4%**

Full Slice 25mm Results:

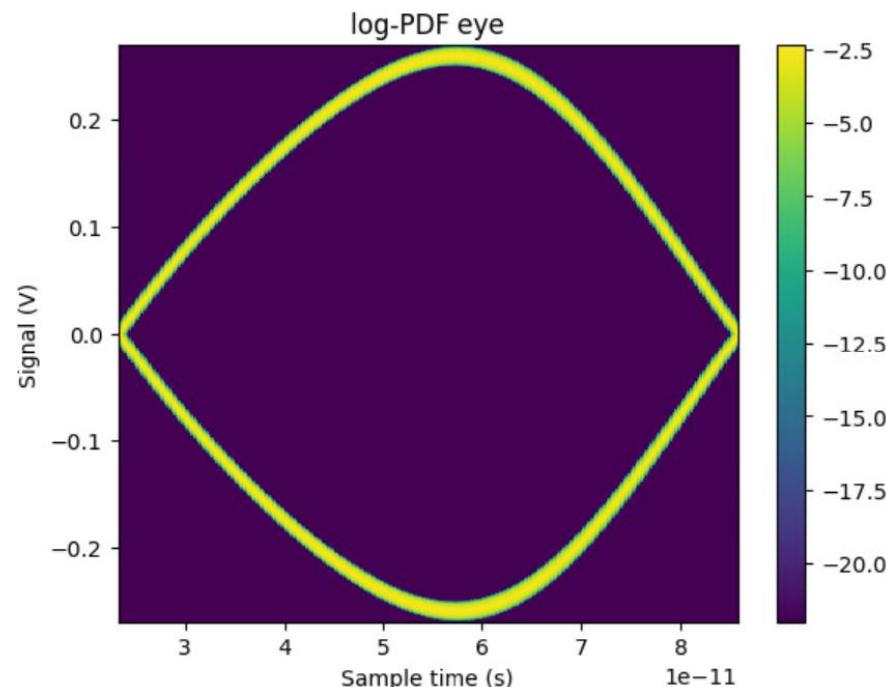


20%-80% risetime = 23% UI, Cpar = 250fF

Worst Data Eye



Diff. Clock



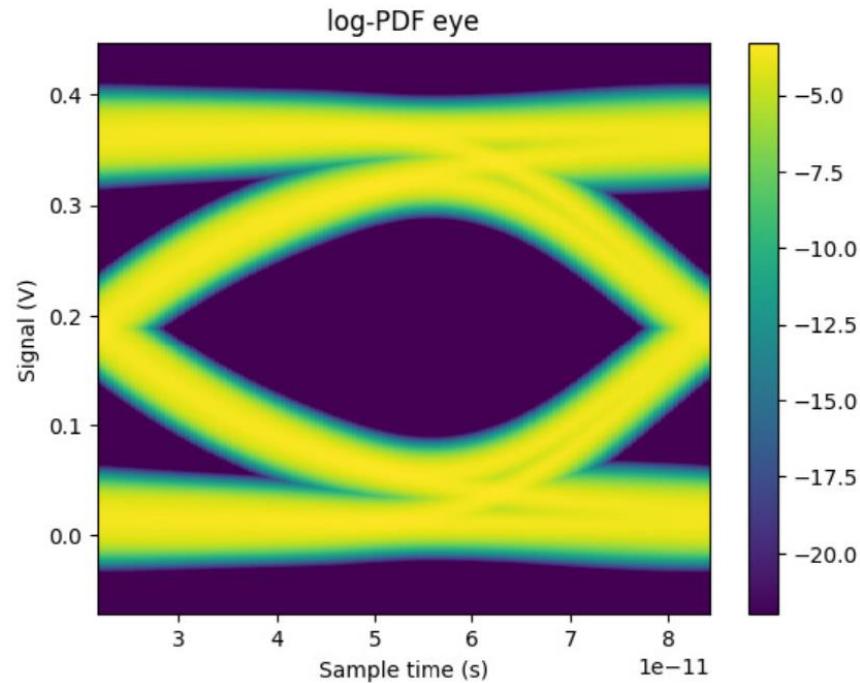
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 67.2% / 2.8%**

Full Slice 25mm Results:

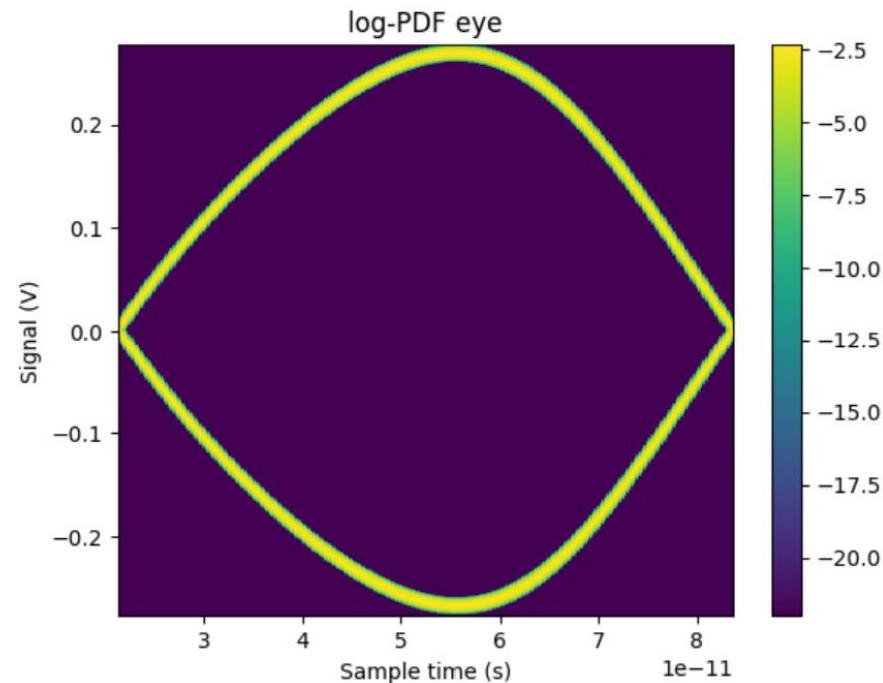


20%-80% risetime = 23% UI, Cpar = 200fF

Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 70% / 2.8%**

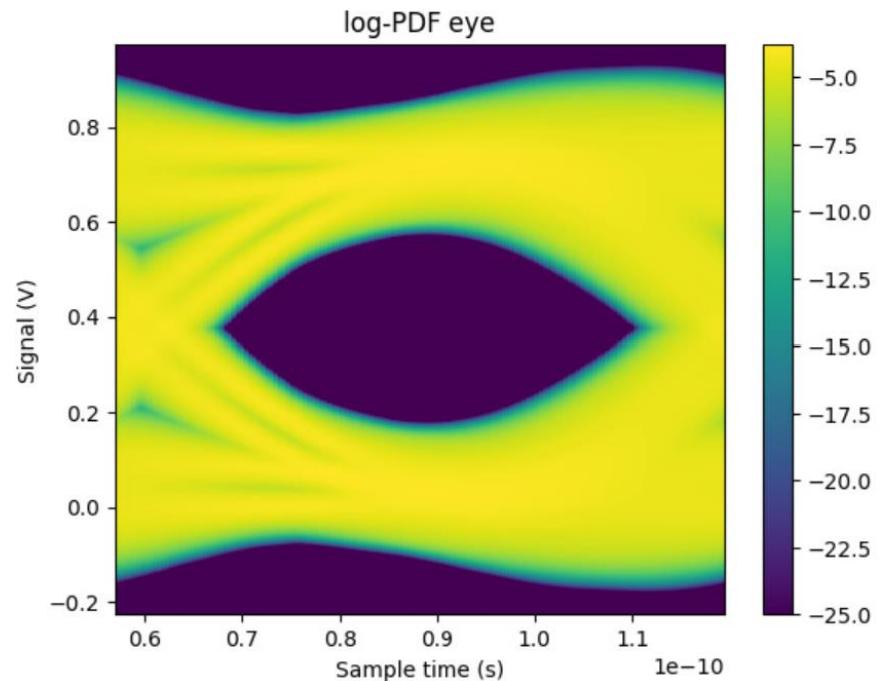
Final Results: 16Gb/s Source Terminated

Full Slice 2mm Results:

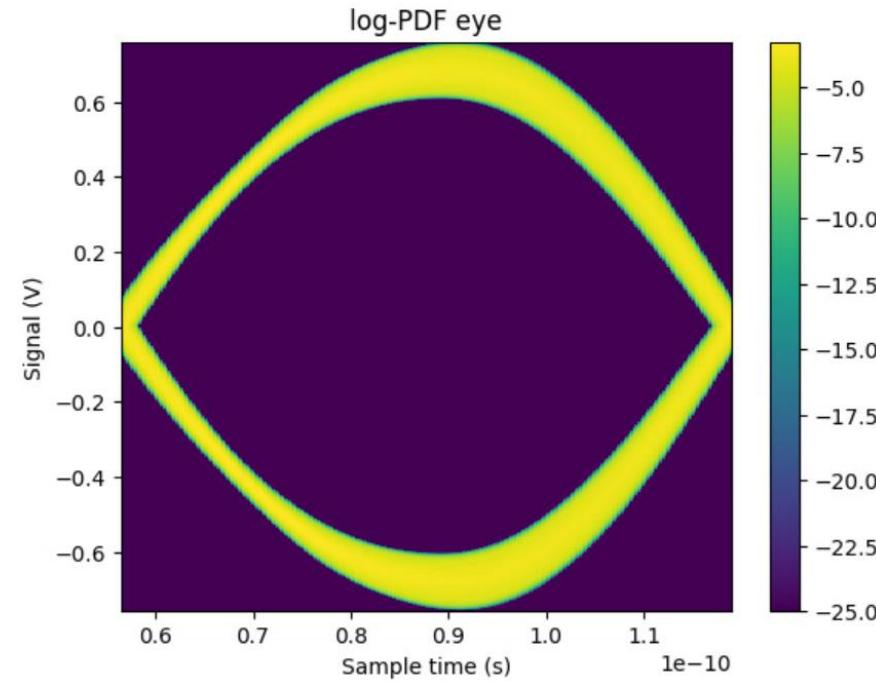
20%-80% risetime = 23% UI, Cpar = 200fF



Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 65.6% / 6.4%**

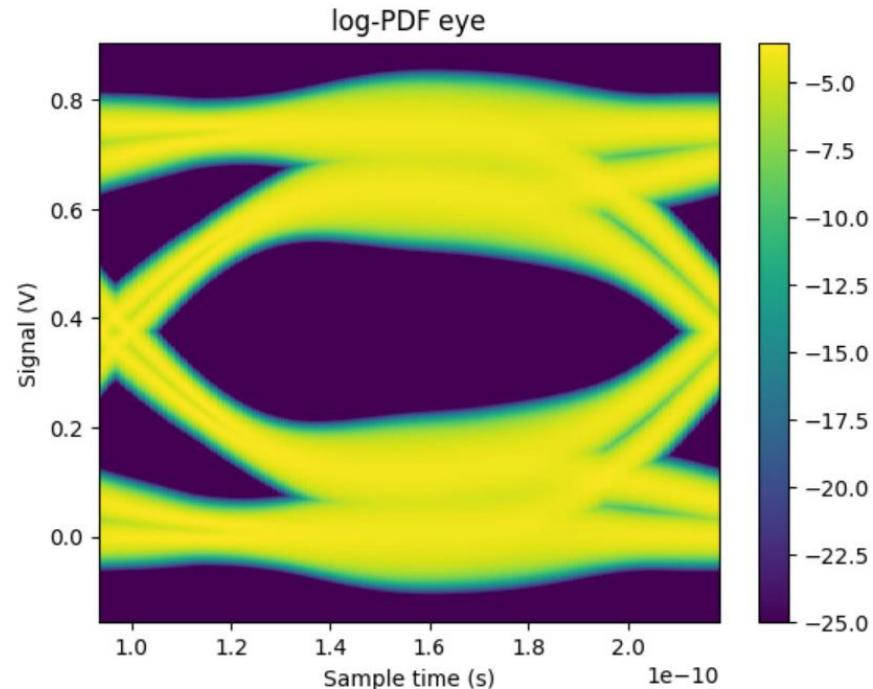
Final Results: 8Gb/s Source Terminated

Full Slice 2mm Results:

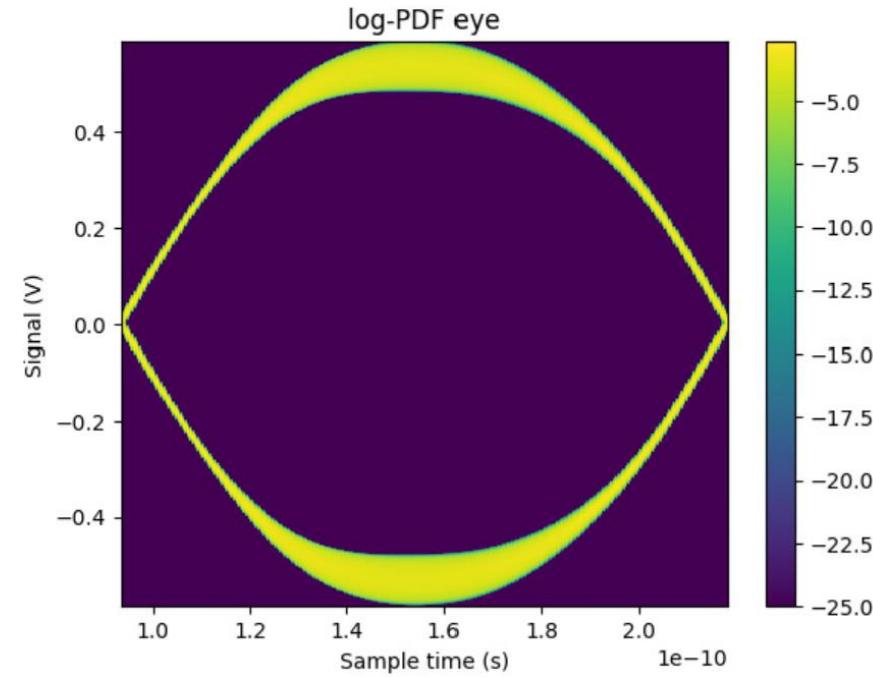
20%-80% risetime = 23% UI, Cpar = 500fF



Worst Data Eye



Diff. Clock



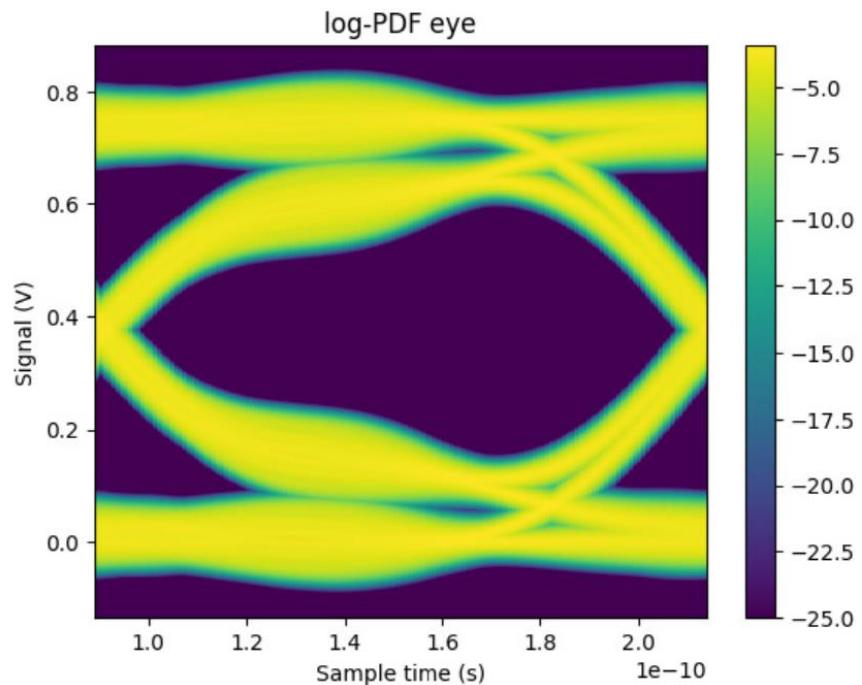
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 100\text{mV}$): 75.6% / 2%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 65\text{mV}$): 80% / 2%**

Full Slice 2mm Results:

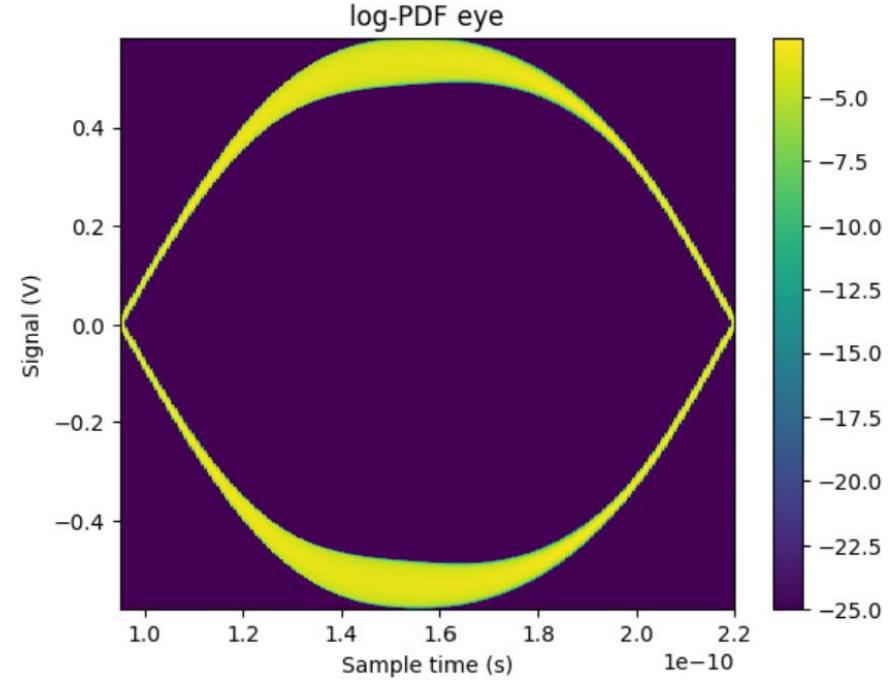
20%-80% risetime = 23% UI, Cpar = 400fF



Worst Data Eye



Diff. Clock



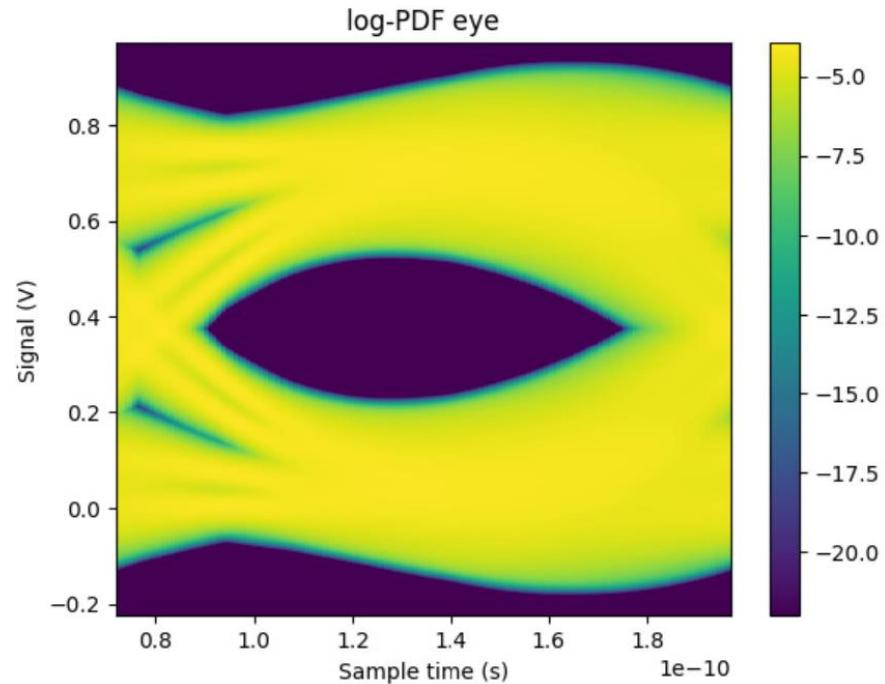
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 100\text{mV}$): 79.6% / 1.6%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 65\text{mV}$): 83.2% / 1.6%**

Keysight Results:

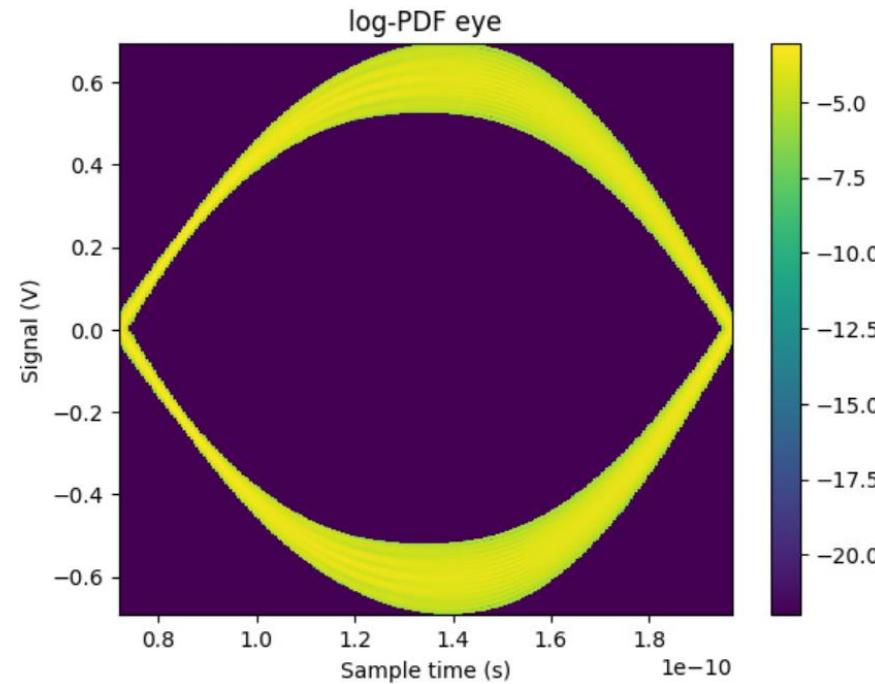
20%-80% risetime = 23% UI, Cpar = 500fF



Worst Data Eye



Diff. Clock



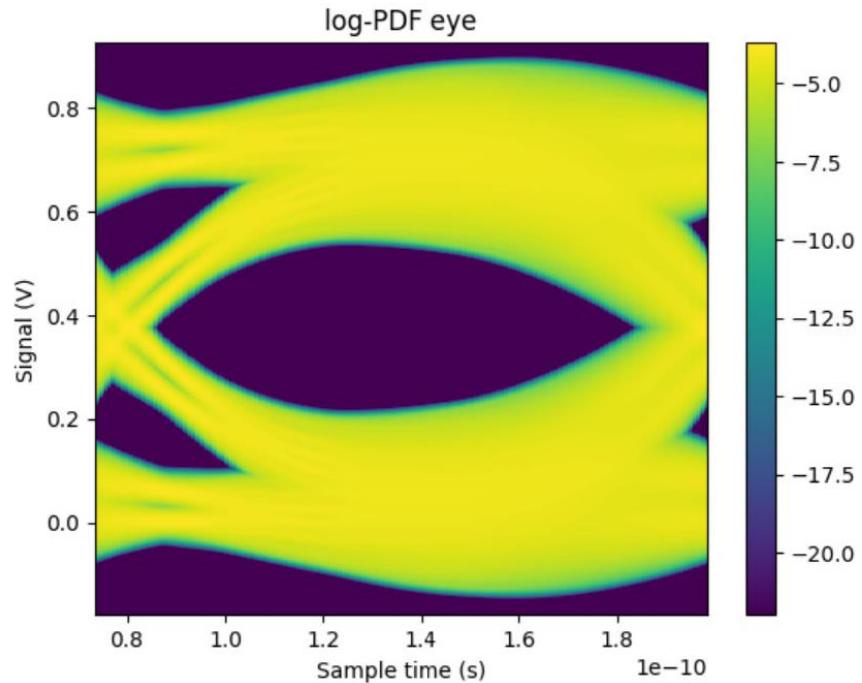
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 100\text{mV}$): 57.2% / 3.6%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 65\text{mV}$): 62.8% / 3.6%**

Keysight Results:

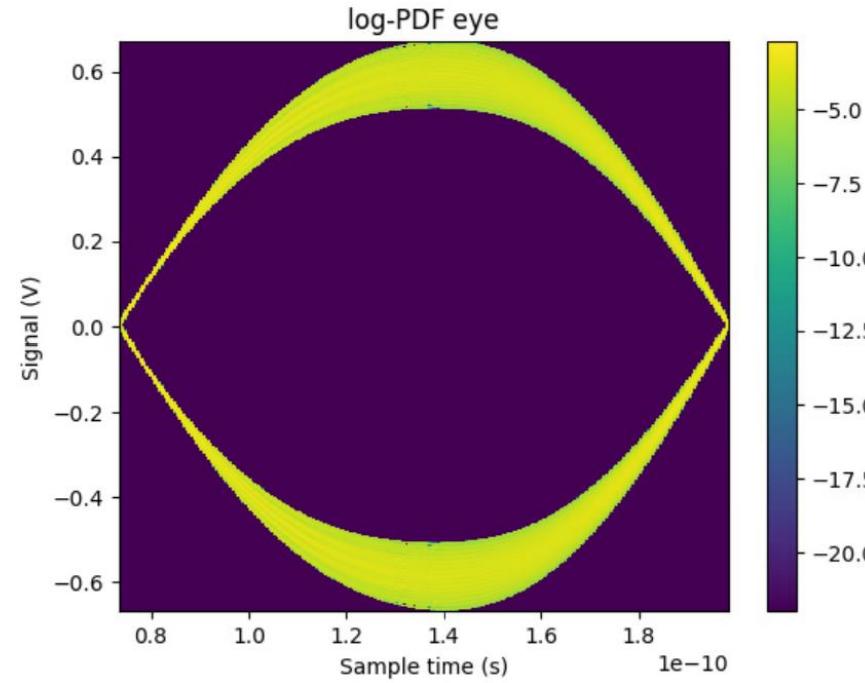
20%-80% risetime = 23% UI, Cpar = 400fF



Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 100\text{mV}$): 70.8% / 1.2%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 2.2\text{mV}$, $V_{sens,det} = 65\text{mV}$): 64.8% / 1.2%**

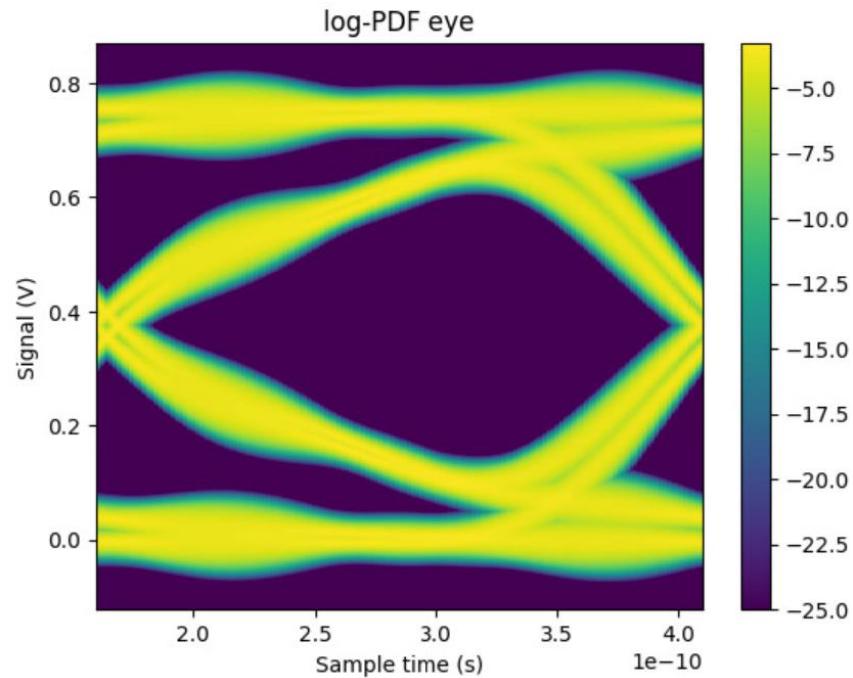
Final Results: 4Gb/s Source Terminated

Full Slice 2mm Results:

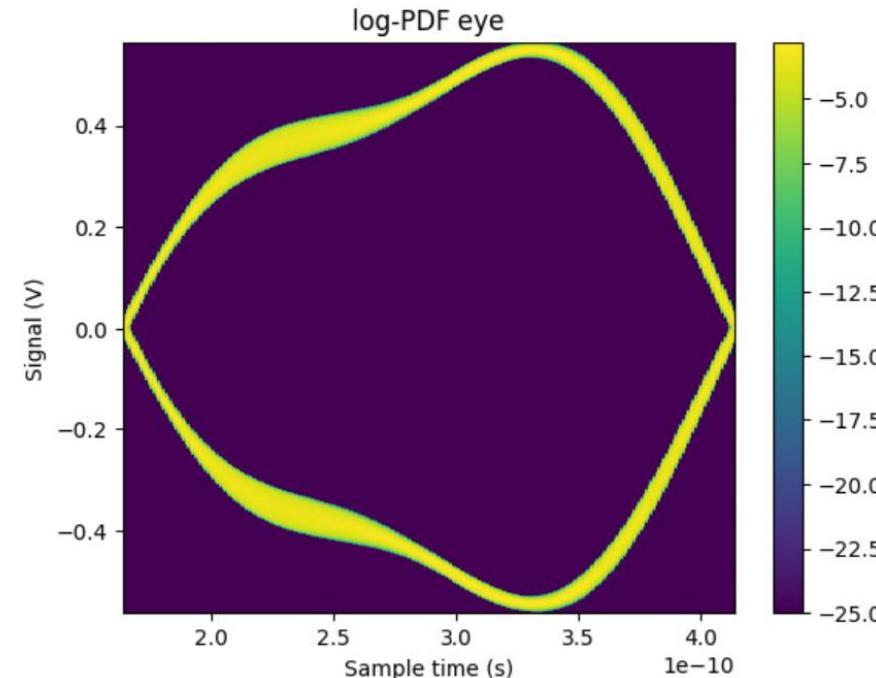
20%-80% risetime = 23% UI, Cpar = 1pF



Worst Data Eye



Diff. Clock



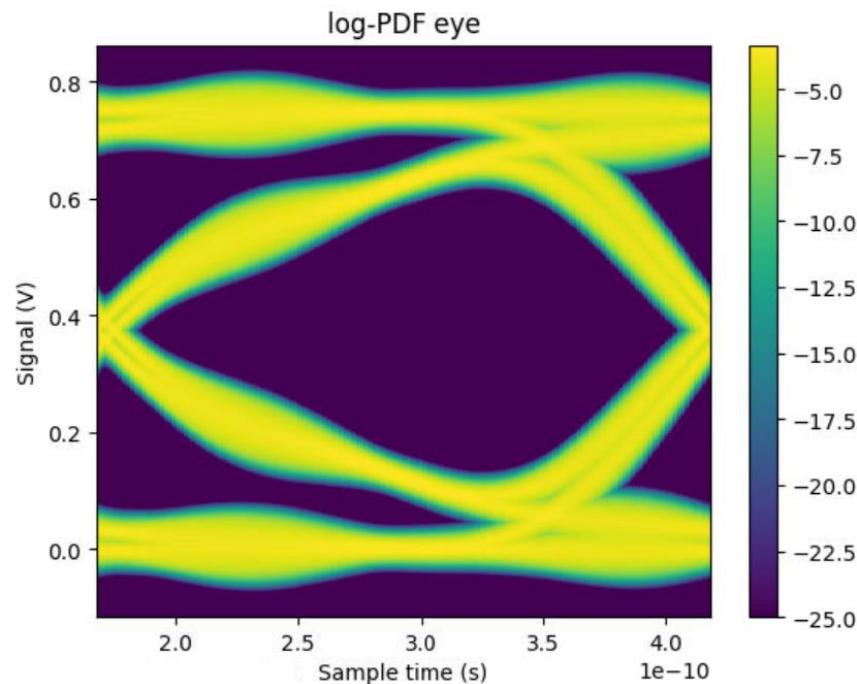
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 4.71\text{mV}$, $V_{sens,det} = 225\text{mV}$): 44.4% / 2.4%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 150\text{mV}$): 63.2% / 2.4%**

Full Slice 2mm Results:

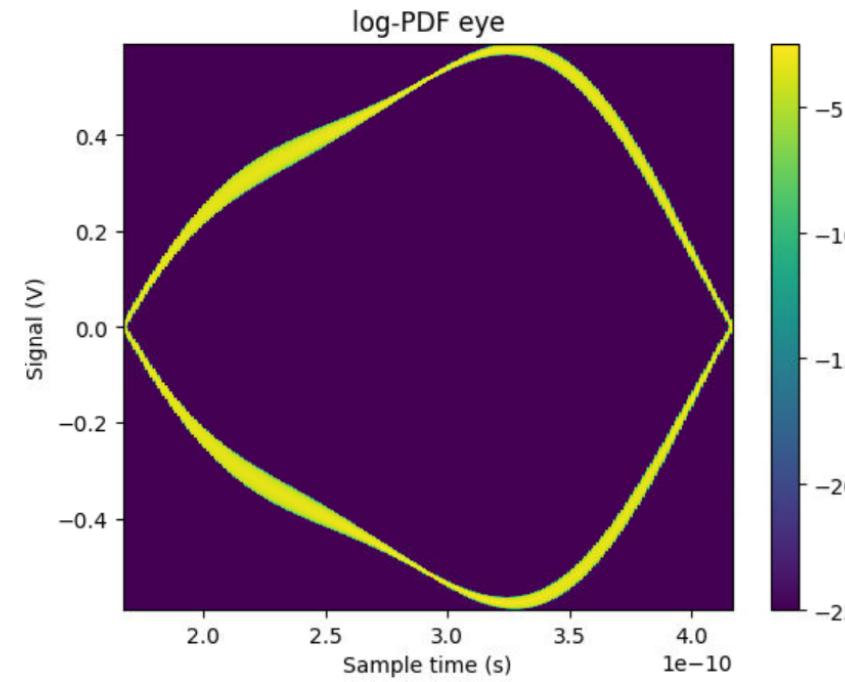


20%-80% risetime = 23% UI, Cpar = 800fF

Worst Data Eye



Diff. Clock



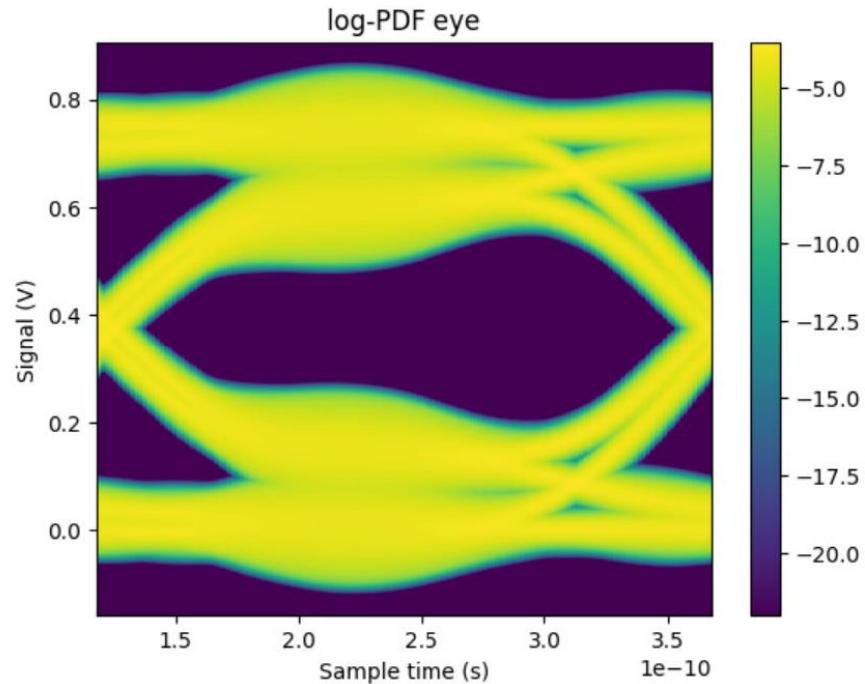
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 4.71\text{mV}$, $V_{sens,det} = 225\text{mV}$): 53.2% / 2.4%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 150\text{mV}$): 68.8% / 0.8%**

Keysight Results:

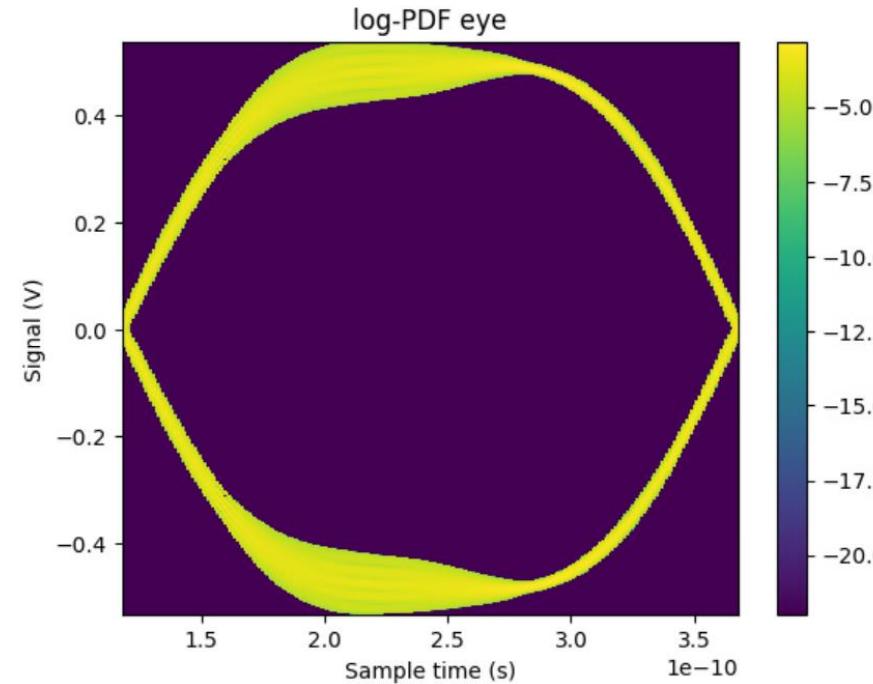
20%-80% risetime = 23% UI, Cpar = 1pF



Worst Data Eye



Diff. Clock



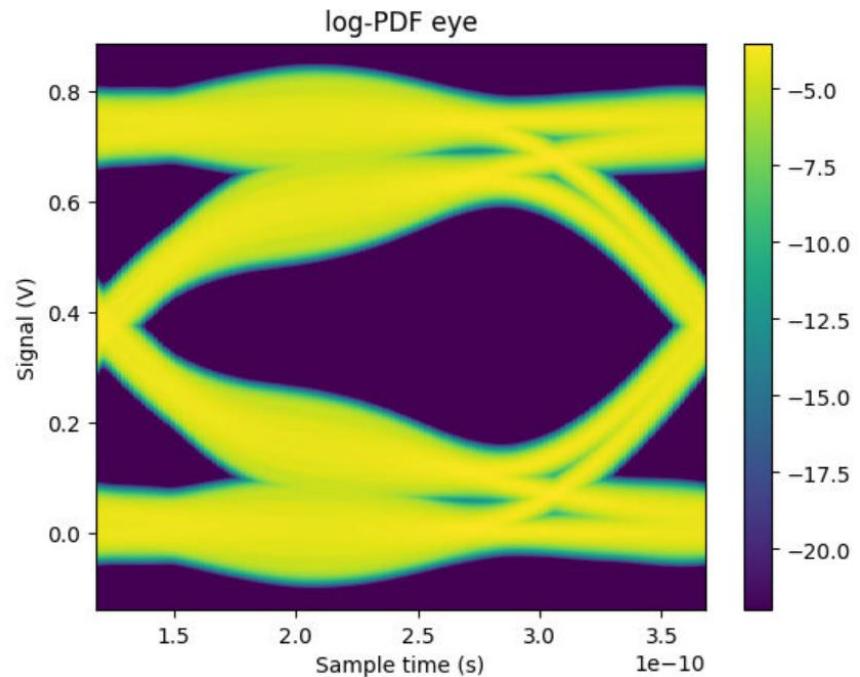
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 4.71\text{mV}$, $V_{sens,det} = 225\text{mV}$): 32% / 2.4%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 150\text{mV}$): 71.2% / 2.4%**

Keysight Results:

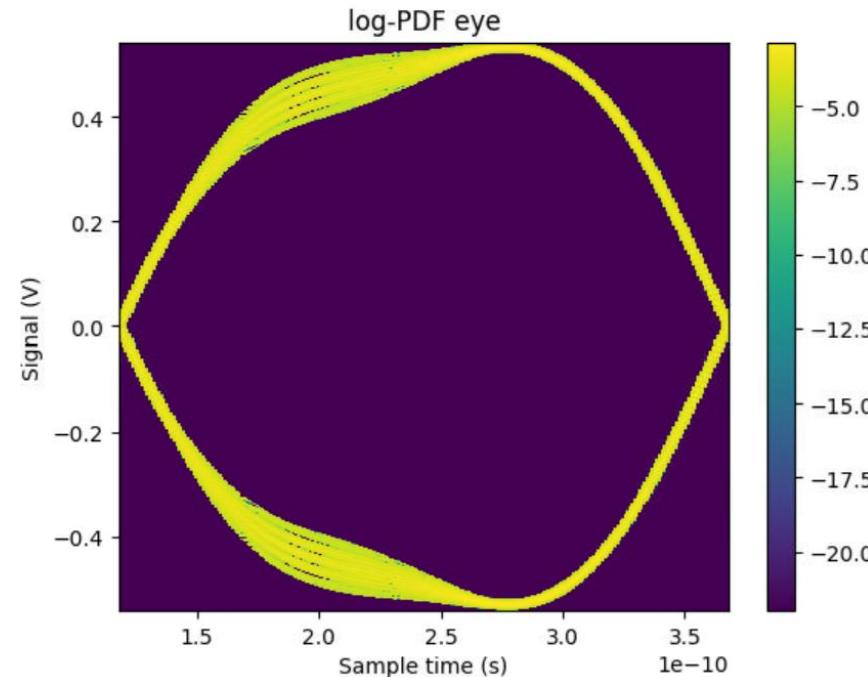
20%-80% risetime = 23% UI, Cpar = 800F



Worst Data Eye



Diff. Clock



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 4.71\text{mV}$, $V_{sens,det} = 225\text{mV}$): 43.6% / 2.4%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER ($\sigma_{rx,vn} = 3.14\text{mV}$, $V_{sens,det} = 150\text{mV}$): 71.6% / 2.4%**

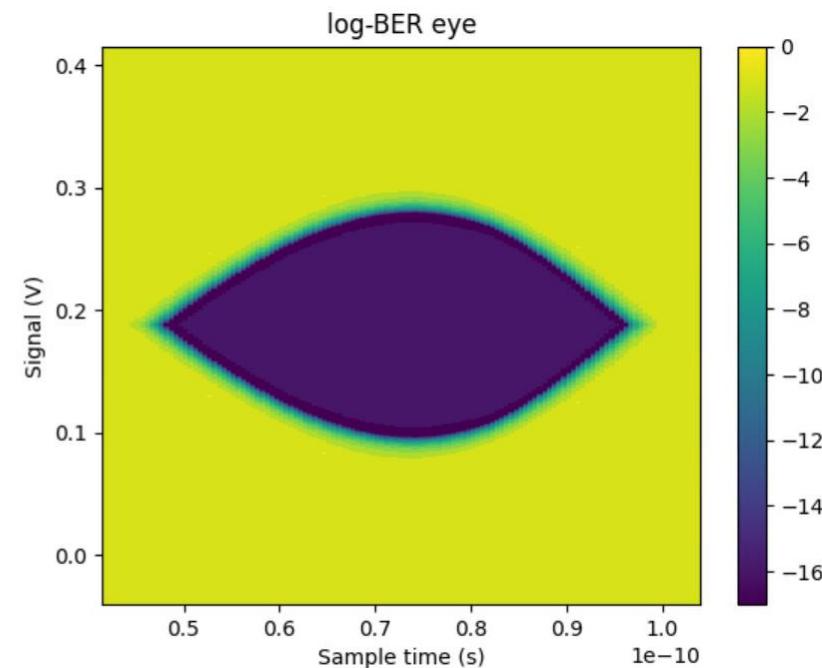
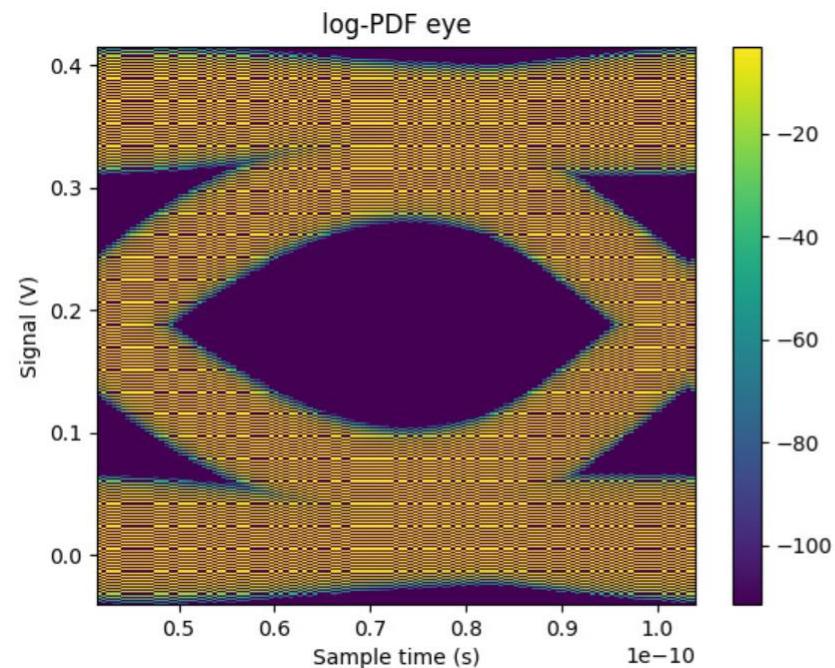
Prior Results

Setup: 16Gb/s Doubly Terminated

- By default, parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):
 - 20% - 80% rise time of 0.32UI
 - $R_{TX} = R_{RX} = 50\Omega$
 - 300fF lumped capacitance on TX/RX
 - VDDIO = 750mV
 - 75mV peak-to-peak RX sensitivity

Full Slice 25mm

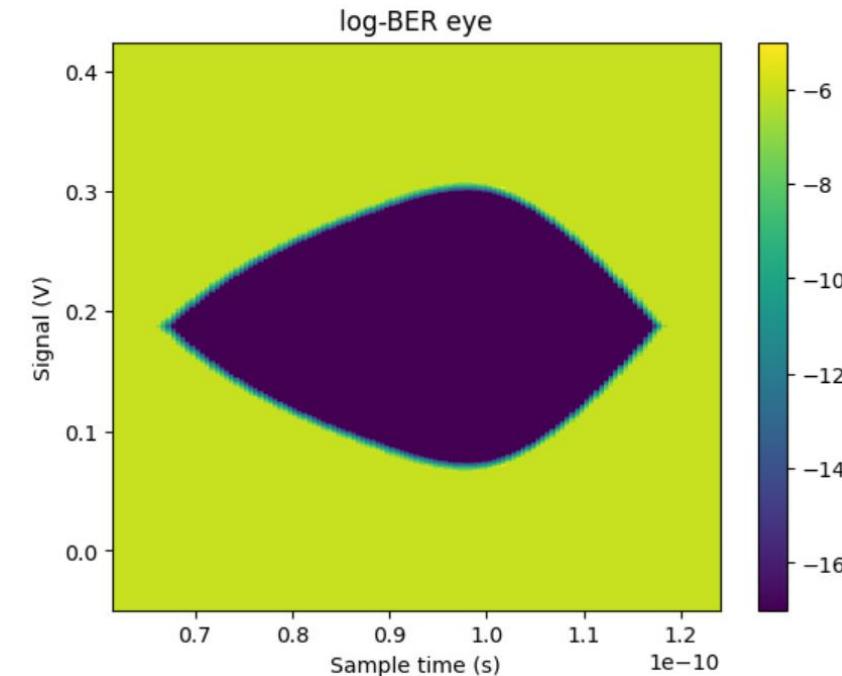
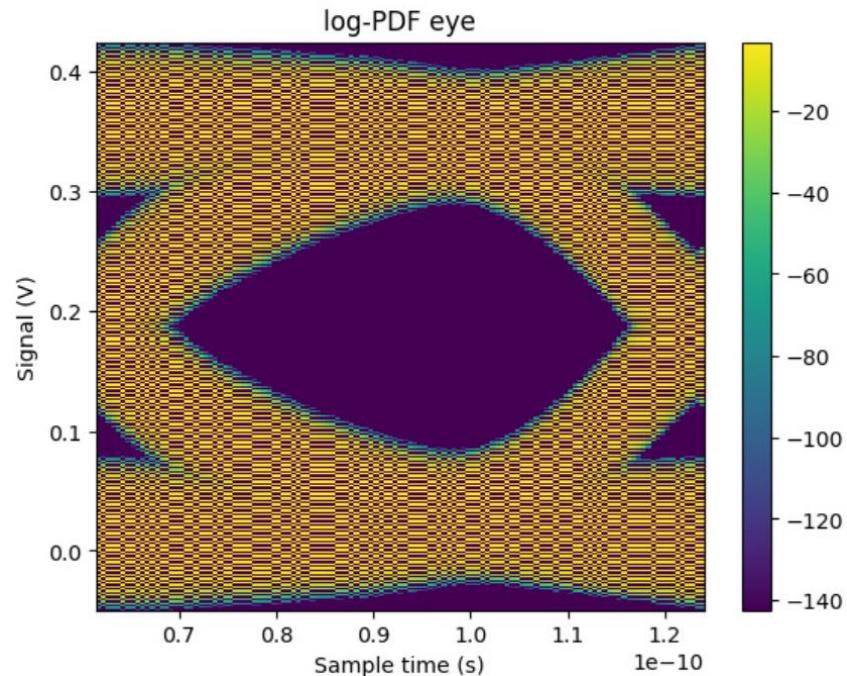
Full Slice 25mm Results



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 56.8% / 3.2%**

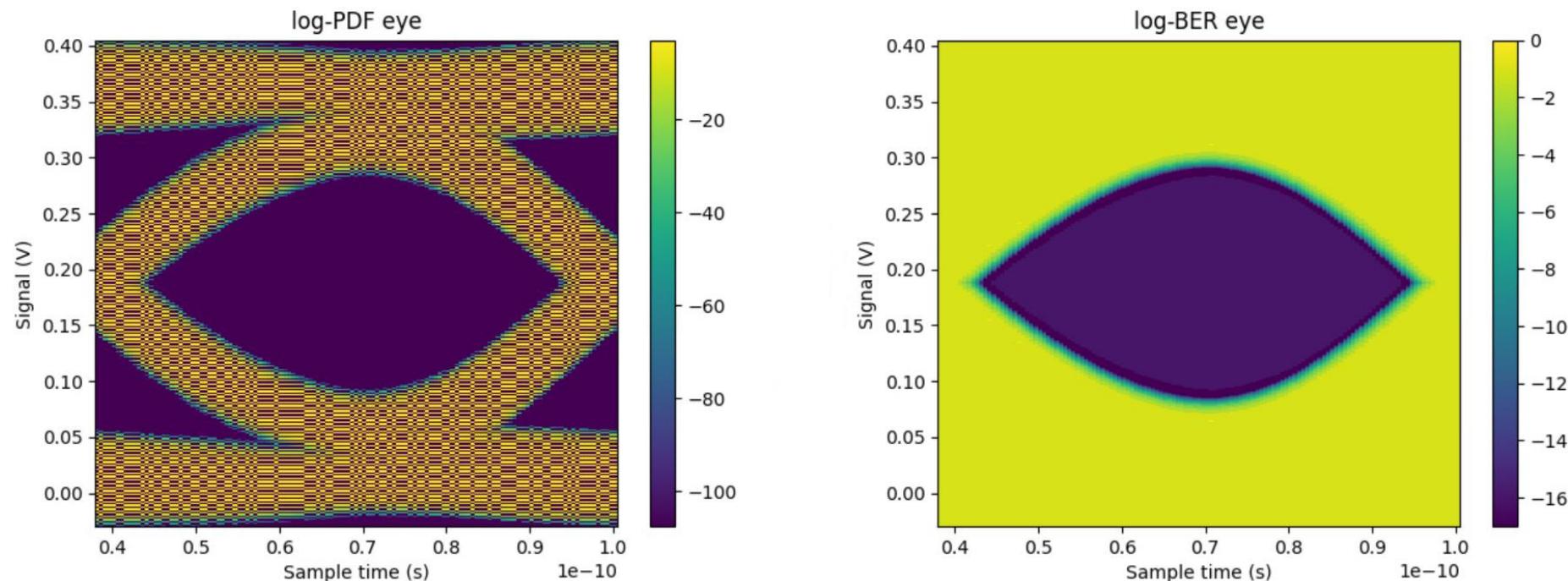
Full Slice 25mm Results:

20%-80% risetime = 23% UI



- **Worst line timing margin @ 1e-15 BER: 63.4%**

Full Slice 25mm Results: Cpar = 200fF

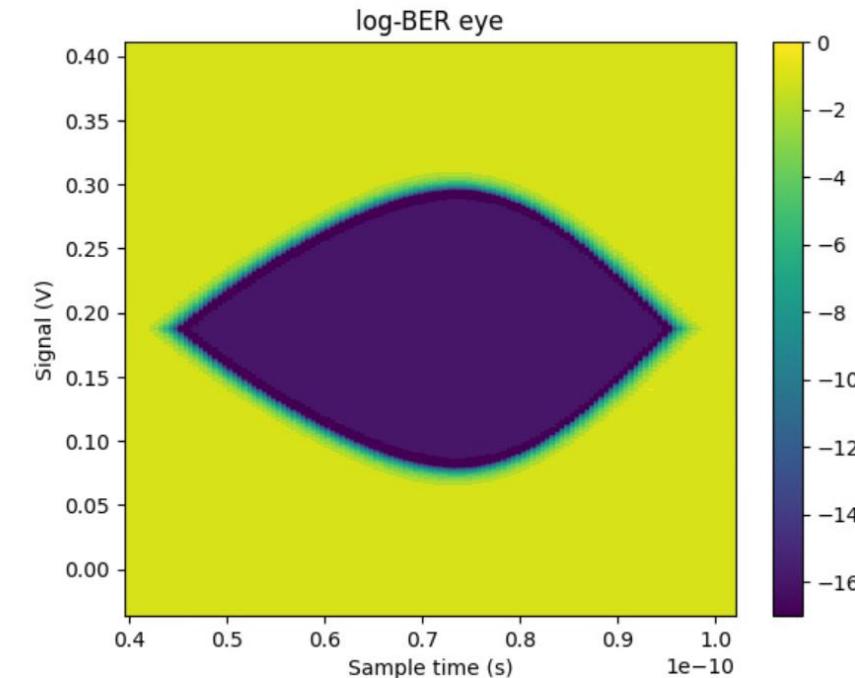
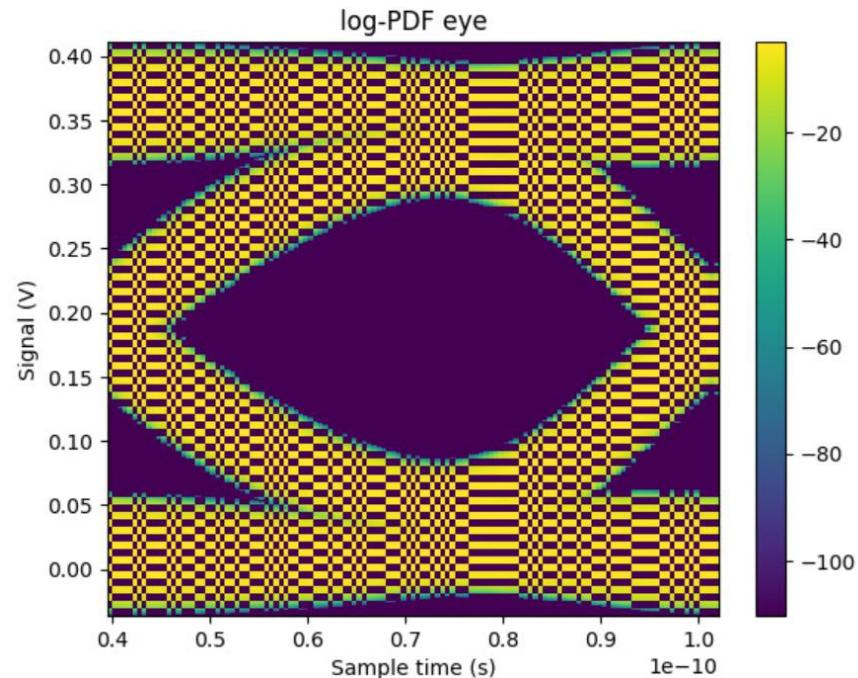


- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **63.2% / 3.2%**

Full Slice 25mm Results:



20%-80% risetime = 23% UI, Cpar = 250fF

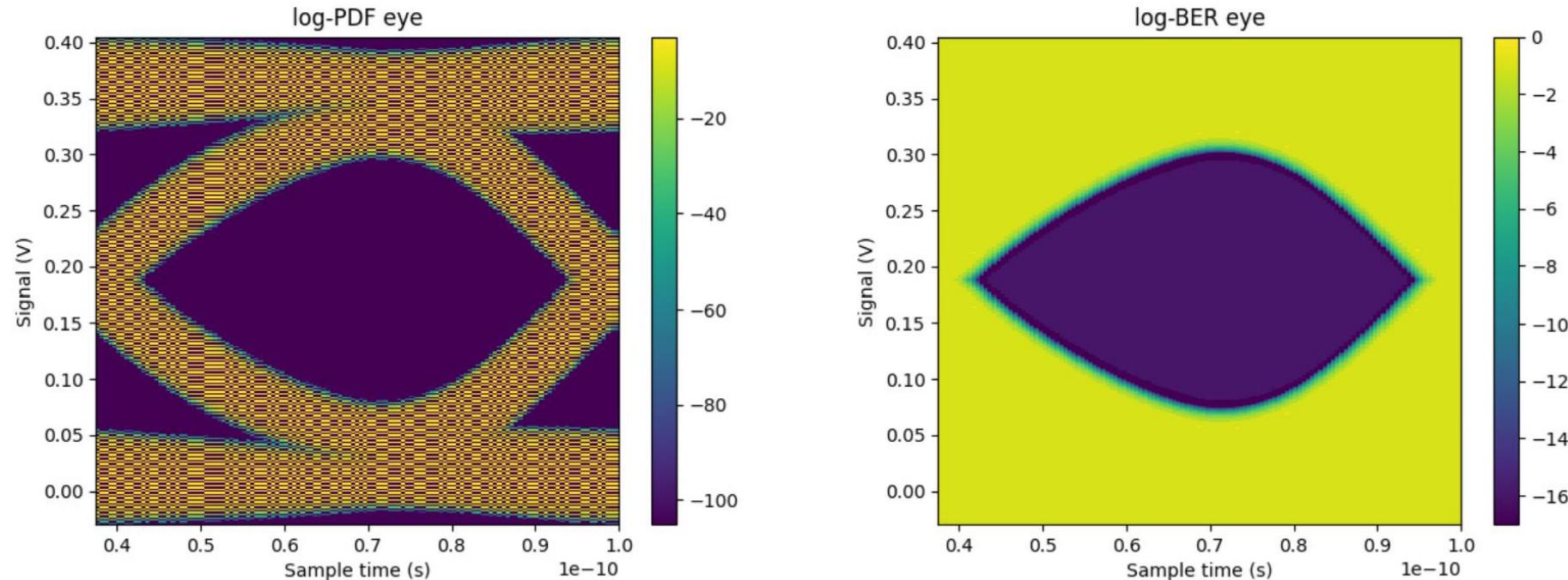


- Worst line timing margin /crosstalk jitter @ 1e-15 BER: **62.4% / 3.2%**

Full Slice 25mm Results:



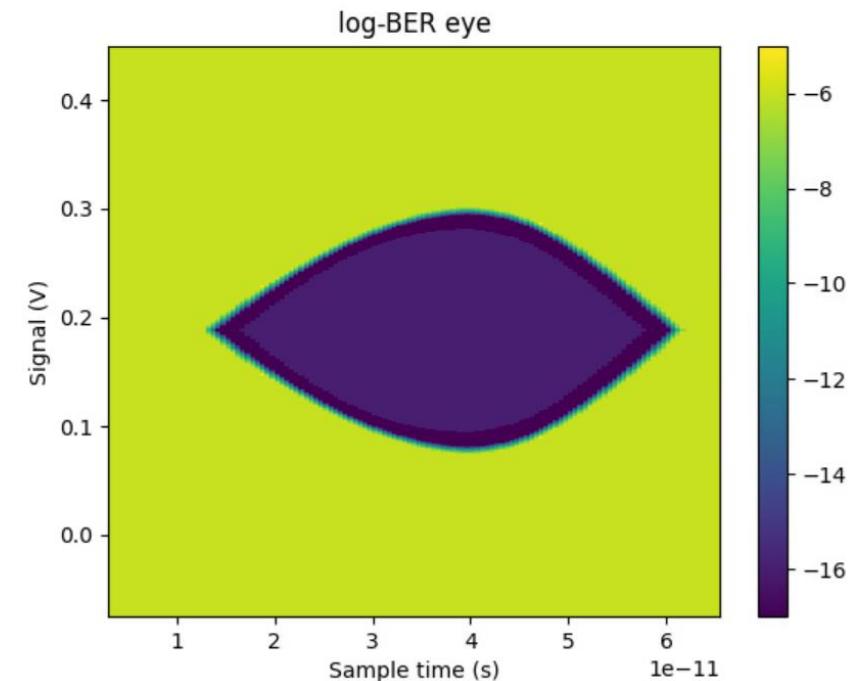
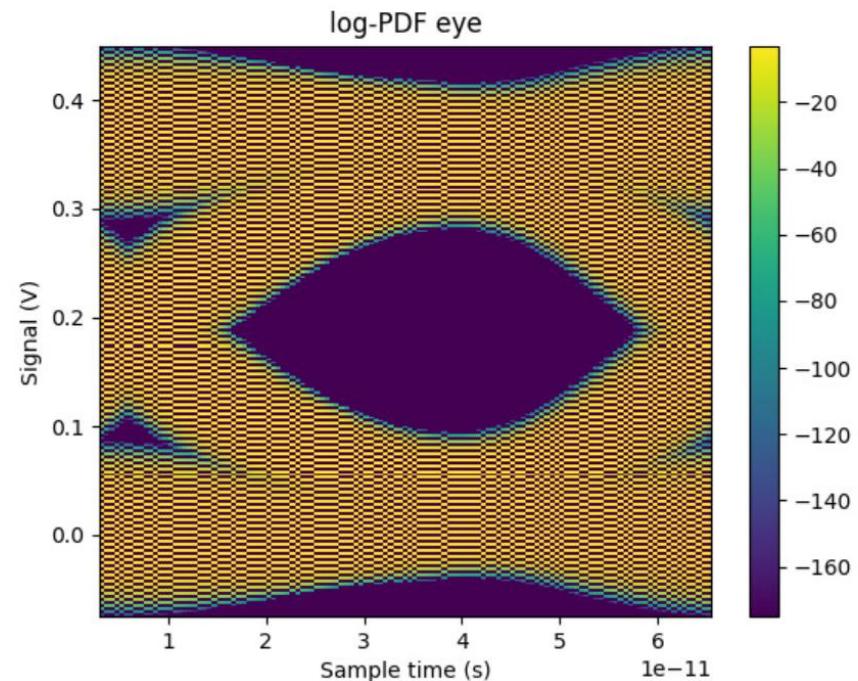
20%-80% risetime = 23% UI, Cpar = 200fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 65.6% / 3.2%**

Full Slice 10mm

Full Slice 10mm Results

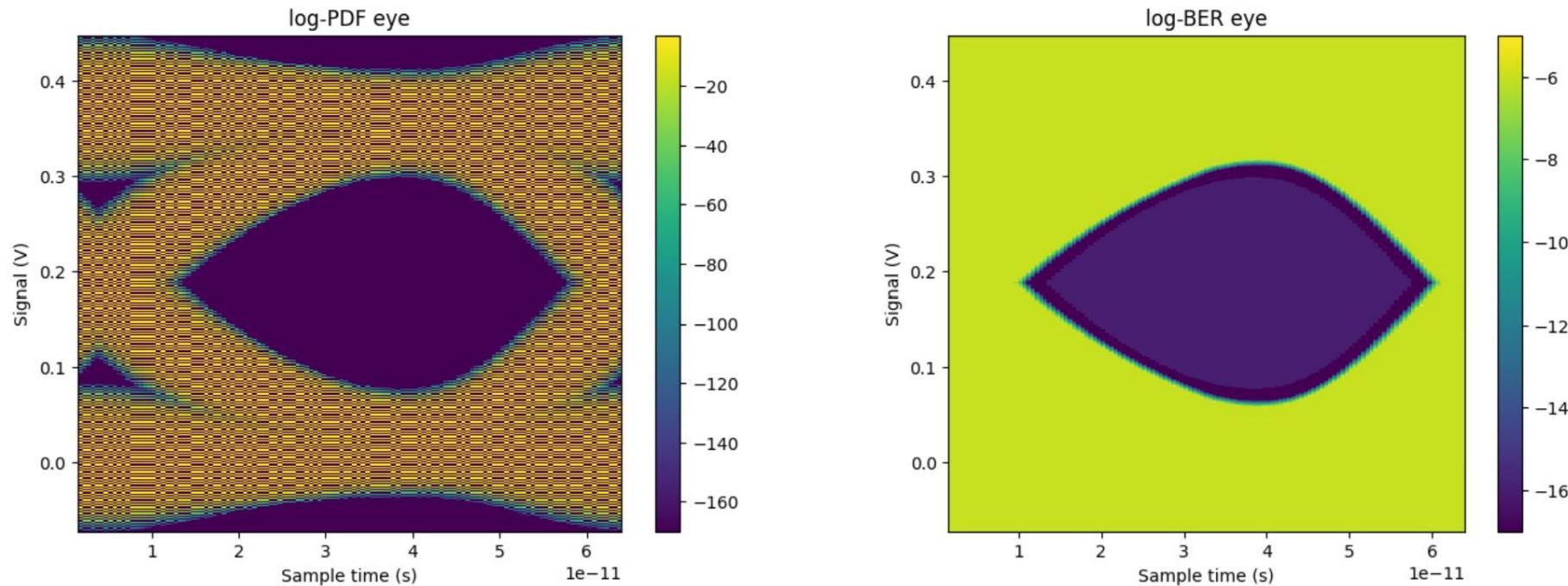


- Worst line timing margin / crosstalk jitter @ $1e-15$ BER: **56.8% / 3.2%**

Full Slice 10mm Results:

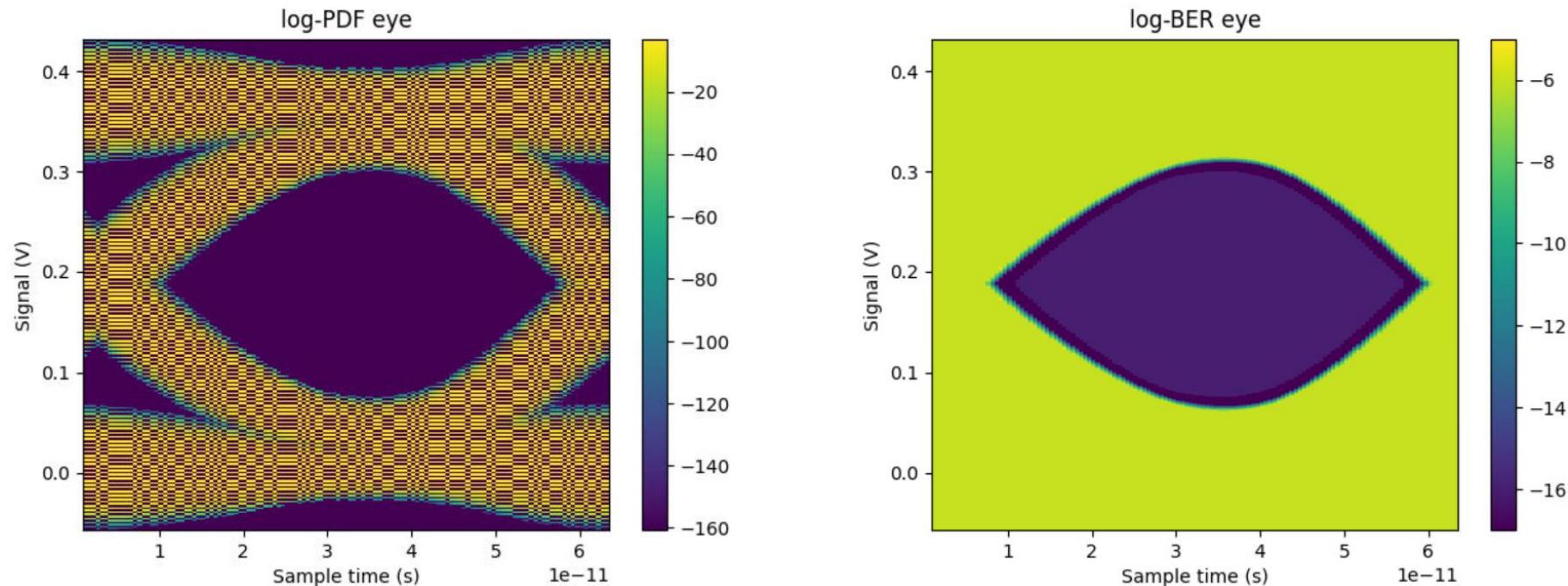


20%-80% risetime = 23% UI, Cpar = 250fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 63.2% / 2.4%**

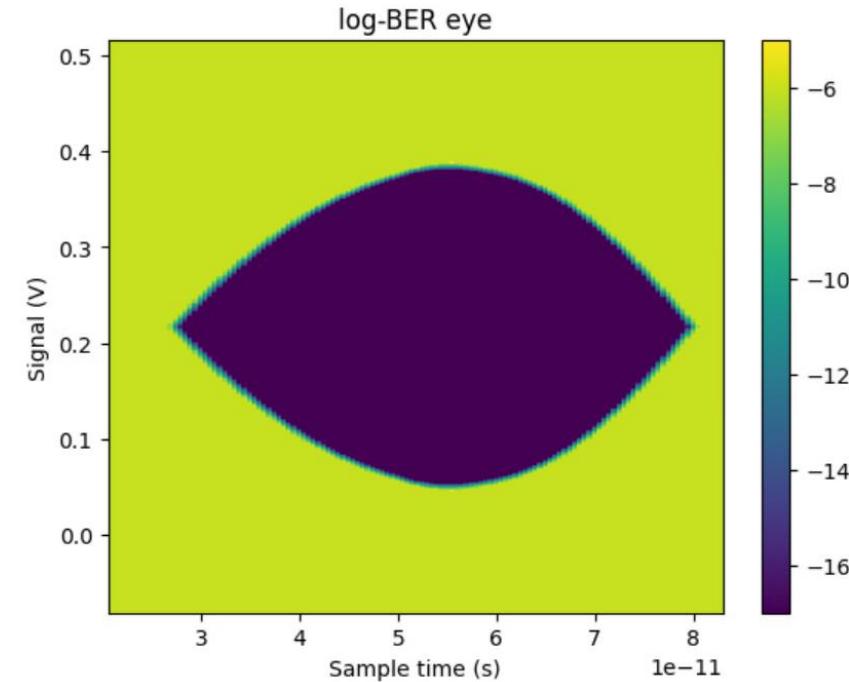
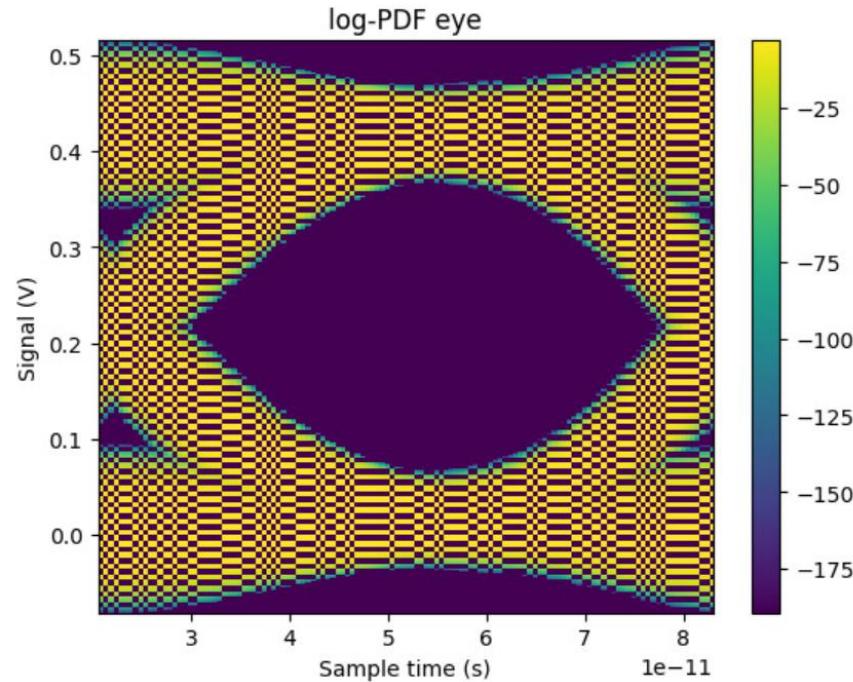
Full Slice 10mm Results: Cpar = 200fF



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **64.8% / 2.4%**

Full Slice 10mm Results:

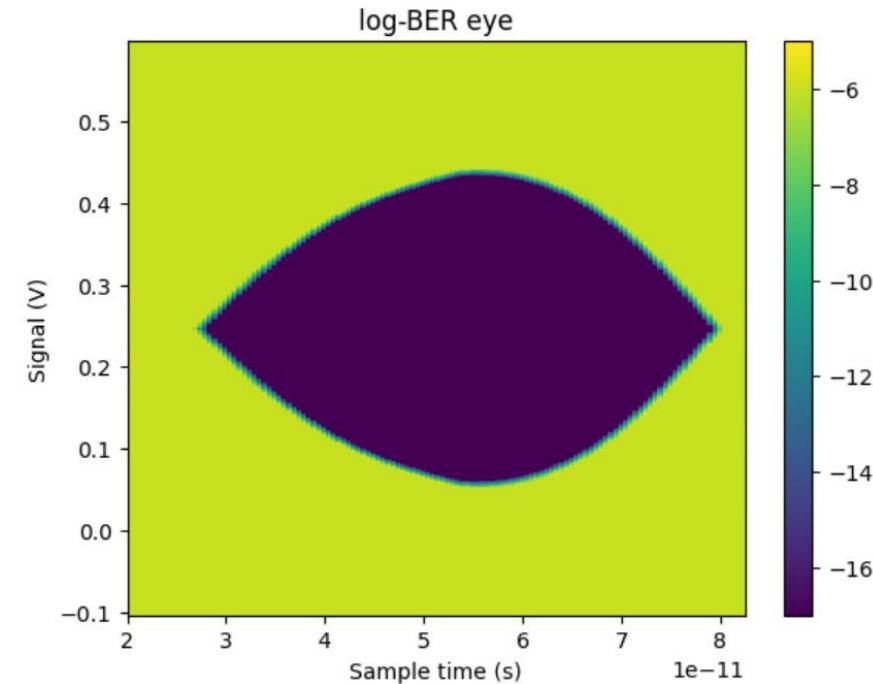
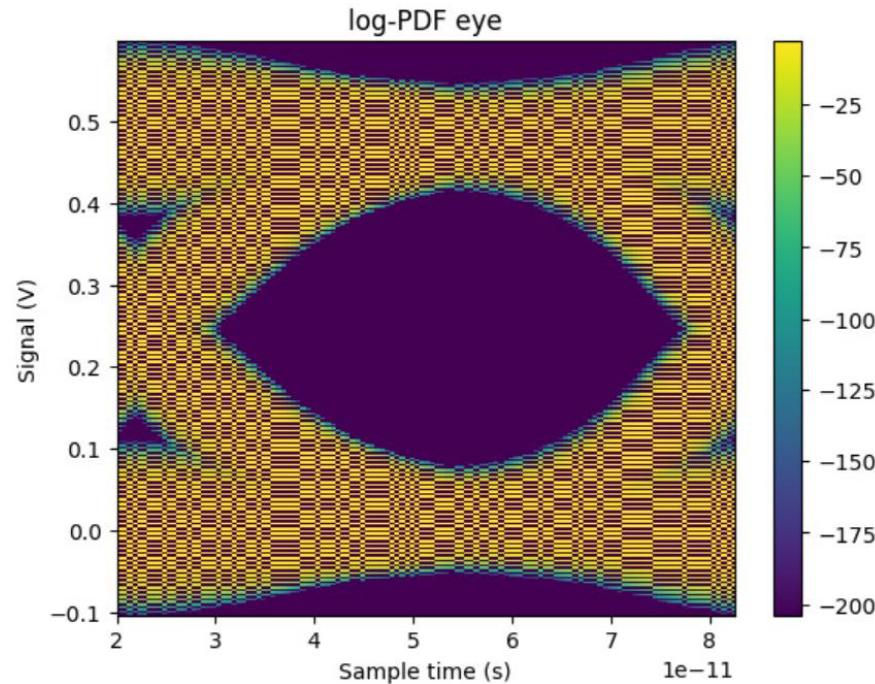
R_{tx} = 43Ω, R_{rx} = 59Ω, C_{par} = 200fF



- Worst line timing margin @ 1e-15 BER: 72%

Full Slice 10mm Results:

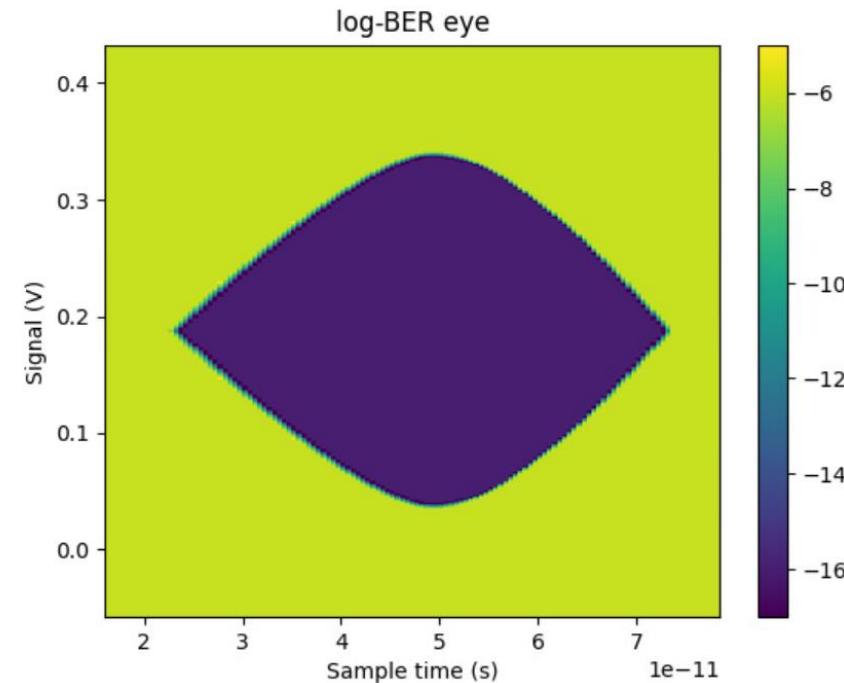
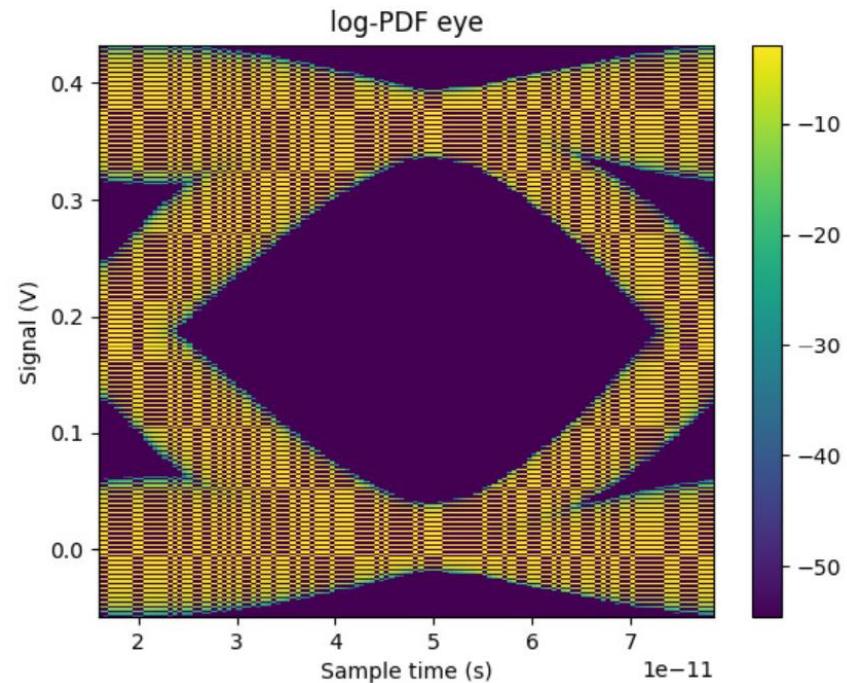
R_{tx} = 36Ω, R_{rx} = 69Ω, C_{par} = 200fF



- Worst line timing margin @ 1e-15 BER: 72.8%

Full Slice 2mm

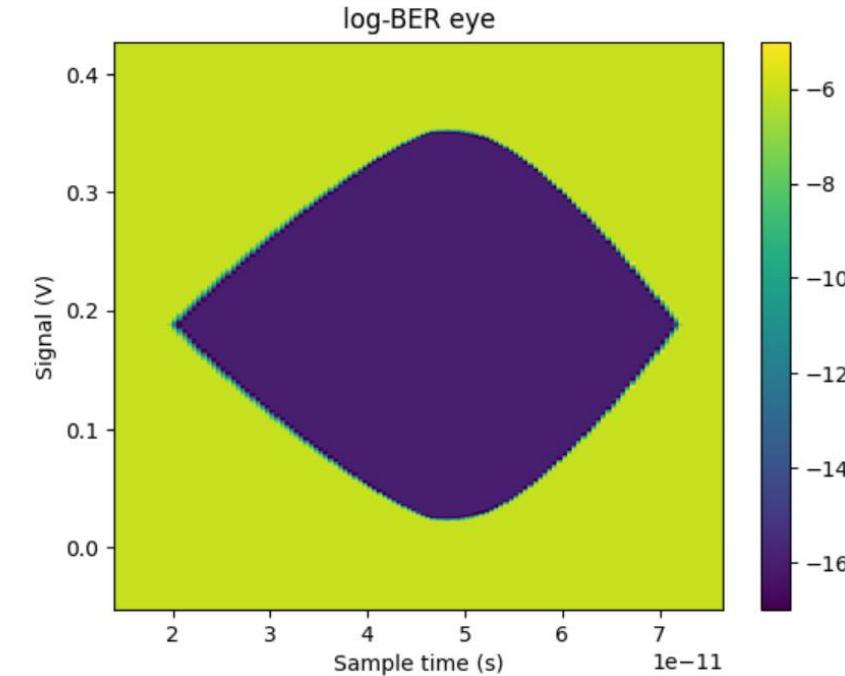
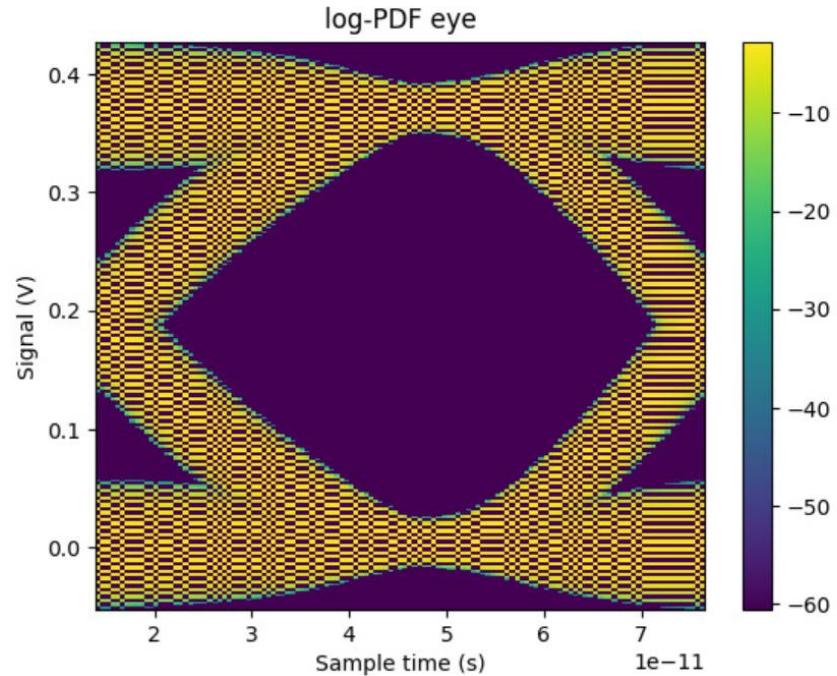
Full Slice 2mm Results



- Worst line timing margin / crosstalk jitter @ $1e-15$ BER: **64.8% / 4.8%**

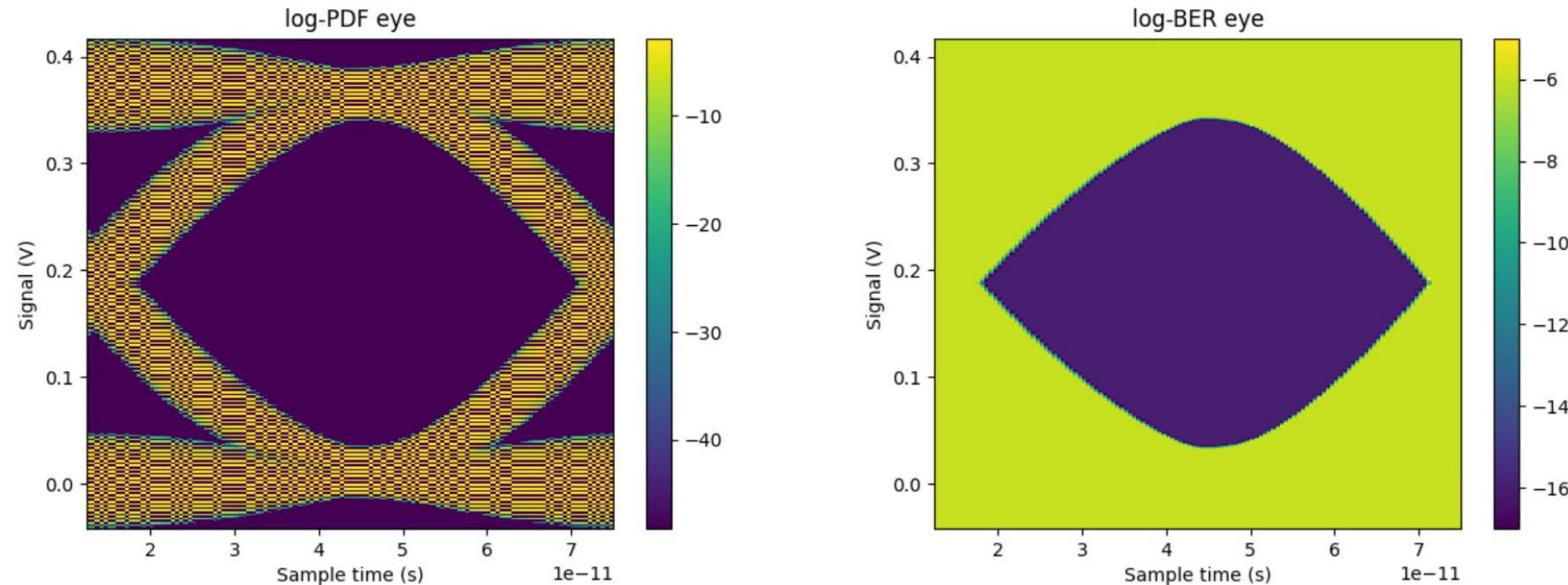
Full Slice 2mm Results:

20%-80% risetime = 23% UI, Cpar = 250fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 68.8% / 4%**

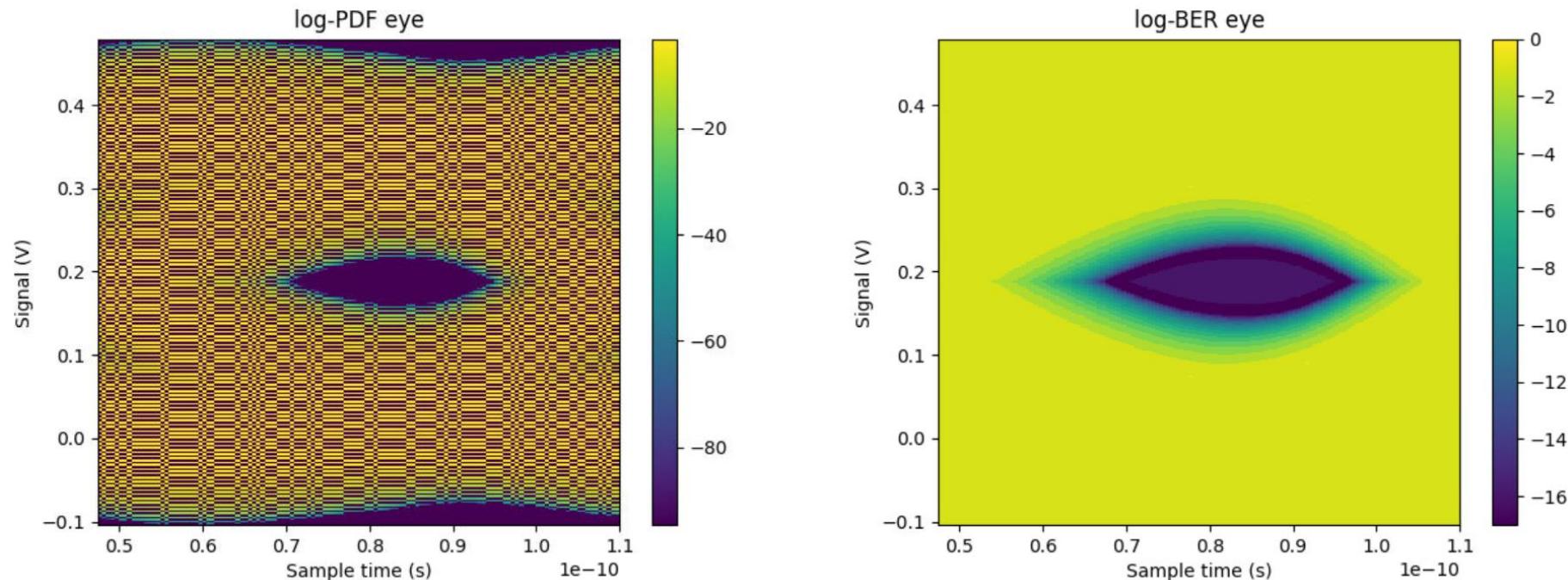
Full Slice 2mm Results: Cpar = 200fF



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: 70.4% / 2.4%

ARM Layer A 20mm

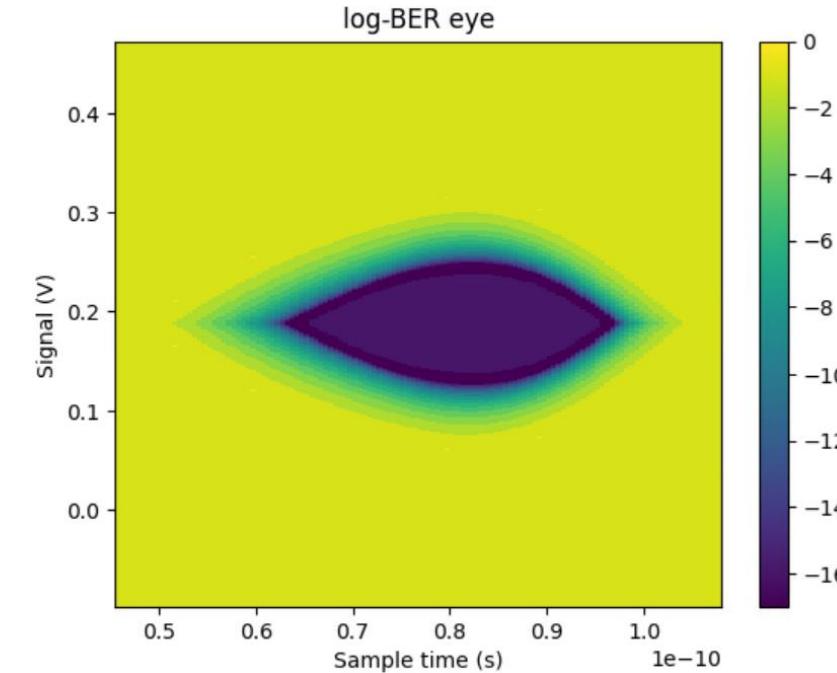
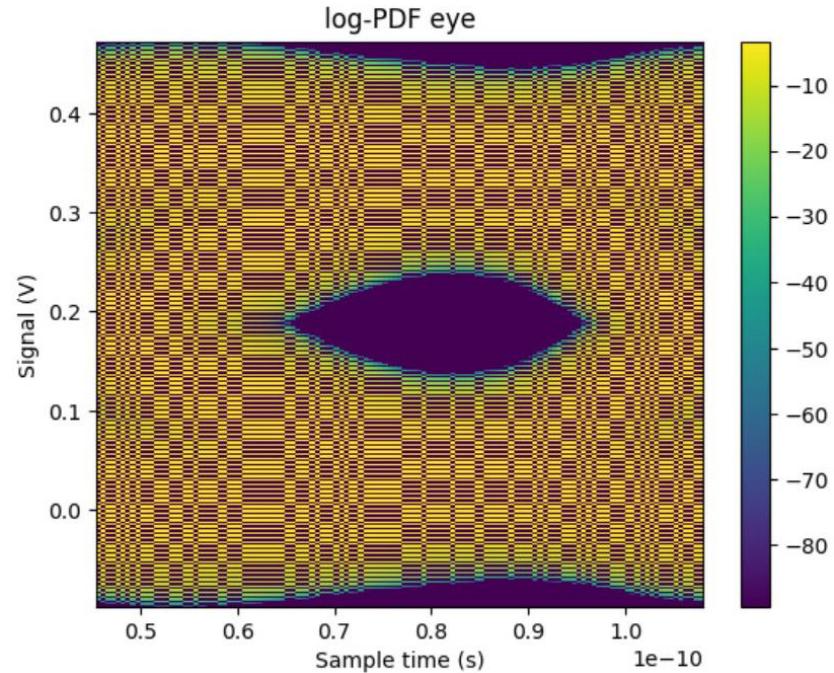
ARM Layer A Results



- **Worst line timing margin / crosstalk jitter @ $1e-15$ BER: 17.6% / 12.8%**

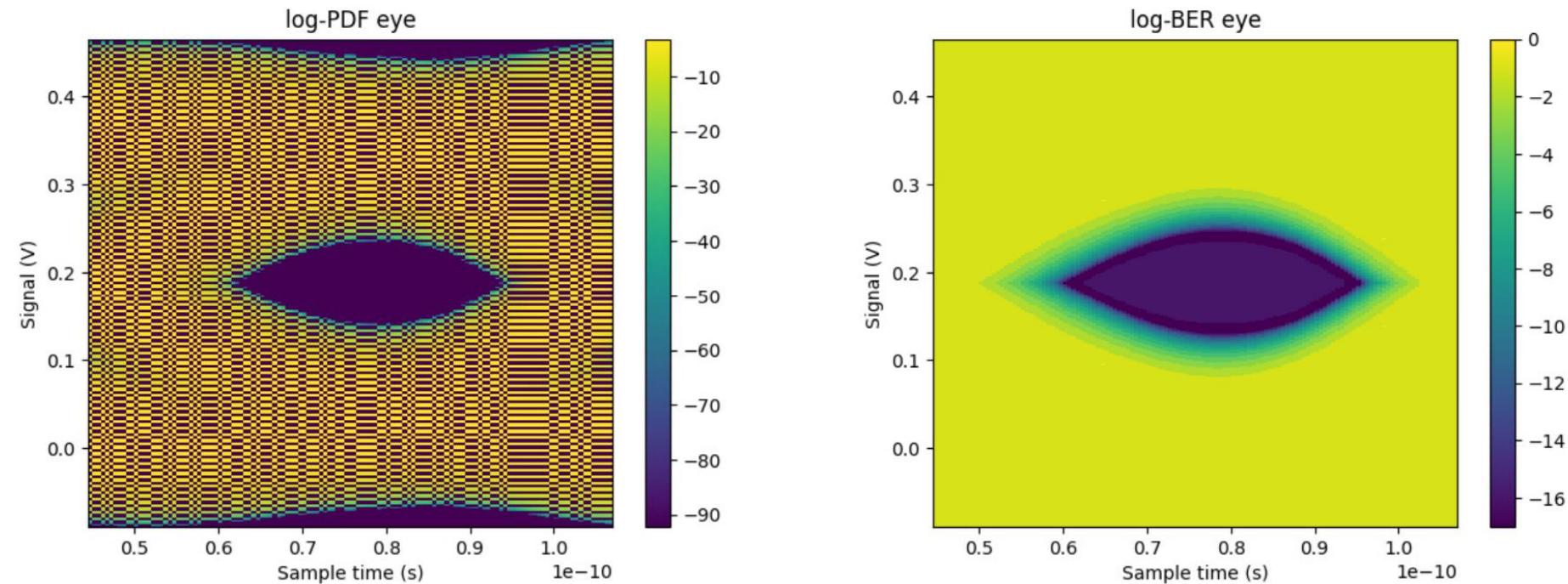
ARM Layer A Results:

20%-80% risetime = 23% UI, Cpar = 250fF



- Worst line timing margin /crosstalk jitter @ 1e-15 BER: **33.6% / 12%**

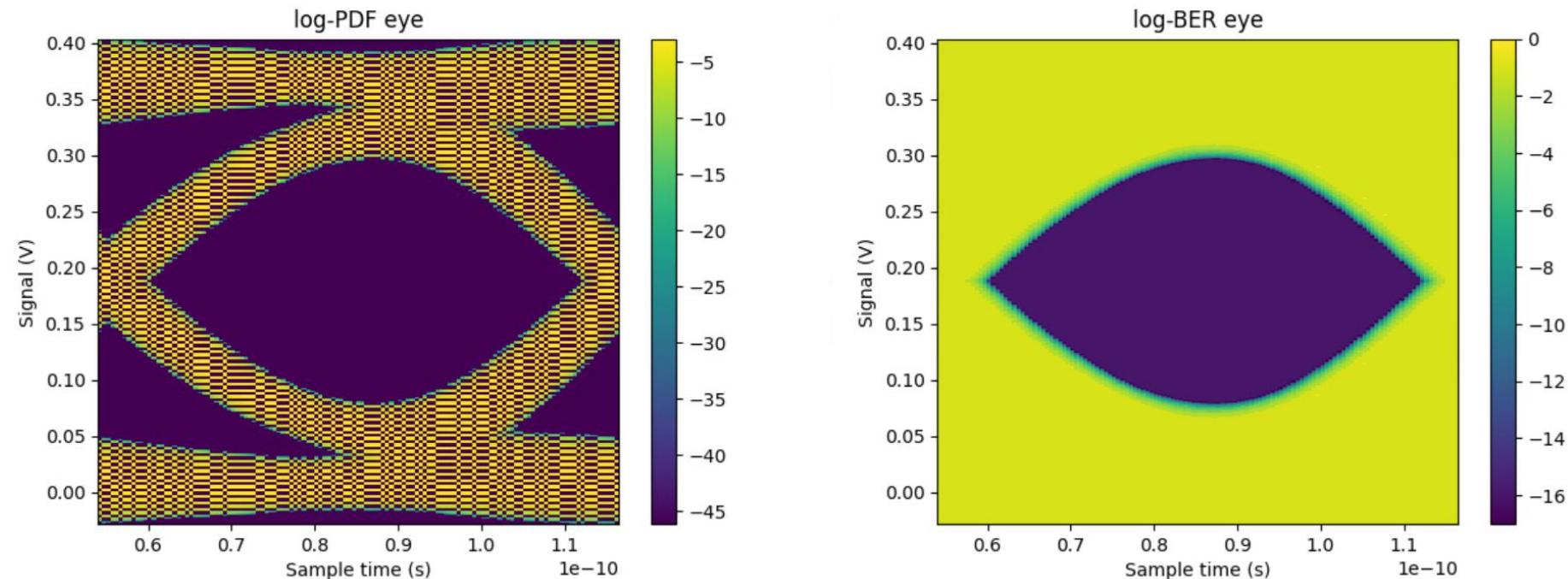
ARM Layer A Results: Cpar = 200fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 34.4% / 12.8%**

ARM Layer B 20mm

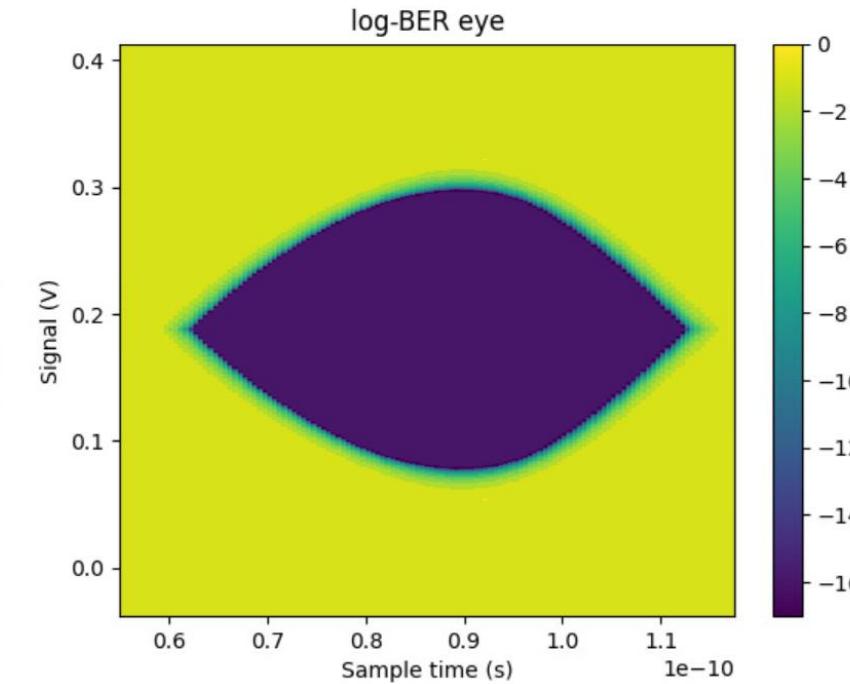
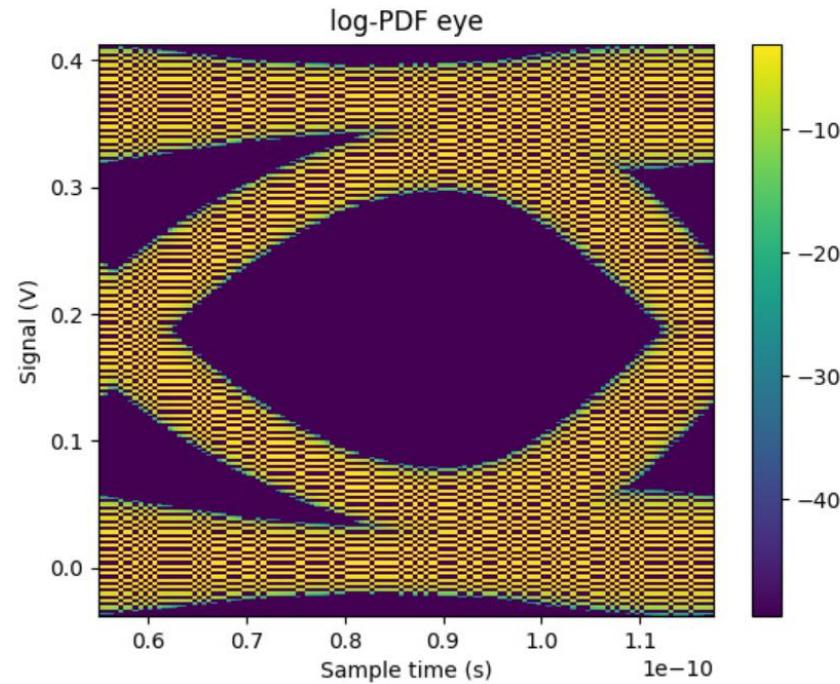
ARM Layer B Results: Cpar = 200fF



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **64.8% / 3.2%**

ARM Layer B Results:

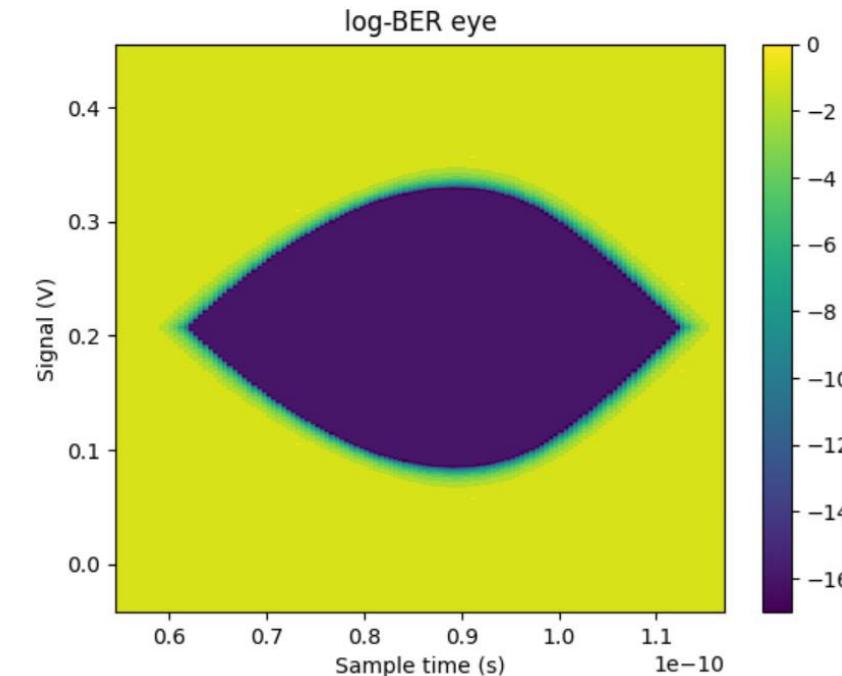
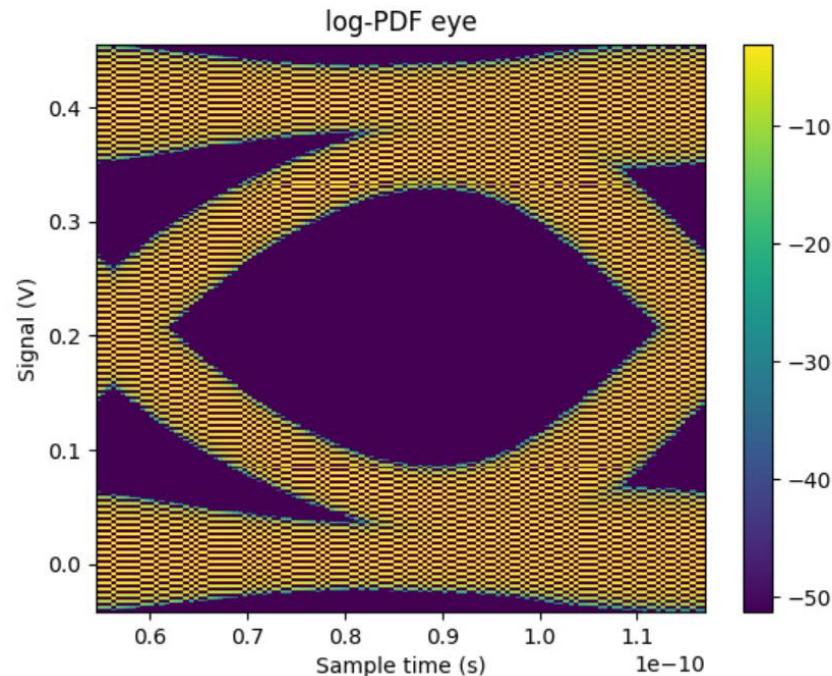
20%-80% risetime = 23% UI, Cpar = 250fF



- Worst line timing margin / crosstalk jitter @ $1e-15$ BER: **64% / 3.2%**

ARM Layer B Results:

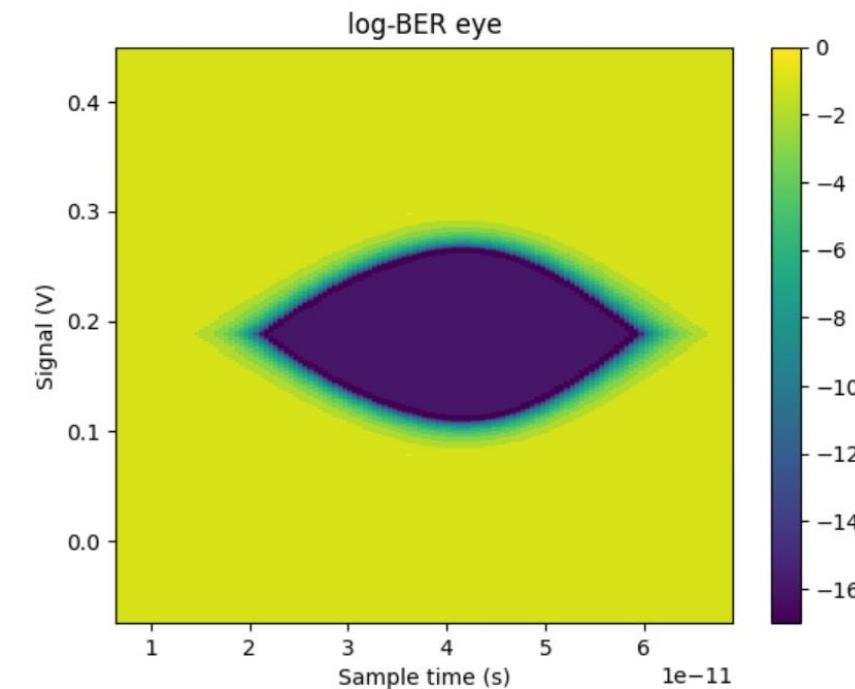
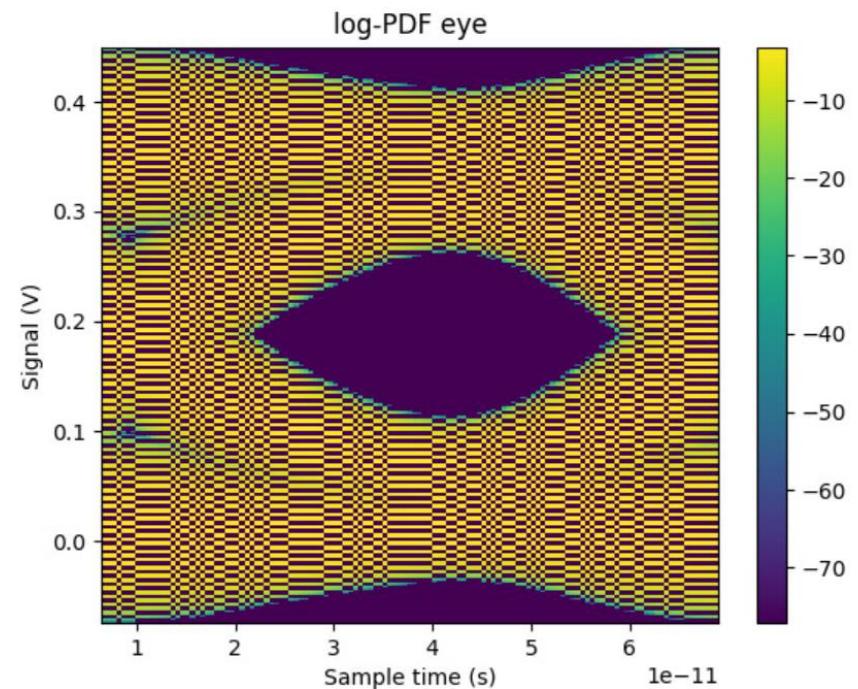
20%-80% risetime = 23% UI, Cpar = 250fF, $R_{TX} = 44\Omega$, $R_{RX} = 54\Omega$



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **65.6% / 3.2%**

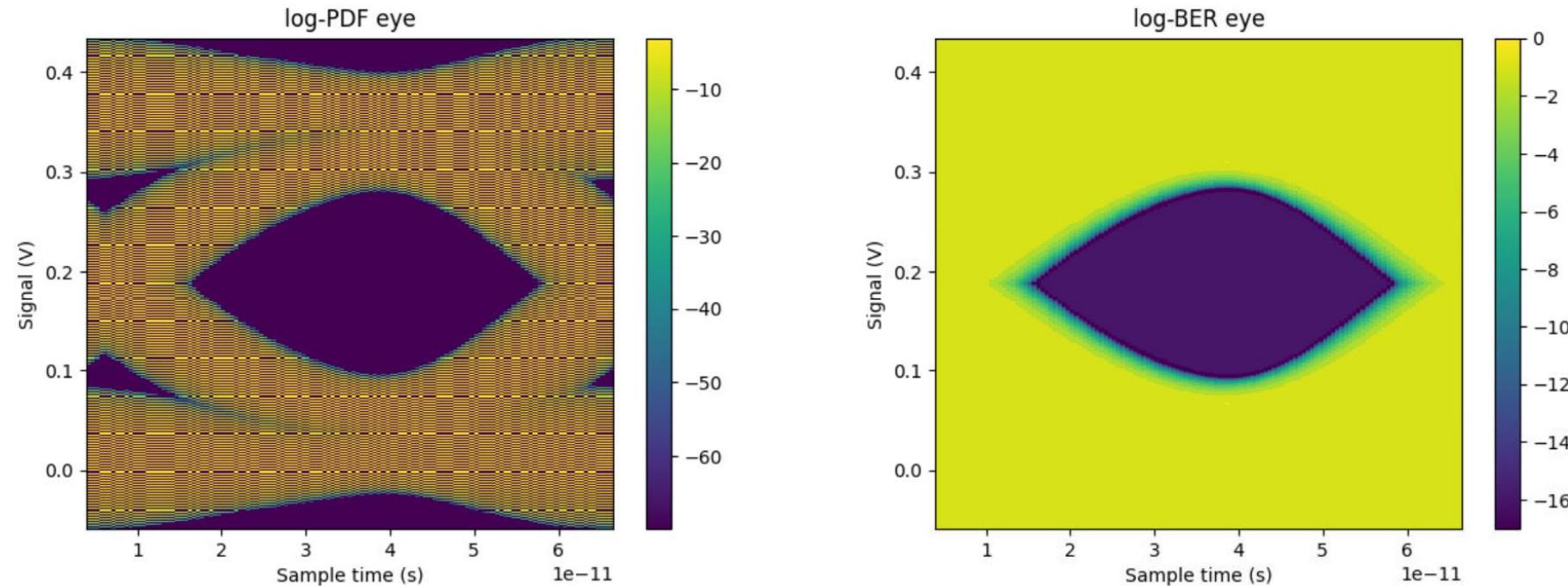
ARM Layer D 20mm

ARM Layer D Results



- **Worst line timing margin / crosstalk jitter @ $1e-15$ BER: 42.4% / 5.6%**

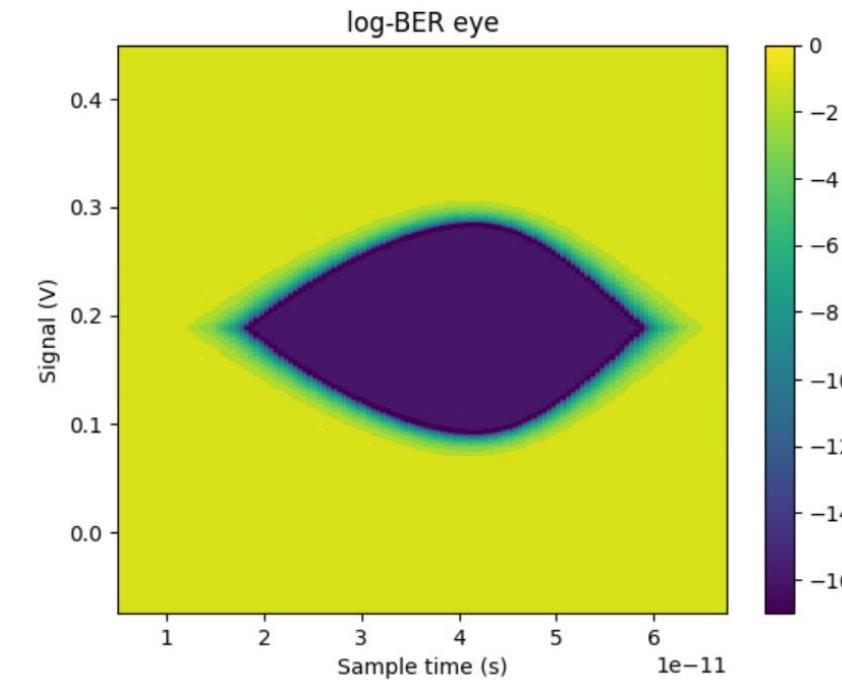
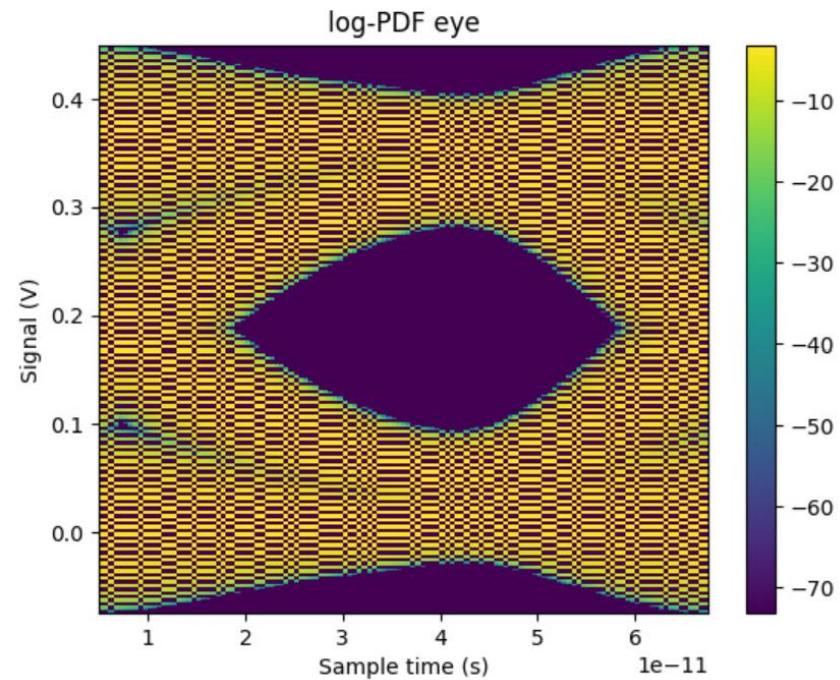
ARM Layer D Results: Cpar = 200fF



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **50.4% / 4.8%**

ARM Layer D Results:

20%-80% risetime = 23% UI, Cpar = 250fF

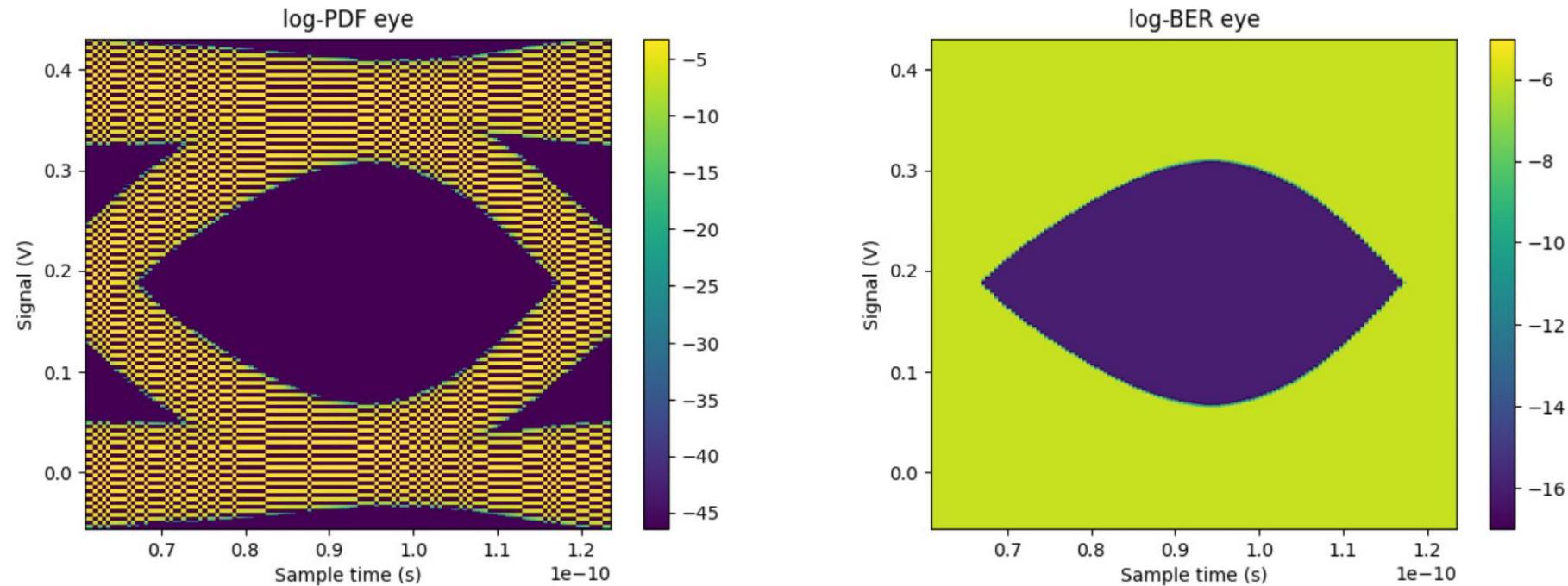


- **Worst line timing margin / crosstalk jitter @ $1e-15$ BER: 48.8% / 5.6%**



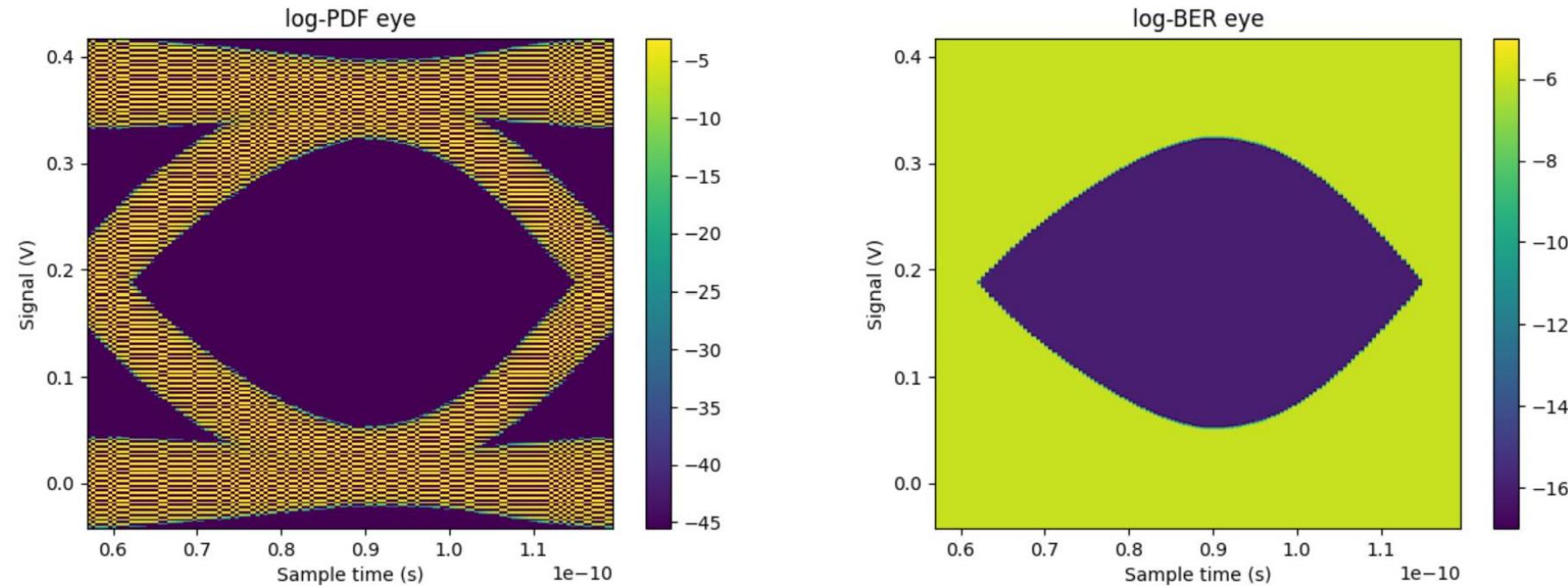
Keysight

Keysight Results



- **Worst line timing margin / crosstalk jitter @ $1e-15$ BER: 64.8% / 4.8%**

Keysight: Cpar = 200fF



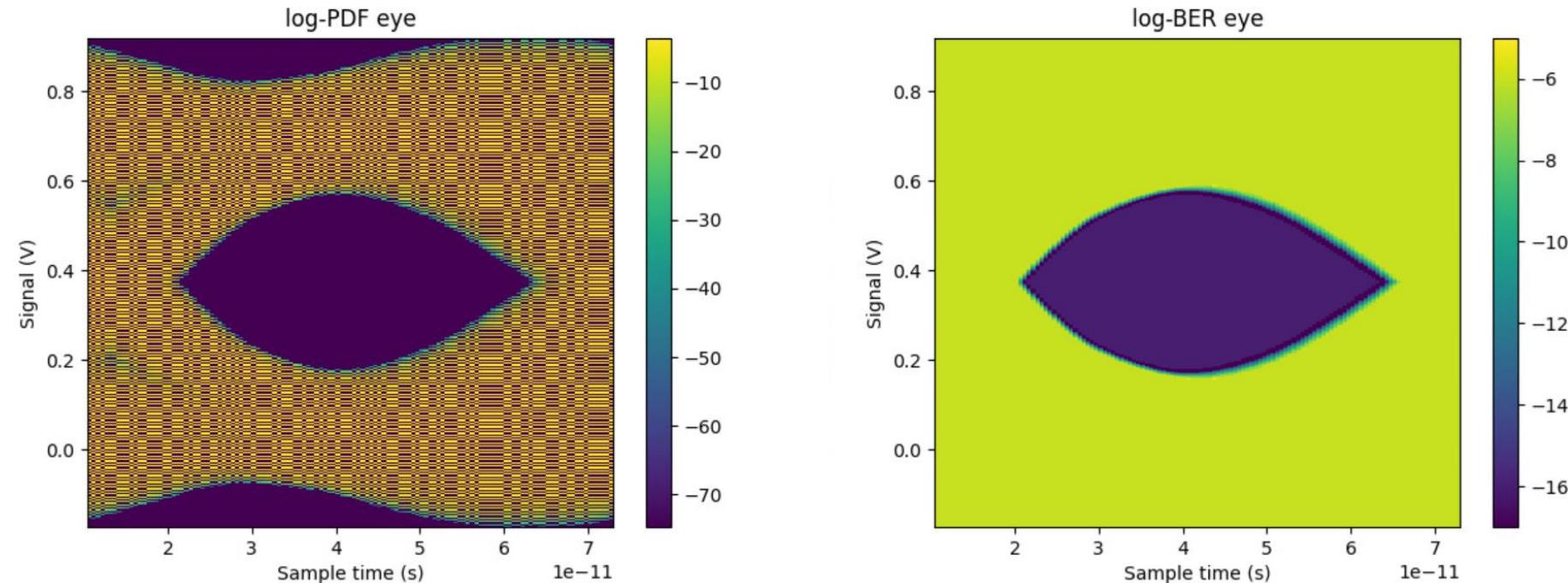
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 70.4% / 3.2%**

Setup: 16Gb/s Source Terminated

- Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):
 - 20% - 80% rise time of 0.32UI
 - $R_{TX} = 50\Omega$ (likely worst case; will check other values later)
 - 300fF lumped capacitance on TX/RX
 - $VDDIO = 750mV$
 - 150mV peak-to-peak RX sensitivity

Full Slice 2mm

Full Slice 2mm Results: Cpar = 200fF



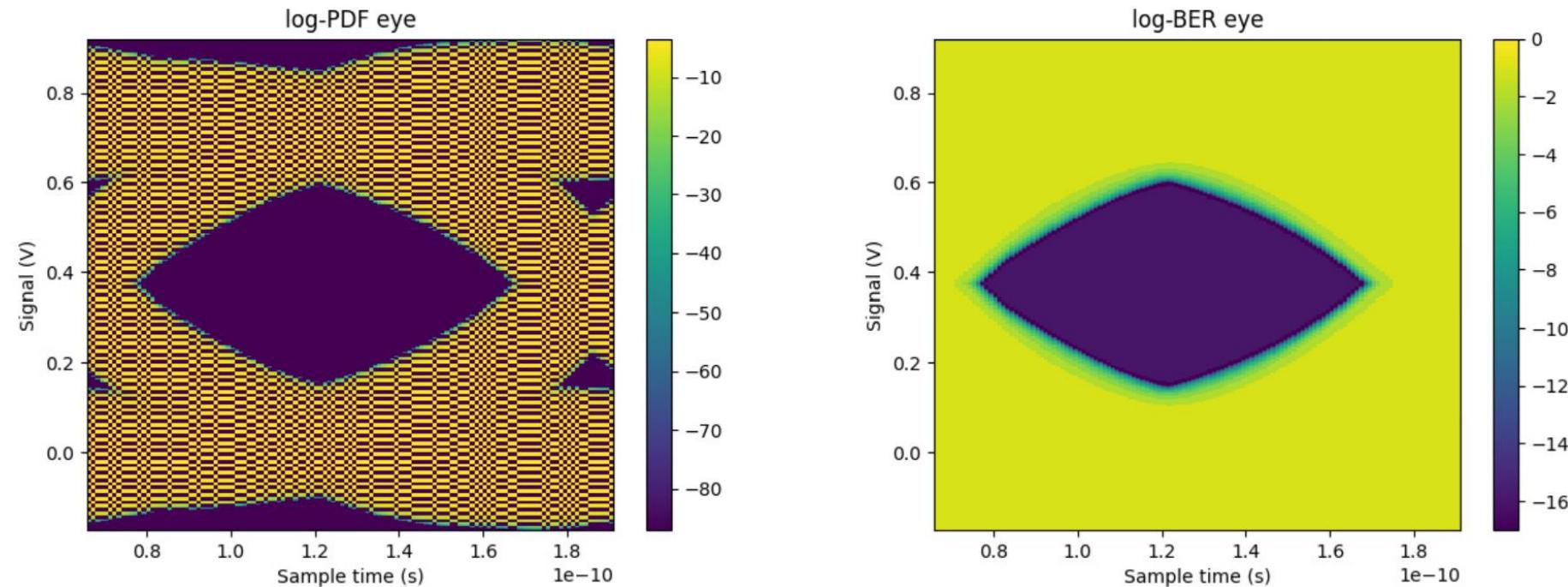
- Worst line timing margin @ 1e-15 BER: **54.4% / 6.4%**
- Worst line timing margin / crosstalk jitter @ 1e-15 BER (75mV sensitivity): **61.6% / 6.4%**

Setup (4): 8Gb/s Source Terminated

- Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):
 - 20% - 80% rise time of 0.32UI
 - $R_{TX} = 50\Omega$ (likely worst-case; will check other values later)
 - 600fF lumped capacitance on TX/RX
 - $VDDIO = 750mV$
 - 150mV peak-to-peak RX sensitivity

Full Slice 10mm

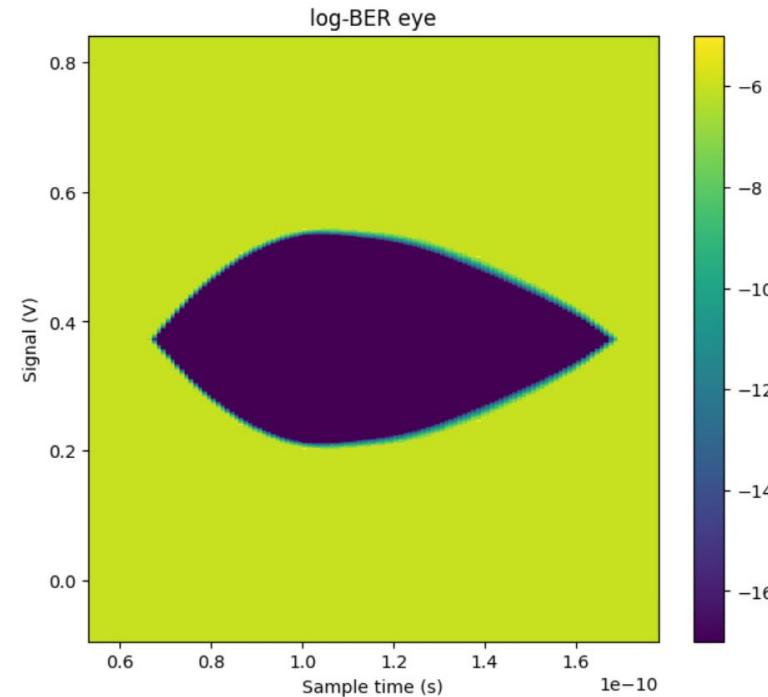
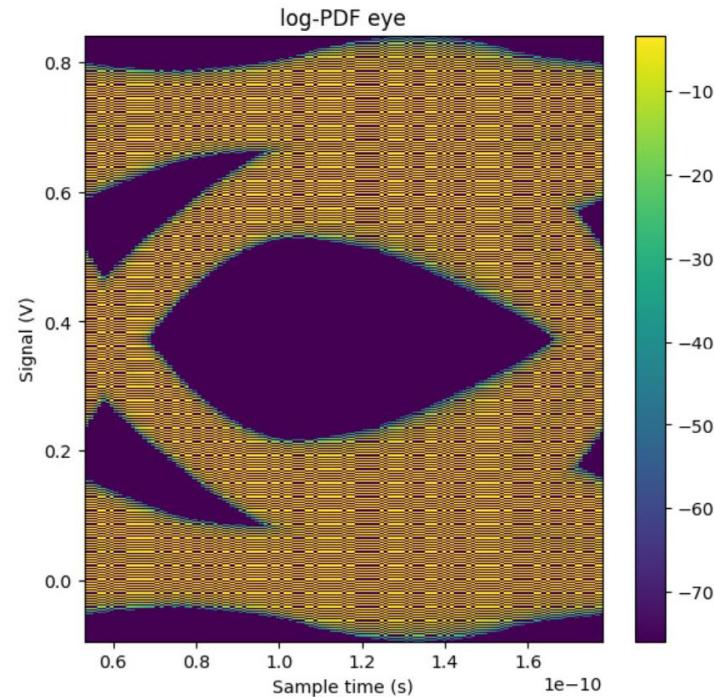
Full Slice 10mm Results: Cpar = 400fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 56.8% / 6.4%**
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER (75mV sensitivity): 65.6% / 6.4%**

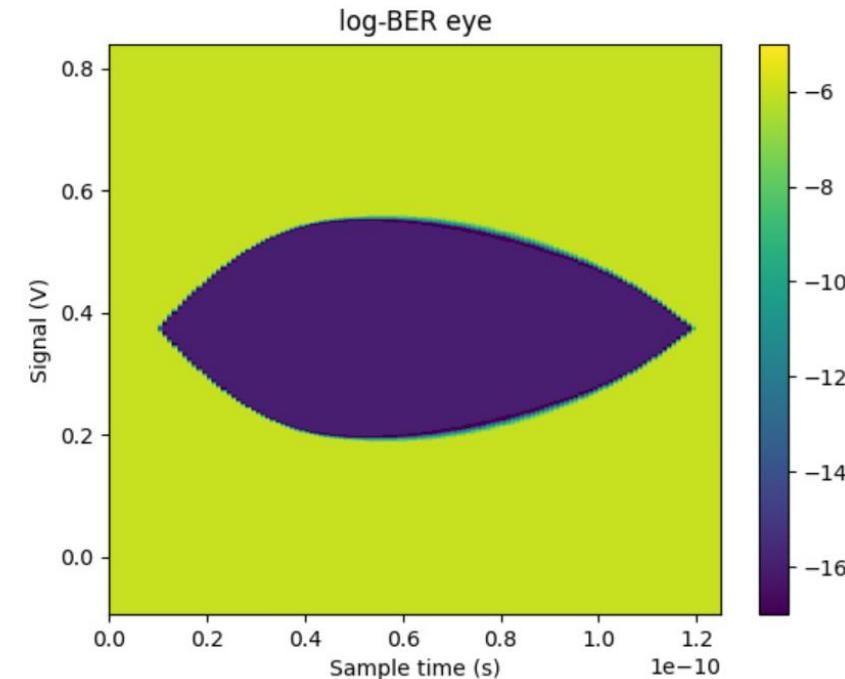
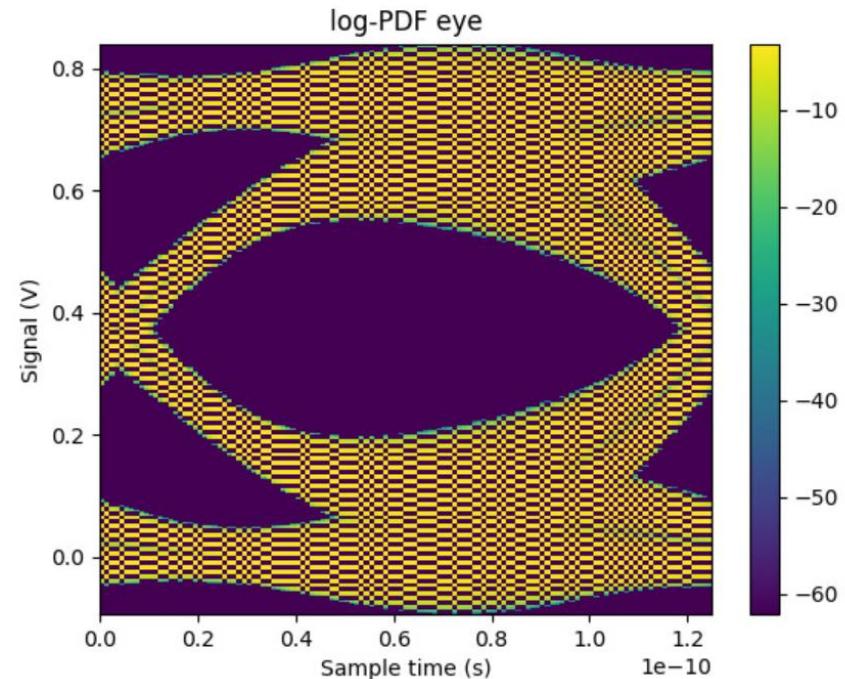
Full Slice 2mm

Full Slice 2mm Results



- Worst line timing margin @ $1e-15$ BER: **57.6%**

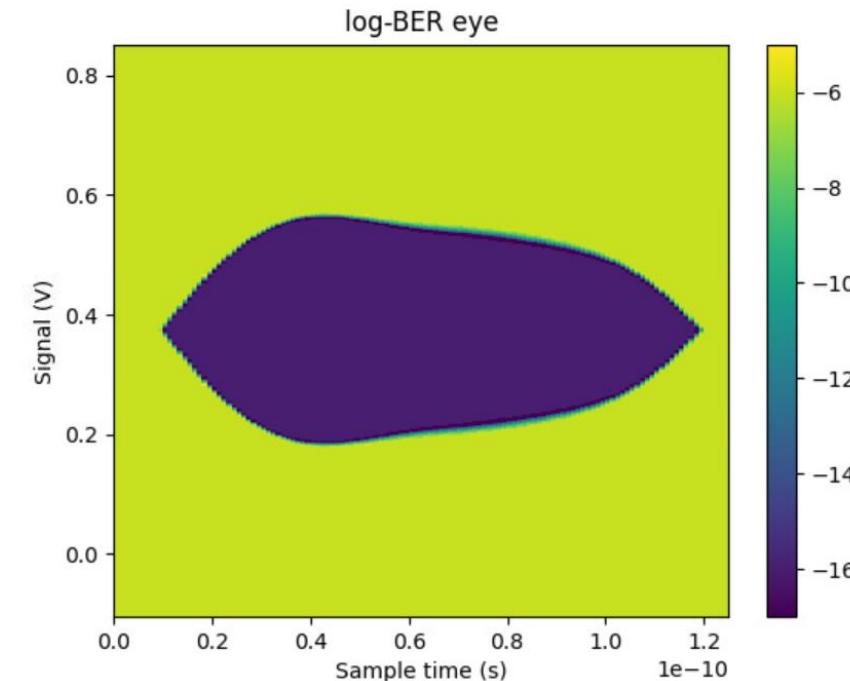
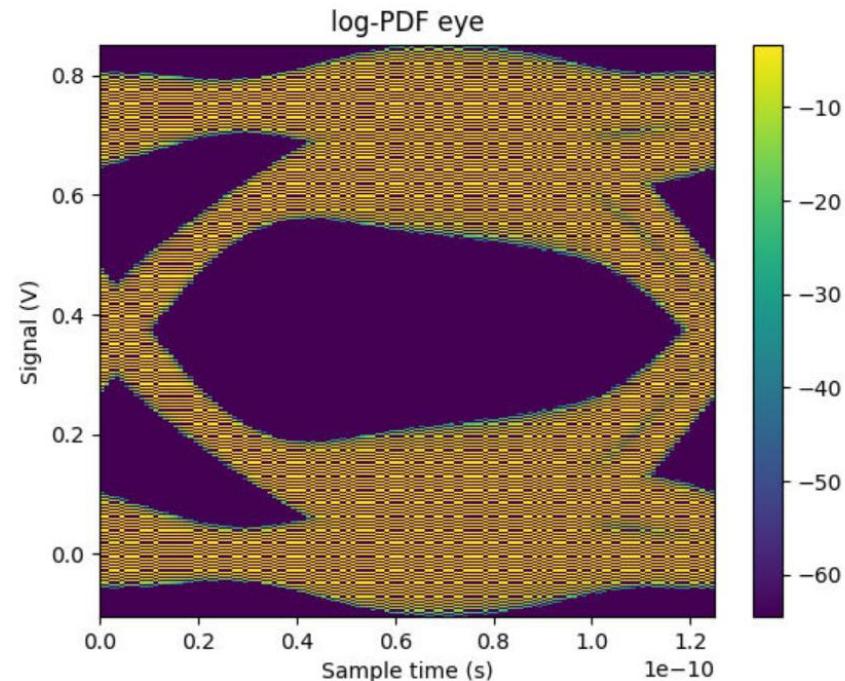
Full Slice 2mm Results: Cpar = 500fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 68.8% / 1.6%**

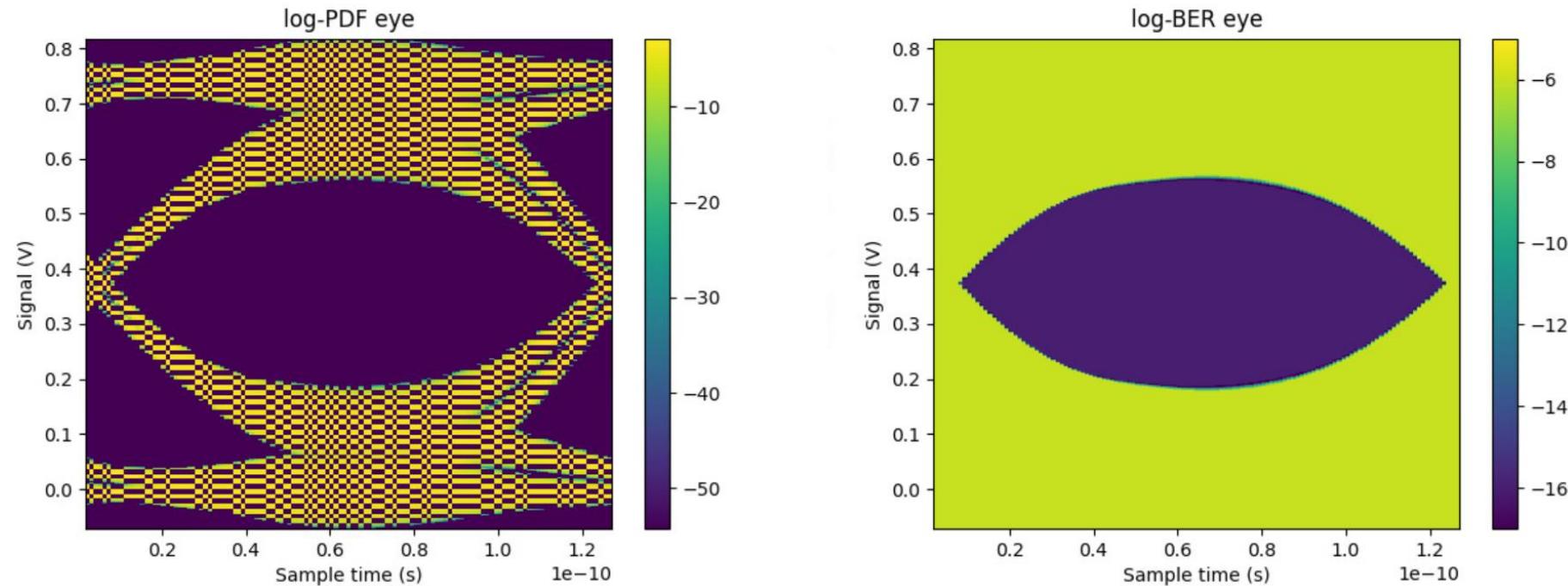
Full Slice 2mm Results:

20%-80% risetime = 23% UI, Cpar = 500fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 72.8% / 1.6%**

Full Slice 2mm Results: Cpar = 400fF



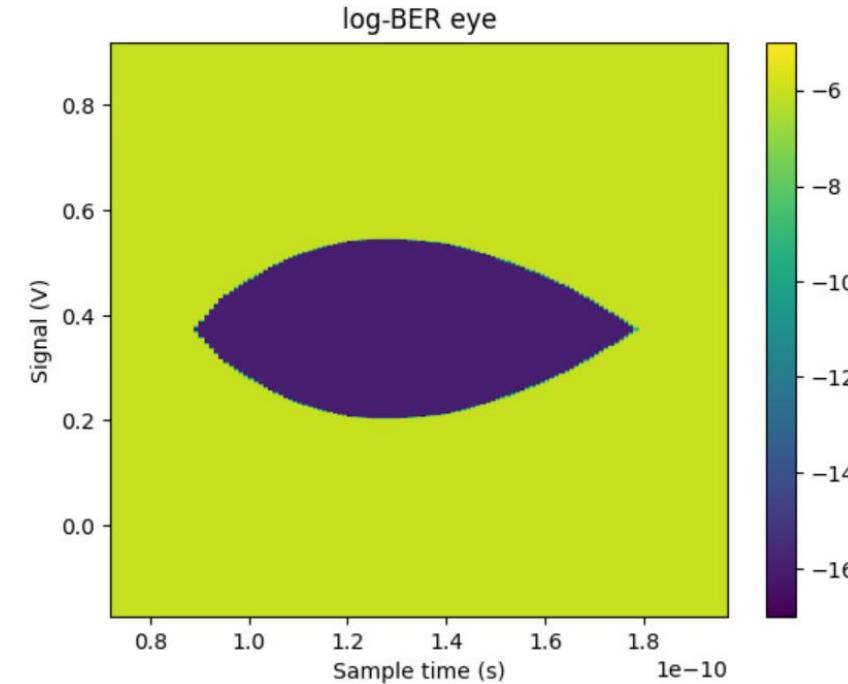
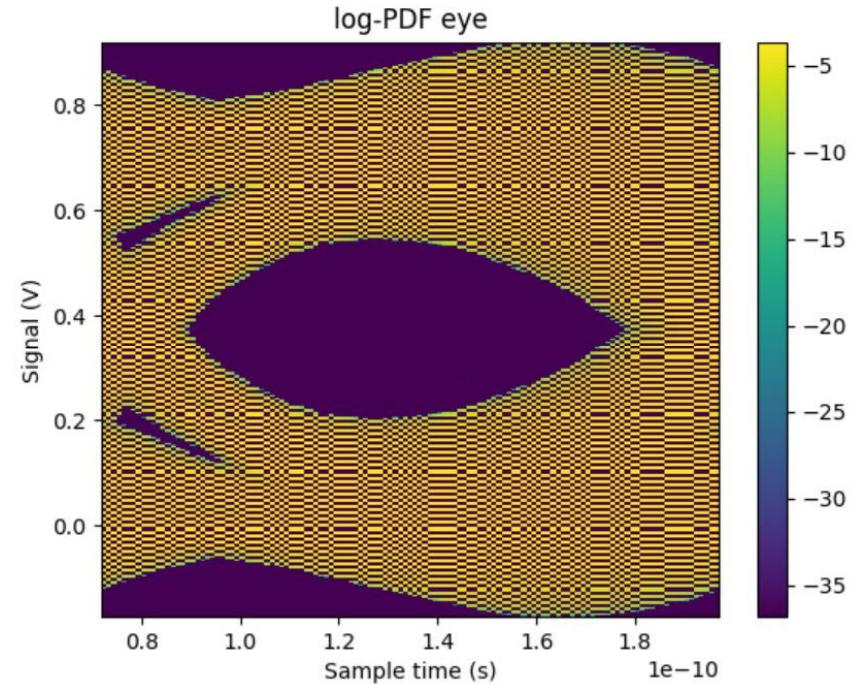
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 74.4% / 0.8%**



Keysight

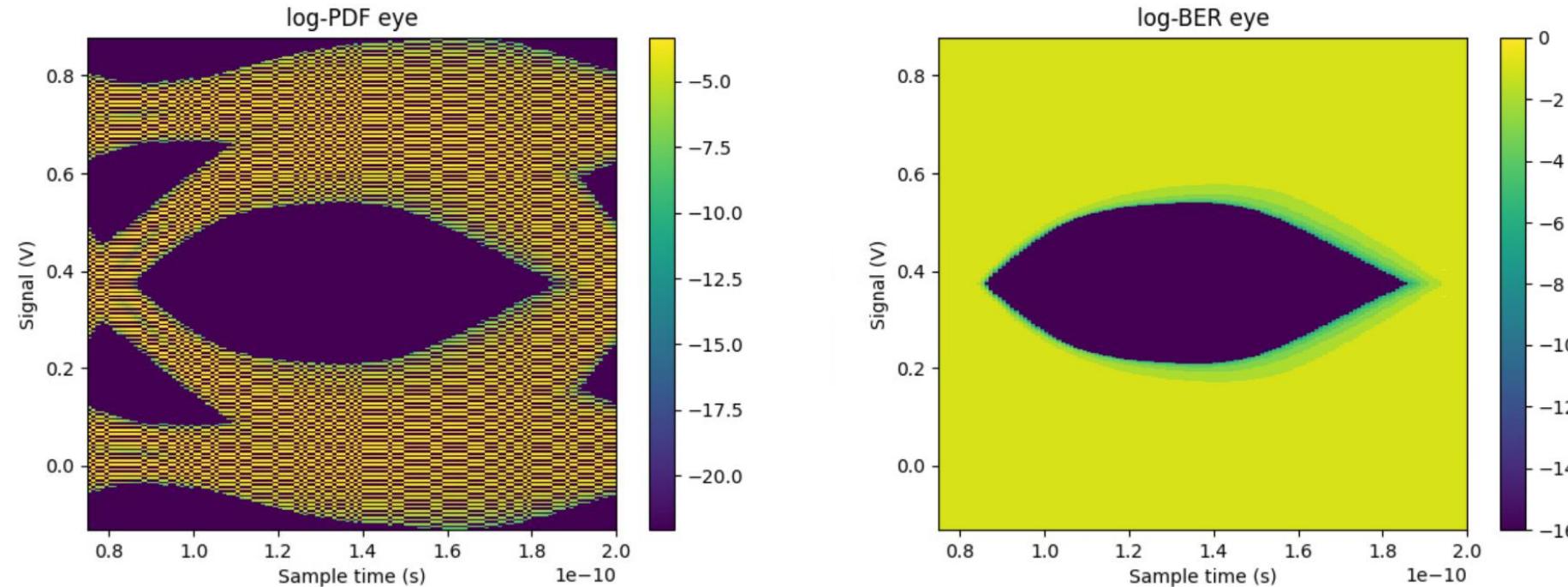
Keysight Results:

20%-80% risetime = 23% UI, Cpar = 500fF



- Worst line timing margin /crosstalk jitter @ 1e-15 BER: **55.2% / 3.2%**

Keysight Results : Cpar = 400fF



- Worst line timing margin / crosstalk jitter @ 1e-15 BER: **58.4% / 0.8%**
- Worst line timing margin / crosstalk jitter @ 1e-15 BER (75mV sensitivity): **68.8% / 0.8%**

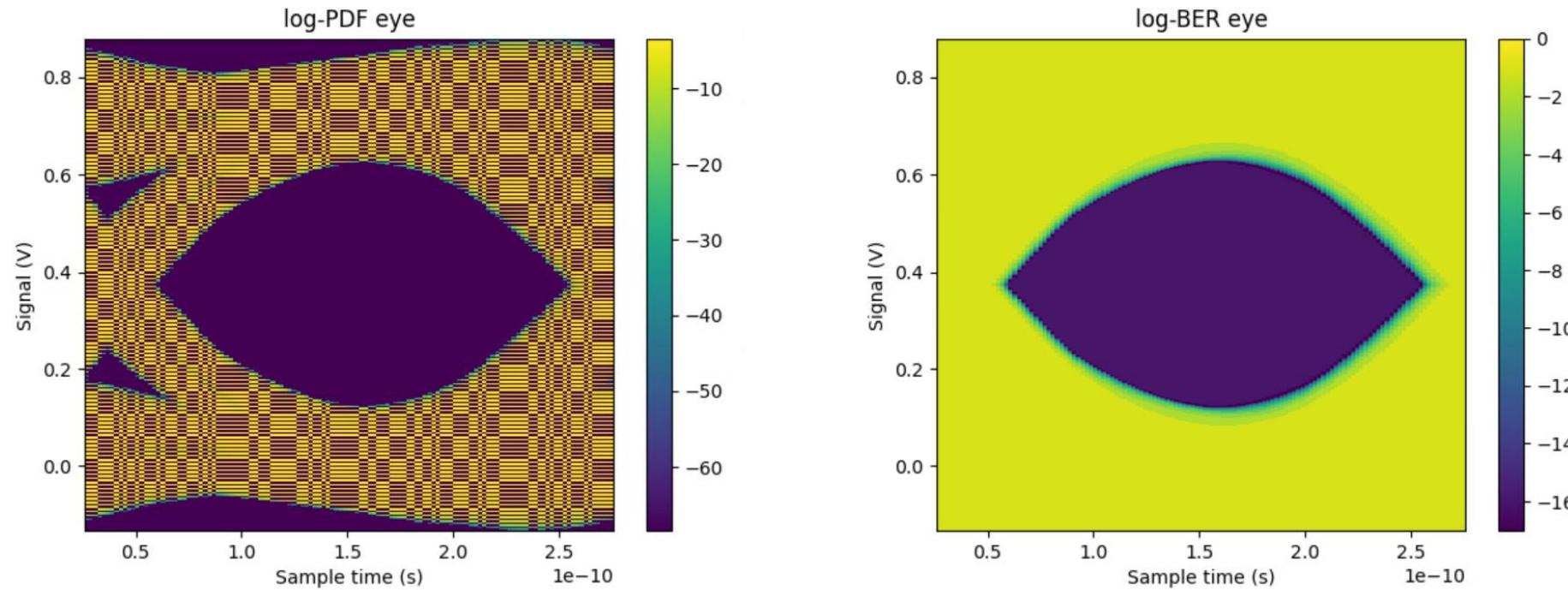
Setup (5): 4Gb/s Source Terminated

- Parameters set according to current (as of 12-2-21) electrical specs (unless otherwise noted on the slide):
 - 20% - 80% rise time of 0.32UI
 - $R_{TX} = 50\Omega$ (likely worst-case; will check other values later)
 - 1200fF lumped capacitance on TX/RX
 - $VDDIO = 750mV$
 - 300mV peak-to-peak RX sensitivity

Full Slice 10mm

Full Slice 10mm Results:

20%-80% risetime = 23% UI, Cpar = 1pF

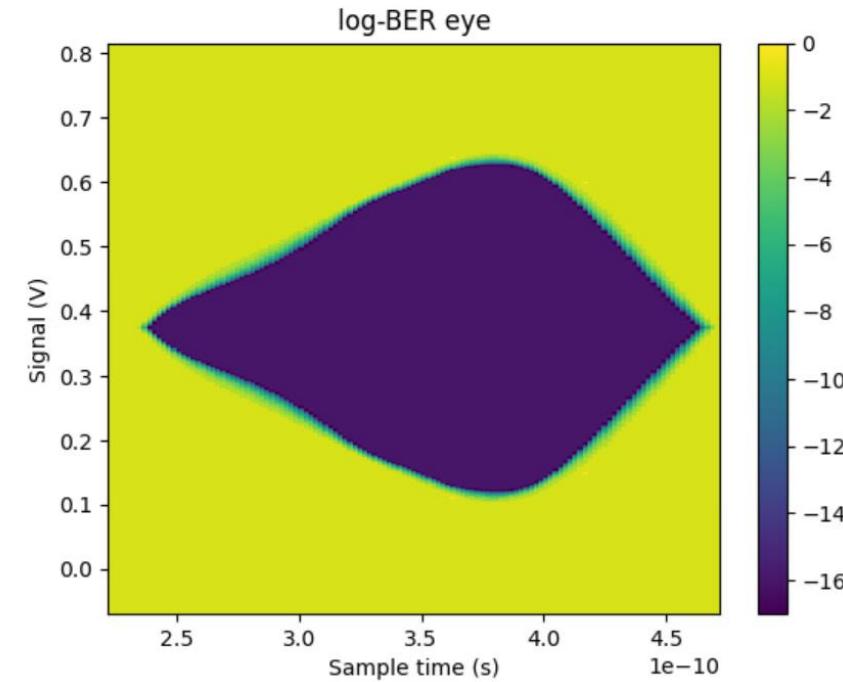
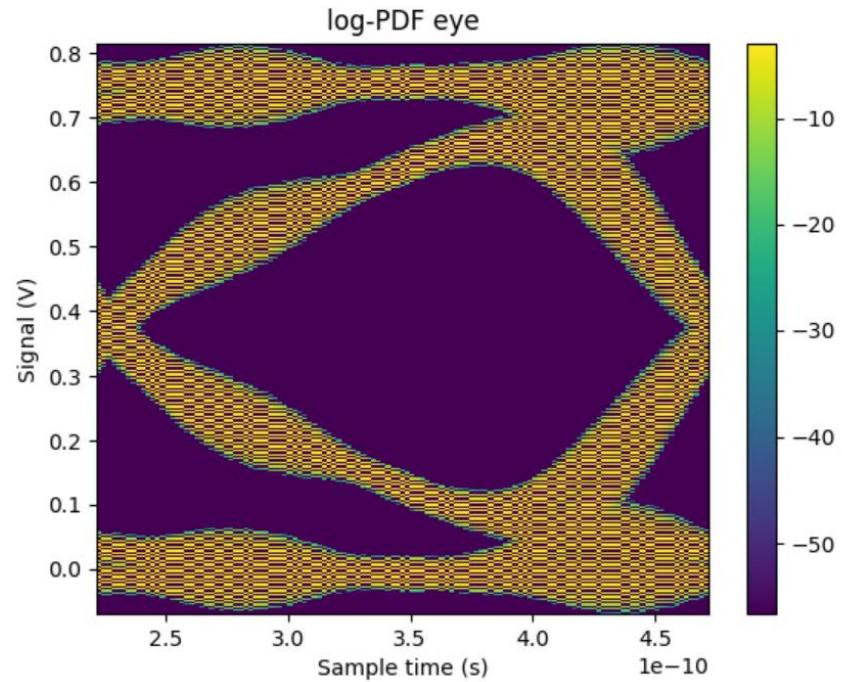


- **Worst line timing margin / crosstalk jitter @ 1e-15 BER (150mV sensitivity): 66.4% / 4%**

Full Slice 2mm

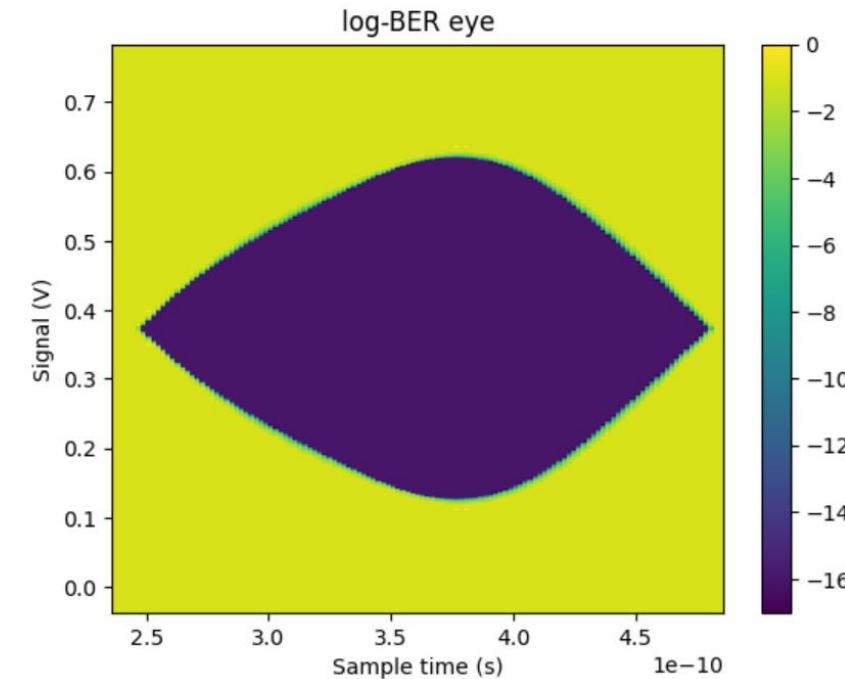
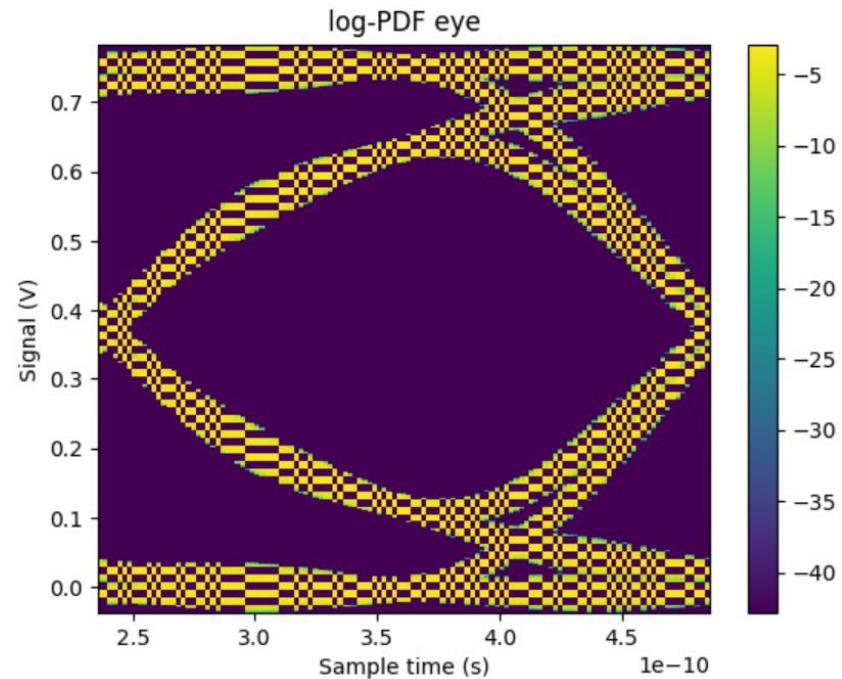
Full Slice 2mm Results:

20%-80% risetime = 23% UI, Cpar = 1pF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER (150mV sensitivity): 68% / 2.4%**

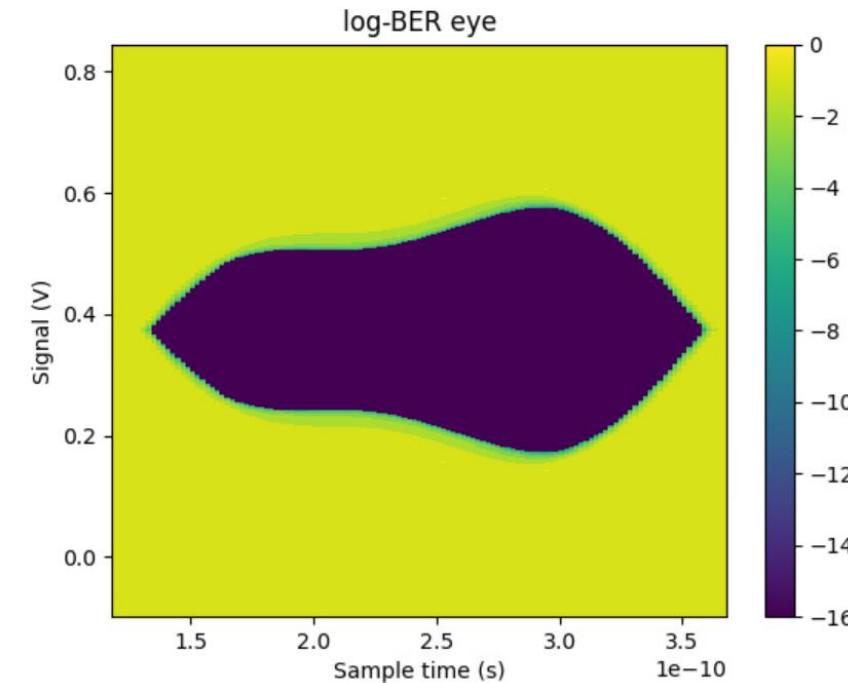
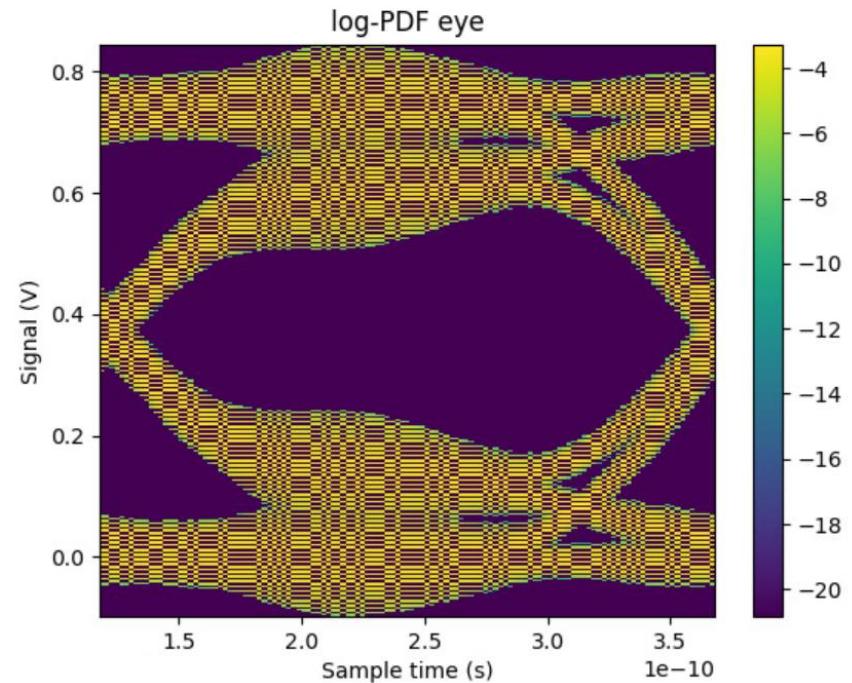
Full Slice 2mm Results: Cpar = 800fF



- **Worst line timing margin / crosstalk jitter @ 1e-15 BER: 51.1% / 0.8%**
- **Worst line timing margin crosstalk jitter @ 1e-15 BER (150mV sensitivity): 74.4% / 0.8%**

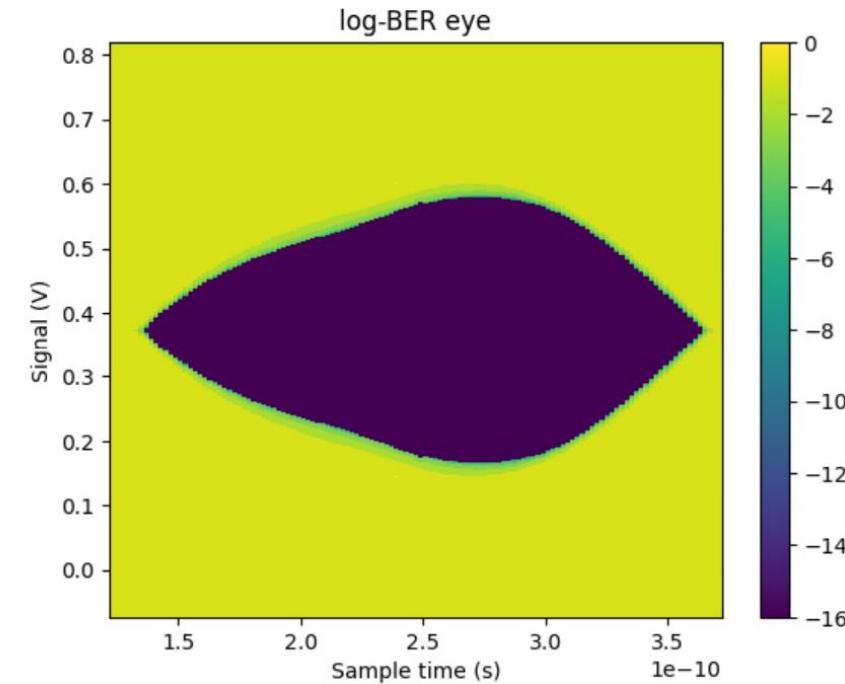
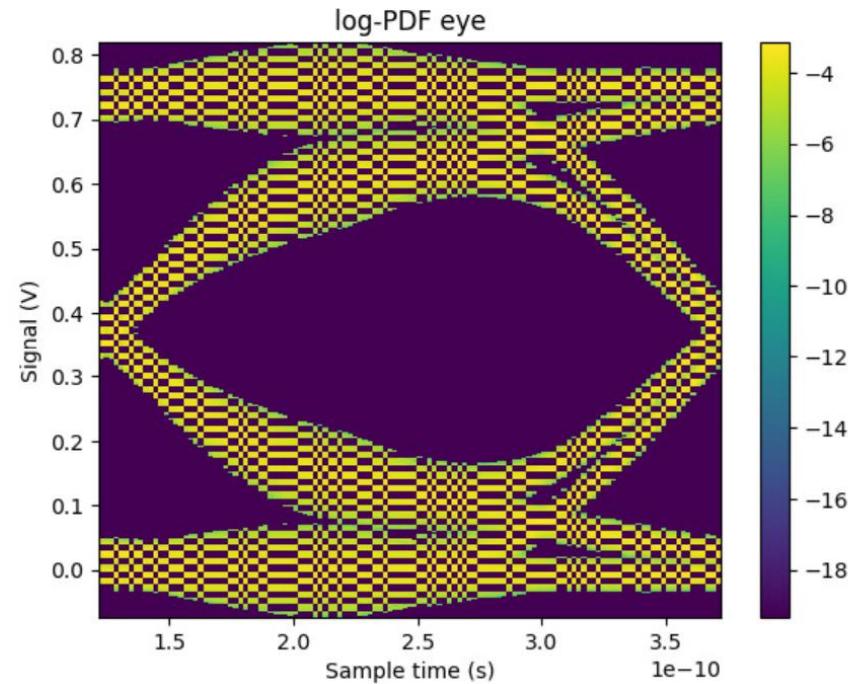
Keysight Results:

20%-80% risetime = 23% UI, Cpar = 1pF



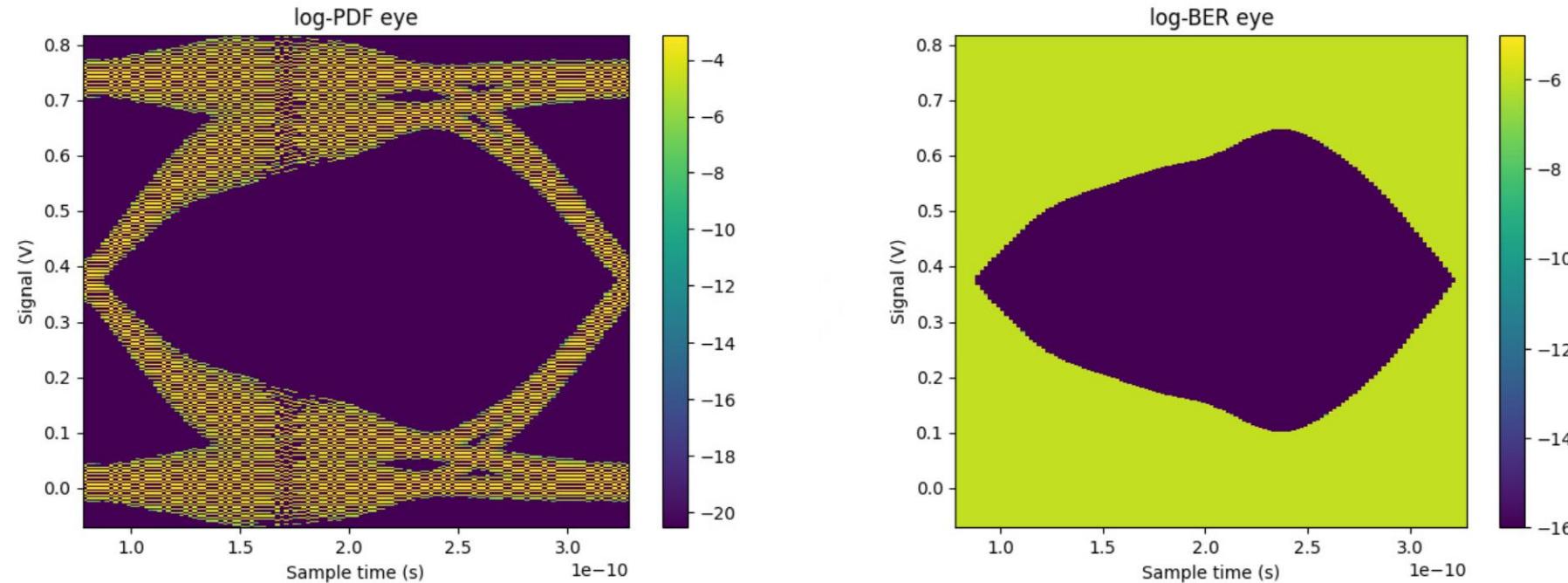
- **Worst line timing margin / crosstalk jitter @ 1e-15 BER (150mV sensitivity): 75.2% / 2.4%**

Keysight Results: $C_{\text{par}} = 800\text{fF}$



- Worst line timing margin / crosstalk jitter @ $1e-15$ BER: **43.2% / 2.4%**
- Worst line timing margin / crosstalk jitter @ $1e-15$ BER (**150mV sensitivity**): **72.8% / 2.4%**

Keysight Results: $C_{\text{par}} = 600\text{fF}$



- **Worst line timing margin @ $1e-15$ BER: 60.8%**
- **Worst line timing margin @ $1e-15$ BER (150mV sensitivity): 80%**