



Chiplet Data Exchange Markup Language (CDXML)

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Executive Summary

Chiplet Design Exchange (CDX) Workstream of ODSA focuses on electrical, mechanical, and thermal design exchange standards related to chiplets and integration in the context of multi chiplet modules, 2.5D and 3D Integrated Circuits (IC). This initial release of Chiplet Data Exchange in XML Format (CDXML) for but not limited to the following chiplets purposes:

* Data exchange between different formats
* Design
* Integration
* Assembly rules

This format is based on the zGlue Chiplets Info Exchange Format (ZEF) released with open-source copyright in 2019. As requested by the authors of ZEF, we acknowledge zGlue Inc for releasing ZEF in the open-source domain. All of the authors of ZEF have agreed to participate in developing this CDXML to replace the obsolete ZEF.

CDX is promoting this chiplet model for wider usage through open initiatives. CDXML sets a foundation for the standard machine-readable description of Chiplets, in order to help automate design and business processes across companies when it comes to chiplet-based business ecosystems. The spirit of this disclosure is to encourage openness in an otherwise closed-source industry of chip design. CDX and OCP are releasing this license based on creative commons open source license. The developers of this document have agreed to adopt the OCP Creative Commons License for this format.

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# 

# Introduction

This CDXML is developed from the ZEF for the following chiplets purposes:

* Common data exchange format between the chiplets
* Standard data structure with XML schema
* D2D interfaces information
* Mechanical information
* IO information
* Electrical information
* Power and thermal information
* Chiplet integration
* Assembly rules

This format is developed from the original zGlue Chiplets Info Exchange Format (ZEF) released with open-source copyright in 2019.

CDXML sets a foundation for the standard machine-readable description of Chiplets in order to help automate design and business processes across companies when it comes to chiplet-based business ecosystems.

What is included in this Repository?

* CDXML document, CDXML.docx
* XSD schema, CDXML.xslx
* CDXML presentation, CDXML.pptx
* CDXML example file, BQ27426YZFT.xml

# Format

CDXML is in Extensible Markup Language format (XML). The earlier version of ZEF consists of a set of ASCII text files in a comma-separated variable (CSV) format. CDXML enhances the format to the XML format, in particular, to support the following:

* Multiple value options data such as the IO modes
* Grouping of data such as min, typical, and max
* Nested values
* Customizable units
* Optional information such as tag and description
* Schema-based with XSD, the XML schema definition
* Easily extensible data
* Backward compatible with the older version

CDXML contains the data file, XML and the schema, XSD. The CDXML.xsd defines the schema for the XML file. The filename will follow the format of <MPN>.xml. MPN stands for Manufacturer's Part Number which is a unique product identifier.

The first line of the XML file consists of the file description and then followed by the name and value pair for each parameter.

There are multiple sections in CDXML; MECH, IO, ELECT and ASSEMBLY in the file, representing the mechanical, IO, electrical and assembly information of chiplets respectively. Most of this information can be found in the datasheets.

# Parameters

The first release of CDXML contains the parameters broken into the following sections

* Mechanical
* IO
* Electrical
* Assembly

These parameters define the interfaces and outside characteristics of these chiplets.

## Mechanical

Mechanical describes all x,y,z, tolerance, solder type and material properties.

| **Parameters** | **Type** | **Unit** | **Descriptions** |
| --- | --- | --- | --- |
| ID | Int |  | This parameter is reserved as a designator for the Chiplet in the chiplet library. This field will be left blank for a single chiplet but will be useful as an identifier in a library. |
| MPN | Str |  | Manufacturer's part number. Refer to unique SKU and ordering information |
| Version | Str |  | Version control |
| Authors | Str |  | Authors |
| Datetime | Date |  | Created time |
| Manufacturer | Txt |  | Manufacturer’s name |
| SMT\_compatible | Int | qty | A predicate that tells the reader whether this part is compatible with SMT or not. Valid values are 0 or 1. For most of the chiplets, this field will be set to 1 |
| Width | Int | um | Chiplet width in (um):  Typ - Typical value  Tol - Tolerance value  Min - Min value  Max - Max value |
| Length | Int | um | Chiplet length in (um):  Typ - Typical value  Tol - Tolerance value  Min - Min value  Max - Max value |
| Thickness | Int | um | Chiplet thickness in (um):  Typ - Typical value  Tol - Tolerance value  Min - Min value  Max - Max value |
| Orientation\_angle\_ccw | Int | Deg | Orientation angle (degree). Possible options are 0 degrees, 90 degrees, 180 degrees, and 270 degrees. If pin A1 (or pin 1) is on the top left with respect to the IO map, the orientation angle is 0 degrees |
| Bump | Int | um | Pitch - Nominal Distance between the centers of 2 consecutive balls. This parameter can be used to populate IO maps that are geometrically regular.  -Typ - Typical value  -Tol - Tolerance value |
| Int | um | Thickness - Typical thickness of the bumps or balls (Refers to z-direction).  -Tol - Tolerance value  -Min - Min value  -Max - Max value |
| Int | um | Dia - Typical diameter of the solder balls (Refers to horizontal footprint)  -Tol - Tolerance |
| Int | qty | Pop\_count - Number of balls, or IOs in a chiplet.  Unpop\_count - For a possibly regular bump pattern, count the unpopulated bumps. |

## IO

IO describes pin location, functionality, mode of operation, EC (Electrical Characteristics), abs max values, operating conditions, allowable RLC, voltage references, temperate based VI (Voltage and Current) pin characteristics.

| **Parameters** | **Type** | **Unit** | **Descriptions** |
| --- | --- | --- | --- |
| Number | Int |  | Index of the pin/ball/bump on the chiplet. For example, pin A1 or pin 1 |
| Name | Str |  | Name of the pin/ball/bump on the chiplet |
| Signal\_type | Str |  | Choose one from {Analog Input, Analog Output, Digital Input, Digital Output, Digital Input/Output, Power, Bypass, Reference, Ground, Clock, Xcvr, I2C, RF, DFT}. |
| Dir | Str |  | This field may seem redundant in addition to the signal type. It is used for determining the direction of the signal as input/output (IO), input(I) or output(O). |
| F | Int | MHz | Frequency of the signal  -Typ - Typical value  -Min - Min value  -Max - Max value |
| Mechanical\_type | Str |  | Choose one from {solderball, ubump, land, lead}. |
| Ball\_position | Int | um | Relative to the center of the chiplet, list the (x, y) coordinate of the ball location.  -x  -y |
| Signal\_group | Str |  | Used for grouping such as a bus or a pair sharing similar constraints. This should correspond to the mode for Pin\_name entry. |
| Int |  | Index - index of the pin in a group of signals. |
| Netlist\_name | Str |  | Default netname used internally (schematic can override). |
| Pin\_mode | Str |  | Mode - Mode of operation. Pins that are used for multiple usages can be described with multiple entries, but each mode should have a unique mode index. Valid values include 0,1,2.... |
| Int |  | Index - Index of Mode of operation. The total number of modes the current pin has. Most of the pins will have only one mode. |
| ESD | Str |  | ESD\_type - Describe any ESD (Electrostatic Discharge) anomaly for this pin. For example, some pins may need special design consideration for ESD purpose. |
| Int | V | Rating (V) - ESD Sensitivity Classification Levels. There are 3 different ESD models from the ESD Association:  1. Human Body Model (HBM) [100 pF @ 1.5 kilohms], ESD STM5.1. This is most common  2. Charge Device Model (CDM) [4 pF/30 pF], ESD DS5.3.1  3. Machine Model (MM) [200 pF @ 0 ohms], ESD STM5.2 |
| Controlled\_Impedance | Int | Ohm | A controlled impedance is desired for the signal trace |
| Vdd\_pin | Str |  | Pin name for the pin that is used as a VDD reference for this signal. Leave empty for VDD or GND pins. |
| Gnd\_pin | Str |  | Pin name for the pin that is used as a GND reference for this signal. Leave empty for VDD or GND pins. |
| V\_max | Int | V | Abs Max Voltage. |
| C | Int | F | Capacitance load  -Max - Maximum recommended capacitance load (including -self-capacitance).  -Typ - Typical load capacitance (includes self-capacitance |
| IO\_temp | Int | C | Temperature used to define the location of IO. Note that due to higher temperature the IO location changes due to expansion. |

## Electrical

Electrical contains overall electrical characteristics information to aid in power scenarios calculations, modes of operation, absolute maximum ratings, recommended operating conditions, and ESD.

| **Parameters** | **Type** | **Unit** | **Descriptions** |
| --- | --- | --- | --- |
| Op\_modes | Str |  | Modes of Operation |
| V\_modes | Str |  | Lists of Voltages vs Modes |
| Current\_modes | Str |  | Lists of Current Draw vs Modes |
| PVT | Str |  | Process, Voltage and Temperature Normalizing Data |
| ESD | Str |  | Type - Describe any ESD (Electrostatic Discharge) anomaly for this pin. For example, some pin may need special design consideration for ESD purpose. |
| Int | V | Rating - ESD Sensitivity Classification Levels. There are 3 different ESD models from the ESD Association:  1. Human Body Model (HBM) [100 pF @ 1.5 kilohms], ESD STM5.1. This is most common  2. Charge Device Model (CDM) [4 pF/30 pF], ESD DS5.3.1  3. Machine Model (MM) [200 pF @ 0 ohms], ESD STM5.2 |

## Assembly

Assembly parameters provide recommended assembly information by the chiplet supplier as part of the model. This information combined with the assembly rules from the assembler are needed to put the chiplets together on the carrier. These primarily include material information such as the coefficient of thermal expansion, young’s modulus, reflow profile, and clearances.

| **Parameters** | **Type** | **Unit** | **Descriptions** |
| --- | --- | --- | --- |
| D2D\_distane | Int | um | Default Die to die distance. Can be overwritten by assembler. |
| D2E\_distance | Int | um | Die to edge distance. Can be overwritten by assembler. |
| CTE | Int |  | Coefficient of Thermal Expansion (CTE) refers to the rate at which material expands with increase in temperature |
| YM | Str |  | Youngs Modulus Matrix |
| Reflow\_profile | Str |  | The recommended reflow profile for SMT or Flipchip process. It should be provided as a list of time vs temperature pairs. (String) |
| Mold\_material | Str |  | For a molded chiplet, name the mold material (String) |

## Checklist

Checklist based on the OCP/ODSA/CDX’s white paper of [Proposed Standardization of Chiplet Modesl for the Hererogeneous](https://www.opencompute.org/documents/ocp-odsa-cdx-proposed-standardization-of-chiplet-models-for-heterogeneous-integration-2-pdf).

Reference: CDK-Checklist.xlsx

| Category | Model | Flow | Status | Description | Notes/Comments |
| --- | --- | --- | --- | --- | --- |
| Thermal | |  |  | Chiplet and SiP level thermal |  |
|  | ECXML – JEDEC JEP181 | SiP Thermal |  | Required for all unique modes of operation | How do we propose updates to ECXML? Would like to include transient power profile support in the format. |
|  | Flotherm | SiP Thermal |  | Required for all unique modes of operation |  |
|  | Other | SiP Thermal |  | Identify alternate format if applicable |  |
| Optional | Chiplet GDS and/or LEF/DEF & SOC IP .LIB | Chiplet Thermal |  | For die level thermal analysis |  |
| Physical | |  |  | Die outline, pin layer, placement, shape | If this ready for 3d stuff, then need to include a 3d stack / configuration file as well. |
|  | LEF | Design Planning |  | Top level, + optional IO ring | Need DEF too. LEF & DEF. For all silicon-friendly formats like LEF/DEF, GDSII, OASIS need a supplemental file to confirm the preferred or required perspective, on package dimensions, and thermal or optical shrink values. |
|  | GDSII | Design Planning |  | Top level, + optional IO ring | This is not ideal for planning but can work for verification. |
|  | OASIS | Design Planning |  | Top level, + optional IO ring | This is not ideal for planning but can work for verification. |
| Optional | CSV | Design Planning |  | Chiplet X/Y/Z dimensions, pin name/locations | In place of csv we hope to propose a simple ASCII format for this. |
| Optional | Spice netlist | Design Planning |  | Top level pins (to support black box LVS) | Can we add Verilog, or Verilog+UPF. If using Verilog/UPF then you also need a mapping file. |
| Generated | JEDEC JEP30-P101/CDXML | Design Planning |  | Can be generated from other views |  |
| Mechanical | |  |  | Used for assembly and manufacturing handoff |  |
|  | CSV | Assembly/Reliability |  | If JEP30 not available. Physical outline of die and thickness, with tolerance on pin/die dimensions |  |
|  | Data sheet | General |  | If JEP30 or CSV not available. Physical outline of die, with tolerance on pin dimensions |  |
| Generated | JEP30-P101 | Assembly/Reliability |  | Can be generated from other views |  |
| Power | |  |  | Required for all unique modes of operation |  |
|  | Liberty (.LIB) | PI Analysis |  | Power (timing optional) |  |
|  | IEEE2416 power model | PI Analysis |  |  |  |
|  | Data sheet | PI Analysis |  | Summary of power per region/ P/G pin |  |
|  | UPF (optional) | Design Planning |  | Chiplet internal power intent |  |
| Behavioral | |  |  |  | Feedback from Intel is to make the bus functional model required - not optional. |
|  | System Verilog | Simulation |  | Functional model |  |
| Optional | Verilog-AMS 2.4 | Simulation |  | Recommended for AMS chiplets (functional model) |  |
| Optional | SystemC IEEE – 1666-2011 | Simulation |  | Functional model |  |
|  | Structural Verilog | RTL/LEC |  | IO Declaration (no functionality required) one P/G pin for each unique domain |  |
|  | CSV | RTL/LEC |  | If .V not available (same description as Structural |  |
| Signal Integrity Analysis | |  |  | For all C2C & D2D high speed interfaces |  |
|  | IBIS | SI Analysis |  |  |  |
|  | IBIS AMI | SI Analysis |  |  |  |
|  | Spice netlist | SI Analysis |  | Implied spice model for Transceiver IO driver |  |
| Optional | Channel model | SI Analysis |  | Sample SI setup |  |
| Optional | TX/RX IO characteristics & equalization options | SI Analysis |  |  |  |
| Power Integrity Analysis | |  |  |  |  |
|  | Chip Power Model (CPM) | PI Analysis |  |  |  |
|  | Chiplet GDS and/or LEF/DEF & SOC IP .LIB | CPM Flow |  | For die level power/IR drop analysis |  |
|  | Other |  |  | Identify alternate format if applicable |  |
| Electrical Rules | |  |  | Electronic data sheets for ESD, voltage min/max, … |  |
|  | Data sheet | General |  |  |  |
| Generated | JEDEC JEP30-E101 | ERC |  | Can be generated from other data sheet |  |
| Test | | SiP DFT |  | D2D, Chiplet and SiP level Test |  |
|  | BSDL – IEEE 1149.1/1149.6 |  |  |  |  |
|  | Internal JTAG (IJTAG) IEEE 1687 with ICL/PDL |  |  |  |  |
|  | ATPG model - Primitive/UDP based Verilog |  |  |  |  |
|  | ATPG vectors - STIL (IEEE1450.1) or WGL |  |  |  |  |
|  | MBIST/repair vectors - STIL (IEEE1450.1), WGL, or PDL/ICL |  |  |  |  |
| Recommended | Gray-box test wrapper netlist |  |  |  |  |
| Optional | IEEE-1500 logic and Core Test Language (CTL) |  |  |  |  |
| Optional | UPF or CPF for power-aware DFT |  |  |  |  |
| Optional | IP Firmware (if applicable) |  |  |  |  |
| Optional | efuse/OTP data for repair, PVT, etc. |  |  |  |  |
|  | 3D Stacked Die Test Access: IEEE 1838 |  |  | For 3D Only |  |
| Recommended | IEEE-1838 Flexible Parallel Port (FPP) |  |  | For 3D Only |  |
| Documentation | |  |  |  |  |
|  | Data sheets | General |  |  |  |
|  | SiP level Physical integration guidelines | General |  |  |  |
|  | Test Integration Guidelines | General |  |  |  |
| Optional | IP Firmware (if applicable) | Firmware support |  |  |  |
| Optional | Security |  |  | Document security modes and application notes |  |
| Optional | Trust and Traceability |  |  |  |  |

### 

### Status

N/A - Not available

A- Available (Availabe in Part Model, Under Contract/Contact Vendor/Comments)

### Notes

Unless otherwise noted, only one model is required for each category

Optional models may be provided in addition to required model

Chiplet providers can add additional models if applicable

# XSD Schema

<xsd:schema xmlns:xsd="http://www.w3.org/2001/XMLSchema" xmlns:tns="http://www.paloaloelectron.com" targetNamespace="http://www.paloaltoelectron.xsd" elementFormDefault="qualified">

<xsd:element name="CDXML" type="xs:string"/>

<xsd:element name="mech"/>

<xsd:complexType name="width" unit=”um”>

<xsd:sequence>

<xsd:element name="typ" type="xs:integer"/>

<xsd:element name="tol" type="xs:integer"/>

<xsd:element name="min" type="xs:integer"/>

<xsd:element name="max" type="xs:integer"/>

</xsd:sequence>

<xsd:complexType/>

<xsd:complexType name="io">

<xsd:sequence>

<xsd:element name="pnum" type="xs:integer"/>

<xsd:element name="pname" type="xs:string"/>

</xsd:sequence>

<xsd:complexType/>

<xsd:element name="elect"/>

<xsd:complexType name="abs\_rating">

<xsd:sequence>

<xsd:element name="v\_max" type="xs:integer" unit=”um”/>

</xsd:sequence>

<xsd:complexType/>

</xsd:schema>

# XML Example

<?xml version="1.0"?>

<name=”ZGL12345FC”>

<mech>

<width>

<typ>1550</typ>

<min>1550</min>

<max>1550</max>

</width>

</mech>

<io>

<pnum>1</pin\_number>

<pname>VDD</pin\_name>

</io>

<elect>

<absolute\_rating>

<v\_max>Input Voltage</v\_max>

</absolute\_rating>

</elect>

# 

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