Zaius / Barreleye G2 Specification
Chassis, Motherboard, Lunchbox Power Supply
Revision 0.6.0

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- IBM POWER9 CPU
- OpenCAPI
- AST2500 or AST2520 pin-compatible chips
- OpenPOWER's open source system firmware
- OpenBMC source code
- TI UCD90160 power sequencer
- TI TUSB2077A USB1.1 hub
- Amphenol G16CE41210W3EU connector
- Lotes AUSBS002-K001C05 connector
- Marvell 88SE9235
- Broadcom BCM5719A PCIe network controller
- Broadcom BCM54612E PHY
- Broadcom Cub SAS35x48
- Reneasas UPD720201K8
- Molex MiniFit Sr connector
- NVLink
- PLX PEX9797

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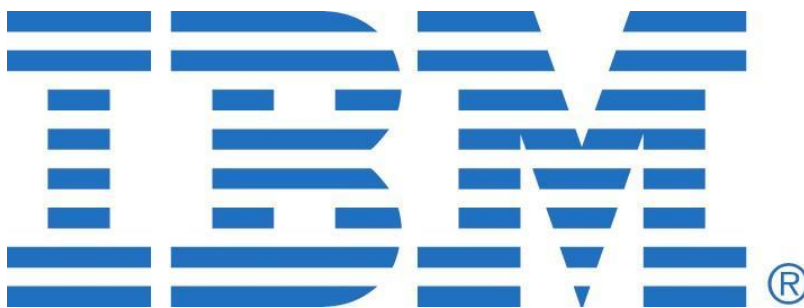
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2   Recognition & Logos

This specification and its associated first implementations in hardware were developed and tested by engineers and software developers at Ingrasys (a Foxconn / Hon Hai Industries subsidiary), Google, Rackspace, and IBM, based in part upon material made available through the OpenPOWER Foundation and community members.

3   Revision History

Revision	Date	Name	Description
0.1	08/10/2016	Aaron Sullivan	Draft Start
0.2	10/1/2016	Adi Gangidi	Added Chapters 6-12
0.3	10/10/2016	Rob Lippert	Added info on Zaius sled, shelf
0.4	10/14/2016	Aaron Sullivan	Reformat for upload to OCP Wiki
0.5	11/29/2016	Poly Yeh	1) Update P/N of SATA and USB/Serial RJ45 stacked connector 2) Add PCB information of BPx24, EXP and FPDB 3) Add Barreleye G2 thermal sensor introduction in page 28 4) Update Memory VR description in page 34 5) Update NVLink connector to 37-pin 6) Update mechanical figures
0.5.1	12/05/2016	Aaron Sullivan	1) Updates to Section 1.2 (Referenced Technologies Not Licenseed…) for readability 2) Removed references to EVT & DVT from section 7.1. Added reference to OpenCAPI. 3) Style changes to heading, table, and figure titles throughout document for consistency and readability 4) Inserted sections 9.9.1 (Zaius Chassis) and 9.9.2 (Barreleye G2 chassis) BMC sensors. 5) Updated section 10.1 (Thermal Design Requirements) for Barreleye G2 solutions, to support 300W CPUs in 2OU designs. 6) Update to section 11.6 (CPU Maximum Power). 7) Updates to section 12 headings and table titles 8) Moved section 12.1 (Memory Connector…) to section 7.4.4. DIMM population rules section number changed to 7.4.5. 9) Added IBM logo and reference to section 2 (Recognition and Logos) 10) Changes to pagination and graphics sizes for readability 11) There is a known issue in the BMC block

			diagram, with the size of BMC SPI and BIOS SPI flash. Both of these are listed as 1GB in size at present, and are actually smaller. This will be corrected in a subsequent revision.
0.5.2	12/07/2016	Aaron Sullivan	1) Spec now bundled with 3D step files for Zaius 1.5 OU sled and deployment shelf.
0.5.3	12/19/2016	Aaron Sullivan	1) Spec now bundled with EE BoM files for Zaius 1.5 OU sled and deployment shelf, Barreleye G2 2OU 5xPCIe chassis.
0.7.0	05/25/2016	Duen Hsu	1) Update vendor of USB/Serial RJ45 stacked connector 2) Add PCB information of Tri-mode BPx24, Tri-mode EXP 3) Update Barreleye G2 boards info 4) Update mechanical figures of system 3D in page 48 to page 57 5) Update Motherboard Component Placement in page 18 6) Update DIMM/CPU mapping table in page 20 7) Update the figure of LEDs in the Front Panel in page 28 8) Update the figure of fan speed control logic for Barreleye G2in page 31 9) Update the figure of hard drive cage power for Barreleye G2 in page 37 10) Update the figure of PCIe slots in page 38 11) Update the figure of LED/Button in page 42

4   Table of Contents

5   Scope

This document describes the specifications for:
- Zaius POWER9 motherboard
- Barreleye G2 server – 2OU
- Zaius server – 1.5OU

Zaius and Barreleye G2 are OpenPOWER-based Open Compute servers, based upon a common Zaius motherboard specification. These servers have mechanical and electrical packages designed for the 48-volt Open Rack v2.

Additional chassis form factors that are based on Zaius motherboard will be added to this document in further revisions. As of this draft, a 1.25 OU variation of the Barreleye G2 chassis remains to be added.

The hardware engineering specification provides technical details for the server board's functional architecture and feature set as well as some mechanical design details.

6   System Block Diagram

The Zaius motherboard can seat 2 IBM POWER9 LaGrange CPUs that support DDR4, PCIe Gen4, and NVLink/OpenCAPI.

- Each POWER9 LaGrange CPU has 8 DDR4 memory channels with 2 DDR4 DIMM slots per memory channel (16 DIMM slots per CPU, 32 DIMM slots total)
- The communication between CPUs is via two 30-bit X-bus coherent interconnections at 16Gbps
- POWER9 LaGrange includes integrated PCI Gen 4 controllers, with a total of 84 lanes spread between processors.
- Each CPU supports two x8 lanes of NVLink/OpenCAPI @ 25Gbps
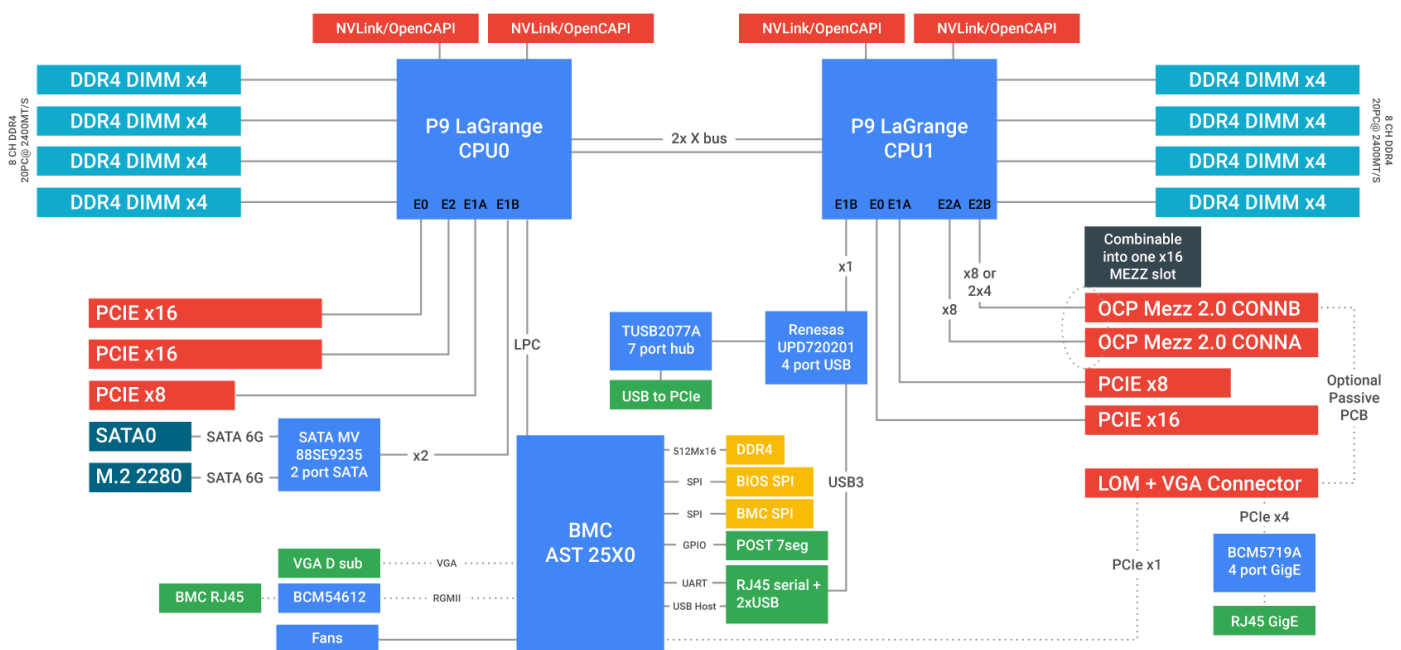
Zaius Block Diagram

7 Product Features:

7.1 Barreleye G2 Server Feature List

Server/Chassis name	Barreleye G2
Motherboard Name	Zaius
Chassis Size	2 OU and 1.25 OU (1.25 OU to be added later)
CPU	IBM POWER9 LaGrange CPUs x 2, 225W TDP CPU, 3899 pin socket
Memory	8 DDR4 channels per processor, up to two DIMMs per channel; total 32 DDR4 RDIMMs (2667 MHz@1DPC, 2400MHz@2DPC), 8/16/32/64GB
On-board SATA Controller	Marvell 88SE9235, support for 1 standard SATA port, and 1 M.2 2280 SATA port
Additional Storage	Tri-mode configuration with 20 x NVMe or 24 x SAS / SATA drive slots (SFF-8639), connected via SAS Expander (Broadcom Cub SAS35x48) and PCIe Switch (PLX PEX9797)
Board Network (Optional)	Broadcom BCM5719A PCIe x4 LAN-on-motherboard(LOM) with 1 front GbE RJ45, and NC-SI connection to BMC
USB Controller	Renesas UPD720201K8, support for USB 3.0. 1 USB3.0 port to front panel, 1 USB2.0 to BMC virtual device hub, and 1 TI TUSB2077A USB1.1 hub provides 5 USB1.1 to PCIe slots
Front I/O	1x USB3.0(from Renesas UPD720201K8), 1x USB2.0(from BMC), 1x serial RJ45(from BMC), 2x GbE RJ45(1 from BMC, 1 from LOM), VGA connector(when AST2500 is used), Power/Reset button, STB Power/All Power LED, SATA HDD LED, Boot Status LED, Attention LED, Fault LEDs, POST Card
Management	ASPEED AST2500/2520 with console to front serial RJ45, RMII1 port to a mux to select between the NC-SI HDMI connector, the MEZZ slot or BCM5719A LOM, and RMII2 port to a Broadcom BCM54612 PHY and front GbE RJ45
PCI-e Slot	1 x16 Gen4 Single-Slot, 2 x8 Gen4 Expanded-Slot, 1 x16 1.5-Slot, 1 x16 Double-Slot, and 1 x16 OCP Mezz 2.0 slot.
Board Size	MB : 13"Wx22.2"L (Dimensions are not final)
SKU	SKU1: Support 2 PCIe GPU and 1 x8 PCIe card; SKU2: Support 2 SXM2 GPU and 1 x8 PCIe card; SKU3: Support 5 PCIe cards

7.2 Zaius Server Feature List

Server/Chassis name	Zaius

Motherboard Name	Zaius
Chassis Size	1.5 OU
CPU	IBM POWER9 LaGrange CPUs x 2, 225W TDP CPU, 3899 pin socket
Memory	8 DDR4 channels per processor, up to two DIMMs per channel; total 32 DDR4 RDIMMs (2400 MHz@1DPC, 2133MHz@2DPC), 8/16/32/64GB
On-board SATA Controller	Marvell 88SE9235, support for 1 standard 22-pin SATA port, and 1 M.2 2280 SATA port
USB Controller	Renesas UPD720201K8, support for USB 3.0. 1 USB3.0 port to front panel, 1 USB2.0 to BMC virtual device hub, and 1 TI TUSB2077A USB1.1 hub provides 5 USB1.1 to PCIe slots
Front I/O	1x USB3.0(from Renesas UPD720201K8), 1x USB2.0(from BMC), 1x serial RJ45(from BMC), 1x GbE RJ45(1 from BMC), Power/Reset button, STB Power/All Power LED, SATA HDD LED, Boot Status LED, Attention LED, Fault LEDs, POST Card
Management	ASPEED AST2520 with console to front serial RJ45, RMII1 port to a mux to select between the NC-SI HDMI connector and MEZZ slot, and RMII2 port to a Broadcom BCM54612 PHY and front GbE RJ45
PCI-e Slot	1 x16 Gen4 Single-Slot, 2 x8 Gen4 Expanded-Slot, 1 x16 1.5-Slot, 1 x16 Double-Slot, and 1 x16 OCP Mezz 2.0 slot.
Board Size	MB : 13"Wx22.2"L

7.3   Motherboard Component Placement

Figure: Motherboard Component Placement
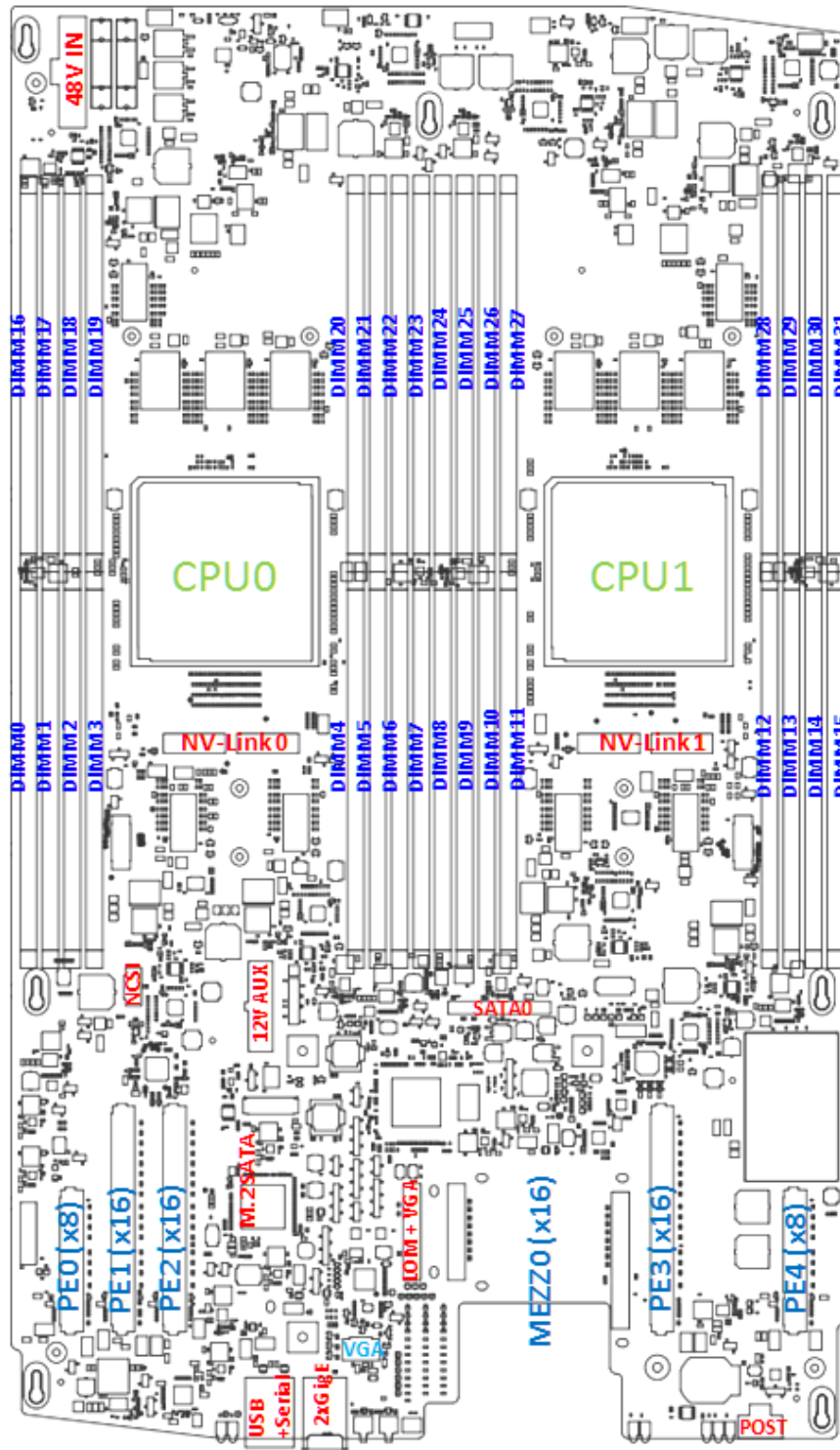
7.4 Processor and Memory

7.4.1 Processor Feature Set

IBM POWER9 LaGrange CPU. 190W, 225W and 300W TDP CPUs available. 3899 pin socket.

7.4.2 Memory

Each LaGrange CPU implements four Memory Bus Adapters (MBAs), each of which can control 2 independent DDR4 channels. Zaius has two DDR4 DIMM slots per memory channel (16 DIMM slots per CPU, 32 DIMM slots total). One or two DIMMs may be installed on each channel, following the IBM population rules.

7.4.3 Memory Support

The primary form of memory supported on this platform are Single and Dual Rank DDR4 RDIMMs with ECC of sizes 4 GB, 8 GB, 16 GB, 32 GB and 64GB.

Full list of DIMMs supported will added to this document in future revisions.

7.4.4 DIMM Connector

DIMM connectors are 288-pin DDR4 compliant and are spaced at 0.34" pitch (i.e. 0.34" between pin 1 of adjacent DIMM slots).

DIMM sockets support up to 25 mating cycles and have guard rails at each end. LLCR (low level contact resistance) DIMM sockets are applied.

7.4.5 DIMM Population Rule

The Zaius motherboard has two DDR4 DIMM slots per memory channel (16 DIMM slots per CPU, 32 DIMM slots total). One or two DIMMs may be installed on each channel, following the IBM population rules.

The table below illustrates CPU memory channel and DIMM interconnect mappings. The CPU memory channels A are the "outer" DIMMs (furthest from CPU, blue colored sockets), while memory channels B are the "inner" DIMMs (closest to CPU, black colored sockets).

Table: DIMM/CPU Mapping

DIMM	CPU	Channel	DIMM	CPU	Channel
DIMM16	CPU0	DDR6 A	DIMM0	CPU0	DDR5 A
DIMM17	CPU0	DDR6 B	DIMM1	CPU0	DDR5 B
DIMM18	CPU0	DDR4 A	DIMM2	CPU0	DDR7 A
DIMM19	CPU0	DDR4 B	DIMM3	CPU0	DDR7 B
DIMM20	CPU0	DDR0 B	DIMM4	CPU0	DDR1 B
DIMM21	CPU0	DDR0 A	DIMM5	CPU0	DDR1 A
DIMM22	CPU0	DDR2 B	DIMM6	CPU0	DDR3 B
DIMM23	CPU0	DDR2 A	DIMM7	CPU0	DDR3 A
DIMM24	CPU1	DDR6 A	DIMM8	CPU1	DDR5 A
DIMM25	CPU1	DDR6 B	DIMM9	CPU1	DDR5 B
DIMM26	CPU1	DDR4 A	DIMM10	CPU1	DDR7 A
DIMM27	CPU1	DDR4 B	DIMM11	CPU1	DDR7 B
DIMM28	CPU1	DDR0 B	DIMM12	CPU1	DDR1 B
DIMM29	CPU1	DDR0 A	DIMM13	CPU1	DDR1 A
DIMM30	CPU1	DDR2 B	DIMM14	CPU1	DDR3 B
DIMM31	CPU1	DDR2 A	DIMM15	CPU1	DDR3 A

For deployment, only full and half-population of DIMM sockets are supported. When there is half-population of memory, only the outer blue DIMM of each memory channel is installed e.g. only DIMMs 0, 2, 5, 7, 8, 10, 13, 15, 16, 18, 21, 23, 24, 26, 29, 31 are installed.

It's possible to boot the system when just one DIMM is populated on any memory channel.

7.5   Storage

Storage consists of 2 forms: On-board storage and in-chassis storage cage. In chassis-storage cage consisting of a storage back-plane is typically wired to the motherboard via PCIe RAID controller and Expander board

	Barreleye G2 2 OU	Zaius Chassis 1.5 OU
On-board Storage	1 M2 SATA and 1 SATA HDD (3.5"/2.5")	1 M2 SATA and 1 SATA HDD (3.5"/2.5")

In-Chassis Drive Cage Support	20 NVMe or 24 SATA / SAS Drives	N/A

7.6   Printed Circuit Board Information

Each PCB material and stack-up are defined in the table below.

Board	PCB Material	PCBA Dimension (L*W*H) （mm）
Motherboard	TU872SLK low-loss material	564x330x3
Tri-mode HDD Back Plane X24 (Barreleye G2 Only)	IT-150DA	536.5 x 88.15 x 4.15
Tri-mode Expander Board (Barreleye G2 Only)	TU-862HF	232 x 130 x 2.37
Fan / Power Board (Barreleye G2 Only)	IT-180I / NP-175F	304.8 x 153.15 x 1.57
RMC board (Barreleye G2 Only)	IT-180/ IT-180A	358.3 x 76 x 1.6

7.6.1   Motherboard 22-Layer Stack-up

Layer Name	Description	Material	Thickness	Copper (Oz)	Dielectric (Er)
	Solder Mask		**0.50**		
Signal1	SIGNAL	Copper	**2.00**	**0.5 + 1 (plating)**	
	PREPREG (2-ply)	**LL FR4**	**3.60**		**3.1**
GPlane2	GND	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
Signal3	SIGNAL	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
GPlane4	GND	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
Signal5	SIGNAL	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
GPlane6	GND	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
Signal7	SIGNAL	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
GPlane8	GND	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
Signal9	SIGNAL	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
GPlane10	GND	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
PPlane11	PWR	Copper	**2.50**	**2.0**	
	PREPREG	**LL FR4**	**7.00**		**3.2**
PPlane12	PWR	Copper	**2.50**	**2.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
GPlane13	GND	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
Signal14	SIGNAL	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
GPlane15	GND	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
Signal16	SIGNAL	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**
GPlane17	GND	Copper	**1.20**	**1.0**	
	PREPREG	**LL FR4**	**4.50**		**3.3**
Signal18	SIGNAL	Copper	**1.20**	**1.0**	
	CORE	**LL FR4**	**4.00**		**3.3**

GPlane19	GND	Copper	1.20	1.0	
	PREPREG	**LL FR4**	**4.50**		3.3
Signal20	SIGNAL	Copper	1.20	1.0	
	CORE	**LL FR4**	**4.00**		3.3
GPlane21	GND	Copper	1.20	1.0	
	PREPREG (2-ply)	**LL FR4**	**3.60**		3.1
Signal22	SIGNAL	Copper	2.00	0.5 + 1 (plating)	
	Solder Mask		0.50		

8   System Firmware (System BIOS)

Zaius uses OpenPOWER's open source system firmware, made available under open source licensing schemes. The OpenPOWER firmware stack is available at https://github.com/open-power. Zaius system based machine configuration data files will be added to this repository soon.

BIOS update methods are available with documentation on https://github/open-power.

9   BMC – System Interaction

The Zaius motherboard uses a BMC (AST2500 or AST 2520 chips) for various platform management services and interfaces with hardware, BIOS.

The BMC is a standalone system in parallel to the host. The health status of the host system should not affect the normal operation and network connectivity of the BMC. The BMC cannot share memory with the host system. BMC management connectivity should work independently from the host. If using a shared NIC, there should be no NIC driver dependency for out-of-band (OOB) communication.

9.1   BMC Hardware Overview

Zaius Motherboard is designed to support dual layout of either AST2500 or AST2520 pin-compatible chips. BoM stuffing options are provided to tie off unused PCIe/VGA pins as specified in AST2520 datasheet when AST2520 is installed. Barreleye G2 Chassis specifically uses AST2500 for its BMC.

ASPEED AST2500 or AST2520 device is connected to the CPU0 LPC bus (refer to Section 5 block diagram) and is used to provide the following functions on Zaius motherboard:
- Fan Monitoring and Control
- Serial Port
- Port 80 Decode to LEDs
- Environmental monitoring
- Remote serial console and reporting capabilities through NC-SI
- SMBus Master (thermal sensors, power monitors)
- FSI master to CPU0
- Virtual USB device slave
- USB host for BMC
- BIOS SPI master
- Gigabit Ethernet
- VGA controller (AST2500 only)

The BMC has its own peripherals:
- 1GB (512Mx16) DDR4 memory
- 64MB socketed SOIC16 SPI flash (BMC firmware interface CS0#)
- 8MB soldered-down writable/scratch SPI flash (BMC SPI2)
- Battery backup (3.3V VBAT for SRAM)
- I2C RTC (PCF8523)

9.2   BMC Connection Diagram

The following diagram provides an overview of the BMC connections on the Zaius motherboard. These connections may change between the present revision and the final release.

Figure: BMC Connection Diagram
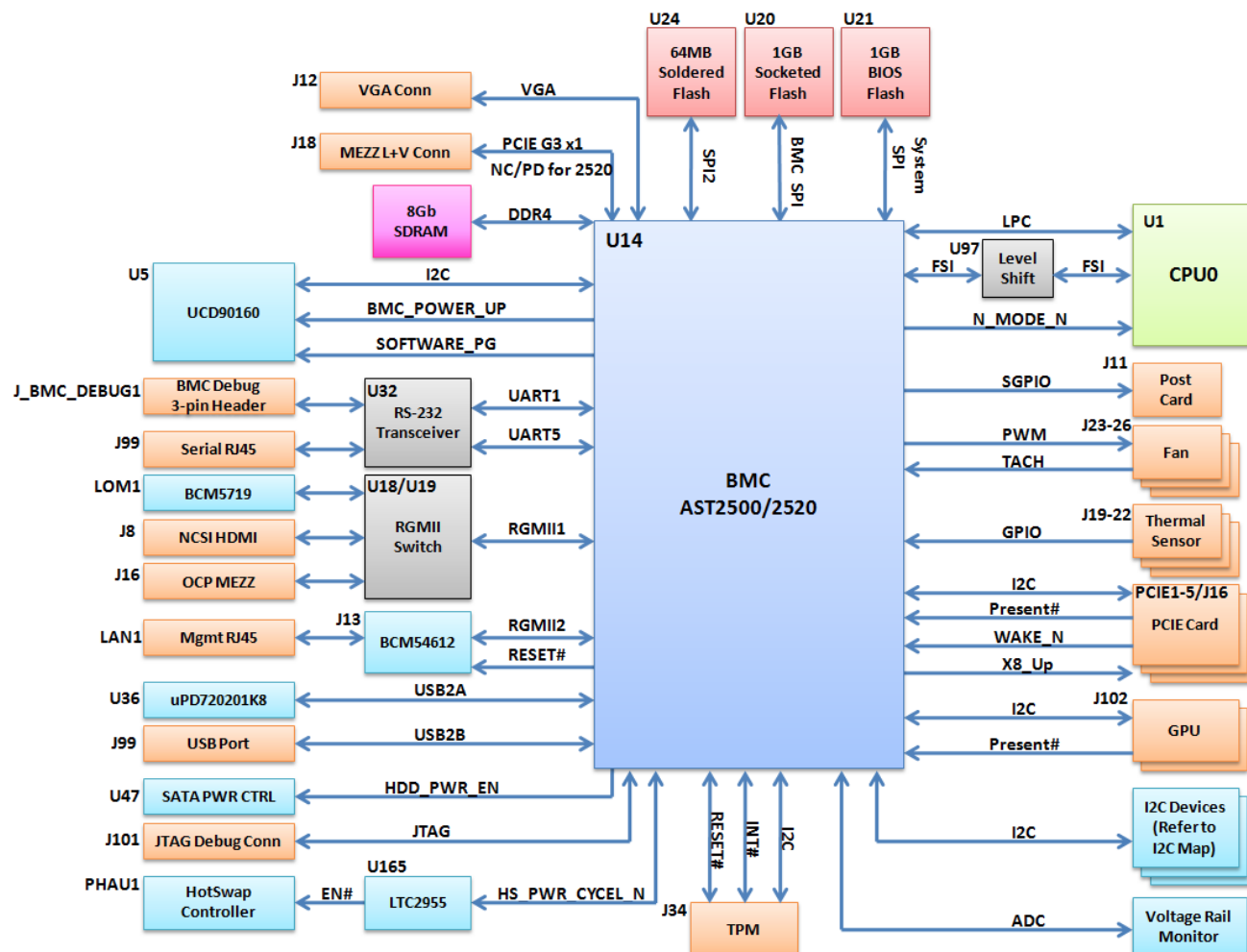
9.3   Management Network Interface

Zaius motherboard front panel optionally provides 2 RJ45 gigabit Ethernet connections in a dual stack connector. The top Ethernet port connects to BCM5719A PCIe Ethernet. The bottom port connects to BMC-only BCM54612 PHY.

9.3.1   BMC-only Gigabit Ethernet (optional)

A Broadcom BCM54612 RGMII capable PHY and front panel RJ45 connector with LINK and ACT LEDs will be used to connect BMC port RGMII2. This Ethernet port is only usable by the BMC for management purposes and is not connected to any PCIe controllers hosted by Power9 CPUs.

9.3.2   BCM5719A PCIe Gigabit Ethernet LOM (optional)

A Broadcom BCM5719A PCIe network controller is used in an optionally stuffed LAN-on-motherboard (LOM) role. Port 0 of the controller connects to a front panel RJ45 connector with LINK and ACT LEDs, the other ports are unused. The 4X PCIe lanes for the LOM are connected to lanes 8,9,10,11 of the LOM+VGA connector (optional).

NC-SI signals of the BCM5719A are be connected to the BMC as specified in the block diagram.

9.4   Local Serial Console and Serial-Over-LAN (SOL)

The BMC will support two access paths to the serial console:
- A local serial console on RJ45 serial port
- A remote console, available via Secure Shell (SSH), through the management network.

9.5   Graphics and GUI

Graphic and GUI features integrated in BMC (ASPEED AST2500 series) chip. Graphics and GUI are optional. This specification also makes reference to ASPEED AST2520 solutions, without graphics support.

9.6   Remote Power Control and Power Policy

BMC firmware will support remote system power on/off/cycle and warm reboot through the REST or SSH commands.

BMC firmware will support power on policy to be last-state, always-on and always-off. The default setting is Last-State. The change of power policy should be supported by REST or SSH command and take effect without a BMC firmware cold reset or a system reboot.

A reset button (black) and a power button (blue) are mounted at the front edge of the Motherboard. Power Button is on the left of the Reset button. All devices are capable of being manually reset to a known state via the Reset button. The power button is pressed for ~4 seconds to power off the server. When the system is powered off a press and release of the power button would power the server on.

More details on exact timing of power and reset button press and subsequent behavior will be added in the next revisions of this document as it is refined.

9.7   LEDs: Power, HDD Status, System Identification, BMC Heartbeat, Faults

These LEDs are located on the front edge of the PCB and exposed to the front panel. They will be clearly labeled on the silkscreen.

On front panel of the tray LEDs are listed in the preferred left-to-right order as seen in the below front panel picture:
- Blue LED: Indicates standby power good.
- Green LED: Indicates All Power Good (from Sequencer).
- Green LED: System Boot Status (driven from BMC GPIO)

- Yellow LED: Indicates HDD activity. There is a GPIO0 signal from the Marvell 88SE9235 for SATA drive activity.
- Yellow LED: Attention (machine locator, driven from BMC GPIO) - this LED should be placed away from the HDD activity LED, either on the left or right side of the mother board.
- Red LED: Platform fault. Driven from BMC GPIO.
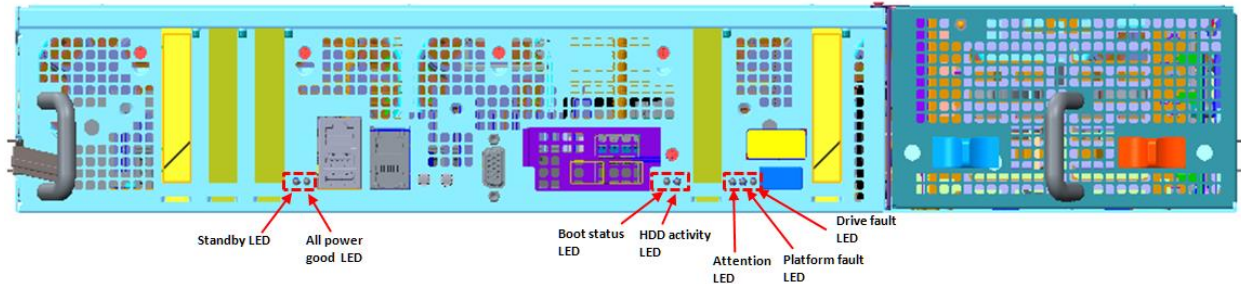- Red LED: Onboard drive fault. Driven from BMC GPIO

Figure: LEDs in the Front Panel of Barreleye G2 Tray

9.8   Power, Thermal Monitoring and Power Limiting

The following hardware monitoring is being provided:
- Voltage monitoring is performed by the TI UCD90160 sequencer device and BMC.
- System fan monitoring and control is performed by the BMC.
- Power monitoring, limiting and thermal monitoring may be performed by the BMC and/or processor OCC.

The following points to be monitored for power:
- 48V input to tray (at the hotswap controller)
- CPU core input at 48V
- Memory input at 48V
- System 12V input at 48V
- Power monitoring connections for off-board drive tray or other I/O device.

9.9   Sensors

9.9.1   Zaius

The Zaius motherboard will provide 4 headers for tray-level thermal air temperature sensors. The thermal sensor will stand approximately 1.6in above the board within the footprint of the connector. One sensor will be in the front/center (inlet sensor), one will be rear/center, and two will be rear/corners behind each CPU. The font inlet sensor to be placed vertically, with pin 1 facing the rear of the motherboard. The rear sensors to be placed horizontally, with pin 1 facing the right of the motherboard.

The thermal sensors will be directly connected to the BMC using 1-wire interfaces. Each sensor should be connected to a separate 1-wire interface for location determination purposes. The AST25X0 BMC does not have native 1-wire support, 1-wire support will be provided by a GPIO and Linux kernel emulation layer (w1_gpio driver).

Table: Thermal Header Pinout

Pin	Signal
1	VDD
2	1-wire data
3	GND

9.9.2   Barreleye G2

The Barreleye G2 system uses three TMP75AIDR thermal chips that is requiring no external components and specified for operation over one temperature range of −40°C to +125°C with a resolution of 0.0625°C. Three thermal sensors will be directly connected to the BMC using two-wire SMBus interface. Two sensors, which are located in front of the motherboard and on fan board, are used to monitor server inlet and outlet temperature. The third temperature sensor on HDD board is to monitor temperature of HDDs.

Table: Thermal Address

Sensor	Location	BMC I2C Port	BMC I2C Address	Application
1	Motherboard	I2C1	0x4A	Server inlet temperature
2	Fan board	I2C10	0x72	Server outlet temperature
3	HDD board	I2C10	0x4F	HDD temperature

9.10 System Event Log (SEL)

System event logs to be accessible via BMC using SSH or REST interface. A more conclusive list and description of all events to be logged is still under development and will added in future revisions.

9.11 Fan Speed Control in BMC

System fan control and monitoring is provided by BMC on Zaius motherboard.

System fan headers support 12V fans. With High-Z PWM output from BMC (e.g. when BMC is first being configured at power-on), system fans should run at full speed. Resistor pull-up options to be included on the motherboard.

For Barreleye G2 chassis an extra fan control board (using PWM comparator NCT73685) helps set the fans to full speed in cases where BMC crashes / goes down abruptly.

Figure: Fan Speed Control logic in Barreleye G2
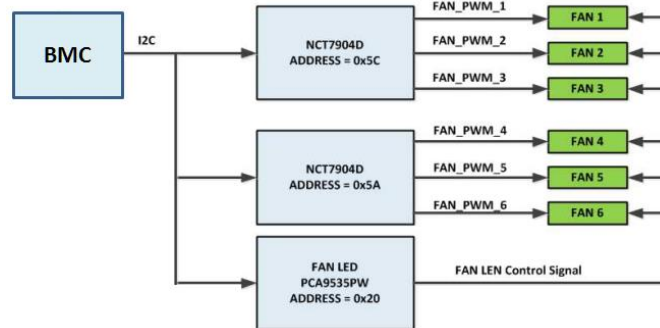
Fan control behavior to change by chassis and in further revisions. Fan control table will be maintained by revision control for each chassis in OpenBMC repository. Chassis specific fan control details to be added in this spec in further revisions.

9.12 BMC Firmware

Machines based on Zaius platform can support a variety of BMC firmware solutions, including OpenBMC. OpenBMC is available primarily through its GitHub repository:
1. The OpenBMC / OpenBMC repository: https://github.com/openbmc/openbmc
    a. This repository will include most OpenPOWER & Zaius based chassis specific contributions.
    b. Specific drivers for OpenPOWER machines were contributed here: https://github.com/openbmc/openbmc/tree/master/meta-openbmc-machines/meta-openpower

OpenBMC source code is available under its own license scheme.

9.13 BMC Firmware Update Methods

9.13.1 Physical Method

Replace BMC Chip with the updated one. A figure showing the location of replaceable BMC ROM to be added in future revisions.

9.13.2 Update BMC via REST API

Exact procedure to be added in future revisions after validation.

9.14 BIOS Update from BMC
● Transfer a copy of the BIOS image (eg. bios.pnor) to flash into the /tmp directory of OpenBMC
● Use the "pflash" utility to erase and program the BIOS PNOR:

o   pflash -E -p /tmp/bios.pnor

The pflash utility might be getting replaced by another BMC utility, during development of this specfication. This document will be updated with corresponding changes in future revisions.

9.15 BMC JTAG Debug Connector

With either AST BMC device, the JTAG debug interface shall be available through the "10-pin connector for ARM targets" as defined in ULINK2 Target Connectors.

Table: BMC signals available at the JTAG connector

Pin	Signal	Signal	Pin
1	VCC_3V3	JTAG_TMS	2
3	GND	JTAG_TCK	4
5	GND	JTAG_TDO	6
7	JTAG_RTCK	JTAG_TDI	8
9	GND	SRST# *	10

* SRST# refers to the system reset pin of BMC device, not its JTAG TRST pin.

10 Thermal Design Requirements

10.1 Barreleye G2 Server

For Barreleye G2, thermal design should support 35degC ambient under one fan failed condition. This should be possible with 2 x 225W Power9 in 1.25OU chassis designs / and 2 x 300W Power9 CPUs in 2 OU chassis designs.

Description	Requirement
System loading	Idle to 100%
Datacenter operating temperatures	20C to 40C
DIMMs	Tcase < 75C at all operating conditions
CPUs	Per IBM required values
Fan Redundancy	N+1 redundancy is required

10.2 Zaius Server

Zaius server is designed to operate under these thermal conditions:

Description	Requirement
System loading	Idle to 100%
Inlet air temperature range	<32°C * CPU throttling is not permitted in this range. * All components must remain below their max spec temperatures
Machine ΔT	>11°C
Cold-Aisle Pressurization	TBD
Relative Humidity	8% to 90%, non-condensing
Location of Data Center/Altitude	1800 meters above sea level or lower
DIMMs	Tcase < 75C at all operating conditions
CPUs	Per IBM required values
System thermal sensors max allowable tolerance	±1°C
Fan Redundancy	N+1 redundancy is not required

11 Motherboard Power system

11.1 Input Voltage

The system uses an always-on power supply unit that delivers a fixed unregulated voltage to Zaius motherboard in the range 40V to 60V; VRs are designed to support this input range.

48V will be regulated down to 12V on motherboard. Regulation down to other rails will be from the 12V rail. 48V will also be regulated down to the CPU core voltage and DDR voltage using CPU and Memory VR respectively.

11.2 Power Input Connector and Hot Swap Controller (HSC) Circuit

Zaius motherboard will use an on-board input power connector to receive 48V from the rear of the tray.

Directly next to the 48V input connector to the motherboard will be a fuse / hot-swap circuit. The circuit is based on Analog Devices ADM1272 hot swap controller.

HOTSWAP_PWR_CYCLE_N signal is driven from BMC and is opto-coupled and sent to the 48V hot swap device enable signal. It can be used for quasi-AC power cycle for test enabling.

Full details on Hot swap controller circuit and how it is leveraged to be added in further revisions of this document.

11.3 Power Sequencing

IBM-specified power sequencing requirements are observed for both power up and power down. The TI UCD90160 power sequencer is used for Zaius CPU rail power sequencing. A signal from BMC is used to reset the sequencer directly. The sequencer is controlled by the BMC.

11.4 CPU Voltage Regulator (VR)

Zaius motherboard provides AVS-compliant VRs to supply the CPU core (VDD/VCS/VDN) rails. More details to be added in further revisions of this document.

11.5 Memory VR

Zaius uses AVS-compliant regulator which is directly converted from 48V to power VDDQ power rail. VPP and VTT are converted from 12V and VDDQ respectively by voltage regulators. More details to be added in further revisions of this document.

11.6 CPU Maximum Power

The motherboard and VR Module interconnect solution implemented on the motherboard is designed for 225W CPUs (with 3 x 75 watt VRs) as a baseline requirement with a potential of supporting up to 300W (with 4 x 75 watt VRs), in future revisions of this this specification.

11.7 Power Efficiency

The target efficiency for VRDs that deliver greater than 10W is 92%; otherwise 75% is the target efficiency.

11.8 Power – Voltage Regulation Requirement Guideline

The following table summarizes the high-level power requirements for design of Zaius motherboard.

Table: High-Level Power Requirements

Rail Name	Rail Net	Quantity	Voltage	Current (each)	Notes
48V	P48V	1	54V	26Atdc/35Amax	Input to tray
12V	P12V	1	12.00V	50A	PCIe slots, fans, SSD's, HD
5V	P5V	1	5.00V	1.50A	HD
CPU Core	Vdd (core)	2	0.86V (0.6V-1.1V)	297Atdc/329.3Apk	300W TDP CPU
CPU Cache	Vcs (cache)	2	1.00V	11.6A	
CPU Nest	Vdn (nest)	2	0.86V	74.4A	
CPU I/O	Vio (I/O bus)	2	1.00V	21.0A	
CPU PLL	Avdd/Dvdd	2	1.50V	2.0A	
CPU STBY	Vsb	2	1.10V	1.0A	
CPU STBY	P3V3 (V3P3sb)	2	3.30V	Xxx mA	Pending. To be added later
DDR4 Memory	VDDQ (CPU Vddr included)	4	1.20V	94.2Atdc /104Apk	16GB DIMM, 8 slots per rail
DDR4 Memory	VTT Term	8	0.60V	1.14Atdc / 2Apk	Derived from VDDQ
DDR4 Memory	VPP	4	2.5V	9.5Atdc /12Apk	DIMMs
AST25X0 EC, E9235 SATA Controller, Renesas USB controller	P3V3_stby	1	3.30V	0.9A (0.2A+0.3A+0.4A)	

11.9 Barreleye G2 Hard Drive Cage Power

Hard drive backplane and expander board is powered from Fan power board independent of motherboard. More details on hard driver power will be added to this section in further revisions.
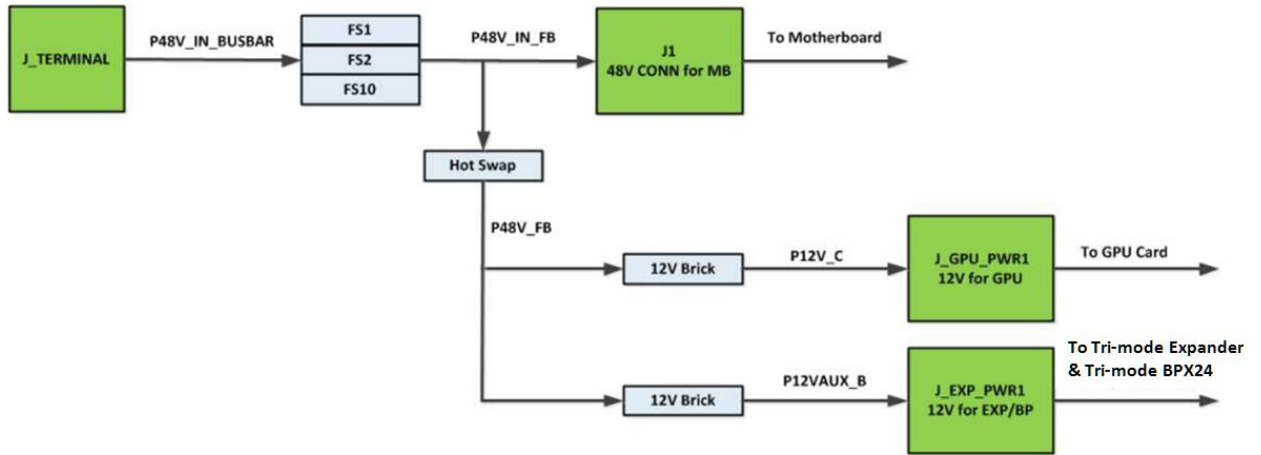
12 I/O System

12.1 PCIe Slot Connector

Zaius motherboard has 64 of the 84 lanes allocated as standard PCIe slot connectors and 16 lanes allocated for a OCP Mezz 2.0 connector as follows:

- 3 x16 PCIe slots
- 2 x8 PCIe slots
- 1 x16 OCP Mezz 2.0 connector (12mm baseboard stacking height)

Figure: 5 PCIe slots (PE0-PE4) / 1 Mezz Slot Placement on Motherboard and Mapping to Chassis Front (Zaius Sled and Barreleye G2 2OU 5xPCI Cage Front)
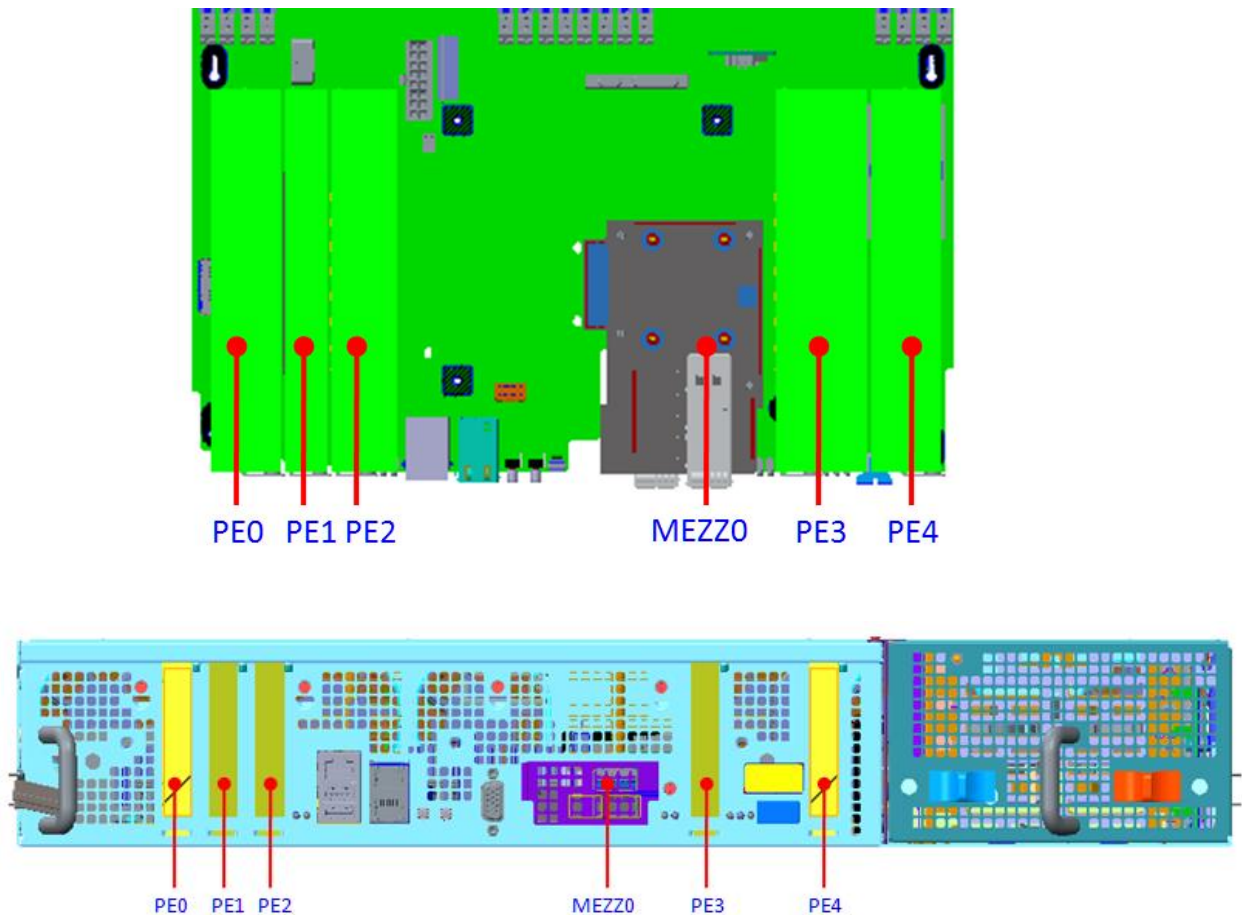
Table: 5 PCIe Slot (PE0-PE4) / 1 Mezz Slot Routing to Respective CPU Ports

(Table Also has Details on Card Form Factors in Each Slot)

PCIe Slot	Bus Width	Source	CPU Port	Speed	Bifurcation	CAPI Support	Supported Card Size	Card Length x Bottom Height x Top Height
PE0	x8	CPU0	PEC1	Gen4	-	-	Expanded-Slot	6.600"x0.570" x0.570"
PE1	x16	CPU0	PEC0	Gen4	-	Y	Single-Slot	6.600"x0.105" x0.570"
PE2	x16	CPU0	PEC2	Gen4	2 x8	Y	1.5-Slot	6.600"x0.105" x0.970"
PE3	x16	CPU1	PEC0	Gen4	-	Y	Double-Slot	6.600"x0.105" x1.370"
PE4	x8	CPU1	PEC1	Gen4	2 x8 or 1 x8+2 x4	-	Expanded-Slot	6.600"x0.570" x0.570"
MEZZ0	x16	CPU1	PEC2	Gen4	2 x8 or 1x8 + 2x4	Y	OCP Mezz 2.0	

12.2 NV-Link/OpenCAPI

Each processor supports 2 bricks (16 total lanes) of 25Gbp/s NVLink/OpenCAPI connections. Zaius motherboard routes the NV-Link/OpenCAPI lanes to two 37-pin connectors directly in front of each processor. For each processor, the "bottom" connector contains x8 lanes numbered 0-10, the "top" connector contains x8 lanes numbered 13-23. Control and clock sideband signals are routed to a separate SATA 7-pin form factor connector in front of each processor.

12.3 Network

Zaius motherboard front panel optionally provides 2 RJ45 gigabit Ethernet connections in a dual stack connector. Top Ethernet port connects to BCM5719A PCIe Ethernet. Bottom port connects to BMC-only BCM54612 PHY.

12.3.1 BMC-only Gigabit Ethernet (optional)

A Broadcom BCM54612 RGMII capable PHY and front panel RJ45 connector with LINK and ACT LEDs will be used to connect BMC port RGMII2. This Ethernet port is only usable by the BMC for management purposes and is not connected to the host CPUs.

12.3.2   BCM5719A PCIe Gigabit Ethernet LOM (optional)

A Broadcom BCM5719A PCIe network controller is used in an optionally stuffed LAN-on-motherboard (LOM) role. Port 0 of the controller connects to a front panel RJ45 connector with LINK and ACT LEDs, the other ports are unused. The 4X PCIe lanes for the LOM are connected to lanes 8,9,10,11 of the LOM+VGA connector (optional).

NCSI signals of the BCM5719A are be connected to the BMC as specified in the block diagram.

12.3.3   NC-SI

Zaius provides 3 sources for high-speed NC-SI/RMII remote management. All NC-SI sources are connected to BMC RMII1 port using an on-board mux that is controllable by the BMC. Multi-drop connections and/or hardware arbitration is not supported. BMC firmware is responsible for enumerating all NC-SI sources during initialization to detect network devices and assigning priority order as follows:
- HDMI connector with custom pinout
- BCM5719A LOM (optional)
- OCP Mezzanine 2.0 slot

12.4   USB

Zaius has two USB ports on a stacked (with RJ45 serial) connector on the front panel.

The top USB port is connected to the Renesas USB controller and routed to support USB 3.0 operation (5Gbps). The bottom USB port is connected to the USB 2.0 host port of the BMC.

Zaius will also support USB on each PCIe slot connected to the 7-port USB hub downstream of the host controller. USB1.1 will be supported on these interfaces.

Overcurrent protection is provided for the USB ports.

12.5   SATA

Marvell 88SE9235 4 port SATA controller is used for SATA support. This controller is wired to a PCIe x2 of CPU0 as showed in block diagram.
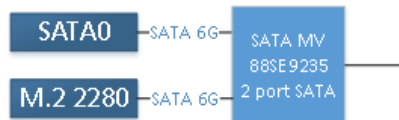
SATA0 port will connect to a 22-pin header supporting both data and power (Amphenol G16CE41210W3EU or equivalent). Standard signal and power pinouts for SATA are used on this connector. See table below. SATA1 port will connect to a M.2 2280 form factor connector (M-keyed).

Marvell 88SE9235 I2C shall be connected to the BMC via appropriate I2C switches.

Table: SATA Connector Pinout

| Pin Number	Net	Function

S1	GND	Tied directly to ground
S2	TX+	Differential Transmit Signal Positive
S3	TX-	Differential Transmit Signal Negative
S4	GND	Tied directly to ground
S5	RX-	Differential Receive Signal Negative
S6	RX+	Differential Receive Signal Positive
S7	GND	Tied directly to ground
		Mechanical Key
P1	NC	No need to supply 3.3V power
P2	NC	No need to supply 3.3V power
P3	NC	No need to supply 3.3V power
P4	GND	Tied directly to ground
P5	GND	Tied directly to ground
P6	GND	Tied directly to ground - SATA present
P7	VDD_5V	Main logic power rail for hard drives
P8	VDD_5V	Main logic power rail for hard drives
P9	VDD_5V	Main logic power rail for hard drives
P10	GND	Tied directly to ground
P11	GND	Tied directly to ground
P12	GND	Tied directly to ground
P13	VDD_12V_PER	Spindle power rail for hard drives
P14	VDD_12V_PER	Spindle power rail for hard drives

P15	VDD_12V_PER	Spindle power rail for hard drives

Signals are to be routed to support operation up to 6Gb/s.

12.6 Buttons and LEDs:

Figure: LEDs and Buttons in the Front Panel of Barreleye G2 Tray
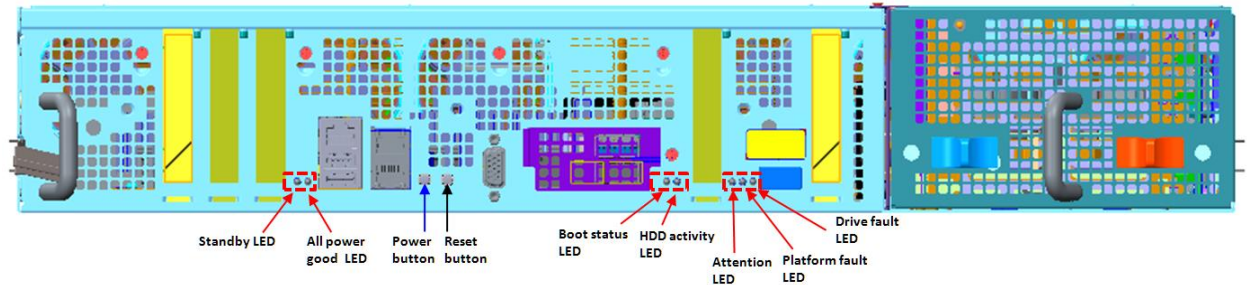
12.6.1 Buttons

A reset button (black) and a power button (blue) are mounted at the front edge of the Motherboard. Power Button is on the left of the Reset button. All devices are capable of being manually reset to a known state via the Reset button. The power button is pressed for ~4 seconds to power off the server. When the system is powered off a press and release of the power button would power the server on. More details on exact timing of power and reset button press and subsequent behavior will be added in the next revisions of this document as it is refined.

12.6.2 LEDs

These LEDs are located on the front edge of the PCB and exposed to the front panel. They will be clearly labeled on the silkscreen.

On front panel of the tray LEDs are listed in the preferred left-to-right order as seen in the below front panel picture:
- Blue LED: Indicates standby power good.
- Green LED: Indicates All Power Good (from Sequencer).
- Green LED: System Boot Status (driven from BMC GPIO)
- Yellow LED: Indicates HDD activity. This is the GPIO0 signal from the Marvell 88SE9235 for SATA drive activity.
- Yellow LED: Attention (machine locator, driven from BMC GPIO) - this LED should be placed away from the HDD activity LED, either on the left or right side of the mother board.
- Red LED: Platform fault. Driven from BMC GPIO.
- Red LED: Onboard drive fault. Driven from BMC GPIO

12.7 Fan Connector & LEDs

12.7.1   Barreleye G2 Fans

12.7.1.1   *Barreleye G2 Fan Connectors*

In Barreleye G2, fan connectors are present on Fan / Power board.

Figure: Fan / Power Board and Cable in Barreleye G2 Chassis

12.7.1.2   *Long FAN cable*

12.7.1.3   *Short FAN cable*
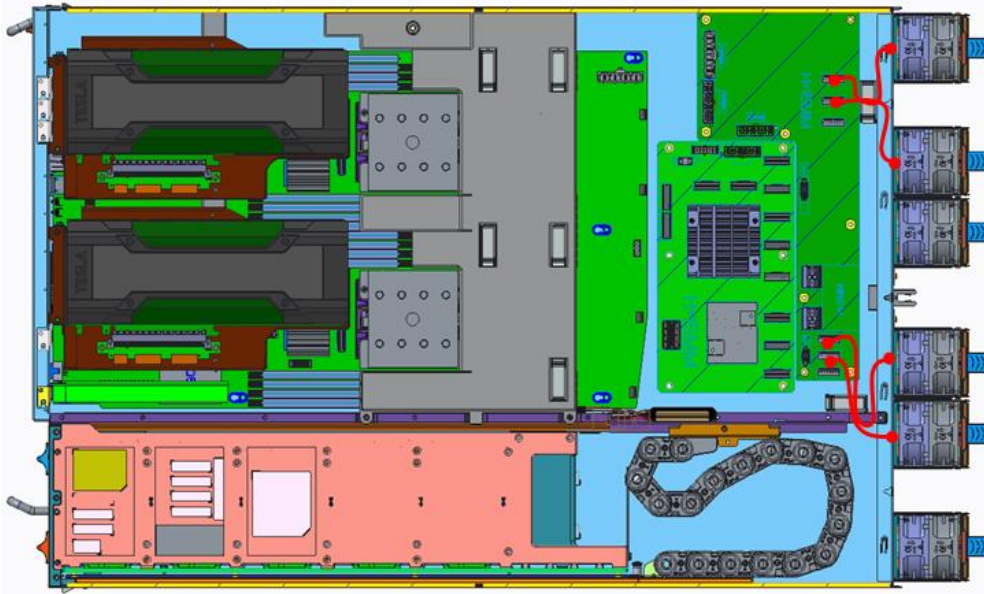
Barreleye G2 Fan LEDs

Each of 6 fan modules in Barreleye G2 Chassis have 2 LEDs each with following behavior.

Fan LED Behavior			
LED Color	Function	LED Pattern	Comment
Blue	Fan normal operation	Always light	Bi-color LED and integrated Fan modules. It will light Red for several seconds when the system is just powered on, it will change to blue when the fan duty exceed 30%.
Red	Fan fault, duty cycle < 30%	Always light	

Figure: 3D Rendering of Barreleye G2 Fans and Rear View Indicating 2 LEDs on Each of the 6 Fans.
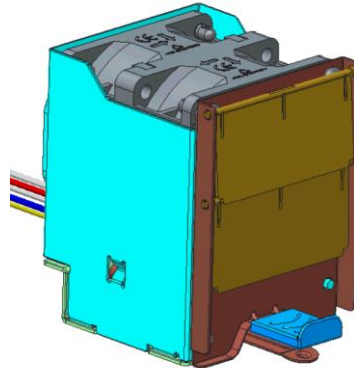
12.7.2   Zaius Fan Connectors

Zaius motherboard has 4 4-pin fan connectors capable of supporting 12V fans. The pinout of the fan connectors is as below. System fan control and monitoring is provided by the BMC. Note this pinout does NOT follow the standard "4-wire PWM fan" specification.

Pin	Function

1	Control (PWM)
2	Sense (Tach)
3	+12V
4	GND

12.8 UART Connector

12.8.1 System UART

The primary system (host) serial port is connected to UART1 of the BMC and routed to a stacked RJ45+USB connector (Foxconn UB11123-YC0F-4F or similar) on the front panel. Pinout for the RJ45 port is to follow the "Cisco" pinout variant. Only TX/RX/GND signals should be connected, the modem control signals are no-connect. Signal levels are to follow RS-232 standard (+12V/-12V).

Table: RJ45 serial pinout

Signal	Pin
UART0_RX	3
GND	4
GND	5
UART0_TX	6

12.8.2 BMC Debug UART

BMC debug console UART5 should be connected to a 3pin 2.54mm header near the front of the board with the following pinout. Signal levels are to follow the RS-232 standard (+12V/-12V):

Table: BMC debug serial header pinout

Signal	Pin
UART5_TX	1
GND	2
UART5_RX	3

13 Mechanical

13.1 Barreleye G2 – 2OU Mechanical

13.1.1 Barreleye G2 Chassis

The 2 OU chassis has the dimensions, 537 x 801 x 92.3mm.

13.1.2 Barreleye G2 Top View

Barreleye G2 supports 24 Hot-Pluggable 2.5" SAS hard drives/ 20 NVMe drives and Fan modules. There are 4 main boards in the system.

They are Motherboard, Tri-mode Expander board, Fan / Power Distribution Board and Tri-mode HDD Back Plane.

Figure: Top View [Barreleye G2 GPU SKU] Diagram
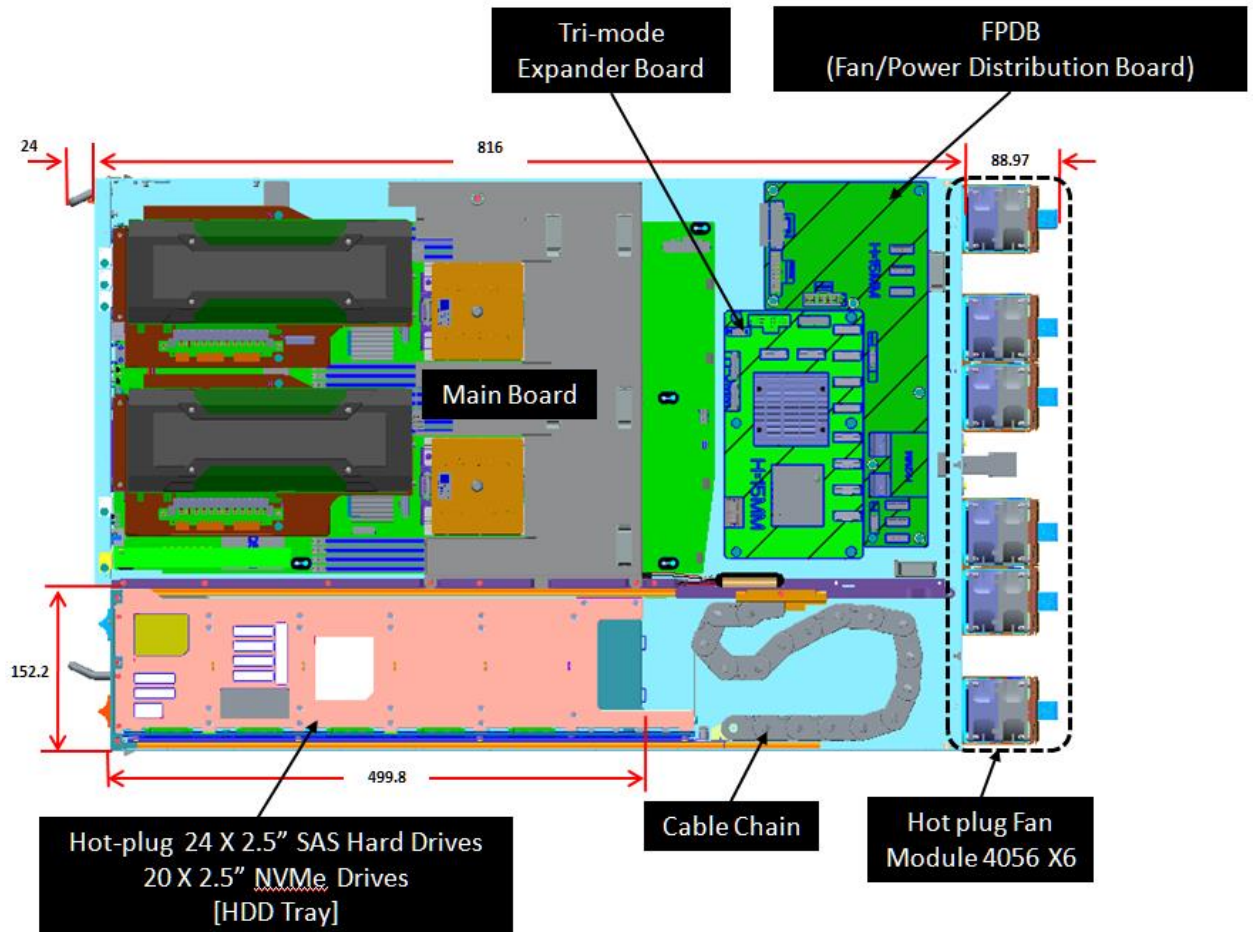
Figure: Top View - System Infrastructure [5* PCI-e Card SKU] Diagram
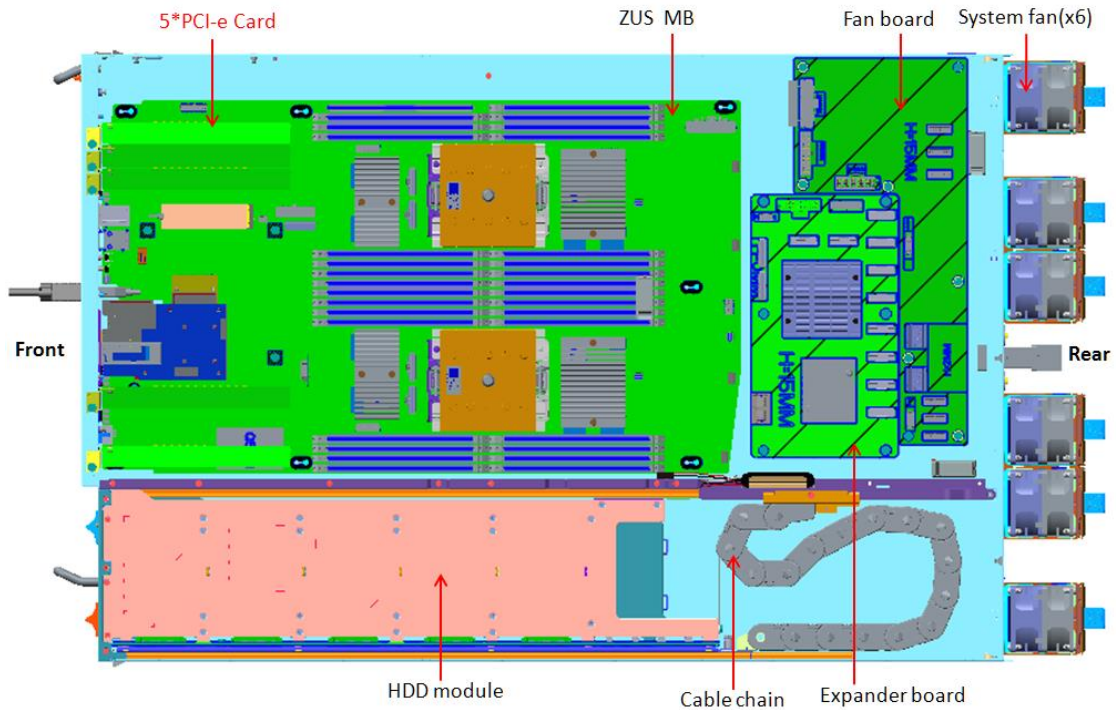
Figure: 3D Barreleye G2 Rendering [5* PCI-e Card SKU] Diagram - In a tray
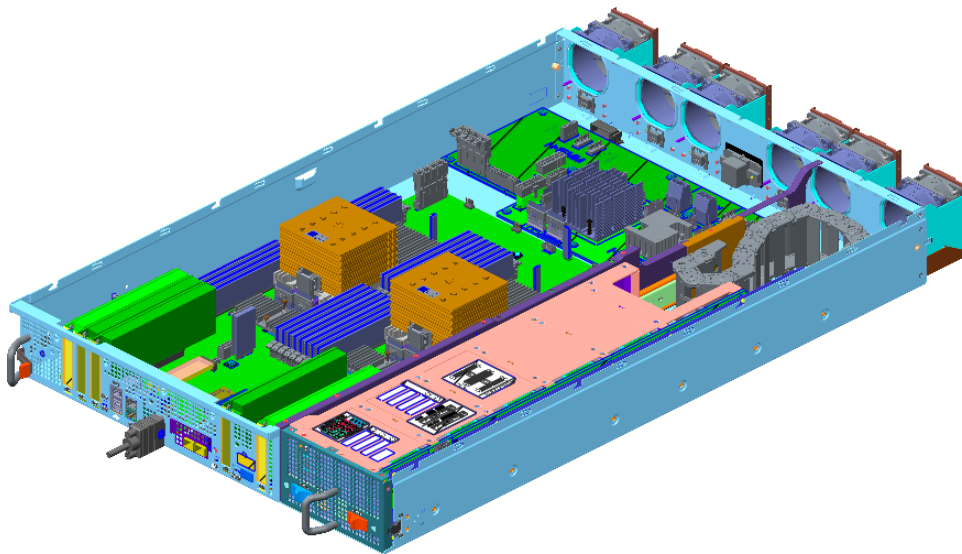
13.1.3 Barreleye G2 Front View

Barreleye supports two 2 x8 PCIe Gen4 3 X16 PCIe and 1 MEZ Card. The I/O connectors are

located on the front. There is one HDD Tray on the right which contains 24pcs Hot-Pluggable 2.5" HDD drives.

Figure: Front View
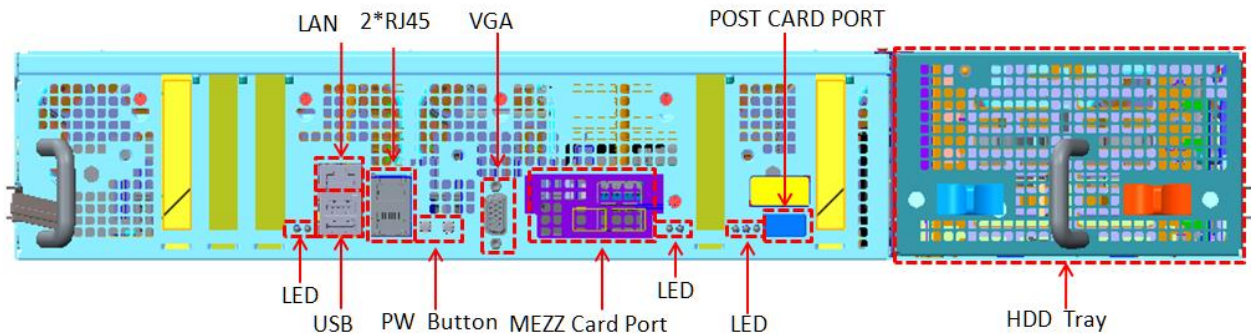
13.1.4   Barreleye G2 Rear View

There is one Bus bar clip and 6 Hot-pluggable Fan Modules on the rear wall.

Figure: Rear View
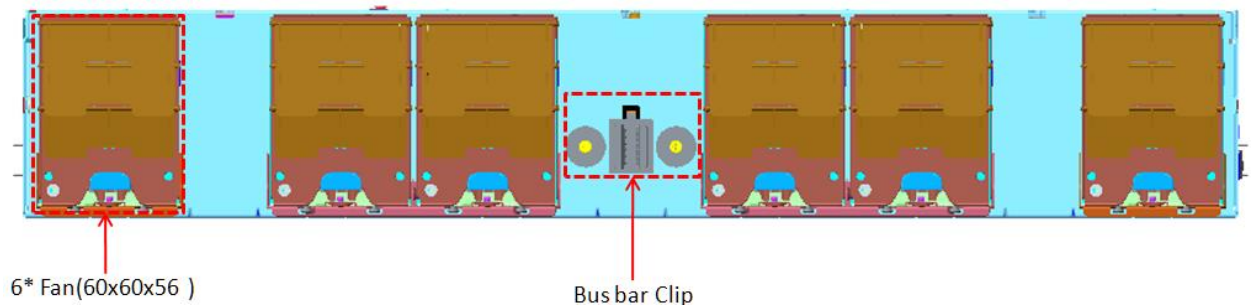
13.1.5   Barreleye G2 / Zaius Mother Board

The dimensions of Barreleye G2's Main board / Zaius Motherboard are 564x330mm. It supports two Power 9 LaGrange CPUs and 32 DIMMs.
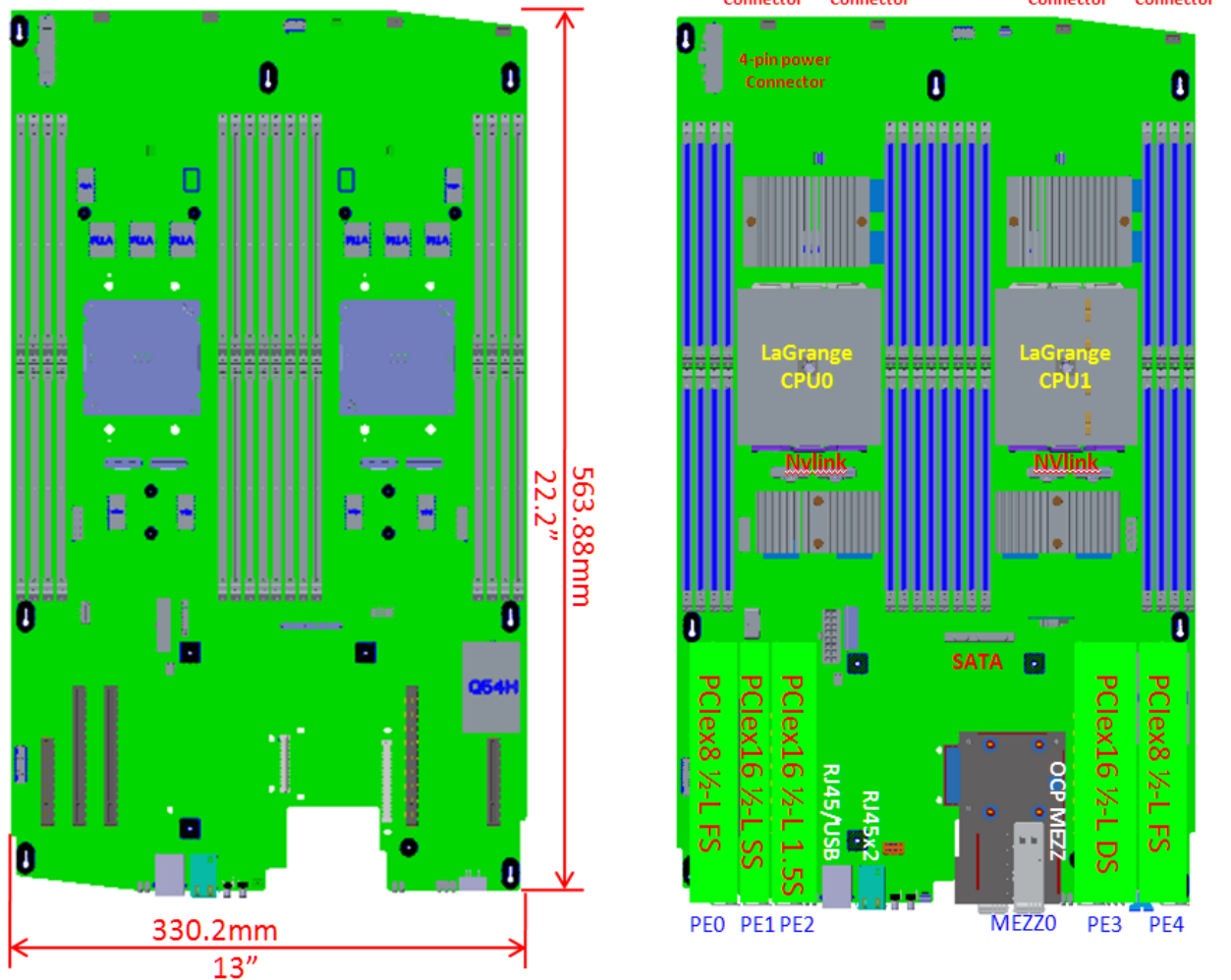
Figure: Front Isometric View of Motherboard
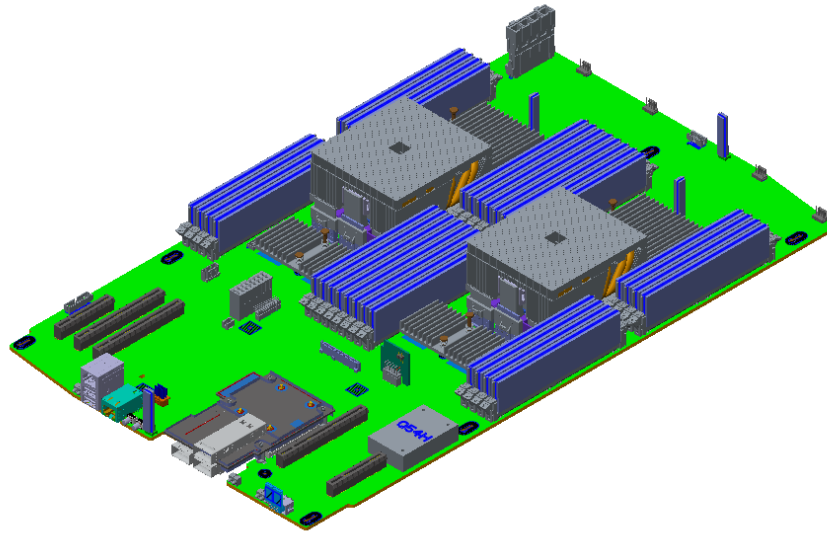
13.1.6 Barreleye G2 FPDB (Fan/Power Distribution Board)

FPDB provides power for 6 fans, Tri-mode Expander board, Tri-mode HDD Back Plane, and GPU using with two 48V- to -12V bricks.
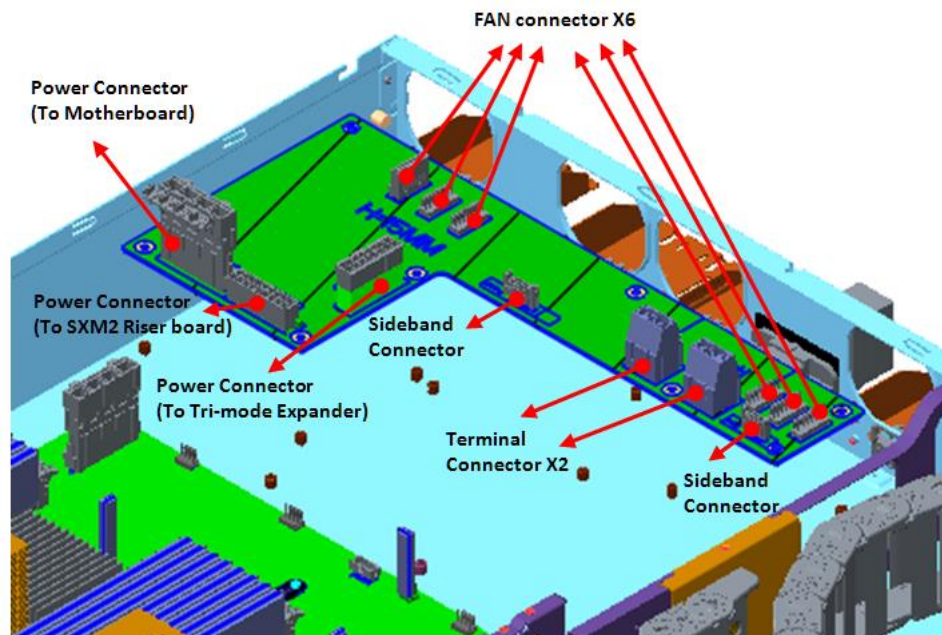
13.1.7   Barreleye G2 Tri-mode Expander Board

This board conducts the SAS/PCIe signals from Tri-mode adapter to Tri-mode HDD BP through the Slim SAS cables.
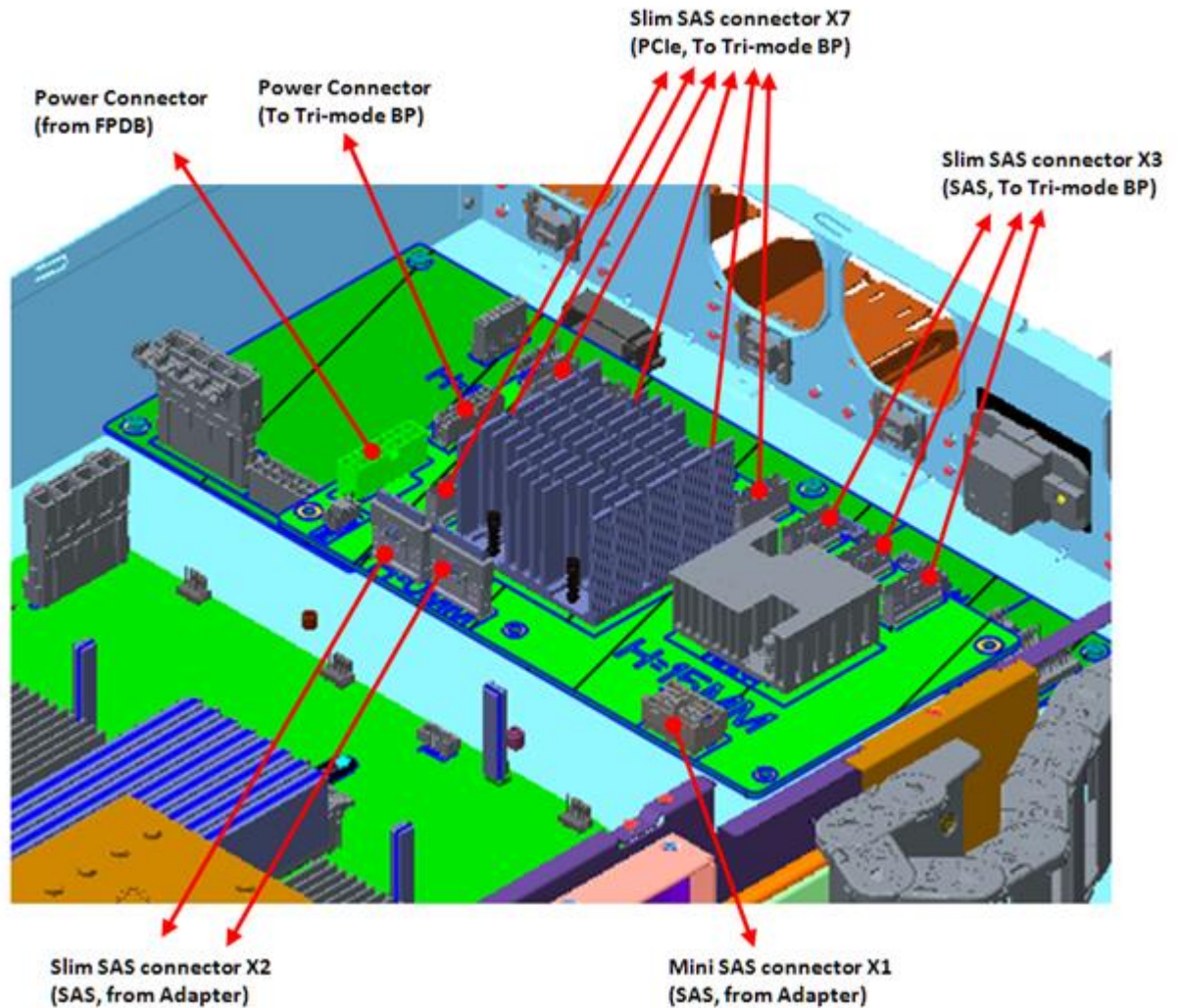
13.1.8   Barreleye G2 OCP MEZZ

The OCP-MEZZ Card with 2 configurations and how they get exposed to the front of chassis
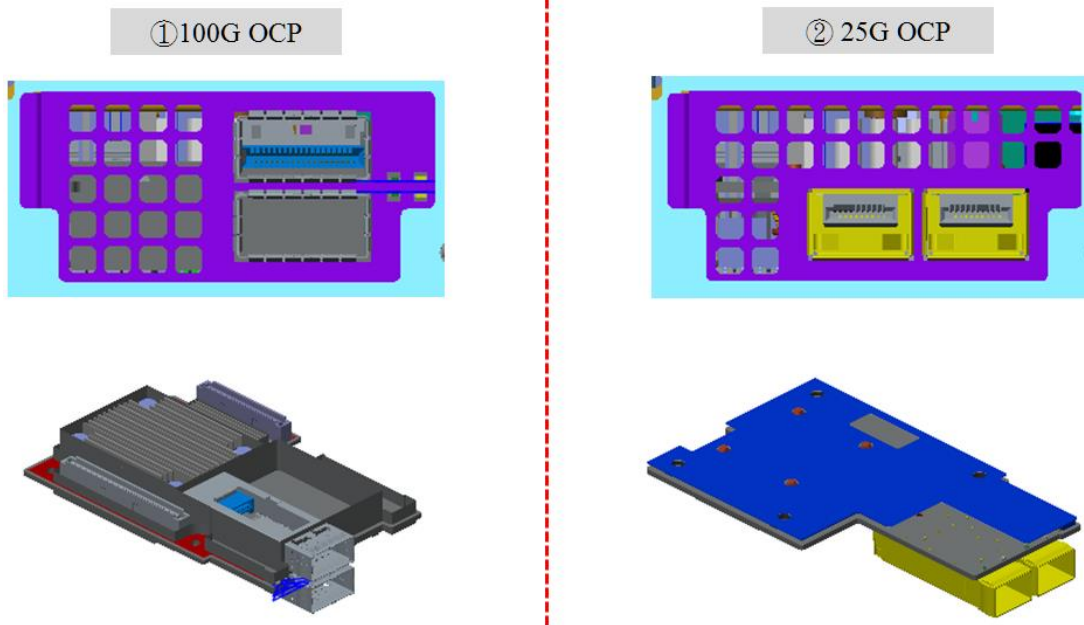
13.1.9 Barreleye G2 Tri-mode Back Plane x 24
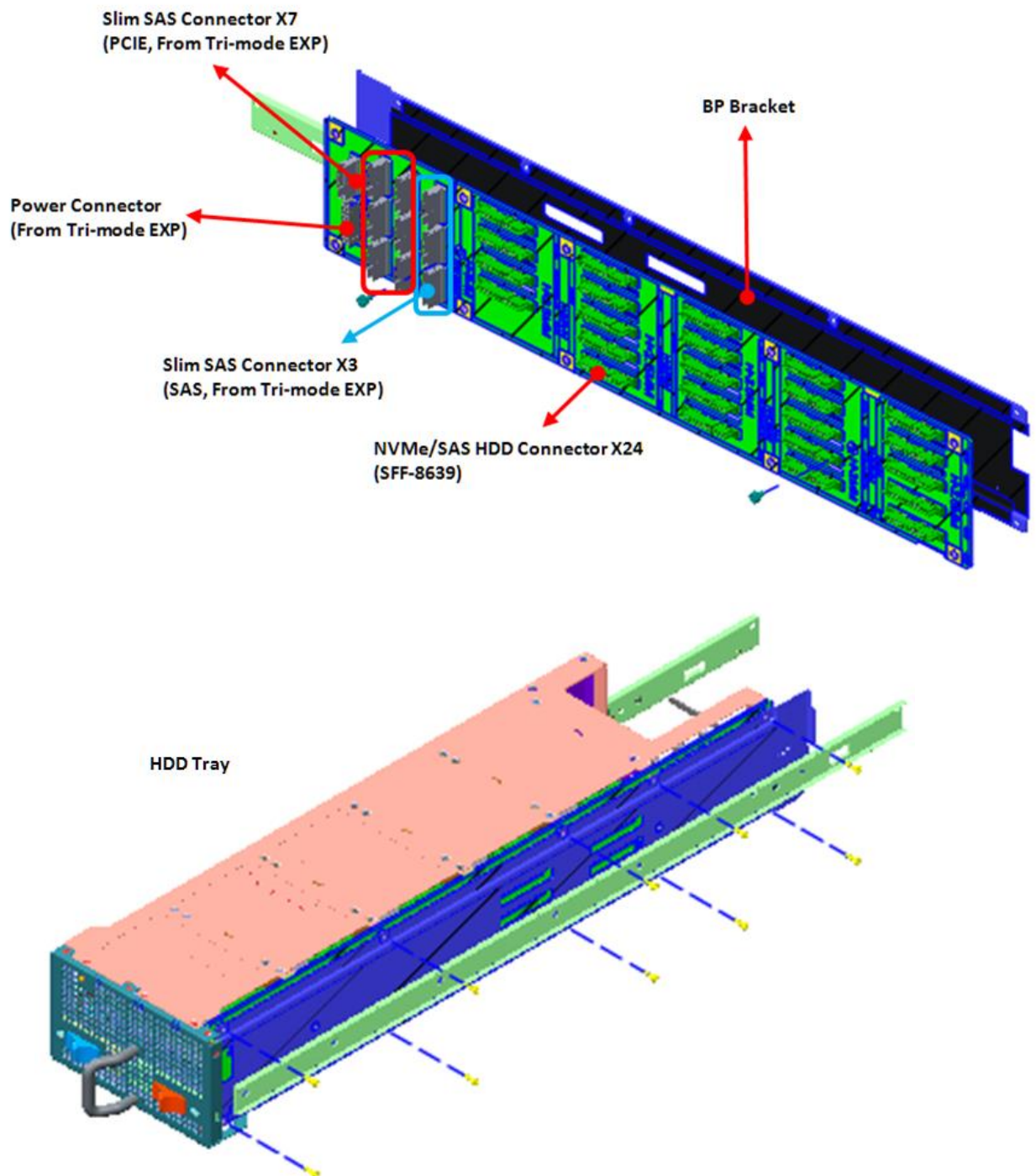
13.1.10 Barreleye G2 Hard Drive Tray & Installation

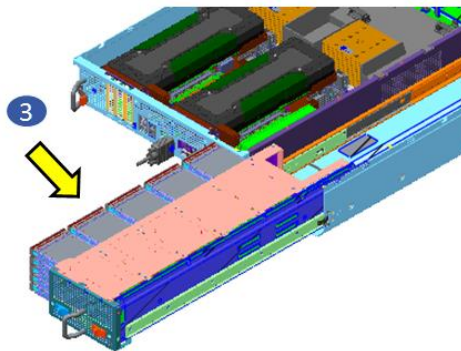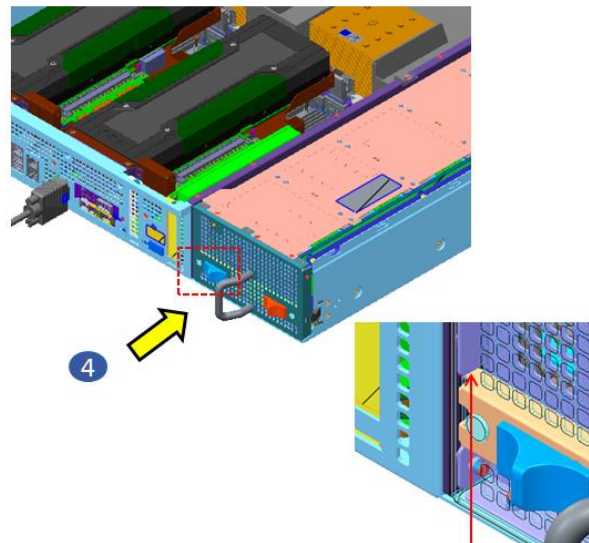The dimension of Hard Drive Tray is 501mm (L) x 151.9mm (W) x 88.9mm (H).

HDD Tray Installation
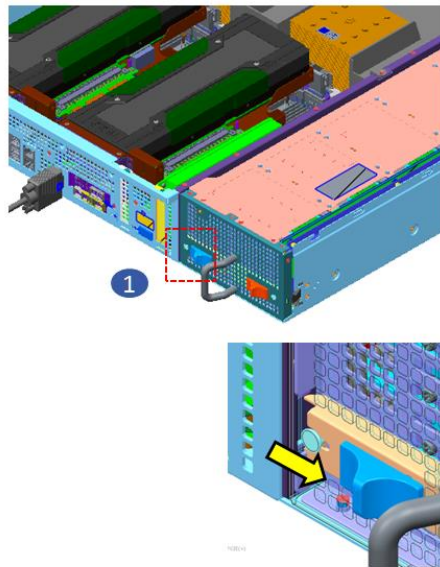
1. Pull the HDD tray latch ,unlock the HDD tray.
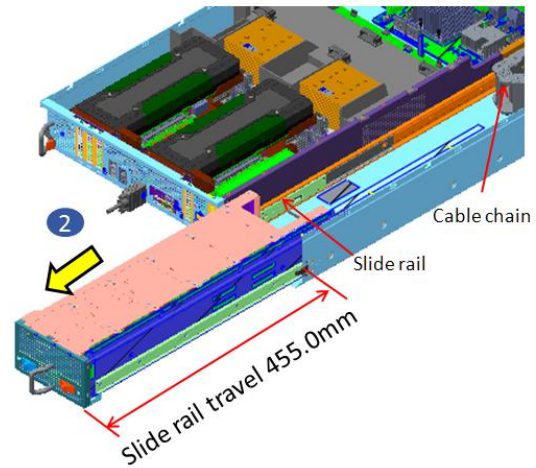
2. Pull out the HDD tray .
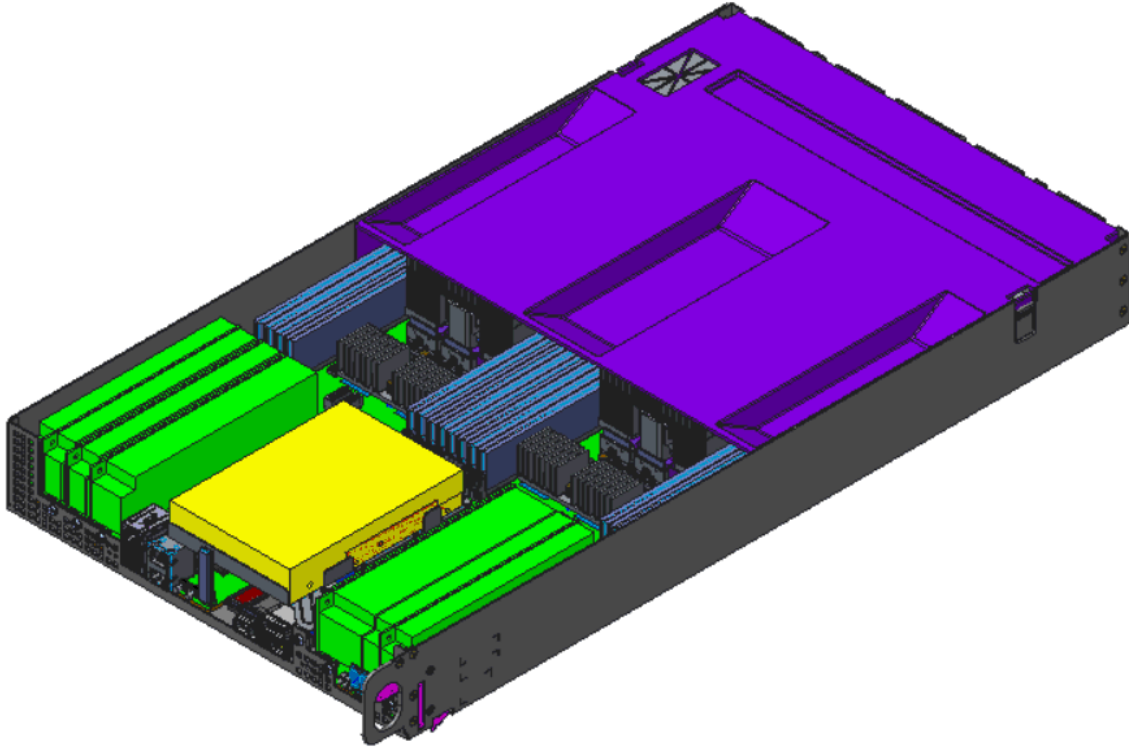
3. Insert 24 HDD into HDD tray.

4. Slide the HDD tray into chassis .The tray is locked to partition by latch.

13.2 Zaius Sled – 2.6" tall

The Zaius sled fits the motherboard and 4 rear 60mm fans. The dimensions of the sled are approximately 340x610x66mm (13.4"x24"x2.6"). It is intended for use in the 1.5OU Open Rack Deployment Shelf.

Figure: Front Isometric View of Zaius Sled

13.2.1 Zaius Sled in 1.5OU Deployment Shelf

The Zaius 1.5OU deployment shelf is 537x660x72mm (21"x26"x2.8"), and fits 1 Zaius sled with a 6.4" wide accessory space to the right of the sled. The shelf latches the sled into position and connects to the rack vertical bus bar. The shelf connects to the rear vertical bus bar provided by the rack and provides a horizontal 48V bus bar in the rear to power the Zaius sled and any additional attached devices in the same shelf.

Figure: Zaius Sled in 1.5OU Deployment Shelf.
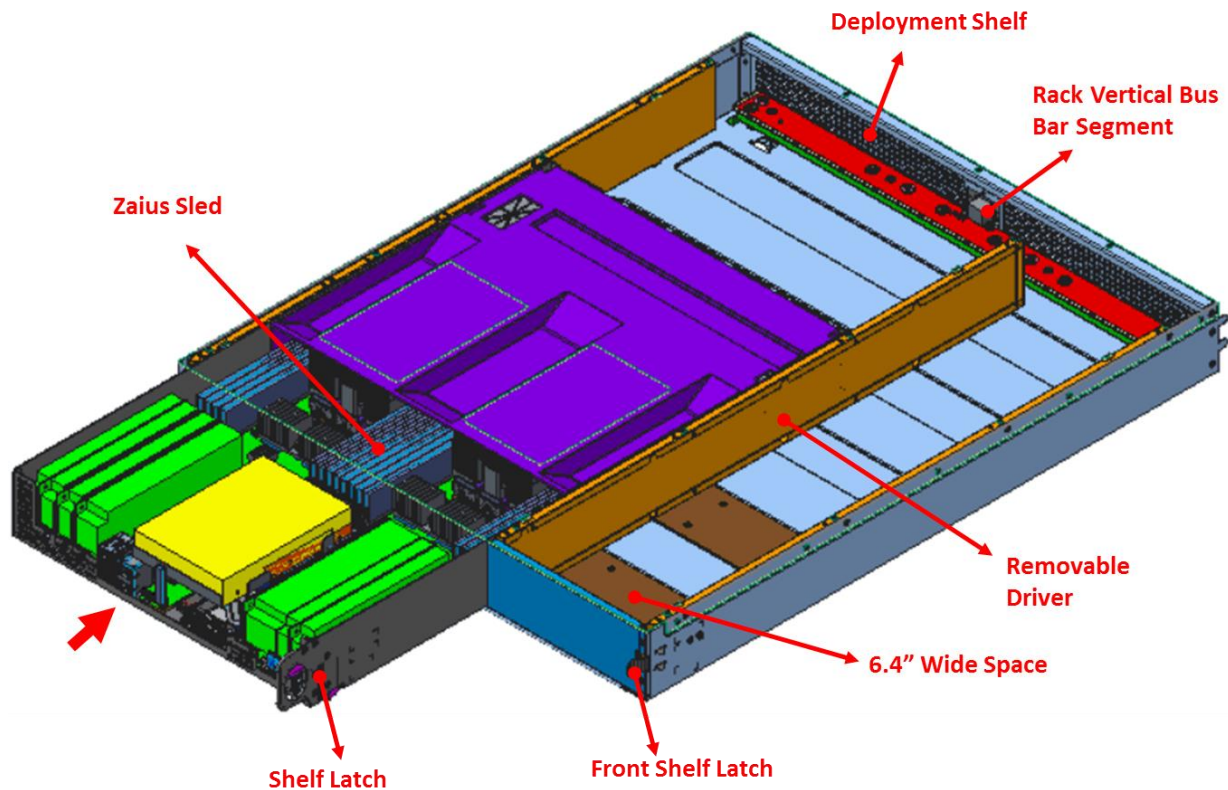
13.3 Rack and Sled Interaction

Rack for Barreleye G2 / Zaius Chassis is standard 48V OCP Rack V2. The rack will follow the Open Rack Specification shown here:

http://files.opencompute.org/oc/public.php?service=files&t=8d2264171f72aa8a86d0e08a3504c740

Rack and power shelf are still under development. Details will be shared in upcoming revisions of this document.
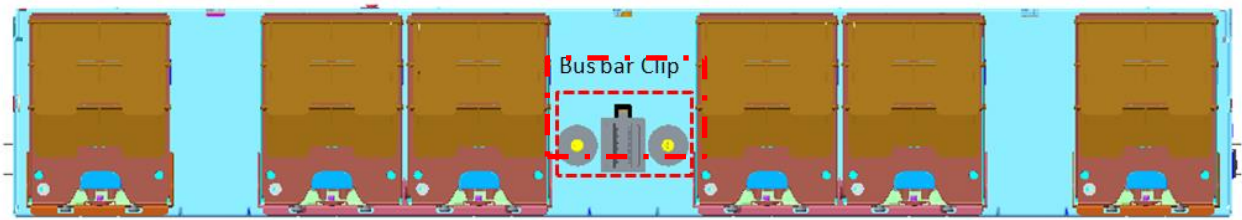
14 Power Distribution from Bus Bar

Power connections from bus bar to mother board might vary based on different chassis implementations of Zaius motherboard.

14.1 Barreleye G2 Chassis

Barreleye G2 Chassis receives its power via a single 48V bus bar clip located at the rear of the server.

Figure: Barreleye G2 Chassis Rear View

14.1.1 Barreleye G2 FPDB (Fan/Power Distribution Board)

Fan /Power distribution board terminal connectors are connected to bus bar clip and provide power for fans, Tri-mode Expander board, HDD Back Plane and GPU from two 48V-to-12V bricks.
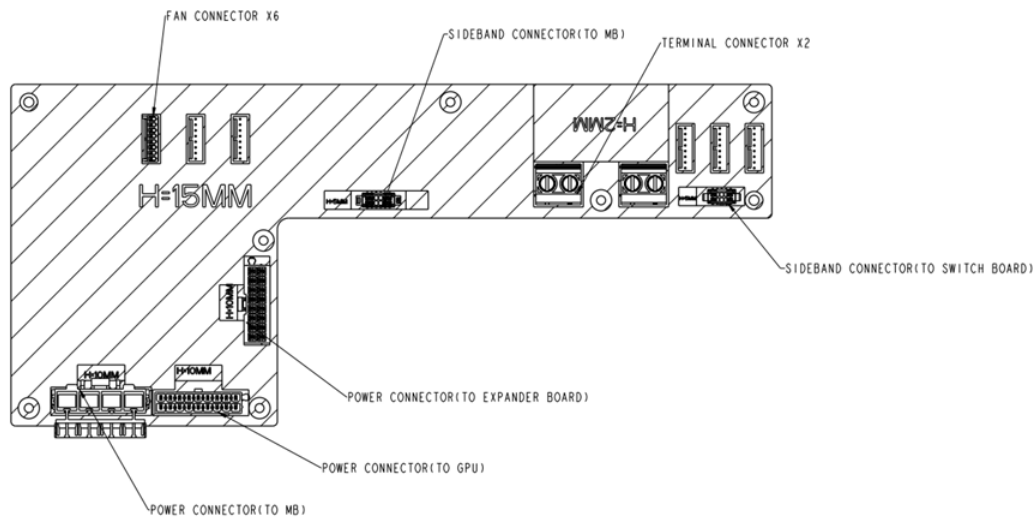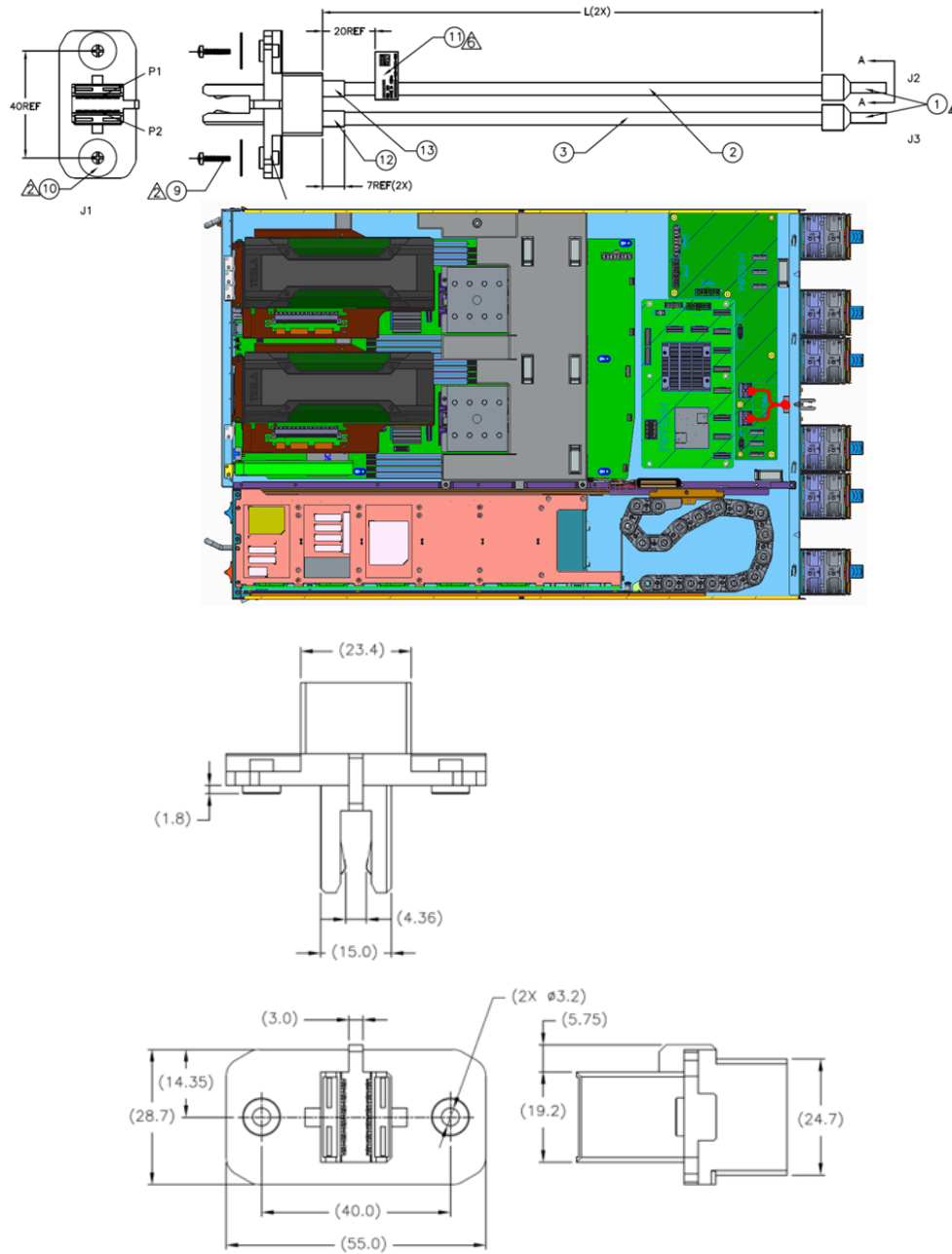
Figure: Barreleye G2 Sled - Cable Connecting Bus Bar Connector to Power / Fan Board

14.2 Zaius Sled Bus Bar Connection

Zaius sled uses a horizontal bus bar connector that connects to the Zaius 1.5OU deployment shelf and allows the tray to be placed anywhere along the length of the horizontal bus bar contained within each deployment shelf.

Figure: Zaius Sled Horizontal Bus Bar Connector
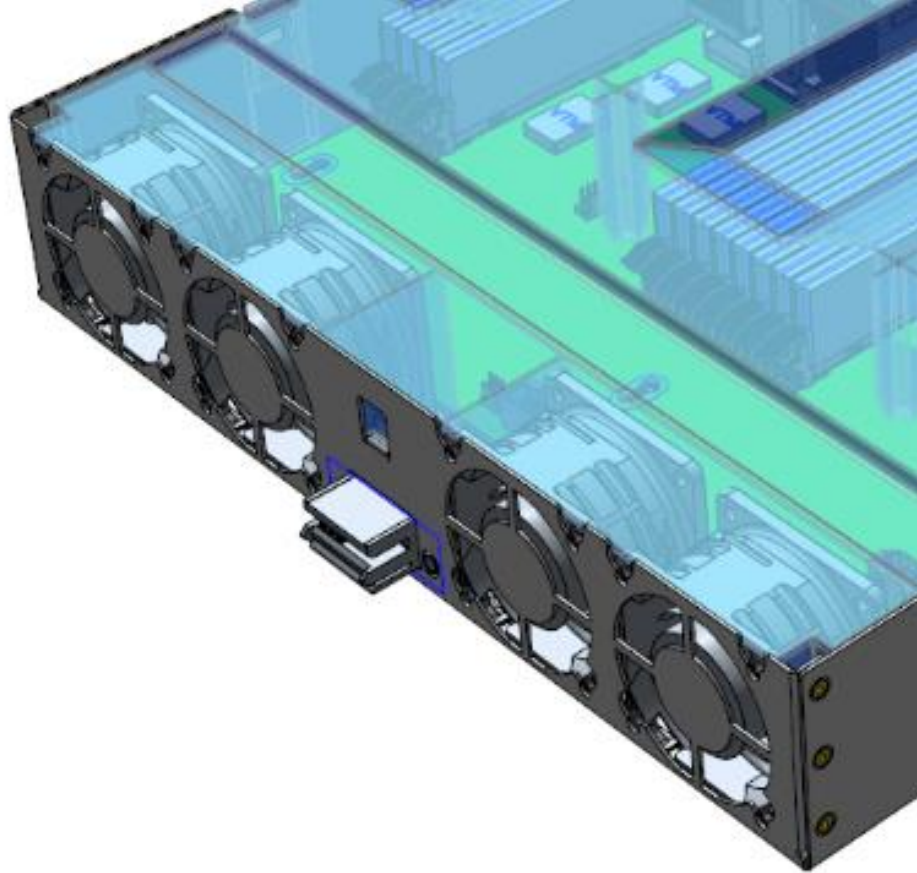
14.2.1 Zaius Sled/Shelf Connection Detail Views
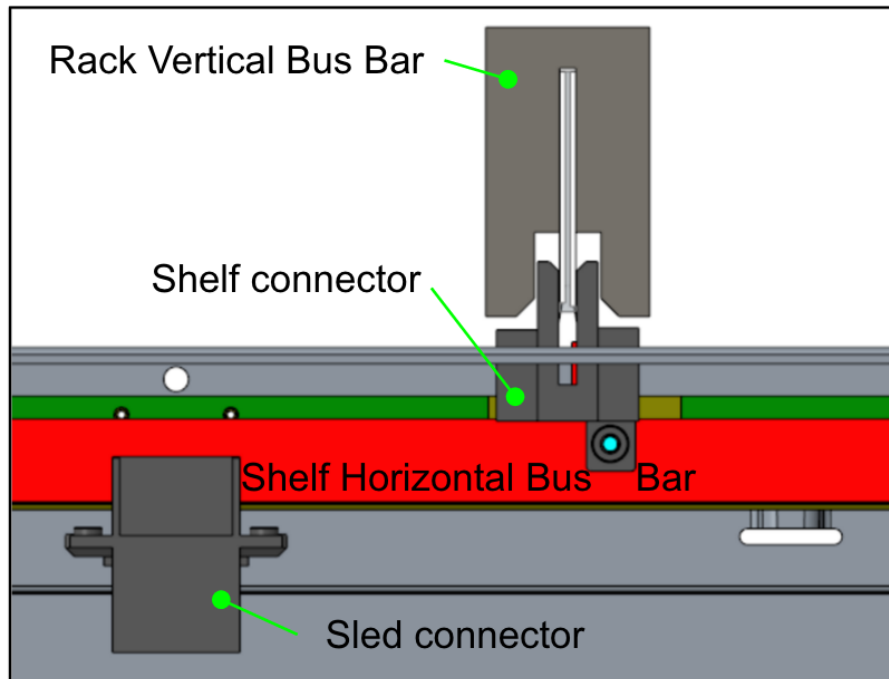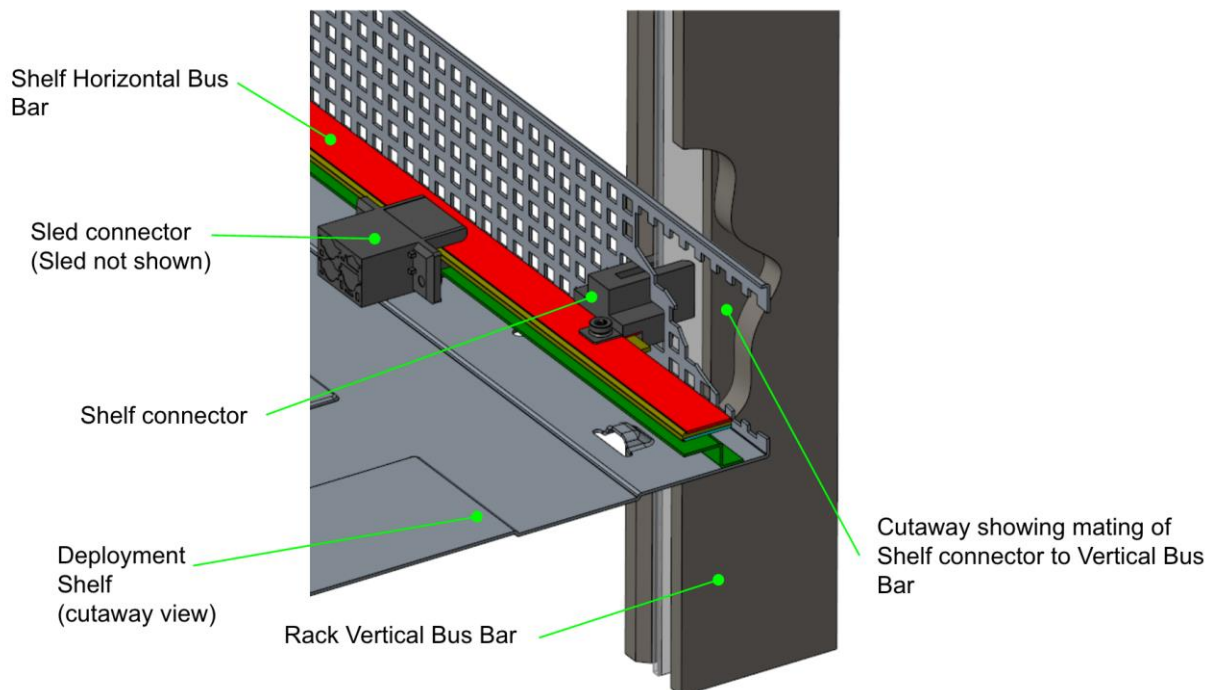
Figure: Sled/Shelf Bus Bar Top View

Figure: Tray/Shelf Bus Bar Isometric Cutaway View

14.3 Motherboard Power Connector

Motherboard uses an on-board input power connector to receive 48V on the rear of the tray. For

Barreleye G2 this input would come from Fan Board, for Zaius the cable directly attaches to the rear bus bar connector. This connector is a latching 4 pin vertical Molex MiniFit Sr connector supporting 40A@48VDC.

14.4 Power Distribution on Motherboard:

Further details on how bus bar clip is wired to the Zaius motherboard, max power rating supported by the server and internal distribution of power on the motherboard are in the "Motherboard Power System" Section.
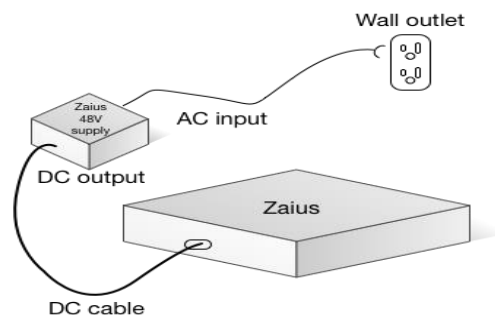
15 48V Lunch Box

15.1 48V Lunch Box Overview

The 48V Lunch Box provides DC input power for server when it is operated in a standalone fashion. Standalone use cases include:
- on a bench for bring up/debug
- on a bench or engineer's desk for evaluation or code development
- Chamber testing of a single unit

The 48V Lunch Box is intended to be a convenient way to power server without having to place it in a rack.

15.2 Objectives

The 48V Lunch Box must:
- Be safe to use in a lab environment with no expose high voltage or high current contacts
- Be flexible in its placement on a bench for those who are evaluating or doing debug
- Not impede airflow if this is important for testing and other needs
- Have a minimum EMI footprint to allow testing of a single unit in the lab
- Use off-the-shelf components where possible (such as the rectifier)
- Support AC cabling to different AC outlets/voltage

15.3 Zaius 48V Lunch Box Interfaces

15.3.1 AC Connector

The Zaius 48V Lunch Box supports an IEC320 C15 connector to connect to a wide range of AC outlets, at the maximum power of Zaius (around 1700W).

15.3.2 AC Input Cable

Different AC cables are supported to allow for different use cases, further details will be provided in future revisions of the spec.

15.3.3 Zaius 48V Lunch Box Power Supply Modules (e.g. Rectifiers)

The rectifier supports a minimum of 1700W at low line (~110VAC) to enable the maximum flexibility.

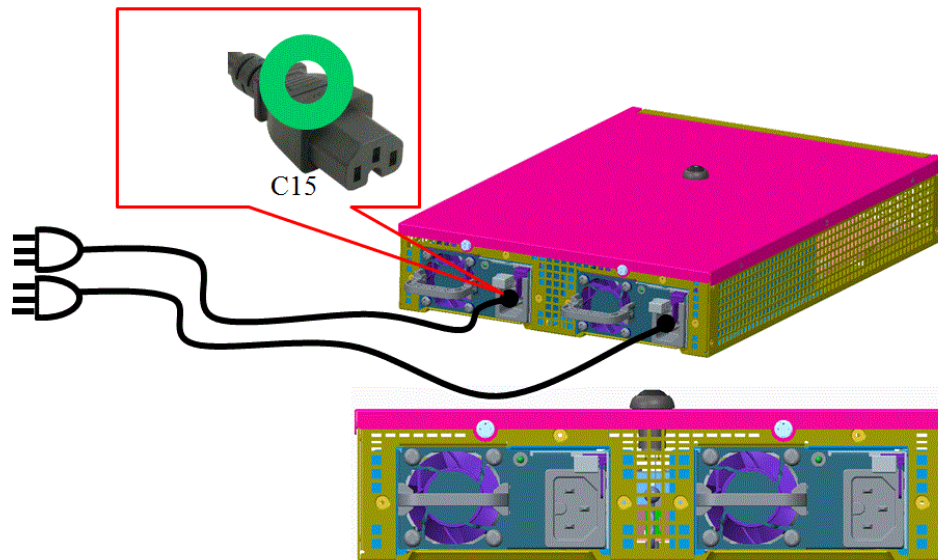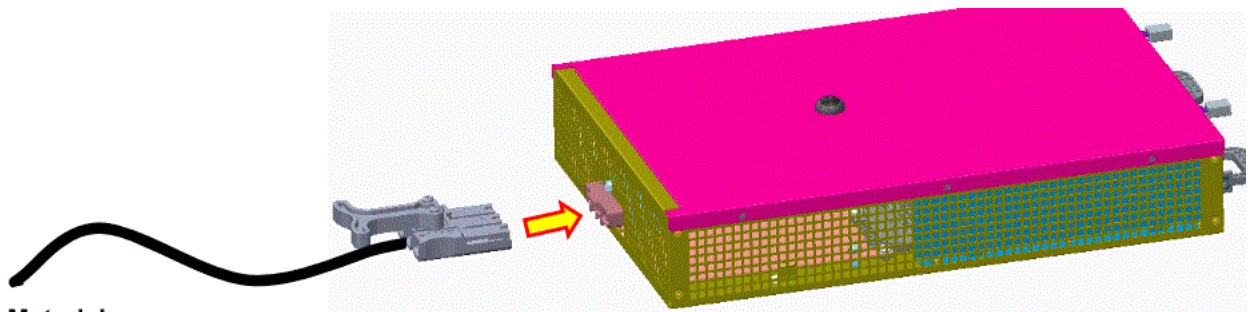**Figure: 3D Rendering of 48V Lunchbox Connected to AC Outlet**
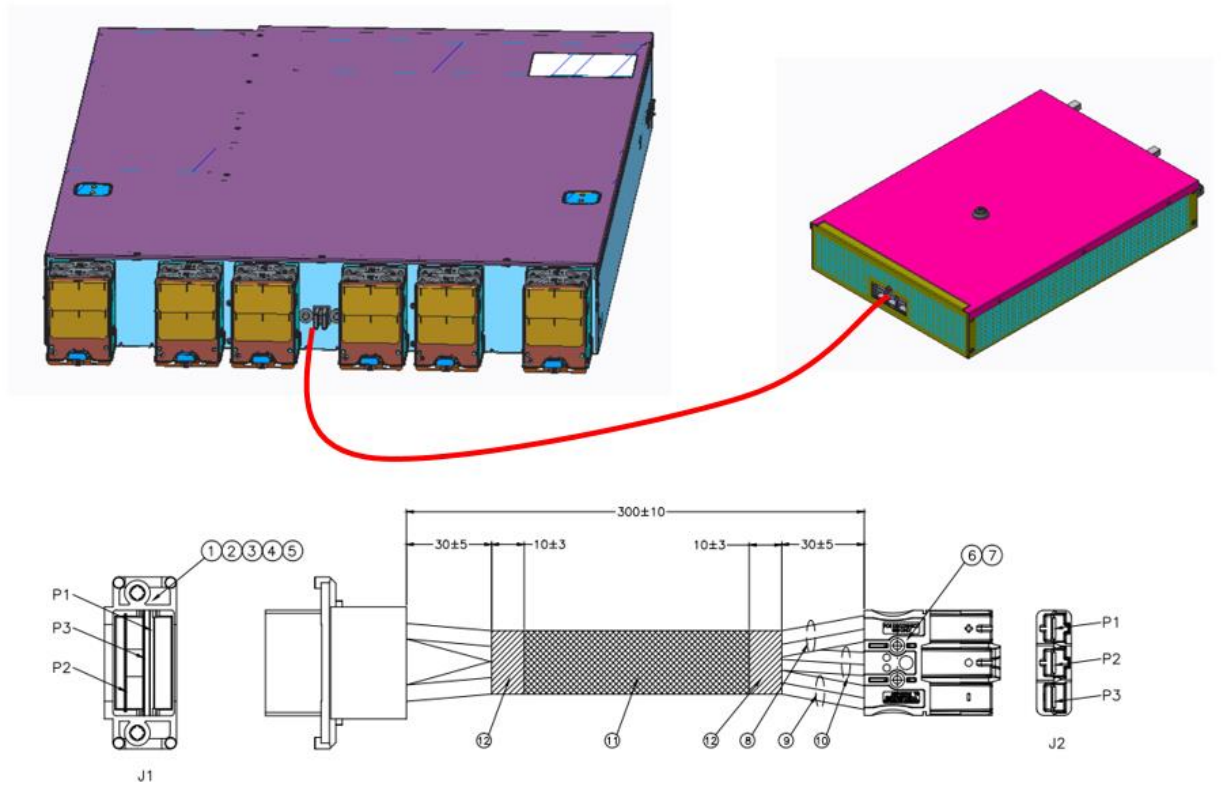

C15

Figure: 3D Rendering of 48V Lunch Box Connected to Server Power Cable

Material:
Power cable P/N: L02WH993-SD-R

Figure: How Lunchbox Connects to Server Chassis / Sled via Cable (Barreleye G2 2OU Example)

16 Regulatory & Safety Requirements

The entire board is RoHS-6 compliant.

Basic Compliance Requirements:

16.1 Safety

The equipment must meet all applicable safety requirements and certifications when operating under maximum normal load conditions. Applicable standards may include the following:

- UL/CSA/IEC/EN 60950-1
- UL/CSA/IEC/EN 62368-1

16.2 EMC

The equipment must meet the following requirements when operating under typical load conditions and with all ports fully loaded.

16.2.1 Emissions

6dB margin from the Class A limit is required for all emission test, both radiated emission and conducted emission. When the EUT is DC powered, DC line conducted emission test is required.

Primary EMC Standards apply to emission test include, but not limited to
- FCC Part 15, Subpart B
- EN 55022: 2010 / CISPR 22: 2008 (Modified)
- EN 55032: 2012 / CISPR 32: 2012 (Modified) - Effective 05/03/2017
- EN61000-3-2: 2006/A1: 2009/A2: 2009
- EN61000-3-3: 2008

For DC power related testing, when applicable GR 1089 / GR 3160 may be referenced.

16.2.2 Immunity

Primary EMC Standards apply to immunity test include, but not limited to
- EN 55024: 2010 / CISPR 24: 2010 (Modified)
- CISPR 35: 2014 (current publication: CISPR/I/463/FDIS 2013-12)

Each individual basic standard for immunity test has its specific passing requirement as illustrated below. When the EUT is DC powered, immunity test involves disturbance applied to power line apply to the DC input power.
- EN61000-4-2 Electrostatic Discharge Immunity (6kV contact, 8kV air)
- EN61000-4-3 Radiated Immunity [> 10V/m]
- EN61000-4-4 Electrical Fast Transient Immunity (1kV power (AC), 0.5kV signal)
- EN61000-4-5 Surge AC Port (2kV CM, 1kV DM)
- EN61000-4-5 Surge Signal Port (2KV CM, 1KVDM)
- EN61000-4-5 Surge DC Port (0.5kVCM, 0.5KVDM)
- EN61000-4-6 Immunity to Conducted Disturbances [> 10V rms]
- EN61000-4-8 Power Frequency Magnetic Field Immunity (30A/m), when applicable
- EN61000-4-11 Voltage Dips, Short Interruptions, and Voltage Variations

For DC power related testing, when applicable GR 1089 / GR 3160 may be referenced.

16.2.3 Country Specific EMC Requirement:

Most countries / region have country specific / regional EMC requirements. In addition to above listed EMC standards, the equipment shall demonstrate compliance to standards which includes, but not limited to
- CNS 13438: 2006
- AS/NZS CISPR22: 2009/A1:2010
- Industry Canada ICES-003
- VCCI V-3/2013-04
- KN 32 (Replacement of KN 22 effective January 1, 2016)
- KN 35 (Replacement of KN 24 effective January 1, 2016)
- ANATEL Resolution 242 / 323 / 442