



# ML605 MIG Design Creation

**March 2011**

# Revision History

Date	Version	Description
03/01/11	13.1	Recompiled under 13.1.
12/14/10	12.4	Recompiled under 12.4.
10/05/10	12.3	Recompiled under 12.3. Added slides on measuring the Read Data Window with VIO
07/23/10	12.2	Recompiled under 12.2.

© Copyright 2011 Xilinx, Inc. All Rights Reserved.

XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

**NOTICE OF DISCLAIMER:** The information disclosed to you hereunder (the “Information”) is provided “AS-IS” with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

# Overview

- **Virtex-6 DDR3 Memory Interface**
- **ML605 Board**
- **ML605 Setup**
- **Generate MIG Example Design**
- **Modifications to Example Design**
- **Compile Example Design**
- **Run MIG Example Design**
- **Adjust Data Pattern using VIO Console**
- **Example Design VIO Consoles**
- **Measure Read Data Window with VIO**
- **References**

# Virtex-6 DDR3 Memory Interface

- **Pre-Engineered Controller and Physical Layer (PHY) memory interface**
- **300-533 MHz (600-1066 Mb/s) Performance**
  - Center Column Interfaces
  - 400 MHz in a -1 speed device
  - 533 MHz in -2, -3 devices
- **1 Gb density memory device support**
- **X4, x8, x16 device support**
- **Configurable data bus widths**
  - Multiples of 8 bits, up to 72 bits

# Virtex-6 Memory Controller and Interfaces

- **Improved performance**

- Higher data rates
  - Faster circuitry (40 nm)
  - Enhanced I/O (50 ps IODELAY)
  - Dedicated clocking paths
  - Real-time calibration
- Higher effective bandwidth
  - Reordering controller (DDR3/DDR2)

ML605 provides DDR3 SO-DIMM

- **Improved functionality**

- DDR3 DIMM write leveling

- **Easy to use**

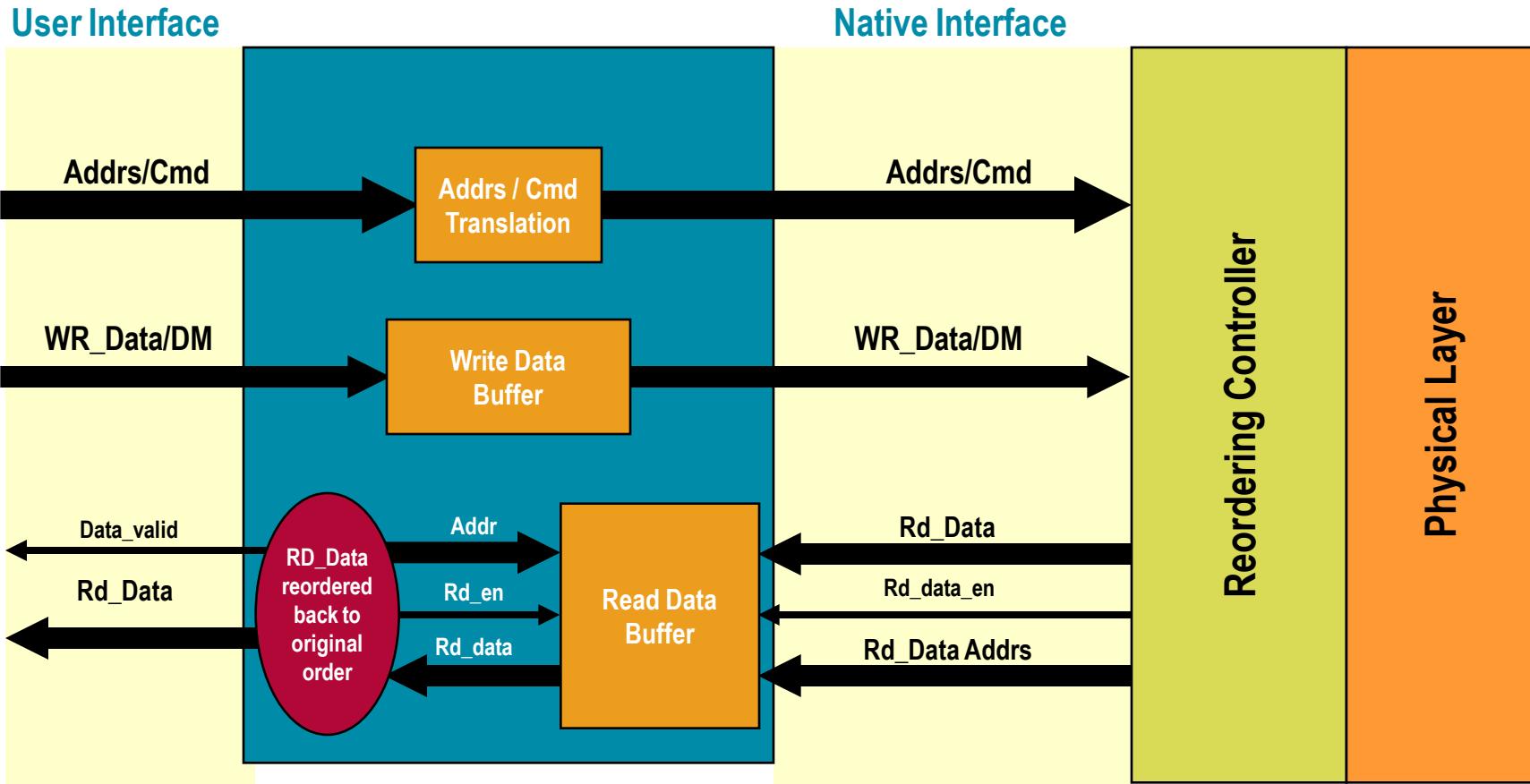
- MIG for ISE design flow
- MPMC for EDK design flow



*Xilinx makes it easier and faster to design with Virtex-6*

# DDR3 User Interfaces

- **Virtex-6 FPGA user interface similar to Virtex-5 architecture**
  - Native interface option available for the advanced users to achieve lower latency

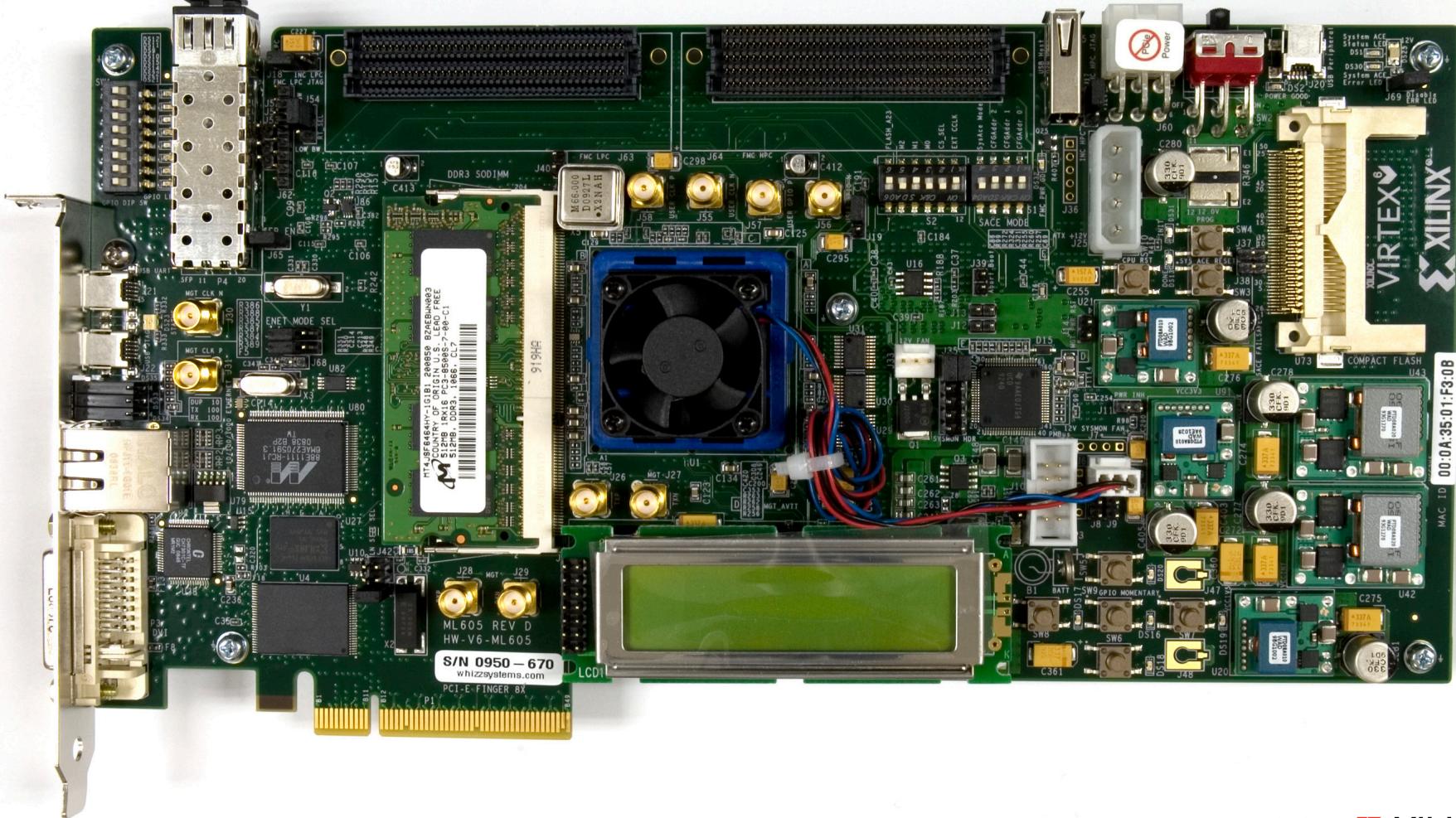


# Reordering for Higher Effective Bandwidth

- **Half-frequency DDR2/DDR3 controller**
  - Control state machine runs at half the memory clock rate
- **Reorder READs to avoid precharge time penalty**
  - Example : Execute out-of-order READs to a different bank while performing precharge for the current bank
- **Regroup READs and WRITEs to minimize bus turnaround**
  - Example : Read A - Write B - Read C - Write D
  - Reordered to: Read A - Read C - Write B - Write D
- **Reordering controller looks ahead several commands**
  - Efficiency is dependent on applications (address / command patterns)

***Reordering can more than double the throughput***

# Xilinx ML605 Board



Note: Presentation applies to the ML605

# ISE Software Requirements

- Xilinx ISE 13.1 software



# ChipScope Pro Software Requirement

- Xilinx ChipScope Pro 13.1 software

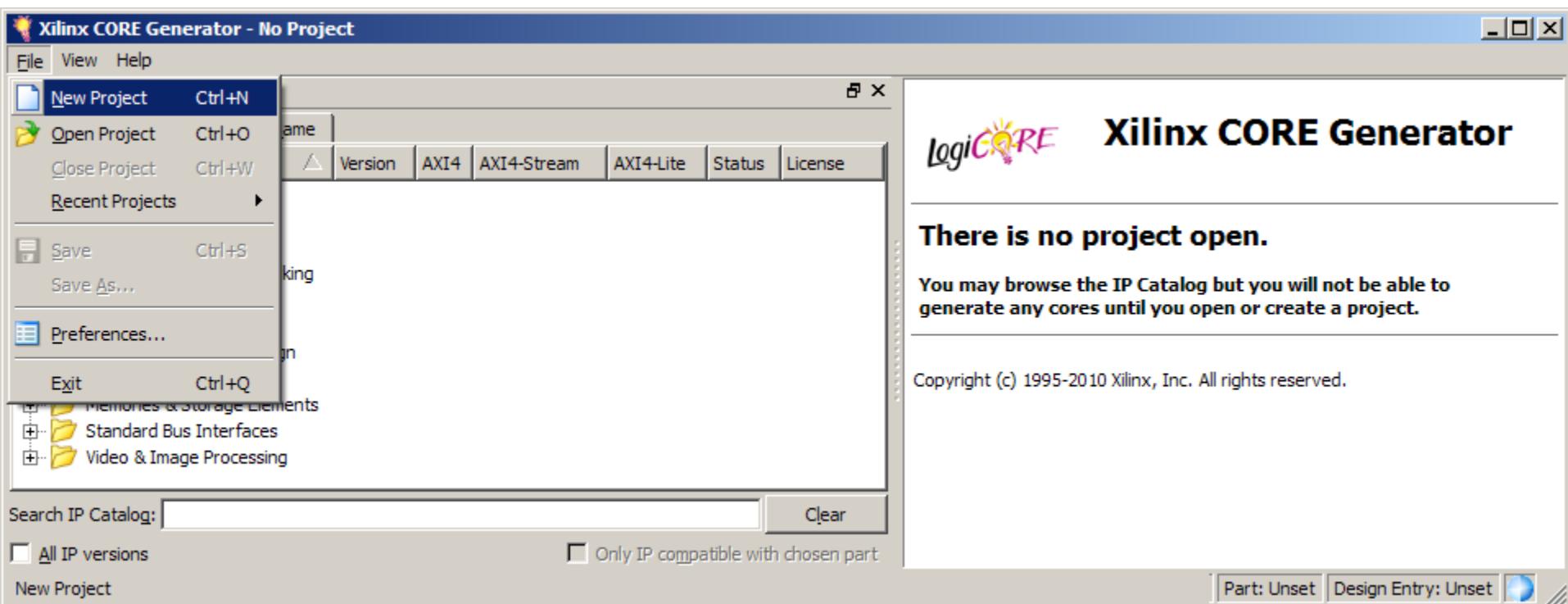


# Generate MIG Example Design

- **Open the CORE Generator**

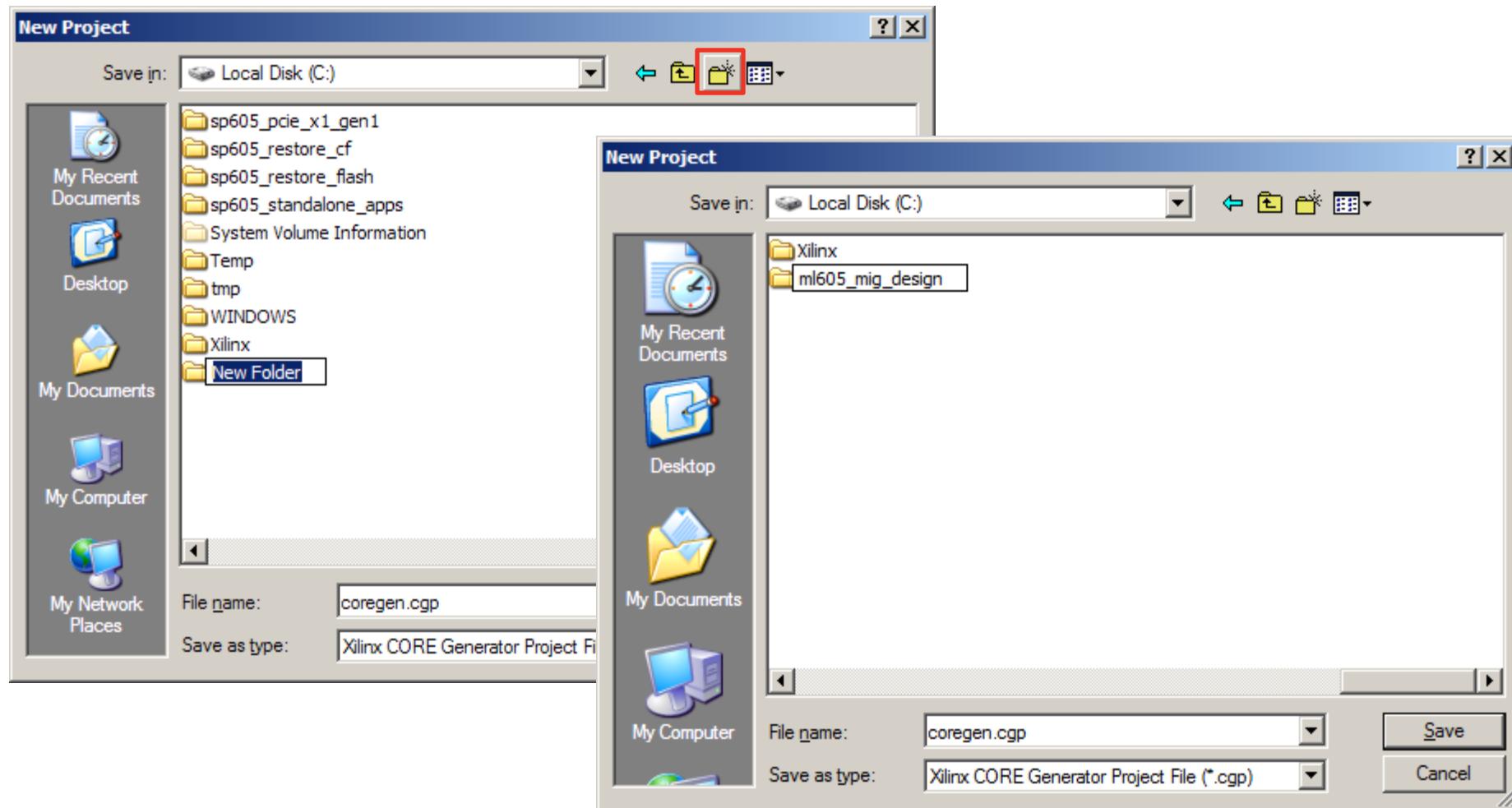
Start → All Programs → Xilinx ISE Design Suite 13.1 →  
ISE Design Tools → Tools → CORE Generator

- **Create a new project; select File → New Project**



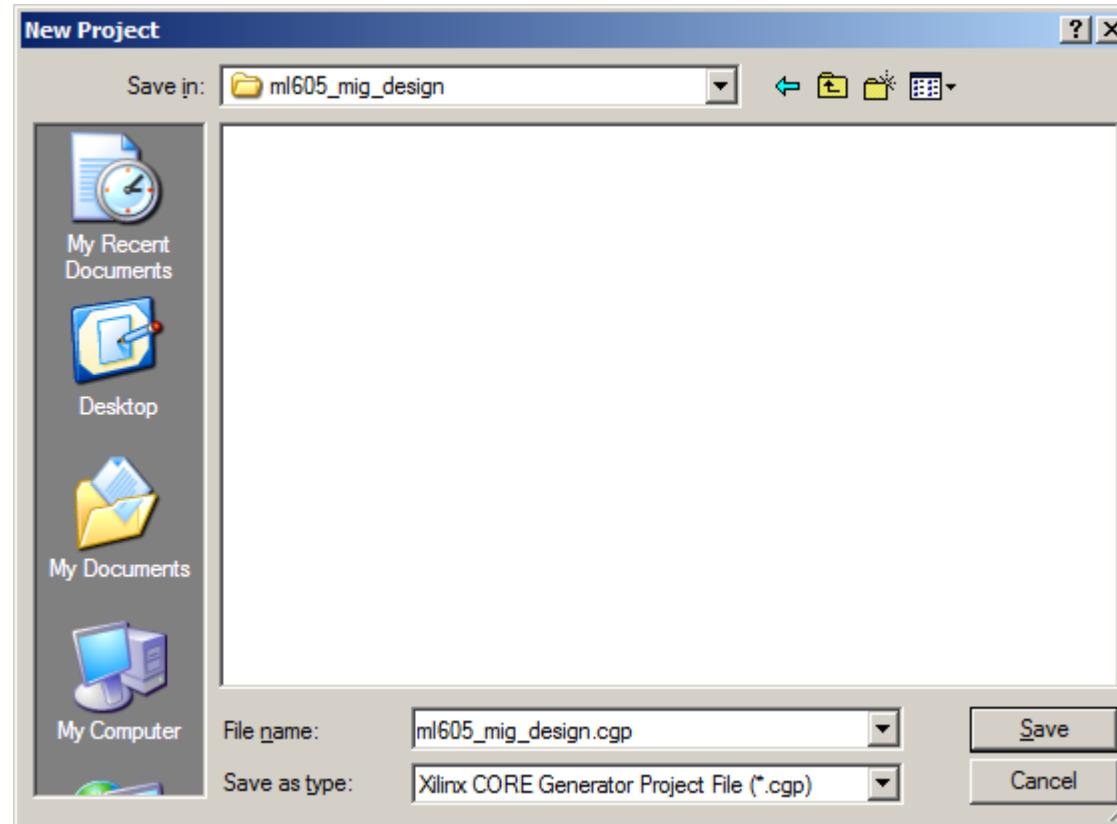
# Generate MIG Example Design

- Create a project directory: ml605\_mig\_design

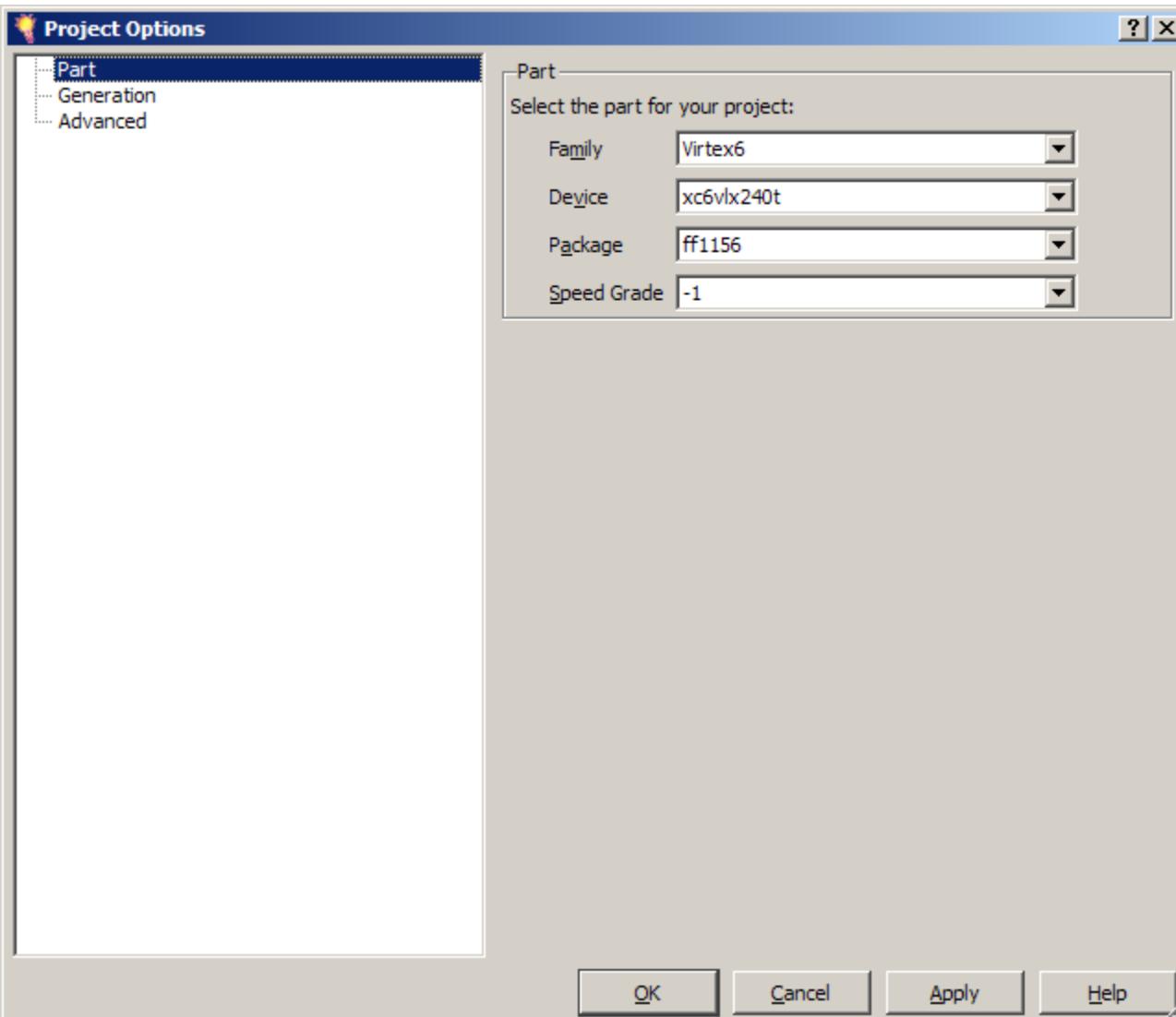


# Generate MIG Example Design

- Name the project: ml605\_mig\_design.cgp

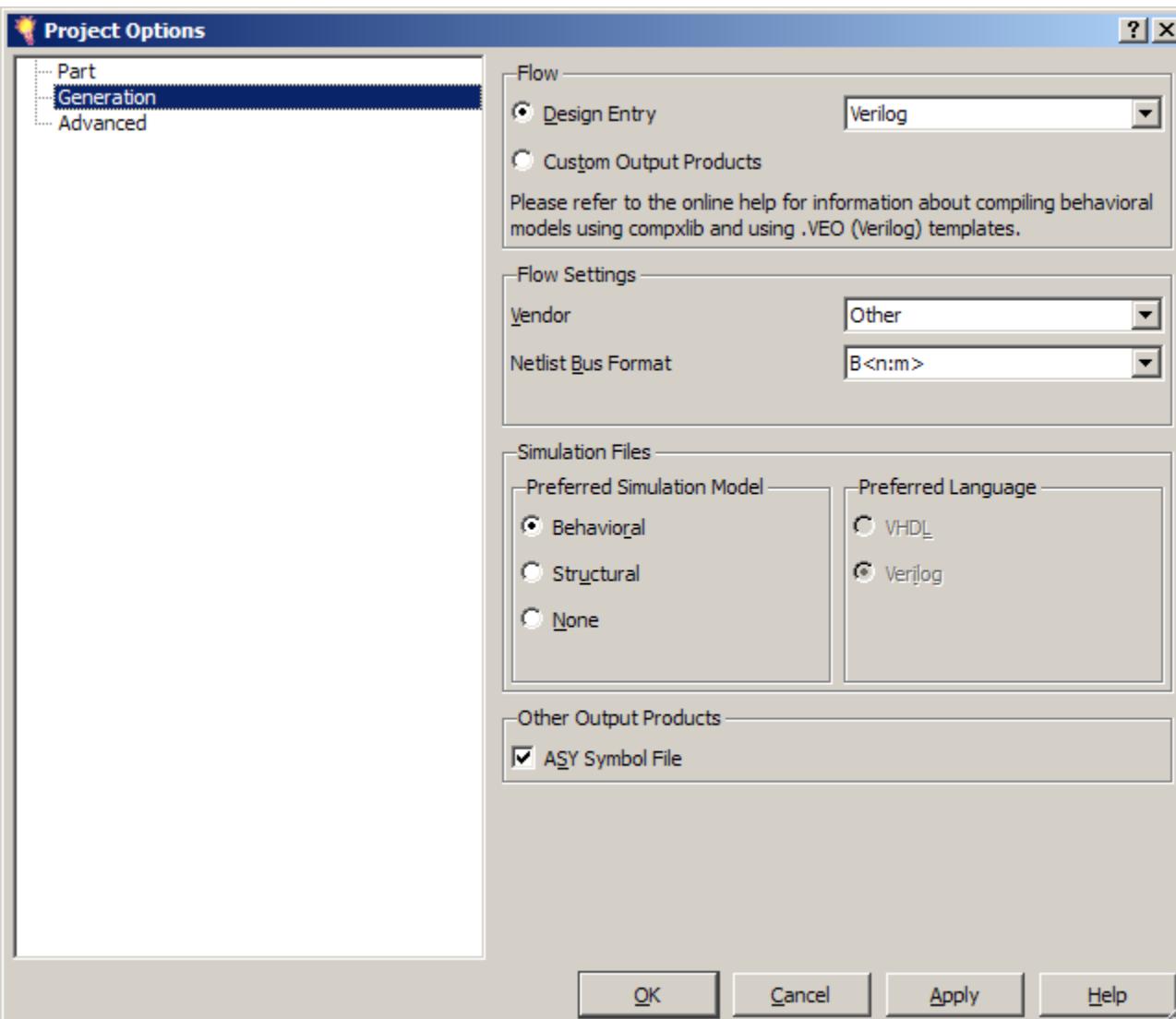


# Generate MIG Example Design



- **Select Part**
- **Set the Part (as shipped on the ML605):**
  - Family: Virtex6
  - Device: xc6vlx240t
  - Package: ff1156
  - Speed Grade: -1
- **Select Generation**

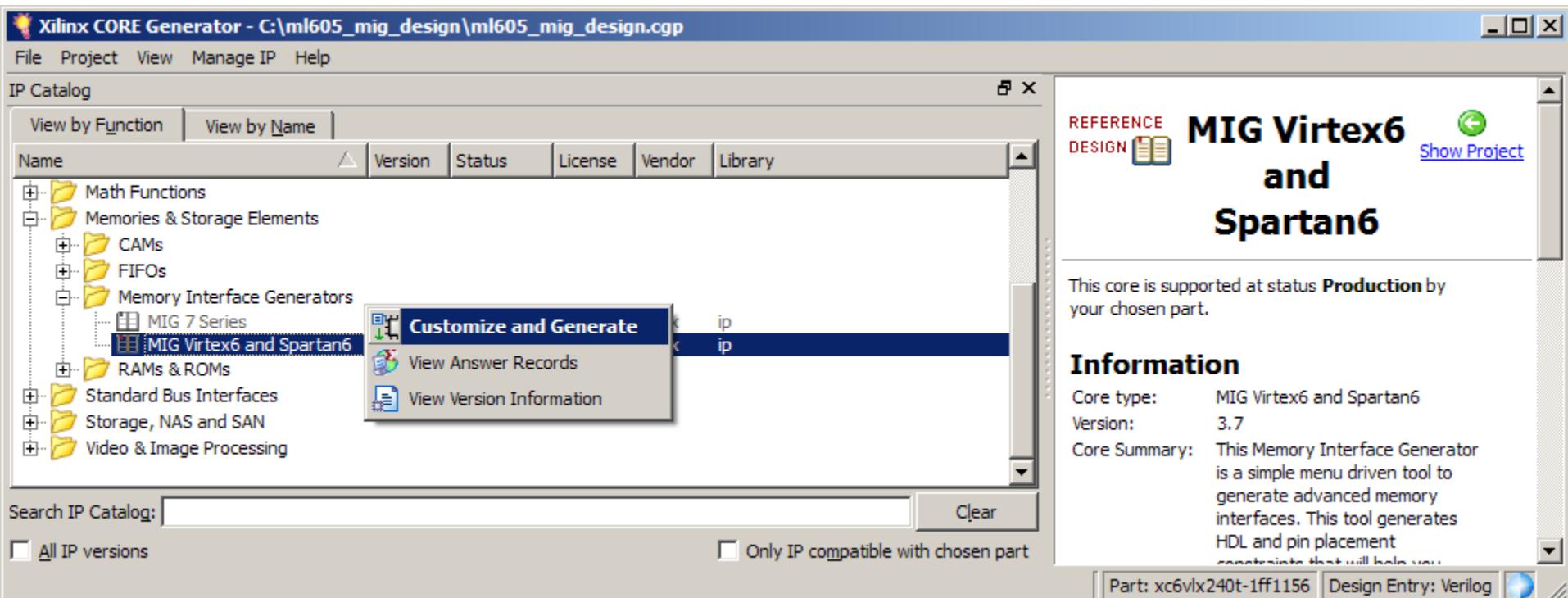
# Generate MIG Example Design



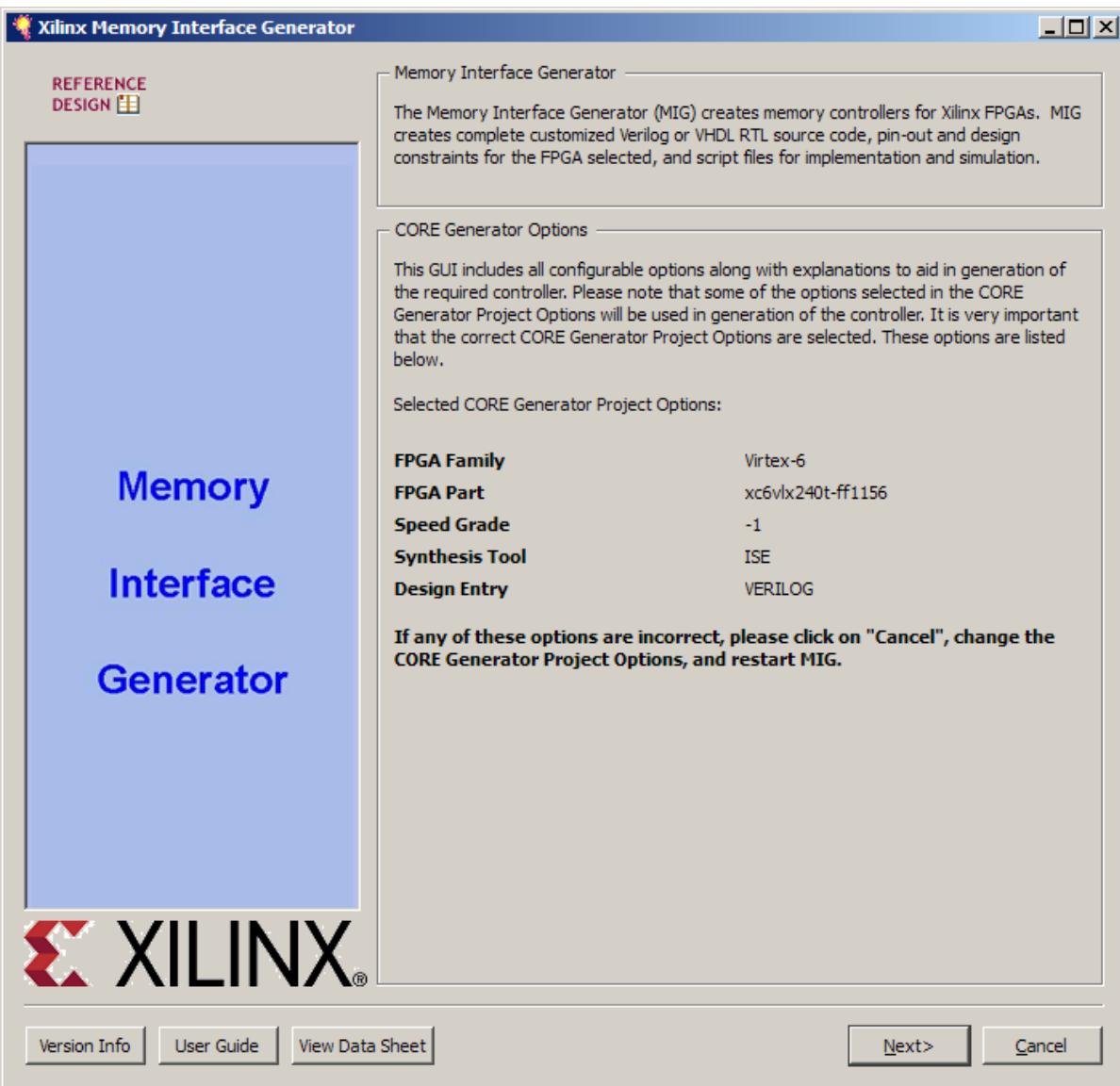
- **Under Generation**
  - Set the Design Entry to Verilog
- **Click OK**

# Generate MIG Example Design

- Right click on MIG Version 3.7
  - Select Customize and Generate

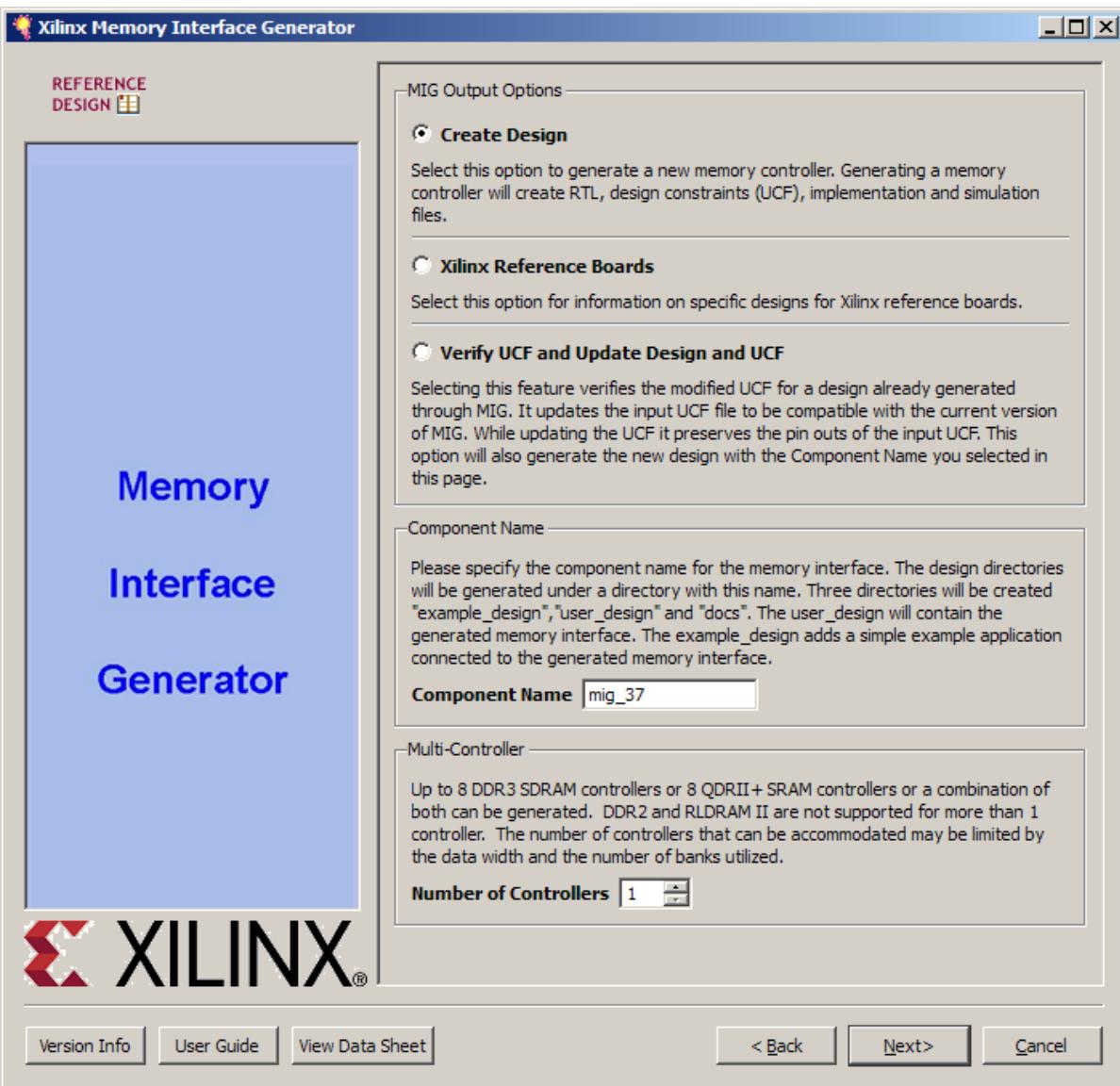


# Generate MIG Example Design



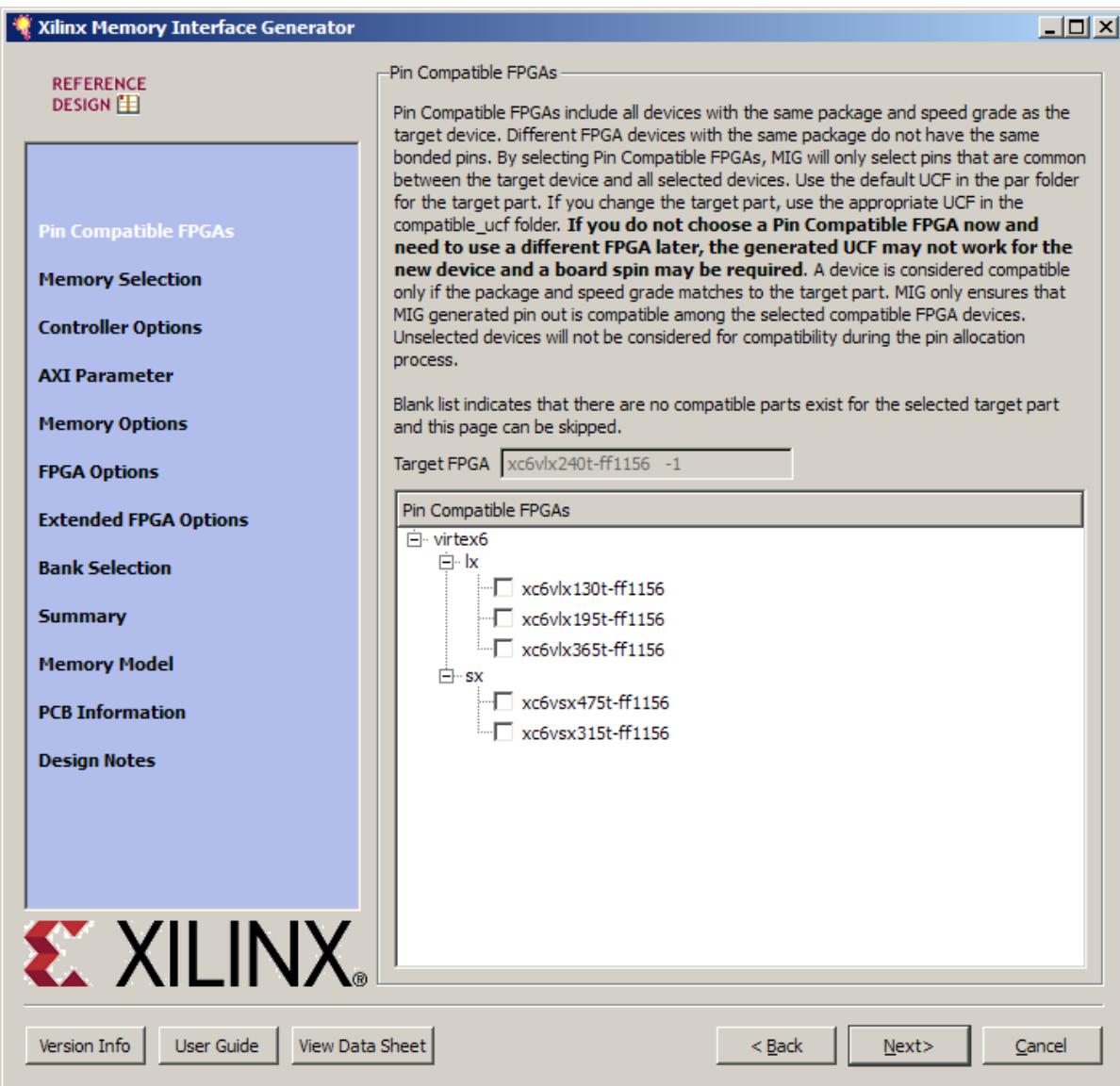
- Leave this page as is
  - Click Next

# Generate MIG Example Design



- Leave this page as is
  - Click Next

# Generate MIG Example Design



- Leave this page as is
  - Click Next

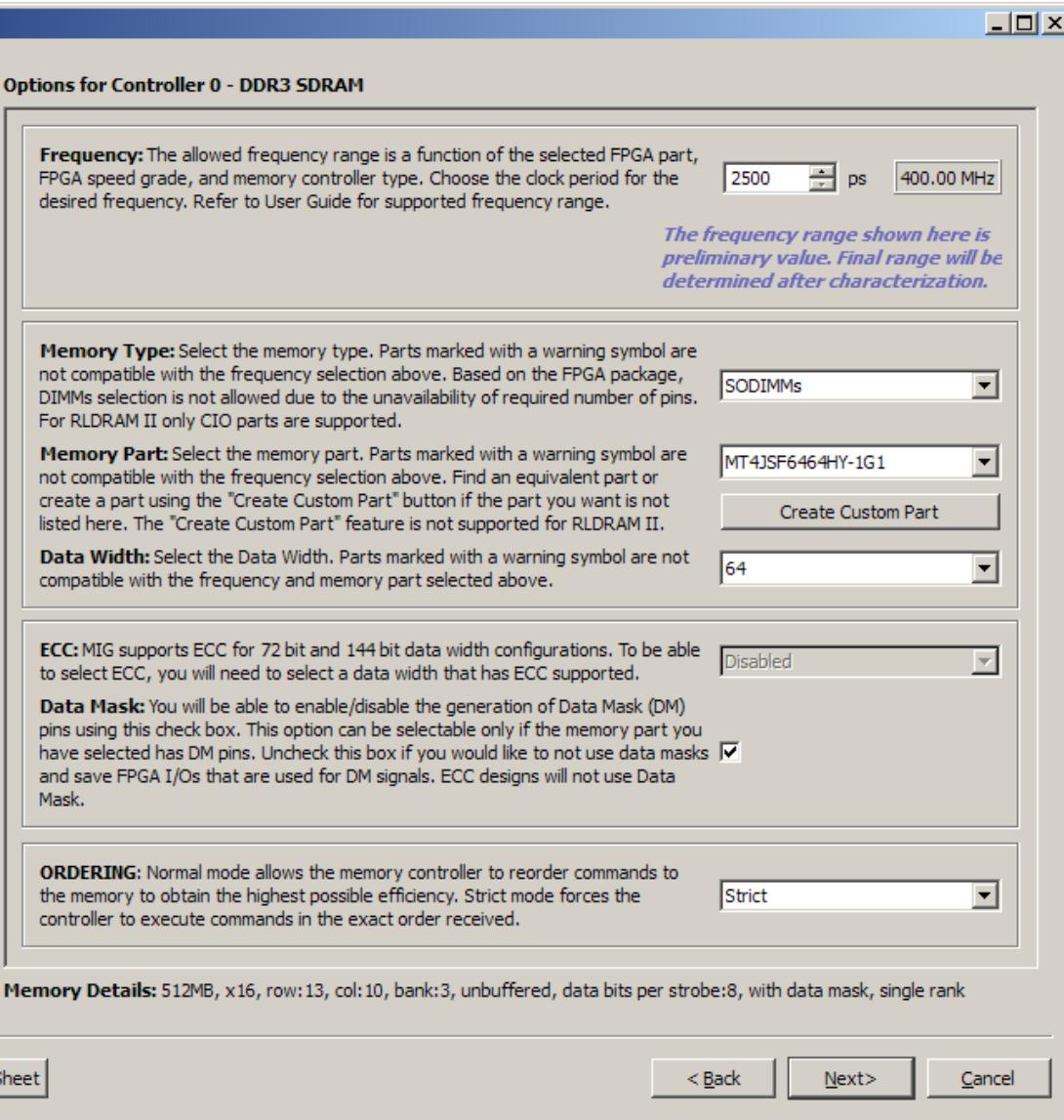
# Generate MIG Example Design



## ▪ Select Memory Type

- DDR3 SDRAM
- Click Next

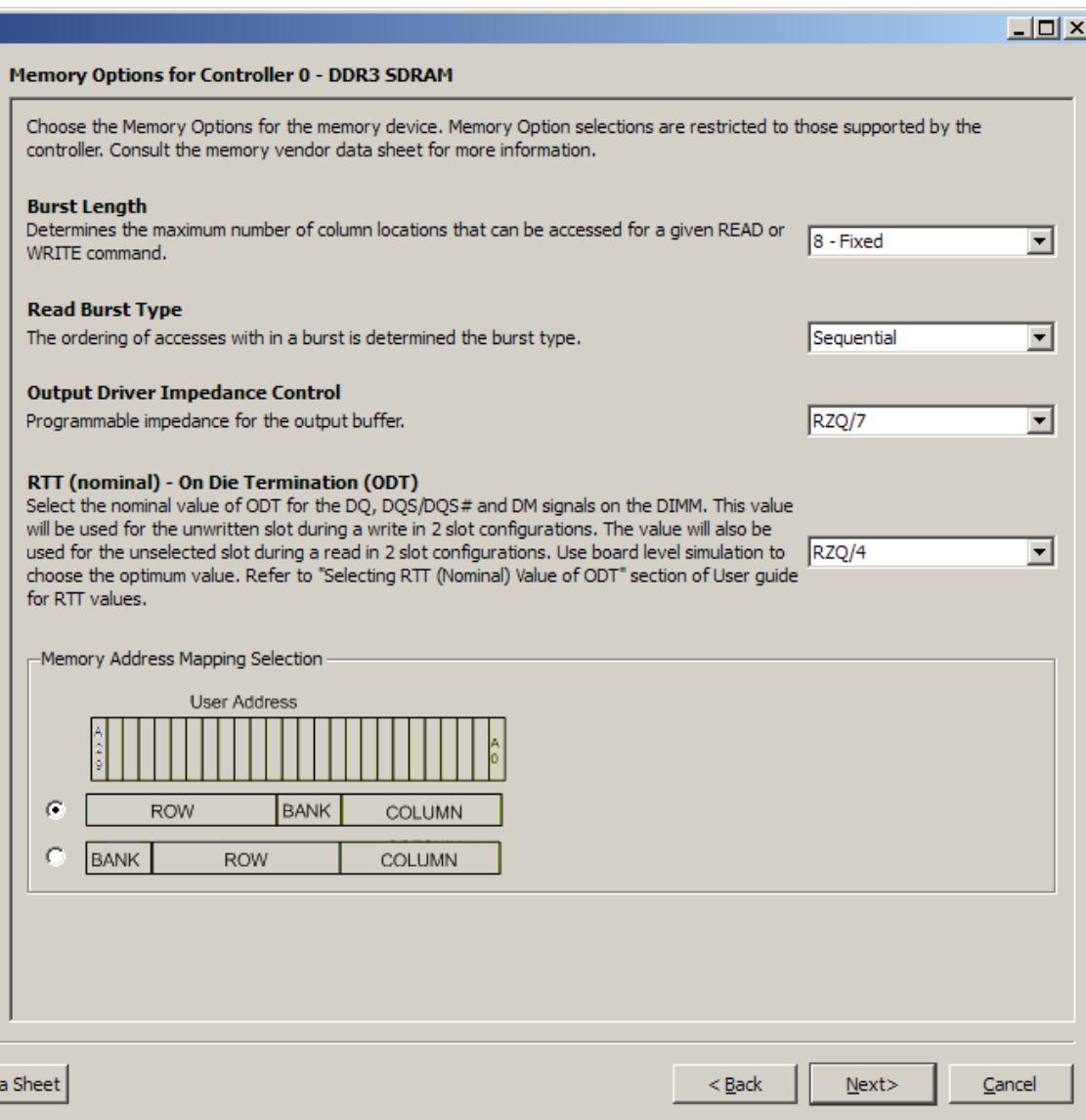
# Generate MIG Example Design



## ▪ Select

- Type: SODIMMs
- Part: MT4JSF6464HY-1G1
- Ordering: Strict

# Generate MIG Example Design



- Leave this page as is
  - Click Next

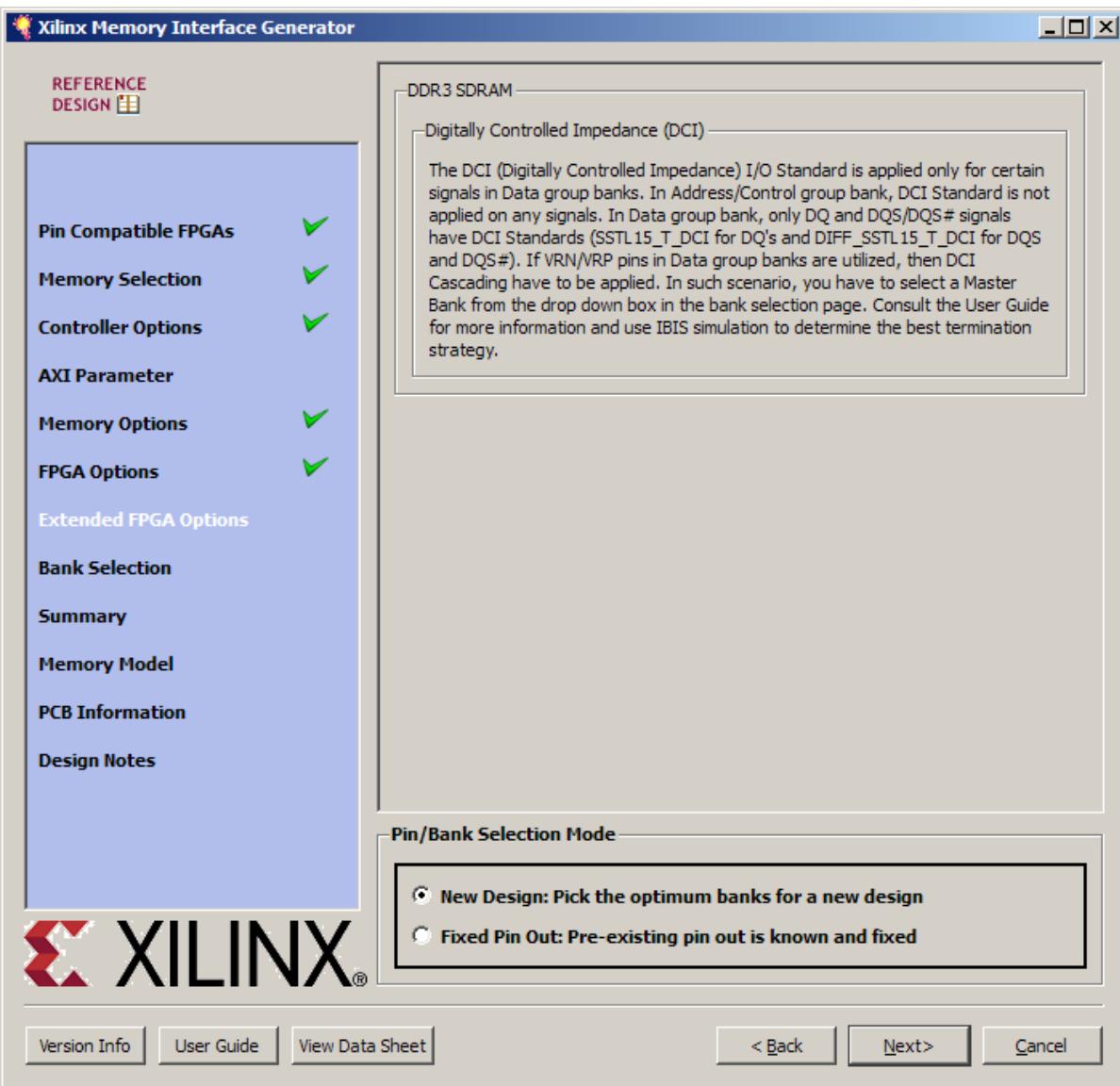
# Generate MIG Example Design



## ▪ Select

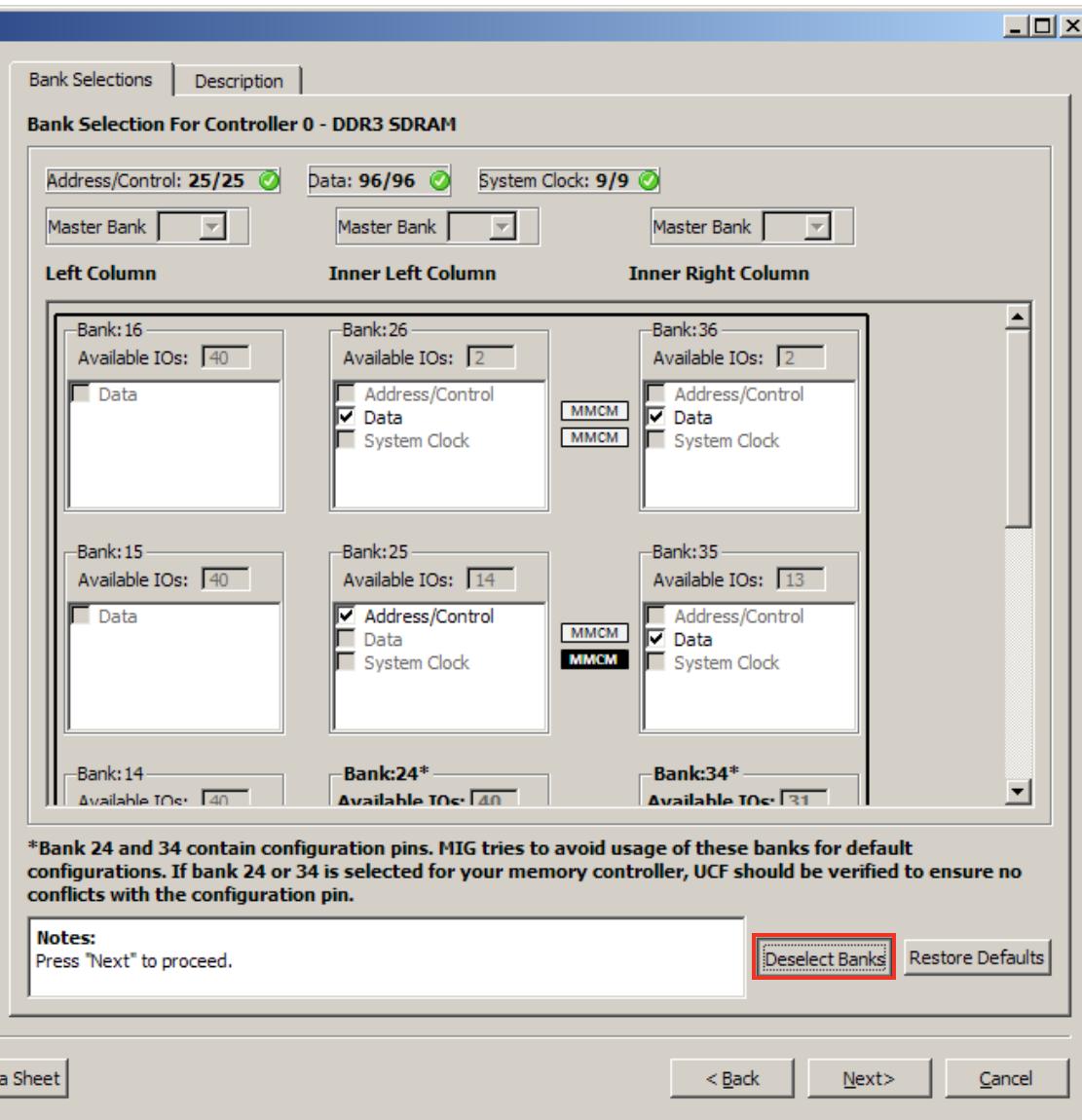
- Debug: ON

# Generate MIG Example Design



- **Select New Design**
  - Click Next

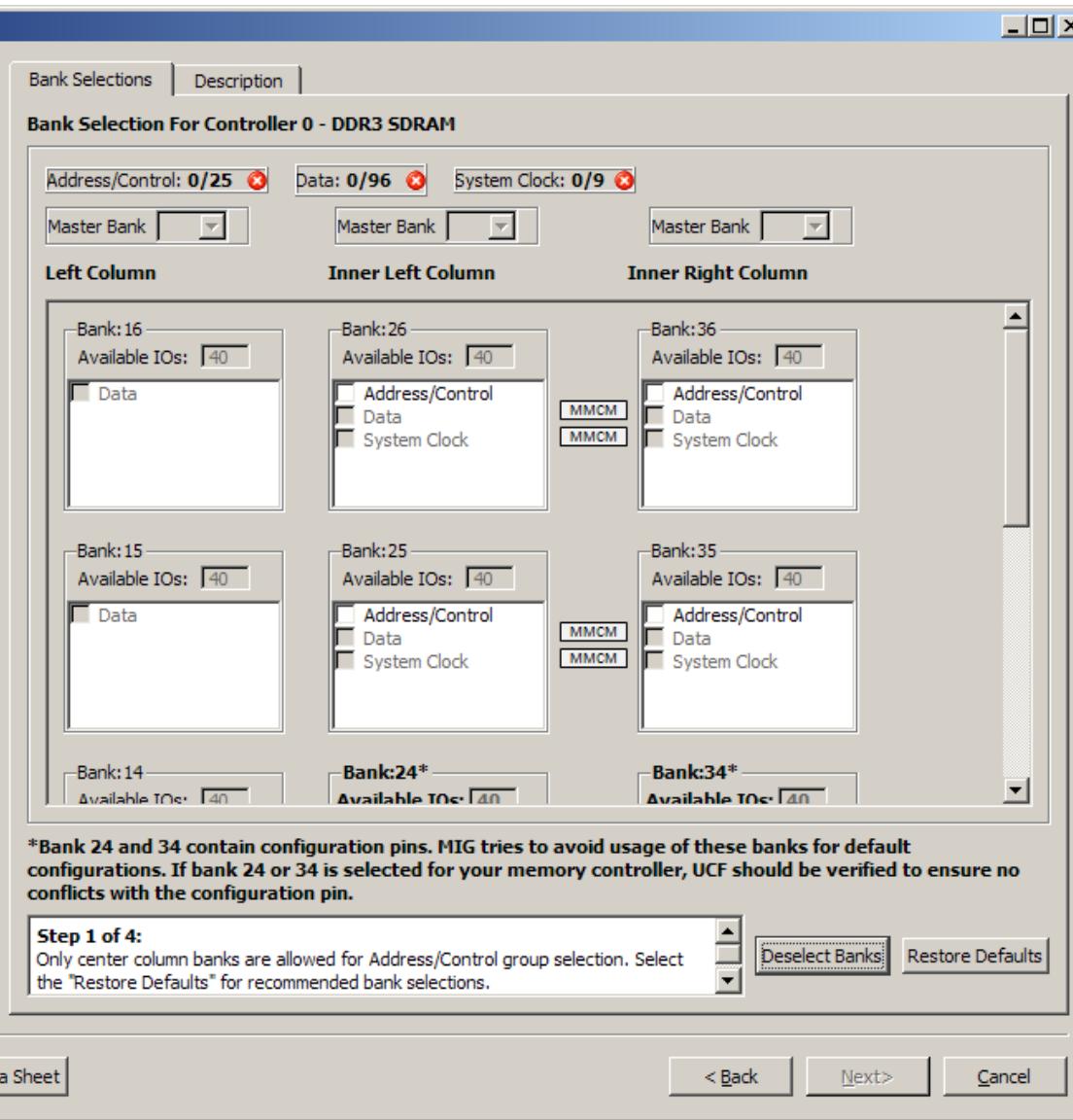
# Generate MIG Example Design



- On this screen select the banks as used on the ML605 SODIMM interface
- Click Deselect Banks

# Generate MIG Example Design

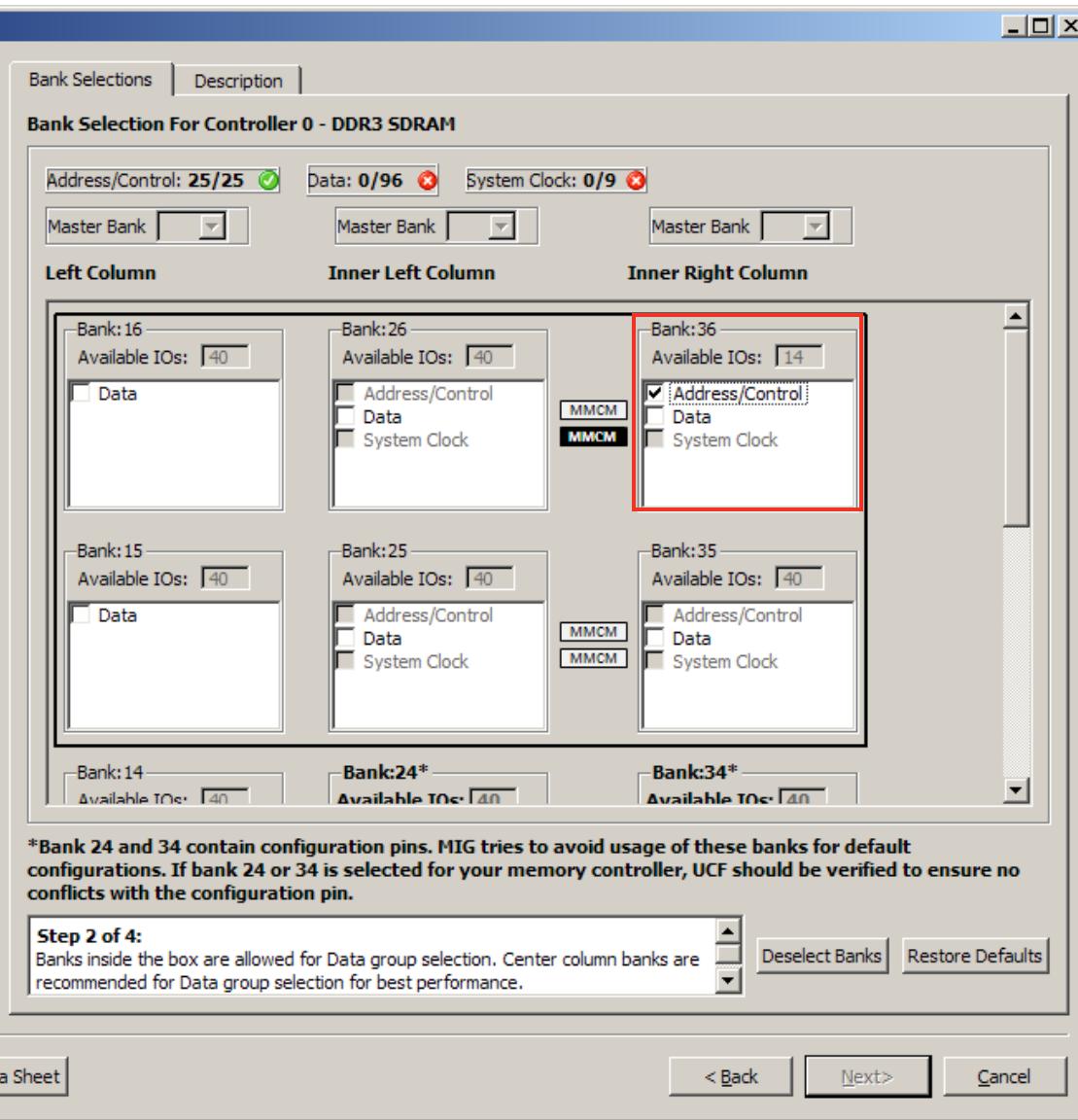
▪ All Banks Deselected



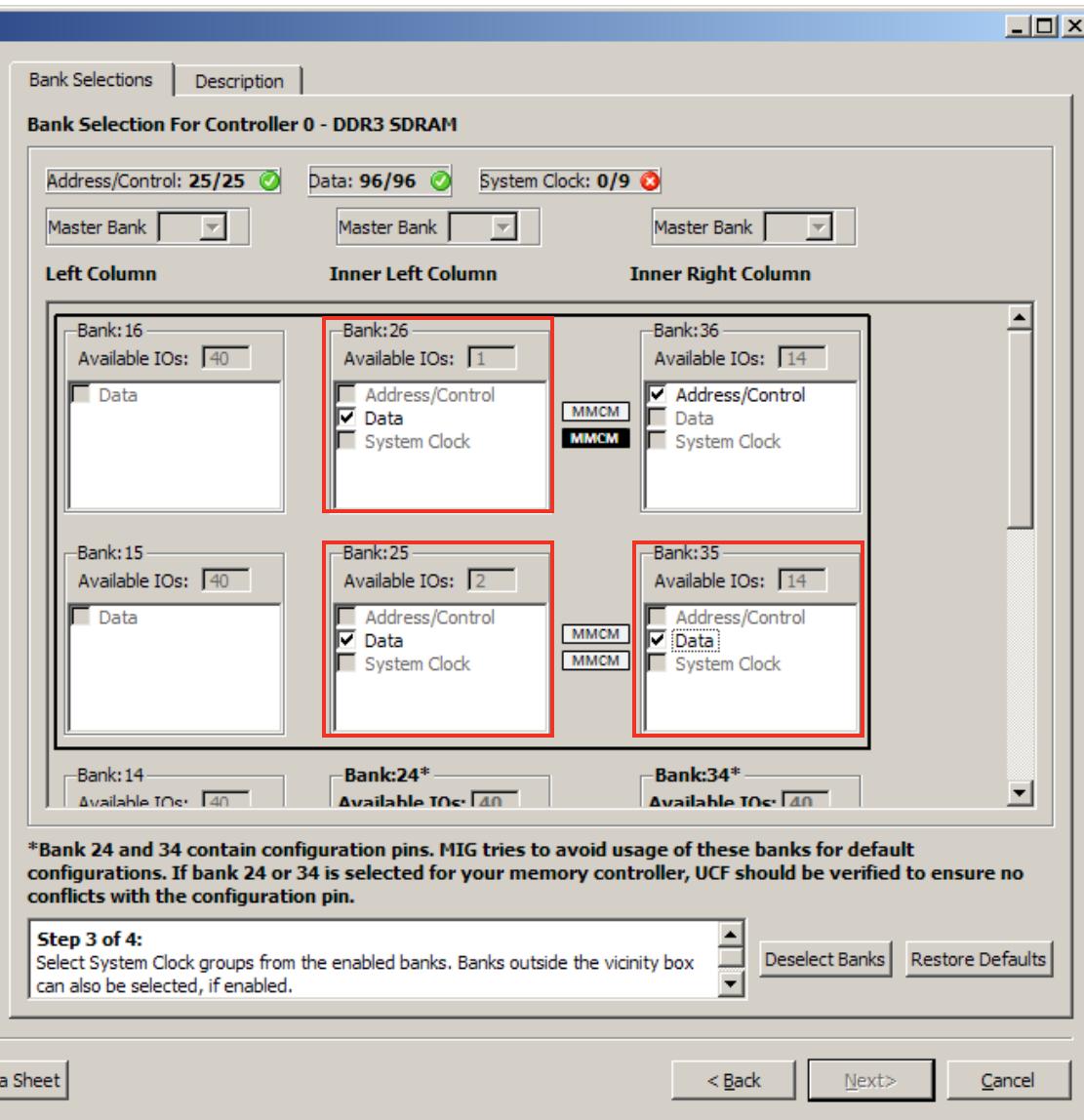
# Generate MIG Example Design

## ▪ Select

- Bank 36: Address/Control



# Generate MIG Example Design



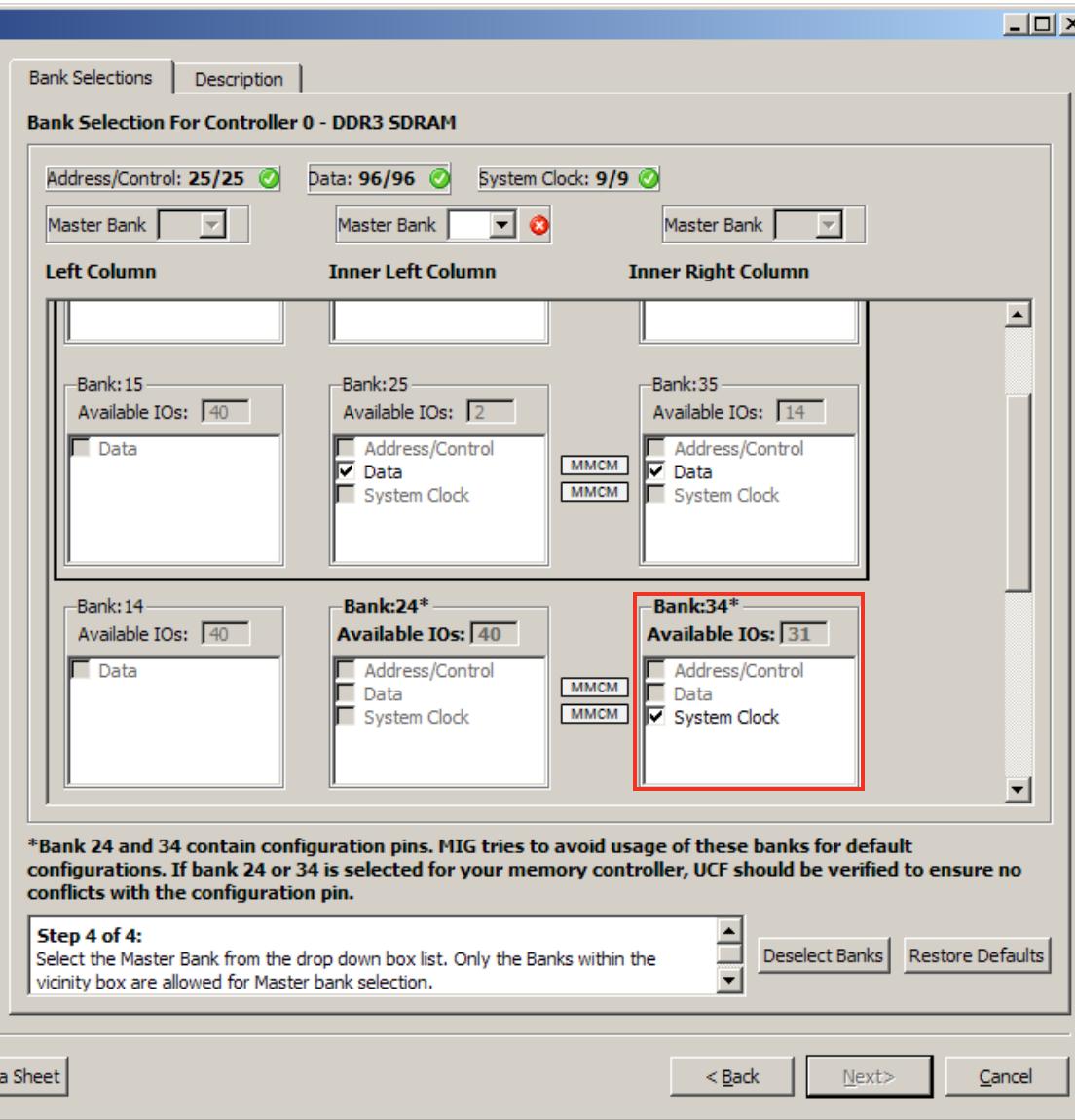
## ▪ Select

- Bank 26: Data
- Bank 25: Data
- Bank 35: Data

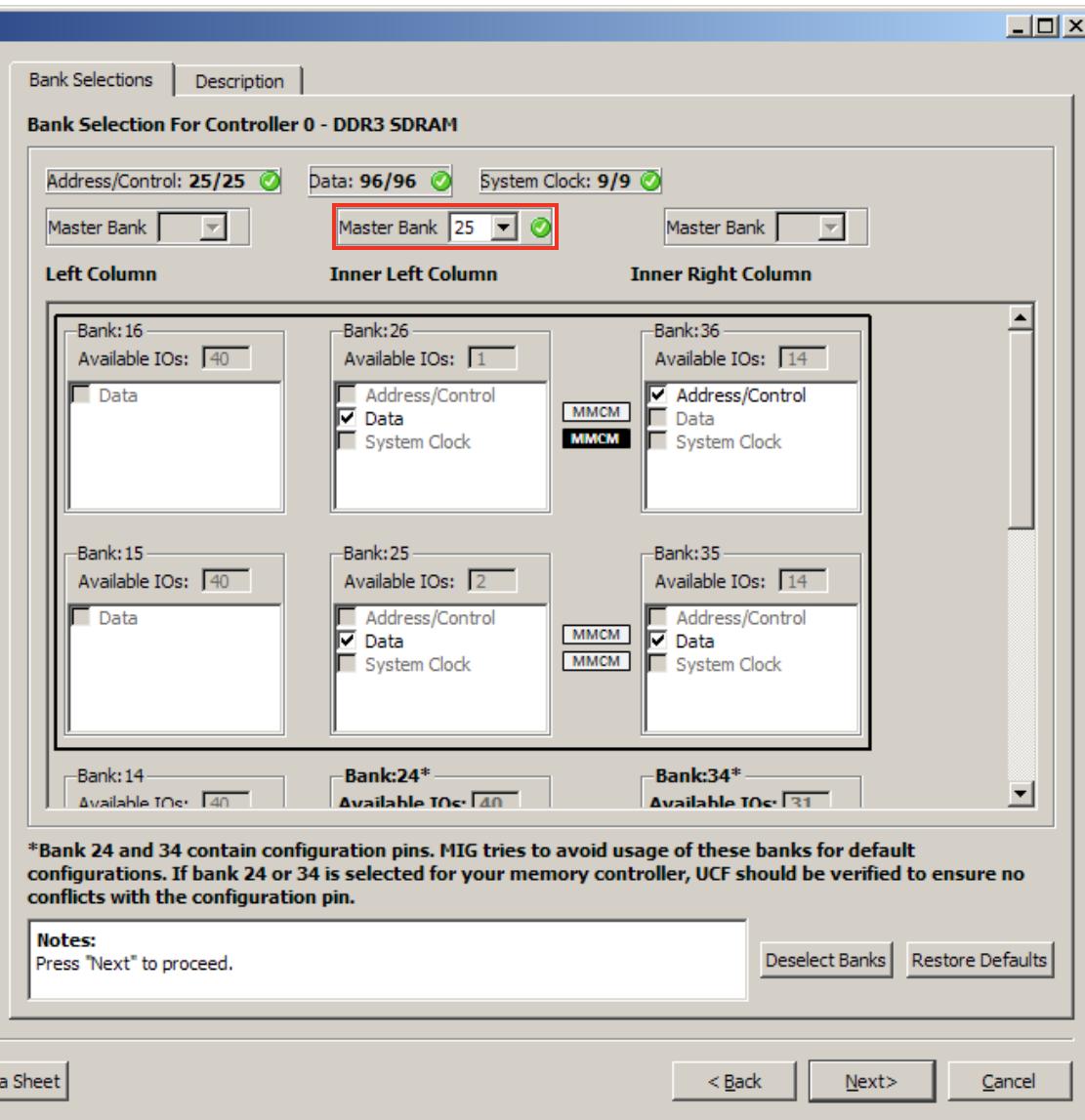
# Generate MIG Example Design

## ▪ Select

- Bank 34: System Clock



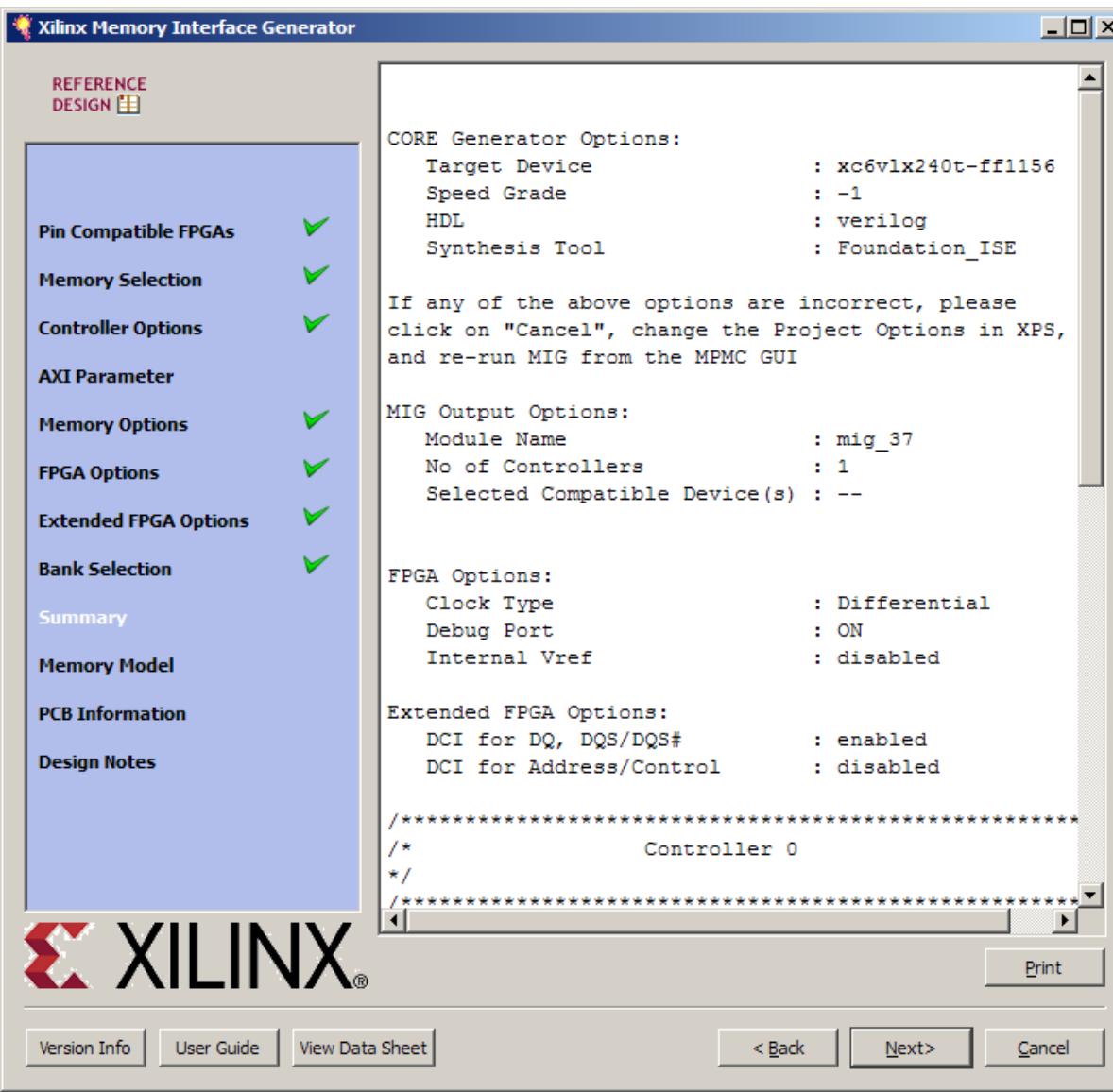
# Generate MIG Example Design



## ▪ Select

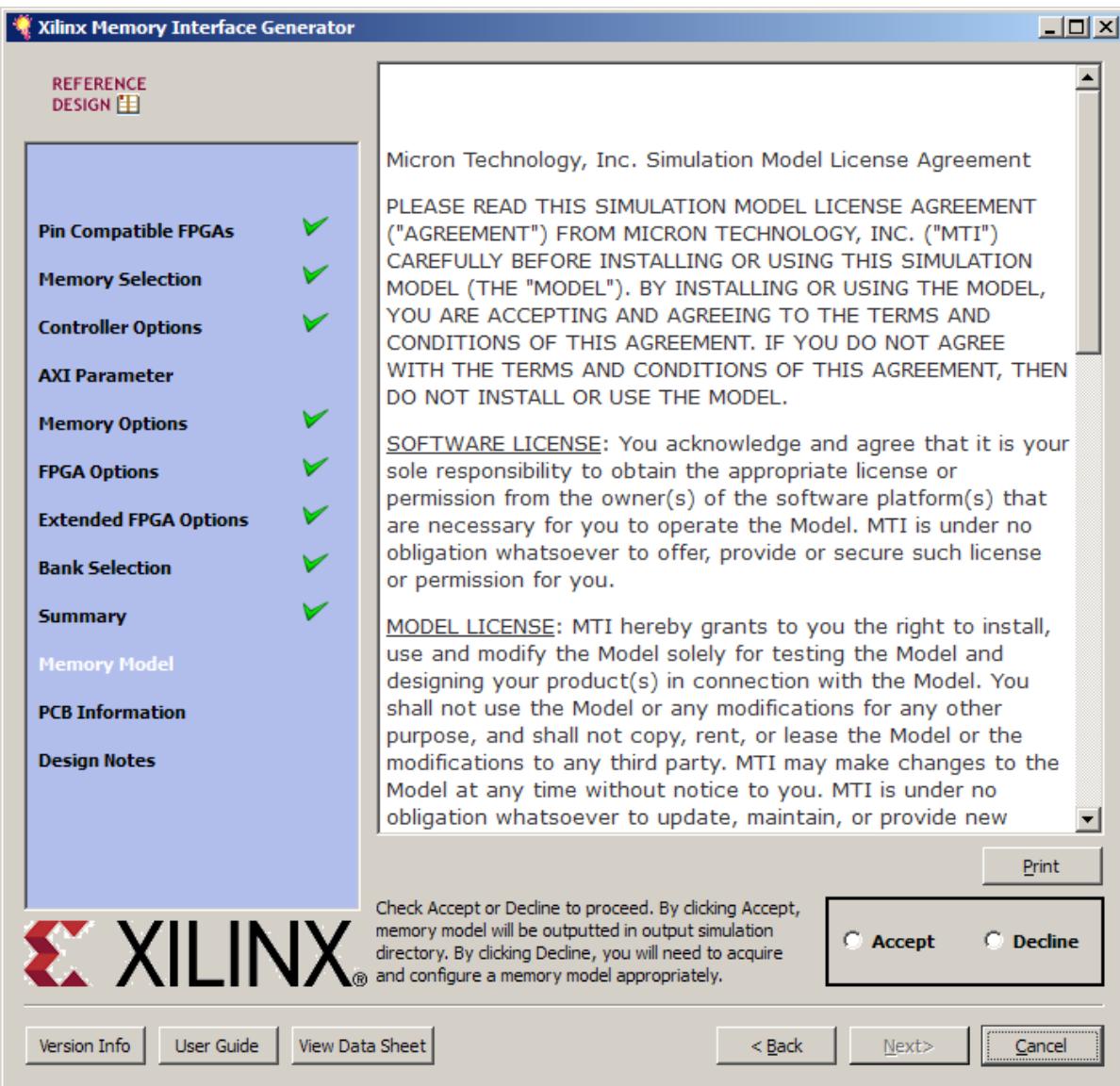
- Master Bank: 25
- Click Next

# Generate MIG Example Design



- Leave this page as is
  - Click Next

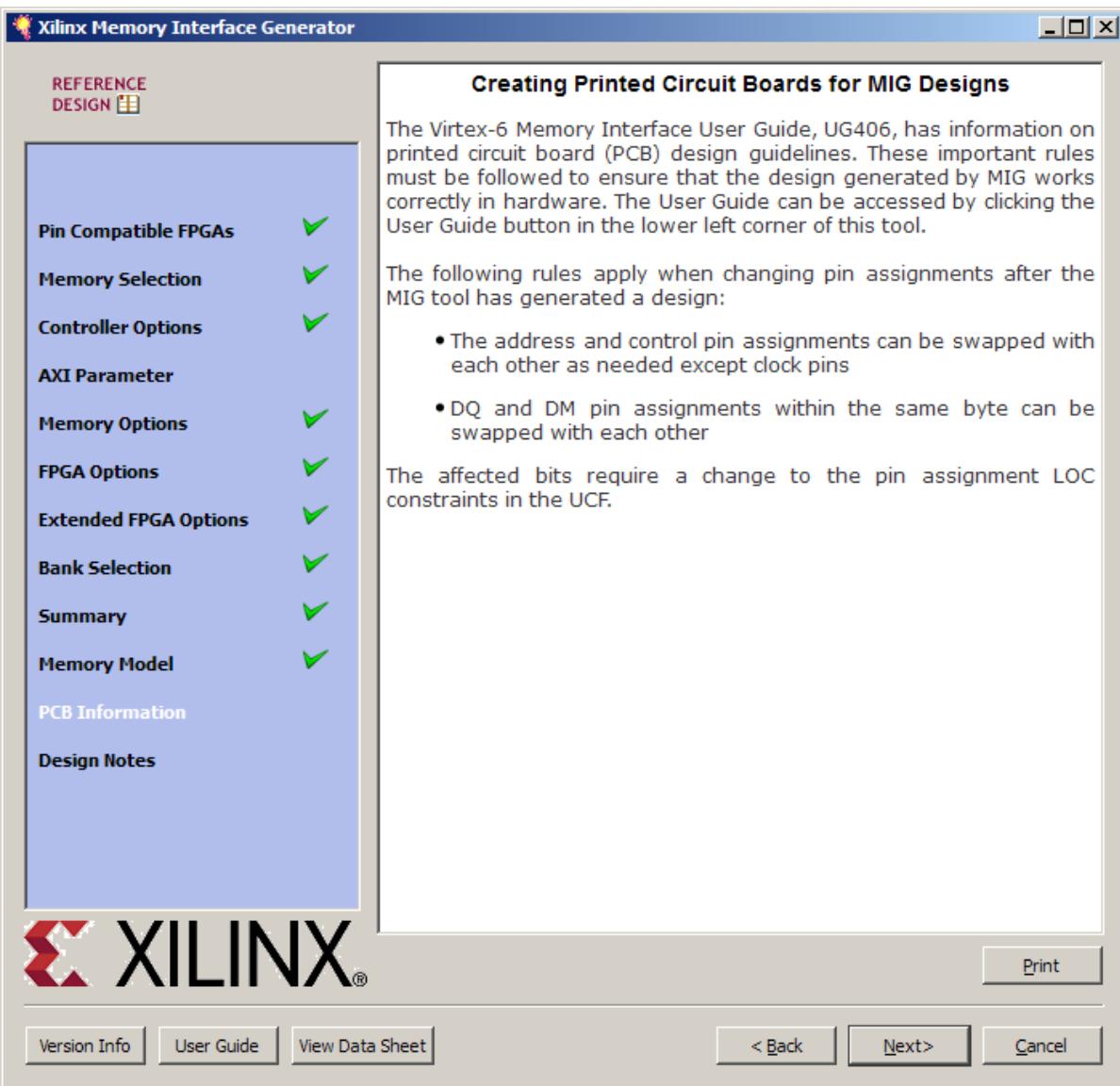
# Generate MIG Example Design



## ▪ Accept Simulation license, if desired

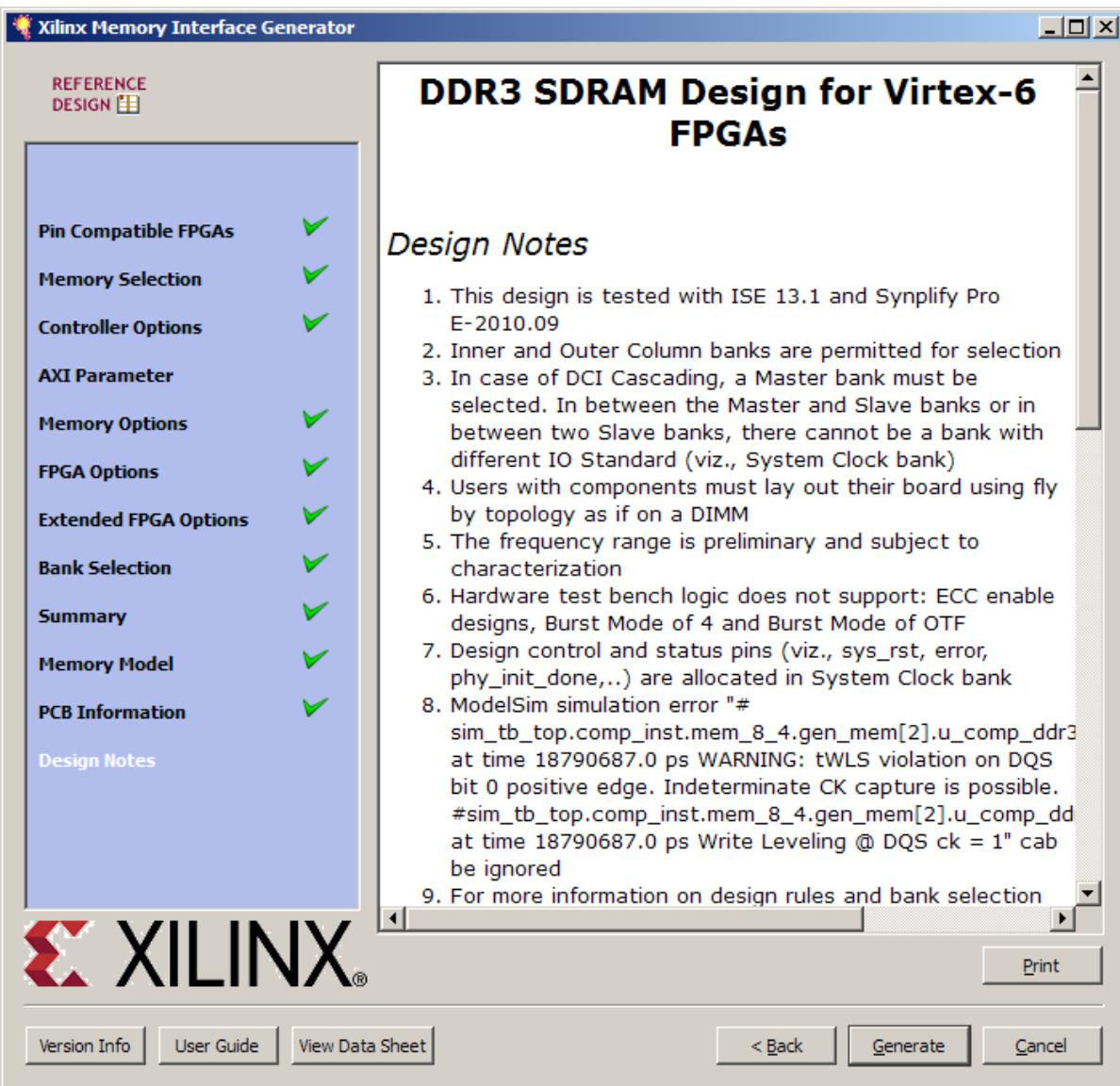
- Otherwise, Decline license
- Click Next

# Generate MIG Example Design



- Leave this page as is
  - Click Next

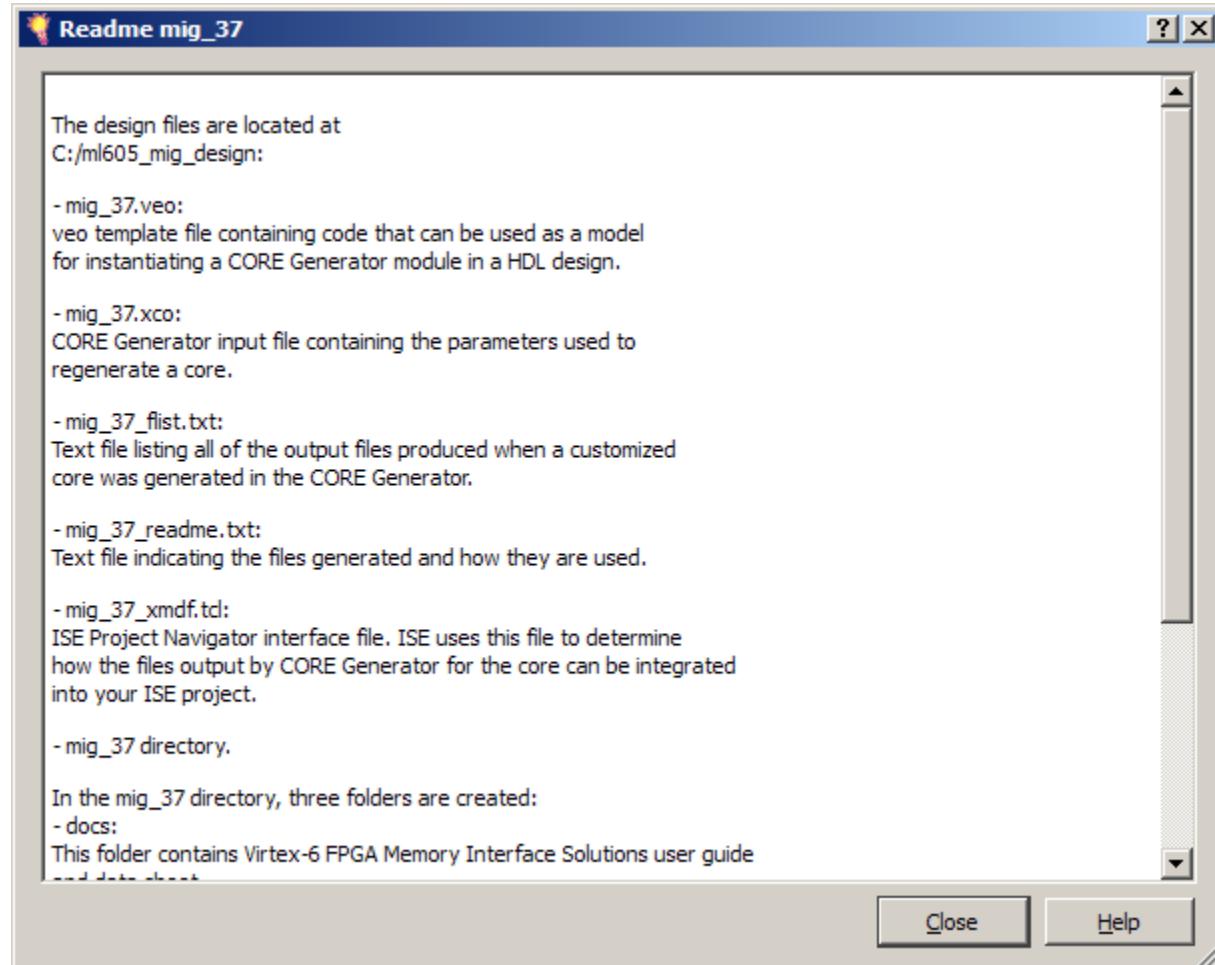
# Generate MIG Example Design



▪ Click Generate

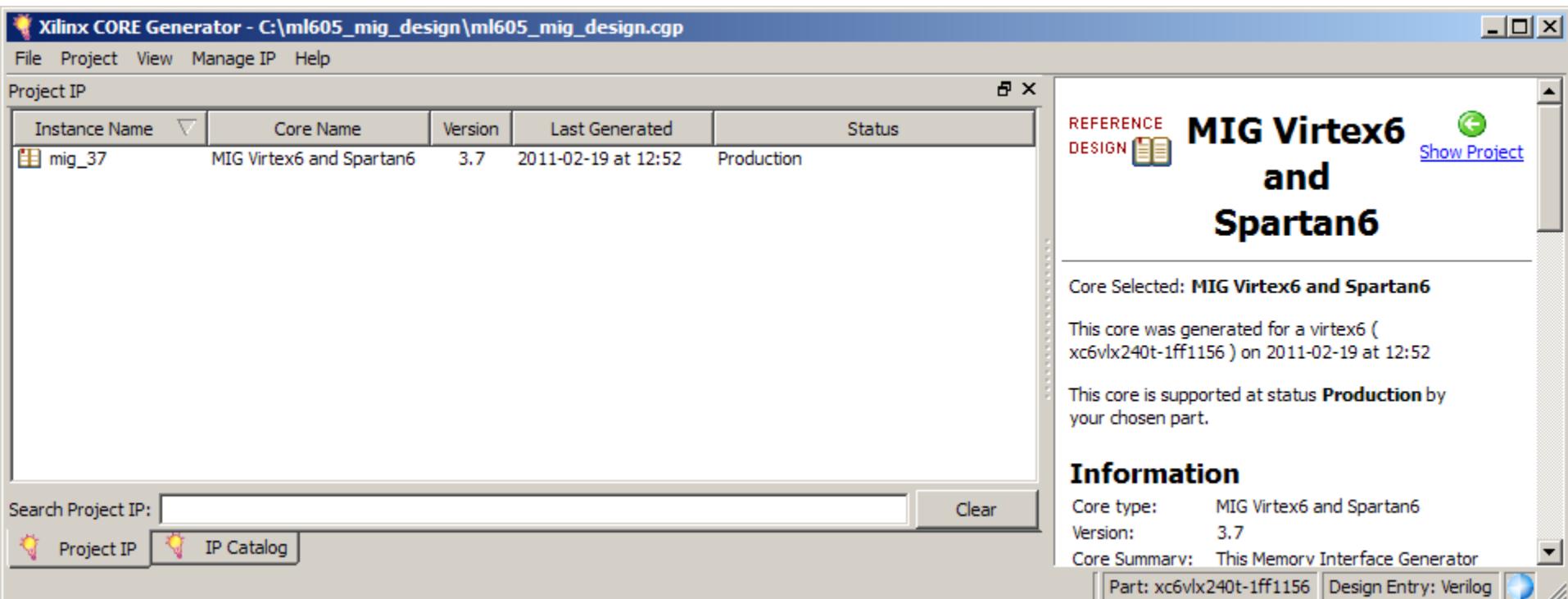
# Generate MIG Example Design

- After the MIG core finishes generating, click Close on the Datasheet window



# Generate MIG Example Design

- MIG design appears in Project IP



# Modifications to Example Design

- **RDF0011.zip includes**

- ChipScope Project File, UCF, and Verilog Files

- **Modifications to RTL Files for ML605 Example Design**

- Changed design to support a single 200 MHz LVDS clock input
  - Added Debug display code to drive LEDs
  - Added ChipScope ILA and VIO port assignments for ML605 board debug
  - Removed IIC Signals – sda, scl
  - Changed various parameter to match the ML605 board
    - DIVCLK\_DIVIDE = 1 (was 2)
    - nDQS\_COLx
    - DQS\_LOC\_COLx
    - RST\_ACT\_LOW = 0 (was 1)

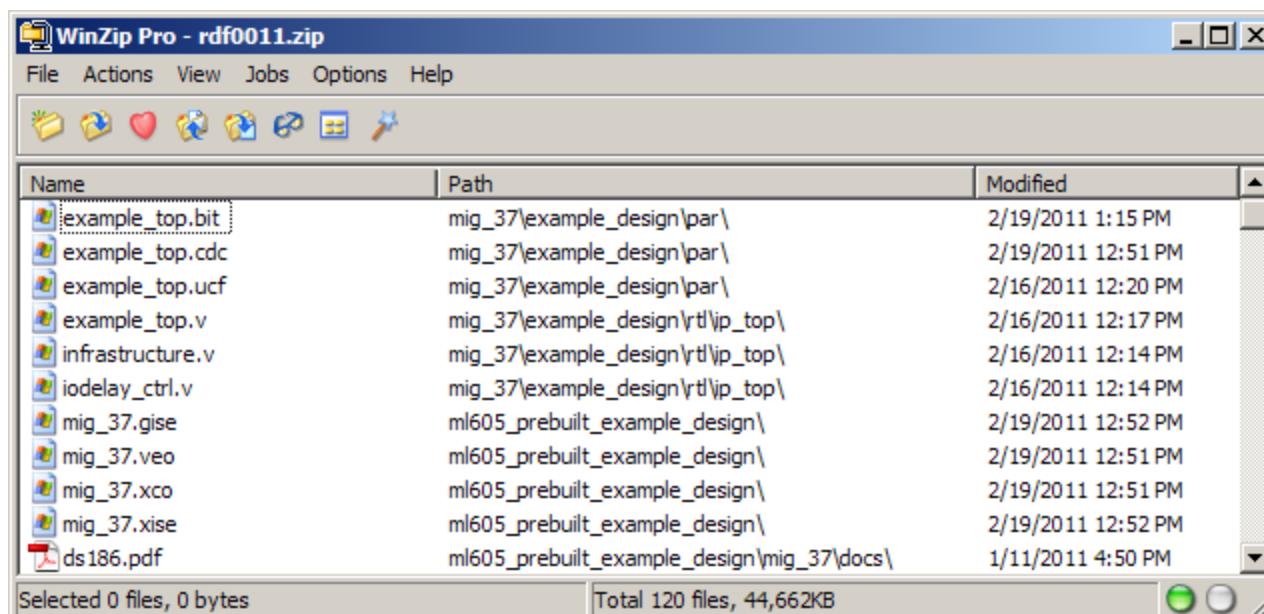
# Modifications to Example Design

- **Updates to UCF file specifically required for ML605 board:**

- Updated IO Locations to match ML605
- Remove IIC Signals – sda, scl
- Merged Default two clocks into one clock for ML605
- Moved sys\_reset to CPU\_RESET
- Edited DCI CASCADE to match ML605
- Removed CONFIG\_PROHIBIT lines
- Added LOC for GPIO LED signals (2.5V bank voltage)
- Added LOCs for RSYNC OSERDES and IODELAY

# Modifications to Example Design

- **Unzip the rdf0011.zip file to your C:\ml605\_mig\_design directory**
  - Available through <http://www.xilinx.com/ml605>
  - This adds modifications to the example design (1)
  - A fully pre-built ML605 example design is included in the zip file (2)
    - Use the included bitstream to [run MIG with ChipScope](#)
    - Run **ise\_flow.bat** in <design directory>\ml605\_prebuilt\_example\_design\mig\_37\example\_design\par to recompile the pre-built example design

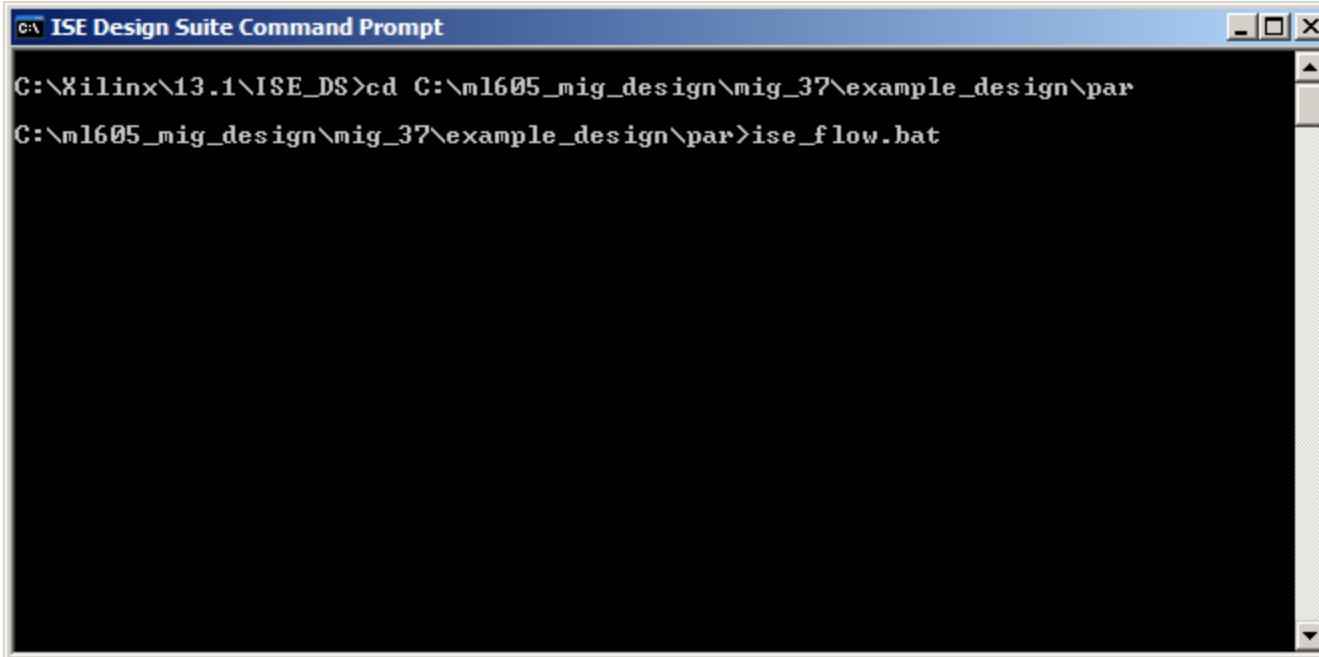


Note: Overwrites Core Generator output files with ML605 specific files

# Compile Example Design

- Start a ISE Design Suite Command Prompt and enter these commands:

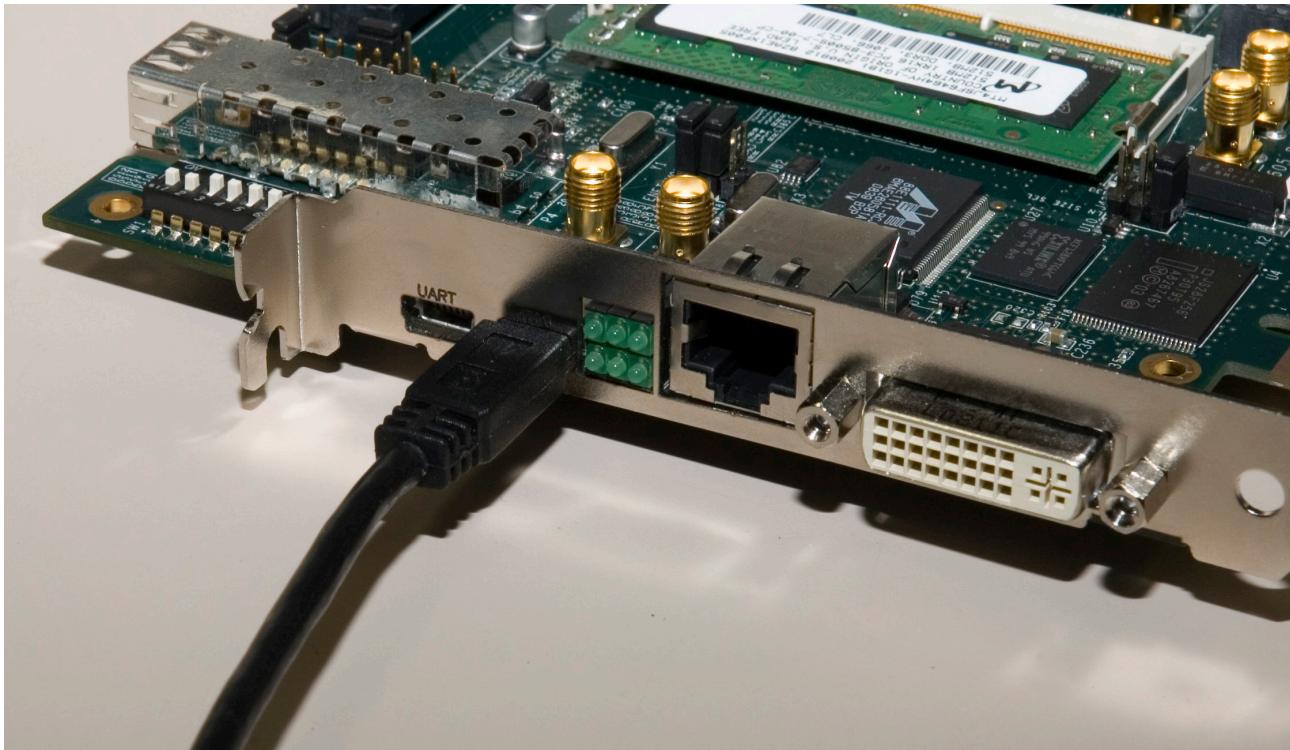
```
cd C:\ml605_mig_design\mig_37\example_design\par  
ise_flow.bat
```



The screenshot shows a Windows Command Prompt window titled "ISE Design Suite Command Prompt". The window has a blue header bar with the title and standard window controls. The main area is black and contains white text. The text shows the command being run:  
C:\Xilinx\13.1\ISE\_DS>cd C:\ml605\_mig\_design\mig\_37\example\_design\par  
C:\ml605\_mig\_design\mig\_37\example\_design\par>ise\_flow.bat

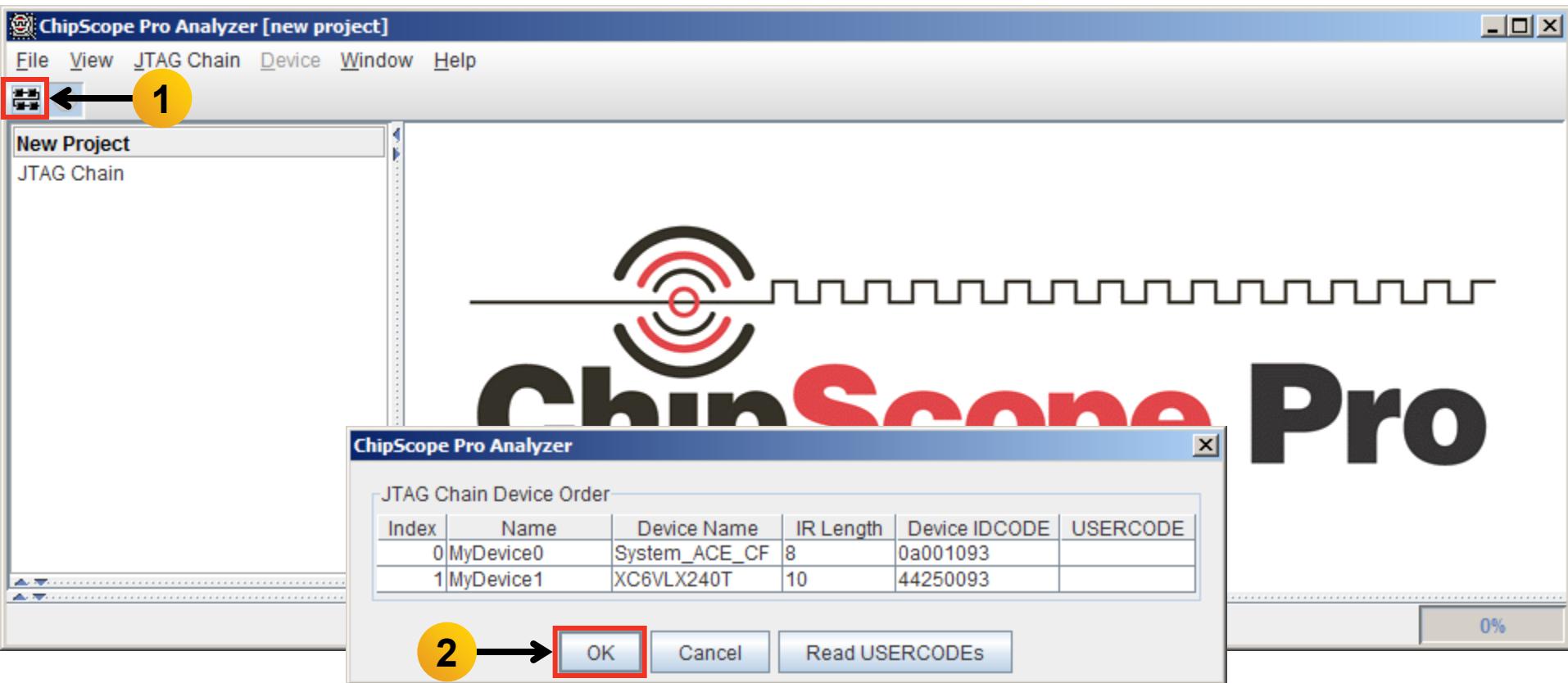
# Run MIG Example Design

- **Power on the ML605 board**
- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
  - Connect this cable to your PC



# Run MIG Example Design

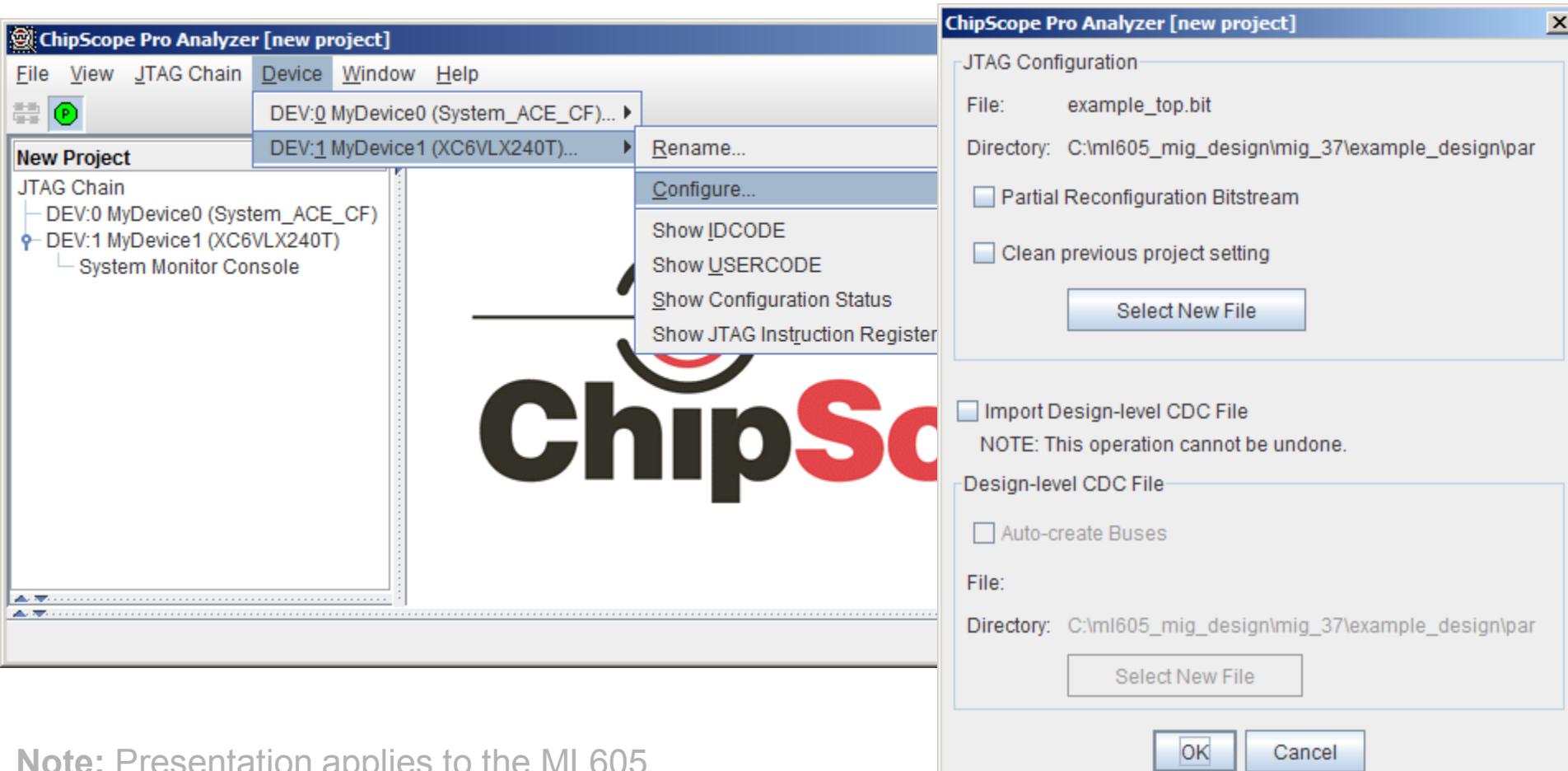
- After the design compiles, open ChipScope Pro Analyzer
  - Click on the Open Cable Button (1)
  - Click OK (2)



Note: Presentation applies to the ML605

# Run MIG Example Design

- Select Device → DEV:0 MyDevice0 (XC6VLX240T) → Configure...
- Select <Design Path>\mig\_37\example\_design\par\example\_top.bit



Note: Presentation applies to the ML605

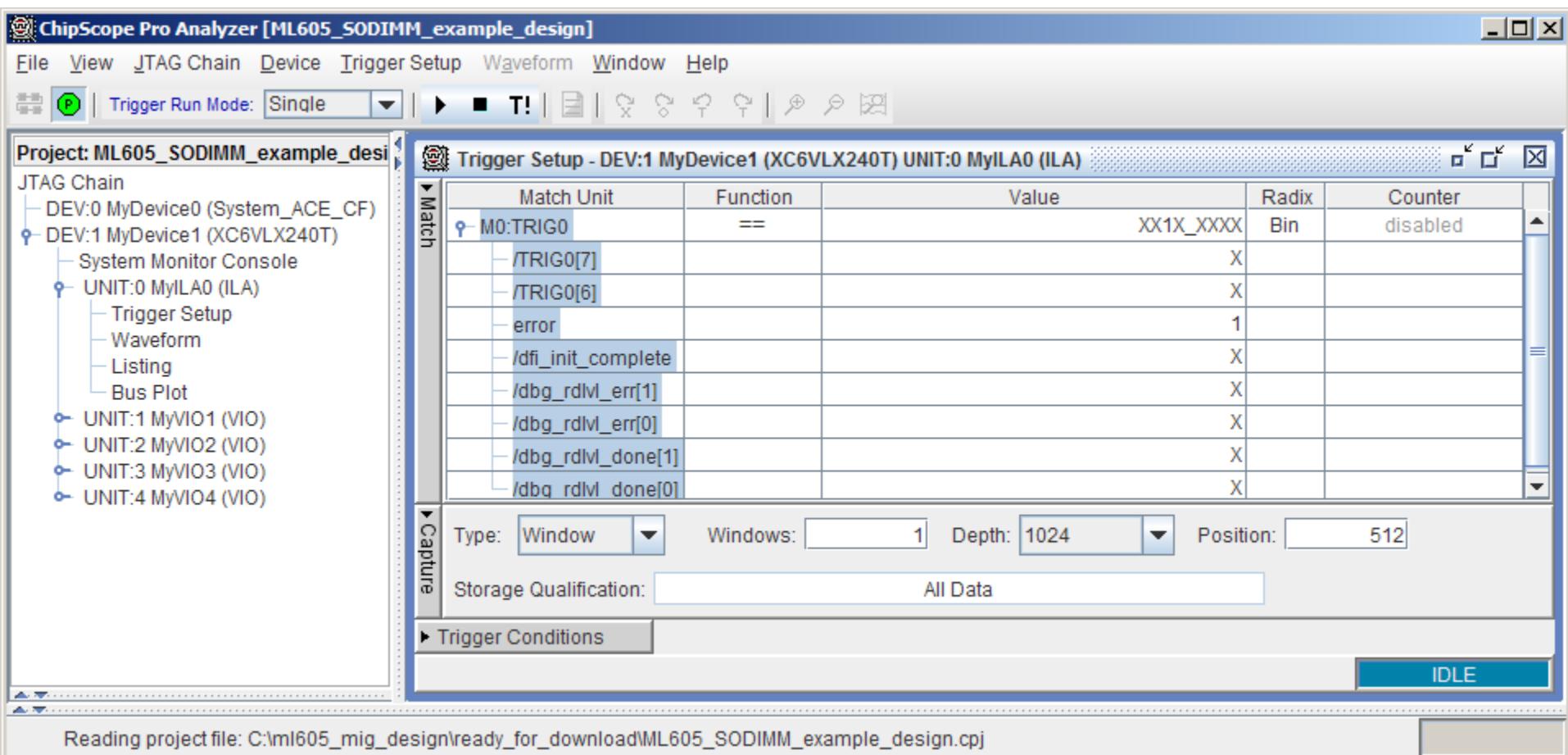
# Run MIG Example Design

- Select File → Open Project...
- Select <Design Path>\ready\_for\_download\ML605\_SODIMM\_example\_design.cpj



# Run MIG Example Design

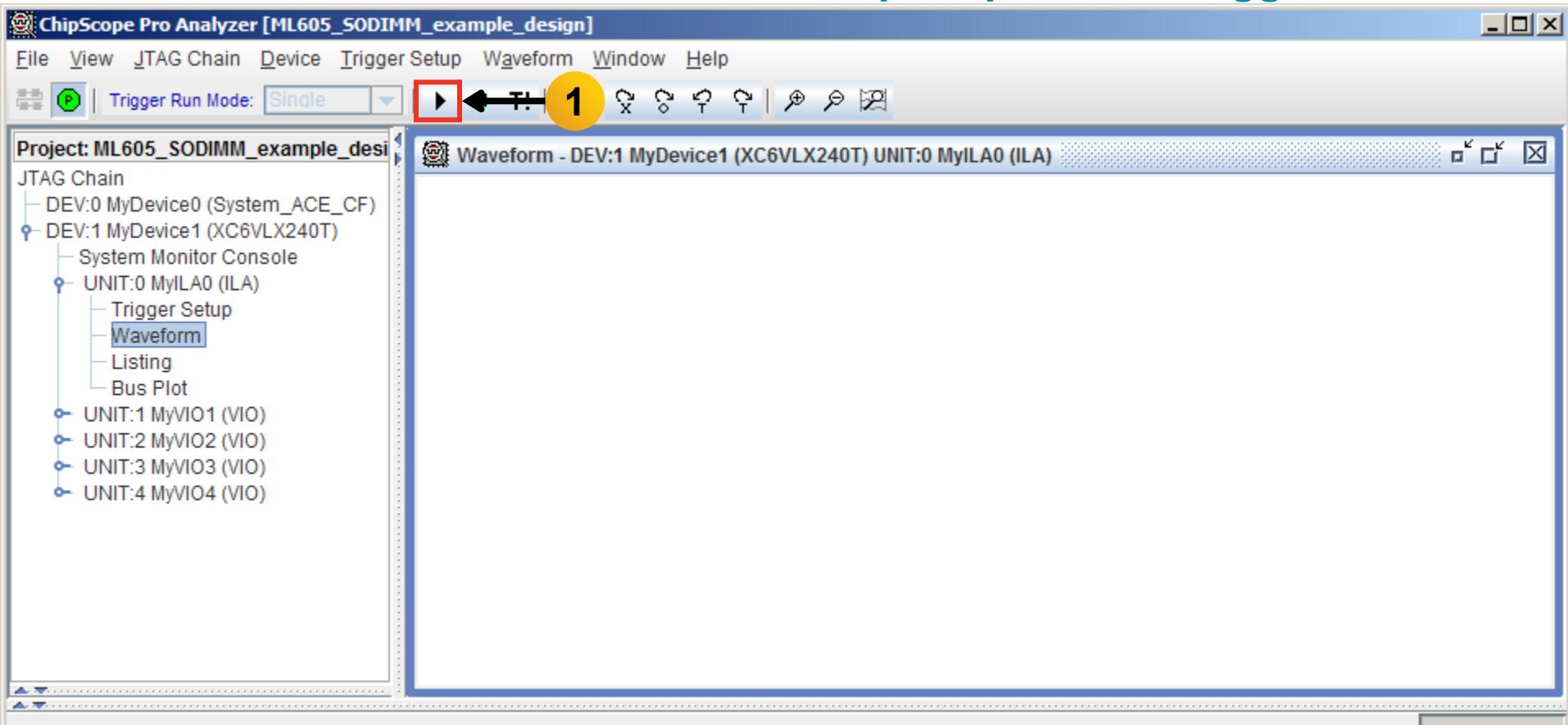
- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1



Note: Presentation applies to the ML605

# Run MIG Example Design

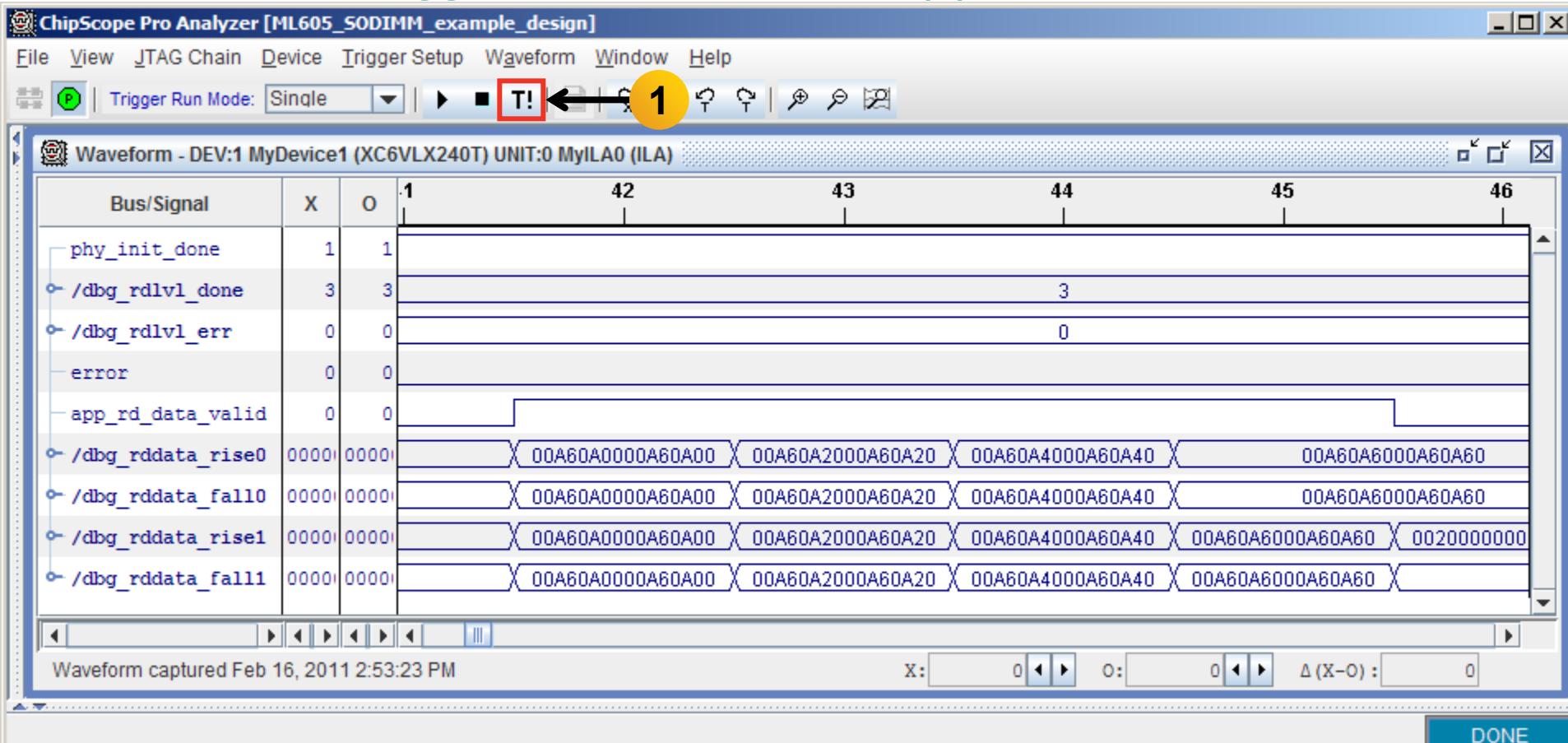
- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



Note: Presentation applies to the ML605

# Run MIG Example Design

- The Example Design should run error free (no trigger on error)
- To force a trigger, click the T! button (1)



# Adjust Data Pattern using VIO Console

- Select VIO Console 4
- Set tg\_mod\_en\_sel to 1

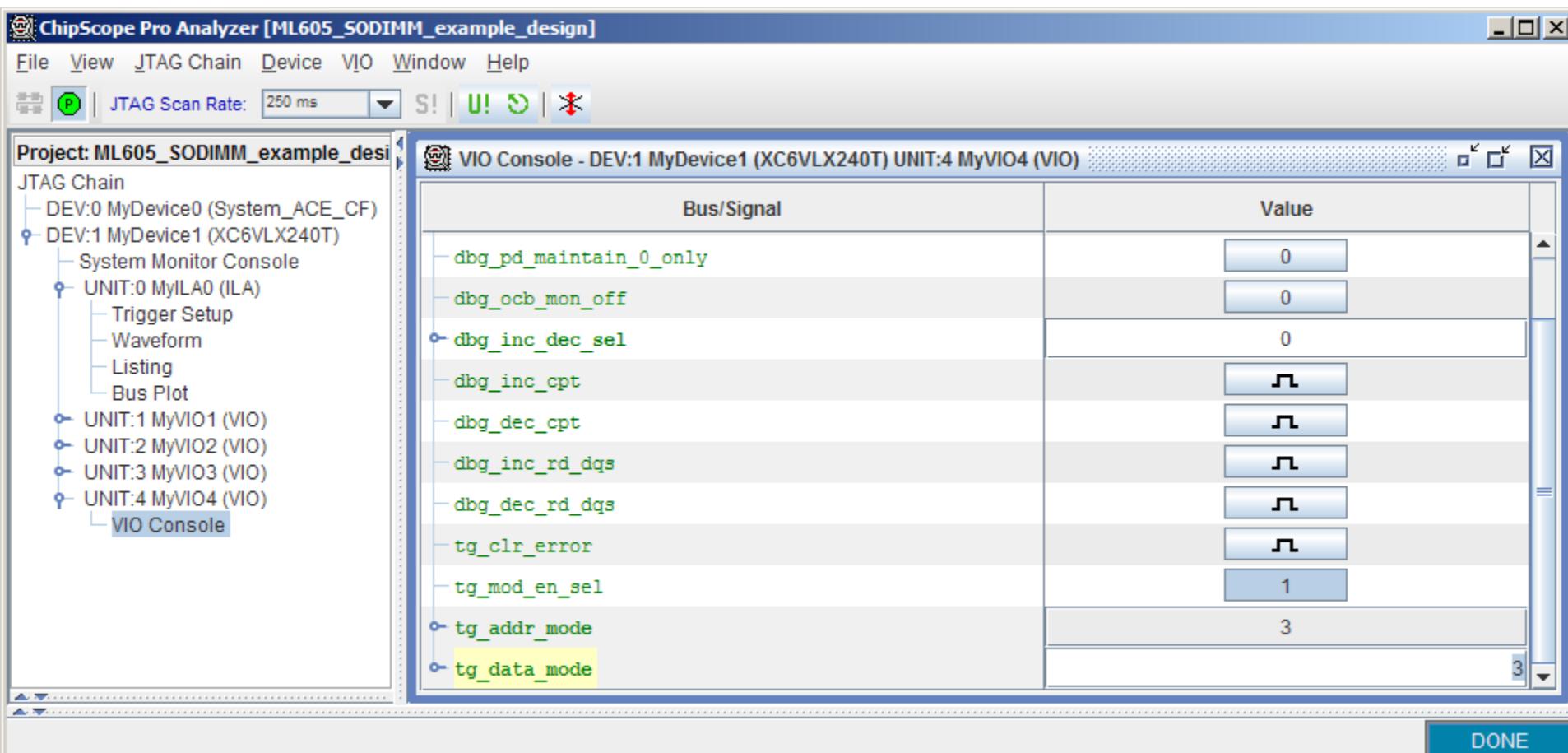
The screenshot shows the ChipScope Pro Analyzer interface with the project "ML605\_SODIMM\_example\_design". The left sidebar displays the JTAG Chain, with "UNIT:4 MyVIO4 (VIO)" selected. The main window shows the "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)" configuration table. The table lists various bus signals and their current values. The value for "tg\_mod\_en\_sel" is highlighted with a red box and set to 1.

Bus/Signal	Value
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	Λ
dbg_dec_cpt	Λ
dbg_inc_rd_dqs	Λ
dbg_dec_rd_dqs	Λ
tg_clr_error	Λ
tg_mod_en_sel	1
tg_addr_mode	3
tg_data_mode	2

DONE

# Adjust Data Pattern using VIO Console

- Set `tg_data_mode` to “3” for `HAMMER_DATA_MODE`



Note: Presentation applies to the ML605

# Adjust Data Pattern using VIO Console

- Select VIO Console 1
- Note error is active

The screenshot shows the ChipScope Pro Analyzer interface. The left pane displays the JTAG Chain for the project "ML605\_SODIMM\_example\_design". The right pane is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)". This window lists various bus signals and their current values. The "error" signal is highlighted with a red circle, indicating an active error condition.

Bus/Signal	Value
dbg_rdlvl_done[0]	Green (1)
dbg_rdlvl_done[1]	Green (1)
dfl_init_complete	Green (1)
rst_pll_ck_fb	Grey (0)
error	Red (1)
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06
dbg_wl_odelay_dqs_tap_cnt_1	10
dbg_wl_odelay_dq_tap_cnt_1	08

DONE

Note: Presentation applies to the ML605

# Adjust Data Pattern using VIO Console



- Press and release the CPU RESET switch, SW10, after each change to tg\_mod\_en\_sel or tg\_data\_mode

# Adjust Data Pattern using VIO Console

- Error is now cleared

The screenshot shows the ChipScope Pro Analyzer interface. The left pane displays the JTAG Chain for the project "ML605\_SODIMM\_example\_design". The right pane shows the "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)" window. This window contains a table of bus signals and their current values.

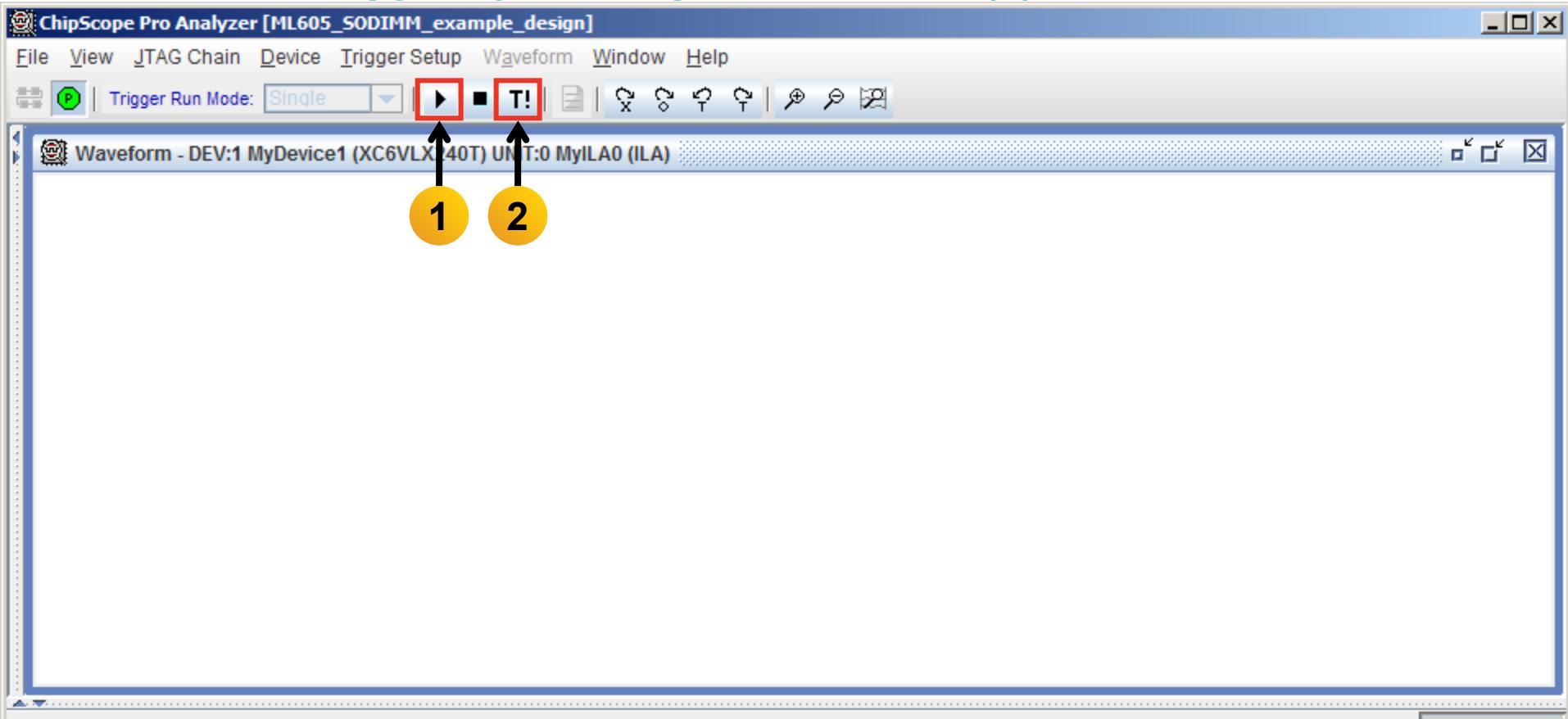
Bus/Signal	Value
dbg_rdlvl_done[0]	Green (1)
dbg_rdlvl_done[1]	Green (1)
dfl_init_complete	Green (1)
rst_pll_ck_fb	Grey (0)
error	Grey (0)
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06
dbg_wl_odelay_dqs_tap_cnt_1	10
dbg_wl_odelay_dq_tap_cnt_1	08

DONE

Note: Presentation applies to the ML605

# Adjust Data Pattern using VIO Console

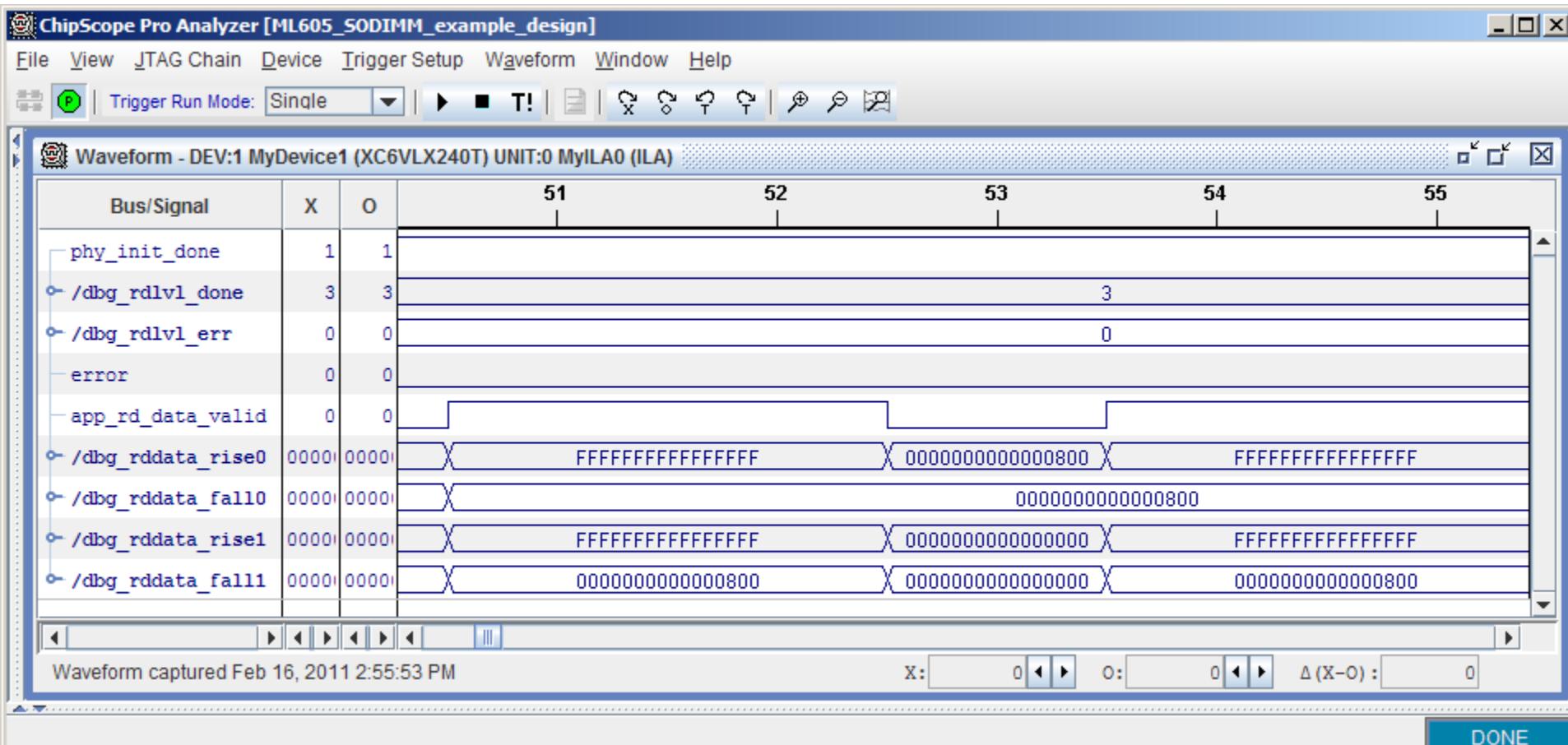
- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)



# Adjust Data Pattern using VIO Console

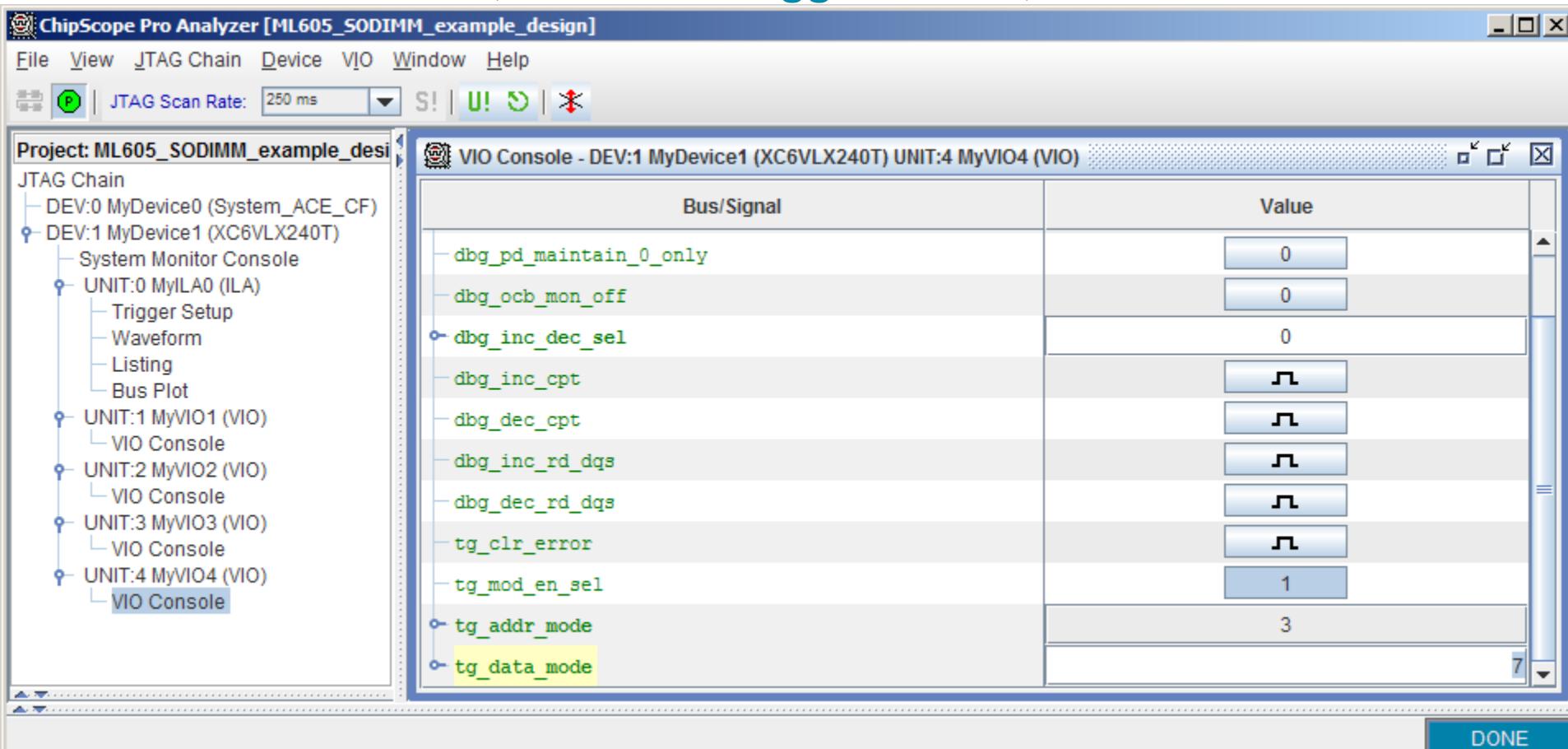
## ▪ Hammer PRBS Data Mode

- 64 bit DQ data bus hammer pattern



# Adjust Data Pattern using VIO Console

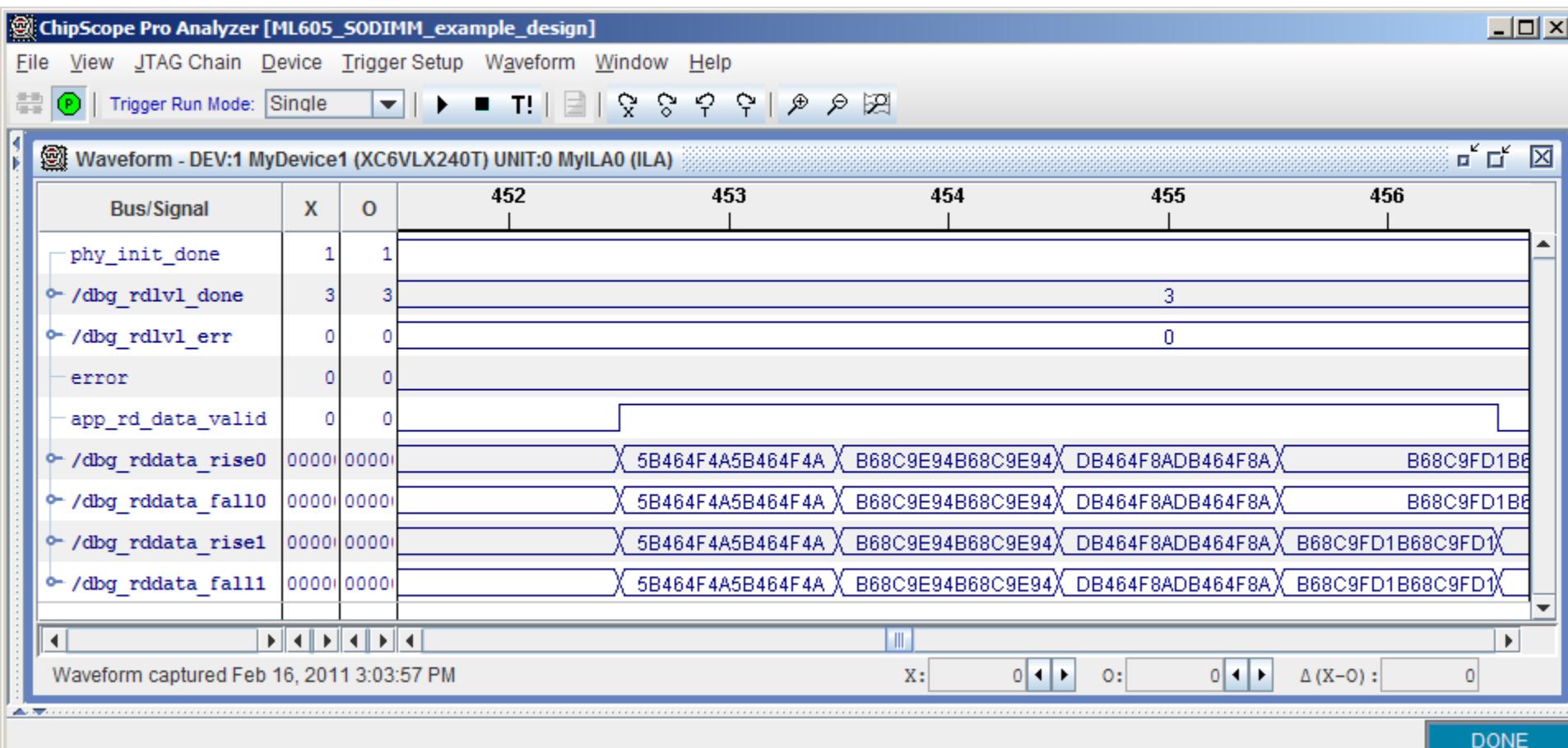
- Set `tg_data_mode` to “7” for PRBS data pattern
- Push CPU Reset, click Arm Trigger button, click T! button



Note: Presentation applies to the ML605

# Adjust Data Pattern using VIO Console

## ▪ PRBS Data Mode



Note: Presentation applies to the ML605

# Example Design VIO Consoles

- **Useful for PHY layer logic debug and status**
- **Available if “debug” option is checked in MIG GUI**
  - Monitor PHY outputs
    - Status of write calibration
    - Status of read calibration
  - Phase detector control
  - Read data capture clock adjustment
  - Disable selected PHY features
- **Reference documentation in UG406**
  - “PHY Layer Debug Port” section
  - Table 1-25 for signal definitions and descriptions
- **VIO port assignments (4 cores) defined in “example\_top.v”**

# Example Design VIO Consoles

The screenshot shows the ChipScope Pro Analyzer interface with a VIO Console window open. The window title is "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. A toolbar below the menu has icons for power, JTAG scan rate (set to 250 ms), and error status (S!, U!, C!, E!). The main area is a table titled "VIO Console" with columns "Bus/Signal" and "Value". The table lists various signals with their current values:

Bus/Signal	Value
dbg_rdlvl_done[0]	●
dbg_rdlvl_done[1]	●
dfl_init_complete	●
rst_pll_ck_fb	●
error	●
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0D
dbg_wl_odelay_dq_tap_cnt_0	05
dbg_wl_odelay_dqs_tap_cnt_1	0E
dbg_wl_odelay_dq_tap_cnt_1	06
dbg_wl_odelay_dqs_tap_cnt_2	0D
dbg_wl_odelay_dq_tap_cnt_2	05
dbg_wl_odelay_dqs_tap_cnt_3	0E
dbg_wl_odelay_dq_tap_cnt_3	06
dbg_wl_odelay_dqs_tap_cnt_4	0F

A "DONE" button is at the bottom right of the table.

## ■ VIO Console 1

- Write Path Calibration Status
- Read Leveling Done, Read Leveling Error
- Initialization complete, PLL reset
- Note: Press CPU RESET to clear error status in this VIO console

# Example Design VIO Consoles

The screenshot shows the ChipScope Pro Analyzer interface with the title bar "ChipScope Pro Analyzer [ML605\_SODIMM\_example\_design]". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. A toolbar below the menu bar includes icons for JTAG Scan Rate (set to 250 ms), Stop, Run, and Exit. The main window is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:2 MyVIO2 (VIO)". It displays a table with two columns: "Bus/Signal" and "Value". The table lists various debug signals with their corresponding hex values:

Bus/Signal	Value
dbg_cpt_tap_cnt_0	12
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	14
dbg_cpt_tap_cnt_3	07
dbg_cpt_tap_cnt_4	07
dbg_cpt_tap_cnt_5	15
dbg_cpt_tap_cnt_6	08
dbg_cpt_tap_cnt_7	07
dbg_rd_active_dly	0C
dbg_rd_bitslip_cnt_0	3
dbg_rd_bitslip_cnt_1	3
dbg_rd_bitslip_cnt_2	3
dbg_rd_bitslip_cnt_3	2
dbg_rd_bitslip_cnt_4	2
dbg_rd_bitslip_cnt_5	3
dbg_rd_bitslip_cnt_6	2

A "DONE" button is located at the bottom right of the table area.

- **VIO Console 2 & VIO Console 3**
  - Read Path Calibration Status

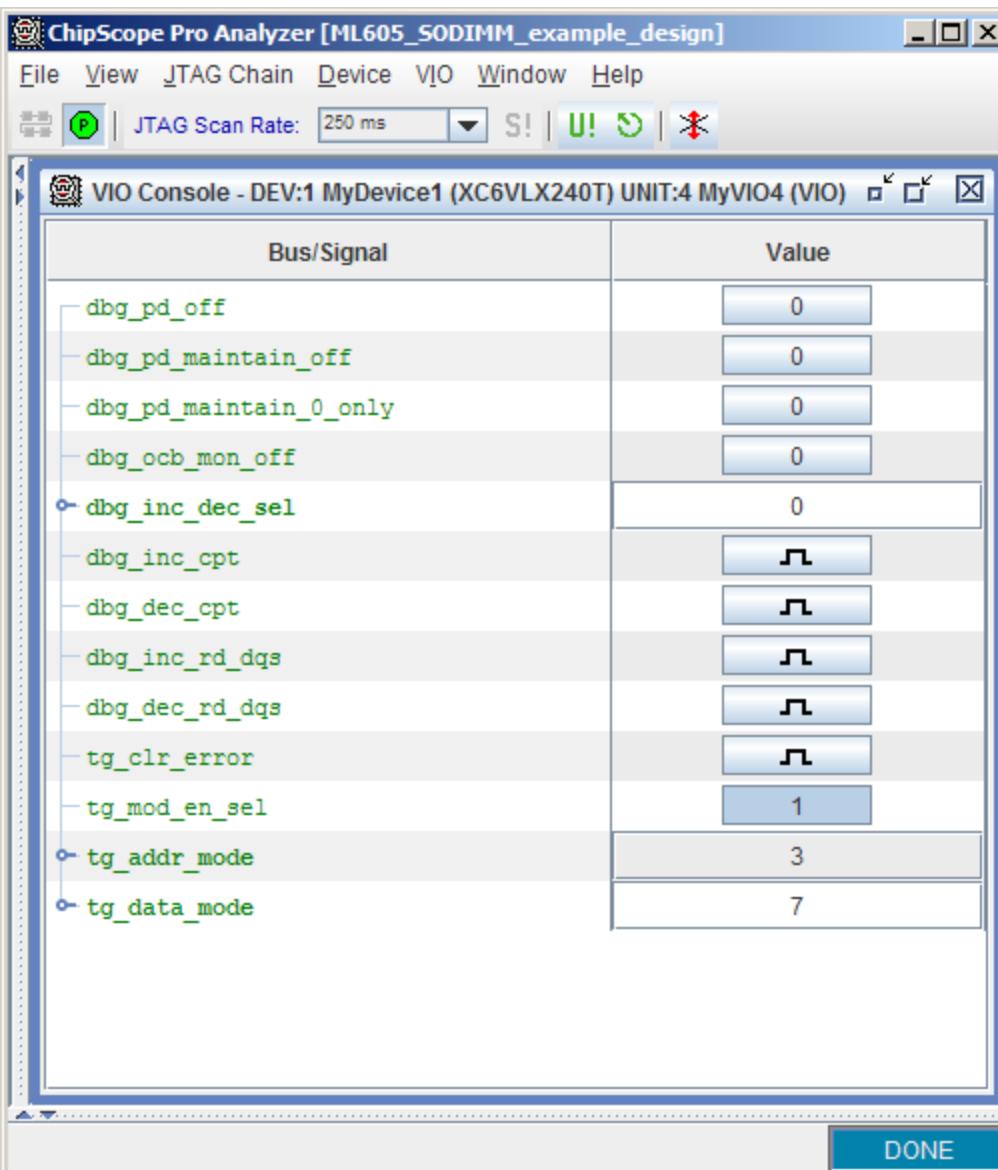
# Example Design VIO Consoles

The screenshot shows the ChipScope Pro Analyzer interface with the title bar "ChipScope Pro Analyzer [ML605\_SODIMM\_example\_design]". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. A toolbar below the menu bar includes icons for power, JTAG scan rate (set to 250 ms), and status indicators (S!, U!, C!, E!). The main window is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:3 MyVIO3 (VIO)". It displays a table with two columns: "Bus/Signal" and "Value". The table lists 16 entries, each starting with "dbg\_cpt\_" followed by a descriptive name and a value from 01 to 0C. The table has scroll bars on the right and bottom.

Bus/Signal	Value
dbg_cpt_first_edge_cnt_0	0C
dbg_cpt_second_edge_cnt_0	17
dbg_cpt_first_edge_cnt_1	0B
dbg_cpt_second_edge_cnt_1	17
dbg_cpt_first_edge_cnt_2	0E
dbg_cpt_second_edge_cnt_2	19
dbg_cpt_first_edge_cnt_3	01
dbg_cpt_second_edge_cnt_3	0C
dbg_cpt_first_edge_cnt_4	01
dbg_cpt_second_edge_cnt_4	0D
dbg_cpt_first_edge_cnt_5	0F
dbg_cpt_second_edge_cnt_5	1A
dbg_cpt_first_edge_cnt_6	02
dbg_cpt_second_edge_cnt_6	0D
dbg_cpt_first_edge_cnt_7	01
dbg_cpt_second_edge_cnt_7	0C

- **VIO Console 2 & VIO Console 3**
  - Read Path Calibration Status

# Example Design VIO Consoles



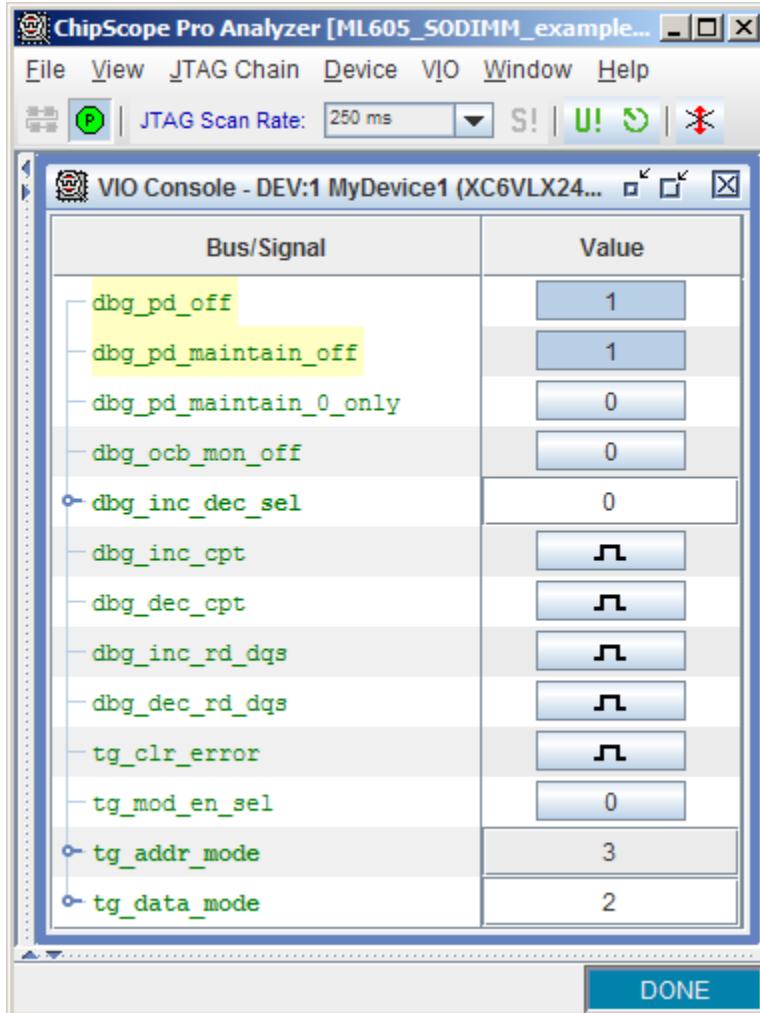
## ■ VIO Console 4

- Phase Detector Controls
- Read Data Capture Clock Adjustment

# Measure Read Data Window with VIO

## ▪ VIO Console 4

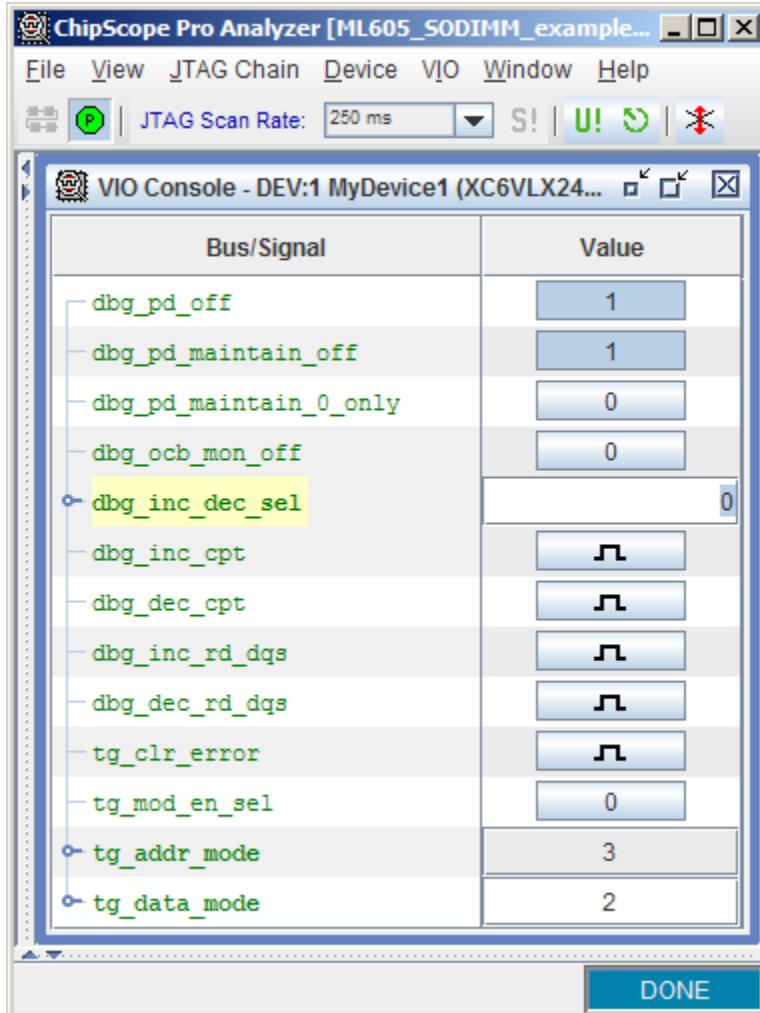
- Set **dbg\_pd\_off** to 1
- This turns off the Phase Detector
- Set **dbg\_pd\_maintain\_off** to 1
- This turns off the Phase Detector Maintenance



# Measure Read Data Window with VIO

## ▪ VIO Console 4

- Set **dbg\_inc\_dec\_sel** to 0
- This selects the data group (0, 1, 2, etc.,)



# Change tap delays to measure window

## ▪ Increment Taps

- Note the initial value of **dbg\_cpt\_tap\_cnt\_0**, in this case 11
- The error LED should be off

The screenshot shows three separate windows of the ChipScope Pro Analyzer interface, all titled "VIO Console - DEV:1 MyDevice1 (XC6...)".

- Left Window:** Shows a table of bus signals and their current values. The columns are "Bus/Signal" and "Value".

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	1
dbg_dec_cpt	1
dbg_inc_rd_dqs	1
dbg_dec_rd_dqs	1
- Middle Window:** Shows a table of bus signals and their current values. The column headers are "Bus/Signal" and "Value". The row for "dbg\_cpt\_tap\_cnt\_0" is highlighted with a red box.

Bus/Signal	Value
dbg_cpt_tap_cnt_0	11
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D
- Right Window:** Shows a table of bus signals and their current values. The column headers are "Bus/Signal" and "Value". The row for "error" is highlighted with a red box.

Bus/Signal	Value
dbg_rdlvl_done[0]	1
dbg_rdlvl_done[1]	1
dfl_init_complete	1
rst_pll_ck_fb	0
error	1
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

A "DONE" button is visible in the bottom right corner of the rightmost window.

# Change tap delays to measure window

## ▪ Increment Taps

- Increment tap delay by clicking on **dbg\_inc\_cpt** until an error occurs
- Note tap value that causes the error and subtract one:  $17 - 1 = 16$
- Take the difference of the final value and the initial value:  $16 - 11 = 5$

ChipScope Pro Analyzer [ML605\_SODIMM\_example\_design]

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	■
dbg_dec_cpt	■
dbg_inc_rd_dqs	■
dbg_dec_rd_dqs	■

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_cpt_tap_cnt_0	17
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D

VIO Console - DEV:1 MyDevice1 (XC6VL...)

Bus/Signal	Value
dbg_rdlvl_done[0]	■
dbg_rdlvl_done[1]	■
dfl_init_complete	■
rst_pll_ck_fb	■
error	■
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

DONE

# Change tap delays to measure window

## ▪ Reset using Switch SW10

- Press and release the CPU RESET switch
- Note that **dbg\_cpt\_tap\_cnt\_0** returns to its original value, 11
- The error LED should be off

The screenshot shows three separate windows of the ChipScope Pro Analyzer interface, all titled "VIO Console - DEV:1 MyDevice1 (XC6...)".

- Left Window:** Displays a table of bus signals and their current values. The columns are "Bus/Signal" and "Value".

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	1
dbg_dec_cpt	1
dbg_inc_rd_dqs	1
dbg_dec_rd_dqs	1
- Middle Window:** Displays a table of bus signals and their current values. The columns are "Bus/Signal" and "Value".

Bus/Signal	Value
dbg_cpt_tap_cnt_0	11
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D
- Right Window:** Displays a table of bus signals and their current values. The columns are "Bus/Signal" and "Value".

Bus/Signal	Value
dbg_rdlvl_done[0]	1
dbg_rdlvl_done[1]	1
dfl_init_complete	1
rst_pll_ck_fb	0
error	0
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

A red box highlights the value of **dbg\_cpt\_tap\_cnt\_0** in the middle window, and another red box highlights the value of **error** in the right window.

DONE

# Change tap delays to measure window

## ▪ Decrement Taps

- Decrement tap delays by clicking on **dbg\_dec\_cpt** until an error occurs
- Note tap value that causes the error and add one:  $0B + 1 = 0C$
- Take the difference of the initial value and the final value:  $11 - 0C = 5$

The screenshot shows three windows of the ChipScope Pro Analyzer interface, all titled "VIO Console - DEV:1 MyDevice1 (XC6...)".

- Left Window:** Shows a table with columns "Bus/Signal" and "Value". The "dbg\_dec\_cpt" row is highlighted with a yellow background and has a red box around its "Value" cell, which contains a switch icon.
- Middle Window:** Shows a table with columns "Bus/Signal" and "Value". The "dbg\_cpt\_tap\_cnt\_0" row is highlighted with a red box around its "Value" cell, which contains the value "0B". Other rows show values like 11, 13, 06, etc.
- Right Window:** Shows a table with columns "Bus/Signal" and "Value". The "error" row is highlighted with a red box around its "Value" cell, which contains a red circle icon.

**Bottom Right Corner:** A blue "DONE" button is visible.

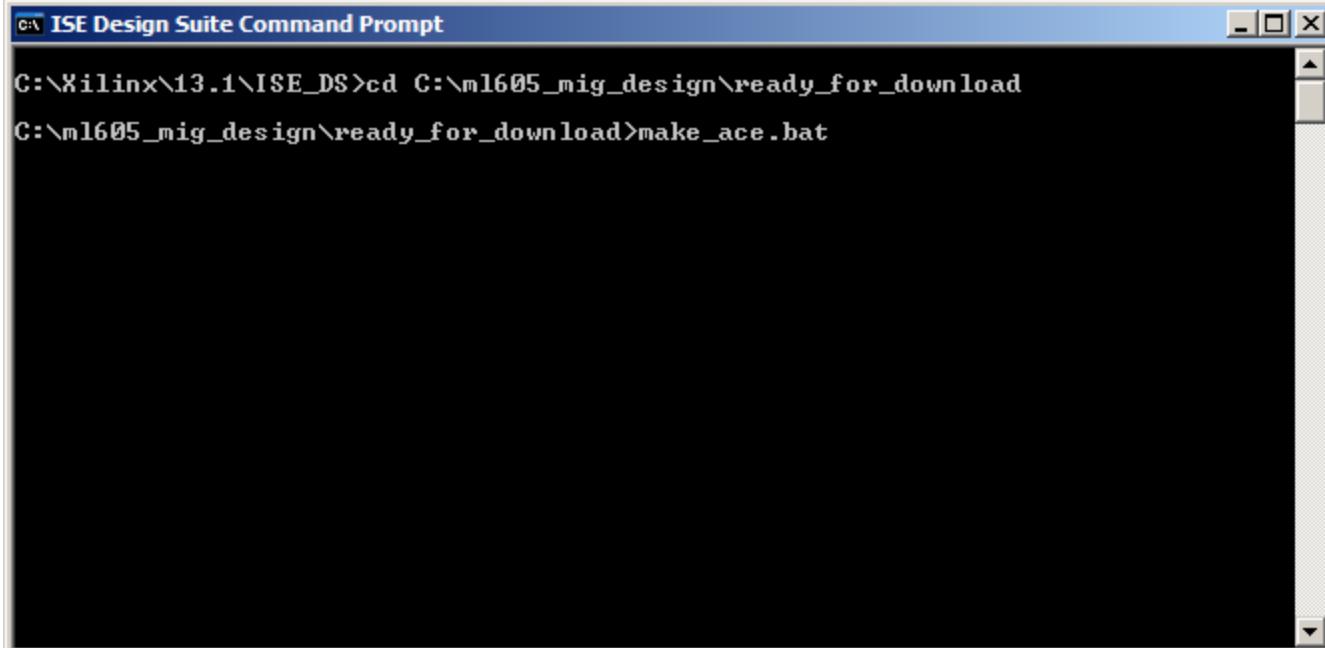
# Change tap delays to measure window

- Add the two values and multiply by the average tap delay:
  - $10 \times 78 \text{ ps} = 780 \text{ ps}$
- Total data period = 1250 ps (800 Mbps)
  - From [DS152](#), page 35: “Average Tap Delay at 200 MHz = 78 ps”

# Generate MIG ACE File (Optional)

- Type these commands in an ISE Design Suite Command Prompt:

```
cd C:\ml605_mig_design\ready_for_download  
make_ace.bat
```



The screenshot shows a Windows command prompt window titled "ISE Design Suite Command Prompt". The window contains the following text:

```
C:\Xilinx\13.1\ISE_DS>cd C:\ml605_mig_design\ready_for_download  
C:\ml605_mig_design\ready_for_download>make_ace.bat
```

# References

# References

## ▪ Virtex-6 Memory

- Virtex-6 FPGA Memory Interface Solutions User Guide – UG406  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ug406.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ug406.pdf)
- Virtex-6 FPGA Memory Interface Solutions – DS186  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ds186.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ds186.pdf)
- Virtex-6 FPGA Data Sheet: DC and Switching Characteristics – DS152  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds152.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf)

# Documentation

# Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

- <http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Getting Started Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug533.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug533.pdf)

- ML605 Hardware User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug534.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf)

- ML605 Reference Design User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug535.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf)