Summary - IQStream Max Calculator

Name	iqstream_max_calculator
Worker Type	Application
Version	v1.4
Release Date	October 2018
Component Library	ocpi.assets.util_comps
Workers	iqstream_max_calculator.hdl, iqstream_max_calculator.rcc
Tested Platforms	ml605, centos7

Functionality

in/out ports

Messages are passed directly from the `in` port to the `out` port. Backpressure is transfered to the `in` port from the `out` port.

max_I_is_valid Property

Indicates `max_I` is valid. Will be false if no data has been received on `in\verb` port since either a) the last read of `max_I` or b) the worker first went into the operating state.

max_Q_is_valid Property

Indicates `max_Q` is valid. Will be false if no data has been received on `in` port since either a) the last read of `max_I` or b) the worker first went into the operating state.

max_I Property

Max I value observed on `in` port. Value will be -32768 when worker first enters the operating state and will be reset to -32768 after each read. `max_I_is_valid` should always be read prior to reading this property because `max_I_is_valid` will immediately be set to false once `max_I` is read.

max_Q Property

Max Q value observed on `in` port. Value will be -32768 when worker first enters the operating state and will be reset to -32768 after each read. `max_Q_is_valid` should always be read prior to reading this property because `max_I_is_valid` will immediately be set to false once `max_Q` is read.

Worker Implementation Details

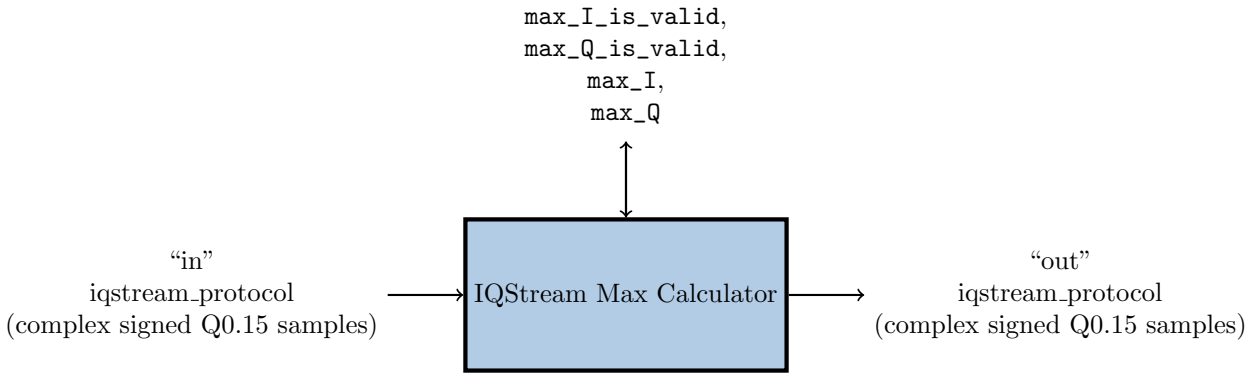
iqstream_max_calculator.hdl

The iqstream_max_calculator.hdl worker has `IDATA_WIDTH_p` and `ODATA_WIDTH_p` parameter properties which facilitate the build parameterization of DataWidth of the `in` and `out` ports.

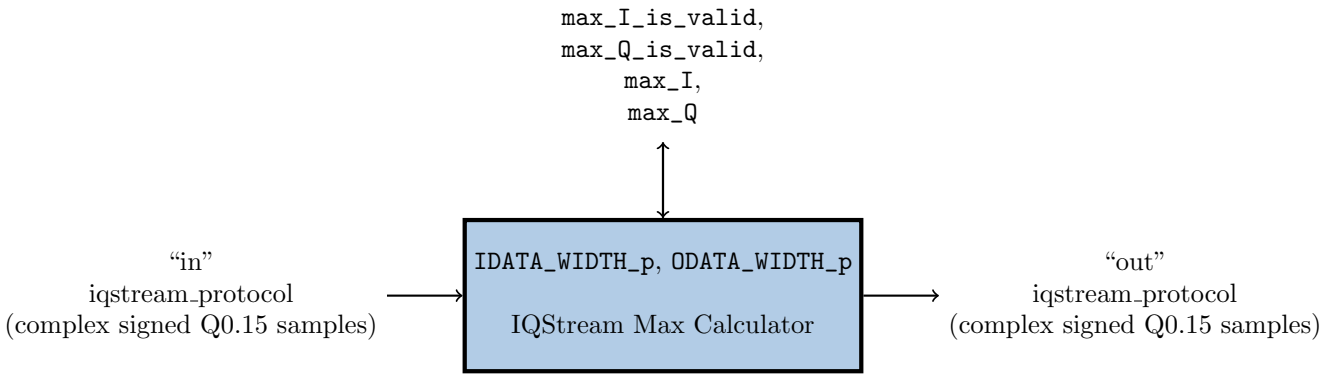
Block Diagrams

Top level

iqstream_max_calculator.rcc



iqstream_max_calculator.hdl



Source Dependencies

iqstream_max_calculator.rcc

assets/components/util_comps/iqstream_max_calculator.hdl/iqstream_max_calculator.cc

iqstream_max_calculator.hdl

assets/components/util_comps/iqstream_max_calculator.hdl/iqstream_max_calculator.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
max_I_is_valid	bool	-	-	Volatile	-	-	Indicates `max_I` is valid.
max_Q_is_valid	bool	-	-	Volatile	-	-	Indicates `max_Q` is valid.
max_I	short	-	-	Volatile	-	-	Max I value observed on in port.
max_Q	short	-	-	Volatile	-	-	Max Q value observed on in port.

Worker Properties

iqstream_max_calculator.hdl

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
IDATA_WIDTH_p	ushort	-	-	Parameter	-	32	-
ODATA_WIDTH_p	ushort	-	-	Parameter	-	32	-

iqstream_max_calculator.rcc

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
max_I	-	-	-	ReadSync	-	-	-
max_Q	-	-	-	ReadSync	-	-	-

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	iqstream_protocol.xml	False	-	-
out	true	iqstream_protocol.xml	true	-	-

Worker Interfaces

iqstream_max_calculator.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	`IDATA_WIDTH_p`	-	-
StreamInterface	out	`ODATA_WIDTH_p`	-	-

Control Timing and Signals

iqstream_max_calculator.hdl

Data is passed from the input port to the output port with the minimum possible latency. In the absence of backpressure, this latency is one clock cycle. Note that, in the absence of backpressure, all input ports have a latency of one clock cycle.

Worker Configuration Parameters

iqstream_max_calculator.hdl

Table 1: Table of Worker Configurations for worker: iqstream_max_calculator

Configuration
0

Performance and Resource Utilization

iqstream_max_calculator.rcc

iqstream_max_calculator.hdl

Table 2: Resource Utilization Table for worker: iqstream_max_calculator

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	zynq	Vivado	2017.1	xc7z020clg400-3	165	146	N/A	N/A
0	virtex6	ISE	14.7	6vcx75tff484-2	162	348	489.093	N/A
0	stratix4	Quartus	17.1.0	N/A	131	252	N/A	N/A

Test and Verification

No unit test for this component exists. However, a hardware-in-the-loop application (which is NOT a unit test) exists for testing purposes (see assets/applications/iqstream_max_calculator_test).