Summary - Complex Mixer (TimeStamped)

Name	complex_mixer_ts
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets_ts.components
Workers	complex_mixer_ts.hdl
Tested Platforms	xsim, isim, modelsim, Matchstiq-Z1(PL)

Functionality

The Complex Mixer consists of a Numerically Controlled Oscillator (NCO) and a complex multiplier. Complex IQ data is received on the input port and is multiplied with the output of the NCO and put on the output port.

Worker Implementation Details

complex_mixer_ts.hdl

Figure 1 diagrams the complex mixer.

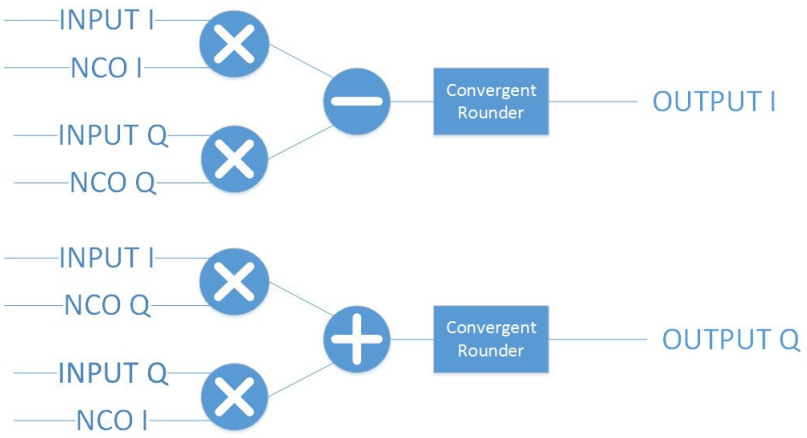

Figure 1: Complex Mixer Functional Diagram

Build time parameters can be used to control the width of the NCO data output, the width of the input data, and the number of stages in the Coordinate Rotation Digital Computer (CORDIC) used to implement the NCO. Additionally, there is a parameter to control insertion of a peak detection circuit.

An `enable` input is available to either enable (true) or bypass (false) the circuit. In bypass mode, pipe-lining registers are not used. FPGA multipliers are used to process input data at the full clock rate. This worker will produce valid output two clock cycles after each valid input.

Theory

The Complex Mixer worker inputs complex signed samples and performs a complex multiply with a digital sine wave produced by an numerically controlled oscillator (NCO). The resulting output data is a frequency shifted version of the input data.

The magnitude of the frequency shift is determined by the output frequency of the NCO, which can be calculated with the following equation:

$$nco\_output\_freq = sample\_freq * \frac{phs\_inc}{2^{phs\_acc\_width}} \tag{1}$$

In this component, `phs_inc` is runtime configurable and has a data type of 16 bit signed short. `phs_acc_width` is fixed at 16. The input clock frequency is the sample rate of the samples. The amplitude of the NCO's sine wave is also runtime configurable via the `mag` property. Note that the `mag` property value should only ever be set to a value within the following range in order for the worker to operate properly.

$$-2^{(NCO\_DATA\_WIDTH\_p-1)} <= mag <= 2^{(NCO\_DATA\_WIDTH\_p-1)} - 1 \tag{2}$$

A positive and negative `phs_inc` will mix up and down, respectively. The following equation can be used as an aid for setting the `phs_inc` to have the desired mixing affect.

$$x_{out}[n] = x_{in}[n] * \frac{mag}{2^{NCO\_DATA\_WIDTH\_p-1}} * e^{\left(j2\pi\left(sample\_freq*\frac{phs\_inc\ *\ n}{2^{phs\_acc\_width}}\right)+phs\_init\right)} \quad \forall\ n,\ n \geq 0 \tag{3}$$

Block Diagrams

Top level

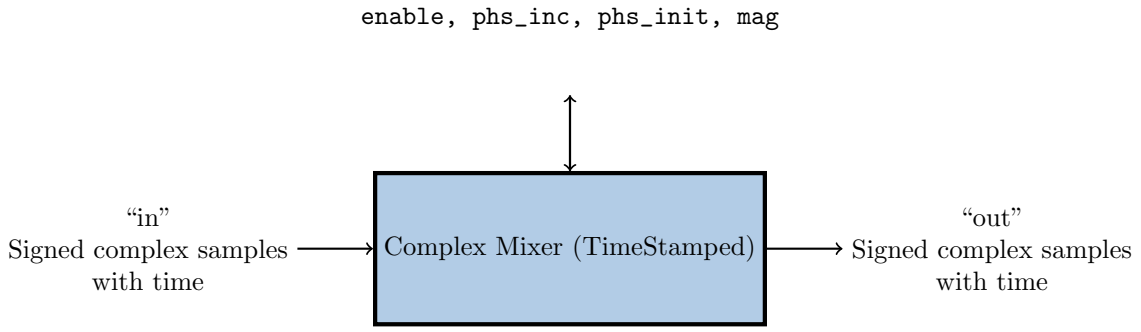

Figure 2: Complex Mixer Top Level Block Diagram

Source Dependencies

complex_mixer_ts.hdl

- projects/assets_ts/components/complex_mixer.hdl/complex_mixer.vhd
- projects/assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  - projects/assets/hdl/primitives/dsp_prims/nco/src/nco.vhd
  - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic_pr.vhd
  - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic.vhd
  - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic_stage.vhd
- projects/assets/hdl/primitives/util_prims/util_prims_pkg.vhd
  - projects/assets/hdl/primitives/util_prims/mult/src/complex_mult.vhd
  - projects/assets/hdl/primitives/util_prims/pd/src/peakDetect.vhd
- projects/assets/hdl/primitives/misc_prims/misc_prims_pkg.vhd
  - projects/assets/hdl/primitives/misc_prims/round_conv/src/round_conv.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
enable	bool	-	-	Writable	-	true	Enable(true) or bypass(false) mixer
phs_inc	short	-	-	Writable	-	-4096	Phase increment of NCO

Worker Properties

complex_mixer_ts.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	NCO_DATA_WIDTH_p	uchar	-	-	Parameter	12/16	12	Output data width of NCO
Property	INPUT_DATA_WIDTH_p	uchar	-	-	Parameter	12/16	12	Input port data width
Property	CORDIC_STAGES_p	uchar	-	-	Parameter	16	16	Number of CORDIC stages implemented in NCO
Property	PEAK_MONITOR_p	bool	-	-	Parameter	-	true	Include peak monitor circuit
Property	LATENCY_p	ushort	-	-	Parameter	2	2	Number of clock cycles between a valid input and a valid output
Property	peak	short	-	-	Volatile	-	-	Output of peak detector
Property	phs_init	ushort	-	-	Writable	-	0	Initial phase of NCO
Property	mag	ushort	-	-	Writable	-	1024	Magnitude of NCO output

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	-	Complex_Short_With_Metadata	-	-	Signed complex samples
out	-	Complex_Short_With_Metadata	-	-	Signed complex samples

Worker Interfaces

complex_mixer_ts.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	-	Signed Complex Samples
Type	Name	DataWidth	Advanced	Usage
StreamInterface	out	32		Signed Complex Samples

Control Timing and Signals

The Complex Mixer HDL worker uses the clock from the Control Plane and standard Control Plane signals.

There is a startup delay for this worker. Once the input is ready and valid and the output is ready, there is a delay of `CORDIC_STAGES_p`+1 before the first sample is taken. After this initial delay, valid output data is given 2 clock cycles after input data is taken.

Latency
2 clock cycles

Worker Configuration Parameters

complex_mixer_ts.hdl

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Table 1: Table of Worker Configurations for worker: complex_mixer_ts

Configuration	INPUT_DATA_WIDTH_p	NCO_DATA_WIDTH_p
0	12	12
1	16	16

Performance and Resource Utilization

Table 2: Resource Utilization Table for worker "complex_mixer_ts"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	N/A	1432	1823	N/A	DSP18: 8
0	zynq_ise	ISE	14.7	7z010clg400-3	1382	2928	293.703	DSP48E1: 6
0	virtex6	ISE	14.7	6vcx75tff484-2	1383	2971	263.336	DSP48E1: 6
0	zynq	Vivado	2017.1	xc7z020clg400-3	1360	2676	N/A	DSP48E1: 6
1	stratix4	Quartus	17.1.0	N/A	1636	2029	N/A	DSP18: 12
1	zynq_ise	ISE	14.7	7z010clg400-3	1578	3442	220.985	DSP48E1: 8
1	virtex6	ISE	14.7	6vcx75tff484-2	1578	3442	195.385	DSP48E1: 8
1	zynq	Vivado	2017.1	xc7z020clg400-3	1590	3221	N/A	DSP48E1: 6

Test and Verification

Test cases are derived from the number of properties, and their respective values, as listed in the complex_mixer_ts-test.xml.

1) Bypass: The input data is forwarded to the output port. For verification of this case, the output file is byte-wise compared to the input file.

2) Normal mode: Input data is generated by first creating a *.dat input file containing all of the operations of the Complex_Short_With_Metadata protocol in the following sequence:

    1. Interval
    2. Sync (this opcode is expected after an Interval operation)
    3. Time
    4. Samples (tone with configurable length and magnitude)
    5. Flush
    6. Samples (tone with configurable length and magnitude)
    7. Sync
    8. Samples (tone with configurable length and magnitude)

    The samples messages consist of a tone with configurable length and magnitude.

    The NCO is configured to tune the input samples operations to baseband. For verification, an FFT of the output data is performed and the max value of the FFT is checked to be at DC (0 Hz).

    The worker will pass through all operations of the Complex_Short_With_Metadata protocol. During sync operations, the NCO is reset.