Summary - matchstiq_z1 Platform

Name	matchstiq_z1
Worker Type	Platform
Version	v1.4
Release Date	February 2018
Component Library	ocpi.assets.platforms
Workers	matchstiq_z1.hdl
Tested Platforms	matchstiq_z1(PL)

Functionality

The Matchstiq-Z1 Platform Worker is the interface between the Processing System and the FPGA on the Matchstiq-Z1 Platform. It makes the connections between the AXI buses on the ARM and the OpenCPI Control and Data Planes. Optionally, it can also be used to interface with the SPI, I2C, and UART buses with device workers.

Worker Implementation Details

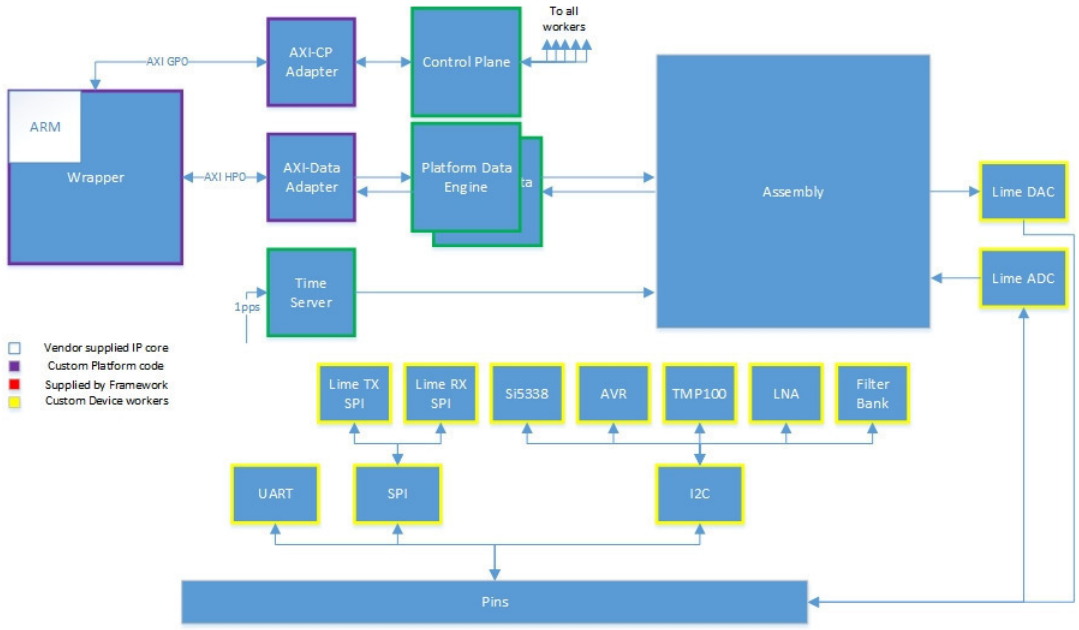


Figure 1: Top Level Block Diagram

The Matchstiq-Z1 platform has several peripherals connected to the FPGA. To incorporate these peripherals into the OpenCPI framework, HDL device workers and Software control proxy workers needed to be written. A overview of these software control proxy workers and HDL Device workers and their interactions can be seen in the diagram below :

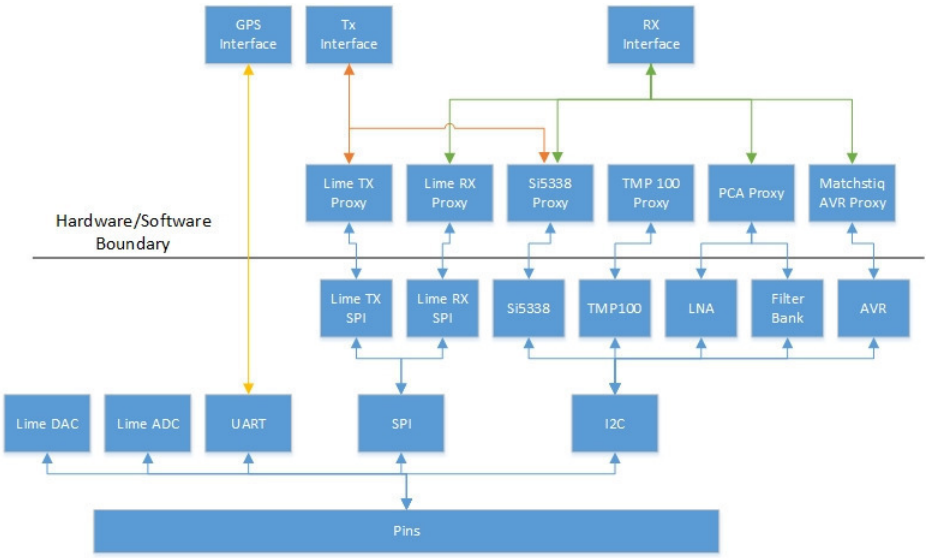


Figure 2: Device Worker & Proxy Diagram

Common Interfaces

This platform has three different software interfaces, the Rx Interface, Tx interface, and GPS Interface. The control of the SDR should use these interfaces in order to maintain commonality between different platforms. More information on each of these interfaces can be found in their respective data sheets.

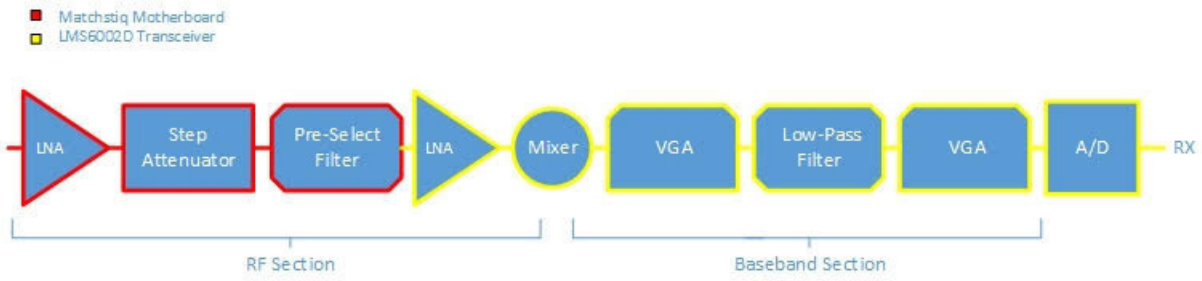


Figure 3: Receiver Hardware Diagram

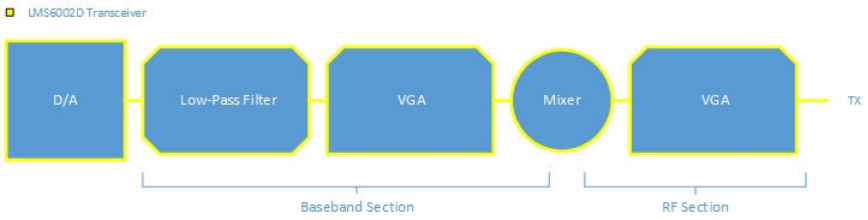


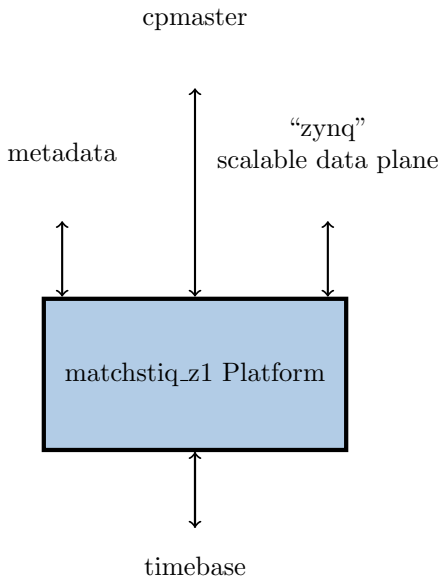
Figure 4: Transmitter Hardware Diagram

Theory

Because there are no data processing algorithms implemented in this worker, no corresponding data processing theory is relevant herein.

Block Diagrams

Top level



State Machines

Various state machines exist in the zynq, axi, and sdp primitive libraries. See primitive library source code for details. The explicit source code files included in the aforementioned primitives are enumerated in the following section.

Source Dependencies:

- assets/hdl/platforms/matchstiq_z1/matchstiq_z1.vhd
- assets/hdl/primitives/zynq/zynq_pkg.vhd
- assets/hdl/primitives/zynq/zynq_ps.vhd
- assets/hdl/primitives/axi/axi_pkg.vhd
- assets/hdl/primitives/axi/axi2cp.vhd
- assets/hdl/primitives/sdp/sdp2axi_rd.vhd
- assets/hdl/primitives/sdp/sdp2axi.vhd
- assets/hdl/primitives/sdp/sdp2axi_wd.vhd
- assets/hdl/primitives/sdp/sdp_axi_pkg.vhd
- assets/hdl/primitives/sdp/sdp_pkg.vhd
- assets/hdl/primitives/sdp/sdp_body.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
platform	String	31	-	Parameter	Standard	-	Name of this platform
sdp_width	UChar	-	-	Parameter	Standard	1	Width of data plane in DWORDS
UUID	ULong	-	16	Readable	Standard	-	UUID of this platform
oldtime	ULongLong	-	-	Padding	Standard	-	N/A
romAddr	UShort	-	-	Writable	Standard	-	
romData	ULong	-	-	Volatile	Standard	-	
nSwitches	ULong	-	-	Readable	Standard	-	Number of switches
nLEDs	ULong	-	-	Readable	Standard	-	Number of LEDs
memories_length	ULong	-	-	Readable	Standard	-	
memories	ULong	-	4	Readable	Standard	-	The memory regions that may be used by various other elements, which inidicates aliasing etc. The values describing each region are: Bit 31:28 - External bus/BAR connected to this memory (0 is none) Bit 27:14 - Offset in bus/BAR of this memory (4KB units) Bit 13:0 - Size of this memory (4KB units) units)
dna	ULongLong	-	-	Readable	Standard	-	DNA (unique chip serial number) of this platform
switches	ULong	-	-	Volatile	Standard	-	Current value of any switches in the platform
LEDS	ULong	-	-	Writable, Readable	Standard	-	Setting of LEDs in the platform, with readback
nSlots	ULong	-	-	Parameter	Standard	0	Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property.
slotNames	String	32	-	Parameter	Standard	""	A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property.
slotCardIsPresent	Bool	-	64	Volatile	Standard	-	An array of booleans, where each index contains an indication whether a card is physically present in the given index's slot. For a description of a given index's slot, see the corresponding comma-separated string contents in the slotName property. Note that only the first min(nSlots,64) of the 64 indices contain pertinent information.

Worker Properties

Property Type	Name	Data Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
SpecProperty	platform	String	31	-	Parameter	Standard	matchstiq_z1	Name of this platform
Property	useGP1	Bool	-	-	Parameter	Standard	false	
Property	axi_error	Bool	-	4	Volatile	Standard	-	
Property	sdpDropCount	UChar	-	-	Volatile	Standard	-	
Property	debug_state	ULongLong	-	4	Volatile	Standard	-	
Property	debug_state1	ULongLong	-	4	Volatile	Standard	-	
Property	debug_state2	ULongLong	-	4	Volatile	Standard	-	

Component Ports

No ports are implemented for the given component specification.

Worker Interfaces

Type	Name	Master	Count	Usage
metadata	-	true	-	Access to container metadata via the platform worker. All platform workers must provide this port.
timebase	-	true	-	Providing a timebase for the time service. All platform workers must provide this port.
cpmaster	-	true	-	This platform worker provides a control plane.
sdp	zynq	true	4	Scalable data plane.

Worker Devices

The following is a table which enumerates which device workers are allowed in platform configurations and in assembly containers. The parameter values specified restrict allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

Name	Property Name	Property Value	Worker Signal	Platform Signal
time_server	frequency	$100*10^6$		
lime_adc	USE_CLK_OUT_p USE_CLK_IN_p USE_CTL_CLK_p DRIVE_CLK_p	1 0 0 0	RX_CLK RX_CLK_IN	- -
lime_dac	USE_CLK_IN_p USE_CTL_CLK_p	1 0	TX_CLK_IN	lime_adc_rx_clk_out
lime_spi	CLK_FREQ_p	$100*10^6$	sclk	-
lime_rx			rxen	-
lime_tx			txen	-
gps_uart				
si5338	CLKIN_PRESENT_p CLKIN_FREQ_p	1 $30.72*10^6$		
matchstiq_z1_avr				
pca9534				
pca9535				
tmp100				
matchstiq_z1_i2c	CLK_FREQ_p	$100*10^6$	SCL	-

Signals

Note that this signal table does not include signals that may be provided by slots.

Name	Type	Differential	Width	Description
SI5338_CLK0A	Input	false	1	Differential clock input from Si5338 Clock Generator
SI5338_CLK0B	Input	false	1	Differential clock input from Si5338 Clock Generator
LIME_RX_CLK	Output	false	1	Single ended clock output to Lime RX_CLK pin
clocktest	Output	false	1	Copy of LIME_RX_CLK. Pin 3 of rear debug connector
GPS_1PPS_IN	Input	false	1	1 PPS output from GPS module
GPS_FIX_IND	Input	false	1	Fix indication output from GPS module
EXT_1PPS_OUT	Output	false	1	1 PPS output from FPGA
ATLAS_LEDS	Output	false	3	LEDs on ATLAS module

Slots

No slots exist in this platform.

Platform Configurations

Name	Platform Configuration Workers	Card	Slot
base	matchstiq_z1	-	-
	time_server	-	-
matchstiq_z1_rx_tx	matchstiq_z1	-	-
	time_server	-	-
	si5338	-	-
	tmp100	-	-
	pca9535	-	-
	matchstiq_z1_avr	-	-
	lime_rx	-	-
	lime_tx	-	-
	lime_adc	-	-
	lime_dac	-	-
	gps_uart	-	-
matchstiq_z1_tx	matchstiq_z1	-	-
	time_server	-	-
	si5338	-	-
	tmp100	-	-
	pca9535	-	-
	matchstiq_z1_avr	-	-
	lime_tx	-	-
	lime_dac	-	-
	gps_uart	-	-
matchstiq_z1_rx	matchstiq_z1	-	-
	time_server	-	-
	si5338	-	-
	tmp100	-	-
	matchstiq_z1_avr	-	-
	lime_rx	-	-
	lime_adc	-	-
	gps_uart	-	-

NOTE: Inclusion of the lime_spi device worker is inferred when the lime_tx or lime_rx device workers are included.

Control Timing and Signals

Control Domain

All control clocking in the Matchstiq-Z1 platform originates from the PS7 processing clock 1 (FCLK1), which is set to 100 MHz.

Sampling Domain

The sampling clock domain originates from the CLK0 output of a SI5338 clock generator, which is connected directly to the Zynq FPGA. The platform worker converts this clock from differential to single ended and outputs this converted clock to the Lime transceiver.

This clock returns as an input to the Zynq FPGA aligned with the ADC data. This clock is connected as an input signal to the lime_adc and lime_dac device workers. See the diagram below for more details.

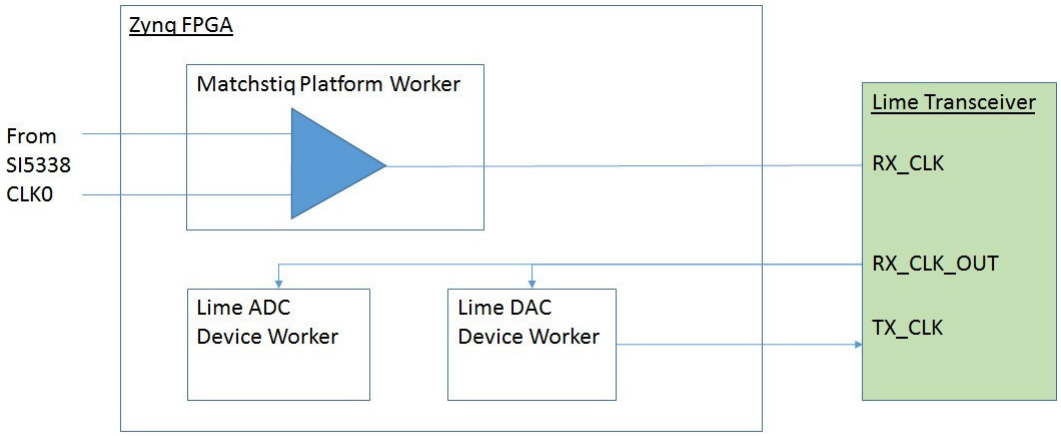


Figure 5: Clock Diagram showing default configuration

Note that the Lime DAC device worker can also be configured at build time to use an independent clock, the control clock or the sample clock (default).

Performance and Resource Utilization

Table 1: Resource Utilization Table for hdl-platform: matchstiq_z1

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
base	zynq	Vivado	2017.1	xc7z020clg484-1	2290	2701	N/A	BUFG: 1 BUFGCTRL: 1
matchstiq_z1_rx	zynq	Vivado	2017.1	xc7z020clg484-1	3179	3869	N/A	RAMB18E1: 2 RAMB36E1: 3 BUFG: 2 BUFGCTRL: 2
matchstiq_z1_rx_tx	zynq	Vivado	2017.1	xc7z020clg484-1	3475	4209	N/A	RAMB18E1: 3 RAMB36E1: 3 BUFG: 3 BUFGCTRL: 3
matchstiq_z1_tx	zynq	Vivado	2017.1	xc7z020clg484-1	3105	3940	N/A	RAMB18E1: 3 BUFG: 2 BUFGCTRL: 2

Test and Verification

To be detailed in a future release.

Example Design

This example design provides the infrastructure necessary to stream samples to/from the DAC/ADC interfaces to file.

To build the example design, enter the example_design directory and type 'make'.

To run the example design, NFS mount the example_design directory on the Matchstiq-Z1 and run the executable in the xilinx13_3 directory.