Summary - Zero Padding

This worker will be deprecated in OpenCPI 2.0. Use the Zero Pad component for new designs.

Name	zero_padding
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets.util_comps
Workers	zero_padding.rcc zero_padding.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL), centos7, xilinx13_3

Functionality

The Zero Padding component functions to expand input bits into signed Qm.n output samples within the range of ± 1.0, while inserting a variable number of zeros between output samples.

Output data widths of 8/16/32/64 are supported resulting in (respectively) Q0.7, Q0.15, Q0.31, and Q0.63 output formats.

Worker Implementation Details

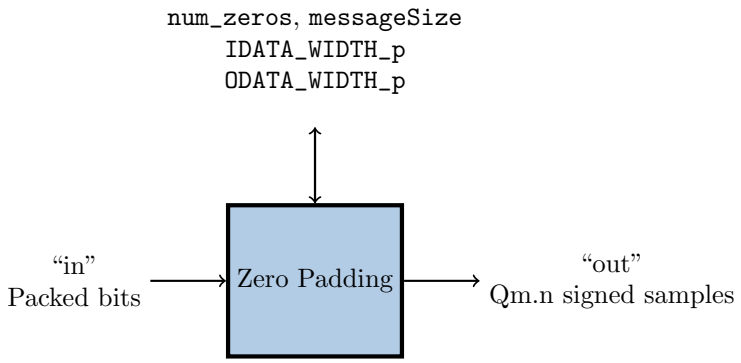
The Zero Padding component couples the underlying data, or protocol, with the size of the output data plane in order to fully load a Qm.n sample within the output bus width. In order to be maximally flexible, the component does not define input/output protocols explicitly. Since the input is simply bits, the input protocol is irrelevant and defined by the component feeding the Zero Padding, such as the File Reader. The input/output data widths are defined at build time, which in turn define the respective input/output sample sizes.

Theory

The Qm.n format defines the range to be -2^m to $2^m - 2^{-n}$, with a resolution of 2^{-n}. For the Zero Padding component, m is equal to zero, while n is defined at compile-time and is equal to the size of the output data width minus one. For example, an output data width of 16 results in Q0.15 format, where numbers are in the range of -1 to $+0.999969482421875$ (almost $+1$) with a bit resolution of 0.000030517578125.

Block Diagrams

Top level



State Machine

Two finite-state machines (FSMs) are implemented by this worker. One FSM implements worker functionality while the other supports Zero-Length Messages.

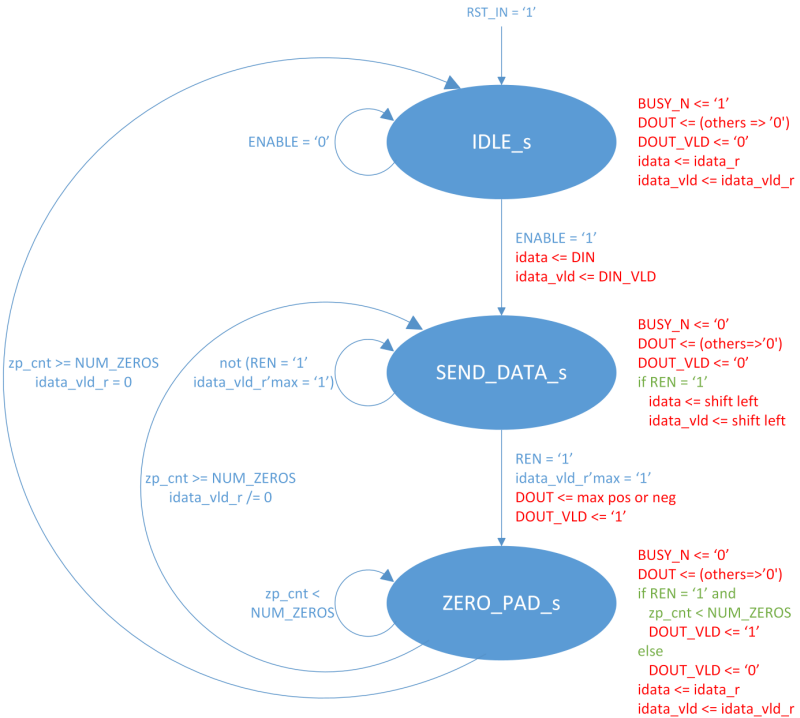


Figure 1: Zero Padding FSM

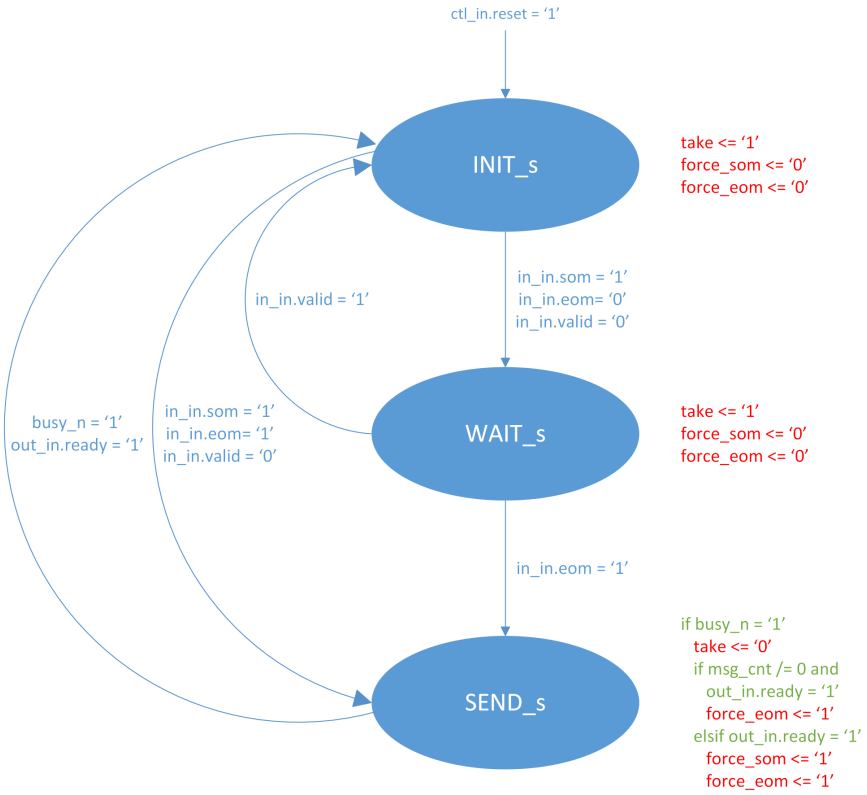


Figure 2: Zero-Length Message FSM

Source Dependencies

zero_padding.rcc

- projects/assets/components/util_comps/zero_padding.rcc/zero_padding.cc

zero_padding.hdl

- projects/assets/components/util_comps/zero_padding.hdl/zero_padding.vhd
- projects/assets/hdl/primitives/util_prims/util_prims_pkg.vhd
  projects/assets/hdl/primitives/util_prims/zp/src/zero_padding_gen.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
IDATA_WIDTH_p	ulong	-	-	Readable, Parameter	8/16/32/64	32	Input port data width
ODATA_WIDTH_p	ulong	-	-	Readable, Parameter	8/16/32/64	32	Output port data width
num_zeros	ushort	-	-	Readable, Writable	Standard	-	number of zeros to be inserted between output samples
messageSize	ushort	-	-	Readable, Writable	Standard	8192	number of bytes in output message

Worker Properties

zero_padding.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	MAX_NUM_ZEROS_p	ulong	-	-	Readable, Parameter	0-255	255	Maximum number of zeros

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	False	-	False	-	Packed bits
out	True	-	False	-	Qm.n signed samples representing 1.0

Worker Interfaces

zero_padding.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	IDATA_WIDTH_p	-	Size defined by IDATA_WIDTH_p
StreamInterface	out	ODATA_WIDTH_p	-	Sample size defined by ODATA_WIDTH_p

Control Timing and Signals

zero_padding.hdl

This worker implementation uses the clock from the Control Plane and standard Control Plane signals.

Performance and Resource Utilization

zero_padding.rcc

Table entries are a result of compiling the worker with the following parameter/property set:

- `IDATA_WIDTH_p`=16
- `ODATA_WIDTH_p`=16
- `num_zeros`=1

Processor Type	Processor Frequency	Run Function Time
linux-c6-x86_64 Intel(R) Xeon(R) CPU E5-1607	3.00 GHz	$\sim$ 5 ms
linux-c7-x86_64 Intel(R) Core(TM) i7-3630QM	2.40 GHz	$\sim$ 5 ms
linux-x13_3-arm ARMv7 Processor rev 0 (v7l)	666 MHz	$\sim$ 21 ms

Worker Configuration Parameters

zero_padding.hdl

Table 1: Table of Worker Configurations for worker: zero_padding

Configuratio	MAX_NUM_ZEROS_p	ODATA_WIDTH_p	ocpi_endian	IDATA_WIDTH_p	ocpi_debug
0	255	8	little	8	false
1	255	16	little	8	false
2	255	32	little	8	false
3	255	64	little	8	false
4	255	8	little	16	false
5	255	16	little	16	false
6	255	32	little	16	false
7	255	64	little	16	false
8	255	8	little	32	false
9	255	16	little	32	false
10	255	32	little	32	false
11	255	64	little	32	false
12	255	8	little	64	false
13	255	16	little	64	false
14	255	32	little	64	false
15	255	64	little	64	false

zero_padding.hdl

Table 2: Resource Utilization Table for worker "zero_padding"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	275	322	N/A	N/A
0	zynq	Vivado	2017.1	xc7z020clg484-1	272	329	N/A	N/A
0	zynq_ise	ISE	14.7	7z020clg484-1	267	448	197.2	N/A
0	virtex6	ISE	14.7	6vlx240tff1156-1	267	448	183.942	N/A
1	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	274	320	N/A	N/A
1	zynq	Vivado	2017.1	xc7z020clg484-1	271	320	N/A	N/A
1	zynq_ise	ISE	14.7	7z020clg484-1	266	443	197.668	N/A
1	virtex6	ISE	14.7	6vlx240tff1156-1	266	443	184.349	N/A
2	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	273	321	N/A	N/A
2	zynq	Vivado	2017.1	xc7z020clg484-1	270	317	N/A	N/A
2	zynq_ise	ISE	14.7	7z020clg484-1	263	439	198.373	N/A
2	virtex6	ISE	14.7	6vlx240tff1156-1	263	439	184.894	N/A
3	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	272	315	N/A	N/A
3	zynq	Vivado	2017.1	xc7z020clg484-1	269	295	N/A	N/A
3	zynq_ise	ISE	14.7	7z020clg484-1	261	439	216.92	N/A

3	virtex6	ISE	14.7	6vlx240tff1156-1	261	440	203.915	N/A
4	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	325	331	N/A	N/A
4	zynq	Vivado	2017.1	xc7z020clg484-1	322	366	N/A	N/A
4	zynq_ise	ISE	14.7	7z020clg484-1	317	493	197.2	N/A
4	virtex6	ISE	14.7	6vlx240tff1156-1	317	493	183.942	N/A
5	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	324	329	N/A	N/A
5	zynq	Vivado	2017.1	xc7z020clg484-1	321	358	N/A	N/A
5	zynq_ise	ISE	14.7	7z020clg484-1	316	488	197.668	N/A
5	virtex6	ISE	14.7	6vlx240tff1156-1	316	488	184.349	N/A
6	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	323	329	N/A	N/A
6	zynq	Vivado	2017.1	xc7z020clg484-1	320	354	N/A	N/A
6	zynq_ise	ISE	14.7	7z020clg484-1	313	483	198.373	N/A
6	virtex6	ISE	14.7	6vlx240tff1156-1	313	484	184.894	N/A
7	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	322	323	N/A	N/A
7	zynq	Vivado	2017.1	xc7z020clg484-1	319	332	N/A	N/A
7	zynq_ise	ISE	14.7	7z020clg484-1	311	511	216.92	N/A
7	virtex6	ISE	14.7	6vlx240tff1156-1	311	484	196.361	N/A
8	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	427	324	N/A	N/A
8	zynq	Vivado	2017.1	xc7z020clg484-1	424	438	N/A	N/A
8	zynq_ise	ISE	14.7	7z020clg484-1	419	588	190.636	N/A
8	virtex6	ISE	14.7	6vlx240tff1156-1	419	588	180.031	N/A
9	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	426	322	N/A	N/A
9	zynq	Vivado	2017.1	xc7z020clg484-1	423	426	N/A	N/A
9	zynq_ise	ISE	14.7	7z020clg484-1	418	577	190.636	N/A
9	virtex6	ISE	14.7	6vlx240tff1156-1	418	572	180.031	N/A
10	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	425	322	N/A	N/A
10	zynq	Vivado	2017.1	xc7z020clg484-1	422	424	N/A	N/A
10	zynq_ise	ISE	14.7	7z020clg484-1	415	568	190.636	N/A
10	virtex6	ISE	14.7	6vlx240tff1156-1	415	568	180.031	N/A
11	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	424	316	N/A	N/A
11	zynq	Vivado	2017.1	xc7z020clg484-1	421	403	N/A	N/A
11	zynq_ise	ISE	14.7	7z020clg484-1	413	556	193.028	N/A
11	virtex6	ISE	14.7	6vlx240tff1156-1	413	556	182.229	N/A
12	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	633	337	N/A	N/A
12	zynq	Vivado	2017.1	xc7z020clg484-1	630	582	N/A	N/A
12	zynq_ise	ISE	14.7	7z020clg484-1	625	766	197.707	N/A
12	virtex6	ISE	14.7	6vlx240tff1156-1	625	766	184.383	N/A
13	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	632	335	N/A	N/A
13	zynq	Vivado	2017.1	xc7z020clg484-1	629	578	N/A	N/A
13	zynq_ise	ISE	14.7	7z020clg484-1	624	755	198.098	N/A
13	virtex6	ISE	14.7	6vlx240tff1156-1	624	750	184.723	N/A
14	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	631	335	N/A	N/A
14	zynq	Vivado	2017.1	xc7z020clg484-1	628	570	N/A	N/A
14	zynq_ise	ISE	14.7	7z020clg484-1	621	745	198.373	N/A
14	virtex6	ISE	14.7	6vlx240tff1156-1	621	745	184.894	N/A
15	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	630	330	N/A	N/A
15	zynq	Vivado	2017.1	xc7z020clg484-1	627	549	N/A	N/A
15	zynq_ise	ISE	14.7	7z020clg484-1	619	733	200.04	N/A
15	virtex6	ISE	14.7	6vlx240tff1156-1	619	733	186.898	N/A

Test and Verification

Both input and output data widths of 8/16/32/64 are supported and fully tested on both RCC and HDL worker implementations. The sixteen cross products of these input/output data width combinations are built for both RCC and HDL workers. These input/output combinations are each tested with `num_zeros` equal to 0, 1, 128, and 255 resulting in 64 test cases for both RCC and HDL workers.

Input data is generated by a python script with an input parameter that defines the number of 32-bit words to produce. The input file consists of a repeating pattern of 0x0123456789ABCDEF. The number of 32-bit words for each test case is 2048, which results in 1024 64-bit samples, 2048 32-bit samples, 4096 16-bit samples, or 8192 8-bit samples. Thus for each test case the 64-bit test pattern is repeated 1024 times to produce a file of 65,536 bits (or 8192 bytes).

The Zero Padding component inputs each bit and expands the bit into Qm.n format within the range of ± 1.0, where $m = 0$, and n is defined by the width of the output data bus. Then `num_zeros` zeros are inserted between each output sample of width `ODATA_WIDTH_p`.

For verification, the output file is first checked that the data is not all zero, and is then checked for the expected length. Once these quick checks are made the output data is compared against expected results sample-by-sample without use of any gold files.