

Zipper Deprecation Notice:

Beginning with OpenCPI Version 1.5, support for Lime Microsystems' Zipper card is now deprecated.

Summary - alst4 Platform

| | |
|--------------|-----------------------|
| Name | alst4 |
| Worker Type | Platform |
| Version | v1.5 |
| Release Date | 4/2019 |
| Library | ocpi.assets.platforms |
| Workers | alst4.hdl |

Functionality

The alst4 platform worker provides an interface between a PCIe-connected processor and the Stratix IV FPGA on the Stratix IV Development board. It makes connections over a PCIe bus for OpenCPI control and data planes. It also provides a 200 MHz clock source for the timebase port and a 125 MHz clock source for the control plane.

Worker Implementation Details

The alst4 platform worker instantiates the pci_alst4 component from the stratix4 primitive library. The pci_alst4 component instantiates several components from the pcie_4243_hip_s4gx_gen2_x4_128 library, each of which represent Altera MegaCore-wizard generated IP cores. Figure 1 diagrams the intra-worker functionality of the alst4 platform worker, including the functionality of the aforementioned primitive libraries. Note that this diagram is not meant to be an exhaustive diagram of components or their interconnected signals, but a high-level overview of the functionality which includes the worker signals and port connections and how they interact with the instantiated primitives.

The pci_alst4 component instantiates version 12.1 of the PCI Express Hard IP Implementation with Avalon-ST Interface. This implementation is compatible with the PCI Express Card Electromechanical v2.0 specification. The 4-lane Gen2 Implementation is used and a 128-bit Avalon-ST interface is included. Detailed information on the Hard IP Implementation Endpoint with Avalon-ST Interface can be found in the Altera IP Compiler for PCI Express User Guide¹.

PCIe clocking and reset

The Implementation's PCIe clock source is the ref_clk signal whose intended frequency is 100 MHz. The pcie_rstn signal is a reset for the PCIe function itself. The reconfig_clk and fixedclk_serdes signals allow for transceiver offset cancellation². The fixedclk_serdes signal must be a 125MHz clock which is not generated from the refclk signal³. The local_rstn is the system-wide asynchronous reset which resets all IP Compiler for PCI Express circuitry not affected by the pcie_rstn signal. The npor signal is an asynchronous active-low power-on reset. The core_clk_out signal produces a clock signal which is fixed at 125 MHz for the given configuration (4 lane, Gen2 Hard IP)⁴. The rc_pll.locked signal indicates that the SERDES receiver PLL is in locked mode with the reference clock.

PCIe transceiver and Avalon interface

Data transmission and reception occurs over the PCIe physical bus via the pci_exp_rx and pci_exp_tx signal buses. The Avalon-ST data in/out is connected to the data plane via various input/output signals to/from the Implementation.

¹Recommended to start at Figure 4-3 (generic block diagram) and Figure 5-2 (signal I/O diagram)

²See Chapter 13 in the IP Compiler for PCI Express User Guide

³See page 13-9 in the IP Compiler for PCI Express User Guide

⁴See Table 7-1 in the IP Compiler for PCI Express User Guide

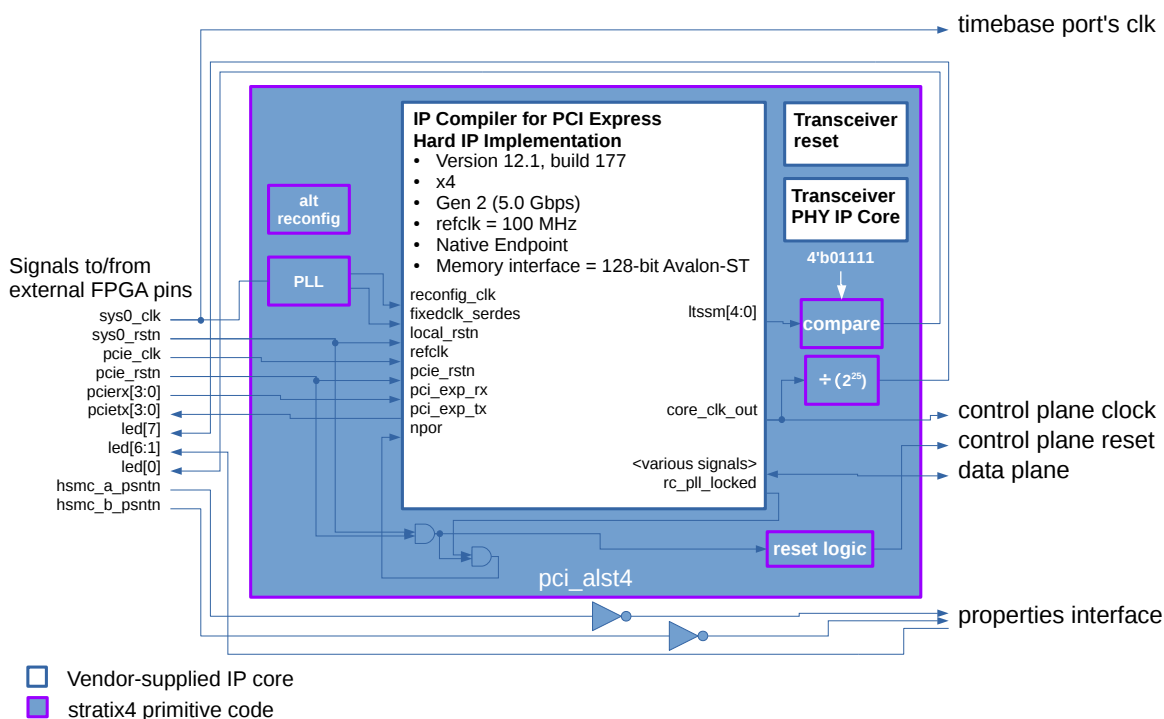


Figure 1: alst4 Functional Diagram

PCIe link status

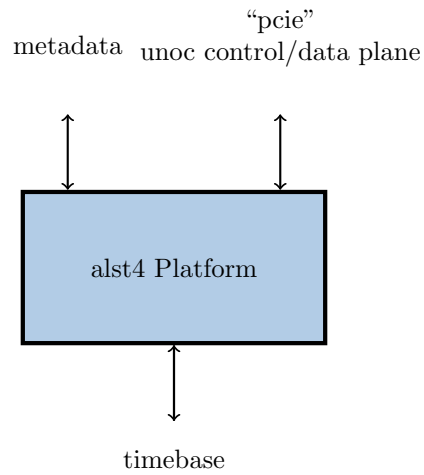
The ltssm signal bus indicates the Link Training and Status state machine (LTSSM) state, with 0'b01111 indicating L0.

Theory

Because there are no data processing algorithms implemented in this worker, no corresponding data processing theory is relevant herein.

Block Diagrams

Top level



State Machines

No state machines exist within the platform worker outside of those within the PCIe MegaCore function. It is not intended for users of MegaCore functions to understand their inner functionality.

Source Dependencies

- assets/hdl/platforms/alst4/alst4.vhd
- assets/hdl/primitives/stratix4/altpcie_reconfig_4sgx.v
- assets/hdl/primitives/stratix4/pci_alst4.v
- assets/hdl/primitives/stratix4/pcie_hip_s4gx_gen2_x4_128_rs_hip.v
- assets/hdl/primitives/stratix4/pcie_hip_s4gx_gen2_x4_128_wrapper.v
- assets/hdl/primitives/stratix4/pll1.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/altpcie_hip_pipen1b.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/altpcie_rs_serdes.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/pcie_hip_s4gx_gen2_x4_128_bb.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/pcie_hip_s4gx_gen2_x4_128_core.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/pcie_hip_s4gx_gen2_x4_128_serdes.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/pcie_hip_s4gx_gen2_x4_128.v
- assets/hdl/primitives/pcie_4243_hip_s4gx_gen2_x4_128/pciexp_dcram.v

Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|-------------------|-----------|----------------|-----------------|--------------------|-------------------------------|---------|---|
| platform | String | 31 | - | Parameter | Standard | - | Name of this platform |
| sdp_width | UChar | - | - | Parameter | Standard | 1 | Width of data plane in DWORDS (SDP is NOT implemented by the alst4) |
| UUID | ULong | - | 16 | Readable | Standard | - | UUID of this platform |
| oldtime | ULongLong | - | - | Padding | Standard | - | N/A |
| romAddr | UShort | - | - | Writable | Standard | - | |
| romData | ULong | - | - | Volatile | Standard | - | |
| nSwitches | ULong | - | - | Readable | Standard | - | Number of switches |
| nLEDs | ULong | - | - | Readable | Standard | - | Number of LEDs |
| memories_length | ULong | - | - | Readable | Standard | - | |
| memories | ULong | - | 4 | Readable | Standard | - | The memory regions that may be used by various other elements, which indicates aliasing etc. The values describing each region are: Bit 31:28 - External bus/BAR connected to this memory (0 is none) Bit 27:14 - Offset in bus/BAR of this memory (4KB units) Bit 13:0 - Size of this memory (4KB units) |
| dna | ULongLong | - | - | Readable | Standard | - | DNA (unique chip serial number) of this platform |
| switches | ULong | - | - | Volatile | Standard | - | Current value of any switches in the platform |
| LEDs | ULong | - | - | Writable, Readable | Standard | - | Setting of LEDs in the platform, with readback |
| nSlots | ULong | - | - | Parameter | Standard | 0 | Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property. |
| slotNames | String | 32 | - | Parameter | Standard | "" | A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property. |
| pci_device_id | Enum | - | - | Parameter | unknown, ml605, alst4, alst4x | unknown | PCI Device ID for PCI devices. This is essentially the "registry" of PCI device IDs. New platforms can use "unknown" before they are registered. |
| slotCardIsPresent | Bool | - | 64 | Volatile | Standard | - | An array of booleans, where each index contains an indication whether a card is physically present in the given index's slot. For a description of a given index's slot, see the corresponding comma-separated string contents in the slotName property. Note that only the first min(nSlots,64) of the 64 indices contain pertinent information. |

Worker Properties

| Property Type | Name | Data Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|---------------|---------------|-----------|----------------|-----------------|---------------|-------------------------------|---------------|--|
| SpecProperty | platform | String | 31 | - | Parameter | Standard | alst4 | Name of this platform |
| SpecProperty | nSlots | ULong | - | - | Parameter | Standard | 2 | Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property. |
| SpecProperty | slotNames | String | 32 | - | Parameter | Standard | hsmc_a,hsmc_b | A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property. |
| SpecProperty | pci_device_id | Enum | - | - | Parameter | unknown, ml605, alst4, alst4x | alst4 | PCI Device ID for PCI devices. This is essentially the “registry” of PCI device IDs. New platforms can use “unknown” before they are registered. |
| Property | pciId | UShort | - | - | Volatile | Standard | - | Contains PCIe configuration space register contents. See tlcfg_ctl in IP Compiler for PCI Express User Guide. |
| Property | unocDropCount | UChar | - | - | Volatile | Standard | - | Invalid packets collected at uNOC terminator |

Component Ports

No ports are implemented for the given component specification.

Worker Interfaces

| Type | Name | Master | Count | Usage |
|----------|------|--------|-------|--|
| metadata | - | true | - | Access to container metadata via the platform worker. All platform workers must provide this port. |
| timebase | - | true | - | Providing a timebase for the time service. All platform workers must provide this port. |
| unoc | pcie | true | - | This platform worker provides a control/data plane called “pcie”. |

Platform Devices

The following table enumerates the device workers that are included in the base platform configuration. The parameter values specified restrict allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

| Name | Property Name | Property Value | Worker Signal | Platform Signal |
|-------------|---------------|---------------------|---------------|-----------------|
| time_server | frequency | 200*10 ⁶ | | |

Signals

Note that this signal table does not include signals that may be provided by slots.

| Name | Type | Differential | Width | Description |
|--------------|--------|--------------|-------|---|
| sys0_clk | Input | false | 1 | 200 MHz clock which is sent to the timebase port as well as supplied to the PCI Express Megacore function for transceiver offset cancellation ⁵ . |
| sys0_rstn | Input | false | 1 | System-wide reset which resets all IP Compiler for PCI Express circuitry not affected by pcie_rstn. This is an asynchronous reset. |
| pcie_clk | Input | false | 1 | 100 MHz reference clock for the PCI Express IP core. |
| pcie_rstn | Input | false | 1 | Directly resets all sticky IP Compiler for PCI Express configuration registers. Sticky registers are those registers that fail to reset in L2 low power mode or upon a fundamental rest. This is an asynchronous reset. |
| pcie_rx | Input | false | 4 | PCIe RX. |
| pcie_tx | Output | false | 4 | PCIe TX. |
| led | Output | false | 16 | led[15:0] drive the LEDs labeled '15' through '0', respectively. led[6:1] are driven by the 6:1 indices of the LEDS property. led[7] is driven by the PCIE-generated control plane clock divided by 2 ²⁵ and led[0] is driven by the PCIE link up indicator. A low voltage on these signals illuminates their respective LEDs. |
| hsmc_a_psntn | Input | false | 1 | Connected to the PSNTn signal of the HSMC Port A slot. (Device workers may not ingest the HSMC Port A PSNTn signal). This active-low signal provides FMC LPC mezzanine card presence indication to index 0 of the slotCardIsPresent property. |
| hsmc_b_psntn | Input | false | 1 | Connected to the PSNTn signal of the HSMC Port B slot. (Device workers may not ingest the HSMC Port B PSNTn signal). This active-low signal provides FMC LPC mezzanine card presence indication to index 0 of the slotCardIsPresent property. |

⁵See Chapter 13 in the IP Compiler for PCI Express User Guide

Slots

The following table enumerates the available slots for this platform and the signals they include. Note that the signals listed are only those who are unconnected on the platform or whose platform signal name differ from the slot signal name.

| Name | Type | Slot Signal | Platform Signal |
|--------------|------------|-------------|-----------------|
| HSMC_ALST4.A | hsmc_alst4 | XCVR_TXp7 | - |
| | | XCVR_RXp7 | - |
| | | XCVR_TXn7 | - |
| | | XCVR_RXn7 | - |
| | | XCVR_TXp6 | - |
| | | XCVR_RXp6 | - |
| | | XCVR_TXn6 | - |
| | | XCVR_RXn6 | - |
| | | XCVR_TXp5 | - |
| | | XCVR_RXp5 | - |
| | | XCVR_TXn5 | - |
| | | XCVR_RXn5 | - |
| | | XCVR_TXp4 | - |
| | | XCVR_RXp4 | - |
| | | XCVR_TXn4 | - |
| | | XCVR_RXn4 | - |
| | | XCVR_TXp3 | - |
| | | XCVR_RXp3 | - |
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| | | XCVR_RXn2 | - |
| | | XCVR_TXp1 | - |
| | | XCVR_RXp1 | - |
| | | XCVR_TXn1 | - |
| | | XCVR_RXn1 | - |
| | | XCVR_TXp0 | - |
| | | XCVR_RXp0 | - |
| | | XCVR_TXn0 | - |
| | | XCVR_RXn0 | - |
| | | JTAG_TCK | - |
| | | JTAG_TMS | - |
| | | JTAG_TDO | - |
| | | JTAG_TDI | - |
| | | PSNTn | - |
| HSMC_ALST4.B | hsmc_alst4 | XCVR_TXp7 | - |
| | | XCVR_RXp7 | - |
| | | XCVR_TXn7 | - |
| | | XCVR_RXn7 | - |
| | | XCVR_TXp6 | - |
| | | XCVR_RXp6 | - |
| | | XCVR_TXn6 | - |
| | | XCVR_RXn6 | - |
| | | XCVR_TXp5 | - |
| | | XCVR_RXp5 | - |
| | | XCVR_TXn5 | - |
| | | XCVR_RXn5 | - |
| | | XCVR_TXp4 | - |

| | | |
|--|-----------|---|
| | XCVR_RXp4 | - |
| | XCVR_TXn4 | - |
| | XCVR_RXn4 | - |
| | XCVR_TXp3 | - |
| | XCVR_RXp3 | - |
| | XCVR_TXn3 | - |
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| | XCVR_TXp1 | - |
| | XCVR_RXp1 | - |
| | XCVR_TXn1 | - |
| | XCVR_RXn1 | - |
| | XCVR_TXp0 | - |
| | XCVR_RXp0 | - |
| | XCVR_TXn0 | - |
| | XCVR_RXn0 | - |
| | JTAG_TCK | - |
| | JTAG_TMS | - |
| | JTAG_TDO | - |
| | JTAG_TDI | - |
| | PSNTn | - |

Platform Configurations

Below is a sample set of supported platform configurations which highlight the device workers included in the platform configuration versus card/slots. For a complete list of supported platform configurations, refer to the alst4 directory.

| Name | Platform Configuration Workers | Card | Slot |
|--------------------------------------|--------------------------------|------------------------|--------------|
| base | alst4 | - | - |
| | time_server | - | - |
| alst4_zipper_hsmc_alst4_port_a_rx_tx | alst4 | - | - |
| | time_server | - | - |
| | lime_adc | lime_zipper_fmc_lpc | hsmc_alst4_a |
| | lime_dac | lime_zipper_fmc_lpc | hsmc_alst4_a |
| | si5351 | lime_zipper_fmc_lpc | hsmc_alst4_a |
| | lime_rx | lime_zipper_fmc_lpc | hsmc_alst4_a |
| | lime_tx | lime_zipper_fmc_lpc | hsmc_alst4_a |
| alst4_zipper_hsmc_alst4_port_a_rx | alst4 | - | - |
| | time_server | - | - |
| | lime_adc | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| | si5351 | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| alst4_zipper_hsmc_alst4_port_a_tx | lime_rx | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| | alst4 | - | - |
| | time_server | - | - |
| | lime_dac | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| alst4_zipper_hsmc_alst4_port_b_rx_tx | si5351 | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| | lime_tx | lime_zipper_hsmc_alst4 | hsmc_alst4_a |
| | alst4 | - | - |
| | time_server | - | - |
| alst4_zipper_hsmc_alst4_port_b_rx | lime_adc | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | lime_dac | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | si5351 | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | lime_rx | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | lime_tx | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | alst4 | - | - |
| | time_server | - | - |
| alst4_zipper_hsmc_alst4_port_b_tx | lime_adc | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | si5351 | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | lime_tx | lime_zipper_hsmc_alst4 | hsmc_alst4_b |
| | alst4 | - | - |

Control Timing and Signals

There are 3 clock domains present in the alst4 platform worker: 100 MHz, 125 MHz, and 200 MHz. The worker ingests an external-to-the FPGA 100 MHz clock. This clock serves as the clock source for the MegaCore function within the worker. The MegaCore function produces a clock via its `core.clk_out` pin which is 125 MHz for the x4 Gen2 Avalon-128 implementation⁶. This 125 MHz clock is subsequently supplied to the control plane as its clock. The worker also feeds a buffered version of the external-to-the-FPGA 200 MHz clock to the timebase port. The timebase port's PPS inputs and outputs are left unconnected.

⁶See Table 7-1 in the IP Compiler for PCI Express User Guide

Performance and Resource Utilization

Table 2: Resource Utilization Table for hdl-platform "alst4"

| Configuration | OCPI Target | Tool | Version | Device | Registers (Typ) | LUTs (Typ) | Fmax (MHz) (Typ) | Memory/Special Functions |
|--------------------------------------|-------------|---------|---------|-----------------|-----------------|------------|------------------|---|
| alst4_zipper_hsmc_alst4_port_a_rx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 4702 | 5955 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 170540 GXB Receiver PMA: 4 |
| alst4_zipper_hsmc_alst4_port_a_rx_tx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 5067 | 6417 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 172076 GXB Receiver PMA: 4 |
| alst4_zipper_hsmc_alst4_port_a_tx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 4736 | 6115 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 73772 GXB Receiver PMA: 4 |
| alst4_zipper_hsmc_alst4_port_b_rx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 4702 | 5955 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 170540 GXB Receiver PMA: 4 |
| alst4_zipper_hsmc_alst4_port_b_rx_tx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 5067 | 6417 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 172076 GXB Receiver PMA: 4 |
| alst4_zipper_hsmc_alst4_port_b_tx | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 4736 | 6115 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 73772 GXB Receiver PMA: 4 |
| base | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 4150 | 5160 | N/A | GXB Receiver PCS: 4 GXB Transmitter PCS: 4 GXB Transmitter PMA: 4 PLL: 1 Block Memory Bits: 72236 GXB Receiver PMA: 4 |

Test and Verification

To be detailed in a future release.

References

- 1) IP Compiler for PCI Express User Guide,
https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug_pci_express.pdf