Summary - Data Src

Name	data_src
Latest Version	v1.5 (release date $4/2019$)
Worker Type	Application
Component Library	ocpi.assets.misc_comps
Workers	data_src.hdl
Tested Platforms	zed, matchstiq_z1, e3xx, alst4, ml605, xsim

Functionality

Data Src selects one DATA_BIT_WIDTH_p bits-wide data bus from multiple data generation sources, packs the DATA_BIT_WIDTH_p bits in bit-forward order in the least significant bits of the I data bus and bit-reverse order in the most significant bits of the Q data bus, and outputs that I/Q bus to the out port. The DATA_BIT_WIDTH_p bits-wide data sources are:

- a unsigned counter,
- a walking ones bus (e.g. $b'100 \rightarrow b'010 \rightarrow b'001 \rightarrow b'100 \rightarrow etc$),
- a Linear Feedback Shift Register (LFSR),
- and a property-driven fixed value.

The bitwidth common to all data source buses is parameterized. In the case that the data source bus width is less than the iqstream I/Q widths of 16 bits, the bus is packed into the most significant bits of I and Q. This aids in data alignment when this component is connected directly to a DAC device worker, which commonly takes the DAC bitwidth-most significant bits of I and Q from an iqstream input port for its data transmission.

This component includes a property-driven setting which can optionally disable the output port once a specified

number of samples have been sent. This component can also be parameterized to send a Zero-Length Message (ZLM) once the output port is disabled.

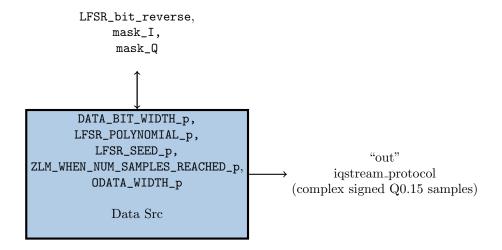
Worker Implementation Details

data_src.hdl

In keeping with good data flow control practices, backpressure from the output port will suspend the advancement of each data generation source. The ZLM_WHEN_NUM_SAMPLES_REACHED_p parameter, when having a value of true, forces the worker to send a single ZLM when the output port has been disabled (i.e. when the num_samples property has a value of more than 1 and num_samples amount of samples have been sent out the output port). This is useful for allowing applications which use this worker to terminate once this worker's output port is disabled.

Block Diagrams

$data_src.hdl$ - Top level



Source Dependencies

$data_src.hdl$

- $\bullet \ assets/components/misc_comps/data_src.hdl/data_src.vhd$
- $\bullet \ assets/components/misc_comps/data_src.hdl/out_port_inject_zlm.vhd\\$
- $\bullet \ assets/components/misc_comps/data_src.hdl/set_clr.vhd \\$
- $\bullet \ assets/primitives/misc_prims/lfsr/src/lfsr.vhd \\$

Component Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
DATA_BIT_WIDTH_p	ushort	-	-		Standard	16	Determines the width of the buses for each
							of the I and Q data generation memory ele-
							ments - if less than 16, the most significant
							DATA_BIT_WIDTH_p bits of I and Q on the
							out port will be filled. Value is expect to be less than or equal to 16.
LFSR_POLYNOMIAL_p	bool				Standard	0	E.g., a value of 1,1,0,1 would correspond to an
LFSR_FOLTNOMIAL_p	0001	-	_		Standard	0	LFSR polynomial of $x^4 + x^3 + (0^*x^2) +$
							\hat{x} 1 + 1 (+1 is always implied regardless of
							value).
LFSR_SEED_p	bool	-	-		Standard	0	Out-of-reset value of the Linear Feedback Shift
							Register (only affects output data in LFSR
							mode). This value should never be all zeros,
							which would cause the register to always have
							a value of all zeros regardless of polynomial
ZI M WILLIA MUM CAMPI EC DE ACHED	1 1				C 1 1	C 1	value.
ZLM_WHEN_NUM_SAMPLES_REACHED_p	bool	-	-		Standard	false	When value is true and num_samples property value is not -1, worker will generate Zero-
							Length-Message after num_samples amount of
							samples have been sent out the output port.
							Note this functionality is independent of the
							value of the enable property.
messageSize_bytes	ulong	-	-	Readable, Ini-	Standard	0	Message size in bytes. When the value of
				tial			(num_samples * num bytes per sample) is
							less than this property's value, the value of
							(num_samples * num bytes per sample) is used as the message size.
num_samples	long	_	_	Readable,	Standard	-1	Maximum number of samples which will be
num_samples	long	_		Writable	Standard	-1	sent out of the output port once out of re-
				***************************************			set. Note that samples are only sent when the
							enable property has a value of true. When the
							value of this property is -1, samples will be
							sent indefinitely (obeying backpressure from
	, ,						the connected worker, of course).
fixed_value	bool	-	-	Readable,	Standard	0x5a5a	The value of this property will be used for I
				Writable			(and the bit-reversed version of this value will be used for Q) to send to the output port when
							the mode property's value is 'fixed'. Array in-
							dex 0 corresponds to the 15th (most signifi-
							cant) I bit and the 16-DATA_BIT_WIDTH_p
							Q bit of the out port, array index 1 corre-
							sponds to the 14th (next-to-most significant)
							I bit and the 15-DATA_BIT_WIDTH_p Q bit
1.				D 1.1.1.			of the out port, etc
mode	enum	-	-	Readable, Writable	count, walking, LFSR, fixed	count	Counter, walking ones, Linear Feedback Shift Register, or fixed value.
enable	bool	_	_	Readable,	Standard	true	When the worker is not in reset, this property
Chapte	5001			Writable	Junidard	or uc	must have a value of true for the data to be
							sent to the output. Note that this property
							has no effect on the ZLM operation (see
							ZLM_WHEN_NUM_SAMPLES_REACHED_p
							parameter property).
LFSR_bit_reverse	bool	-	-	Readable,	Standard	true	Used to determine the LFSR shift direc-
				Writable			tion. When true, the DATA_BIT_WIDTH_p- bits wide LFSR will be reversed for both I and
							bits wide LFSR will be reversed for both I and Q.
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mask_I	ushort	-	-	Readable,	Standard	0xffff	I data will be bitwise anded with this mask
				Writable			before being sent to out port.
mask_Q	ushort	-	-	Readable,	Standard	0xffff	Q data will be bitwise anded with this mask
				Writable			before being sent to out port.

Worker Properties

$data_src.hdl$

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
ODATA_WIDTH_p	ushort	-	-		Standard	32	-

Component Ports

Name	Producer	Protocol	Optional
out	true	iqstream_protocol	False

Worker Interfaces

$data_src.hdl$

Type	Name	DataWidth
StreamInterface	out	ODATA_WIDTH_p

Control Timing and Signals

$data_src.hdl$

The Data Src worker uses the clock from the Control Plane and standard Control Plane signals.

$Worker\ Configuration\ Parameters$

$data_src.hdl$

Table 6: Table of Worker Configurations for worker: data_src

Configuration	n DATA_BIT_WIDTH_p ODATA_WIDTH_p		DTH_p ODATA_WIDTH_p LFSR_SEED_p ZLM_WHEN_NUM_SAMPLES_REACH		LFSR_POLYNOMIAL_p
0	12	32	1111111111111	true	111000001000
1	12	32	1111111111111	false	111000001000

Performance and Resource Utilization

$data_src.hdl$

Table 7: Resource Utilization Table for worker "data_src"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	N/A	342	614	N/A	N/A
0	zynq	Vivado	2017.1	xc7z020clg400-3	339	482	N/A	N/A
0	zynq_ise	ISE	14.7	7z010clg400-3	322	610	211.211	N/A
0	virtex6	ISE	14.7	6vcx75tff484-2	322	610	168.108	N/A
1	stratix4	Quartus	17.1.0	N/A	319	543	N/A	N/A
1	zynq	Vivado	2017.1	xc7z020clg400-3	335	452	N/A	N/A
1	zynq_ise	ISE	14.7	7z010clg400-3	318	607	293.462	N/A
1	virtex6	ISE	14.7	6vcx75tff484-2	318	607	231.801	N/A

Test and Verification

For verification, multiple test are run with varying values for the num_samples property for each of the available data source modes. The output file is checked for expected length and data contents, with the data content check being specific to the given data source mode.