Summary - CIC Decimator

Name	cic_dec
Worker Type	Application
Version	v1.3
Release Date	February 2018
Component Library	ocpi.assets.dsp_comps
Workers	cic_dec.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The CIC decimator has `N` cascaded integrator stages with an input data rate of f_s, followed by a rate change by a factor `R`, followed by `N` cascaded comb stages with an output data rate of $\frac{f_s}{R}$. The differential delay, `M`, affects the slope of the transition region. Figure 1 diagrams the decimating CIC filter.

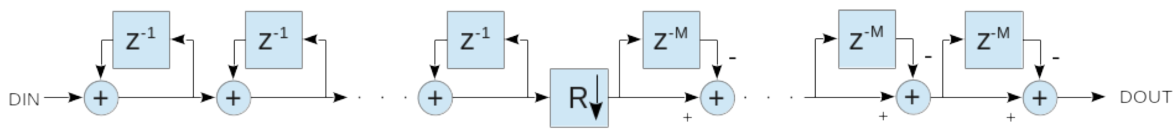

Figure 1: Cascaded Integration Comb Decimation filter Block Diagram

Worker Implementation Details

cic_dec.hdl

Number of Stages

The generic `N` sets the number of integrators and comb stages in the filter. Increasing the number of stages increases the attenuation in the sidelobes, as well as the bandwidth of the passband. The recommended range for this parameter is 3 to 6. Consult the reference material for an in depth discussion of the frequency response of the filter as a function of the generics in this module.

Bit Growth

For this design, the output data width for the comb stages is configurable via `ACC_WIDTH`. To adjust for bit growth in the data path and to ensure no quantization error at the output, this equation should be used to determine the value of `ACC_WIDTH`.

$$ACC\_WIDTH = N * CEIL(log_2(R * M)) + DIN\_WIDTH \tag{1}$$

Theory

A CIC filter is comprised of `N` integrator sections cascaded together with `N` comb sections. Combining the transfer functions for the two sections, we arrive at the system response function seen in Equation 1.

$$H(z) = [H_{int}(z)]^N [H_{comb}(z)]^N = \frac{1}{(1-z^{-1})^N}(1-z^{-R+M})^N = \frac{(1-z^{-R+M})^N}{(1-z^{-1})^N} \tag{2}$$

The magnitude response of the CIC filter is low pass with nulls at multiples of $f = \frac{1}{RM}$. The region surrounding the nulls is where aliasing occurs, so this aliasing effect must be considering when choosing `N`, `M`, and `R`.

Block Diagrams

Top level

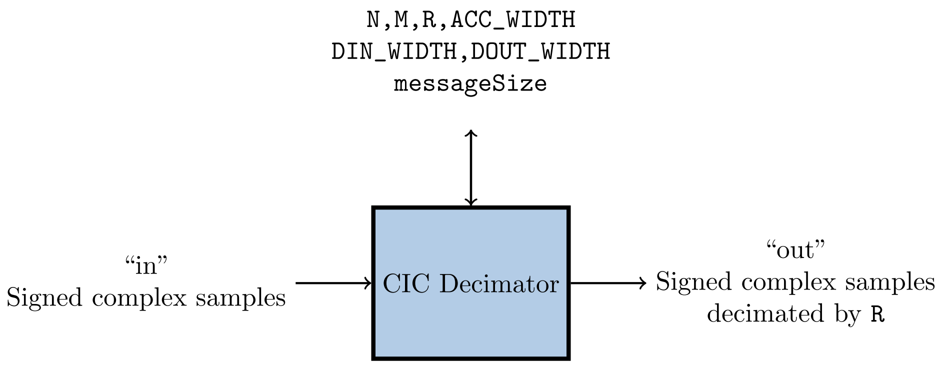

Figure 2: Top Level Block Diagram

State Machine

Only one finite-state machine (FSM) is implemented by this worker. The FSM supports Zero-Length Messages.

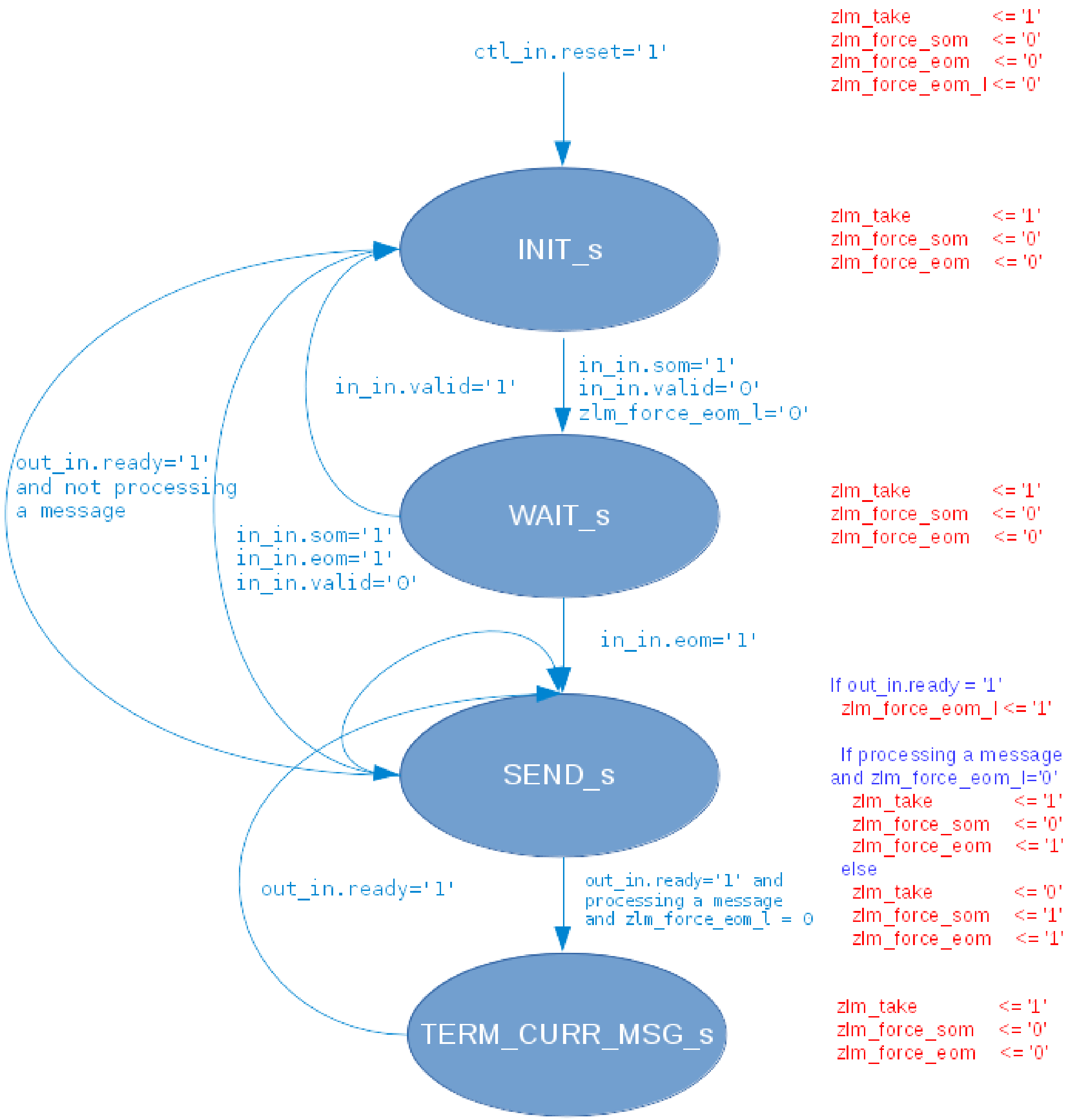

Figure 3: Zero-Length Message FSM

Source Dependencies

cic_dec.hdl

- ocpiassets/components/dsp_comps/cic_dec.hdl/cic_dec.vhd
- ocpiassets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  ocpiassets/hdl/primitives/dsp_prims/cic/src/cic_dec_gen.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
`N`	UChar	-	-	Readable	-	-	Number of Stages
`M`	UChar	-	-	Readable	-	-	Differential Delay
`R`	UShort	-	-	Readable	-	-	Decimation Factor
`ACC_WIDTH`	UChar	-	-	Readable	-	-	Accumulation Width *(2)
`DIN_WIDTH`	UChar	-	-	Readable	-	-	Input data width
`DOUT_WIDTH`	UChar	-	-	Readable	-	-	Output data width
`messageSize`	UShort	-	-	Readable, Writable	-	8192	Number of bytes in output message

Worker Properties

cic_dec.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
SpecProperty	`N`	-	-	-	Parameter	3-6	3	Number of Stages
SpecProperty	`M`	-	-	-	Parameter	1-2	1	Differential Delay
SpecProperty	`R`	-	-	-	Parameter	4-8192	4	Decimation Factor
SpecProperty	`DIN_WIDTH`	-	-	-	Parameter	16	16	Input Data Width
SpecProperty	`ACC_WIDTH`	-	-	-	Parameter	*	22	Accumulation Width *(2)
SpecProperty	`DOUT_WIDTH`	-	-	-	Parameter	16	16	Output Data Width

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	iqstream_protocol	false	-	Signed complex samples
out	true	iqstream_protocol	false	-	Signed complex samples

Worker Interfaces

cic_dec.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	ZeroLengthMessages=true	Signed complex samples
StreamInterface	out	32	ZeroLengthMessages=true	Signed complex samples

Control Timing and Signals

The CIC Decimation filter HDL worker uses the clock from the Control Plane and standard Control Plane signals.

This worker has a latency of N*2+1 valid input data clock cycles.

Latency
N*2+1

Performance and Resource Utilization

cic_dec.hdl

Worker Build Configuration "0":
Table entries are a result of building the worker with the following parameter sets:

- `DOUT_WIDTH=16`
- `DIN_WIDTH=16`
- `ACC_WIDTH=22`
- `M=1`
- `N=3`
- `ocpi_endian=little`
- `R=4`
- `ocpi_debug=false`

Table 1: Worker Build Configuration "0"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Function
stratix4	Quartus	15.1.0	EP4SGX230KF40C2	629	454	N/A	N/A
virtex6	ISE	14.7	6vlx240tff1156-1	628	550	346.081	N/A
zynq	Vivado	2017.1	xc7z020clg484-1	630	415	228.938	N/A
zynq_ise	ISE	14.7	7z020clg484-1	628	547	362.845	N/A

Test and Verification

Two test cases are implemented to validate the CIC Decimator component:

1. Unity gain response to DC: The CIC Decimator gain is calculated using the following equation:

$$CIC\ Gain = \frac{(R * M)^N}{2^{CEIL(N * log_2(R * M))}} \tag{3}$$

2. Tone waveform: A waveform containing tones at 50 Hz, 100 Hz and Fs/R sampled at 1024000 is processed by the worker. The tones at 50 Hz and 100 Hz are within the bandwidth of the filter, while the Fs/R tone is at the first null. The power levels of the input tones and output tones are measured and compared.

For the plots below, a CIC decimator with the following parameter set was used: `N`=3, `M`=1, `R`=2048, and `ACC_WIDTH`=49.

For Case #1, the plots below show the input with the I-leg zoomed in the show the amplitude is 32767, and output data with the I-leg zoomed to show an amplitude of 32767, which can be calculated using 3, shown below, and the Q-leg showing the worker delay before reaching it steady-state value.

$$OutputAmplitude = 32767 * \frac{(2048 * 1)^3}{2^{CEIL(3*log_2(2038*1))}} = 32767 * 1 = 32767 \tag{4}$$

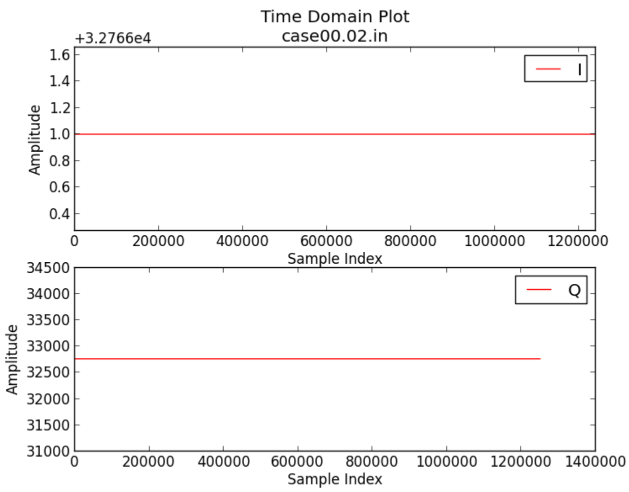

Figure 4: Time Domain: DC with amp=32767

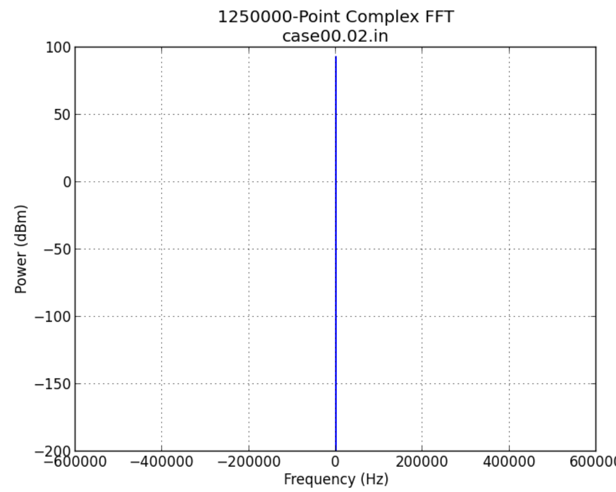

Figure 5: Frequency Domain: 0 Hz

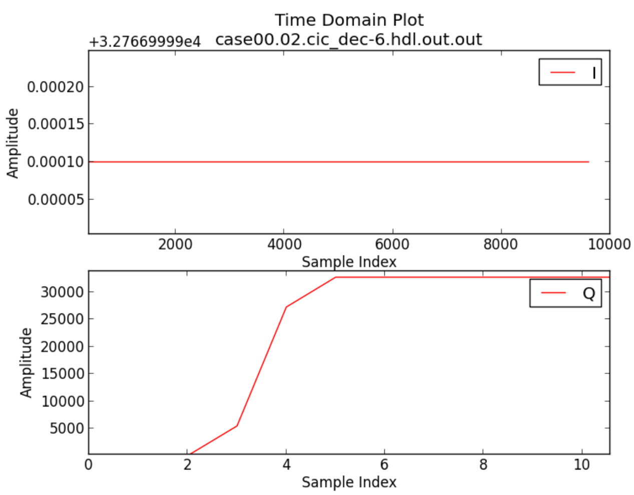

Figure 6: Time Domain: DC with amp=32767

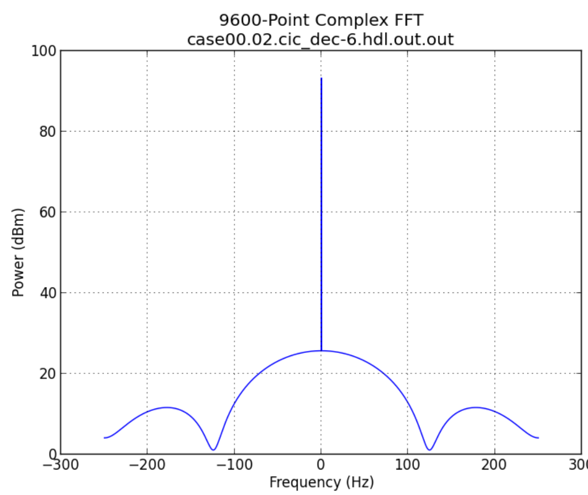

Figure 7: Frequency Domain: 0 Hz

For Case #2, the plots below show the input and output data (I-leg zoomed). The input plots show a complex waveform with frequency=50 Hz, 100 Hz, Fs/R Hz, where Fs=1024000 Hz and R=2048. The output FFT plot shows the Fs/R Hz has been filtered by the CIC decimator, but 50 Hz, 100 Hz were retained because they are within the bandwidth of the filter.

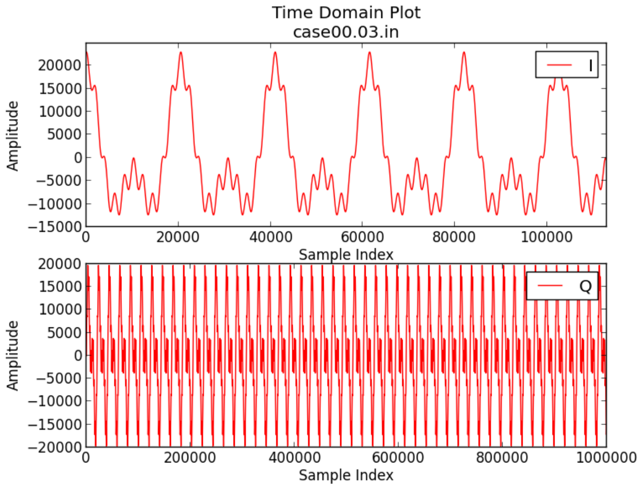

Figure 8: Time Domain

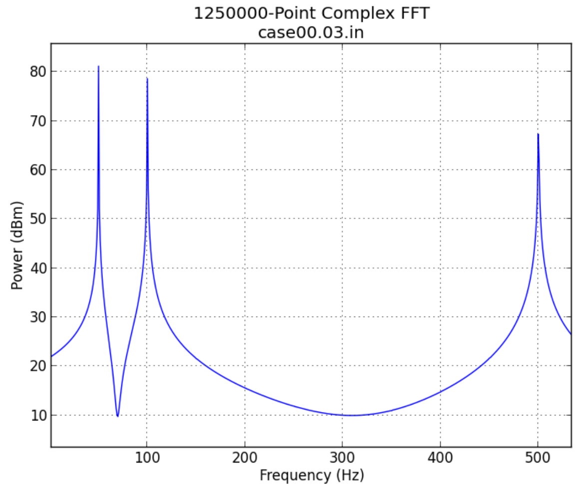

Figure 9: Frequency Domain: 50 Hz, 100 Hz, 1024000/2048 Hz

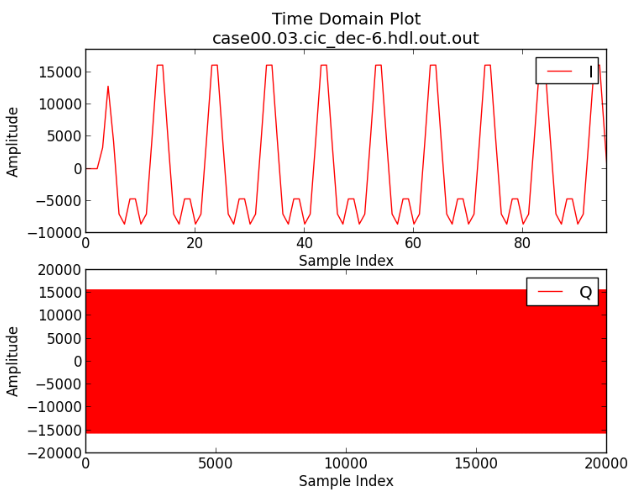

Figure 10: Time Domain

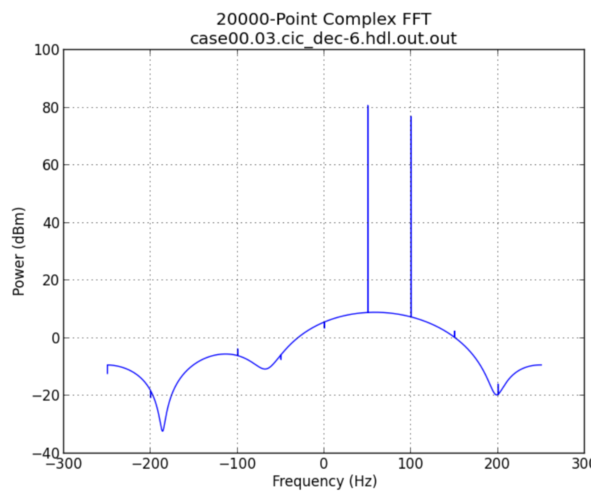

Figure 11: Frequency Domain: 50 Hz, 100 Hz

References

(1) Ronald E. Crochiere and Lawrence R. Rabiner. Multirate Digital Signal Processing. Prentice-Hall Signal Processing Series. Prentice Hall, Englewood Cli_s, 1983.
(2) Eugene B. Hogenauer, An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, April 1981.