# Summary - MFSK Mapper

| | |
|---|---|
| Name | mfsk_mapper |
| Worker Type | Application |
| Version | v1.3 |
| Release Date | February 2018 |
| Component Library | ocpi.assets.comms_comps |
| Workers | mfsk_mapper.hdl |
| Tested Platforms | xsim, isim, modelsim, Matchstiq-Z1(PL) |

# Functionality

The MFSK Mapper component translates bits or groups of bits to Q0.15 signed real FSK symbol values.

The number of FSK symbols is set with the `M_p` parameter, and the number of bits per FSK symbol is related by 1.

$$bits\_per\_symbol = log2(M\_p) \tag{1}$$

The MFSK Mapper component parses the bits on its input in bits per symbol sized pieces. The parsing begins on the MSB and ends on the LSB.

The possible FSK symbol values that can appear on the output of the component is set with the property `symbols`. `symbols` is an array property with Q0.15 values with size `M_p`. The FSK symbol value produced on the output will be the value of the symbols property at the index equal to value of the bits being parsed.

For example, if `M_p` was set to 4, the number of bits per symbol is equal to 2 and the symbols property is an array with 4 values indexed from 0 to `M_p`. If the bit sequence 00011011 appeared on the input, it would be interpreted as 4 symbols: 00,01,10,11. The output of the component would be equal to symbols[0], symbols[1], symbols[2], and symbols[3].

# Worker Implementation Details

## mfsk_mapper.hdl

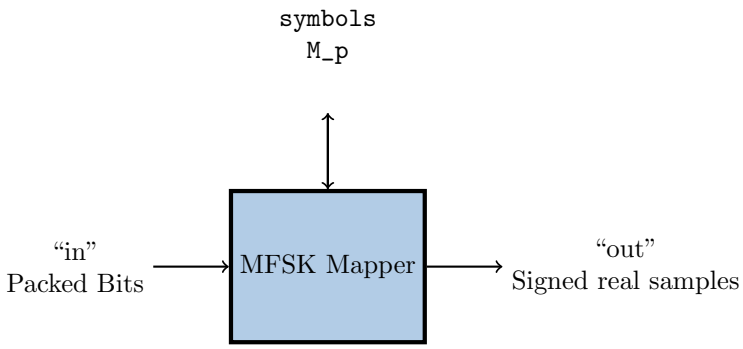
The message size for the output is equal to DIN_WIDTH_p divided by the number of bits per symbol multiplied by 2.

## mfsk_mapper.rcc

The message size for the output is equal to the input message size in bits divided by the number of bits per symbol multiplied by 2.

# Block Diagrams

## Top level




# Source Dependencies

## mfsk_mapper.hdl

- ocpiassets/components/comms_comps/mfsk_mapper.hdl/mfsk_mapper.vhd

# Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|---|---|---|---|---|---|---|---|
| M_p | UChar | - | - | Readable, Parameter | 2,4 | 2 | Number of FSK levels |
| symbols | Short | - | M_p | Readable, Writable | Standard | - | FSK symbol values |

# Worker Properties

## mfsk_mapper.hdl

| Type | Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|---|---|---|---|---|---|---|---|---|
| Property | DIN_WIDTH_p | Ulong | - | - | Readable, Parameter | 16 | 16 | Input port data width |

# Component Ports

| Name | Producer | Protocol | Optional | Advanced | Usage |
|---|---|---|---|---|---|
| in | false | - | false | - | Packed bits |
| out | true | rstream_protocol | false | ZeroLengthMessages=true | Q0.15 signed real samples |

# Worker Interfaces

## mfsk_mapper.hdl

| Type | Name | DataWidth | Advanced | Usage |
|---|---|---|---|---|
| StreamInterface | in | DIN_WIDTH_p | - | Packed bits |
| StreamInterface | out | 16 | - | Q0.15 signed real samples |

# Control Timing and Signals

The MFSK Mapper HDL worker uses the clock from the Control Plane and standard Control Plane signals.

# Performance and Resource Utilization

**mfsk_mapper.hdl**

**Worker Build Configuration "0":**
Table entries are a result of building the worker with the following parameter sets:

- `ocpi_endian=little`
- `ocpi_debug=false`
- `M_p=2`
- `DIN_WIDTH_p=16`

Table 1: Worker Build Configuration "0"

| OpenCPI Target | Tool | Version | Device | Registers | LUTs | Fmax (MHz) | Memory/Special Function |
|---|---|---|---|---|---|---|---|
| stratix4 | Quartus | 15.1.0 | EP4SGX230KF40C2 | 151 | 189 | N/A | N/A |
| virtex6 | ISE | 14.7 | 6vlx240tff1156-1 | 137 | 464 | 303.306 | N/A |
| zynq | Vivado | 2017.1 | xc7z020clg484-1 | 150 | 144 | 201.654 | N/A |
| zynq_ise | ISE | 14.7 | 7z020clg484-1 | 139 | 464 | 331.455 | N/A |

# Test and Verification

The input file consists of packed bits with a series of ramps from 0 to the number of FSK levels minus 1. The

The expected output waveform is a matching series of ramps of 16 bit values from 0 to the number of FSK levels minus 1. For verification, the values in the ramp are verified to match the input.