Summary - MATCHSTIQ_Z1_AVR

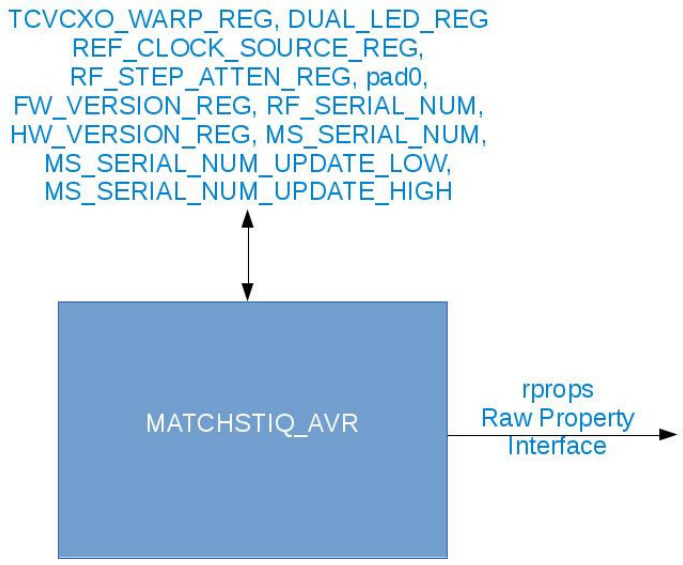
Name	matchstiq_z1_avr
Worker Type	Device
Version	v1.3
Release Date	February 2018
Component Library	ocpi.assets.platforms.matchstiq_z1.devices
Workers	matchstiq_z1_avr.hdl
Tested Platforms	Matchstiq-Z1(PL)

Worker Implementation Details

On the Matchstiq-Z1 platform, there is an AVR microcontroller which contains platform information and controls platform peripherals via registers accessible via I2C transactions. The MATCHSTIQ_Z1_AVR device worker uses the raw property interface to expose the features and hardware registers of the AVR microcontroller to the ANGRYVIPER framework.

Block Diagrams

Top level



Source Dependencies

matchstiq_z1_avr.hdl

- ocpiassets/hdl/devices/matchstiq_z1_avr.hdl/matchstiq_z1_avr.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
TCVCXO_WARP_REG	UShort	-	-	Writable	648-3413	2048	Register used for fine grained adjustments of the TCVCXO on Matchstiq-Z1 platform.
DUAL_LED_REG	UShort	-	-	Writable	0-3	1	Register used for controlling the LED on the front panel of the Matchstiq-Z1 platform. Bit 0 controls the green LED (0=off, 1=on) and bit 1 controls the red LED (0=off, 1=on).
REF_CLOCK_SOURCE_REG	UShort	-	-	Writable	-	-	
RF_STEP_ATTEN_REG	UShort	-	-	Writable	0-63	0	Register used to set the attenuation level of the programmable step attenuator in the RF receiver
pad0	UShort	-	12	Padding	-	-	Unused address space
FW_VERSION_REG	UShort	-	-	Padding	-	-	Firmware version register
RF_SERIAL_NUM	UShort	-	-	Padding	-	-	RF serial number register
HW_VERSION_REG	UShort	-	-	Padding	-	-	Hardware version register
MS_SERIAL_NUM	UShort	-	-	Volatile	-	-	Matchstiq serial number register
MS_SERIAL_NUM_UPDATE_LOW	UShort	-	-	Padding	-	-	
MS_SERIAL_NUM_UPDATE_HIGH	UShort	-	-	Padding	-	-	

Worker Interfaces

matchstiq_z1_avr.hdl

Type	Name	DataWidth	Advanced	Usage
RawProp	rprops	-	Master=true	Raw properties connection for slave I2C device worker
ControlInterface	-	-	Timeout=131072	Control clock cycles required to complete property read/write. I2C transactions require additional clock cycles to complete than the default of 16

Control Timing and Signals

The MATCHSTIQ_Z1_AVR HDL device worker uses the clock from the Control Plane and standard Control Plane signals.

Performance and Resource Utilization

matchstiq_z1_avr.hdl

Table 1: Worker Build Configuration "0"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Functions
zynq	Vivado	2017.1	xc7z020clg484-1	41	77	234.082	N/A

Test and Verification

There is no unit test for this device worker. The test and verification of this worker is covered in the Matchstiq I2C device worker. See the component datasheet of this worker for more details.