Limitations: Myriad-RF 1 and Zipper Daughtercard

The following is a list of the known limitations with ANGRYVIPER and the Myriad-RF 1 and Zipper Daughtercard:

1) The Zipper Carrier card is no longer being produced by the manufacturer. The card is Open Source so you are able to fabricate one yourself.
2) Sample Rate Limit on ML605, Stratix IV and ZedBoard Rev D
3) Clock initialization error with SI5351 proxy RCC component
4) Only VADJ supported on ZedBoard is 2.5 V

This document will describe the limitations and any workarounds.

Sample Rate Limitations

During testing of the ANGRYVIPER reference applications, data fidelity issues have been observed in the following scenarios:

Platform	Maximum Sample Rate
ML605	34 MS/s
Stratix IV	25 MS/s
ZedBoard Rev D	34 MS/s

Table 1: Sample rate limitations per platform

Note: ZedBoard Rev C does not show any such limitations. The Matchstiq-Z1 and Picoflexor T6A-S1 do not use use the Zipper daughtercard and therefore do not show any such limitations.

As of the 1.2 release of ANGRYVIPER, it is suspected that these upper sampling rate data fidelity problems are caused by phase incoherence due to the non-source-synchronous ADC/DAC clock source on the Zipper that are not being accounted for. This will be investigated during future release(s).

Clock Initialization Error with SI5351 Proxy RCC Component

When using ANGRYVIPER and the Myriad-RF 1 and Zipper Daughtercard, the SI5351 proxy component experiences the following intermittent errors:

```
Exception thrown: Code 0x17, level 0, error: 'Worker 'clock_gen' produced error during the 'stop'
control operation: SI5351 has not completed system initialization'
```

```
Exception thrown: Code 0x17, level 0, error: 'Worker 'clock_gen' produced error during the 'initialize'
control operation: SI5351 has not completed system initialization'
```

Per an application note of the SI5351[1], this error means that the IC is in 'System Initialization Mode'. It isn't recommended to read or write registers during this period, so the proxy correctly throws an exception. This mode is only supposed to be encountered during power up, but the error occurs intermittently during use of this platform.

There is no known workaround for this error. The error does not typically occur multiple times in a row, so re-running the application after an occurrence typically completes successfully.

Only VADJ supported on ZedBoard is 2.5 V

The ZedBoard platform and the Myriad-RF 1 and Zipper Daughtercard support three different Vadj voltages for the FMC LPC connector. During testing of the ANGRYVIPER reference applications, the only working configuration was 2.5 V. 3.3 V was not tested and 1.8 V showed data fidelity issues. It is recommended that 2.5 V be used.

References

[1] AN 619: Manually Generating an Si5351 Register Map
https://www.silabs.com/Support Documents/TechnicalDocs/AN619.pdf