Summary - Lime DAC(PRELIMINARY RELEASE)

Name	lime_dac
Worker Type	Device
Version	v1.3
Release Date	February 2018
Component Library	ocpi.assets.devices
Workers	lime_dac.hdl
Tested Platforms	

Functionality

The Lime DAC device worker converts the OpenCPI WSI interface into the Lime LMS6002Dr2 Transceiver DAC interface. The data enters the worker in the control clock domain and is converted to the sample clock domain (DAC_CLK).

Worker Implementation Details

lime_dac.hdl

The clock domain crossing (CDC) from the OpenCPI control clock to the sample clock is performed using a two-clocked synchronizing FIFO. The WSI interface can be seen in Figure 1. The incoming 32 bit data contains one complex sample, with the lower 16 bits containing I and the upper 16 bits containing Q. Before it is loaded into the CDC FIFO, the 32 bit sample is reduced to 24 bits by taking the top 11 bits and rounding the 12th bit for both I and Q. The FIFO has a data width of 24 bits and depth of 64. Data is loaded into the FIFO when the upstream worker is ready and unloaded using TX_IQ_SEL. In the event that a sample cannot be unloaded from the FIFO, the `underrun` property is set and remains set until it is cleared. The FIFO output signals are then translated into the DAC interface.

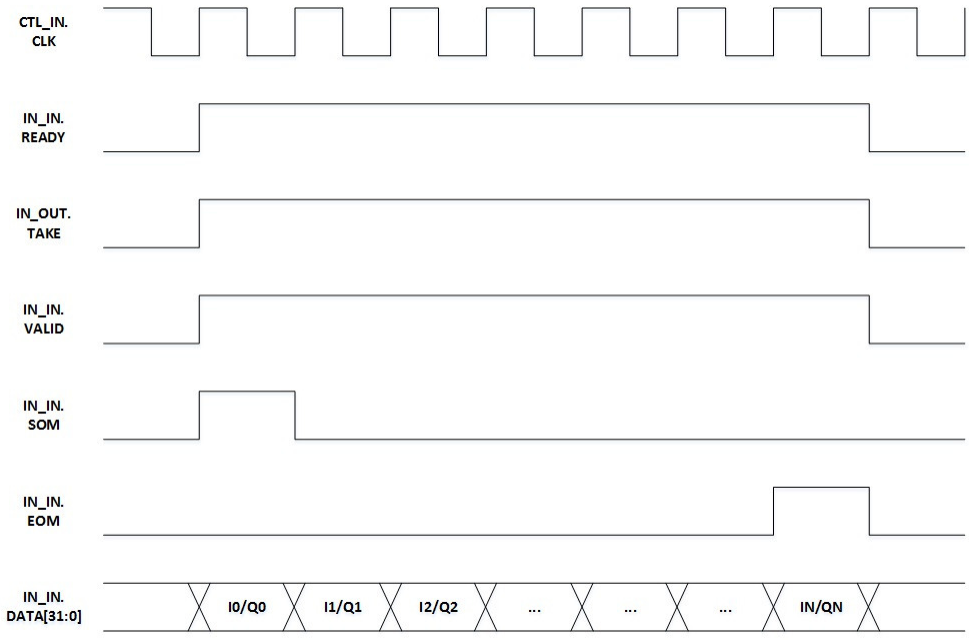


Figure 1: WSI Interface: Control Clock Domain

Figure 2 shows the Lime DAC Interface in the sample clock domain. There are 14 output signals in the interface: DAC_CLK(1), TX_IQ_SEL(1), and TXD(12). One data sample (I and Q) is clocked in every two DAC_CLK cycles

with TX_IQ_SEL serving as the qualifier for the I sample. The data width for the DAC is 12 bits and the data format is two's complement.

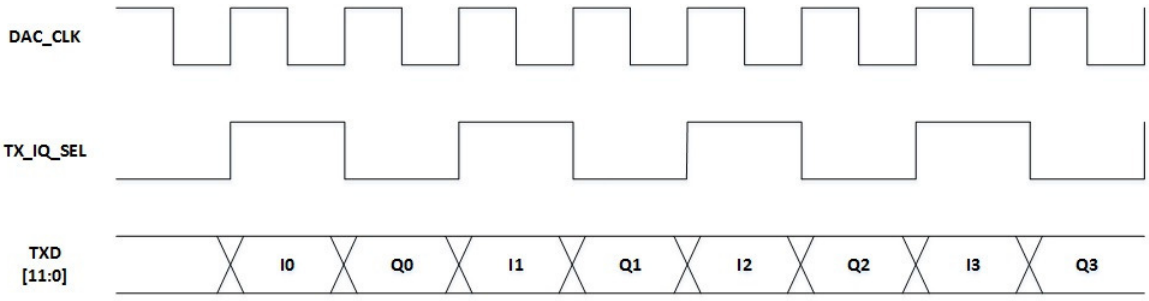


Figure 2: Lime DAC Interface: Sample Clock Domain

DAC_CLK can originate from one of two sources based on the value of the parameters. The table below describes the valid settings.

USE_CLK_IN_p	USE_CTL_CLK_p	DAC_CLK
True	X	TX_CLK_IN
False	True	ctl_in.clk

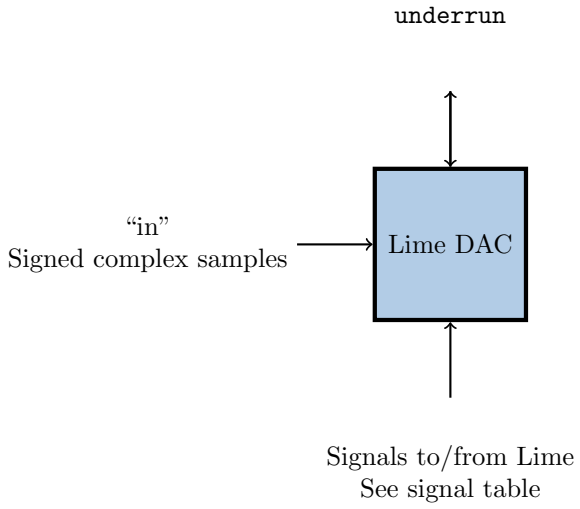
TX_CLK can be driven by this worker by setting the DRIVE_CLK_p parameter or it can be driven from another source external to the worker.

Theory

The main purpose of this worker is to perform a CDC for a data bus. The decision was made to implement the CDC using a two-clocked FIFO in an effort to target resources native the FPGA.

Block Diagrams

Top level



Source Dependencies

lime_dac.hdl

- ocpi.assets/hdl/devices/lime_dac.hdl/lime_dac.vhd
- ocpi.assets/hdl/devices/lime_adc.hdl/sync_status.vhd
  - Generates the *underrun* event when the DAC tries to unload a sample and the DAC FIFO is empty
- ocpi.core/hdl/primitives/util/dac_fifo.vhd
  - Performs the clock domain crossing between the control clock and sample clock domains

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
underrun	Bool	-	-	Writable, Volatile	Standard	-	This property is set when the DAC tries to unload a sample and the DAC FIFO is empty.

Worker Properties

lime_dac.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	other_present	Bool	-	-	Readable	-	-	Not implemented. Flag to indicated presence of ADC worker
Property	DRIVE_CLK_p	Bool	-	-	Parameter	Standard	1	Drive the clock sent to Lime (TX_CLK). Some platforms do not connect TX_CLK to the FPGA, making this parameter false
Property	USE_CLK_IN_p	Bool	-	-	Parameter	Standard	0	Use copy of clock sent to Lime (TX_CLK) as DAC_CLK.
Property	USE_CTL_CLK_p	Bool	-	-	Parameter	Standard	1	Use control clock as DAC_CLK. This is primarily for testing the component.
Property	divisor	-	-	-	Writable	-	-	Not implemented. Divider for DAC clock. This is primarily for testing the component.
SpecProperty	underrun	-	-	-	-	-	0	This property is set when the DAC tries to unload a sample and the DAC FIFO is empty.

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	iqstream_protocol	-	-	Signed complex samples

Worker Interfaces

lime_dac.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	Optional=true	Signed complex samples

Signals

Name	Type	Width	Description
TX_CLK	Output	1	Clock input to Lime
TX_IQ_SEL	Output	1	IQ Select to Lime
TXD	Output	12	Lime DAC data bus. IQ interleaved
TX_CLK_IN	Input	1	Copy of TX_CLK sent to FPGA

Control Timing and Signals

The Lime DAC device worker uses the clock from the Control Plane and Control Plane signals.

The latency through the worker from the input port to the DAC pins is 1 control clock cycle and 2 sample clock cycles. The data is loaded from the input port into the FIFO in one control clock cycle and unloaded to the DAC pins every other sample clock cycle (when TX_IQ_SEL is high).

Performance and Resource Utilization

lime_dac.hdl

Worker Build Configuration "0":
Table entries are a result of building the worker with the following parameter sets:

- `ocpi_endian=little`
- `ocpi_debug=false`
- `DRIVE_CLK_p=1`
- `USE_CTL_CLK_p=0`
- `USE_CLK_IN_p=1`

Table 1: Worker Build Configuration "0"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Functions
stratix4	Quartus	15.1.0	N/A	151	179	N/A	N/A
virtex6	ISE	14.7	6vcx75tff484-2	172	316	444.109	RAM64Ms=8
zynq	Vivado	2017.1	xc7z020clg400-3	152	135	309.215	N/A
zynq_ise	ISE	14.7	7z010clg400-3	172	314	547.555	RAM64Ms=8

Test and Verification

To be detailed in a future release.

References

1) LMS6002D Datasheet, www.limemicro.com