Configure Environment for ModelSim

Version 1.2

Revision History

Revision	Description of Change	Date
v1.0	Initial Release	2/2016
v1.1	Updated for OpenCPI 1.1	3/2017
v1.2	Updated for OpenCPI 1.2	8/2017

Table of Contents

1 Overview

This document describes how to compile Xilinx simulation libraries of a device(s) for a particular 3rd party simulator, such as ModelSim.

1. Compile Xilinx libraries for ModelSim
2. Modify `modelsim.ini` to include path of compiled Xilinx libraries

2 Compile Xilinx/Zynq simulation libraries for ModelSim

2.1 Compile Vivado's simulation libraries

This section provides the steps necessary to compile Xilinx Vivado's simulation libraries of the Zynq device, for ModelSim. If using Modelsim 10.4c, note that Vivado 2017.1 does not support compilation of simulation libraries for ModelSim versions earlier than 10.5c. Therefore, if using a ModelSim 10.4c, you will need to use an earlier version of Vivado (*e.g* 2015.4) to compile the simulation libraries. For this example, we use Vivado 2017.1 with Modelsim DE 10.6a.

1. Open a terminal window and switch the user to root:

   ```
   > sudo su -
   ```

2. Configure the terminal for Xilinx Vivado by sourcing the setup script (for bash):

   ```
   > source /opt/Xilinx/Vivado/<version>/settings64.sh
   ```

3. Launch Vivado:

   ```
   > vivado
   ```

4. Select Tools → Compile Simulation Libraries...

5. Select the following:

   Simulator: Modelsim Simulator

   Language: VHDL

   Library: All

   Family: Zynq-7000

   Compiled library location: `/opt/Xilinx/Vivado/<version>/vhdl/modelsim/<version>/lin64`

   Simulator executable path: `/opt/Modelsim/modelsim_dlx/linuxpe`

   Compile 32-bit libraries: Yes

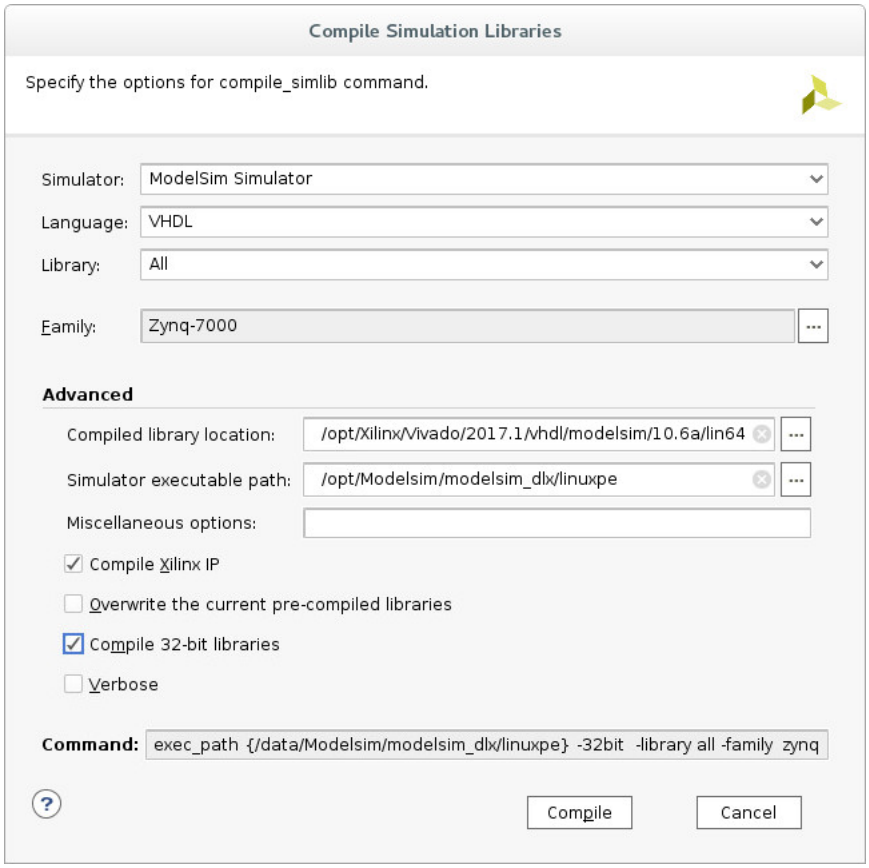

Figure 1: Vivado 2017.1 Compile Simulation Libraries

6. Click “Compile”
7. Note that 2017.1 Vivado will result in errors for Modelsim versions earlier than 10.5c. Here, we show the results for Vivado 2017.1 with Modelsim DE 10.6a, and Vivado 2015.4 with Modelsim DE 10.4c.

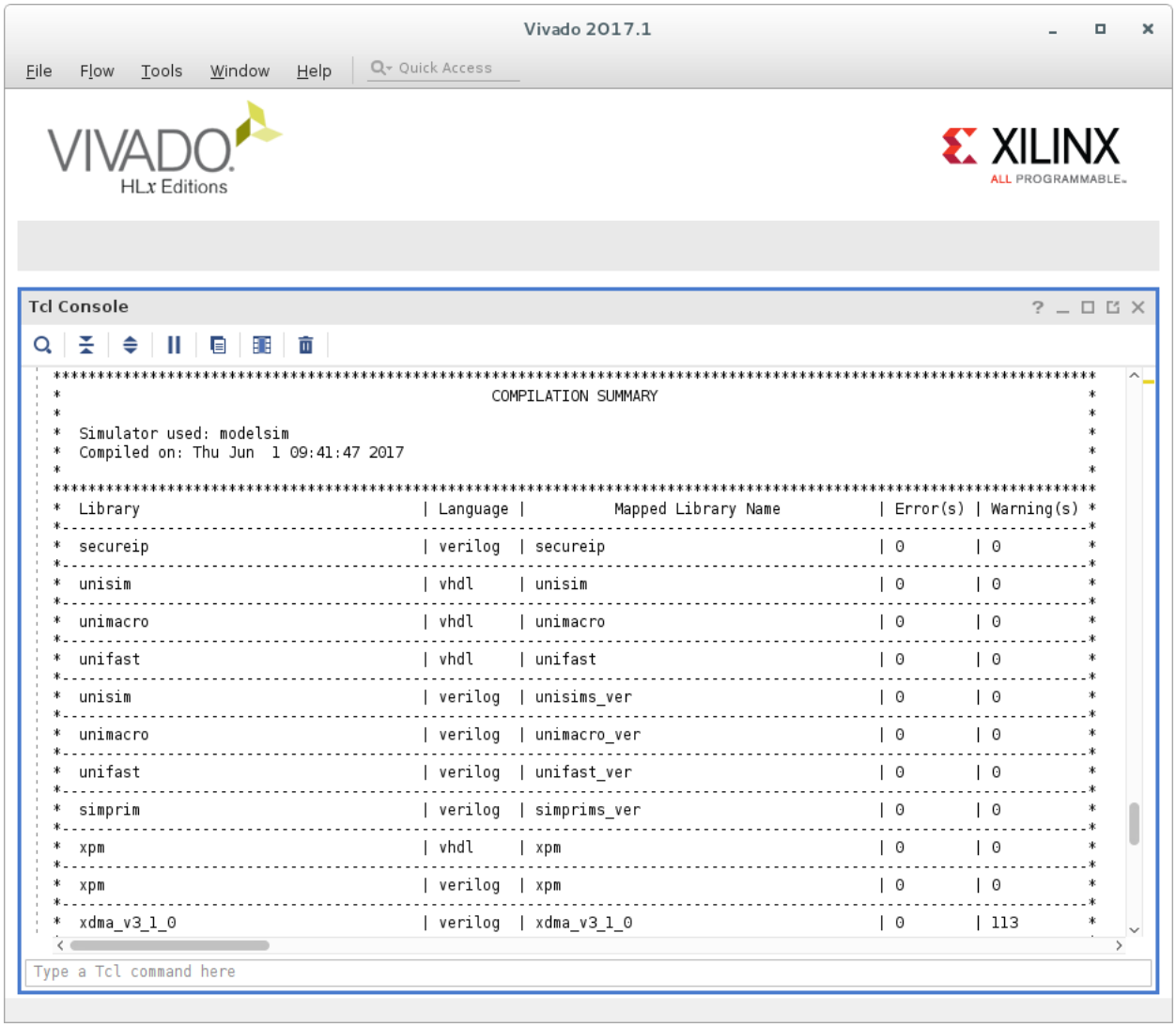

Figure 2: Vivado 2017.1 Compilation Output with Modelsim DE 10.6a

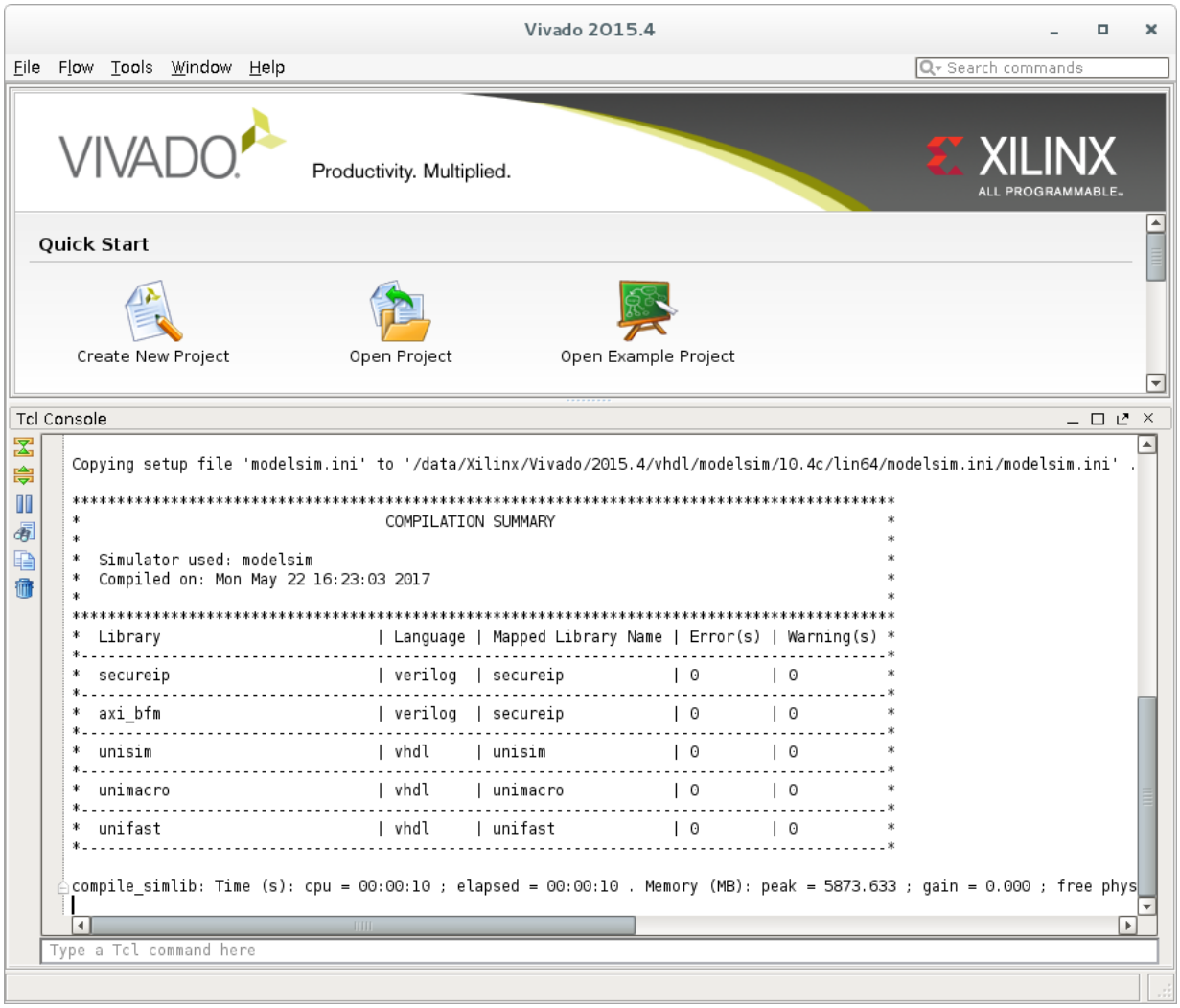

Figure 3: Vivado 2015.4 Compilation Output with Modelsim DE 10.4c

2.2 Compile ISE's simulation libraries

This section provides the steps necessary to compile Xilinx ISE's simulation libraries of the Zynq device, for ModelSim.

1. Open a terminal window and switch the user to root:

   ```
   > sudo su -
   ```

2. Configure the terminal window for Xilinx ISE by sourcing the setup script (for bash):

   ```
   > cd /opt/Xilinx/14.7/ISE_DS/
   > source settings64.sh
   ```

3. Launch the Xilinx CompXLib GUI:

   ```
   > cd /opt/Xilinx/14.7/ISE_DS/ISE/bin/lin64
   > ./compxlib
   ```

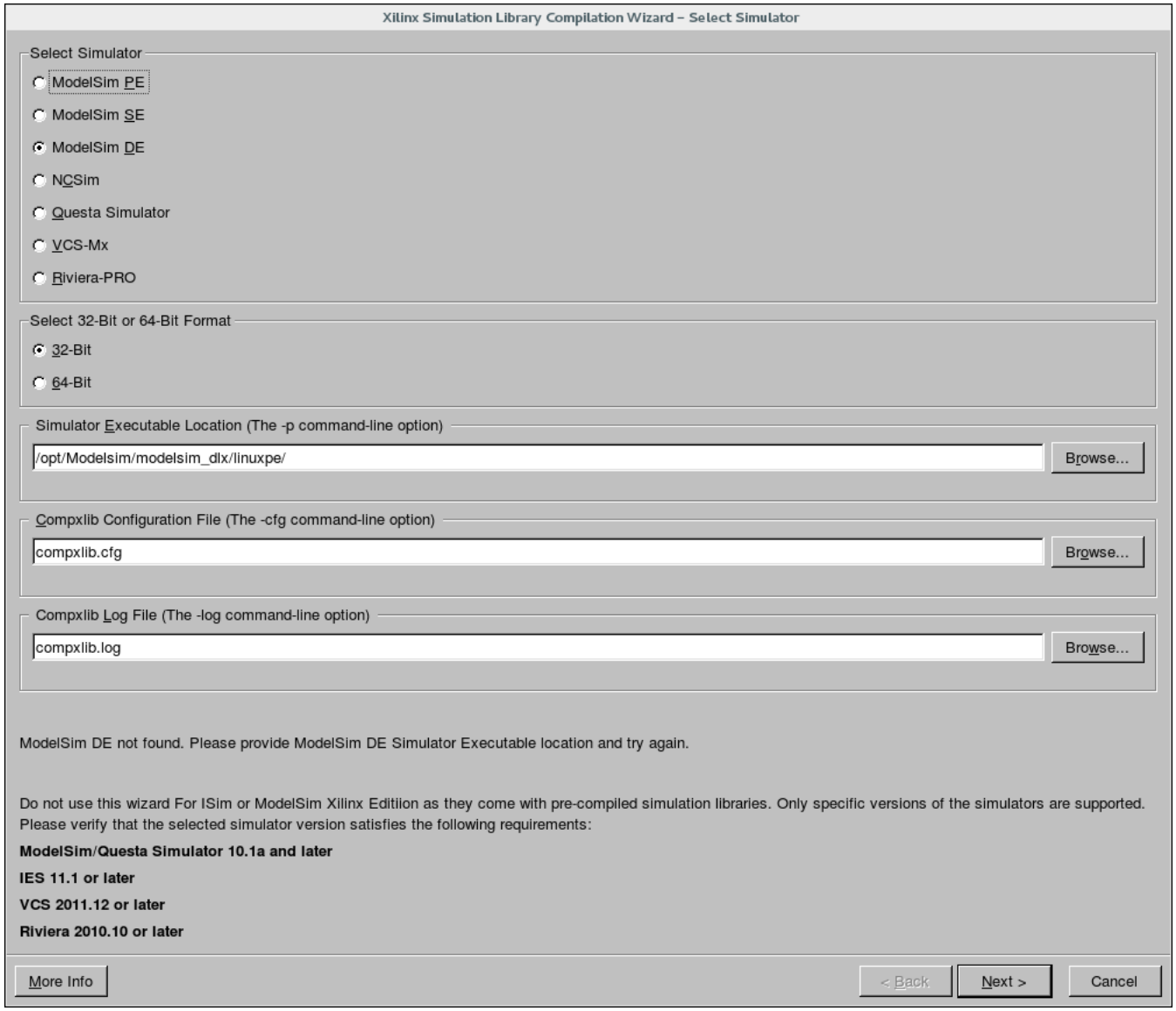

Figure 4: Compilation Wizard - Select Simulator

4. Select ModelSim DE.
5. Set Simulator Executable Location.
6. Click “Next”.

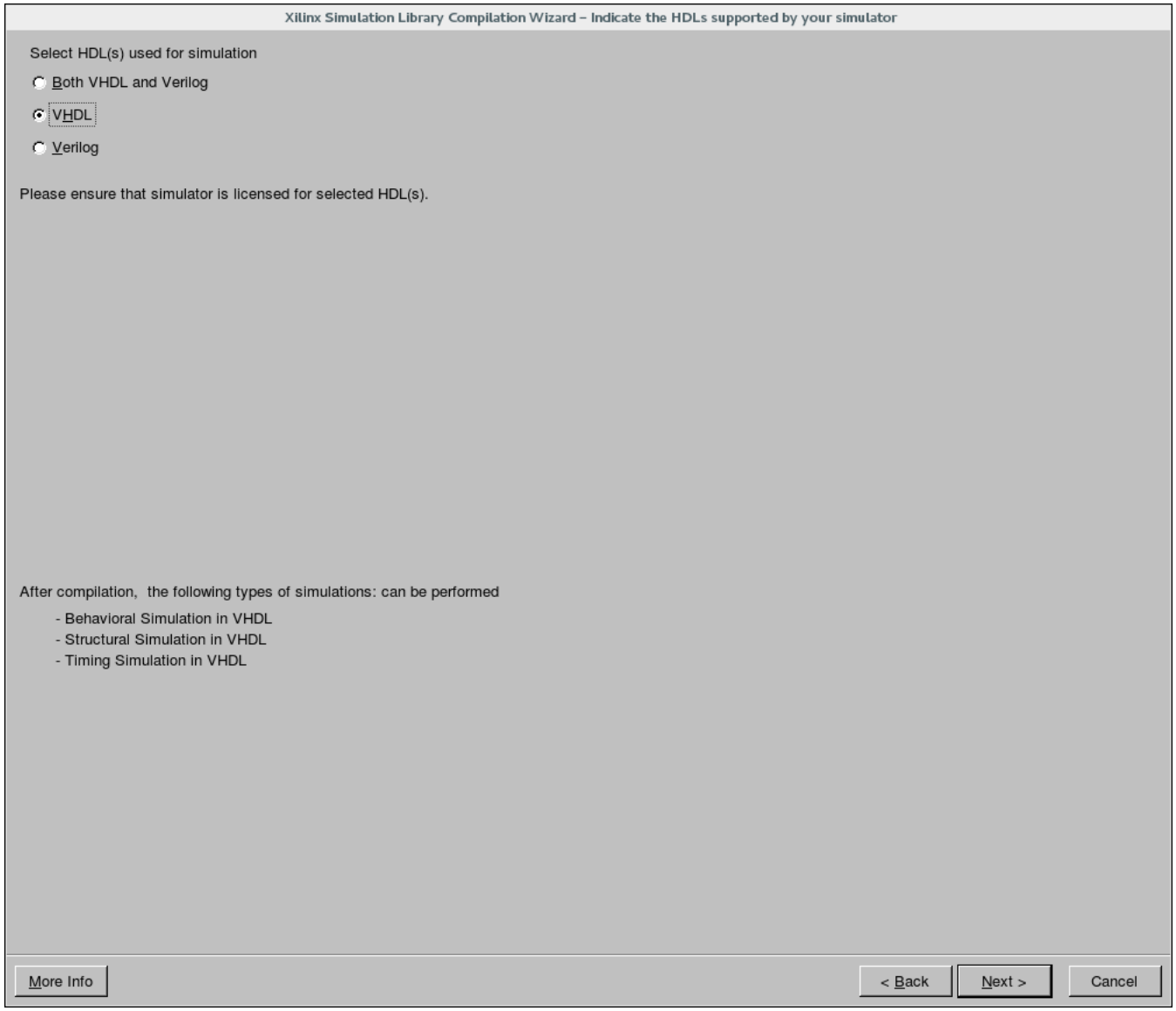

Figure 5: Compilation Wizard - HDLs to support simulator

7. Select “VHDL”.
8. Click “Next”.

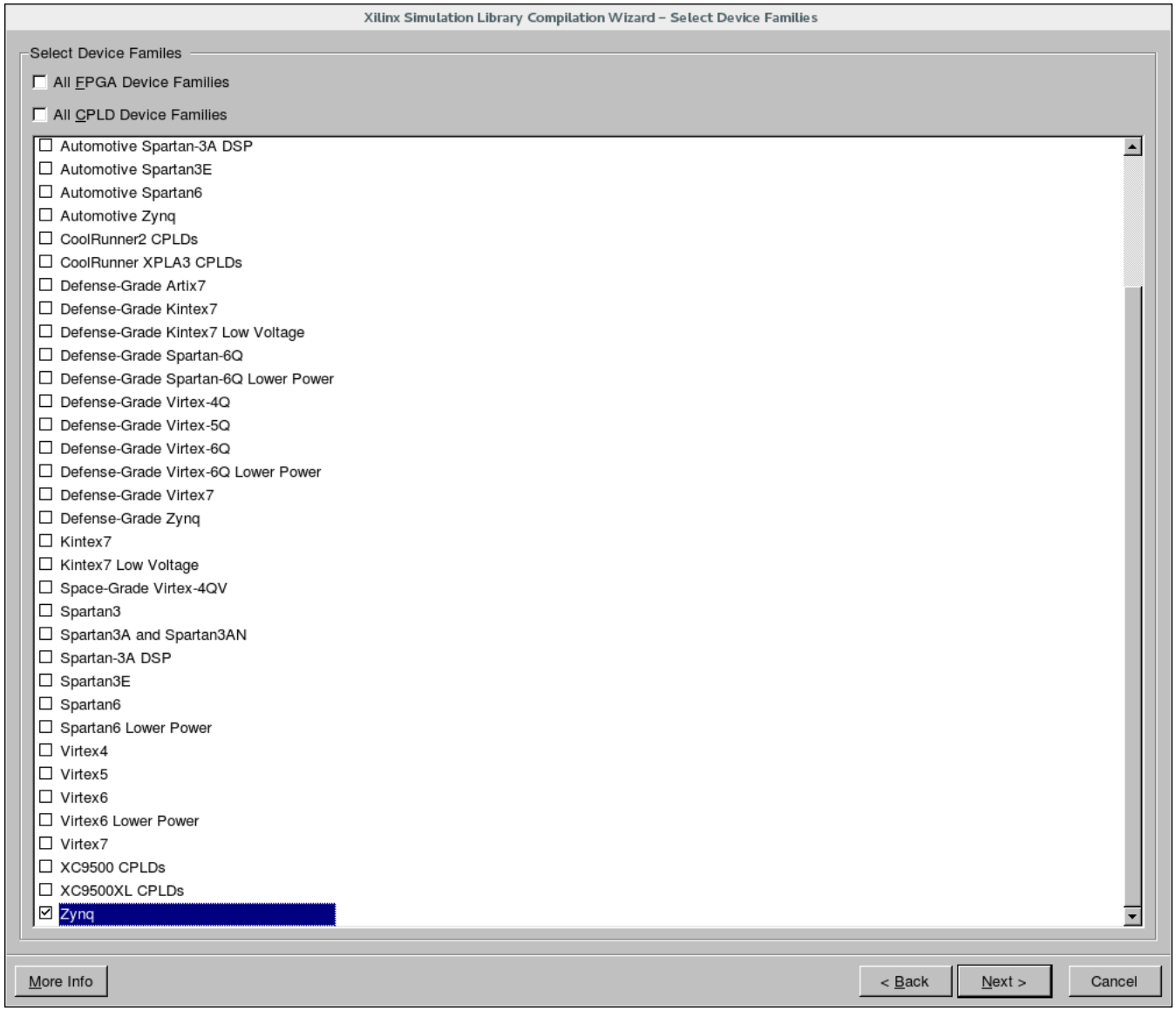

Figure 6: Compilation Wizard - Select Device Families

9. Uncheck “All FPGA Device Families”.
10. Uncheck “All CPLD Device Families”.
11. Check “Zynq”.
12. Click “Next”.

Figure 7: Compilation Wizard - Select Simulation Libraries

13. No change.
14. Click “Next”.

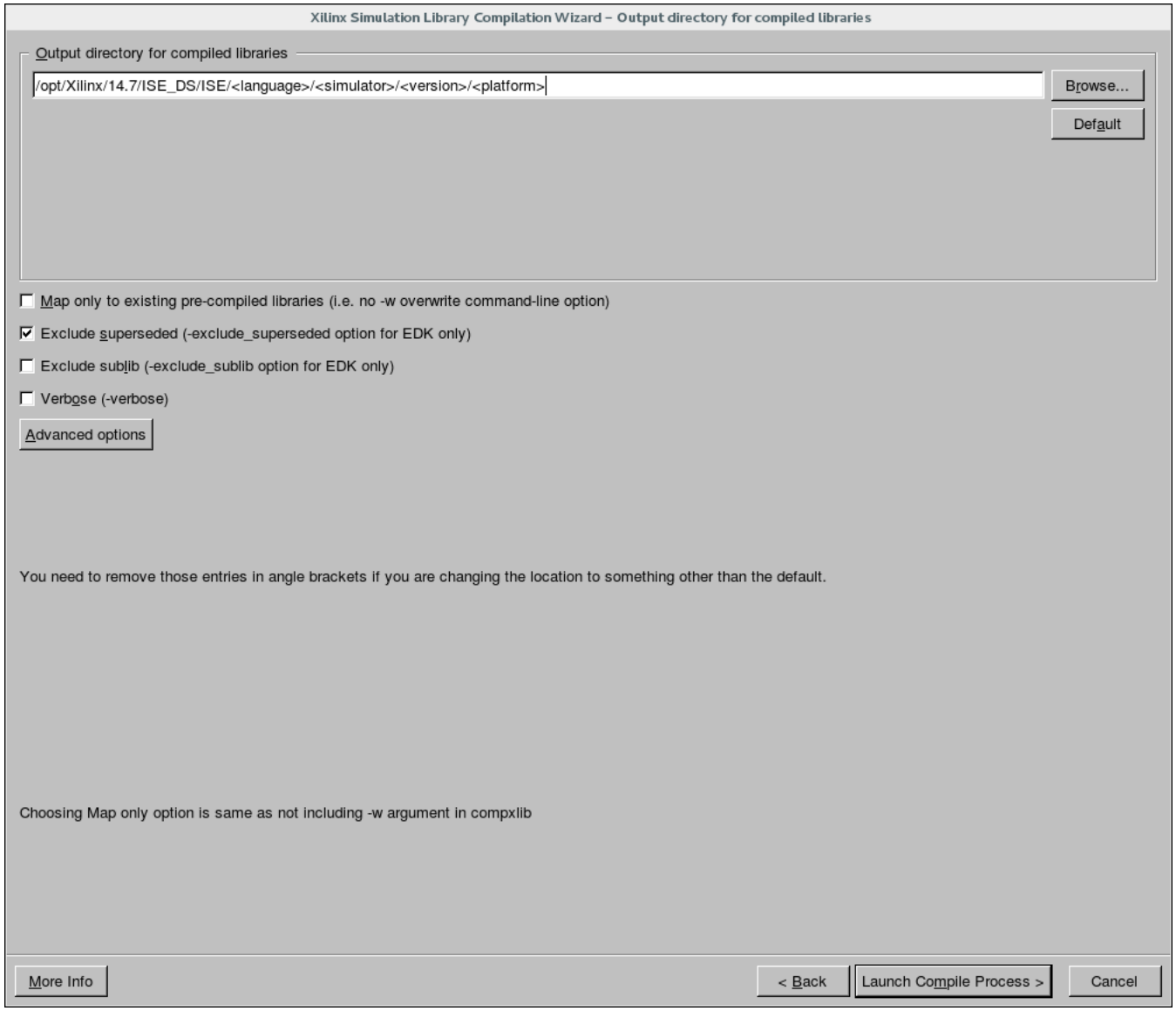

Figure 8: Compilation Wizard - Select Output directory

15. Select defaults.
16. Click “Launch Compile Process”.

    Note: This step will take approximately 20 mins.

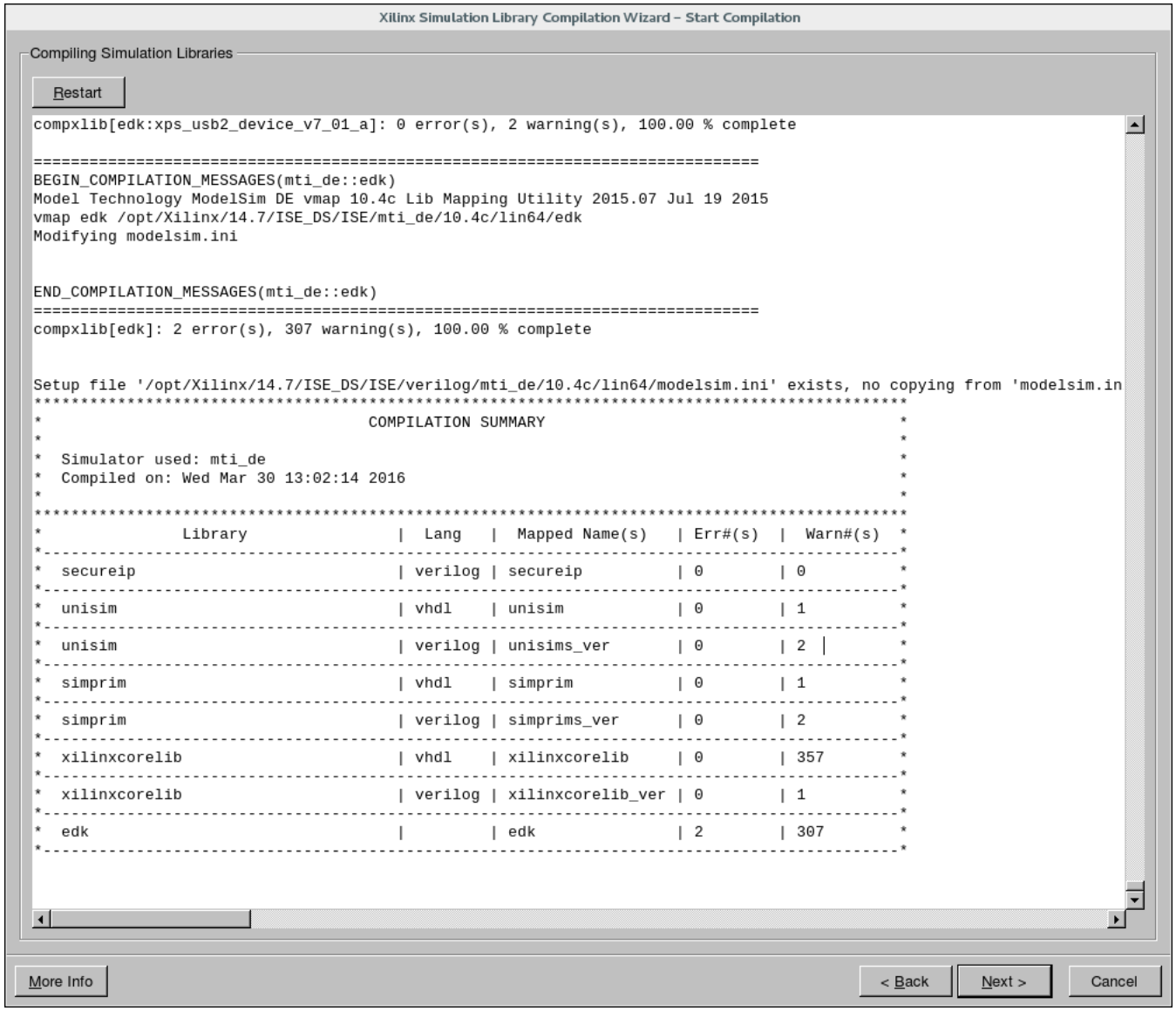

Figure 9: Compilation Wizard - Start Compilation

17. Click “Next”.

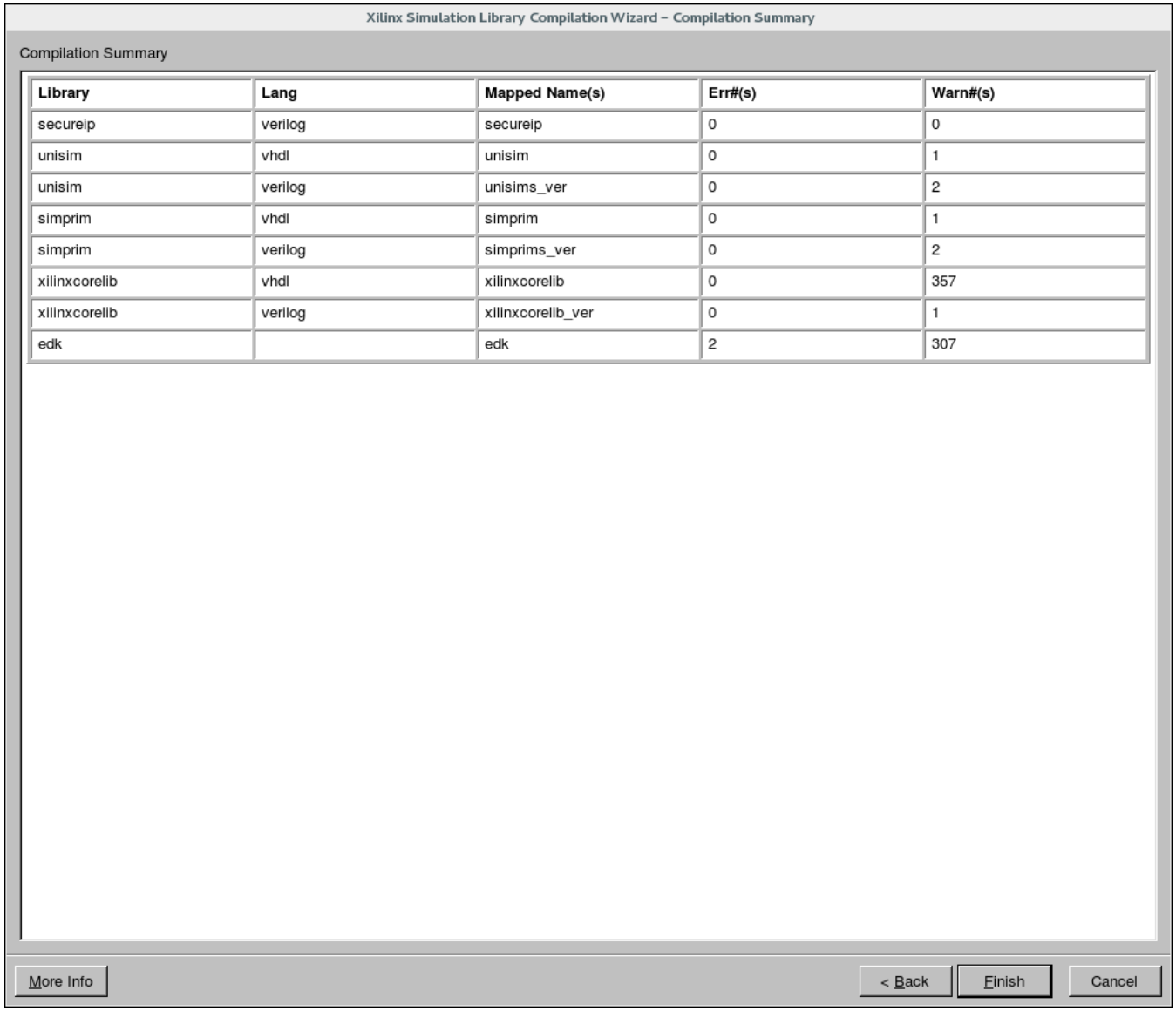

Figure 10: Compilation Wizard - Compilation Summary

18. Click “Finish”.

3 Modify "modelsim.ini" to include path to built library

This section details the steps to modify the "`modelsim.ini`" file.

1. Browse to the install directory of ModelSim
   ```
   > cd /opt/Modelsim/modelsim_dlx
   ```
2. Open the modelsim.ini file as the root user
   ```
   > vi modelsim.ini
   ```
3. Locate the bottom of the "`[Library]`" section and add the following for Vivado:
   unifast = /opt/Xilinx/Vivado/2017.1/vhdl/modelsim/10.6a/lin64/unifast
   unisim = /opt/Xilinx/Vivado/2017.1/vhdl/modelsim/10.6a/lin64/unisim
4. Or, add the following for ISE:
   xilinxcorelib = /opt/Xilinx/14.7/ISE_DS/ISE/vhdl/mti_de/10.4c/lin64/xilinxcorelib
   unisim = /opt/Xilinx/14.7/ISE_DS/ISE/vhdl/mti_de/10.4c/lin64/unisim