Summary - DC Offset Filter

Name	dc_offset_filter
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets.dsp_comps
Workers	dc_offset_filter.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The DC Offset Cancellation Filter worker inputs complex signed samples, filters the DC bias from both I and Q input rails using separate 1st-order IIR filters, and outputs complex signed samples. The response time of the filter is programmable, as is the ability to bypass the filter and to update/hold the calculated DC value to be removed. For the HDL worker, a generic controls insertion of a peak detection circuit applied to the worker's output samples.

The time constant input $TC = 128 * \alpha$ is limited to a signed eight-bit number, which helps to control the bit growth of the multiplier. Rearranging the equation, $\alpha = TC/128$, where a maximum value of +127 is allowed due to signed multiplication. Furthermore, $0 < \alpha < 1$ for stable operation. Larger values of TC give both a faster filter response and a narrower frequency magnitude notch at zero Hertz. A typical value of $TC = 121$ ($\alpha = 0.95$) is used by default.

Worker Implementation Details

dc_offset_filter.hdl

This implementation uses a single multiplier per I/Q rail to process input data at the clock rate - i.e. this worker can handle a new input value every clock cycle. A peak detection circuit may be optionally included at build-time, which provides monitoring of the output amplitude, and may be used to influence the input gain. It is recommended to attenuate the input by one bit to prevent overflows; i.e. the input should not be driven more than half-scale to avoid overflow. This filter will produce valid output one clock cycle after each valid input.

The DC Offset Cancellation Filter worker utilizes the OCPI *iqstream_protocol* for both input and output ports. The *iqstream_protocol* defines an interface of 16-bit complex signed samples. The `DATA_WIDTH_p` parameter may be used to reduce the worker's internal data width to less than 16-bits.

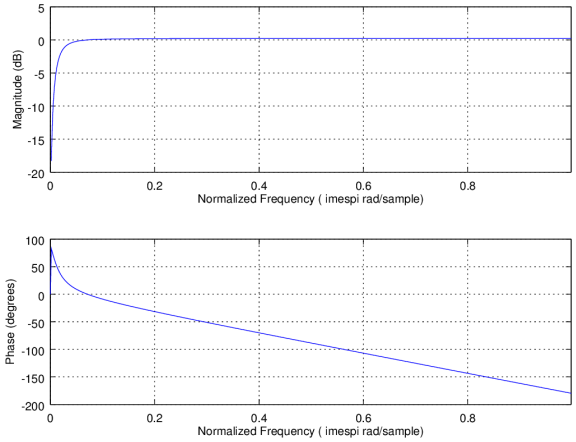


Figure 1: Ideal Filter Magnitude & Phase Response for $\alpha = .95$

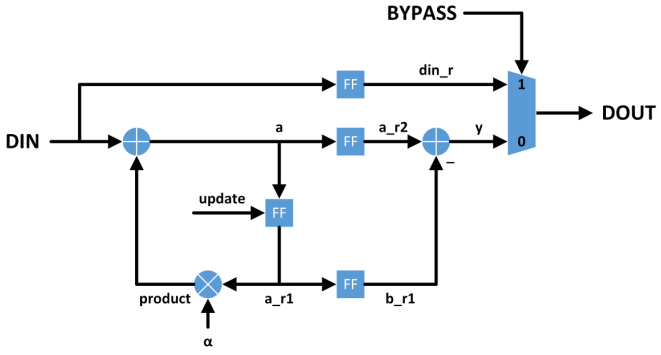


Figure 2: Circuit Diagram

The BYPASS input is available to either enable (true) or bypass (false) the circuit. Note that a single bypass register is used, as shown in Figure 2 below.

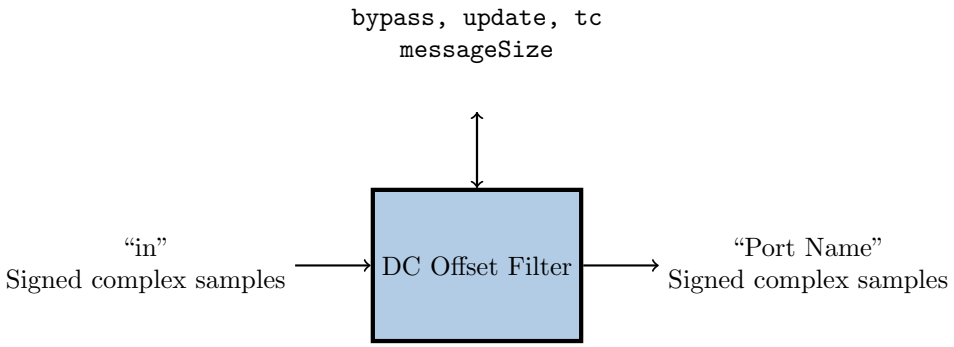
Theory

The filter is based upon Richard G. Lyons' "Understanding Digital Signal Processing, Third Edition" DC Removal circuit found on Page 761. The text may also be found online here: DSP-Tricks-DC-Removal. Lyons' circuit in Figure 13-62d implements the transfer function given in (13-118), which is a 1st-order IIR filter. From Lyons: "a zero resides at $z = 1$ providing infinite attenuation at DC (zero Hz) and a pole at $z = \alpha$ making the magnitude notch at DC very sharp. The closer α is to unity, the narrower the frequency magnitude notch centered at zero Hz."

Adding a delay element to the output, y, does not change the transfer function. Moving the single delay element following the output adder to two delay elements feeding the output adder also does not change the transfer function.

Block Diagrams

Top level



Source Dependencies

dc_offset_filter.hdl

- projects/assets/components/dsp_comps/dc_offset_filter/dc_offset_filter.vhd
- projects/assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  projects/assets/hdl/primitives/dsp_prims/dc_offset/src/dc_offset_cancellation.vhd
- projects/assets/hdl/primitives/util_prims/util_prims_pkg.vhd
  projects/assets/hdl/primitives/util_prims/pd/src/peakDetect.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
bypass	Bool	-	-	Readable, Writable	Standard	false	Bypass control
update	Bool	-	-	Readable, Writable	Standard	true	Update the calculated DC value to be removed, or hold a previously calculated value
tc	UChar	-	-	Readable, Writable	1-127	121	The location of the filter pole along the x-axis between 0 (the origin) and 1 (the unit circle), where $\alpha = tc/128$
messageSize	UShort	-	-	Readable, Writable	8192	8192	Number of bytes in output message

Worker Properties

dc_offset_filter.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	DATA_WIDTH_p	ULong	-	-	Readable,Parameter	1-16	16	Worker internal non-sign-extended data width
Property	PEAK_MONITOR_p	Bool	-	-	Readable,Parameter	Standard	true	Include a peak detection circuit
Property	LATENCY_p	Ushort	-	-	Readable,Parameter	Standard	1	Number of clock cycles between a valid input and a valid output
Property	peak	Short	-	-	Volatile	Standard	0	Read-only amplitude which may be useful for gain control

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	iqstream_protocol	false	-	Signed complex samples
out	true	iqstream_protocol	false	-	Signed complex samples

Worker Interfaces

dc_offset_filter.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	ZeroLengthMessages=true	Signed complex samples
StreamInterface	out	32	ZeroLengthMessages=true, InsertEOM=1	Signed complex samples

Control Timing and Signals

The DC Offset Cancellation Filter worker uses the clock from the Control Plane and standard Control Plane signals.

Worker Configuration Parameters

dc_offset_filter.hdl

Table 1: Table of Worker Configurations for worker: dc_offset_filter

Configuration
0

Performance and Resource Utilization

dc_offset_filter.hdl

Table 2: Resource Utilization Table for worker "dc_offset_filter"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	465	371	N/A	DSP18: 4
0	zynq	Vivado	2017.1	xc7z020clg484-1	460	398	N/A	DSP48E1: 2
0	zynq_ise	ISE	14.7	7z020clg484-1	457	535	167.403	DSP48E1: 2
0	virtex6	ISE	14.7	6vlx240tff1156-1	457	535	165.245	DSP48E1: 2

Test and Verification

Two test cases are implemented to validate the DC Offset Filter component:

1) Normal mode

2) Bypass mode

For both cases, the input file is a waveform with tones at 5 Hz, 13 Hz, and 27 Hz, and adds a DC bias at 0 Hz. The values are scaled to fixed-point signed 16-bit integers, with a maximum amplitude of 22938 to avoid internal overflow.

Time and frequency domain plots may be viewed in Figures 3 and 4 below, respectively, where the time domain plot represents the first 128 complex samples in the file.

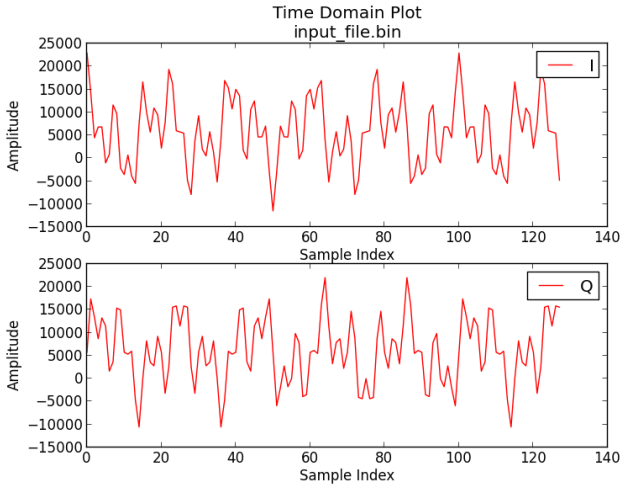


Figure 3: Time Domain Tones with DC bias

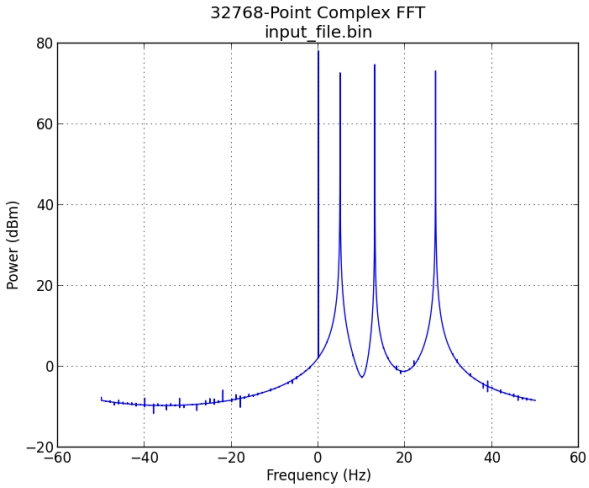


Figure 4: Frequency Domain Tones with DC bias

For verification of case 1, the output file is first checked that the data is not all zero, and is then checked for the expected length of 32,768 complex samples. Additionally, both the input and output data are translated to the frequency domain, where a FFT is performed, and then power measurements are taken at DC (zero Hz), 5 Hz, 13 Hz, and 27 Hz. The input and output power measurements are compared to validate that the DC bias has been attenuated and that the other tones have not been attenuated. Figures 5 and 6 depict the filtered results of the three tone input. Again, the time domain figure represents the first 128 complex samples in the output time domain file.

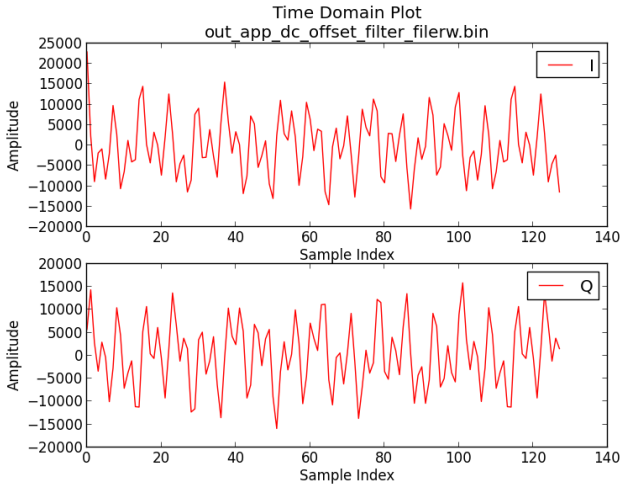


Figure 5: Time Domain Tones with DC removed

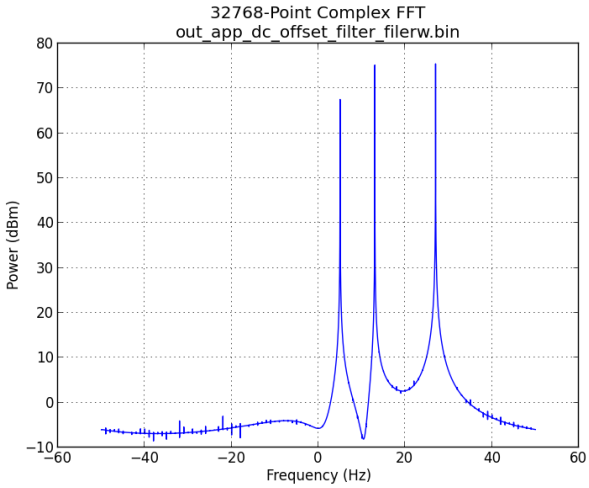


Figure 6: Frequency Domain Tones with DC removed

For case 2, the input data is forwarded to the output port. For verification of this case, the output file is byte-wise compared to the input file.

References

1) Richard G. Lyons. *Understanding Digital Signal Processing.* Third Edition. Pearson Education, Inc., Boston. 2001.

2) Richard G. Lyons. (2008, August 11). *DSP Tricks: DC Removal.* Retrieved from http://www.embedded.com/ design/configurable-systems/4007653/DSP-Tricks-DC-Removal.