Summary - AD9361 Data Sub

Name	ad9361_data_sub
Worker Type	Device
Version	v1.4
Release Date	10/2018
Component Library	ocpi.assets.devices
Workers	ad9361_data_sub.hdl
Tested Platforms	• Agilent Zedboard/Analog Devices FMCOMMS2 • Agilent Zedboard/Analog Devices FMCOMMS3 • x86/Xilinx ML605/Analog Devices FMCOMMS2 • x86/Xilinx ML605/Analog Devices FMCOMMS3 • Ettus E310 (Vivado only)

Functionality

The AD9361 Data Sub is a subdevice worker that interfaces with the AD9361 IC[1]'s DATA_CLK_P/DATA_CLK_N, P0_D[11:0], P1_D[11:0], RX_FRAME_P, RX_FRAME_N, TX_FRAME_P, TX_FRAME_N, TXNRX, and ENABLE pins. P0_D and P1_D pins are routed to whichever ad9361_adc_sub.hdl or ad9361_dac_sub.hdl device worker is appropriate for the given AD9361 data pin interface configuration.

Worker Implementation Details

ad9361_data_sub.hdl

This worker's `LVDS_p`, `HALF_DUPLEX_p`, `SINGLE_PORT_p`, and `SWAP_PORTS_p` parameter properties enforce build-time configuration[1] for all of the possible AD9361 data pin interface configurations[2]:

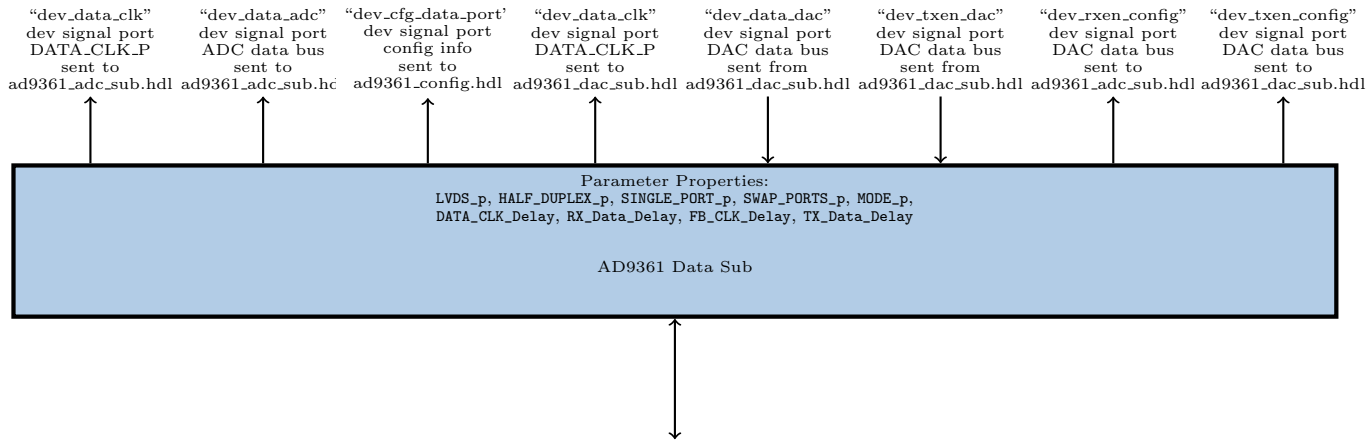
- CMOS Single Port Half Duplex,
- CMOS Single Port Half Duplex Swapped Ports,
- CMOS Single Port Full Duplex,
- CMOS Single Port Full Duplex Swapped Ports,
- CMOS Dual Port Half Duplex,
- CMOS Dual Port Half Duplex Swapped Ports,
- CMOS Dual Port Full Duplex,
- CMOS Dual Port Full Duplex Swapped Ports, and
- LVDS (Dual Port Full Duplex).

Note that the half duplex data interface formats allow for AD9361 P0/P1 port routing to be runtime-dynamic.

[1] Although this worker successfully builds for all data interface configurations, LVDS is the only configuration which has been tested and fully verified.

Block Diagrams

Top level



Source Dependencies

ad9361_data_sub.hdl

- assets/hdl/devices/ad9361_data_sub.hdl/ad9361_data_sub.cpp_vhd

Component Spec Attributes

Attribute	Value
NoControl	True

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
-	-	-	-	-	-	-	-

Worker Properties

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Scope	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	LVDS_p	Bool	-	-	Parameter	Standard	False	Use LVDS mode for Data/clock/frame signals, otherwise use CMOS mode. Default is CMOS/single-ended mode.
Property	HALF_DUPLEX_p	Bool	-	-	Parameter	Standard	False	Use half duplex mode, otherwise use full duplex mode. Must be false when using LVDS mode.
Property	SINGLE_PORT_p	Bool	-	-	Parameter	Standard	False	Use single port, otherwise use both (dual) ports. Default is to use both ports. Must be false when using LVDS mode.
Property	SWAP_PORTS_p	Bool	-	-	Parameter	Standard	False	Swaps Port 0 and Port 1. Must be false when using LVDS mode.
Property	MODE_p	UShort	-	-	Parameter	Standard	lvds_p ? 7 : single_port_p ? (half_duplex_p ? (swap_ports_p ? 1 : 0) : (swap_ports_p ? 3 : 2)) : half_duplex_p ? 4 : swap_ports_p ? 6 : 5)	a convenience parameter to map the various options into 8 modes.

Property	DATA_CLK_Delay	UShort	-	-	Parameter	Standard	-	Ushort representation of AD9361 SPI Register 0x006 - DATA_CLK Delay bits. These bits affect the DATA_CLK delay. The typical delay is approximately 0.3 ns/LSB. Minimum delay setting is 0x0 and maximum delay setting is 0xF. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the DATA_CLK delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.
Property	RX_Data_Delay	UShort	-	-	Parameter	Standard	-	Ushort representation of AD9361 SPI Register 0x006 - RX Data Delay bits. These bits affect the Rx data delay. The typical delay is approximately 0.3 ns/LSB. Minimum delay setting is 0x0 and maximum delay setting is 0xF. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the Rx data delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.

Property	FB_CLK_Delay	UShort	-	-	Parameter	Standard	-	Ushort representation of AD9361 SPI Register 0x007 - FB_CLK Delay bits. These bits function the same as DATA_CLK and RX data delays but affect the FB_CLK delay. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the FB_CLK delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.
Property	TX_Data_Delay	UShort	-	-	Parameter	Standard	-	Ushort representation of AD9361 SPI Register 0x007 - TX Data Delay bits. These bits function the same as DATA_CLK and RX data delays but affect the Tx_FRAME and TX Data delay. Tx frame sync is delayed the same amount as the data port bits. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the Tx_FRAME/TX Data delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

Worker Interfaces

ad9361_data_sub.hdl

Type	Name	Count	Optional	Master	Signal	Direction	Width	Description
DevSignal	dev_cfg_data_port	1	False	False	iostandard_is_lvds	Input	1	Value is 1 if the buildtime configuration was for the LVDS mode and 0 otherwise.
					p0_p1_are_swapped	Input	1	Value is 1 if the buildtime configuration was with the AD9361 P0 and P1 data port roles inverted and 0 otherwise.
DevSignal	dev_data_clk	3	True	False	DATA_CLK_P	Input	1	Buffered version of AD9361 DATA_CLK_P pin.
DevSignal	dev_data_adc	1	True	False	data	Input	24	Data bus driven by configuration-specific AD9361 pins corresponding to the RX data path: * CMOS single port half duplex: [12'b0 P0_D[11:0]], * CMOS single port full duplex: [18'b0 P0_D[5:0]], * CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]], * CMOS dual port full duplex: [12'b0 P0_D[11:0]], * LVDS: [18'b0 RX_D[5:0]], or, if ports are swapped: * CMOS single port half duplex: [12'b0 P1_D[11:0]], * CMOS single port full duplex: [18'b0 P1_D[5:0]], * CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]], * CMOS dual port full duplex: [12'b0 P1_D[11:0]], * LVDS: (unsupported with port swap).
					rx_frame	Input	1	Output of buffer whose input is the AD9361 RX_FRAME_P pin's signal.
DevSignal	dev_data_dac	1	True	False	data	Output	24	Data bus which drives configuration-specific AD9361 pins corresponding to the TX data path: * CMOS single port half duplex: [12'b0 P0_D[11:0]], * CMOS single port full duplex: [18'b0 P0_D[11:6]], * CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]], * CMOS dual port full duplex: [12'b0 P1_D[11:0]], * LVDS: [18'b0 TX_D[5:0]], or, if ports are swapped: * CMOS single port half duplex: [12'b0 P1_D[11:0]], * CMOS single port full duplex: [18'b0 P1_D[11:6]], * CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]], * CMOS dual port full duplex: [12'b0 P0_D[11:0]], * LVDS: (unsupported with port swap).
					tx_frame	Output	1	Signal which will drive the output buffer which drives the AD9361 TX_FRAME_P pin.
DevSignal	dev_txen_dac	1	True	False	txen	Output	1	
DevSignal	dev_rxen_config	1	True	False	rxen	Input	1	
DevSignal	dev_txen_config	1	True	False	txen	Input	1	

Subdevice Connections

Supports Worker	Supports Worker Port	ad9361_data_sub.hdl Port	ad9361_data_sub.hdl Port Index
ad9361_config	dev_cfg_data_port	dev_cfg_data_port	0
	dev_rxen_data_sub	dev_rxen_config	0
	dev_txen_data_sub	dev_txen_config	0
	dev_data_clk	dev_data_adc	2
ad9361_adc_sub	dev_data_clk	dev_data_clk	0
	dev_data_from_pins	dev_data_adc	0
ad9361_dac_sub	dev_data_clk	dev_data_clk	1
	dev_data_to_pins	dev_data_adc	0

Control Timing and Signals

Because this worker does not include a control plane and serves purely as an IC pin buffering and routing mechanism, there are no latency or clock domain considerations. For considerations specific to the RX/TX data paths, see the supports-connected device worker data sheets for ad9361_adc_sub.hdl[3] and ad9361_dac_sub.hdl[4].

Performance and Resource Utilization

Worker Configuration Parameters

ad9361_data_sub.hdl

Table 2: Table of Worker Configurations for worker: ad9361_data_sub

Configuration	LVDS_p	HALF_DUPLEX_p	FB_CLK_Delay	RX_Data_Delay	SINGLE_PORT_p	TX_Data_Delay	SWAP_PORTS_p	DATA_CLK_Delay
0	true	false	7	0	false	0	false	2
1	true	false	7	0	false	0	false	3
2	false	false	12	0	true	0	false	7
3	false	false	12	0	true	0	true	7
4	false	false	12	0	false	0	false	7
5	false	false	12	0	false	0	true	7

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Because every possible parameter property combination of this worker has no control plane and no registered data paths, no registers or LUTS are used and the Fmax measurement does not exist.

Table 3: Resource Utilization Table for worker "ad9361_data_sub"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	1	N/A	ODDR: 1 BUFR: 1
0	zynq_ise	ISE	14.7	7z020clg484-1	1	1	N/A	BUFR: 1 ODDR: 1
0	virtex6	ISE	14.7	6vlx240tff1156-1	1	1	N/A	BUFR: 1 ODDR: 1
1	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	1	N/A	ODDR: 1 BUFR: 1
1	zynq_ise	ISE	14.7	7z020clg484-1	1	1	N/A	BUFR: 1 ODDR: 1
1	virtex6	ISE	14.7	6vlx240tff1156-1	1	1	N/A	BUFR: 1 ODDR: 1
2	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
2	zynq_ise	ISE	14.7	7z020clg484-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
2	virtex6	ISE	14.7	6vlx240tff1156-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
3	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
3	zynq_ise	ISE	14.7	7z020clg484-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
3	virtex6	ISE	14.7	6vlx240tff1156-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
4	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
4	zynq_ise	ISE	14.7	7z020clg484-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
4	virtex6	ISE	14.7	6vlx240tff1156-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
5	zynq	Vivado	2017.1	xc7z020clg484-1	N/A	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1

5	zynq_ise	ISE	14.7	7z020clg484-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1
5	virtex6	ISE	14.7	6vlx240tff1156-1	1	N/A	N/A	BUFGCTRL: 1 BUFG: 1 ODDR: 1

Test and Verification

The test outlined in [4] includes validation of this worker's functionality (for LVDS mode and CMOS Single Port Full Duplex DDR mode).

References

[1] AD9361 Datasheet and Product Info
`http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband`

[2] AD9361 Reference Manual UG-570
AD9361_Reference_Manual_UG-570.pdf

[3] AD9361 ADC Component Data Sheet
`https://opencpi.github.io/assets/AD9361_ADC.pdf`

[4] AD9361 DAC Component Data Sheet
`https://opencpi.github.io/assets/AD9361_DAC.pdf`