Summary - FIR Real SSE

WARNING: Run-time failures have been observed for several unit tests and applications on PCIe-based platforms. The work around requires modifying the **buffersize** attribute of the PL to PS (egress) boundary connection, as defined in the OAS. An example for modifying the OAS for executing on PCIe-based platforms is provided in a below section.

Name	fir_real_sse
Worker Type	Application
Version	v1.4
Release Date	September 2018
Component Library	ocpi.assets.dsp_comps
Workers	fir_real_sse.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The FIR Real SSE (Systolic Symmetric Even) component inputs real signed samples and filters them based upon a programmable number of coefficient tap values. The underlying FIR Filter implementation makes use of a symmetric systolic structure to construct a filter with an even number of taps and symmetry about its midpoint.

Worker Implementation Details

fir_real_sse.hdl

The `NUM_TAPS_p` parameter defines N/2 coefficient values. Care should be taken to ensure that the `COEFF_WIDTH_p` parameter is $\leq$ the type (size) of the taps property - i.e. a `COEFF_WIDTH_p` of 1-8 should use a taps type of char; a `COEFF_WIDTH_p` of 9-16 should use a taps type of short; and a `COEFF_WIDTH_p` of 17-32 should use a taps type of long.

This implementation uses `NUM_TAPS_p` multipliers to process input data at the clock rate - i.e. this worker can handle a new input value every clock cycle. It is unnecessary to round the output data from this filter at the worker level because it is already being done within the macc_systolic_sym primitive.

The FIR Real SSE worker utilizes the OCPI *rstream_protocol* for both input and output ports. The *rstream_protocol* defines an interface of 16-bit real signed samples. The `DATA_WIDTH_p` parameter may be used to reduce the worker's internal data width to less than 16-bits.

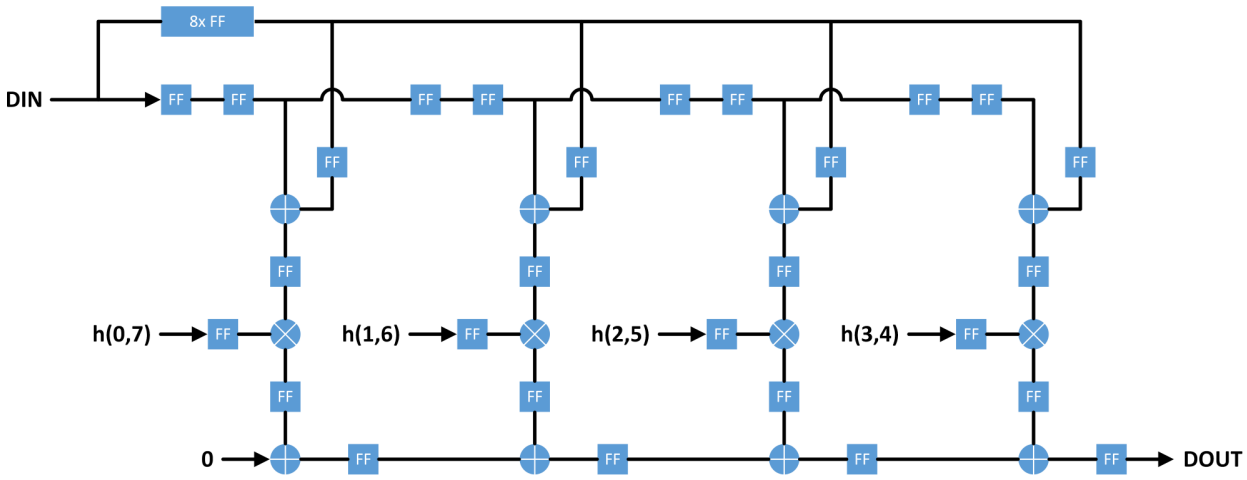


Figure 1: FIR Real SSE Block Diagram - 8-tap example

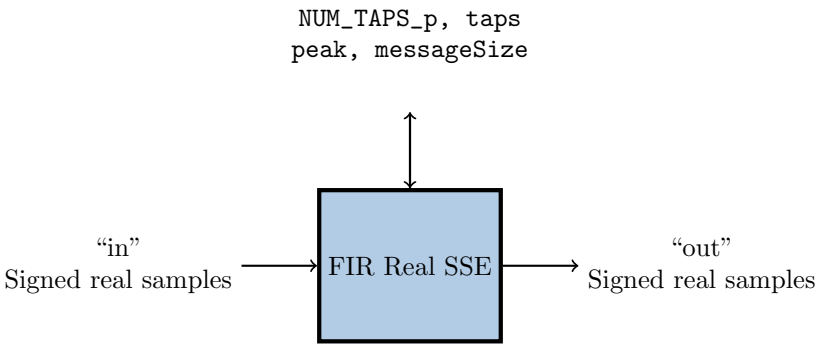
Theory

This filter will produce valid outputs one clock after each valid input, but care must be exercised when attempting to align outputs according to the filter's actual group delay and propagation delay.

For a FIR filter with symmetric impulse response we are guaranteed to have linear phase response and thus constant group delay vs. frequency. In general, the group delay will be equal to (N-1)/2, where N is the number of filter taps. The filter topology itself will add some propagation delay to the response. For this design the total delay from an impulse input to the beginning of the impulse response will be `NUM_TAPS_p` + 4 samples.

Block Diagrams

Top level



State Machine

Only one finite-state machine (FSM) is implemented by this worker. The FSM supports Zero-Length Messages.

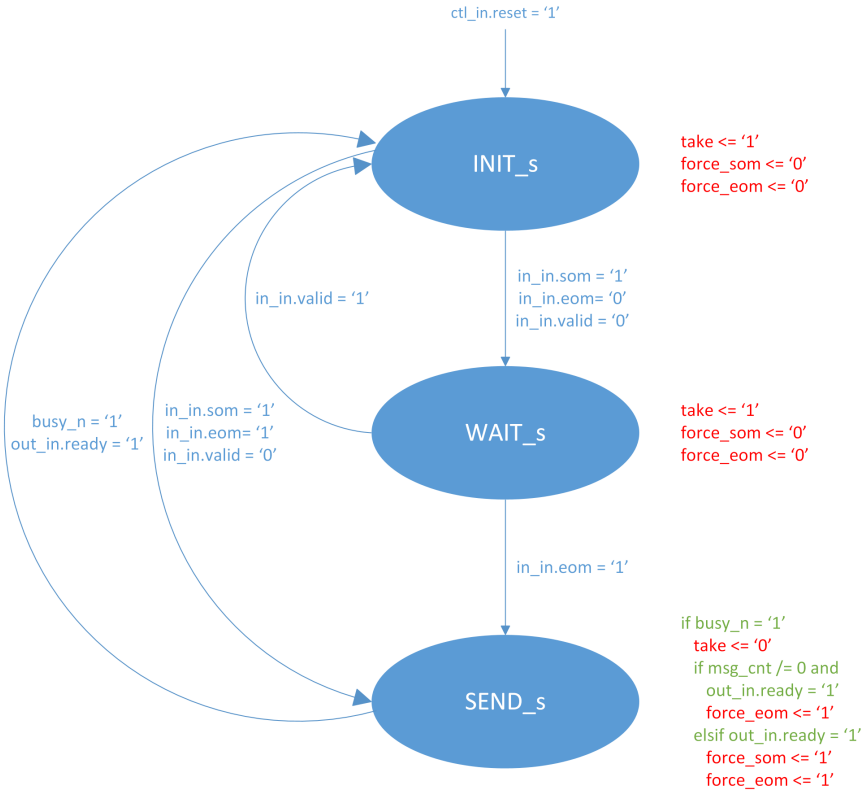


Figure 2: Zero-Length Message FSM

Note: In future releases this finite-state machine will be replaced with a register-delay based mechanism, currently exemplified in the dc offset filter

Source Dependencies

fir_real_sse.hdl

- assets/components/dsp_comps/fir_real_sse.hdl/fir_real_sse.vhd
- assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  assets/hdl/primitives/dsp_prims/fir/src/fir_systolic_sym_even.vhd
  assets/hdl/primitives/dsp_prims/fir/src/macc_systolic_sym.vhd
- assets/hdl/primitives/misc_prims/misc_prims_pkg.vhd
  assets/hdl/primitives/misc_prims/round_conv/src/round_conv.vhd
- assets/hdl/primitives/util_prims/util_prims_pkg.vhd
  assets/hdl/primitives/util_prims/pd/src/peakDetect.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
NUM_TAPS_p	ULong	-	-	Readable, Parameter	1-?	16	Half the number of coefficients used by each even symmetric filter
peak	Short	-	-	Volatile	Standard	0	Read-only amplitude which may be useful for gain control
messageSize	UShort	-	-	Writable, Readable	8192	8192	Number of bytes in output message
taps	Short	-	NUM_TAPS_p	Writable, Readable	$-2^{\text{COEFF\_WIDTH\_p-1}}$ to $+2^{\text{COEFF\_WIDTH\_p-1}}-1$	-	Symmetric filter coefficient values

Worker Properties

fir_real_sse.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	DATA_WIDTH_p	ULong	-	-	Readable, Parameter	1-16	16	Worker internal non-sign-extended data width
Property	COEFF_WIDTH_p	ULong	-	-	Readable, Parameter	1-32	16	Coefficient width

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	rstream_protocol	false	-	Real signed samples
out	true	rstream_protocol	false	-	Real signed samples

Worker Interfaces

fir_real_sse.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	16	ZeroLengthMessages=true	Signed real samples
StreamInterface	out	16	ZeroLengthMessages=true	Signed real samples

Control Timing and Signals

The FIR Real SSE worker uses the clock from the Control Plane and standard Control Plane signals. The Raw Property interface is used to read/write coefficient values.

Worker Configuration Parameters

fir_real_sse.hdl

Table 1: Table of Worker Configurations for worker: fir_real_sse

Configuration	DATA_WIDTH_p	NUM_TAPS_p	ocpi_endian	ocpi_debug	COEFF_WIDTH_p
0	16	64	little	false	16
1	16	128	little	false	16

Performance and Resource Utilization

fir_real_sse.hdl

Table 2: Resource Utilization Table for worker: fir_real_sse

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	zynq	Vivado	2017.1	xc7z020clg484-1	5319	3596	N/A	DSP48E1: 64
0	virtex6	ISE	14.7	6vlx240tff1156-1	4295	5038	156.495	DSP48E1: 64
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	6426	5063	N/A	DSP18: 128
1	zynq	Vivado	2017.1	xc7z020clg484-1	9448	7229	N/A	DSP48E1: 128
1	virtex6	ISE	14.7	6vlx240tff1156-1	8392	9805	156.495	DSP48E1: 128
1	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	12635	9912	N/A	DSP18: 256

Test and Verification

WARNING: Run-time failures have been observed for several unit tests and applications on PCIe-based platforms. The work around requires modifying the **buffersize** attribute of the PL to PS (egress) boundary connection, as defined in the OAS.
The OAS XML must be changed to resolve this issue for the unit tests as shown below:

```
<Connection>
 <Port Instance="last_PL_worker" Name="out"/>
 <Port Instance="first_PS_worker" Name="in" Buffersize="8192" Buffercount="4"/>
</Connection>
```

Two test cases are implemented to validate the FIR Real SSE component as dictated by parameter values for `NUM_TAPS_p`: 64 and 128. In each case the python script *gen_lpf_taps.py* is used to generate a taps file consisting of `NUM_TAPS_p` filter coefficients. Input data is generated by first creating a *.dat input file consisting of a single maximum signed value of +32767 followed by 2*(`NUM_TAPS_p`-1) zero samples. The *.bin input file is the binary version of the *.dat ASCII file repeated 2*`NUM_TAPS_p` times.

The FIR Real SSE worker inputs real signed samples, filters the input as defined by the coefficient filter taps, and outputs real signed samples. Since the input consists of an impulse response - that is, a maximal 'one' sample followed by all zeros equal to the length of the filter - the output is simply the coefficient values.

For verification, the output file is compared against the taps file, where a ±1 difference is allowed in value while comparing the output against the filter coefficient values. Figures 3 and 4 depict the filtered results of the impulse input for the case `NUM_TAPS_p`=128.

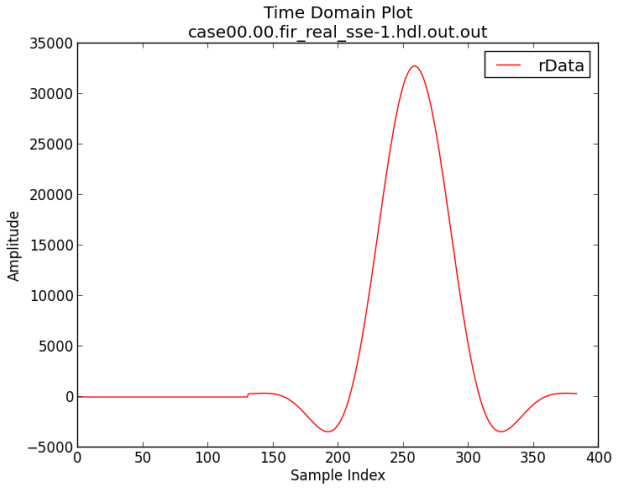


Figure 3: Time Domain Impulse Response

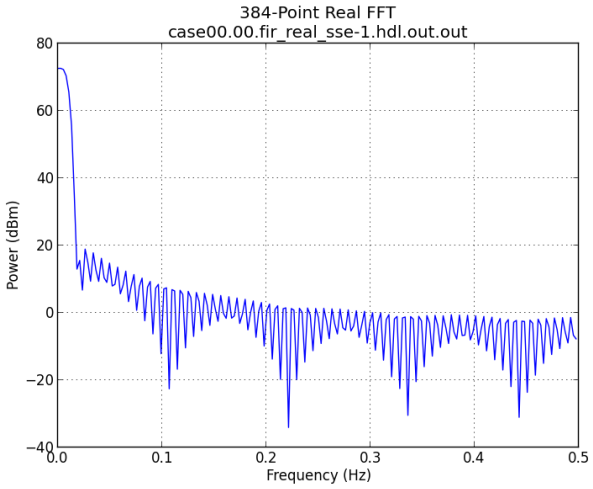


Figure 4: Frequency Domain Impulse Response