Summary - AD9361 Config

Name	ad9361_config
Worker Type	Device
Version	v1.5
Release Date	9/2018
Component Library	ocpi.assets.devices
Workers	ad9361_config.hdl
Tested Platforms	• Agilent Zedboard/Analog Devices FMCOMMS2 (Vivado only) • Agilent Zedboard/Analog Devices FMCOMMS3 (Vivado only) • x86/Xilinx ML605/Analog Devices FMCOMMS2 • x86/Xilinx ML605/Analog Devices FMCOMMS3 • Ettus E310 (Vivado only)

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1 Functionality

The AD9361 Config is a subdevice worker which provides an entry point to the major functionality of the AD9361 IC[1]. This includes both SPI bus functionality for intercommunication with the AD9361 register map as well as additional command/control between the software and the FPGA. Note that, while the register address decoding is performed within this worker, the SPI state machine itself is implemented in one or more separate, platform-specific or card-specific subdevice workers[1]. This worker's register map provides an API for integrating with Analog Devices's No-OS software[2]. This integration is implemented in [7].

2 Worker Implementation Details

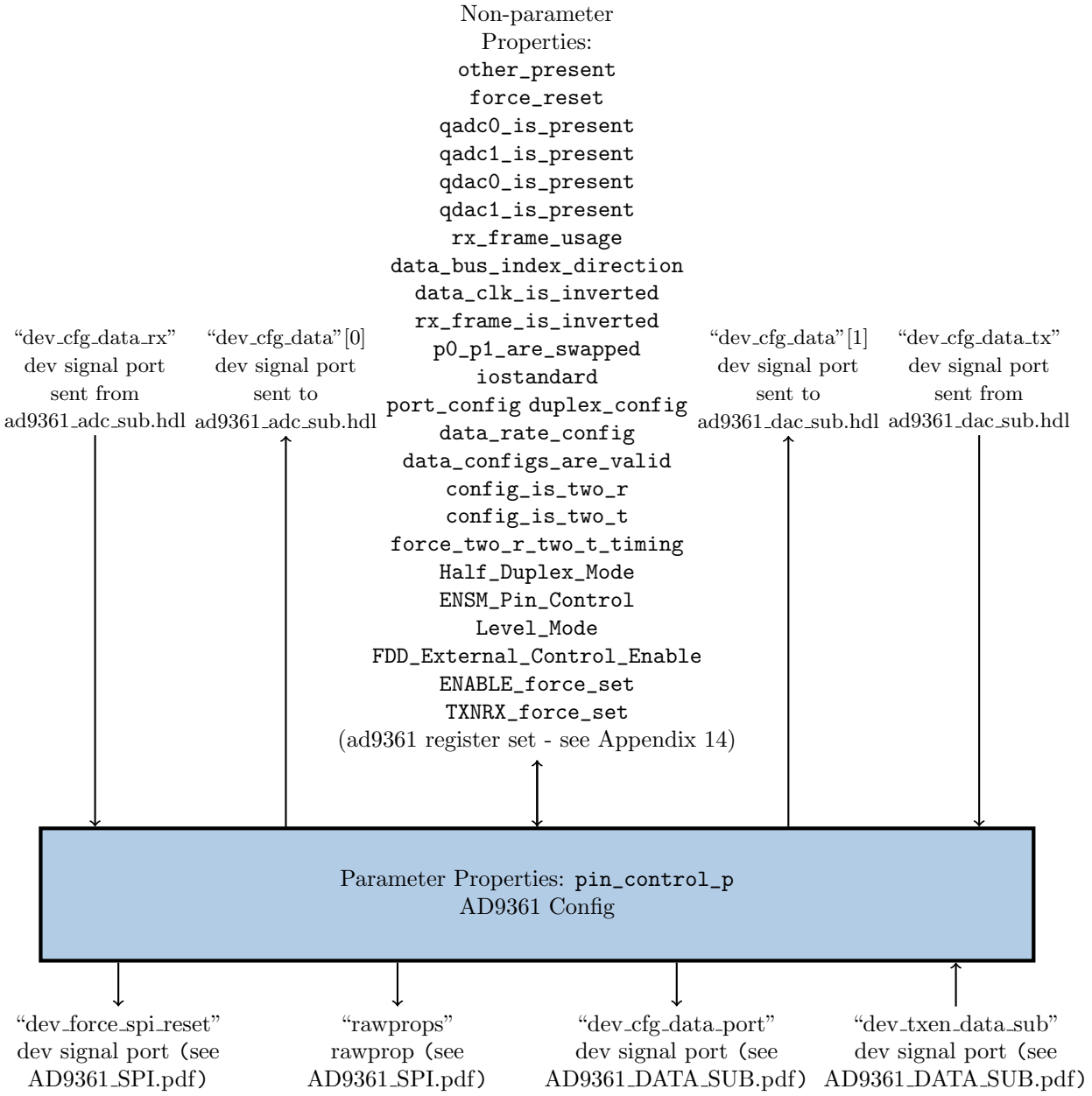
2.1 ad9361_config.hdl

The AD9361 register map is realized via a rawprops port whose communication is forwarded on to a SPI subdevice worker. The register map is implemented via the Component Spec properties for this worker, all of which correspond with the AD9361 register map specified in [4]. This worker also operates itself as subdevice which 1) conveys build-time information from the ad9361_adc_sub.hdl and ad9361_dac_sub.hdl device workers up to the processor via properties and 2) conveys processor-known assumptions about the AD9361 multichannel configuration to the ad9361_adc_sub.hdl and ad9361_dac_sub.hdl workers.

[1] For an example, see [5]

3 Block Diagrams

3.1 Top level



4 Source Dependencies

4.1 ad9361_config.hdl

- assets/hdl/devices/ad9361_config.hdl/ad9361_config.vhd
- assets/hdl/devices/ad9361_config.hdl/signals.vhd

5 Component Spec Properties

See Appendix 14.

6 Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

7 Worker Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
pin_control_p	Bool	-	-	Parameter	Standard	-	Whether RX/TX powerdown via pin control is possible.

8 Worker Interfaces

8.1 ad9361_config.hdl

Type	Name	Master
Rawprop	rawprops	True

Type	Name	Count	Optional	Master	Signal	Direction	Width	Description
DevSignal	dev_force_spi_reset	1	False	True	force_reset	Output	1	Used to force AD9361 RESETB pin, which is active-low, to logic 0.
DevSignal	dev_cfg_data_port	1	False	True	iostandard_is_lvds	Input	1	Value is 1 if the buildtime configuration was for the LVDS mode and 0 otherwise.
					p0_p1_are_swapped	Input	1	Value is 1 if the buildtime configuration was with the AD9361 P0 and P1 data port roles inverted and 0 otherwise.
DevSignal	dev_cfg_data	2	True	False	config_is_two_r	Input	1	Some data port configurations (such as LVDS) require the TX bus to use 2R2T timing if either 2 TX or 2 RX channels are used. For example, if using LVDS and this has a value of 1, 2R2T timing will be forced.
					ch0_handler_is_present	Output	1	Value is 1 if the dev_data_ch0 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					ch1_handler_is_present	Output	1	Value is 1 if the dev_data_ch1 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					data_bus_index_direction	Output	1	Value is 1 if the bus indexing of the P0_D/P1_D signals from dev_data_from_pins was reversed before processing. This is expected to be hardcoded at buildtime.
					data_clk_is_inverted	Output	1	Value is 1 if the clock in via dev_data_clk was inverted inside this worker before used as an active-edge rising clock. This is expected to be hardcoded at buildtime.
					islvds	Output	1	Value is 1 if `DIFFERENTIAL_p` has a value of true and 0 if `DIFFERENTIAL_p` has a value of false. Because `DIFFERENTIAL_p` is a parameter property, this is hardcoded at buildtime.
					isdualport	Output	1	Value is 1 if `PORT_CONFIG_p` has a value of dual and 0 if `PORT_CONFIG_p` has a value of single. Because `PORT_CONFIG_p` is a parameter property, this is hardcoded at buildtime.
					isfullduplex	Output	1	Value is 1 if `DUPLEX_CONFIG_p` has a value of full_duplex and 0 if `DUPLEX_CONFIG_p` has a value of half_duplex. Because `DUPLEX_CONFIG_p` is a parameter property, this is hardcoded at buildtime.
					isDDR	Output	1	Value is 1 if `DATA_RATE_CONFIG_p` has a value of DDR and 0 if `DATA_RATE_CONFIG_p` has a value of SDR. Because `DATA_RATE_CONFIG_p` is a parameter property, this is hardcoded at buildtime.
					present	Output	1	Used to communicate to ad9361_config.hdl that it should validate the islvds, isdualport, isfullduplex, and isddr signals against similar signals in the ad9361_adc_sub.hdl and ad9361_data_sub.hdl workers if they are present in the bitstream. This is expected to be hardcoded at buildtime.
DevSignal	dev_cfg_data_rx	1	True	False	rx_frame_usage	Output	1	Value is 1 of worker was built with the assumption that the RX frame operates in its toggle setting and 0 if the assumption was that RX frame has a rising edge on the first sample and then stays high. This value is intended to match that of AD9361 register 0x010 BIT D3[4]. This is expected to be hardcoded at buildtime.
					rx_frame_is_inverted	Output	1	Rx path-specific data port configuration. Used to tell other workers about the configuration that was enforced when this worker was compiled. This is expected to be hardcoded at buildtime.
DevSignal	dev_cfg_data_tx	1	True	False	config_is_two_t	Input	1	Some data port configurations (such as LVDS) require the TX bus to use 2R2T timing if either 2 TX or 2 RX channels are used. For example, if using LVDS and this has a value of 1, 2R2T timing will be forced.
					force_two_r_two_t_timing	Input	1	Expected to match value of AD9361 register 0x010 bit D2[4].
DevSignal	dev_rxen_data_sub	1	False	True	rxen	Input	1	
DevSignal	dev_txen_data_sub	1	False	True	txen	Input	1	

9 Subdevice Connections

Supports Worker	Supports Worker Port	ad9361_config.hdl Port	Index
ad9361_adc_sub	dev_cfg_data dev_cfg_data_rx	dev_cfg_data dev_cfg_data_rx	0 0
ad9361_dac_sub	dev_cfg_data dev_cfg_data_tx	dev_cfg_data dev_cfg_data_tx	1 0

10 Control Timing and Signals

The AD9361 Config subdevice worker operates in the control plane clock domain. Note that this worker is essentially the central worker that command/control passes through, and no RX or TX data paths flow through this worker.

11 Performance and Resource Utilization

12 Worker Configuration Parameters

12.1 ad9361_config.hdl

Table 3: Table of Worker Configurations for worker: ad9361_config

Configuration	ocpi_debug	pin_control_p	ocpi_endian
0	false	true	little

12.2 ad9361_config.hdl

Fmax refers to the maximum allowable clock rate for any registered signal paths within a given clock domain for an FPGA design. Fmax in the table below is specific only to this worker and represents the maximum possible Fmax for any OpenCPI bitstream built with this worker included. Note that the Fmax value for a given clock domain for the final bitstream is often worse than the Fmax specific to this worker, even if this worker is the only one included in the bitstream.

Table 4: Resource Utilization Table for worker: ad9361_config

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	zynq	Vivado	2017.1	xc7z020clg484-1	77	123	318 [1]	N/A
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	80	167	N/A	N/A
0	virtex6	ISE	14.7	6vlx240tff1156-1	86	217	331.126	N/A

13 Test and Verification

No standalone unit test currently exists for this worker. However, the test outlined in [6] includes validation of a subset of this worker's functionality (for LVDS only).

References

[1] AD9361 Datasheet and Product Info
`http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband-transceivers-ic/ad9361.html`

[2] AD9361 No-OS Software [Analog Devices Wiki]
`https://wiki.analog.com/resources/eval/user-guides/ad-fmcomms2-ebz/software/no-os-functions`

[3] AD9361 Reference Manual UG-570
AD9361_Reference_Manual_UG-570.pdf

[4] AD9361 Register Map Reference Manual UG-671
AD9361_Register_Map_Reference_Manual_UG-671.pdf

[5] AD361 SPI Component Data Sheet
`https://opencpi.github.io/assets/AD9361_SPI.pdf`

[6] AD361 DAC Component Data Sheet
`https://opencpi.github.io/assets/AD9361_DAC.pdf`

[7] AD361 Config Proxy Component Data Sheet
`https://opencpi.github.io/assets/AD9361_Config_Proxy.pdf`

[1] These measurements were the result of a Vivado timing analysis which was different from the Vivado analysis performed by default for OpenCPI worker builds. For more info see Appendix 15

14 Appendix - ad9361_config.hdl Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
other_present	bool	-	-	Readable	-	-	-
force_reset	bool	-	-	Readable, Writeable	-	0	Forces reset pin low (active low). Reset pin is otherwise the same level as the OpenCPI control plane reset signal.
qadc0_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qadc0, which supports first RX channel
qadc1_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qadc1, which supports second RX channel
qdac0_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qdac0, which supports first TX channel
qdac1_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qdac1, which supports second TX channel
rx_frame_usage	enum	-	-	Volatile	-	-	enable : Register 0x010 bit D3 is 0, meaning Rx frame goes high coincident with the first valid receive sample. It stays high., toggle: Register 0x010 bit D3 is 1, meaning the Rx frame signal toggles with a duty cycle of 50
data_bus_index_direction	enum	-	-	Volatile	-	-	normal : Register 0x010 bit D1 is 0, meaning each RX sample's bit index direction is normal, i.e. [11:0], reverse: Register 0x010 bit D1 is 1, meaning each RX sample's bit direction is inverted, i.e. [0:11].
data_clk_is_inverted	bool	-	-	Volatile	-	-	false : Register 0x010 bit D0 is 0, meaning that the DATA_CLK follows the DATA_CLK_P signal in the UG570 timing diagrams, true : Register 0x010 bit D0 is 1, meaning that the DATA_CLK follows the DATA_CLK_N signal in the UG570 timing diagrams
rx_frame_is_inverted	bool	-	-	Volatile	-	-	false : Register 0x011 bit D2 is 0, meaning that the RX_FRAME follows the RX_FRAME_P signal in the UG570 timing diagrams, true : Register 0x011 bit D2 is 1, meaning that the RX_FRAME follows the RX_FRAME_N signal in the UG570 timing diagrams
LVDS	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use LVDS mode for Data/clock-/frame signals, and false if CMOS mode was used.
single_port	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use single port, and false if dual ports.
swap_ports	bool	-	-	Volatile	-	-	Value is true if bitstream was built to swap Port 0 and Port 1, and false if there was no swap.

half_duplex	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use half duplex mode, and false if full duplex mode.
data_rate_config	enum	-	-	Volatile	-	-	Value indicates which data rate mode (SDR/DDR) the bitstream was built to use.
data_configs_are_valid	bool	-	-	Volatile	-	-	Value is false if bitstream was built using erroneous combination of LVDS/single port/half duplex/data rate config modes (takes into account build configurations for both ad9361_adc_sub and ad9361_dac_sub workers).
config_is_two_r	bool	-	-	Readable, Writeable	-	-	Used to tell the ad9361_adc_sub and ad9361_dac_sub workers what data paths are enabled. Note that, just because a qadc or qdac worker is present in the bitstream, that doesn't mean it is enabled.
config_is_two_t	bool	-	-	Readable, Writeable	-	-	Used to tell the ad9361_dac_sub worker what data paths are enabled. Note that, just because a qdac worker is present in the bitstream, that doesn't mean it is enabled.
force_two_r_two_t_timing	bool	-	-	Readable, Writeable	-	-	Used to force the ad9361_dac_sub worker to use the 2R2T timing diagram regardless of what TX channels are enabled. This property is expected to correspond to the D2 bit of the Parallel Port Configuration 1 register at SPI address 0x010.
Half_Duplex_Mode	bool	-	-	Writeable	-	false	-
ENSM_Pin_Control	bool	-	-	Writeable	-	true	Intended to match AD9361 register 0x014 bit D4.
Level_Mode	bool	-	-	Writeable	-	false	Intended to match AD9361 register 0x014 bit D3.
FDD_External_Control_Enable	bool	-	-	Writeable	-	false	Intended to match AD9361 register 0x014 bit D7.
ENABLE_force_set	bool	-	-	Writeable	-	false	Forces set of AD9361 ENABLE pin
TXNRX_force_set	bool	-	-	Writeable	-	false	Forces set of AD9361 TXNRX pin
general_spi_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d0_0x0000 Table 1: CHIP LEVEL SETUP: SPI Configuration
general_multichip_sync_and_tx_mon_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d1_0x0001 Table 1: CHIP LEVEL SETUP: Multichip Sync and Tx Mon Control
general_tx_enable_filter_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d2_0x0002 Table 1: CHIP LEVEL SETUP: Tx Enable & Filter Control
general_rx_enable_filter_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d3_0x0003 Table 1: CHIP LEVEL SETUP: Rx Enable & Filter Control
general_input_select	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d4_0x0004 Table 1: CHIP LEVEL SETUP: Input Select
general_rfpll_dividers	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d5_0x0005 Table 1: CHIP LEVEL SETUP: RFPLL Dividers
general_rx_clock_data_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d6_0x0006 Table 1: CHIP LEVEL SETUP: Rx Clock and Data Delay

general_tx_clock_data_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d7_0x0007 Table 1: CHIP LEVEL SETUP: Tx Clock and Data Delay
ocpi_pad_008	uchar	-	-		-	-	-
clock_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d9_0x0009 Table 8: CLOCK CONTROL: Clock Enable
clock_bbpll	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d10_0x000a Table 8: CLOCK CONTROL: BBPLL
temp_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d11_0x000b Table 10: TEMPERATURE SENSOR: Offset
temp_start_reading	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d12_0x000c Table 10: TEMPERATURE SENSOR: Start Temp Reading
temp_sense2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d13_0x000d Table 10: TEMPERATURE SENSOR: Temp Sense2
temp_temperature	uchar	-	-	Volatile	-	-	reg_addr_d14_0x000e Table 10: TEMPERATURE SENSOR: Temperature
temp_sensor_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d15_0x000f Table 10: TEMPERATURE SENSOR: Temp Sensor Config
parallel_port_conf_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d16_0x0010 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 1
parallel_port_conf_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d17_0x0011 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 2
parallel_port_conf_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d18_0x0012 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 3
ensm_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d19_0x0013 Table 12: ENABLE STATE MACHINE: ENSM Mode
ensm_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d20_0x0014 Table 12: ENABLE STATE MACHINE: ENSM Config 1
ensm_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d21_0x0015 Table 12: ENABLE STATE MACHINE: ENSM Config 2
ensm_calibration_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d22_0x0016 Table 12: ENABLE STATE MACHINE: Calibration Control
ensm_state	uchar	-	-	Volatile	-	-	reg_addr_d23_0x0017 Table 12: ENABLE STATE MACHINE: State
auxdac_1_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d24_0x0018 Table 15: AUXDAC: AuxDAC 1 Word
auxdac_2_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d25_0x0019 Table 15: AUXDAC: AuxDAC 2 Word
auxdac_1_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d26_0x001a Table 15: AUXDAC: AuxDAC 1 Config
auxdac_2_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d27_0x001b Table 15: AUXDAC: AuxDAC 2 Config
auxadc_clock_divider	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d28_0x001c Table 17: AUXILARYADC: AuxADC Clock Divider

auxadc_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d29_0x001d Table 17: AUXILARYADC: Aux ADC Config
auxadc_word_msb	uchar	-	-	Volatile	-	-	reg_addr_d30_0x001e Table 17: AUXILARYADC: AuxADC Word MSB
auxadc_world_lsb	uchar	-	-	Volatile	-	-	reg_addr_d31_0x001f Table 17: AUXILARYADC: AuxADC Word LSB
misc_auto_gpo	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d32_0x0020 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: Auto GPO
misc_agc_gain_lock_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d33_0x0021 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AGC Gain Lock Delay
misc_agc_attack_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d34_0x0022 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AGC Attack Delay
misc_auxdac_enable_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d35_0x0023 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC Enable Control
misc_rx_load_synth_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d36_0x0024 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: RX Load Synth Delay
misc_tx_load_synth_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d37_0x0025 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: TX Load Synth Delay
misc_external_lna_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d38_0x0026 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: External LNA control
misc_gpo_force_and_init	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d39_0x0027 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO Force and Init
misc_gpo0_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d40_0x0028 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO0 Rx delay
misc_gpo1_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d41_0x0029 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO1 Rx delay
misc_gpo2_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d42_0x002a Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO2 Rx delay
misc_gpo3_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d43_0x002b Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO3 Rx delay
misc_gpo0_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d44_0x002c Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO0 Tx Delay

misc_gpo1_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d45_0x002d Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO1 Tx Delay
misc_gpo2_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d46_0x002e Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO2 Tx Delay
misc_gpo3_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d47_0x002f Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO3 Tx Delay
misc_auxdac1_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d48_0x0030 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC1 Rx Delay
misc_auxdac1_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d49_0x0031 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC1 Tx Delay
misc_auxdac2_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d50_0x0032 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC2 Rx Delay
misc_auxdac2_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d51_0x0033 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC2 Tx Delay
ocpi_pad_034	uchar	-	-		-	-	-
ctrl_output_pointer	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d53_0x0035 Table 19: CONTROL OUTPUT: Control Output Pointer
ctrl_output_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d54_0x0036 Table 19: CONTROL OUTPUT: Control Output Enable
product_id	uchar	-	-	Volatile	-	-	reg_addr_d55_0x0037 Table 20: PRODUCT ID: Product ID
ocpi_pad_038	uchar	-	-		-	-	-
reference_clock_cycles	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d58_0x003a Table 22: REFERENCE CLOCK CYCLES: Reference Clock Cycles
digital_io_digital_io_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d59_0x003b Table 23: DIGITAL IO CONTROL: Digital I/O Control
digital_io_lvds_bias_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d60_0x003c Table 23: DIGITAL IO CONTROL: LVDS Bias control
digital_io_lvds_invert_ctrl1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d61_0x003d Table 23: DIGITAL IO CONTROL: LVDS Invert control1
digital_io_lvds_invert_ctrl2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d62_0x003e Table 23: DIGITAL IO CONTROL: LVDS Invert control2
bbpll_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d63_0x003f Table 25: BB-PLL CONTROL: BPLL Control 1
bbpll_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d64_0x0040 Table 25: BB-PLL CONTROL: Must be 0
bbpll_fract_bb_freq_word_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d65_0x0041 Table 25: BB-PLL CONTROL: Fractional BB Freq Word 1

bbpll_fract_bb_freq_word_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d66_0x0042 Table 25: BBPLL CONTROL: Fractional BB Freq Word 2
bbpll_fract_bb_freq_word_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d67_0x0043 Table 25: BBPLL CONTROL: Fractional BB Freq Word 3
bbpll_integer_bb_freq_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d68_0x0044 Table 25: BBPLL CONTROL: Integer BB Freq Word
bbpll_ref_clock_scaler	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d69_0x0045 Table 25: BBPLL CONTROL: Ref Clock Scaler
bbpll_cp_current	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d70_0x0046 Table 25: BBPLL CONTROL: CP Current
bbpll_msc_scale	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d71_0x0047 Table 25: BBPLL CONTROL: MSC Scale
bbpll_loop_filter_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d72_0x0048 Table 25: BBPLL CONTROL: Loop Filter 1
bbpll_loop_filter_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d73_0x0049 Table 25: BBPLL CONTROL: Loop Filter 2
bbpll_loop_filter_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d74_0x004a Table 25: BBPLL CONTROL: Loop Filter 3
bbpll_vco_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d75_0x004b Table 25: BBPLL CONTROL: VCO Control
bbpll_mustbe0x86	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d76_0x004c Table 25: BBPLL CONTROL: Must be_0x86
bpll_control_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d77_0x004d Table 25: BBPLL CONTROL: BPLL Control 2
bpll_control_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d78_0x004e Table 25: BBPLL CONTROL: BPLL Control 3
ocpi_pad_04f	uchar	-	-		-	-	-
power_down_override_rx_synth	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d80_0x0050 Table 26: POWER DOWN OVERRIDE: Rx Synth Power Down Override
power_down_override_tx_synth	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d81_0x0051 Table 26: POWER DOWN OVERRIDE: TX Synth Power Down Override
power_down_override_rx_control_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d82_0x0052 Table 26: POWER DOWN OVERRIDE: Control 0
power_down_override_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d83_0x0053 Table 26: POWER DOWN OVERRIDE: Must be 0
power_down_override_rx1_adc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d84_0x0054 Table 26: POWER DOWN OVERRIDE: Rx1 ADC Power Down Override
power_down_override_rx2_adc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d85_0x0055 Table 26: POWER DOWN OVERRIDE: Rx2 ADC Power Down Override
power_down_override_tx_analog	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d86_0x0056 Table 26: POWER DOWN OVERRIDE: Tx Analog Power Down Override 1
power_down_override_analog	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d87_0x0057 Table 26: POWER DOWN OVERRIDE: Analog Power Down Override
power_down_override_misc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d88_0x0058 Table 26: POWER DOWN OVERRIDE: Misc Power Down Override
ocpi_pad_059	uchar	-	-		-	-	-
overflow_ch_1	uchar	-	-	Volatile	-	-	reg_addr_d94_0x005e Table 27: OVERFLOW: CH 1 Overflow

overflow_ch_2	uchar	-	-	Volatile	-	-	reg_addr_d95_0x005f Table 27: OVERFLOW: CH 2 Overflow
tx_filter_coef_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d96_0x0060 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Address
tx_filter_coef_write_data_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d97_0x0061 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Write Data 1
tx_filter_coef_write_data_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d98_0x0062 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Write Data 2
tx_filter_coef_read_data_1	uchar	-	-	Volatile	-	-	reg_addr_d99_0x0063 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Read Data 1
tx_filter_coef_read_data_2	uchar	-	-	Volatile	-	-	reg_addr_d100_0x0064 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Read Data 2
tx_filter_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d101_0x0065 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Configuration
ocpi_pad_066	uchar	-	-		-	-	-
tx_mon_low_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d103_0x0067 Table 29: Tx MONITOR: Tx Mon Low Gain
tx_mon_high_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d104_0x0068 Table 29: Tx MONITOR: Tx Mon High Gain
tx_mon_delay_counter	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d105_0x0069 Table 29: Tx MONITOR: Tx Mon Delay Counter
tx_mon_level_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d106_0x006a Table 29: Tx MONITOR: Tx Level Threshold
tx_mon_rssi1	uchar	-	-	Volatile	-	-	reg_addr_d107_0x006b Table 29: Tx MONITOR: TX RSSI1
tx_mon_rssi2	uchar	-	-	Volatile	-	-	reg_addr_d108_0x006c Table 29: Tx MONITOR: TX RSSI2
tx_mon_rssi_lsb	uchar	-	-	Volatile	-	-	reg_addr_d109_0x006d Table 29: Tx MONITOR: TX RSSI LSB
tx_mon_tpm_mode_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d110_0x006e Table 29: Tx MONITOR: TPM Mode Enable
tx_mon_temp_gain_coef	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d111_0x006f Table 29: Tx MONITOR: Temp Gain Coefficient
tx_mon_1_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d112_0x0070 Table 29: Tx MONITOR: Tx Mon 1 Config
tx_mon_2_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d113_0x0071 Table 29: Tx MONITOR: Tx Mon 2 Config
ocpi_pad_072	uchar	-	-		-	-	-
tx_pwr_atten_tx1_atten_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d115_0x0073 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx1 Atten 0
tx_pwr_atten_tx1_atten_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d116_0x0074 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx1 Atten 1
tx_pwr_atten_tx2_atten_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d117_0x0075 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx2 Atten 0
tx_pwr_atten_tx2_atten_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d118_0x0076 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx2 Atten 1
tx_pwr_atten_tx_atten_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d119_0x0077 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx Atten Offset

tx_pwr_atten_tx_atten_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d120_0x0078 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx Atten Threshold
tx_pwr_atten_set_tx1_tx2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d121_0x0079 Table 31: Tx POWER CONTROL AND ATTENUATION: Set Tx1/Tx2
ocpi_pad_07a	uchar	-	-		-	-	-
tx_pwr_atten_immediate_update	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d124_0x007c Table 31: Tx POWER CONTROL AND ATTENUATION: Immediate Update
ocpi_pad_07d	uchar	-	-		-	-	-
tx_pgo_phase_corr_tx1_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d142_0x008e Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Phase Corr
tx_pgo_gain_corr_tx1_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d143_0x008f Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Gain Corr
tx_pgo_phase_corr_tx2_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d144_0x0090 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Phase Corr
tx_pgo_gain_corr_tx2_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d145_0x0091 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Gain Corr
tx_pgo_offset_corr_tx1_out1_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d146_0x0092 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Offset I
tx_pgo_offset_corr_tx1_out1_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d147_0x0093 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Offset Q
tx_pgo_offset_corr_tx2_out1_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d148_0x0094 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Offset I
tx_pgo_offset_corr_tx2_out1_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d149_0x0095 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Offset Q
tx_pgo_phase_corr_tx1_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d150_0x0096 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Phase Corr
tx_pgo_gain_corr_tx1_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d151_0x0097 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Gain Corr

tx_pgo_phase_corr_tx2_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d152_0x0098 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Phase Corr
tx_pgo_gain_corr_tx2_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d153_0x0099 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Gain Corr
tx_pgo_offset_corr_tx1_out2_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d154_0x009a Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Offset I
tx_pgo_offset_corr_tx1_out2_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d155_0x009b Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Offset Q
tx_pgo_offset_corr_tx2_out2_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d156_0x009c Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Offset I
tx_pgo_offset_corr_tx2_out2_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d157_0x009d Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Offset Q
ocpi_pad_09e	uchar	-	-		-	-	-
tx_quad_cal_pgo_force_bits	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d159_0x009f Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Force Bits
tx_quad_cal_nco_freq_phase_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d160_0x00a0 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad Cal NCO Freq & Phase Offset
tx_quad_cal_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d161_0x00a1 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad Cal Control
tx_quad_cal_kexp_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d162_0x00a2 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Kexp 1
tx_quad_cal_kexp_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d163_0x00a3 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Kexp 2
tx_quad_cal_settle_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d164_0x00a4 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: QUAD Settle count
tx_quad_cal_mag_ftest_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d165_0x00a5 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Mag. Ftest Thresh
tx_quad_cal_mag_ftest_thresh_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d166_0x00a6 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Mag. Ftest Thresh 2

tx_quad_cal_status_tx1	uchar	-	-	Volatile	-	-	reg_addr_d167_0x00a7 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal status Tx1
tx_quad_cal_status_tx2	uchar	-	-	Volatile	-	-	reg_addr_d168_0x00a8 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal status Tx2
tx_quad_cal_count	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d169_0x00a9 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal Count
tx_quad_cal_full_lmt_gain	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d170_0x00aa Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Tx Quad Full/LMT Gain
tx_quad_cal_squarer_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d171_0x00ab Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Squarer Config
tx_quad_cal_atten	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d172_0x00ac Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: TX Quad Cal Atten
tx_quad_cal_thresh_accum	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d173_0x00ad Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Thresh Accum
tx_quad_cal_lpf_gain	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d174_0x00ae Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Tx Quad LPF Gain
ocpi_pad_0af	uchar	-	-		-	-	-
tx_bbf_r1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d194_0x00c2 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R1
tx_bbf_r2	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d195_0x00c3 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R2
tx_bbf_r3	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d196_0x00c4 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R3
tx_bbf_r4	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d197_0x00c5 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R4
tx_bbf_rp	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d198_0x00c6 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF RP
tx_bbf_c1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d199_0x00c7 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF C1
tx_bbf_c2	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d200_0x00c8 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF C2
tx_bbf_cp	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d201_0x00c9 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF CP
tx_bbf_tuner_pd	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d202_0x00ca Table 34: Tx BASEBAND FILTER REGISTERS: Tx Tuner PD
tx_bbf_r2b	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d203_0x00cb Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R2b

ocpi_pad_0cc	uchar	-	-		-	-	-
tx_secondf_config0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d208_0x00d0 Table 35: Tx SECONDARY FILTER REGISTERS: Config0
tx_secondf_resistor	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d209_0x00d1 Table 35: Tx SECONDARY FILTER REGISTERS: Resistor
tx_secondf_capacitor	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d210_0x00d2 Table 35: Tx SECONDARY FILTER REGISTERS: Capacitor
tx_secondf_mustbe0x60	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d211_0x00d3 Table 35: Tx SECONDARY FILTER REGISTERS: Must be 0x60
ocpi_pad_0d4	uchar	-	-		-	-	-
tx_bbf_tune_divider	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d214_0x00d6 Table 38: Tx BBF TUNER CONFIGURATION: TX BBF Tune Divider
tx_bbf_tune_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d215_0x00d7 Table 38: Tx BBF TUNER CONFIGURATION: TX BBF Tune Mode
ocpi_pad_0d8	uchar	-	-		-	-	-
rx_filter_coef_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d240_0x00f0 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Addr
rx_filter_coef_write_data_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d241_0x00f1 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Data 1
rx_filter_coef_write_data_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d242_0x00f2 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Data 2
rx_filter_coef_read_data_1	uchar	-	-	Volatile	-	-	reg_addr_d243_0x00f3 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Read Data 1
rx_filter_coef_read_data_2	uchar	-	-	Volatile	-	-	reg_addr_d244_0x00f4 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Read Data 2
rx_filter_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d245_0x00f5 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Configuration
rx_filter_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d246_0x00f6 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Gain
ocpi_pad_0f7	uchar	-	-		-	-	-
gain_agc_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d250_0x00fa Table 42: GAIN CONTROL SETUP: AGC Config1
gain_agc_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d251_0x00fb Table 42: GAIN CONTROL SETUP: AGC config2
gain_agc_config_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d252_0x00fc Table 42: GAIN CONTROL SETUP: AGC Config3
gain_max_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d253_0x00fd Table 42: GAIN CONTROL SETUP: Max LMT/Full Gain
gain_peak_wait_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d254_0x00fe Table 42: GAIN CONTROL SETUP: Peak Wait Time
ocpi_pad_0ff	uchar	-	-		-	-	-

gain_digital_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d256_0x0100 Table 42: GAIN CONTROL SETUP: Digital Gain
gain_agc_lock_level	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d257_0x0101 Table 42: GAIN CONTROL SETUP: AGC Lock Level
ocpi_pad_102	uchar	-	-		-	-	-
gain_gain_stp_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d259_0x0103 Table 42: GAIN CONTROL SETUP: Gain Step Config 1
gain_adc_small_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d260_0x0104 Table 42: GAIN CONTROL SETUP: ADC Small Overload Threshold
gain_adc_large_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d261_0x0105 Table 42: GAIN CONTROL SETUP: ADC Large Overload Threshold
gain_stp_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d262_0x0106 Table 42: GAIN CONTROL SETUP: Gain Step Config 2
gain_small_lmt_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d263_0x0107 Table 42: GAIN CONTROL SETUP: Small LMT Overload Threshold
gain_large_lmt_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d264_0x0108 Table 42: GAIN CONTROL SETUP: Large LMT Overload Threshold
gain_rx1_manual_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d265_0x0109 Table 42: GAIN CONTROL SETUP: Rx1 Manual LMT/Full Gain
gain_rx1_manual_lpf_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d266_0x010a Table 42: GAIN CONTROL SETUP: Rx1 Manual LPF gain
gain_rx1_manual_digitalforced_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d267_0x010b Table 42: GAIN CONTROL SETUP: Rx1 Manual Digital/Forced Gain
gain_rx2_manual_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d268_0x010c Table 42: GAIN CONTROL SETUP: Rx2 Manual LMT/Full Gain
gain_rx2_manual_lpf_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d269_0x010d Table 42: GAIN CONTROL SETUP: Rx2 Manual LPF Gain
gain_rx2_manual_digitalforced_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d270_0x010e Table 42: GAIN CONTROL SETUP: Rx2 Manual Digital/Forced Gain
ocpi_pad_10f	uchar	-	-		-	-	-
fast_agc_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d272_0x0110 Table 44: FAST ATTACK AGC SETUP: Config 1
fast_agc_config_2_settling_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d273_0x0111 Table 44: FAST ATTACK AGC SETUP: Config 2 & Settling Delay
fast_agc_energy_lost_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d274_0x0112 Table 44: FAST ATTACK AGC SETUP: Energy Lost Threshold
fast_agc_stronger_signal_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d275_0x0113 Table 44: FAST ATTACK AGC SETUP: Stronger Signal Threshold
fast_agc_low_power_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d276_0x0114 Table 44: FAST ATTACK AGC SETUP: Low Power Threshold

fast_agc_strong_signal_freeze	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d277_0x0115 Table 44: FAST ATTACK AGC SETUP: Strong Signal Freeze
fast_agc_final_over_range_and_opt_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d278_0x0116 Table 44: FAST ATTACK AGC SETUP: Final Over Range and Opt Gain
fast_agc_energy_detect_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d279_0x0117 Table 44: FAST ATTACK AGC SETUP: Energy Detect Count
fast_agc_agcll_upper_limit	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d280_0x0118 Table 44: FAST ATTACK AGC SETUP: AGCLL Upper Limit
fast_agc_gain_lock_exit_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d281_0x0119 Table 44: FAST ATTACK AGC SETUP: Gain Lock Exit Count
fast_agc_initial_lmt_gain_limit	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d282_0x011a Table 44: FAST ATTACK AGC SETUP: Initial LMT Gain Limit
fast_agc_increment_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d283_0x011b Table 44: FAST ATTACK AGC SETUP: Increment Time
ocpi_pad_11c	uchar	-	-		-	-	-
slowhybrid_agc_inner_low_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d288_0x0120 Table 45: SLOW ATTACK AND HYBRID AGC: AGC Inner Low Threshold
slowhybrid_agc_lmt_overload_counters	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d289_0x0121 Table 45: SLOW ATTACK AND HYBRID AGC: LMT Overload Counters
slowhybrid_agc_adc_overload_counters	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d290_0x0122 Table 45: SLOW ATTACK AND HYBRID AGC: ADC Overload Counters
slowhybrid_agc_gain_stp1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d291_0x0123 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Step1
slowhybrid_agc_gain_update_counter1	uchar	-	-	Volatile	-	-	reg_addr_d292_0x0124 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Update Counter1
slowhybrid_agc_gain_update_counter2	uchar	-	-	Volatile	-	-	reg_addr_d293_0x0125 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Update Counter2
ocpi_pad_126	uchar	-	-		-	-	-
slowhybrid_agc_digital_sat_counter	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d296_0x0128 Table 45: SLOW ATTACK AND HYBRID AGC: Digital Sat Counter
slowhybrid_agc_outer_power_threshs	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d297_0x0129 Table 45: SLOW ATTACK AND HYBRID AGC: Outer Power Thresholds
slowhybrid_agc_gain_stp_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d298_0x012a Table 45: SLOW ATTACK AND HYBRID AGC: Gain Step 2
ocpi_pad_12b	uchar	-	-		-	-	-
ext_lna_high_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d300_0x012c Table 46: EXTERNAL LNA GAIN WORD: Ext LNA High Gain
ext_lna_low_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d301_0x012d Table 46: EXTERNAL LNA GAIN WORD: Ext LNA Low Gain
ocpi_pad_12e	uchar	-	-		-	-	-

gain_table	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d304_0x0130 Table 47: AGC GAIN TABLE: Gain Table Address
gain_table_write_data1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d305_0x0131 Table 47: AGC GAIN TABLE: Gain Table Write Data1
gain_table_write_data2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d306_0x0132 Table 47: AGC GAIN TABLE: Gain Table Write Data2
gain_table_write_data3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d307_0x0133 Table 47: AGC GAIN TABLE: Gain Table Write Data 3
gain_table_read_data1	uchar	-	-	Volatile	-	-	reg_addr_d308_0x0134 Table 47: AGC GAIN TABLE: Gain Table Read Data 1
gain_table_read_data2	uchar	-	-	Volatile	-	-	reg_addr_d309_0x0135 Table 47: AGC GAIN TABLE: Gain Table Read Data 2
gain_table_read_data3	uchar	-	-	Volatile	-	-	reg_addr_d310_0x0136 Table 47: AGC GAIN TABLE: Gain Table Read Data 3
gain_table_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d311_0x0137 Table 47: AGC GAIN TABLE: Gain Table Config
mixer_subtable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d312_0x0138 Table 48: MIXER SUBTABLE: Mixer Subtable Address
mixer_subtable_gain_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d313_0x0139 Table 48: MIXER SUBTABLE: Mixer Subtable Gain Word Write
mixer_subtable_bias_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d314_0x013a Table 48: MIXER SUBTABLE: Mixer Subtable Bias Word Write
mixer_subtable_ctrl_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d315_0x013b Table 48: MIXER SUBTABLE: Mixer Subtable Control Word Write
mixer_subtable_gain_read	uchar	-	-	Volatile	-	-	reg_addr_d316_0x013c Table 48: MIXER SUBTABLE: Mixer Subtable Gain Word Read
mixer_subtable_bias_read	uchar	-	-	Volatile	-	-	reg_addr_d317_0x013d Table 48: MIXER SUBTABLE: Mixer Subtable Bias Word Read
mixer_subtable_ctrl_read	uchar	-	-	Volatile	-	-	reg_addr_d318_0x013e Table 48: MIXER SUBTABLE: Mixer Subtable Control Word Read
mixer_subtable_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d319_0x013f Table 48: MIXER SUBTABLE: Mixer Subtable Config
calib_gain_table_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d320_0x0140 Table 49: CALIBRATION GAIN TABLE: Word_Address
calib_gain_table_diff_worderror_write	uchar	-	-	Writeable	-	-	reg_addr_d321_0x0141 Table 49: CALIBRATION GAIN TABLE: Gain Diff Word/Error Write
calib_gain_table_gain_error_read	uchar	-	-	Volatile	-	-	reg_addr_d322_0x0142 Table 49: CALIBRATION GAIN TABLE: Gain Error Read
calib_gain_table_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d323_0x0143 Table 49: CALIBRATION GAIN TABLE: Config

calib_gain_table_lna_diff_read_back	uchar	-	-	Volatile	-	-	reg_addr_d324_0x0144 Table 49: CALIBRATION GAIN TABLE: LNA Gain Diff Read Back
gen_calib_max_mixer_gain_index	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d325_0x0145 Table 50: GENERAL CALIBRATION: Max Mixer Calibration Gain Index
gen_calib_temp_gain_coef	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d326_0x0146 Table 50: GENERAL CALIBRATION: Temp Gain Coefficient
gen_calib_settle_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d327_0x0147 Table 50: GENERAL CALIBRATION: Settle Time
gen_calib_measure_duration	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d328_0x0148 Table 50: GENERAL CALIBRATION: Measure Duration
gen_calib_cal_temp_sensor_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d329_0x0149 Table 50: GENERAL CALIBRATION: Cal Temp sensor word
ocpi_pad_14a	uchar	-	-		-	-	-
rssi_measure_duration_01	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d336_0x0150 Table 51: RSSI MEASUREMENT CONFIGURATION: Measure Duration 0,1
rssi_measure_duration_23	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d337_0x0151 Table 51: RSSI MEASUREMENT CONFIGURATION: Measure Duration 2,3
rssi_weight_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d338_0x0152 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 0
rssi_weight_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d339_0x0153 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 1
rssi_weight_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d340_0x0154 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 2
rssi_weight_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d341_0x0155 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 3
rssi_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d342_0x0156 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI delay
rssi_wait_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d343_0x0157 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI wait time
rssi_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d344_0x0158 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Config
ocpi_pad_159	uchar	-	-		-	-	-
rssi_dec_power_duration_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d348_0x015c Table 51: RSSI MEASUREMENT CONFIGURATION: Dec Power Duration
rssi_lna_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d349_0x015d Table 51: RSSI MEASUREMENT CONFIGURATION: LNA Gain
ocpi_pad_15e	uchar	-	-		-	-	-
power_ch1_rx_filter_power	uchar	-	-	Volatile	-	-	reg_addr_d353_0x0161 Table 53: POWER WORD: CH1 Rx filter Power
ocpi_pad_162	uchar	-	-		-	-	-

power_ch2_rx_filter_power	uchar	-	-	Volatile	-	-	reg_addr_d355_0x0163 Table 53: POWER WORD: CH2 Rx filter Power
ocpi_pad_164	uchar	-	-		-	-	-
calibration_config_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d361_0x0169 Table 54: Rx QUADRATURE CALIBRATION: Calibration Config 1
calibration_mustbe0x75	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d362_0x016a Table 54: Rx QUADRATURE CALIBRATION: Must be 0x75
calibration_mustbe0x95	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d363_0x016b Table 54: Rx QUADRATURE CALIBRATION: Must be 0x95
ocpi_pad_16c	uchar	-	-		-	-	-
rx_pgo_phase_corr_rx1_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d368_0x0170 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Phase Corr
rx_pgo_gain_corr_rx1_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d369_0x0171 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Gain Corr
rx_pgo_phase_corr_rx2_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d370_0x0172 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Phase Corr
rx_pgo_gain_corr_rx2_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d371_0x0173 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Gain Corr
rx_pgo_offset_corr_rx1_ina_q	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d372_0x0174 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Q Offset
rx_pgo_offset_corr_rx1_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d373_0x0175 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Offset
rx_pgo_offset_corr_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d374_0x0176 Table 55: Rx PHASE AND GAIN CORRECTION: Input A Offsets
rx_pgo_offset_corr_rx2_ina	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d375_0x0177 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Offset
rx_pgo_offset_corr_rx2_ina_i	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d376_0x0178 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A I Offset
rx_pgo_phase_corr_rx1_inbc	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d377_0x0179 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Phase Corr
rx_pgo_gain_corr_rx1_inbc	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d378_0x017a Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Gain Corr
rx_pgo_phase_corr_rx2_inbc	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d379_0x017b Table 55: Rx PHASE AND GAIN CORRECTION: Rx2B/C Phase Corr
rx_pgo_gain_corr_rx2_inbc	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d380_0x017c Table 55: Rx PHASE AND GAIN CORRECTION: Rx2B/C Gain Corr
rx_pgo_offset_corr_rx1_inbc_q	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d381_0x017d Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Q Offset
rx_pgo_offset_corr_rx1_inbc_i	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d382_0x017e Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C I Offset

rx_pgo_offset_corr_inpbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d383_0x017f Table 55: Rx PHASE AND GAIN CORRECTION: Input B/C Offsets
rx_pgo_offset_corr_rx2_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d384_0x0180 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2 B/C Offset
rx_pgo_offset_corr_rx2_inbc_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d385_0x0181 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2 B/C I Offset
rx_pgo_force_bits	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d386_0x0182 Table 55: Rx PHASE AND GAIN CORRECTION: Force Bits
ocpi_pad_183	uchar	-	-		-	-	-
rx_dc_offset_wait_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d389_0x0185 Table 56: Rx DC OFFSET CONTROL: Wait Count
rx_dc_offset_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d390_0x0186 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Count
rx_dc_offset_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d391_0x0187 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Config 1
rx_dc_offset_atten	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d392_0x0188 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Attenuation
rx_dc_offset_mustbe0x30	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d393_0x0189 Table 56: Rx DC OFFSET CONTROL: Must be 0x30
ocpi_pad_18a	uchar	-	-		-	-	-
rx_dc_offset_config2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d395_0x018b Table 56: Rx DC OFFSET CONTROL: DC Offset Config2
rx_dc_offset_rf_cal_gain_index	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d396_0x018c Table 56: Rx DC OFFSET CONTROL: RF Cal Gain Index
rx_dc_offset_soi_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d397_0x018d Table 56: Rx DC OFFSET CONTROL: SOI Threshold
ocpi_pad_18e	uchar	-	-		-	-	-
rx_dc_offset_bb_shift	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d400_0x0190 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Shift
rx_dc_offset_bb_fast_settle_shift	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d401_0x0191 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Fast Settle Shift
rx_dc_offset_bb_fast_settle_dur	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d402_0x0192 Table 56: Rx DC OFFSET CONTROL: BB Fast Settle Dur
rx_dc_offset_bb_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d403_0x0193 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Count
rx_dc_offset_bb_atten	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d404_0x0194 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Attenuation
ocpi_pad_195	uchar	-	-		-	-	-
rx_bb_dc_offset_rx1_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d410_0x019a Table 60: Rx BB DC OFFSET: RX1 BB DC word I MSB

rx_bb_dc_offset_rx1_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d411_0x019b Table 60: Rx BB DC OFFSET: RX1 BB DC word I LSB
rx_bb_dc_offset_rx1_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d412_0x019c Table 60: Rx BB DC OFFSET: RX1 BB DC word Q MSB
rx_bb_dc_offset_rx1_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d413_0x019d Table 60: Rx BB DC OFFSET: RX1 BB DC word Q LSB
rx_bb_dc_offset_rx2_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d414_0x019e Table 60: Rx BB DC OFFSET: RX2 BB DC word I MSB
rx_bb_dc_offset_rx2_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d415_0x019f Table 60: Rx BB DC OFFSET: RX2 BB DC word I LSB
rx_bb_dc_offset_rx2_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d416_0x01a0 Table 60: Rx BB DC OFFSET: RX2 BB DC word Q MSB
rx_bb_dc_offset_rx2_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d417_0x01a1 Table 60: Rx BB DC OFFSET: RX2 BB DC word Q LSB
rx_bb_dc_offset_track_corr_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d418_0x01a2 Table 60: Rx BB DC OFFSET: BB Track corr word I MSB
rx_bb_dc_offset_track_corr_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d419_0x01a3 Table 60: Rx BB DC OFFSET: BB Track corr word I LSB
rx_bb_dc_offset_track_corr_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d420_0x01a4 Table 60: Rx BB DC OFFSET: BB Track corr word Q MSB
rx_bb_dc_offset_track_corr_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d421_0x01a5 Table 60: Rx BB DC OFFSET: BB Track corr word Q LSB
ocpi_pad_1a6	uchar	-	-		-	-	-
rssi_readback_rx1_symbol	uchar	-	-	Volatile	-	-	reg_addr_d423_0x01a7 Table 61: RSSI READBACK: Rx1 RSSI Symbol
rssi_readback_rx1_preamble	uchar	-	-	Volatile	-	-	reg_addr_d424_0x01a8 Table 61: RSSI READBACK: Rx1 RSSI preamble
rssi_readback_rx2_symbol	uchar	-	-	Volatile	-	-	reg_addr_d425_0x01a9 Table 61: RSSI READBACK: Rx2 RSSI symbol
rssi_readback_rx2_preamble	uchar	-	-	Volatile	-	-	reg_addr_d426_0x01aa Table 61: RSSI READBACK: Rx2 RSSI preamble
rssi_readback_symbol_lsb	uchar	-	-	Volatile	-	-	reg_addr_d427_0x01ab Table 61: RSSI READBACK: Symbol LSB
rssi_readback_preamble_lsb	uchar	-	-	Volatile	-	-	reg_addr_d428_0x01ac Table 61: RSSI READBACK: Preamble LSB
ocpi_pad_1ad	uchar	-	-		-	-	-
rx_tia_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d475_0x01db Table 62: Rx TIA: Rx TIA Config
rx_tia_1_c_lsb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d476_0x01dc Table 62: Rx TIA: TIA1 C LSB
rx_tia_1_c_msb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d477_0x01dd Table 62: Rx TIA: TIA1 C MSB
rx_tia_2_c_lsb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d478_0x01de Table 62: Rx TIA: TIA2 C LSB

rx_tia_2_c_msb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d479_0x01df Table 62: Rx TIA: TIA2 C MSB
rx_bbf_rx1_r1a	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d480_0x01e0 Table 65: Rx BFF: Rx1 BBF R1A
rx_bbf_rx2_r1a	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d481_0x01e1 Table 65: Rx BFF: Rx2 BBF R1A
rx_bff_rx1_tune_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d482_0x01e2 Table 65: Rx BFF: Rx1 Tune Control
rx_bff_rx2_tune_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d483_0x01e3 Table 65: Rx BFF: Rx2 Tune Control
rx_bff_rx1_bbf_r5	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d484_0x01e4 Table 65: Rx BFF: Rx1 BBF R5
rx_bff_rx2_bbf_r5	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d485_0x01e5 Table 65: Rx BFF: Rx2 BBF R5
rx_bbf_r2346	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d486_0x01e6 Table 65: Rx BFF: Rx BBF R2346
rx_bbf_c1_msb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d487_0x01e7 Table 65: Rx BFF: Rx BBF C1 MSB
rx_bbf_c1_lsb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d488_0x01e8 Table 65: Rx BFF: Rx BBF C1 LSB
rx_bbf_c2_msb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d489_0x01e9 Table 65: Rx BFF: Rx BBF C2 MSB
rx_bbf_c2_lsb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d490_0x01ea Table 65: Rx BFF: Rx BBF C2 LSB
rx_bbf_c3_msb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d491_0x01eb Table 65: Rx BFF: Rx BBF C3 MSB
rx_bbf_c3_lsb	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d492_0x01ec Table 65: Rx BFF: Rx BBF C3 LSB
rx_bbf_cc1_ctr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d493_0x01ed Table 65: Rx BFF: Rx BBF CC1 Ctr
rx_bbf_mustbe0x60	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d494_0x01ee Table 65: Rx BFF: Must be 0x60
rx_bbf_cc2_ctr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d495_0x01ef Table 65: Rx BFF: Rx BBF CC2 Ctr
rx_bbf_pow_rz_byte1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d496_0x01f0 Table 65: Rx BFF: Rx BBF Pow Rz Byte1
rx_bbf_cc3_ctr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d497_0x01f1 Table 65: Rx BFF: Rx BBF CC3 Ctr
rx_bbf_r5_tune	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d498_0x01f2 Table 65: Rx BFF: Rx BBF R5 Tune
rx_bbf_tune	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d499_0x01f3 Table 65: Rx BFF: Rx BBF Tune
rx_bff_rx1_bbf_man_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d500_0x01f4 Table 65: Rx BFF: Rx1 BBF Man Gain
rx_bff_rx2_bbf_man_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d501_0x01f5 Table 65: Rx BFF: Rx2 BBF Man Gain
ocpi_pad_1f6	uchar	-	-		-	-	-
rx_bbf_tune_config_divide	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d504_0x01f8 Table 66: Rx BBF TUNER CONFIGURATION: RX BBF Tune Divide
rx_bbf_tune_config_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d505_0x01f9 Table 66: Rx BBF TUNER CONFIGURATION: RX BBF Tune Config
rx_bbf_tune_config_mustbe0x01	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d506_0x01fa Table 66: Rx BBF TUNER CONFIGURATION: Must be 0x01
rx_bbf_tune_config_rx_bbbw_mhz	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d507_0x01fb Table 66: Rx BBF TUNER CONFIGURATION: Rx BBBW MHz

rx_bbf_tune_config_rx_bbbw_khz	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d508_0x01fc Table 66: Rx BBF TUNER CONFIGURATION: Rx BBBW kHz
ocpi_pad_1fd	uchar	-	-		-	-	-
rx_synth_disable_vco_cal	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d560_0x0230 Table 67: Rx SYNTHESIZER: Disable VCO Cal
rx_synth_integer_byte_0	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d561_0x0231 Table 67: Rx SYNTHESIZER: RX Integer Byte 0
rx_synth_integer_byte_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d562_0x0232 Table 67: Rx SYNTHESIZER: RX Integer Byte 1
rx_synth_fract_byte_0	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d563_0x0233 Table 67: Rx SYNTHESIZER: RX Fractional Byte 0
rx_synth_fract_byte_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d564_0x0234 Table 67: Rx SYNTHESIZER: RX Fractional Byte 1
rx_synth_fract_byte_2	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d565_0x0235 Table 67: Rx SYNTHESIZER: RX Fractional Byte 2
rx_synth_force_alc	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d566_0x0236 Table 67: Rx SYNTHESIZER: RX Force ALC
rx_synth_force_vco_tune_0	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d567_0x0237 Table 67: Rx SYNTHESIZER: RX Force VCO Tune 0
rx_synth_force_vco_tune_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d568_0x0238 Table 67: Rx SYNTHESIZER: RX Force VCO Tune 1
rx_synth_alc_varactor	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d569_0x0239 Table 67: Rx SYNTHESIZER: RX ALC/Varactor
rx_synth_vco_output	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d570_0x023a Table 67: Rx SYNTHESIZER: RX VCO Output
rx_synth_cp_current	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d571_0x023b Table 67: Rx SYNTHESIZER: RX CP Current
rx_synth_cp_offset	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d572_0x023c Table 67: Rx SYNTHESIZER: RX CP Offset
rx_synth_cp_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d573_0x023d Table 67: Rx SYNTHESIZER: RX CP Config
rx_synth_loop_filter_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d574_0x023e Table 67: Rx SYNTHESIZER: RX Loop Filter 1
rx_synth_loop_filter_2	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d575_0x023f Table 67: Rx SYNTHESIZER: RX Loop Filter 2
rx_synth_loop_filter_3	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d576_0x0240 Table 67: Rx SYNTHESIZER: RX Loop Filter 3
rx_synth_dithercp_cal	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d577_0x0241 Table 67: Rx SYNTHESIZER: RX Dither/CP Cal
rx_synth_vco_bias_1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d578_0x0242 Table 67: Rx SYNTHESIZER: RX VCO Bias 1
rx_synth_mustbe0x0d	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d579_0x0243 Table 67: Rx SYNTHESIZER: Must be 0x0D
rx_synth_cal_status	uchar	-	-	Volatile	-	-	reg_addr_d580_0x0244 Table 67: Rx SYNTHESIZER: RX Cal Status
rx_synth_mustbe0x00	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d581_0x0245 Table 67: Rx SYNTHESIZER: Must be 0x00
rx_synth_mustbe0x02	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d582_0x0246 Table 67: Rx SYNTHESIZER: Set to 0x02 (Must be 0x02)
rx_synth_cp_ovrg_vco_lock	uchar	-	-	Volatile	-	-	reg_addr_d583_0x0247 Table 67: Rx SYNTHESIZER: RX CP Ovrg/VCO Lock

rx_synth_mustbe0x0b	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d584_0x0248 Table 67: Rx SYNTHESIZER: Set to 0x0B (Must be 0x0B)
rx_synth_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d585_0x0249 Table 67: Rx SYNTHESIZER: RX VCO Cal
rx_synth_lock_detect_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d586_0x024a Table 67: Rx SYNTHESIZER: RX Lock Detect Config
rx_synth_mustbe0x17	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d587_0x024b Table 67: Rx SYNTHESIZER: Must be 0x17
rx_synth_mustbe0x00_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d588_0x024c Table 67: Rx SYNTHESIZER: Must be 0x00
rx_synth_mustbe0x00_also_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d589_0x024d Table 67: Rx SYNTHESIZER: Must be 0x00
ocpi_pad_24e	uchar	-	-		-	-	-
rx_synth_must_be_0x70	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d592_0x0250 Table 67: Rx SYNTHESIZER: Set to 0x70 (Must be 0x70)
rx_synth_vco_varactor_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d593_0x0251 Table 67: Rx SYNTHESIZER: RX VCO Varactor Control 1
ocpi_pad_252	uchar	-	-		-	-	-
rx_fast_lock_setup	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d602_0x025a Table 71: Rx FAST LOCK: Rx Fast Lock Setup
rx_fast_lock_setup_init_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d603_0x025b Table 71: Rx FAST LOCK: Rx Fast Lock Setup Init Delay
rx_fast_lock_program_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d604_0x025c Table 71: Rx FAST LOCK: Rx Fast Lock Program Address
rx_fast_lock_program_data	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d605_0x025d Table 71: Rx FAST LOCK: Rx Fast Lock Program Data
rx_fast_lock_program_read	uchar	-	-	Volatile	-	-	reg_addr_d606_0x025e Table 71: Rx FAST LOCK: Rx Fast Lock Program Read
rx_fast_lock_program_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d607_0x025f Table 71: Rx FAST LOCK: Rx Fast Lock Program Control
ocpi_pad_260	uchar	-	-		-	-	-
rx_lo_gen_power_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d609_0x0261 Table 72: Rx LO GENERATION: Rx LO Gen Power Mode
ocpi_pad_262	uchar	-	-		-	-	-
tx_synth_disable_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d624_0x0270 Table 73: Tx SYNTHESIZER: Disable VCO Cal
tx_synth_integer_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d625_0x0271 Table 73: Tx SYNTHESIZER: Integer Byte 0
tx_synth_integer_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d626_0x0272 Table 73: Tx SYNTHESIZER: Integer Byte 1
tx_synth_fract_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d627_0x0273 Table 73: Tx SYNTHESIZER: Fractional Byte 0
tx_synth_fract_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d628_0x0274 Table 73: Tx SYNTHESIZER: Fractional Byte 1
tx_synth_fract_byte_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d629_0x0275 Table 73: Tx SYNTHESIZER: Fractional Byte 2
tx_synth_force_alc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d630_0x0276 Table 73: Tx SYNTHESIZER: Force ALC
tx_synth_force_vco_tune_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d631_0x0277 Table 73: Tx SYNTHESIZER: Force VCO Tune 0

tx_synth_force_vco_tune_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d632_0x0278 Table 73: Tx SYNTHESIZER: Force VCO Tune 1
tx_synth_alcvaract_or	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d633_0x0279 Table 73: Tx SYNTHESIZER: ALC/Varactor
tx_synth_vco_output	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d634_0x027a Table 73: Tx SYNTHESIZER: VCO Output
tx_synth_cp_current	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d635_0x027b Table 73: Tx SYNTHESIZER: CP Current
tx_synth_cp_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d636_0x027c Table 73: Tx SYNTHESIZER: CP Offset
tx_synth_cp_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d637_0x027d Table 73: Tx SYNTHESIZER: CP Config
tx_synth_loop_filter_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d638_0x027e Table 73: Tx SYNTHESIZER: Loop Filter 1
tx_synth_loop_filter_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d639_0x027f Table 73: Tx SYNTHESIZER: Loop Filter 2
tx_synth_loop_filter_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d640_0x0280 Table 73: Tx SYNTHESIZER: Loop Filter 3
tx_synth_dithercp_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d641_0x0281 Table 73: Tx SYNTHESIZER: Dither/CP Cal
tx_synth_vco_bias_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d642_0x0282 Table 73: Tx SYNTHESIZER: VCO Bias 1
tx_synth_mustbe0x0d	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d643_0x0283 Table 73: Tx SYNTHESIZER: Must be 0x0D
tx_synth_cal_status	uchar	-	-	Volatile	-	-	reg_addr_d644_0x0284 Table 73: Tx SYNTHESIZER: Cal Status
tx_synth_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d645_0x0285 Table 73: Tx SYNTHESIZER: Must be 0x00
tx_synth_mustbe0x02	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d646_0x0286 Table 73: Tx SYNTHESIZER: Set to 0x02 (Must be 0x02)
tx_synth_cp_overrange_vco_lock	uchar	-	-	Volatile	-	-	reg_addr_d647_0x0287 Table 73: Tx SYNTHESIZER: CP Over Range/VCO Lock
tx_synth_mustbe0x0b	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d648_0x0288 Table 73: Tx SYNTHESIZER: Set to 0x0B (Must be 0x0B)
tx_synth_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d649_0x0289 Table 73: Tx SYNTHESIZER: VCO Cal
tx_synth_lock_detect_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d650_0x028a Table 73: Tx SYNTEHSIZER: Lock Detect Config
tx_synth_mustbe0x17	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d651_0x028b Table 73: Tx SYNTEHSIZER: Must be 0x17
tx_synth_mustbe0x00_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d652_0x028c Table 73: Tx SYNTEHSIZER: Must be 0x00
tx_synth_mustbe0x00_also_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d653_0x028d Table 73: Tx SYNTEHSIZER: Must be 0x00
ocpi_pad_28e	uchar	-	-		-	-	-
tx_synth_mustbe0x70	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d656_0x0290 Table 73: Tx SYNTEHSIZER: Set to 0x70 (Must be 0x70)
tx_synth_vco_varactor_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d657_0x0291 Table 73: Tx SYNTEHSIZER: VCO Varactor Control 1
dcxo_coarse_tune	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d658_0x0292 Table 74: DCXO: DCXO Coarse Tune
dcxo_fine_tune_high	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d659_0x0293 Table 74: DCXO: DCXO Fine Tune2

dcxo_fine_tune_low	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d660_0x0294 Table 74: DCXO: DCXO Fine Tune1
ocpi_pad_295	uchar	-	-		-	-	-
tx_fast_lock_setup	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d666_0x029a Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Setup
tx_fast_lock_setup_init_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d667_0x029b Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Setup Init Delay
tx_fast_lock_program_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d668_0x029c Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Addr
tx_fast_lock_program_data	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d669_0x029d Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Data
tx_fast_lock_program_read	uchar	-	-	Volatile	-	-	reg_addr_d670_0x029e Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Read
tx_fast_lock_program_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d671_0x029f Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Ctrl
ocpi_pad_2a0	uchar	-	-		-	-	-
tx_lo_gen_power_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d673_0x02a1 Table 76: Tx LO GENERATION: Tx LO Gen Power Mode
ocpi_pad_2a2	uchar	-	-		-	-	-
bandgap_mustbe0x0e	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d678_0x02a6 Table 77: MASTER BIAS AND BANDGAP CONFIGURATION: Set to 0x0E (Must be 0x0E)
ocpi_pad_2a7	uchar	-	-		-	-	-
bandgap_mustbe0x0e_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d680_0x02a8 Table 77: MASTER BIAS AND BANDGAP CONFIGURATION: Set to 0x0E (Must be 0x0E)
ocpi_pad_2a9	uchar	-	-		-	-	-
ref_divide_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d683_0x02ab Table 78: REFERENCE DIVIDER: Ref Divide Config 1
ref_divide_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d684_0x02ac Table 78: REFERENCE DIVIDER: Ref Divide Config 2
ocpi_pad_2ad	uchar	-	-		-	-	-
gain_readback_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d688_0x02b0 Table 80: Rx GAIN READ BACK: Gain Rx1
gain_readback_lpf_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d689_0x02b1 Table 80: Rx GAIN READ BACK: LPF Gain Rx1
gain_readback_dig_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d690_0x02b2 Table 80: Rx GAIN READ BACK: Dig gain Rx1
gain_readback_fast_attack_state	uchar	-	-	Volatile	-	-	reg_addr_d691_0x02b3 Table 80: Rx GAIN READ BACK: Fast Attack State
gain_readback_slow_loop_state	uchar	-	-	Volatile	-	-	reg_addr_d692_0x02b4 Table 80: Rx GAIN READ BACK: Slow Loop State
gain_readback_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d693_0x02b5 Table 80: Rx GAIN READ BACK: Gain Rx2
gain_readback_lpf_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d694_0x02b6 Table 80: Rx GAIN READ BACK: LPF Gain Rx2

gain_readback_dig_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d695_0x02b7 Table 80: Rx GAIN READ BACK: Dig Gain Rx2
gain_readback_ovrg_sigs_rx1	uchar	-	-	Volatile	-	-	reg_addr_d696_0x02b8 Table 80: Rx GAIN READ BACK: Ovrg Sigs Rx1
gain_readback_ovrg_sigs_rx2	uchar	-	-	Volatile	-	-	reg_addr_d697_0x02b9 Table 80: Rx GAIN READ BACK: Ovrg Sigs Rx2
ocpi_pad_2ba	uchar	-	-		-	-	-
ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d991_0x03df Table 83: CONTROL: Control
ocpi_pad_3e0	uchar	-	-		-	-	-
test_bist_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d1012_0x03f4 Table 84: DIGITAL TEST: BIST Config
test_observe_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d1013_0x03f5 Table 84: DIGITAL TEST: Observe Config
test_bist_and_data_port_test_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d1014_0x03f6 Table 84: DIGITAL TEST: BIST and Data Port Test Config
pin_control_p	bool	-	-		-	-	Whether RX/TX powerdown via pin control is possible.
other_present	bool	-	-	Readable	-	-	-
force_reset	bool	-	-	Readable, Writeable	-	0	Forces reset pin low (active low). Reset pin is otherwise the same level as the OpenCPI control plane reset signal.
qadc0_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qadc0, which supports first RX channel
qadc1_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qadc1, which supports second RX channel
qdac0_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qdac0, which supports first TX channel
qdac1_is_present	bool	-	-	Volatile	-	-	Inidicates whether or not bitstream was built with qdac1, which supports second TX channel
rx_frame_usage	enum	-	-	Volatile	-	-	enable : Register 0x010 bit D3 is 0, meaning Rx frame goes high coincident with the first valid receive sample. It stays high., toggle: Register 0x010 bit D3 is 1, meaning the Rx frame signal toggles with a duty cycle of 50
data_bus_index_direction	enum	-	-	Volatile	-	-	normal : Register 0x010 bit D1 is 0, meaning each RX sample's bit index direction is normal, i.e. [11:0], reverse: Register 0x010 bit D1 is 1, meaning each RX sample's bit direction is inverted, i.e. [0:11].
data_clk_is_inverted	bool	-	-	Volatile	-	-	false : Register 0x010 bit D0 is 0, meaning that the DATA_CLK follows the DATA_CLK_P signal in the UG570 timing diagrams, true : Register 0x010 bit D0 is 1, meaning that the DATA_CLK follows the DATA_CLK_N signal in the UG570 timing diagrams

rx_frame_is_inverted	bool	-	-	Volatile	-	-	false : Register 0x011 bit D2 is 0, meaning that the RX_FRAME follows the RX_FRAME_P signal in the UG570 timing diagrams, true : Register 0x011 bit D2 is 1, meaning that the RX_FRAME follows the RX_FRAME_N signal in the UG570 timing diagrams
LVDS	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use LVDS mode for Data/clock-/frame signals, and false if CMOS mode was used.
single_port	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use single port, and false if dual ports.
swap_ports	bool	-	-	Volatile	-	-	Value is true if bitstream was built to swap Port 0 and Port 1, and false if there was no swap.
half_duplex	bool	-	-	Volatile	-	-	Value is true if bitstream was built to use half duplex mode, and false if full duplex mode.
data_rate_config	enum	-	-	Volatile	-	-	Value indicates which data rate mode (SDR/DDR) the bitstream was built to use.
data_configs_are_valid	bool	-	-	Volatile	-	-	Value is false if bitstream was built using erroneous combination of LVDS/single port/half duplex/data rate config modes (takes into account build configurations for both ad9361_adc_sub and ad9361_dac_sub workers).
config_is_two_r	bool	-	-	Readable, Writeable	-	-	Used to tell the ad9361_adc_sub and ad9361_dac_sub workers what data paths are enabled. Note that, just because a qadc or qdac worker is present in the bitstream, that doesn't mean it is enabled.
config_is_two_t	bool	-	-	Readable, Writeable	-	-	Used to tell the ad9361_dac_sub worker what data paths are enabled. Note that, just because a qdac worker is present in the bitstream, that doesn't mean it is enabled.
force_two_r_two_t_timing	bool	-	-	Readable, Writeable	-	-	Used to force the ad9361_dac_sub worker to use the 2R2T timing diagram regardless of what TX channels are enabled. This property is expected to correspond to the D2 bit of the Parallel Port Configuration 1 register at SPI address 0x010.
Half_Duplex_Mode	bool	-	-	Writeable	-	false	-
ENSM_Pin_Control	bool	-	-	Writeable	-	true	Intended to match AD9361 register 0x014 bit D4.
Level_Mode	bool	-	-	Writeable	-	false	Intended to match AD9361 register 0x014 bit D3.
FDD_External_Control_Enable	bool	-	-	Writeable	-	false	Intended to match AD9361 register 0x014 bit D7.
ENABLE_force_set	bool	-	-	Writeable	-	false	Forces set of AD9361 ENABLE pin
TXNRX_force_set	bool	-	-	Writeable	-	false	Forces set of AD9361 TXNRX pin
general_spi_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d0_0x0000 Table 1: CHIP LEVEL SETUP: SPI Configuration

general_multichip_sync_and_tx_mon_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d1_0x0001 Table 1: CHIP LEVEL SETUP: Multichip Sync and Tx Mon Control
general_tx_enable_filter_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d2_0x0002 Table 1: CHIP LEVEL SETUP: Tx Enable & Filter Control
general_rx_enable_filter_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d3_0x0003 Table 1: CHIP LEVEL SETUP: Rx Enable & Filter Control
general_input_select	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d4_0x0004 Table 1: CHIP LEVEL SETUP: Input Select
general_rfpll_dividers	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d5_0x0005 Table 1: CHIP LEVEL SETUP: RFPLL Dividers
general_rx_clock_data_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d6_0x0006 Table 1: CHIP LEVEL SETUP: Rx Clock and Data Delay
general_tx_clock_data_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d7_0x0007 Table 1: CHIP LEVEL SETUP: Tx Clock and Data Delay
ocpi_pad_008	uchar	-	-		-	-	-
clock_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d9_0x0009 Table 8: CLOCK CONTROL: Clock Enable
clock_bbpll	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d10_0x000a Table 8: CLOCK CONTROL: BBPLL
temp_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d11_0x000b Table 10: TEMPERATURE SENSOR: Offset
temp_start_reading	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d12_0x000c Table 10: TEMPERATURE SENSOR: Start Temp Reading
temp_sense2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d13_0x000d Table 10: TEMPERATURE SENSOR: Temp Sense2
temp_temperature	uchar	-	-	Volatile	-	-	reg_addr_d14_0x000e Table 10: TEMPERATURE SENSOR: Temperature
temp_sensor_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d15_0x000f Table 10: TEMPERATURE SENSOR: Temp Sensor Config
parallel_port_conf_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d16_0x0010 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 1
parallel_port_conf_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d17_0x0011 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 2
parallel_port_conf_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d18_0x0012 Table 11: PARALLEL PORT CONFIGURATION: Parallel Port Configuration 3
ensm_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d19_0x0013 Table 12: ENABLE STATE MACHINE: ENSM Mode
ensm_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d20_0x0014 Table 12: ENABLE STATE MACHINE: ENSM Config 1
ensm_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d21_0x0015 Table 12: ENABLE STATE MACHINE: ENSM Config 2

ensm_calibration_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d22_0x0016 Table 12: ENABLE STATE MACHINE: Calibration Control
ensm_state	uchar	-	-	Volatile	-	-	reg_addr_d23_0x0017 Table 12: ENABLE STATE MACHINE: State
auxdac_1_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d24_0x0018 Table 15: AUXDAC: AuxDAC 1 Word
auxdac_2_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d25_0x0019 Table 15: AUXDAC: AuxDAC 2 Word
auxdac_1_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d26_0x001a Table 15: AUXDAC: AuxDAC 1 Config
auxdac_2_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d27_0x001b Table 15: AUXDAC: AuxDAC 2 Config
auxadc_clock_divider	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d28_0x001c Table 17: AUXILARYADC: AuxADC Clock Divider
auxadc_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d29_0x001d Table 17: AUXILARYADC: Aux ADC Config
auxadc_word_msb	uchar	-	-	Volatile	-	-	reg_addr_d30_0x001e Table 17: AUXILARYADC: AuxADC Word MSB
auxadc_world_lsb	uchar	-	-	Volatile	-	-	reg_addr_d31_0x001f Table 17: AUXILARYADC: AuxADC Word LSB
misc_auto_gpo	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d32_0x0020 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: Auto GPO
misc_agc_gain_lock_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d33_0x0021 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AGC Gain Lock Delay
misc_agc_attack_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d34_0x0022 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AGC Attack Delay
misc_auxdac_enable_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d35_0x0023 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC Enable Control
misc_rx_load_synth_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d36_0x0024 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: RX Load Synth Delay
misc_tx_load_synth_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d37_0x0025 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: TX Load Synth Delay
misc_external_lna_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d38_0x0026 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: External LNA control
misc_gpo_force_and_init	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d39_0x0027 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO Force and Init
misc_gpo0_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d40_0x0028 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO0 Rx delay

misc_gpo1_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d41_0x0029 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO1 Rx delay
misc_gpo2_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d42_0x002a Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO2 Rx delay
misc_gpo3_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d43_0x002b Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO3 Rx delay
misc_gpo0_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d44_0x002c Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO0 Tx Delay
misc_gpo1_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d45_0x002d Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO1 Tx Delay
misc_gpo2_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d46_0x002e Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO2 Tx Delay
misc_gpo3_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d47_0x002f Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: GPO3 Tx Delay
misc_auxdac1_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d48_0x0030 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC1 Rx Delay
misc_auxdac1_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d49_0x0031 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC1 Tx Delay
misc_auxdac2_rx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d50_0x0032 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC2 Rx Delay
misc_auxdac2_tx_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d51_0x0033 Table 18: GPO, AUXDAC, AGC DELAY, AND SYNTH DELOY CONTROL: AuxDAC2 Tx Delay
ocpi_pad_034	uchar	-	-		-	-	-
ctrl_output_pointer	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d53_0x0035 Table 19: CONTROL OUTPUT: Control Output Pointer
ctrl_output_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d54_0x0036 Table 19: CONTROL OUTPUT: Control Output Enable
product_id	uchar	-	-	Volatile	-	-	reg_addr_d55_0x0037 Table 20: PRODUCT ID: Product ID
ocpi_pad_038	uchar	-	-		-	-	-
reference_clock_cycles	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d58_0x003a Table 22: REFERENCE CLOCK CYCLES: Reference Clock Cycles
digital_io_digital_io_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d59_0x003b Table 23: DIGITAL IO CONTROL: Digital I/O Control

digital_io_lvds_bias_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d60_0x003c Table 23: DIGITAL IO CONTROL: LVDS Bias control
digital_io_lvds_invert_ctrl1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d61_0x003d Table 23: DIGITAL IO CONTROL: LVDS Invert control1
digital_io_lvds_invert_ctrl2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d62_0x003e Table 23: DIGITAL IO CONTROL: LVDS Invert control2
bbpll_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d63_0x003f Table 25: BBPLL CONTROL: BPLL Control 1
bbpll_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d64_0x0040 Table 25: BBPLL CONTROL: Must be 0
bbpll_fract_bb_freq_word_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d65_0x0041 Table 25: BBPLL CONTROL: Fractional BB Freq Word 1
bbpll_fract_bb_freq_word_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d66_0x0042 Table 25: BBPLL CONTROL: Fractional BB Freq Word 2
bbpll_fract_bb_freq_word_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d67_0x0043 Table 25: BBPLL CONTROL: Fractional BB Freq Word 3
bbpll_integer_bb_freq_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d68_0x0044 Table 25: BBPLL CONTROL: Integer BB Freq Word
bbpll_ref_clock_scaler	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d69_0x0045 Table 25: BBPLL CONTROL: Ref Clock Scaler
bbpll_cp_current	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d70_0x0046 Table 25: BBPLL CONTROL: CP Current
bbpll_msc_scale	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d71_0x0047 Table 25: BBPLL CONTROL: MSC Scale
bbpll_loop_filter_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d72_0x0048 Table 25: BBPLL CONTROL: Loop Filter 1
bbpll_loop_filter_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d73_0x0049 Table 25: BBPLL CONTROL: Loop Filter 2
bbpll_loop_filter_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d74_0x004a Table 25: BBPLL CONTROL: Loop Filter 3
bbpll_vco_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d75_0x004b Table 25: BBPLL CONTROL: VCO Control
bbpll_mustbe0x86	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d76_0x004c Table 25: BBPLL CONTROL: Must be_0x86
bpll_control_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d77_0x004d Table 25: BBPLL CONTROL: BPLL Control 2
bpll_control_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d78_0x004e Table 25: BBPLL CONTROL: BPLL Control 3
ocpi_pad_04f	uchar	-	-		-	-	-
power_down_override_rx_synth	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d80_0x0050 Table 26: POWER DOWN OVERRIDE: Rx Synth Power Down Override
power_down_override_tx_synth	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d81_0x0051 Table 26: POWER DOWN OVERRIDE: TX Synth Power Down Override
power_down_override_rx_control_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d82_0x0052 Table 26: POWER DOWN OVERRIDE: Control 0
power_down_override_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d83_0x0053 Table 26: POWER DOWN OVERRIDE: Must be 0

power_down_override_rx1_adc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d84_0x0054 Table 26: POWER DOWN OVERRIDE: Rx1 ADC Power Down Override
power_down_override_rx2_adc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d85_0x0055 Table 26: POWER DOWN OVERRIDE: Rx2 ADC Power Down Override
power_down_override_tx_analog	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d86_0x0056 Table 26: POWER DOWN OVERRIDE: Tx Analog Power Down Override 1
power_down_override_analog	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d87_0x0057 Table 26: POWER DOWN OVERRIDE: Analog Power Down Override
power_down_override_misc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d88_0x0058 Table 26: POWER DOWN OVERRIDE: Misc Power Down Override
ocpi_pad_059	uchar	-	-		-	-	-
overflow_ch_1	uchar	-	-	Volatile	-	-	reg_addr_d94_0x005e Table 27: OVERFLOW: CH 1 Overflow
overflow_ch_2	uchar	-	-	Volatile	-	-	reg_addr_d95_0x005f Table 27: OVERFLOW: CH 2 Overflow
tx_filter_coef_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d96_0x0060 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Address
tx_filter_coef_write_data_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d97_0x0061 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Write Data 1
tx_filter_coef_write_data_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d98_0x0062 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Write Data 2
tx_filter_coef_read_data_1	uchar	-	-	Volatile	-	-	reg_addr_d99_0x0063 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Read Data 1
tx_filter_coef_read_data_2	uchar	-	-	Volatile	-	-	reg_addr_d100_0x0064 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Coefficient Read Data 2
tx_filter_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d101_0x0065 Table 28: Tx PROGRAMMABLE FIR FILTER: TX Filter Configuration
ocpi_pad_066	uchar	-	-		-	-	-
tx_mon_low_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d103_0x0067 Table 29: Tx MONITOR: Tx Mon Low Gain
tx_mon_high_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d104_0x0068 Table 29: Tx MONITOR: Tx Mon High Gain
tx_mon_delay_counter	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d105_0x0069 Table 29: Tx MONITOR: Tx Mon Delay Counter
tx_mon_level_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d106_0x006a Table 29: Tx MONITOR: Tx Level Threshold
tx_mon_rssi1	uchar	-	-	Volatile	-	-	reg_addr_d107_0x006b Table 29: Tx MONITOR: TX RSSI1
tx_mon_rssi2	uchar	-	-	Volatile	-	-	reg_addr_d108_0x006c Table 29: Tx MONITOR: TX RSSI2
tx_mon_rssi_lsb	uchar	-	-	Volatile	-	-	reg_addr_d109_0x006d Table 29: Tx MONITOR: TX RSSI LSB
tx_mon_tpm_mode_enable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d110_0x006e Table 29: Tx MONITOR: TPM Mode Enable
tx_mon_temp_gain_coef	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d111_0x006f Table 29: Tx MONITOR: Temp Gain Coefficient
tx_mon_1_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d112_0x0070 Table 29: Tx MONITOR: Tx Mon 1 Config

tx_mon_2_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d113_0x0071 Table 29: Tx MONITOR: Tx Mon 2 Config
ocpi_pad_072	uchar	-	-		-	-	-
tx_pwr_atten_tx1_atten_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d115_0x0073 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx1 Atten 0
tx_pwr_atten_tx1_atten_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d116_0x0074 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx1 Atten 1
tx_pwr_atten_tx2_atten_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d117_0x0075 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx2 Atten 0
tx_pwr_atten_tx2_atten_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d118_0x0076 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx2 Atten 1
tx_pwr_atten_tx_atten_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d119_0x0077 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx Atten Offset
tx_pwr_atten_tx_atten_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d120_0x0078 Table 31: Tx POWER CONTROL AND ATTENUATION: Tx Atten Threshold
tx_pwr_atten_set_tx1_tx2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d121_0x0079 Table 31: Tx POWER CONTROL AND ATTENUATION: Set Tx1/Tx2
ocpi_pad_07a	uchar	-	-		-	-	-
tx_pwr_atten_immediate_update	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d124_0x007c Table 31: Tx POWER CONTROL AND ATTENUATION: Immediate Update
ocpi_pad_07d	uchar	-	-		-	-	-
tx_pgo_phase_corr_tx1_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d142_0x008e Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Phase Corr
tx_pgo_gain_corr_tx1_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d143_0x008f Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Gain Corr
tx_pgo_phase_corr_tx2_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d144_0x0090 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Phase Corr
tx_pgo_gain_corr_tx2_out1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d145_0x0091 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Gain Corr
tx_pgo_offset_corr_tx1_out1_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d146_0x0092 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Offset I
tx_pgo_offset_corr_tx1_out1_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d147_0x0093 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 1 Offset Q

tx_pgo_offset_corr_tx2_out1_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d148_0x0094 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Offset I
tx_pgo_offset_corr_tx2_out1_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d149_0x0095 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 1 Offset Q
tx_pgo_phase_corr_tx1_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d150_0x0096 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Phase Corr
tx_pgo_gain_corr_tx1_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d151_0x0097 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Gain Corr
tx_pgo_phase_corr_tx2_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d152_0x0098 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Phase Corr
tx_pgo_gain_corr_tx2_out2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d153_0x0099 Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Gain Corr
tx_pgo_offset_corr_tx1_out2_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d154_0x009a Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Offset I
tx_pgo_offset_corr_tx1_out2_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d155_0x009b Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx1 Out 2 Offset Q
tx_pgo_offset_corr_tx2_out2_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d156_0x009c Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Offset I
tx_pgo_offset_corr_tx2_out2_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d157_0x009d Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Tx2 Out 2 Offset Q
ocpi_pad_09e	uchar	-	-		-	-	-
tx_quad_cal_pgo_force_bits	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d159_0x009f Table 32: Tx QUADRATURE CALIBRATION, PHASE, GAIN, AND OFFSET CORRECTION: Force Bits
tx_quad_cal_nco_freq_phase_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d160_0x00a0 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad Cal NCO Freq & Phase Offset
tx_quad_cal_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d161_0x00a1 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad Cal Control

tx_quad_cal_kexp_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d162_0x00a2 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Kexp 1
tx_quad_cal_kexp_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d163_0x00a3 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Kexp 2
tx_quad_cal_settle_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d164_0x00a4 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: QUAD Settle count
tx_quad_cal_mag_ftest_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d165_0x00a5 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Mag. Ftest Thresh
tx_quad_cal_mag_ftest_thresh_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d166_0x00a6 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Mag. Ftest Thresh 2
tx_quad_cal_status_tx1	uchar	-	-	Volatile	-	-	reg_addr_d167_0x00a7 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal status Tx1
tx_quad_cal_status_tx2	uchar	-	-	Volatile	-	-	reg_addr_d168_0x00a8 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal status Tx2
tx_quad_cal_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d169_0x00a9 Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Quad cal Count
tx_quad_cal_full_lmt_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d170_0x00aa Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Tx Quad Full/LMT Gain
tx_quad_cal_squarer_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d171_0x00ab Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Squarer Config
tx_quad_cal_atten	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d172_0x00ac Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: TX Quad Cal Atten
tx_quad_cal_thresh_accum	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d173_0x00ad Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Thresh Accum
tx_quad_cal_lpf_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d174_0x00ae Table 33: Tx QUADRATE CALIBRATION CONFIGURATION: Tx Quad LPF Gain
ocpi_pad_0af	uchar	-	-		-	-	-
tx_bbf_r1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d194_0x00c2 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R1
tx_bbf_r2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d195_0x00c3 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R2
tx_bbf_r3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d196_0x00c4 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R3
tx_bbf_r4	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d197_0x00c5 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R4

tx_bbf_rp	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d198_0x00c6 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF RP
tx_bbf_c1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d199_0x00c7 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF C1
tx_bbf_c2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d200_0x00c8 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF C2
tx_bbf_cp	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d201_0x00c9 Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF CP
tx_bbf_tuner_pd	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d202_0x00ca Table 34: Tx BASEBAND FILTER REGISTERS: Tx Tuner PD
tx_bbf_r2b	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d203_0x00cb Table 34: Tx BASEBAND FILTER REGISTERS: Tx BBF R2b
ocpi_pad_0cc	uchar	-	-		-	-	-
tx_secondf_config0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d208_0x00d0 Table 35: Tx SECONDARY FILTER REGISTERS: Config0
tx_secondf_resistor	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d209_0x00d1 Table 35: Tx SECONDARY FILTER REGISTERS: Resistor
tx_secondf_capacitor	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d210_0x00d2 Table 35: Tx SECONDARY FILTER REGISTERS: Capacitor
tx_secondf_mustbe0x60	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d211_0x00d3 Table 35: Tx SECONDARY FILTER REGISTERS: Must be 0x60
ocpi_pad_0d4	uchar	-	-		-	-	-
tx_bbf_tune_divider	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d214_0x00d6 Table 38: Tx BBF TUNER CONFIGURATION: TX BBF Tune Divider
tx_bbf_tune_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d215_0x00d7 Table 38: Tx BBF TUNER CONFIGURATION: TX BBF Tune Mode
ocpi_pad_0d8	uchar	-	-		-	-	-
rx_filter_coef_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d240_0x00f0 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Addr
rx_filter_coef_write_data_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d241_0x00f1 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Data 1
rx_filter_coef_write_data_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d242_0x00f2 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Data 2
rx_filter_coef_read_data_1	uchar	-	-	Volatile	-	-	reg_addr_d243_0x00f3 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Read Data 1
rx_filter_coef_read_data_2	uchar	-	-	Volatile	-	-	reg_addr_d244_0x00f4 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Coeff Read Data 2
rx_filter_conf	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d245_0x00f5 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Configuration
rx_filter_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d246_0x00f6 Table 39: Rx PROGRAMMABLE FIR FILTER: Rx Filter Gain

ocpi_pad_0f7	uchar	-	-		-	-	-
gain_agc_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d250_0x00fa Table 42: GAIN CONTROL SETUP: AGC Config1
gain_agc_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d251_0x00fb Table 42: GAIN CONTROL SETUP: AGC config2
gain_agc_config_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d252_0x00fc Table 42: GAIN CONTROL SETUP: AGC Config3
gain_max_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d253_0x00fd Table 42: GAIN CONTROL SETUP: Max LMT/Full Gain
gain_peak_wait_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d254_0x00fe Table 42: GAIN CONTROL SETUP: Peak Wait Time
ocpi_pad_0ff	uchar	-	-		-	-	-
gain_digital_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d256_0x0100 Table 42: GAIN CONTROL SETUP: Digital Gain
gain_agc_lock_level	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d257_0x0101 Table 42: GAIN CONTROL SETUP: AGC Lock Level
ocpi_pad_102	uchar	-	-		-	-	-
gain_gain_stp_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d259_0x0103 Table 42: GAIN CONTROL SETUP: Gain Step Config 1
gain_adc_small_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d260_0x0104 Table 42: GAIN CONTROL SETUP: ADC Small Overload Threshold
gain_adc_large_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d261_0x0105 Table 42: GAIN CONTROL SETUP: ADC Large Overload Threshold
gain_stp_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d262_0x0106 Table 42: GAIN CONTROL SETUP: Gain Step Config 2
gain_small_lmt_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d263_0x0107 Table 42: GAIN CONTROL SETUP: Small LMT Overload Threshold
gain_large_lmt_overload_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d264_0x0108 Table 42: GAIN CONTROL SETUP: Large LMT Overload Threshold
gain_rx1_manual_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d265_0x0109 Table 42: GAIN CONTROL SETUP: Rx1 Manual LMT/Full Gain
gain_rx1_manual_lpf_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d266_0x010a Table 42: GAIN CONTROL SETUP: Rx1 Manual LPF gain
gain_rx1_manual_digitalforced_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d267_0x010b Table 42: GAIN CONTROL SETUP: Rx1 Manual Digital/Forced Gain
gain_rx2_manual_lmt_full_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d268_0x010c Table 42: GAIN CONTROL SETUP: Rx2 Manual LMT/Full Gain
gain_rx2_manual_lpf_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d269_0x010d Table 42: GAIN CONTROL SETUP: Rx2 Manual LPF Gain
gain_rx2_manual_digitalforced_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d270_0x010e Table 42: GAIN CONTROL SETUP: Rx2 Manual Digital/Forced Gain

ocpi_pad_10f	uchar	-	-		-	-	-
fast_agc_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d272_0x0110 Table 44: FAST ATTACK AGC SETUP: Config 1
fast_agc_config_2_settling_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d273_0x0111 Table 44: FAST ATTACK AGC SETUP: Config 2 & Settling Delay
fast_agc_energy_lost_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d274_0x0112 Table 44: FAST ATTACK AGC SETUP: Energy Lost Threshold
fast_agc_stronger_signal_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d275_0x0113 Table 44: FAST ATTACK AGC SETUP: Stronger Signal Threshold
fast_agc_low_power_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d276_0x0114 Table 44: FAST ATTACK AGC SETUP: Low Power Threshold
fast_agc_strong_signal_freeze	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d277_0x0115 Table 44: FAST ATTACK AGC SETUP: Strong Signal Freeze
fast_agc_final_over_range_and_opt_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d278_0x0116 Table 44: FAST ATTACK AGC SETUP: Final Over Range and Opt Gain
fast_agc_energy_detect_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d279_0x0117 Table 44: FAST ATTACK AGC SETUP: Energy Detect Count
fast_agc_agcll_upper_limit	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d280_0x0118 Table 44: FAST ATTACK AGC SETUP: AGCLL Upper Limit
fast_agc_gain_lock_exit_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d281_0x0119 Table 44: FAST ATTACK AGC SETUP: Gain Lock Exit Count
fast_agc_initial_lmt_gain_limit	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d282_0x011a Table 44: FAST ATTACK AGC SETUP: Initial LMT Gain Limit
fast_agc_increment_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d283_0x011b Table 44: FAST ATTACK AGC SETUP: Increment Time
ocpi_pad_11c	uchar	-	-		-	-	-
slowhybrid_agc_inner_low_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d288_0x0120 Table 45: SLOW ATTACK AND HYBRID AGC: AGC Inner Low Threshold
slowhybrid_agc_lmt_overload_counters	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d289_0x0121 Table 45: SLOW ATTACK AND HYBRID AGC: LMT Overload Counters
slowhybrid_agc_adc_overload_counters	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d290_0x0122 Table 45: SLOW ATTACK AND HYBRID AGC: ADC Overload Counters
slowhybrid_agc_gain_stp1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d291_0x0123 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Step1
slowhybrid_agc_gain_update_counter1	uchar	-	-	Volatile	-	-	reg_addr_d292_0x0124 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Update Counter1
slowhybrid_agc_gain_update_counter2	uchar	-	-	Volatile	-	-	reg_addr_d293_0x0125 Table 45: SLOW ATTACK AND HYBRID AGC: Gain Update Counter2
ocpi_pad_126	uchar	-	-		-	-	-
slowhybrid_agc_digital_sat_counter	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d296_0x0128 Table 45: SLOW ATTACK AND HYBRID AGC: Digital Sat Counter

slowhybrid_agc_outer_power_threshs	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d297_0x0129 Table 45: SLOW ATTACK AND HYBRID AGC: Outer Power Thresholds
slowhybrid_agc_gain_stp_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d298_0x012a Table 45: SLOW ATTACK AND HYBRID AGC: Gain Step 2
ocpi_pad_12b	uchar	-	-		-	-	-
ext_lna_high_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d300_0x012c Table 46: EXTERNAL LNA GAIN WORD: Ext LNA High Gain
ext_lna_low_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d301_0x012d Table 46: EXTERNAL LNA GAIN WORD: Ext LNA Low Gain
ocpi_pad_12e	uchar	-	-		-	-	-
gain_table	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d304_0x0130 Table 47: AGC GAIN TABLE: Gain Table Address
gain_table_write_data1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d305_0x0131 Table 47: AGC GAIN TABLE: Gain Table Write Data1
gain_table_write_data2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d306_0x0132 Table 47: AGC GAIN TABLE: Gain Table Write Data2
gain_table_write_data3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d307_0x0133 Table 47: AGC GAIN TABLE: Gain Table Write Data 3
gain_table_read_data1	uchar	-	-	Volatile	-	-	reg_addr_d308_0x0134 Table 47: AGC GAIN TABLE: Gain Table Read Data 1
gain_table_read_data2	uchar	-	-	Volatile	-	-	reg_addr_d309_0x0135 Table 47: AGC GAIN TABLE: Gain Table Read Data 2
gain_table_read_data3	uchar	-	-	Volatile	-	-	reg_addr_d310_0x0136 Table 47: AGC GAIN TABLE: Gain Table Read Data 3
gain_table_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d311_0x0137 Table 47: AGC GAIN TABLE: Gain Table Config
mixer_subtable	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d312_0x0138 Table 48: MIXER SUBTABLE: Mixer Subtable Address
mixer_subtable_gain_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d313_0x0139 Table 48: MIXER SUBTABLE: Mixer Subtable Gain Word Write
mixer_subtable_bias_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d314_0x013a Table 48: MIXER SUBTABLE: Mixer Subtable Bias Word Write
mixer_subtable_ctrl_write	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d315_0x013b Table 48: MIXER SUBTABLE: Mixer Subtable Control Word Write
mixer_subtable_gain_read	uchar	-	-	Volatile	-	-	reg_addr_d316_0x013c Table 48: MIXER SUBTABLE: Mixer Subtable Gain Word Read
mixer_subtable_bias_read	uchar	-	-	Volatile	-	-	reg_addr_d317_0x013d Table 48: MIXER SUBTABLE: Mixer Subtable Bias Word Read
mixer_subtable_ctrl_read	uchar	-	-	Volatile	-	-	reg_addr_d318_0x013e Table 48: MIXER SUBTABLE: Mixer Subtable Control Word Read

mixer_subtable_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d319_0x013f Table 48: MIXER SUBTABLE: Mixer Subtable Config
calib_gain_table_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d320_0x0140 Table 49: CALIBRATION GAIN TABLE: Word_Address
calib_gain_table_diff_worderror_write	uchar	-	-	Writeable	-	-	reg_addr_d321_0x0141 Table 49: CALIBRATION GAIN TABLE: Gain Diff Word/Error Write
calib_gain_table_gain_error_read	uchar	-	-	Volatile	-	-	reg_addr_d322_0x0142 Table 49: CALIBRATION GAIN TABLE: Gain Error Read
calib_gain_table_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d323_0x0143 Table 49: CALIBRATION GAIN TABLE: Config
calib_gain_table_lna_diff_read_back	uchar	-	-	Volatile	-	-	reg_addr_d324_0x0144 Table 49: CALIBRATION GAIN TABLE: LNA Gain Diff Read Back
gen_calib_max_mixer_gain_index	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d325_0x0145 Table 50: GENERAL CALIBRATION: Max Mixer Calibration Gain Index
gen_calib_temp_gain_coef	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d326_0x0146 Table 50: GENERAL CALIBRATION: Temp Gain Coefficient
gen_calib_settle_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d327_0x0147 Table 50: GENERAL CALIBRATION: Settle Time
gen_calib_measure_duration	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d328_0x0148 Table 50: GENERAL CALIBRATION: Measure Duration
gen_calib_cal_temp_sensor_word	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d329_0x0149 Table 50: GENERAL CALIBRATION: Cal Temp sensor word
ocpi_pad_14a	uchar	-	-		-	-	-
rssi_measure_duration_01	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d336_0x0150 Table 51: RSSI MEASUREMENT CONFIGURATION: Measure Duration 0,1
rssi_measure_duration_23	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d337_0x0151 Table 51: RSSI MEASUREMENT CONFIGURATION: Measure Duration 2,3
rssi_weight_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d338_0x0152 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 0
rssi_weight_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d339_0x0153 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 1
rssi_weight_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d340_0x0154 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 2
rssi_weight_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d341_0x0155 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Weight 3
rssi_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d342_0x0156 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI delay
rssi_wait_time	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d343_0x0157 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI wait time

rssi_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d344_0x0158 Table 51: RSSI MEASUREMENT CONFIGURATION: RSSI Config
ocpi_pad_159	uchar	-	-		-	-	-
rssi_dec_power_duration_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d348_0x015c Table 51: RSSI MEASUREMENT CONFIGURATION: Dec Power Duration
rssi_lna_gain	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d349_0x015d Table 51: RSSI MEASUREMENT CONFIGURATION: LNA Gain
ocpi_pad_15e	uchar	-	-		-	-	-
power_ch1_rx_filter_power	uchar	-	-	Volatile	-	-	reg_addr_d353_0x0161 Table 53: POWER WORD: CH1 Rx filter Power
ocpi_pad_162	uchar	-	-		-	-	-
power_ch2_rx_filter_power	uchar	-	-	Volatile	-	-	reg_addr_d355_0x0163 Table 53: POWER WORD: CH2 Rx filter Power
ocpi_pad_164	uchar	-	-		-	-	-
calibration_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d361_0x0169 Table 54: Rx QUADRATURE CALIBRATION: Calibration Config 1
calibration_mustbe0x75	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d362_0x016a Table 54: Rx QUADRATURE CALIBRATION: Must be 0x75
calibration_mustbe0x95	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d363_0x016b Table 54: Rx QUADRATURE CALIBRATION: Must be 0x95
ocpi_pad_16c	uchar	-	-		-	-	-
rx_pgo_phase_corr_rx1_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d368_0x0170 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Phase Corr
rx_pgo_gain_corr_rx1_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d369_0x0171 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Gain Corr
rx_pgo_phase_corr_rx2_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d370_0x0172 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Phase Corr
rx_pgo_gain_corr_rx2_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d371_0x0173 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Gain Corr
rx_pgo_offset_corr_rx1_ina_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d372_0x0174 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Q Offset
rx_pgo_offset_corr_rx1_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d373_0x0175 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1A Offset
rx_pgo_offset_corr_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d374_0x0176 Table 55: Rx PHASE AND GAIN CORRECTION: Input A Offsets
rx_pgo_offset_corr_rx2_ina	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d375_0x0177 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A Offset
rx_pgo_offset_corr_rx2_ina_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d376_0x0178 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2A I Offset
rx_pgo_phase_corr_rx1_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d377_0x0179 Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Phase Corr

rx_pgo_gain_corr_rx1_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d378_0x017a Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Gain Corr
rx_pgo_phase_corr_rx2_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d379_0x017b Table 55: Rx PHASE AND GAIN CORRECTION: Rx2B/C Phase Corr
rx_pgo_gain_corr_rx2_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d380_0x017c Table 55: Rx PHASE AND GAIN CORRECTION: Rx2B/C Gain Corr
rx_pgo_offset_corr_rx1_inbc_q	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d381_0x017d Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C Q Offset
rx_pgo_offset_corr_rx1_inbc_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d382_0x017e Table 55: Rx PHASE AND GAIN CORRECTION: Rx1B/C I Offset
rx_pgo_offset_corr_inpbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d383_0x017f Table 55: Rx PHASE AND GAIN CORRECTION: Input B/C Offsets
rx_pgo_offset_corr_rx2_inbc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d384_0x0180 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2 B/C Offset
rx_pgo_offset_corr_rx2_inbc_i	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d385_0x0181 Table 55: Rx PHASE AND GAIN CORRECTION: Rx2 B/C I Offset
rx_pgo_force_bits	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d386_0x0182 Table 55: Rx PHASE AND GAIN CORRECTION: Force Bits
ocpi_pad_183	uchar	-	-		-	-	-
rx_dc_offset_wait_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d389_0x0185 Table 56: Rx DC OFFSET CONTROL: Wait Count
rx_dc_offset_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d390_0x0186 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Count
rx_dc_offset_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d391_0x0187 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Config 1
rx_dc_offset_atten	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d392_0x0188 Table 56: Rx DC OFFSET CONTROL: RF DC Offset Attenuation
rx_dc_offset_mustbe0x30	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d393_0x0189 Table 56: Rx DC OFFSET CONTROL: Must be 0x30
ocpi_pad_18a	uchar	-	-		-	-	-
rx_dc_offset_config2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d395_0x018b Table 56: Rx DC OFFSET CONTROL: DC Offset Config2
rx_dc_offset_rf_cal_gain_index	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d396_0x018c Table 56: Rx DC OFFSET CONTROL: RF Cal Gain Index
rx_dc_offset_soi_thresh	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d397_0x018d Table 56: Rx DC OFFSET CONTROL: SOI Threshold
ocpi_pad_18e	uchar	-	-		-	-	-
rx_dc_offset_bb_shift	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d400_0x0190 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Shift
rx_dc_offset_bb_fast_settle_shift	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d401_0x0191 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Fast Settle Shift

rx_dc_offset_bb_fast_settle_dur	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d402_0x0192 Table 56: Rx DC OFFSET CONTROL: BB Fast Settle Dur
rx_dc_offset_bb_count	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d403_0x0193 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Count
rx_dc_offset_bb_atten	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d404_0x0194 Table 56: Rx DC OFFSET CONTROL: BB DC Offset Attenuation
ocpi_pad_195	uchar	-	-		-	-	-
rx_bb_dc_offset_rx1_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d410_0x019a Table 60: Rx BB DC OFFSET: RX1 BB DC word I MSB
rx_bb_dc_offset_rx1_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d411_0x019b Table 60: Rx BB DC OFFSET: RX1 BB DC word I LSB
rx_bb_dc_offset_rx1_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d412_0x019c Table 60: Rx BB DC OFFSET: RX1 BB DC word Q MSB
rx_bb_dc_offset_rx1_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d413_0x019d Table 60: Rx BB DC OFFSET: RX1 BB DC word Q LSB
rx_bb_dc_offset_rx2_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d414_0x019e Table 60: Rx BB DC OFFSET: RX2 BB DC word I MSB
rx_bb_dc_offset_rx2_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d415_0x019f Table 60: Rx BB DC OFFSET: RX2 BB DC word I LSB
rx_bb_dc_offset_rx2_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d416_0x01a0 Table 60: Rx BB DC OFFSET: RX2 BB DC word Q MSB
rx_bb_dc_offset_rx2_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d417_0x01a1 Table 60: Rx BB DC OFFSET: RX2 BB DC word Q LSB
rx_bb_dc_offset_track_corr_word_i_msb	uchar	-	-	Volatile	-	-	reg_addr_d418_0x01a2 Table 60: Rx BB DC OFFSET: BB Track corr word I MSB
rx_bb_dc_offset_track_corr_word_i_lsb	uchar	-	-	Volatile	-	-	reg_addr_d419_0x01a3 Table 60: Rx BB DC OFFSET: BB Track corr word I LSB
rx_bb_dc_offset_track_corr_word_q_msb	uchar	-	-	Volatile	-	-	reg_addr_d420_0x01a4 Table 60: Rx BB DC OFFSET: BB Track corr word Q MSB
rx_bb_dc_offset_track_corr_word_q_lsb	uchar	-	-	Volatile	-	-	reg_addr_d421_0x01a5 Table 60: Rx BB DC OFFSET: BB Track corr word Q LSB
ocpi_pad_1a6	uchar	-	-		-	-	-
rssi_readback_rx1_symbol	uchar	-	-	Volatile	-	-	reg_addr_d423_0x01a7 Table 61: RSSI READBACK: Rx1 RSSI Symbol
rssi_readback_rx1_preamble	uchar	-	-	Volatile	-	-	reg_addr_d424_0x01a8 Table 61: RSSI READBACK: Rx1 RSSI preamble
rssi_readback_rx2_symbol	uchar	-	-	Volatile	-	-	reg_addr_d425_0x01a9 Table 61: RSSI READBACK: Rx2 RSSI symbol
rssi_readback_rx2_preamble	uchar	-	-	Volatile	-	-	reg_addr_d426_0x01aa Table 61: RSSI READBACK: Rx2 RSSI preamble

rssi_readback_symbol_lsb	uchar	-	-	Volatile	-	-	reg_addr_d427_0x01ab Table 61: RSSI READBACK: Symbol LSB
rssi_readback_preamble_lsb	uchar	-	-	Volatile	-	-	reg_addr_d428_0x01ac Table 61: RSSI READBACK: Preamble LSB
ocpi_pad_1ad	uchar	-	-		-	-	-
rx_tia_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d475_0x01db Table 62: Rx TIA: Rx TIA Config
rx_tia_1_c_lsb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d476_0x01dc Table 62: Rx TIA: TIA1 C LSB
rx_tia_1_c_msb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d477_0x01dd Table 62: Rx TIA: TIA1 C MSB
rx_tia_2_c_lsb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d478_0x01de Table 62: Rx TIA: TIA2 C LSB
rx_tia_2_c_msb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d479_0x01df Table 62: Rx TIA: TIA2 C MSB
rx_bbf_rx1_r1a	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d480_0x01e0 Table 65: Rx BFF: Rx1 BBF R1A
rx_bbf_rx2_r1a	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d481_0x01e1 Table 65: Rx BFF: Rx2 BBF R1A
rx_bff_rx1_tune_ctrl	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d482_0x01e2 Table 65: Rx BFF: Rx1 Tune Control
rx_bff_rx2_tune_ctrl	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d483_0x01e3 Table 65: Rx BFF: Rx2 Tune Control
rx_bff_rx1_bbf_r5	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d484_0x01e4 Table 65: Rx BFF: Rx1 BBF R5
rx_bff_rx2_bbf_r5	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d485_0x01e5 Table 65: Rx BFF: Rx2 BBF R5
rx_bbf_r2346	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d486_0x01e6 Table 65: Rx BFF: Rx BBF R2346
rx_bbf_c1_msb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d487_0x01e7 Table 65: Rx BFF: Rx BBF C1 MSB
rx_bbf_c1_lsb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d488_0x01e8 Table 65: Rx BFF: Rx BBF C1 LSB
rx_bbf_c2_msb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d489_0x01e9 Table 65: Rx BFF: Rx BBF C2 MSB
rx_bbf_c2_lsb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d490_0x01ea Table 65: Rx BFF: Rx BBF C2 LSB
rx_bbf_c3_msb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d491_0x01eb Table 65: Rx BFF: Rx BBF C3 MSB
rx_bbf_c3_lsb	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d492_0x01ec Table 65: Rx BFF: Rx BBF C3 LSB
rx_bbf_cc1_ctr	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d493_0x01ed Table 65: Rx BFF: Rx BBF CC1 Ctr
rx_bbf_mustbe0x60	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d494_0x01ee Table 65: Rx BFF: Must be 0x60
rx_bbf_cc2_ctr	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d495_0x01ef Table 65: Rx BFF: Rx BBF CC2 Ctr
rx_bbf_pow_rz_byte1	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d496_0x01f0 Table 65: Rx BFF: Rx BBF Pow Rz Byte1
rx_bbf_cc3_ctr	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d497_0x01f1 Table 65: Rx BFF: Rx BBF CC3 Ctr
rx_bbf_r5_tune	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d498_0x01f2 Table 65: Rx BFF: Rx BBF R5 Tune
rx_bbf_tune	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d499_0x01f3 Table 65: Rx BFF: Rx BBF Tune
rx_bff_rx1_bbf_man_gain	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d500_0x01f4 Table 65: Rx BFF: Rx1 BBF Man Gain
rx_bff_rx2_bbf_man_gain	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d501_0x01f5 Table 65: Rx BFF: Rx2 BBF Man Gain
ocpi_pad_1f6	uchar	-	-		-	-	-

rx_bbf_tune_config_divide	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d504_0x01f8 Table 66: Rx BBF TUNER CONFIGURATION: RX BBF Tune Divide
rx_bbf_tune_config_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d505_0x01f9 Table 66: Rx BBF TUNER CONFIGURATION: RX BBF Tune Config
rx_bbf_tune_config_mustbe0x01	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d506_0x01fa Table 66: Rx BBF TUNER CONFIGURATION: Must be 0x01
rx_bbf_tune_config_rx_bbbw_mhz	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d507_0x01fb Table 66: Rx BBF TUNER CONFIGURATION: Rx BBBW MHz
rx_bbf_tune_config_rx_bbbw_khz	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d508_0x01fc Table 66: Rx BBF TUNER CONFIGURATION: Rx BBBW kHz
ocpi_pad_1fd	uchar	-	-		-	-	-
rx_synth_disable_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d560_0x0230 Table 67: Rx SYNTHESIZER: Disable VCO Cal
rx_synth_integer_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d561_0x0231 Table 67: Rx SYNTHESIZER: RX Integer Byte 0
rx_synth_integer_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d562_0x0232 Table 67: Rx SYNTHESIZER: RX Integer Byte 1
rx_synth_fract_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d563_0x0233 Table 67: Rx SYNTHESIZER: RX Fractional Byte 0
rx_synth_fract_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d564_0x0234 Table 67: Rx SYNTHESIZER: RX Fractional Byte 1
rx_synth_fract_byte_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d565_0x0235 Table 67: Rx SYNTHESIZER: RX Fractional Byte 2
rx_synth_force_alc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d566_0x0236 Table 67: Rx SYNTHESIZER: RX Force ALC
rx_synth_force_vco_tune_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d567_0x0237 Table 67: Rx SYNTHESIZER: RX Force VCO Tune 0
rx_synth_force_vco_tune_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d568_0x0238 Table 67: Rx SYNTHESIZER: RX Force VCO Tune 1
rx_synth_alc_varactor	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d569_0x0239 Table 67: Rx SYNTHESIZER: RX ALC/Varactor
rx_synth_vco_output	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d570_0x023a Table 67: Rx SYNTHESIZER: RX VCO Output
rx_synth_cp_current	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d571_0x023b Table 67: Rx SYNTHESIZER: RX CP Current
rx_synth_cp_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d572_0x023c Table 67: Rx SYNTHESIZER: RX CP Offset
rx_synth_cp_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d573_0x023d Table 67: Rx SYNTHESIZER: RX CP Config
rx_synth_loop_filter_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d574_0x023e Table 67: Rx SYNTHESIZER: RX Loop Filter 1
rx_synth_loop_filter_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d575_0x023f Table 67: Rx SYNTHESIZER: RX Loop Filter 2
rx_synth_loop_filter_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d576_0x0240 Table 67: Rx SYNTHESIZER: RX Loop Filter 3
rx_synth_dithercp_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d577_0x0241 Table 67: Rx SYNTHESIZER: RX Dither/CP Cal
rx_synth_vco_bias_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d578_0x0242 Table 67: Rx SYNTHESIZER: RX VCO Bias 1

rx_synth_mustbe0x0d	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d579_0x0243 Table 67: Rx SYNTHESIZER: Must be 0x0D
rx_synth_cal_status	uchar	-	-	Volatile	-	-	reg_addr_d580_0x0244 Table 67: Rx SYNTHESIZER: RX Cal Status
rx_synth_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d581_0x0245 Table 67: Rx SYNTHESIZER: Must be 0x00
rx_synth_mustbe0x02	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d582_0x0246 Table 67: Rx SYNTHESIZER: Set to 0x02 (Must be 0x02)
rx_synth_cp_ovrg_vco_lock	uchar	-	-	Volatile	-	-	reg_addr_d583_0x0247 Table 67: Rx SYNTHESIZER: RX CP Ovrg/VCO Lock
rx_synth_mustbe0x0b	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d584_0x0248 Table 67: Rx SYNTHESIZER: Set to 0x0B (Must be 0x0B)
rx_synth_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d585_0x0249 Table 67: Rx SYNTHESIZER: RX VCO Cal
rx_synth_lock_detect_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d586_0x024a Table 67: Rx SYNTHESIZER: RX Lock Detect Config
rx_synth_mustbe0x17	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d587_0x024b Table 67: Rx SYNTHESIZER: Must be 0x17
rx_synth_mustbe0x00_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d588_0x024c Table 67: Rx SYNTHESIZER: Must be 0x00
rx_synth_mustbe0x00_also_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d589_0x024d Table 67: Rx SYNTHESIZER: Must be 0x00
ocpi_pad_24e	uchar	-	-		-	-	-
rx_synth_must_be_0x70	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d592_0x0250 Table 67: Rx SYNTHESIZER: Set to 0x70 (Must be 0x70)
rx_synth_vco_varactor_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d593_0x0251 Table 67: Rx SYNTHESIZER: RX VCO Varactor Control 1
ocpi_pad_252	uchar	-	-		-	-	-
rx_fast_lock_setup	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d602_0x025a Table 71: Rx FAST LOCK: Rx Fast Lock Setup
rx_fast_lock_setup_init_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d603_0x025b Table 71: Rx FAST LOCK: Rx Fast Lock Setup Init Delay
rx_fast_lock_program_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d604_0x025c Table 71: Rx FAST LOCK: Rx Fast Lock Program Address
rx_fast_lock_program_data	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d605_0x025d Table 71: Rx FAST LOCK: Rx Fast Lock Program Data
rx_fast_lock_program_read	uchar	-	-	Volatile	-	-	reg_addr_d606_0x025e Table 71: Rx FAST LOCK: Rx Fast Lock Program Read
rx_fast_lock_program_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d607_0x025f Table 71: Rx FAST LOCK: Rx Fast Lock Program Control
ocpi_pad_260	uchar	-	-		-	-	-
rx_lo_gen_power_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d609_0x0261 Table 72: Rx LO GENERATION: Rx LO Gen Power Mode
ocpi_pad_262	uchar	-	-		-	-	-
tx_synth_disable_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d624_0x0270 Table 73: Tx SYNTHESIZER: Disable VCO Cal
tx_synth_integer_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d625_0x0271 Table 73: Tx SYNTHESIZER: Integer Byte 0

tx_synth_integer_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d626_0x0272 Table 73: Tx SYNTHESIZER: Integer Byte 1
tx_synth_fract_byte_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d627_0x0273 Table 73: Tx SYNTHESIZER: Fractional Byte 0
tx_synth_fract_byte_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d628_0x0274 Table 73: Tx SYNTHESIZER: Fractional Byte 1
tx_synth_fract_byte_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d629_0x0275 Table 73: Tx SYNTHESIZER: Fractional Byte 2
tx_synth_force_alc	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d630_0x0276 Table 73: Tx SYNTHESIZER: Force ALC
tx_synth_force_vco_tune_0	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d631_0x0277 Table 73: Tx SYNTHESIZER: Force VCO Tune 0
tx_synth_force_vco_tune_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d632_0x0278 Table 73: Tx SYNTHESIZER: Force VCO Tune 1
tx_synth_alcvaract_or	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d633_0x0279 Table 73: Tx SYNTHESIZER: ALC/Varactor
tx_synth_vco_output	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d634_0x027a Table 73: Tx SYNTHESIZER: VCO Output
tx_synth_cp_current	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d635_0x027b Table 73: Tx SYNTHESIZER: CP Current
tx_synth_cp_offset	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d636_0x027c Table 73: Tx SYNTHESIZER: CP Offset
tx_synth_cp_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d637_0x027d Table 73: Tx SYNTHESIZER: CP Config
tx_synth_loop_filter_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d638_0x027e Table 73: Tx SYNTHESIZER: Loop Filter 1
tx_synth_loop_filter_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d639_0x027f Table 73: Tx SYNTHESIZER: Loop Filter 2
tx_synth_loop_filter_3	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d640_0x0280 Table 73: Tx SYNTHESIZER: Loop Filter 3
tx_synth_dithercp_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d641_0x0281 Table 73: Tx SYNTHESIZER: Dither/CP Cal
tx_synth_vco_bias_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d642_0x0282 Table 73: Tx SYNTHESIZER: VCO Bias 1
tx_synth_mustbe0x0d	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d643_0x0283 Table 73: Tx SYNTHESIZER: Must be 0x0D
tx_synth_cal_status	uchar	-	-	Volatile	-	-	reg_addr_d644_0x0284 Table 73: Tx SYNTHESIZER: Cal Status
tx_synth_mustbe0x00	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d645_0x0285 Table 73: Tx SYNTHESIZER: Must be 0x00
tx_synth_mustbe0x02	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d646_0x0286 Table 73: Tx SYNTHESIZER: Set to 0x02 (Must be 0x02)
tx_synth_cp_overrange_vco_lock	uchar	-	-	Volatile	-	-	reg_addr_d647_0x0287 Table 73: Tx SYNTHESIZER: CP Over Range/VCO Lock
tx_synth_mustbe0x0b	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d648_0x0288 Table 73: Tx SYNTHESIZER: Set to 0x0B (Must be 0x0B)
tx_synth_vco_cal	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d649_0x0289 Table 73: Tx SYNTHESIZER: VCO Cal
tx_synth_lock_detect_config	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d650_0x028a Table 73: Tx SYNTEHSIZER: Lock Detect Config
tx_synth_mustbe0x17	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d651_0x028b Table 73: Tx SYNTEHSIZER: Must be 0x17
tx_synth_mustbe0x00_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d652_0x028c Table 73: Tx SYNTEHSIZER: Must be 0x00
tx_synth_mustbe0x00_also_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d653_0x028d Table 73: Tx SYNTEHSIZER: Must be 0x00

ocpi_pad_28e	uchar	-	-		-	-	-
tx_synth_mustbe0x70	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d656_0x0290 Table 73: Tx SYNTEHSIZER: Set to 0x70 (Must be 0x70)
tx_synth_vco_varactor_ctrl_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d657_0x0291 Table 73: Tx SYNTEHSIZER: VCO Varactor Control 1
dcxo_coarse_tune	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d658_0x0292 Table 74: DCXO: DCXO Coarse Tune
dcxo_fine_tune_high	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d659_0x0293 Table 74: DCXO: DCXO Fine Tune2
dcxo_fine_tune_low	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d660_0x0294 Table 74: DCXO: DCXO Fine Tune1
ocpi_pad_295	uchar	-	-		-	-	-
tx_fast_lock_setup	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d666_0x029a Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Setup
tx_fast_lock_setup_init_delay	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d667_0x029b Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Setup Init Delay
tx_fast_lock_program_addr	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d668_0x029c Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Addr
tx_fast_lock_program_data	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d669_0x029d Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Data
tx_fast_lock_program_read	uchar	-	-	Volatile	-	-	reg_addr_d670_0x029e Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Read
tx_fast_lock_program_ctrl	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d671_0x029f Table 65: Tx SYNTH FAST LOCK: Tx Fast Lock Program Ctrl
ocpi_pad_2a0	uchar	-	-		-	-	-
tx_lo_gen_power_mode	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d673_0x02a1 Table 76: Tx LO GENERATION: Tx LO Gen Power Mode
ocpi_pad_2a2	uchar	-	-		-	-	-
bandgap_mustbe0x0e	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d678_0x02a6 Table 77: MASTER BIAS AND BANDGAP CONFIGURATION: Set to 0x0E (Must be 0x0E)
ocpi_pad_2a7	uchar	-	-		-	-	-
bandgap_mustbe0x0e_also	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d680_0x02a8 Table 77: MASTER BIAS AND BANDGAP CONFIGURATION: Set to 0x0E (Must be 0x0E)
ocpi_pad_2a9	uchar	-	-		-	-	-
ref_divide_config_1	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d683_0x02ab Table 78: REFERENCE DIVIDER: Ref Divide Config 1
ref_divide_config_2	uchar	-	-	Volatile, Writeable	-	-	reg_addr_d684_0x02ac Table 78: REFERENCE DIVIDER: Ref Divide Config 2
ocpi_pad_2ad	uchar	-	-		-	-	-
gain_readback_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d688_0x02b0 Table 80: Rx GAIN READ BACK: Gain Rx1
gain_readback_lpf_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d689_0x02b1 Table 80: Rx GAIN READ BACK: LPF Gain Rx1
gain_readback_dig_gain_rx1	uchar	-	-	Volatile	-	-	reg_addr_d690_0x02b2 Table 80: Rx GAIN READ BACK: Dig gain Rx1

gain_readback_fast_attack_state	uchar	-	-	Volatile	-	-	reg_addr_d691_0x02b3 Table 80: Rx GAIN READ BACK: Fast Attack State
gain_readback_slow_loop_state	uchar	-	-	Volatile	-	-	reg_addr_d692_0x02b4 Table 80: Rx GAIN READ BACK: Slow Loop State
gain_readback_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d693_0x02b5 Table 80: Rx GAIN READ BACK: Gain Rx2
gain_readback_lpf_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d694_0x02b6 Table 80: Rx GAIN READ BACK: LPF Gain Rx2
gain_readback_dig_gain_rx2	uchar	-	-	Volatile	-	-	reg_addr_d695_0x02b7 Table 80: Rx GAIN READ BACK: Dig Gain Rx2
gain_readback_ovrg_sigs_rx1	uchar	-	-	Volatile	-	-	reg_addr_d696_0x02b8 Table 80: Rx GAIN READ BACK: Ovrg Sigs Rx1
gain_readback_ovrg_sigs_rx2	uchar	-	-	Volatile	-	-	reg_addr_d697_0x02b9 Table 80: Rx GAIN READ BACK: Ovrg Sigs Rx2
ocpi_pad_2ba	uchar	-	-		-	-	-
ctrl	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d991_0x03df Table 83: CONTROL: Control
ocpi_pad_3e0	uchar	-	-		-	-	-
test_bist_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d1012_0x03f4 Table 84: DIGITAL TEST: BIST Config
test_observe_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d1013_0x03f5 Table 84: DIGITAL TEST: Observe Config
test_bist_and_data_port_test_config	uchar	-	-	Volatile, Write-able	-	-	reg_addr_d1014_0x03f6 Table 84: DIGITAL TEST: BIST and Data Port Test Config
pin_control_p	bool	-	-	Parameter	-	-	Whether RX/TX powerdown via pin control is possible.

15 Appendix - Vivado Timing Analysis

The Vivado timing report that OpenCPI runs for device workers may erroneously report a max delay for a clocking path which should have been ignored. Custom Vivado tcl commands had to be run for this device worker to extract pertinent information from Vivado timing analysis. After building the worker, the following commands were run from the assets project directory (after the Vivado settings64.sh was sourced):

```
cd hdl/devices/
vivado -mode tcl
```

Then the following commands were run inside the Vivado tcl terminal:

```
open_project ad9361_config.hdl/target-zynq/ad9361_config_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_config_rv -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets {ctl_in[Clk]}]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
```

The following is the output of the timing report. The Fmax for the control plane clock for this worker is computed as the maximum magnitude slack with a control plane clock of 1 ps plus 2 times the assumed 1 ps control plane clock period (3.135 ns + 0.002 ns = 3.137 ns, 1/3.137 ns = 318.78 MHz).

```
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk1


Timing Report


Slack (VIOLATED) :     -3.135ns (required time - arrival time)
 Source:               wci/wci_decode/my_state_r_reg[2]/C
                         (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
 Destination:          wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
                         (rising edge-triggered cell FDSE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
 Path Group:           clk1
 Path Type:            Setup (Max at Slow Process Corner)
 Requirement:          0.002ns (clk1 rise@0.002ns - clk1 rise@0.000ns)
 Data Path Delay:      2.884ns (logic 0.937ns (32.490%) route 1.947ns (67.510%))
 Logic Levels:         2  (LUT6=2)
 Clock Path Skew:      -0.049ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
   Source Clock Delay    (SCD):   0.973ns
   Clock Pessimism Removal (CPR): 0.000ns
 Clock Uncertainty:    0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter  (TSJ):   0.071ns
   Total Input Jitter   (TIJ):   0.000ns
   Discrete Jitter       (DJ):   0.000ns
   Phase Error           (PE):   0.000ns
```

```
  Location           Delay type              Incr(ns) Path(ns)   Netlist Resource(s)
-------------------------------------------------------------------- -------------------
                     (clock clk1 rise edge)    0.000    0.000 r
                                               0.000    0.000 r ctl_in[Clk] (IN)
                     net (fo=66, unset)        0.973    0.973   wci/wci_decode/ctl_in[Clk]
                     FDRE                                   r  wci/wci_decode/my_state_r_reg[2]/C
-------------------------------------------------------------------- -------------------
                     FDRE (Prop_fdre_C_Q)      0.518    1.491 r wci/wci_decode/my_state_r_reg[2]/Q
                     net (fo=5, unplaced)      0.993    2.484   wci/wci_decode/wci_state[2]
                                                        r  wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/I0
                     LUT6 (Prop_lut6_I0_O)     0.295    2.779 r wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/O
                     net (fo=4, unplaced)      0.443    3.222   wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2_n_0
                                                        r  wci/wci_decode/FSM_onehot_my_access_r[4]_i_1/I2
                     LUT6 (Prop_lut6_I2_O)     0.124    3.346 r wci/wci_decode/FSM_onehot_my_access_r[4]_i_1/O
                     net (fo=8, unplaced)      0.511    3.857   wci/wci_decode/my_access_r
                     FDSE                                   r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
-------------------------------------------------------------------- -------------------


                     (clock clk1 rise edge)    0.002    0.002 r
                                               0.000    0.002 r ctl_in[Clk] (IN)
                     net (fo=66, unset)        0.924    0.926   wci/wci_decode/ctl_in[Clk]
                     FDSE                                   r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/C
                     clock pessimism           0.000    0.926
                     clock uncertainty        -0.035    0.891
                     FDSE (Setup_fdse_C_CE)   -0.169    0.722   wci/wci_decode/FSM_onehot_my_access_r_reg[0]
-------------------------------------------------------------------
                     required time                      0.722
                     arrival time                      -3.857
-------------------------------------------------------------------
                     slack                             -3.135




report_timing: Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 2093.707 ; gain = 496.523 ; free physical = 13626 ; free virtual = 87791
```