Summary - CIC Decimator (TimeStamped)

Name	cic_dec_ts
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets_ts.components
Workers	cic_dec_ts.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The CIC decimator has `N` cascaded integrator stages with an input data rate of f_s, followed by a rate change by a factor `R`, followed by `N` cascaded comb stages with an output data rate of $\frac{f_s}{R}$. The differential delay, `M`, affects the slope of the transition region. Figure 1 diagrams the decimating CIC filter.

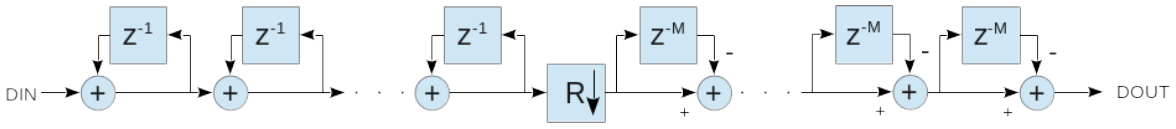

Figure 1: Cascaded Integration Comb Decimation filter Block Diagram

Worker Implementation Details

cic_dec_ts.hdl

Number of Stages

The generic `N` sets the number of integrators and comb stages in the filter. Increasing the number of stages increases the attenuation in the sidelobes and decreases the 3dB bandwidth of the passband. The recommended range for this parameter is 3 to 6. Consult the reference material for an in depth discussion of the frequency response of the filter as a function of the generics in this module.

Bit Growth

For this design, the output data width for the comb stages is configurable via `ACC_WIDTH`. To adjust for bit growth in the data path and to ensure no quantization error at the output, this equation should be used to determine the value of `ACC_WIDTH`.

$$ACC\_WIDTH = N * CEIL(log_2(R * M)) + DIN\_WIDTH \tag{1}$$

Theory

A CIC filter is comprised of `N` integrator sections cascaded together with `N` comb sections. Combining the transfer functions for all sections results in the system response function seen in Equation 2. Note that the filter has zeros at integer multiples of $\frac{f_s}{RM}$ Hz.

$$H(z) = \Big[H_{int}(z)\Big]^N \Big[H_{comb}(z)\Big]^N = \Big[\frac{1}{(1-z^{-1})^N}\Big]\Big[(1-z^{-RM})^N\Big] = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \tag{2}$$

Block Diagrams

Top level

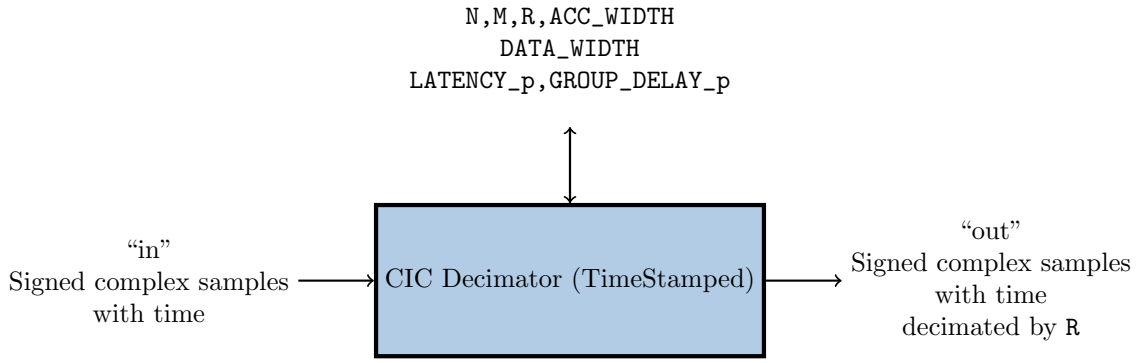

Figure 2: Top Level Block Diagram

Source Dependencies

cic_dec_ts.hdl

- assets_ts/components/cic_dec_ts.hdl/cic_dec_ts.vhd
- assets_ts/components/cic_dec_ts.hdl/cic_dec_gen2.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
N	UChar	-	-	Parameter	-	3	Number of Stages
M	UChar	-	-	Parameter	-	1	Differential Delay
R	UShort	-	-	Parameter	-	4	Decimation Factor
ACC_WIDTH	UChar	-	-	Parameter	-	-	Accumulation Width *(2)
DATA_WIDTH	UChar	-	-	Readable	-	16	Data width

Worker Properties

cic_dec_ts.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	LATENCY_p	Ushort	-	-	Parameter	-	1	Number of clock cycles between a valid input and a valid output
Property	GROUP_DELAY_p	Ushort	-	-	Parameter	-	(N+1)*R	Number of valid inputs before a valid output is given

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	False	Complex_Short_With_Metadata	False	-	Complex signed samples with time
out	True	Complex_Short_With_Metadata	False	-	Complex signed samples with time

Worker Interfaces

cic_dec_ts.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32		Complex signed samples with time
StreamInterface	out	32	insertEOM=true, workerEOF='true'	Complex signed samples with time

Control Timing and Signals

The CIC Dec worker uses the clock from the Control Plane and standard Control Plane signals.

Worker Configuration Parameters

cic_dec_ts.hdl

Table 1: Table of Worker Configurations for worker: cic_dec_ts

Configuration	M	N	R	ACC_WIDTH
0	1	3	8	25

Performance and Resource Utilization

cic_dec_ts.hdl

Table 2: Resource Utilization Table for worker "cic_dec_ts"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	N/A	753	623	N/A	N/A
0	zynq_ise	ISE	14.7	7z010clg400-3	748	1007	327.437	N/A
0	virtex6	ISE	14.7	6vcx75tff484-2	748	1021	258.419	N/A
0	zynq	Vivado	2017.1	xc7z020clg400-3	760	684	N/A	N/A

Test and Verification

Two test cases are implemented to validate the CIC Decimator component:

1. Unity gain response to DC: The CIC Decimator gain is calculated using the following equation:

$$CIC\ Gain = \frac{(R * M)^N}{2^{CEIL(N * log_2(R * M))}} \tag{3}$$

2. Tone waveform: A waveform containing tones at 50 Hz, 100 Hz and Fs/R sampled at 1024000 is processed by the worker. The tones at 50 Hz and 100 Hz are within the bandwidth of the filter, while the Fs/R tone is at the first null. The power levels of the input tones and output tones are measured and compared.

In both of the test cases, the samples data is interleaved with all of the operations of the Complex_Short_With_Metadata protocol in the following sequence:

1. Interval
2. Sync (this opcode is expected after an Interval operation)
3. Time
4. Samples
5. Flush
6. Samples
7. Sync
8. Samples

References

(1) Ronald E. Crochiere and Lawrence R. Rabiner. Multirate Digital Signal Processing. Prentice-Hall Signal Processing Series. Prentice Hall, Englewood Cli_s, 1983.
(2) Eugene B. Hogenauer, An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, April 1981.
(3) Matthew P. Donadio, CIC Filter Introduction, http://home.mit.bme.hu/ kollar/papers/cic.pdf