Summary - ML605 Platform

Name	ml605
Worker Type	Platform
Version	v1.4
Release Date	October 2018
Component Library	ocpi
Workers	ml605.hdl

Functionality

The ML605 platform worker provides an interface between a PCIe-connected processor and the Virtex-6 FPGA on the ML605 board. It makes connections over a PCIe bus for OpenCPI control and data planes. It also provides a 200 MHz clock source for the timebase port and a 125 MHz clock source for the control plane.

Worker Implementation Details

The ML605 platform worker instantiates version 1.7 of the Xilinx LogiCORE IP Virtex-6 FPGA Integrated Block for PCI Express. This Integrated Block is compatible with the PCI Express Card Electromechanical v2.0 and PCI Industrial Computer Manufacturers Group 3.4 specifications. The 4-lane Gen1/Gen2 implementation is used. The intended clock source frequency is 250 MHz. For detailed information of the LogiCORE functionality and usage, refer to Xilinx UG715 and Xilinx DS517. Figure 1 diagrams the intra-worker functionality of the ml605 platform worker.

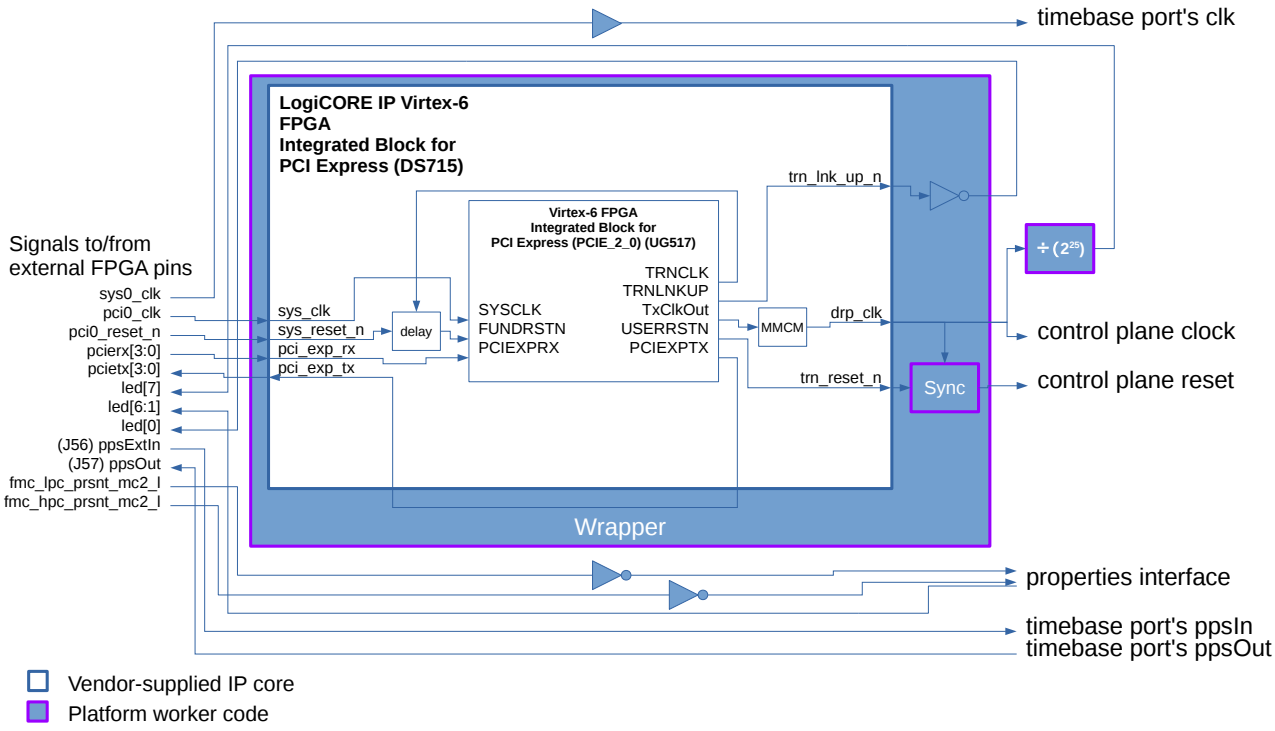


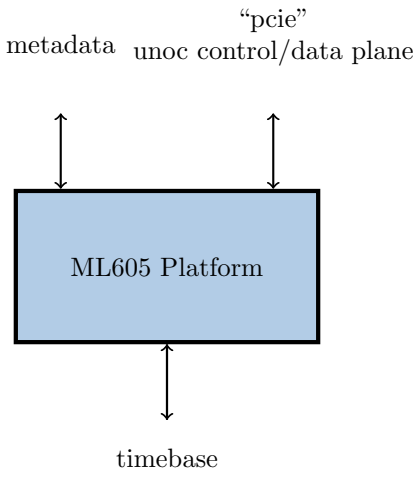
Figure 1: ml605 Functional Diagram

Theory

Because there are no data processing algorithms implemented in this worker, no corresponding data processing theory is relevant herein.

Block Diagrams

Top level



State Machines

No state machines exist within the platform worker outside of those within the PCIe LogiCORE IP block. It is not intended for users of LogiCORE IP blocks to understand their inner functionality.

Source Dependencies

- assets/hdl/platforms/ml605/ml605.vhd
- assets/hdl/platforms/ml605/pci_ml605.v
- assets/hdl/platforms/ml605/ml605_pkg.vhd
- assets/hdl/primitives/virtex6/xilinx_v6_pcie_wrapper.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/gtx_drp_chanalign_fix_3752_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/gtx_rx_valid_filter_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/gtx_tx_sync_rate_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/gtx_wrapper_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/Makefile
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_2_0_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_brams_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_bram_top_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_bram_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_clocking_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_gtx_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_pipe_lane_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_pipe_misc_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_pipe_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_reset_delay_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/pcie_upconfig_fix_3451_v6.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/v6_pcie_v1_7_bb.v
- assets/hdl/primitives/pcie_4243_trn_v6_gtx_x4_250/v6_pcie_v1_7.v

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
platform	String	31	-	Parameter	Standard	-	Name of this platform
sdp_width	UChar	-	-	Parameter	Standard	1	Width of data plane in DWORDS
UUID	ULong	-	16	Readable	Standard	-	UUID of this platform
oldtime	ULongLong	-	-	Padding	Standard	-	N/A
romAddr	UShort	-	-	Writable	Standard	-	
romData	ULong	-	-	Volatile	Standard	-	
nSwitches	ULong	-	-	Readable	Standard	-	Number of switches
nLEDs	ULong	-	-	Readable	Standard	-	Number of LEDs
memories_length	ULong	-	-	Readable	Standard	-	
memories	ULong	-	4	Readable	Standard	-	The memory regions that may be used by various other elements, which indicates aliasing etc. The values describing each region are: Bit 31:28 - External bus/BAR connected to this memory (0 is none) Bit 27:14 - Offset in bus/BAR of this memory (4KB units) Bit 13:0 - Size of this memory (4KB units) units)
dna	ULongLong	-	-	Readable	Standard	-	DNA (unique chip serial number) of this platform
switches	ULong	-	-	Volatile	Standard	-	Current value of any switches in the platform
LEDS	ULong	-	-	Writable, Readable	Standard	-	Setting of LEDs in the platform, with readback. A value of true illuminates the given LED. The indices and their corresponding LEDs are index 12: LED DS17, 11: DS18, 10: DS20, 9: DS19, 8: DS16, 7: unused, 6: DS22, 5: DS15, 4: DS13, 3: DS10, 2: DS9, 1: DS11, 0: unused. For example, writing a value of 0x1002 will illuminate only LEDs DS17 and DS11.
nSlots	ULong	-	-	Parameter	Standard	0	Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property.
slotNames	String	32	-	Parameter	Standard	""	A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property.
pci_device_id	Enum	-	-	Parameter	unknown, ml605, alst4, alst4x	unknown	PCI Device ID for PCI devices. This is essentially the "registry" of PCI device IDs. New platforms can use "unknown" before they are registered.
slotCardIsPresent	Bool	-	64	Volatile	Standard	-	An array of booleans, where each index contains an indication whether a card is physically present in the given index's slot. For a description of a given index's slot, see the corresponding comma-separated string contents in the slotName property. Note that only the first min(nSlots,64) of the 64 indices contain pertinent information.

Worker Properties

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
SpecProperty	`platform`	String	31	-	Parameter	Standard	ml605	Name of this platform
SpecProperty	`nSlots`	ULong	-	-	Parameter	Standard	2	Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property.
SpecProperty	`slotNames`	String	32	-	Parameter	Standard	fmc_lpc,fmc_hpc	A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property.
SpecProperty	`pci_device_id`	Enum	-	-	Parameter	unknown, ml605, alst4, alst4x	ml605	PCI Device ID for PCI devices. This is essentially the "registry" of PCI device IDs. New platforms can use "unknown" before they are registered.
Property	`pciId`	UShort	-	-	Volatile	Standard	-	
Property	`unocDropCount`	UChar	-	-	Volatile	Standard	-	Invalid packets collected at uNOC terminator

Component Ports

No ports are implemented for the given component specification.

Worker Interfaces

Type	Name	Master	Count	Usage
metadata	-	true	-	Access to container metadata via the platform worker. All platform workers must provide this port.
timebase	-	true	-	Providing a timebase for the time service. All platform workers must provide this port.
unoc	pcie	true	-	This platform worker provides a control/data plane called "pcie".

Platform Devices

The following is a table which enumerates which device workers are allowed in platform configurations and in assembly containers. The parameter values specified restrict allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

Name	Property Name	Property Value	Worker Signal	Platform Signal
time_server	frequency	$200*10^6$		
flash				

Signals

Note that this signal table does not include signals that may be provided by slots.

Name	Type	Differential	Width	Description
sys0_clk	Input	true	1	200 MHz clock which is sent to the timebase port.
sys1_clk	Input	true	1	GBE clock (unused).
pci0_clk	Input	true	1	250 MHz clock which is sent to the LogiCORE PCIE block.
pci0_reset_n	Input	false	1	PCIe reset.
pcie_rx	Input	true	4	PCIe RX.
pcie_tx	Output	true	4	PCIe TX.
led	Output	false	13	led[12:8] drive the LEDs labelled DS17, DS18, DS20, DS19, and DS16 in the schematic, respectively. led[7:0] drive the LEDs labelled DS21, DS22, DS14, DS15, DS10, DS9, DS11, DS12 in the schematic, respectively. led[12:8] and led[6:1] are driven by the 12:8 and 6:1 indices of the LEDS property. led[7] is driven by the PCIE-generated control plane clock divided by 2^{25} and led[0] is driven by the PCIE link up indicator. A high voltage on these signals illuminates their respective LEDs.
ppsExtIn	Input	false	1	This signal is driven by external hardware connected to the ML605 board's J56 SMA connector. The purpose of this signal is to provide a PPS clock source to the worker connected to the timebase port. Note that said worker may or may not use this signal.
ppsOut	Output	false	1	The worker connected to the timebase port drives this signal, which is connected to the J57 SMA connector. The purpose of this signal is for said worker to output the PPS signal it produces. Note that said worker may use a variety of clock sources to produce its PPS, not necessarily the corresponding ppsExtIn signal.
fmc_lpc_prsnt_mc2_l	Input	false	1	Connected to the PRSNTn signal of the FMC LPC slot. (Device workers may not ingest the FMC HPC PRSNTn signal). This active-low signal provides FMC LPC mezzanine card presence indication to index 0 of the slotCardIsPresent property.
fmc_hpc_prsnt_mc2_l	Input	false	1	Connected to the PRSNTn signal of the FMC HPC slot. (Device workers may not ingest the FMC HPC PRSNTn signal). This active-low signal provides FMC HPC mezzanine card presence indication to index 1 of the slotCardIsPresent property.

Slots

The following table enumerates the available slots for this platform and the signals they include. Note that the signals listed are only those who are unconnected on the platform or whose platform signal name do not match the slot signal name.

Name	Type	Slot Signal	Platform Signal
FMC_LPC	fmc_lpc	LA00_P_CC	FMC_LPC_LA00_CC_P
		LA00_P_CC	FMC_LPC_LA00_CC_P
		LA00_N_CC	FMC_LPC_LA00_CC_N
		LA01_P_CC	FMC_LPC_LA01_CC_P
		LA01_N_CC	FMC_LPC_LA01_CC_N
		LA17_P_CC	FMC_LPC_LA17_CC_P
		LA17_N_CC	FMC_LPC_LA17_CC_N
		DP0_C2M_P	-
		DP0_C2M_N	-
		DP0_M2C_P	-
		DP0_M2C_N	-
		LA18_P_CC	FMC_LPC_LA18_CC_P
		LA18_N_CC	FMC_LPC_LA18_CC_N
		SCL	FMC_LPC_IIC_SCL_LS
		SDA	FMC_LPC_IIC_SDA_LS
FMC_HPC	fmc_hpc	LA00_P_CC	FMC_HPC_LA00_CC_P
		LA00_N_CC	FMC_HPC_LA00_CC_N
		LA01_P_CC	FMC_HPC_LA01_CC_P
		LA01_N_CC	FMC_HPC_LA01_CC_N
		LA17_P_CC	FMC_HPC_LA17_CC_P
		LA17_N_CC	FMC_HPC_LA17_CC_N
		DP0_C2M_P	-
		DP0_C2M_N	-
		DP0_M2C_P	-
		DP0_M2C_N	-
		LA18_P_CC	FMC_HPC_LA18_CC_P
		LA18_N_CC	FMC_HPC_LA18_CC_N
		DP9_M2C_P	-
		DP9_M2C_N	-
		DP8_M2C_P	-
		DP8_M2C_N	-
		DP7_M2C_P	-
		DP7_M2C_N	-
		DP6_M2C_P	-
		DP6_M2C_N	-
		DP9_C2M_P	-
		DP9_C2M_N	-
		DP8_C2M_P	-
		DP8_C2M_N	-
		DP7_C2M_P	-
		DP7_C2M_N	-
		DP6_C2M_P	-
		DP6_C2M_N	-
		DP1_M2C_P	-
		DP1_M2C_N	-
		DP2_M2C_P	-
		DP2_M2C_N	-
		DP3_M2C_P	-
		DP3_M2C_N	-
		DP4_M2C_P	-

		DP4_M2C_N	-
		DP5_M2C_P	-
		DP5_M2C_N	-
		DP1_C2M_P	-
		DP1_C2M_N	-
		DP2_C2M_P	-
		DP2_C2M_N	-
		DP3_C2M_P	-
		DP3_C2M_N	-
		DP4_C2M_P	-
		DP4_C2M_N	-
		DP5_C2M_P	-
		DP5_C2M_N	-
		HA00_P_CC	HA00_CC_P
		HA00_N_CC	HA00_CC_N
		HA01_P_CC	HA01_CC_P
		HA01_N_CC	HA01_CC_N
		HA17_P_CC	HA17_CC_P
		HA17_N_CC	HA17_CC_N
		HB00_P_CC	HB00_CC_P
		HB00_N_CC	HB00_CC_N
		HB06_P_CC	HB06_CC_P
		HB06_N_CC	HB06_CC_N
		HB17_P_CC	HB17_CC_P
		HB17_N_CC	HB17_CC_N
		PG_M2C	PG_M2C_LS
		SCL	IIC_SCL_LS
		SDA	IIC_SDA_LS

Platform Configurations

Name	Platform Configuration Workers	Card	Slot
base	ml605	-	-
	time_server	-	-
ml605_flash	ml605	-	-
	time_server	-	-
	flash	-	-
ml605_zipper_fmc_lpc_rx_tx	ml605	-	-
	time_server	-	-
	lime_adc	lime_zipper_fmc_lpc	fmc_lpc
	lime_dac	lime_zipper_fmc_lpc	fmc_lpc
	si5351	lime_zipper_fmc_lpc	fmc_lpc
	lime_rx	lime_zipper_fmc_lpc	fmc_lpc
	lime_tx	lime_zipper_fmc_lpc	fmc_lpc
ml605_zipper_fmc_lpc_rx	ml605	-	-
	time_server	-	-
	lime_adc	lime_zipper_fmc_lpc	fmc_lpc
	si5351	lime_zipper_fmc_lpc	fmc_lpc
	lime_rx	lime_zipper_fmc_lpc	fmc_lpc
ml605_zipper_fmc_lpc_tx	ml605	-	-
	time_server	-	-
	lime_dac	lime_zipper_fmc_lpc	fmc_lpc
	si5351	lime_zipper_fmc_lpc	fmc_lpc
	lime_tx	lime_zipper_fmc_lpc	fmc_lpc
ml605_zipper_fmc_hpc_rx_tx	ml605	-	-
	time_server	-	-
	lime_adc	lime_zipper_fmc_hpc	fmc_hpc
	lime_dac	lime_zipper_fmc_hpc	fmc_hpc
	si5351	lime_zipper_fmc_hpc	fmc_hpc
	lime_rx	lime_zipper_fmc_hpc	fmc_hpc
	lime_tx	lime_zipper_fmc_hpc	fmc_hpc
ml605_zipper_fmc_hpc_rx	ml605	-	-
	time_server	-	-
	lime_adc	lime_zipper_fmc_hpc	fmc_hpc
	si5351	lime_zipper_fmc_hpc	fmc_hpc
	lime_rx	lime_zipper_fmc_hpc	fmc_hpc
ml605_zipper_fmc_hpc_tx	ml605	-	-
	time_server	-	-
	lime_dac	lime_zipper_fmc_hpc	fmc_hpc
	si5351	lime_zipper_fmc_hpc	fmc_hpc
	lime_tx	lime_zipper_fmc_hpc	fmc_hpc

Control Timing and Signals

There are 3 clock domains present in the ml605 platform worker: 250 MHz, 125 MHz, and 200 MHz. The worker ingests an external-to-the FPGA 250 MHz clock. This clock serves as the clock source for the LogiCORE PCIe Integrated Block within the worker. The LogiCORE block divides the 250 MHz clock down to a 125 MHz clock which is subsequently supplied to the control plane as its clock. The worker also feeds a buffered version of the external-to-the-FPGA 200 MHz clock to the timebase port. The timebase port is also supplied with a PPS from the ML605 board's J56 SMA connector. The timebase port also include a PPS output which is fed to the J57 SMA connector.

Performance and Resource Utilization

In the following Platform Worker Utilization tables, the Worker Build Configuration "0" refers to the Platform Worker itself. Named configurations refer to platform configurations (*e.g.* they may include other device workers along with the Platform Worker).

Table 2: Resource Utilization Table for hdl-platform: ml605

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
base	virtex6	ISE	14.7	6vcx75tff484-2	2414	3079	288.476	RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_0rx_1tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	2921	3915	288.476	ODDR: 8 RAM64M: 8 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_0rx_1tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	2921	3915	288.476	ODDR: 8 RAM64M: 8 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_0rx_2tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3175	4286	288.476	ODDR: 8 RAM64M: 16 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_0rx_2tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3175	4286	288.476	ODDR: 8 RAM64M: 16 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_0tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	2929	3852	288.476	ODDR: 1 RAM64M: 8 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_0tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	2929	3852	288.476	ODDR: 1 RAM64M: 8 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_1tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3284	4336	288.476	ODDR: 8 RAM64M: 16 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_1tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3284	4336	288.476	ODDR: 8 RAM64M: 16 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_2tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3538	4707	288.476	ODDR: 8 RAM64M: 24 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_1rx_2tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3538	4707	288.476	ODDR: 8 RAM64M: 24 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7

cfg_2rx_0tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3137	4110	288.476	ODDR: 1 RAM64M: 16 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_2rx_0tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3137	4110	288.476	ODDR: 1 RAM64M: 16 BUFR: 2 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_2rx_1tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3492	4594	288.476	ODDR: 8 RAM64M: 24 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_2rx_1tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3492	4594	288.476	ODDR: 8 RAM64M: 24 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_2rx_2tx_fmcomms_2_3_hpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3746	4965	288.476	ODDR: 8 RAM64M: 32 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
cfg_2rx_2tx_fmcomms_2_3_lpc_lvds	virtex6	ISE	14.7	6vcx75tff484-2	3746	4965	288.476	ODDR: 8 RAM64M: 32 BUFR: 3 RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
ml605_flash	virtex6	ISE	14.7	6vcx75tff484-2	2415	3080	288.476	RAMB36E1: 8 BUFG: 7 BUFGCTRL: 7
ml605_lime_tx	virtex6	ISE	14.7	6vcx75tff484-2	2748	3708	288.476	RAM64M: 8 RAMB36E1: 8 BUFG: 8 BUFGCTRL: 8
ml605_zipper_fmc_hpc_rx	virtex6	ISE	14.7	6vcx75tff484-2	2910	4024	288.476	RAMB36E1: 11 BUFG: 8 BUFGCTRL: 8
ml605_zipper_fmc_hpc_rx_tx	virtex6	ISE	14.7	6vcx75tff484-2	3222	4547	288.476	RAM64M: 8 RAMB36E1: 11 BUFG: 9 BUFGCTRL: 9
ml605_zipper_fmc_hpc_tx	virtex6	ISE	14.7	6vcx75tff484-2	2900	4188	288.476	RAM64M: 8 RAMB36E1: 8 BUFG: 8 BUFGCTRL: 8
ml605_zipper_fmc_lpc_rx	virtex6	ISE	14.7	6vcx75tff484-2	2910	4024	288.476	RAMB36E1: 11 BUFG: 8 BUFGCTRL: 8
ml605_zipper_fmc_lpc_rx_tx	virtex6	ISE	14.7	6vcx75tff484-2	3222	4547	288.476	RAM64M: 8 RAMB36E1: 11 BUFG: 9 BUFGCTRL: 9
ml605_zipper_fmc_lpc_tx	virtex6	ISE	14.7	6vcx75tff484-2	2900	4188	288.476	RAM64M: 8 RAMB36E1: 8 BUFG: 8 BUFGCTRL: 8

Test and Verification

To be detailed in a future release.

References

1) Virtex-6 FPGA Integrated Block for PCI Express User Guide (DS715),
`https://www.xilinx.com/support/documentation/user_guides/v6_pcie_ug517.pdf`

2) LogiCORE IP Virtex-6 FPGA Integrated Block v1.7 for PCI Express (UG517),
`https://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ds715.pdf`