Summary - FIFO

Name	fifo
Worker Type	Application
Version	1.3
Release Date	February 2018
Component Library	ocpi.assets.util_comps
Workers	fifo.hdl
Tested Platforms	isim

Functionality

The FIFO component passes complex signed samples (Q0.15 I, Q0.15 Q) from the input port through a First-In-First-Out (FIFO) buffer and onward to the output port. The depth, in number of complex samples, of the FIFO buffer is parameterized. This component includes a property-driven oneshot mode which, when enabled, allows the first FIFO depth number of samples to be sent to the output port and then disables the output port. After the output port is disabled, the input port still ingests available samples, effectively operating as a data sink. This worker can also be parameterized to send a Zero-Length Message (ZLM) once the output port is disabled.

Worker Implementation Details

fifo.hdl

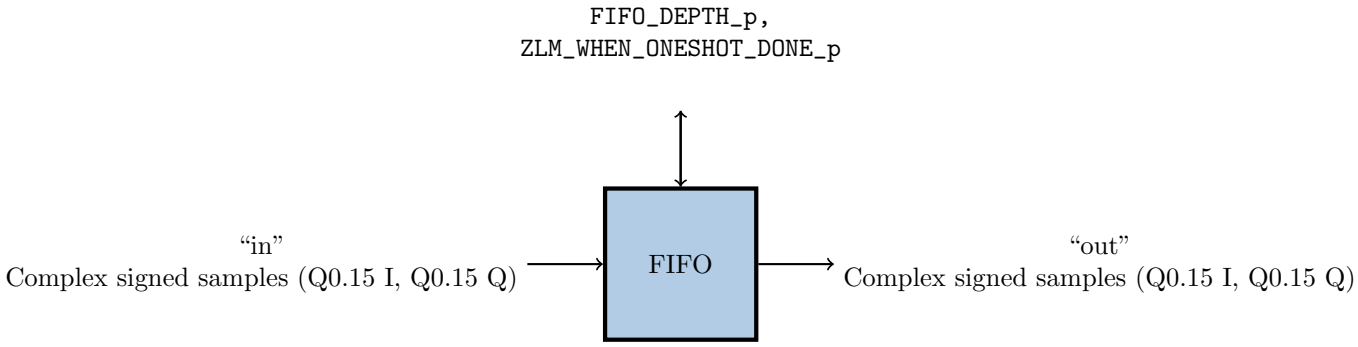
In keeping with good data flow control practices, backpressure is transferred, when necessary, from the output port to the input port. Backpressure is never transferred when in oneshot mode and after the output port is disabled. Backpressure from the output port and forwardpressure from the input port are both alleviated by the FIFO buffer, with the degree of alleviation being directly proportional to the parameterized depth of the FIFO buffer (`FIFO_DEPTH_p`).

The input port's SOM, EOM, byte_enable, and valid indicators are passed through the FIFO to the output port when it is enabled. Consequently, ZLMs will be passed through this worker. If operating in oneshot mode and the output port has been disabled, the EOM will be set (i.e. logic value of 1 applied) on the same clock pulse as the last output sample.

The `ZLM_WHEN_ONESHOT_DONE_p` parameter, when having a value of true, forces the worker to send a single ZLM when in oneshot mode and the output port has been disabled (i.e. when oneshot is 'done'). This is useful for allowing applications which use this worker to terminate once this worker's output port is disabled.

Block Diagrams

Top level



Source Dependencies

fifo.hdl

- ocpiassets/components/util_comps/fifo.hdl/fifo.vhd
- ocpi_base_project/hdl/primitives/bsv/bsv_pkg.vhd
  ocpi_base_project/hdl/primitives/bsv/imports/SizedFIFO.v

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
FIFO_DEPTH_p	ULong	-	-	Parameter	Standard	1024	Maximum number of complex samples which the FIFO can hold at any given time.
ZLM_WHEN_ONESHOT_DONE_p	Bool	-	-	Readable, Initial	Standard	False	When true, worker will generate Zero-Length-Message after oneshot was enabled and completed (should be used for simulation 'done' purposes only).

Worker Properties

fifo.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
-	-	-	-	-	-	-	-	-

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	iqstream_protocol	false	ZeroLengthMessages=true	Complex signed samples (Q0.15 I, Q0.15 Q). This port effectively becomes a data sink when oneshot is true and FIFO_DEPTH_p samples have been passed through this port. Note that input Zero-Length Messages will not be counted when using oneshot mode.
out	true	iqstream_protocol	false	ZeroLengthMessages=true	Complex signed samples (Q0.15 I, Q0.15 Q). This port will pass through all samples from the input port, while obeying and transferring backpressure. If oneshot is true and FIFO_DEPTH_p samples have been passed through this port, no more data will be passed through this port until a reset occurs. Note that Zero-Length Messages will not be counted when using oneshot mode.

Worker Interfaces

fifo.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	-	-
StreamInterface	out	32	-	-

Control Timing and Signals

The FIFO worker uses the clock from the Control Plane and standard Control Plane signals.

Performance and Resource Utilization

fifo.hdl

Worker Build Configuration "0":
Table entries are a result of building the worker with the following parameter sets:

- `ocpi_endian=little`
- `ocpi_debug=false`
- `ZLM_WHEN_ONESHOT_DONE_p=false`
- `FIFO_DEPTH_p=8192`

Table 1: Worker Build Configuration "0"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Functions
stratix4	Quartus	15.1.0	N/A	291	350	N/A	N/A
virtex6	ISE	14.7	6vcx75tff484-2	191	8044	255.582	RAM64Ms=1536
zynq	Vivado	2017.1	xc7z020clg400-3	373	7948	249.004	N/A
zynq_ise	ISE	14.7	7z010clg400-3	191	8028	307.390	RAM64Ms=1536

Worker Build Configuration "1":
Table entries are a result of building the worker with the following parameter sets:

- `ocpi_endian=little`
- `ocpi_debug=false`
- `ZLM_WHEN_ONESHOT_DONE_p=true`
- `FIFO_DEPTH_p=8192`

Table 2: Worker Build Configuration "1"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Functions
stratix4	Quartus	15.1.0	N/A	291	342	N/A	N/A
virtex6	ISE	14.7	6vcx75tff484-2	191	8034	253.615	RAM64Ms=1536
zynq	Vivado	2017.1	xc7z020clg400-3	372	7956	249.004	N/A
zynq_ise	ISE	14.7	7z010clg400-3	191	8031	307.390	RAM64Ms=1536

Test and Verification

For verification, multiple test files are generated of varying lengths. Each test file is passed into the input port, and the output of the output port is saved to a file. The output file is compared against the input file to make sure they have the same binary contents and length. For the tests that use oneshot mode, the output file is only compared to the first min(input file size,8192) samples, with 8192 hardcoded to correspond to `FIFO_DEPTH_p`.