Summary - AD9361 Config Proxy

Package Prefix	ocpi.assets.devices
Name	ad9361_config_proxy
Worker Type	Device Proxy
OpenCPI Release	v1.5 (released 4/2019)
Workers	ad9361_config_proxy.rcc
Slaves	ad9361_config.hdl
Tested Platforms	• Agilent Zedboard/Analog Devices FMCOMMS2 (xilinx13_3 RCC platform only) • Agilent Zedboard/Analog Devices FMCOMMS3 (xilinx13_3 RCC platform only) • x86/Xilinx ML605/Analog Devices FMCOMMS2 (centos7 RCC platform only) • x86/Xilinx ML605/Analog Devices FMCOMMS3 (centos7 RCC platform only) • Ettus E310 (xilinx13_4 RCC platform only)

Revision History

Revision	Description of Change	Date
v1.3	Initial release	8/2017
v1.4	• Worker updated to latest No-OS 2017_R1 release - `rx_rf_gain` default value removed from OCS as they conflicted with the default startup RX gain mode which is non-manual • Default value removed from `en_state_machine_mode` property to avoid confusion (state now handled by tx event port on ad9361_config.hdl)	10/2018
v1.5	• Added `digital_rx_block_delay` worker property • Updated new source dependencies	4/2019

Functionality

The AD9361 Config Proxy device worker proxy is a software wrapper for Analog Device's No-OS software library[2]. No-OS provides command and control of the AD9361 IC[4] via a high-level API which ultimately controls SPI writes to the AD9361 register set. In order to provide functionality analogous to the No-OS API, this worker provides a one-to-one mapping between the No-OS function calls and worker properties.

Worker Implementation Details

ad9361_config_proxy.rcc

The version of No-OS used was GitHub commit 06bfc76060d5b9767ae9aad7bf40e3648474ebb7[1], which was the latest update to the Analog Devices-recommended 2017_R1 release at the time of development.

No-OS features "platform layers" which are .c/.h files which implement hardware-specific SPI register accesses within generic API calls. No-OS includes several platform layers which are all specific to the Analog Devices HDL design[3]. In order to use No-OS with OpenCPI, a new platform layer was added within the ad9361_config_proxy.rcc code which provided OpenCPI-specific functionality for SPI accesses via slave device property read/writes. This new platform layer was implemented via the ad9361_platform.cc, ad9361_platform.h, and parameter.h files.

This worker implements every No-OS API call as a property, with the matching ad9361_get...()/ad9361_set...() API calls collapsed into a single volatile and writable ad9361_config_proxy.rcc property. Each property's type(s)/data structure(s) map directly to the type(s)/data structure(s) passed as argument(s) to that property's analogous No-OS function. The only exception to this methodology are:

- The No-OS ad9361_do_mcs() function is not implemented as a worker property since it performs a multi-chip-sync operation which could not yet be verified.
- The No-OS ad9361_set_rx_fir_config() / ad9361_get_rx_fir_config() and ad9361_set_tx_fir_config() / ad9361_get_tx_fir_config() functions are implemented as separate `rx_fir_config_write/rx_fir_config_read` and `tx_fir_config_write/tx_fir_config_read` properties, respectively, instead of collapsed into a single rx_fir_config and tx_fir_config properties due to the fact that the ...get...() calls ignore the ...path_clks and _bandwidth struct members, whereas the ..set..() calls do not. Consequently, in an attempt to avoid confusion by the end user, different structs were implemented for the write properties than were for the read properties.

The No-OS API calls often require passing integer values which, according to the No-OS documentation, are intended to correlate with C macros. For example, the No-OS ad9361_set_rx_fir_en_dis() function has a argument of type uint8_t, but the comments indicate its value should be one of the ENABLE or DISABLE ad9361_api.h integer macros:

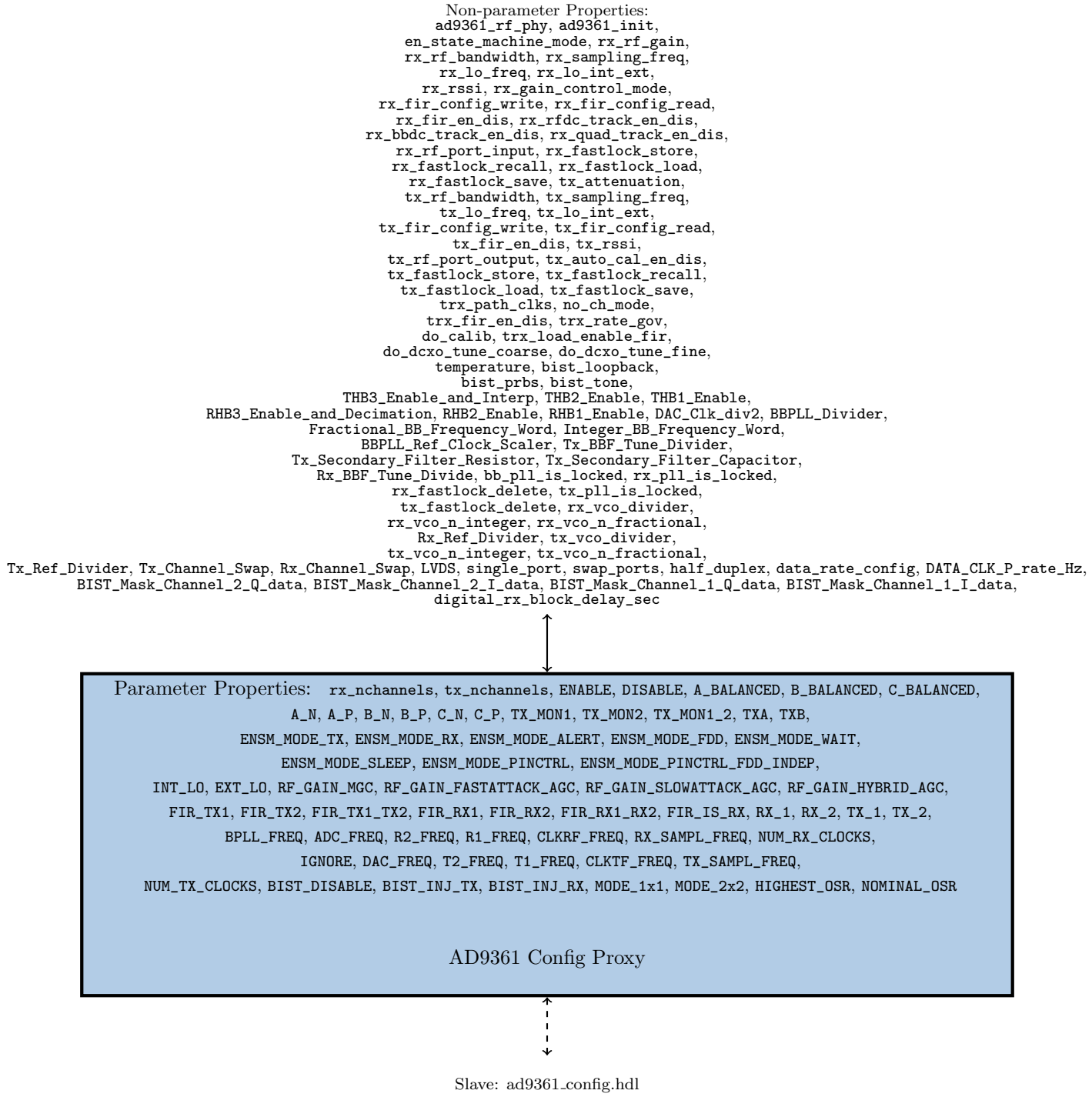
```
/**
 * Enable/disable the RX FIR filter.
 * @param phy The AD9361 current state structure.
 * @param en_dis The option (ENABLE, DISABLE).
 *               Accepted values:
 *                ENABLE (1)
 *                DISABLE (0)
 * @return 0 in case of success, negative error code otherwise.
 *
 * Note: This function will/may affect the data path.
 */
int32_t ad9361_set_rx_fir_en_dis (struct ad9361_rf_phy *phy,
                                  uint8_t en_dis)
```

Because a design decision was made to have a strict one-to-one mapping between No-OS API calls and ad9361_config_proxy.rcc properties, and because No-OS passes integers as arguments instead of forcing strictly enumerated types, this worker likewise uses integer types for properties instead of enumerated ones. To aid in alleviating confusion when using this worker's properties, many of the No-OS C macros are mapped to parameter properties of this worker and the property descriptions reference the parameter properties which are intended to be used. This way, parameter properties can be read at runtime, and the read values used to set a property. For example, the `ad9361_set_rx_fir_en_dis` property's description references the `ENABLE` and `DISABLE` parameter properties which have values of 1 and 0, respectively.

In addition to the worker's properties which map to No-OS API calls, other properties exist which provide further functionality. This includes PLL lock status, low-level PLL divider values which can be used to validate the LO frequencies read by No-OS, fastlock memory management (deletion), the FPGA data mode configuration (LVDS, CMOS, etc) via the `LVDS`, `single_port`, `swap_ports`, `half_duplex`, `data_rate_config` properties, and the

DATA_CLK_P_rate_Hz.

Note also that this worker's usage of no-OS not only makes SPI register accesses but also sets the AD9361 RESETB, ENABLE, and TXNRX pins via the ad9361_config.hdl[6] and ad9361_spi.hdl[7] workers.



Source Dependencies

ad9361_config_proxy.rcc

- assets/hdl/devices/ad9361_config_proxy.rcc/ad9361_config_proxy.cc
- assets/hdl/devices/ad9361_config_proxy.rcc/ad9361_platform.cc
- assets/hdl/devices/ad9361_config_proxy.rcc/parameters.h
- assets/hdl/devices/ad9361_config_proxy.rcc/supporting/include/OCPIProjects/AD9361ConfigProxy.hh
- assets/hdl/devices/ad9361_config_proxy.rcc/supporting/include/OCPIProjects/LogForwarder.hh
- assets/hdl/devices/ad9361_config_proxy.rcc/supporting/src/OCPIProjects/AD9361ConfigProxy.cc
- assets/hdl/devices/ad9361_config_proxy.rcc/supporting/src/OCPIProjects/LogForwarder.cc
- libad9361.a (no-OS static library installed with OpenCPI)

Component Spec Properties

Name	Type	Array Dimensions	Accessibility	Valid Range	Default	Usage
rx_nchannels	UChar	-	Parameter	Standard	2	-
tx_nchannels	UChar	-	Parameter	Standard	2	-
ENABLE	UChar	-	Parameter	Standard	1	-
DISABLE	UChar	-	Parameter	Standard	0	-
A_BALANCED	ULong	-	Parameter	Standard	0	-
B_BALANCED	ULong	-	Parameter	Standard	1	-
C_BALANCED	ULong	-	Parameter	Standard	2	-
A_N	ULong	-	Parameter	Standard	3	-
A_P	ULong	-	Parameter	Standard	4	-
B_N	ULong	-	Parameter	Standard	5	-
B_P	ULong	-	Parameter	Standard	6	-
C_N	ULong	-	Parameter	Standard	7	-
C_P	ULong	-	Parameter	Standard	8	-
TX_MON1	ULong	-	Parameter	Standard	9	-
TX_MON2	ULong	-	Parameter	Standard	10	-
TX_MON1_2	ULong	-	Parameter	Standard	11	-
TXA	ULong	-	Parameter	Standard	0	-
TXB	ULong	-	Parameter	Standard	1	-
ENSM_MODE_TX	Long	-	Parameter	Standard	0	-
ENSM_MODE_RX	Long	-	Parameter	Standard	1	-
ENSM_MODE_ALERT	Long	-	Parameter	Standard	2	-
ENSM_MODE_FDD	Long	-	Parameter	Standard	3	-
ENSM_MODE_WAIT	Long	-	Parameter	Standard	4	-
ENSM_MODE_SLEEP	Long	-	Parameter	Standard	5	-
ENSM_MODE_PINCTRL	Long	-	Parameter	Standard	6	-
ENSM_MODE_PINCTRL_FDD_INDEP	Long	-	Parameter	Standard	7	-
INT_LO	UChar	-	Parameter	Standard	0	-
EXT_LO	UChar	-	Parameter	Standard	1	-
RF_GAIN_MGC	UChar	-	Parameter	Standard	0	-
RF_GAIN_FASTATTACK_AGC	UChar	-	Parameter	Standard	1	-
RF_GAIN_SLOWATTACK_AGC	UChar	-	Parameter	Standard	2	-
RF_GAIN_HYBRID_AGC	UChar	-	Parameter	Standard	3	-
FIR_TX1	UChar	-	Parameter	Standard	0x01	-
FIR_TX2	UChar	-	Parameter	Standard	0x02	-
FIR_TX1_TX2	UChar	-	Parameter	Standard	0x03	-
FIR_RX1	UChar	-	Parameter	Standard	0x81	-
FIR_RX2	UChar	-	Parameter	Standard	0x82	-
FIR_RX1_RX2	UChar	-	Parameter	Standard	0x83	-
FIR_IS_RX	UChar	-	Parameter	Standard	0x80	-
RX_1	UChar	-	Parameter	Standard	1	-
RX_2	UChar	-	Parameter	Standard	2	-
TX_1	UChar	-	Parameter	Standard	1	-
TX_2	UChar	-	Parameter	Standard	2	-
BPLL_FREQ	UChar	-	Parameter	Standard	0	-
ADC_FREQ	UChar	-	Parameter	Standard	1	-
R2_FREQ	UChar	-	Parameter	Standard	2	-
R1_FREQ	UChar	-	Parameter	Standard	3	-
CLKRF_FREQ	UChar	-	Parameter	Standard	4	-
RX_SAMPL_FREQ	UChar	-	Parameter	Standard	5	-
NUM_RX_CLOCKS	UChar	-	Parameter	Standard	6	-
IGNORE	UChar	-	Parameter	Standard	0	-
DAC_FREQ	UChar	-	Parameter	Standard	1	-
T2_FREQ	UChar	-	Parameter	Standard	2	-
T1_FREQ	UChar	-	Parameter	Standard	3	-

CLKTF_FREQ	UChar	-	Parameter	Standard	4	-
TX_SAMPL_FREQ	UChar	-	Parameter	Standard	5	-
NUM_TX_CLOCKS	UChar	-	Parameter	Standard	6	-
BIST_DISABLE	ULong	-	Parameter	Standard	0	-
BIST_INJ_TX	ULong	-	Parameter	Standard	1	-
BIST_INJ_RX	ULong	-	Parameter	Standard	2	-
MODE_1x1	UChar	-	Parameter	Standard	1	-
MODE_2x2	UChar	-	Parameter	Standard	2	-
HIGHEST_OSR	ULong	-	Parameter	Standard	0	-
NOMINAL_OSR	ULong	-	Parameter	Standard	2	-
ad9361_rf_phy	Struct (see Table 1)	-	Volatile	Standard	-	-
ad9361_init	Struct (see Table 2)	-	Initial	Standard	reference_clk_rate 40e6,one_rx_one_tx_mode_use_rx_num 1,one_rx_one_tx_mode_use_tx_num 1,frequency_division_duplex_mode_enable 1,xo_disable_use_ext_refclk_enable 0,two_t_two_r_timing_enable 0,pp_tx_swap_enable 1,pp_rx_swap_enable 1,tx_channel_swap_enable 1,rx_channel_swap_enable 1,delay_rx_data 0,rx_data_clock_delay 0,rx_data_delay 4,tx_fb_clock_delay 7,tx_data_delay 0	Initialize the AD9361 part.
en_state_machine_mode	ULong	-	Volatile, Writable	Standard	-	Get/set the Enable State Machine (ENSM) mode. Value should be set using one of the ENSM_MODE_ parameters.
rx_rf_gain	Long	rx_nchannels	Volatile, Writable	Standard	-	Get/set the receive RF gain for the selected channel. The gain is in dB. Note that the written value to the second index of this property will not be applied when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false.
rx_rf_bandwidth	ULong	-	Volatile, Writable	Standard	18e6	Get/set the RX RF bandwidth. The bandwidth is in Hz.
rx_sampling_freq	ULong	-	Volatile, Writable	Standard	30.72e6	Get the RX sampling frequency. The frequency is in Hz.
rx_lo_freq	ULongLong	-	Volatile, Writable	Standard	2.4e9	Get/set the RX LO frequency. The frequency is in Hz.
rx_lo_int_ext	Char	-	Readble, Writable	Standard	INT_LO	Switch between the internal and external LO. The RX LO is affected.
rx_rssi	Struct (see Table 3)	rx_nchannels	Volatile	Standard	-	Get the RSSI for the selected channel.

<table>
<tr><th></th><th></th><th></th><th></th><th></th><th></th><th></th></tr>
<tr><td>rx_gain_control_mode</td><td>UChar</td><td>rx_nchannels</td><td>Volatile, Writable</td><td>Standard</td><td>RF_GAIN_MGC, RF_GAIN_MGC</td><td>Get/set the gain control mode for the selected channel. Note that, when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false, the value read from the second index of this property should be ignored and the value written to the second index won't be applied.</td></tr>
<tr><td>rx_fir_config_write</td><td><table><tr><th>Name</th><th>Type</th><th>ArrayLength</th></tr><tr><td>rx</td><td>ULong</td><td>-</td></tr><tr><td>rx_gain</td><td>Long</td><td>-</td></tr><tr><td>rx_dec</td><td>ULong</td><td>-</td></tr><tr><td>rx_coef</td><td>Short</td><td>128</td></tr><tr><td>rx_coef_size</td><td>UChar</td><td>-</td></tr></table></td><td>-</td><td>Writable</td><td>Standard</td><td>rx 0x83,rx_gain 0,rx_dec 1,rx_coef {1,0},rx_coef_size 128</td><td>-</td></tr>
<tr><td>rx_fir_config_read</td><td><table><tr><th>Name</th><th>Type</th><th>ArrayLength</th></tr><tr><td>rx_gain</td><td>Long</td><td>-</td></tr><tr><td>rx_dec</td><td>ULong</td><td>-</td></tr><tr><td>rx_coef</td><td>Short</td><td>128</td></tr><tr><td>rx_coef_size</td><td>UChar</td><td>-</td></tr></table></td><td>rx_nchannels</td><td>Volatile</td><td>Standard</td><td>-</td><td>Note that the readback value of the second index of this property should be ignored when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false.</td></tr>
<tr><td>rx_fir_en_dis</td><td>UChar</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>DISABLE</td><td>Get/set the status of the RX FIR filter. The status is one of the parameter values ENABLE or DISABLE.</td></tr>
<tr><td>rx_rfdc_track_en_dis</td><td>UChar</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>DISABLE</td><td>Get/set the status of the RX RFDC Tracking. The status is one of the parameter values ENABLE or DISABLE.</td></tr>
<tr><td>rx_bbdc_track_en_dis</td><td>UChar</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>DISABLE</td><td>Get/set the status of the RX BasebandDC Tracking. The status is one of the parameter values ENABLE or DISABLE.</td></tr>
<tr><td>rx_quad_track_en_dis</td><td>UChar</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>DISABLE</td><td>Get/set the status of the RX Quadrate Tracking. The status is one of the parameter values ENABLE or DISABLE.</td></tr>
<tr><td>rx_rf_port_input</td><td>ULong</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>A_BALANCED</td><td>Get/set the RX RF input port. Accepted values: one of the parameter values A_BALANCED, B_BALANCED, C_BALANCED, A_N, A_P, B_N, B_P, C_N, C_P, TX_MON1, TX_MON_2, TX_MON1_2.</td></tr>
</table>

`rx_fastlock_store`	ULong	-	Writable	Standard	-	Store RX fastlock profile. Writing a value will initiate the process of creating an RX fast lock profile and store it in the AD9361 in the RX profile index indicated by the value written.
`rx_fastlock_recall`	ULong	-	Writable	Standard	-	Recall specified RX fastlock profile. Writing a value will initiate the process of applying an RX fast lock profile that was previously stored inside the AD9361. The written value indicates the index of the RX profile to be applied.
`rx_fastlock_load`	Struct (see Table 4)	-	Writable	Standard	-	-
`rx_fastlock_save`	Struct (see Table 5)	-	Writable	Standard	-	-
`tx_attenuation`	ULong	`tx_nchannels`	Volatile, Writable	Standard	1000, 1000	Get/set the transmit attenuation for the selected channel. The attenuation is in millidB. Values written will be rounded down to the nearest 250 millidB. Note that the written value to the second index of this property will not be applied when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false.
`tx_rf_bandwidth`	ULong	-	Volatile, Writable	Standrad	18e6	Get/set the TX RF bandwidth. The bandwidth is in Hz.
`tx_sampling_freq`	ULong	-	Volatile, Writable	Standard	30.72e6	Get/set the TX sampling frequency. The frequency is in Hz.
`tx_lo_freq`	ULongLong	-	Volatile, Writable	Standard	2.4e9	Get/set the TX LO frequency. The frequency is in Hz.
`tx_lo_int_ext`	UChar	-	Readable, Writable	Standard	`INT_LO`	Switch between the internal and external LO. The TX LO is affected.
`tx_fir_config_write`	Name / Type / ArrayLength: tx / ULong / - tx_gain / Long / - tx_int / ULong / - tx_coef / Short / 128 tx_coef_size / UChar / -	-	Writable	Standard	tx 0x03,tx_gain 0,tx_int 1,tx_coef {1,0},rx_coef_size 128	-

tx_fir_config_read	<table><tr><th>Name</th><th>Type</th><th>ArrayLength</th></tr><tr><td>tx_gain</td><td>Long</td><td>-</td></tr><tr><td>tx_int</td><td>ULong</td><td>-</td></tr><tr><td>tx_coef</td><td>Short</td><td>128</td></tr><tr><td>tx_coef_size</td><td>UChar</td><td>-</td></tr></table>	tx_nchannels	Volatile	Standard	-	Note that the readback value of the second index of this property should be ignored when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false.
tx_fir_en_dis	UChar	-	Volatile, Writable	Stabdard	DISABLE	Get/set the status of the TX FIR filter. The status is one of the parameter values ENABLE or DISABLE.
tx_rssi	ULong	tx_nchannels	Volatile	Standard	-	Get the TX RSSI for the selected channel. The value read represents the RSSI in millidB. Note that the readback value of the second index of this property should be ignored when this worker's ad9361_rf_phy.pdata.rx2tx2 property member is false.
tx_rf_port_output	ULong	-	Volatile, Writable	Standard	TXA	Get/set the TX RF output port.
tx_auto_cal_en_dis	UChar	-	Volatile, Writable	Standard	DISABLE	Get/set the status of the auto calibration flag. The value should be one of the parameter values ENABLE or DISABLE.
tx_fastlock_store	ULong	-	Writable	Standard	-	Store TX fastlock profile. Writing a value will initiate the process of creating a TX fast lock profile and store it in the AD9361 in the TX profile index indicated by the value written.
tx_fastlock_recall	ULong	-	Writable	Standard	-	Recall specified TX fastlock profile. Writing a value will initiate the process of applying an TX fast lock profile that was previously stored inside the AD9361. The written value indicates the index of the TX profile to be applied.
tx_fastlock_load	Struct (see Table 6)	-	Writable	Standard	-	-
tx_fastlock_save	Struct (see Table 7)	-	Writable	Standard	-	-
trx_path_clks	Struct (see Table 8)	-	Volatile, Writable	Standard	-	Set the RX and TX path rates.
no_ch_mode	UChar	-	Writable	Standard	-	Set the number of channels mode. Accepted values are one of the parameter values MODE_1x1 or MODE_2x2.
trx_fir_en_dis	UChar	-	Writable	Standard	-	Enable/disable the TRX FIR filters. Accepted values are one of the parameter values ENABLE or DISABLE.
trx_rate_gov	ULong	-	Volatile, Writable	Standard	-	Get/set the OSR rate governor. Accepted values are one of the parameter values HIGHEST_OSR or NOMINAL_OSR.

<table>
<tr><td>do_calib</td><td>Struct (see Table 9)</td><td>-</td><td>Writable</td><td>Standard</td><td>-</td><td>Perform the selected calibration.</td></tr>
<tr><td>trx_load_enable_fir</td><td><table><tr><th>Name</th><th>Type</th><th>ArrayLength</th></tr><tr><td>rx</td><td>ULong</td><td>-</td></tr><tr><td>rx_gain</td><td>Long</td><td>-</td></tr><tr><td>rx_dec</td><td>ULong</td><td>-</td></tr><tr><td>rx_coef</td><td>Short</td><td>-</td></tr><tr><td>rx_coef_size</td><td>UChar</td><td>128</td></tr><tr><td>rx_path_clks</td><td>UChar</td><td>6</td></tr><tr><td>rx_bandwidth</td><td>UChar</td><td>-</td></tr><tr><td>tx</td><td>ULong</td><td>-</td></tr><tr><td>tx_gain</td><td>Long</td><td>-</td></tr><tr><td>tx_int</td><td>ULong</td><td>-</td></tr><tr><td>tx_coef</td><td>Short</td><td>128</td></tr><tr><td>tx_coef_size</td><td>UChar</td><td>-</td></tr><tr><td>tx_path_clks</td><td>UChar</td><td>6</td></tr><tr><td>tx_bandwidth</td><td>UChar</td><td>-</td></tr></table></td><td>-</td><td>Writable</td><td>Standard</td><td>-</td><td>Load and enable TRX FIR filters configurations.</td></tr>
<tr><td>do_dcxo_tune_coarse</td><td>ULong</td><td>-</td><td>Writable</td><td>Standard</td><td>-</td><td>Do DCXO coarse tuning.</td></tr>
<tr><td>do_dcxo_tune_fine</td><td>ULong</td><td>-</td><td>Writable</td><td>Standard</td><td>-</td><td>Do DCXO fine tuning.</td></tr>
<tr><td>temperature</td><td>Long</td><td>-</td><td>Volatile</td><td>Standard</td><td>-</td><td>Get the temperature in millidegrees C.</td></tr>
<tr><td>bist_loopback</td><td>Long</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>-</td><td>BIST loopback mode. Valid values are 0 (disables loopback), 1 (loopback AD9361 internal TX-RX), or 2 (loopback (FPGA internal RX-.TX). While a value of 2 is handled by no-os, it is not expected to work with OpenCPI's AD9361 device workers</td></tr>
<tr><td>bist_prbs</td><td>UChar</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>-</td><td>BIST mode. Valid values are either BIST_DISABLE or BIST_INJ_RX.</td></tr>
<tr><td>bist_tone</td><td>Struct (see Table 10)</td><td>-</td><td>Volatile, Writable</td><td>Standard</td><td>-</td><td>BIST tone. Valid values are either BIST_DISABLE, BIST_INJ_TX, or BIST_INJ_RX.</td></tr>
<tr><td>THB3_Enable_and_Interp</td><td>Enum</td><td>-</td><td>Volatile</td><td>Interpolate_by_1_no_filtering, Interpolate_by_2_half_band_filter, Interpolate_by_3_and_filter, Invalid</td><td>-</td><td>Note that there are several functional that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. This sets interpolation of the digital filter that feeds the DAC. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal DAC clock rate (No-OS does not provide a method for high-precision calculation of the nominal DAC rate).</td></tr>
</table>

THB2_Enable	Bool	-	Volatile	Standard	-	Note that there are several functions that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. Setting to true enables the interpolate-by-2 THB2 half-band filter. Setting to false bypasses the filter. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal DAC clock rate (No-OS does not provide a method for high-precision calculation of the nominal DAC rate).
THB1_Enable	Bool	-	Volatile	Standard	-	Note that there are several functions that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. Setting to true enables the interpolate-by-2 THB1 half-band filter. Setting to false bypasses the filter. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal DAC clock rate (No-OS does not provide a method for high-precision calculation of the nominal DAC rate).
RHB3_Enable_and_Decimation	Enum	-	Volatile	Decimate_by_1_no_filtering, Decimate_by_2_half_band_filter, Decimate_by_3_and_filter, Invalid	-	Note that there are several functional that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. This sets decimation of the first filter stage after the ADC. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal ADC clock rate (No-OS does not provide a method for high-precision calculation of the nominal ADC rate).

RHB2_Enable	Bool	-	Volatile	Standard	-	Note that there are several functions that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. Setting to true enables the decimate-by-2 RHB2 half-band filter. Setting to false bypasses the filter. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal ADC clock rate (No-OS does not provide a method for high-precision calculation of the nominal ADC rate).
RHB1_Enable	Bool	-	Volatile	Standard	-	Note that there are several functions that calculate digital filter settings. The ad9361_calculate_rf_clock_chain function calculates all Rx and Tx rates. Setting to true enables the decimate-by-2 RHB1 half-band filter. Setting to false bypasses the filter. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal ADC clock rate (No-OS does not provide a method for high-precision calculation of the nominal ADC rate).
DAC_Clk_div2	Bool	-	Volatile	Standard	-	The ad9361_calculate_rf_clock_chain function configures this value. When false, the DAC clock rate equals the ADC clock rate. When true, the DAC clock equals 1/2 of the ADC rate. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal DAC clock rate (No-OS does not provide a method for high-precision calculation of the nominal DAC rate).

BBPLL_Divider	Enum	-	Volatile	invalid, 1, 2, 3, 4, 5, 6	-	The ad9361_bbpll_set_rate function controls this value. The ADC clock rate equals the BBPLL divided by the factor which is a function of this value, shown in the following equation. ADC Clock Rate=BBPLL Clock Rate / [2^(BBPLL Divider)]. BBPLL Divider is valid from 1 through 6.
Fractional_BB_Frequency_Word	ULong	-	Volatile	Standard	-	Fractional BB Frequency Word.
Integer_BB_Frequency_Word	UShort	-	Volatile	Standard	-	Integer BB Frequency Word.
BBPLL_Ref_Clock_Scaler	Float	-	Volatile	Standard	-	Ref Clock Scaler. The reference clock frequency is scaled before it enters the BBPLL. Only possible scaler values are: x1; x1/2; x1/4; x2.
Tx_BBF_Tune_Divider	Enum	-	Volatile	invalid, 1 to 511	-	Tx BBF Tune Divider. The baseband Tx analog filter calibration sets the 3dB cutoff frequency of the third-order Butterworth Tx anti-imaging filter based on the Tx BBF Tune Divider. The third-order Tx filter is located just after the DAC in the Tx signal path and is normally calibrated to 1.6x the BBBW. Note that the BBBW is half the complex bandwidth. To set the cutoff frequency value, the BBPLL is divided down using a divide by 1 to 511 divider dedicated to the Tx tuner block.
Tx_Secondary_Filter_Resistor	Enum	-	Volatile	invalid, 800, 400, 200, 100	-	Secondary Tx filter resistor, which, along with the secondary Tx Capacitor, sets the 3 dB corner frequency of the secondary single-pole Tx RC filter via the equation 1/(2*pi*R*C). Value is represented in ohms.
Tx_Secondary_Filter_Capacitor	UShort	-	Volatile	Standard	-	Secondary Tx filter capacitor, which, along with the secondary Tx Resistor, sets the 3 dB corner frequency of the secondary single-pole Tx RC filter via the equation 1/(2*pi*R*C). Resolution: 1pF/LSB. Total capacitance (C in previous equation) is 12pF + (Tx_Secondary_Filter_Capacitor *1pF)

Rx_BBF_Tune_Divide	Enum	-	Volatile	invalid, 1 to 511	-	Rx BBF Tune Divide. The tuning algorithm generates a tune clock derived from the BBPLL frequency. This divider outputs the tune clock, set per for following equation. Rx BBF Tune Divider[8:0] = ceil(BBPLL Frequency x ln(2) / (BBBW x 1.4 x 2 x pi)). The range of the divider is 1 to 511.
bb_pll_is_locked	Bool	-	Volatile	Standard	-	-
rx_pll_is_locked	Enum	-	Volatile	false, true, unknown	-	-
rx_fastlock_delete	ULong	-	Writable	Standard	-	Performs a deletion of an RX fastlock profile saved in this worker's memory. The profile which is deleted is the one whose profile ID matches the value written to this property.
tx_pll_is_locked	Enum	-	Volatile	false, true, unknown	-	-
tx_fastlock_delete	ULong	-	Writable	Standard	-	Performs a deletion of an RX fastlock profile saved in this worker's memory. The profile which is deleted is the one whose profile ID matches the value written to this property.
rx_vco_divider	Enum	-	Volatile	2, 4, 8, 16, 32, 64, 128, external_2, invalid	-	-
rx_vco_n_integer	UShort	-	Volatile	Standard	-	-
rx_vco_n_fractional	UShort	-	Volatile	Standard	-	-
Rx_Ref_Divider	Float	-	Volatile	Standard	-	Rx Ref Divider. This controls the Rx path divider which scales the rate of the analog clock which is input to the Rx PLL Synthesizer (which generates the Rx LO clock). Only possible ratios are: 1, 1/2, 1/4, 2. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal Rx LO frequency value (No-OS does not provide a method for high-precision calculation of the nominal LO frequencies).
tx_vco_divider	Enum	-	Volatile	2, 4, 8, 16, 32, 64, 128, external_2, invalid	-	-
tx_vco_n_integer	UShort	-	Volatile	Standard	-	-
tx_vco_n_fractional	UShort	-	Volatile	Standard	-	-

Tx_Ref_Divider	Float	-	Volatile	Standard	-	Tx Ref Divider. This controls the Tx path divider which scales the rate of the analog clock which is input to the Tx PLL Synthesizer (which generates the Tx LO clock). Only possible ratios are: 1, 1/2, 1/4, 2. The purpose of this property is to expose this value as it exists on the AD9361 IC in order to precisely calculate the current on-chip (in-situ) nominal Tx LO frequency value (No-OS does not provide a method for high-precision calculation of the nominal LO frequencies).
Tx_Channel_Swap	Bool	-	Volatile	Standard	-	Setting this to true swaps the positions of Tx1 and Tx2 samples.
Rx_Channel_Swap	Bool	-	Volatile	Standard	-	Setting this to true swaps the positions of Rx1 and Rx2 samples.
LVDS	Bool	-	Volatile	Standard	-	Value is true if bitstream monitored by instance of this worker was built to use LVDS mode for Data/clock/frame signals, and false if CMOS mode was used.
single_port	Bool	-	Volatile	Standard	-	Value is true if bitstream monitored by instance of this worker was built to use single port, and false if dual ports.
swap_ports	Bool	-	Volatile	Standard	-	Value is true if bitstream monitored by instance of this worker was built to swap Port 0 and Port 1, and false if there was no swap.
half_duplex	Bool	-	Volatile	Standard	-	Value is true if bitstream monitored by instance of this worker was built to use half duplex mode, and false if full duplex mode.
data_rate_config	Enum	-	Volatile	SDR, DDR	-	Value indicates which data rate mode (SDR/DDR) the bitstream was built to use.
DATA_CLK_P_rate_Hz	Double	-	Volatile	Standard	-	-
BIST_Mask_Channel_2_Q_data	Bool	-	Volatile, Writable	Standard	-	Setting zeros out Channel 2 Q data.
BIST_Mask_Channel_2_I_data	Bool	-	Volatile, Writable	Standard	-	Setting zeros out Channel 2 I data.
BIST_Mask_Channel_1_Q_data	Bool	-	Volatile, Writable	Standard	-	Setting zeros out Channel 1 Q data.
BIST_Mask_Channel_1_I_data	Bool	-	Volatile, Writable	Standard	-	Setting zeros out Channel 1 I data.

Table 1: Structure declaration for ad9361_config_proxy.rcc ad9361_rf_phy property.

Name	Type		
clk_ref_in	Name	Type	Description
	clk_ref_in	ULong	-
pdata	Name	Type	Description
	rx2tx2	Bool	When this value is false, the read values from the second index of following properties should be ignored: rx_gain_control_mode, rx_fir_config_read, tx_fir_config_read, and tx_rssi. When this value is false, the written values to the second index of the following properties will not be applied: rx_rf_gain, rx_gain_control_mode, and tx_attenuation.
	fdd	Bool	-
	use_extclk	Bool	-
	dcxo_coarse	ULong	-
	dcxo_fine	ULong	-
	rx1tx1_mode_use_rx_num	ULong	-
	rx1tx1_mode_use_tx_num	ULong	-

Table 2: Structure declaration for ad9361_config_proxy.rcc ad9361_init property.

Name	Type	Description
reference_clk_rate	ULong	-
one_rx_one_tx_mode_use_rx_num	UChar	Set to RX_1 or RX_2 to set desired channel in 1x1 mode. For example, When set to RX_2 mode, the R1 and R2 data paths in the timing diagrams will be swapped.
one_rx_one_tx_mode_use_tx_num	UChar	Set to TX_1 or TX_2 to set desired channel in 1x1 mode. For example, When set to TX_2 mode, the T1 and T2 data paths in the timing diagrams will be swapped.
frequency_division_duplex_mode_enable	UChar	Acceptable values are 1 for true and 0 for false.
xo_disable_use_ext_refclk_enable	UChar	-
two_t_two_r_timing_enable	Bool	Setting to true forces 2R2T timing regardless of number of enabled RX/TX channels. Recommended to set to false if only using at most one RX or one TX channel for the duration of an application (this will lower needed DATA_CLK_P rate). Setting to true has the advantage of ensuring that the timing diagram for each of the RX and TX data paths will not change when dynamically enabling/disabling any of the 4 possible channels (2 RX, 2 TX) at runtime - this comes at the cost of a higher required DATA_CLK_P rate).
pp_tx_swap_enable	UChar	Setting to 1 swaps I and Q (performs spectral inversion). Setting to 0 does not swap.
pp_rx_swap_enable	UChar	Setting to 1 swaps I and Q (performs spectral inversion). Setting to 0 does not swap.
tx_channel_swap_enable	UChar	Setting to 1 swaps RX channels 0 and 1. Setting to 0 does not swap.
rx_channel_swap_enable	UChar	-
delay_rx_data	ULong	Sets the delay of the Rx data relative to Rx frame, measured in 1/2 DATA_CLK cycles for DDR and full DATA_CLK cycles for SDR. Valid values are 0, 1, 2, or 3.
rx_data_clock_delay	ULong	-
rx_data_delay	ULong	-
tx_fb_clock_delay	ULong	Delay in multiples of 0.3 ns to add to the FB_CLK_P pin inside the AD9361 in order to account for the setup/hold requirements of the FB_CLK_P and TX data bus pins. Valid range is [0 15]. This value should be calculated using the setup/hold requiremed values and the reported skews in the FPGA bitstream timing report for the FB_CLK_P, TX data bus, and TX_FRAME_P pins.
tx_data_delay	ULong	Delay in multiples of 0.3 ns to add to the TX data bus and TX_FRAME_P pins inside the AD9361 in order to account for their setup/hold requirements. Valid range is [0 15]. This value should be calculated using the setup/hold requiremed values and the reported skews in the FPGA bitstream timing report for the FB_CLK_P, TX data bus, and TX_FRAME_P pins.

Table 3: Structure declaration for ad9361_config_proxy.rcc rx_rssi property.

Name	Type	Description
ant	ULong	Antenna number for which RSSI is reported.
symbol	ULong	Runtime RSSI.
preamble	ULong	Initial RSSI.
multiplier	Long	Multiplier to convert reported RSSI.
duration	UChar	Duration to be considered for measuring.

Table 4: Structure declaration for ad9361_config_proxy.rcc rx_fastlock_load property.

Name	Type	Description
ad9361_profile_id	ULong	Profile ID/index of the AD9361 profile which is to be overwritten by the indicated worker profile.
worker_profile_id	ULong	Profile ID of the worker profile which will be loaded into the AD9361.

Table 5: Structure declaration for ad9361_config_proxy.rcc rx_fastlock_save property.

Name	Type	Description
ad9361_profile_id	ULong	Profile ID/index of the AD9361 profile which will be saved into a worker profile (i.e. in memory within this worker).
worker_profile_id	ULong	Profile ID to assign to the profile saved in this worker's memory. This is for future record keeping of profiles saved within this worker.

Table 6: Structure declaration for ad9361_config_proxy.rcc tx_fastlock_load property.

Name	Type	Description
ad9361_profile_id	ULong	Profile ID/index of the AD9361 profile which is to be overwritten by the indicated worker profile.
worker_profile_id	ULong	Profile ID of the worker profile which will be loaded into the AD9361.

Table 7: Structure declaration for ad9361_config_proxy.rcc tx_fastlock_save property.

Name	Type	Description
ad9361_profile_id	ULong	Profile ID/index of the AD9361 profile which will be saved into a worker profile (i.e. in memory within this worker).
worker_profile_id	ULong	Profile ID to assign to the profile saved in this worker's memory. This is for future record keeping of profiles saved within this worker.

Table 8: Structure declaration for ad9361_config_proxy.rcc trx_path_clks property.

Name	Type	Description
rx_path_clks	ULong	RX path rates buffer. Indices are indicated bye one of the parameter values BPLL_FREQ, ADC_FREQ, R2_FREQ, R1_FREQ, CLKRF_FREQ, and RX_SAMPL_FREQ.
tx_path_clks	ULong	TX path rates buffer. Indices are indicated bye one of the parameter values IGNORE, DAC_FREQ, T2_FREQ, T1_FREQ, CLKTF_FREQ, and TX_SAMPL_FREQ.

Table 9: Structure declaration for ad9361_config_proxy.rcc do_calib property.

Name	Type	Description
cal	ULong	The selected calibration. Accepted values are one of the parameter values TX_QUAD_CAL or RFDC_CAL.
arg	Long	For TX_QUAD_CAL - the optional RX phase value overwrite (set to zero).

Table 10: Structure declaration for ad9361_config_proxy.rcc bist_tone property.

Name	Type	Description
mode	UChar	-
freq_Hz	ULong	-
level_dB	ULong	-
mask	ULong	Valid values are 0, 1, 2, 4, or 8 for no masking, chan 1 I, chan 1 Q, chan 2 I, chan 2 Q masking, respectively.

Worker Properties

ad9361_config_proxy.rcc

Scope	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
SpecProperty	ad9361_init	-	-	-	WriteSync	-	-	-
SpecProperty	ad9361_rf_phy	-	-	-	ReadSync	-	-	-
SpecProperty	en_state_machine_mode	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_rf_gain	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_rf_bandwidth	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_sampling_freq	-	-	-	ReadSync	-	-	-
SpecProperty	rx_lo_freq	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_lo_int_ext	-	-	-	WriteSync	-	-	-
SpecProperty	rx_rssi	-	-	-	ReadSync	-	-	-
SpecProperty	rx_gain_control_mode	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_fir_config_write	-	-	-	WriteSync	-	-	-
SpecProperty	rx_fir_config_read	-	-	-	ReadSync	-	-	-
SpecProperty	rx_fir_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_rfdc_track_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_bbdc_track_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_quad_track_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_rf_port_input	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	rx_fastlock_store	-	-	-	WriteSync	-	-	-
SpecProperty	rx_fastlock_recall	-	-	-	WriteSync	-	-	-
SpecProperty	rx_fastlock_load	-	-	-	WriteSync	-	-	-
SpecProperty	rx_fastlock_save	-	-	-	WriteSync	-	-	-
SpecProperty	tx_attenuation	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_rf_bandwidth	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_sampling_freq	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_lo_freq	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_lo_int_ext	-	-	-	WriteSync	-	-	-
SpecProperty	tx_fir_config_write	-	-	-	WriteSync	-	-	-
SpecProperty	tx_fir_config_read	-	-	-	ReadSync	-	-	-
SpecProperty	tx_fir_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_rssi	-	-	-	ReadSync	-	-	-
SpecProperty	tx_rf_port_output	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_auto_cal_en_dis	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	tx_fastlock_store	-	-	-	WriteSync	-	-	-
SpecProperty	tx_fastlock_recall	-	-	-	WriteSync	-	-	-
SpecProperty	tx_fastlock_load	-	-	-	WriteSync	-	-	-
SpecProperty	tx_fastlock_save	-	-	-	WriteSync	-	-	-

SpecProperty	trx_path_clks	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	no_ch_mode	-	-	-	WriteSync	-	-	-
SpecProperty	trx_fir_en_dis	-	-	-	WriteSync	-	-	-
SpecProperty	trx_rate_gov	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	do_calib	-	-	-	WriteSync	-	-	-
SpecProperty	trx_load_enable_fir	-	-	-	WriteSync	-	-	-
SpecProperty	do_dcxo_tune_coarse	-	-	-	WriteSync	-	-	-
SpecProperty	do_dcxo_tune_fine	-	-	-	WriteSync	-	-	-
SpecProperty	temperature	-	-	-	ReadSync	-	-	-
SpecProperty	bist_loopback	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	bist_prbs	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	bist_tone	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	THB3_Enable_and_Interp	-	-	-	ReadSync	-	-	-
SpecProperty	THB2_Enable	-	-	-	ReadSync	-	-	-
SpecProperty	THB1_Enable	-	-	-	ReadSync	-	-	-
SpecProperty	RHB3_Enable_and_Decimation	-	-	-	ReadSync	-	-	-
SpecProperty	RHB2_Enable	-	-	-	ReadSync	-	-	-
SpecProperty	RHB1_Enable	-	-	-	ReadSync	-	-	-
SpecProperty	DAC_Clk_div2	-	-	-	ReadSync	-	-	-
SpecProperty	BBPLL_Divider	-	-	-	ReadSync	-	-	-
SpecProperty	Fractional_BB_Frequency_Word	-	-	-	ReadSync	-	-	-
SpecProperty	Integer_BB_Frequency_Word	-	-	-	ReadSync	-	-	-
SpecProperty	BBPLL_Ref_Clock_Scaler	-	-	-	ReadSync	-	-	-
SpecProperty	Tx_BBF_Tune_Divider	-	-	-	ReadSync	-	-	-
SpecProperty	Tx_Secondary_Filter_Resistor	-	-	-	ReadSync	-	-	-
SpecProperty	Tx_Secondary_Filter_Capacitor	-	-	-	ReadSync	-	-	-
SpecProperty	Rx_BBF_Tune_Divider	-	-	-	ReadSync	-	-	-
SpecProperty	bb_pll_is_locked	-	-	-	ReadSync	-	-	-
SpecProperty	rx_pll_is_locked	-	-	-	ReadSync	-	-	-
SpecProperty	rx_fastlock_delete	-	-	-	WriteSync	-	-	-
SpecProperty	tx_pll_is_locked	-	-	-	ReadSync	-	-	-
SpecProperty	tx_fastlock_delete	-	-	-	WriteSync	-	-	-
SpecProperty	rx_vco_divider	-	-	-	ReadSync	-	-	-
SpecProperty	rx_vco_n_integer	-	-	-	ReadSync	-	-	-
SpecProperty	rx_vco_n_fractional	-	-	-	ReadSync	-	-	-
SpecProperty	Rx_Ref_Divider	-	-	-	ReadSync	-	-	-
SpecProperty	tx_vco_divider	-	-	-	ReadSync	-	-	-
SpecProperty	tx_vco_n_integer	-	-	-	ReadSync	-	-	-
SpecProperty	tx_vco_n_fractional	-	-	-	ReadSync	-	-	-
SpecProperty	Tx_Ref_Divider	-	-	-	ReadSync	-	-	-
SpecProperty	LVDS	-	-	-	ReadSync	-	-	-
SpecProperty	single_port	-	-	-	ReadSync	-	-	-
SpecProperty	swap_ports	-	-	-	ReadSync	-	-	-
SpecProperty	half_duplex	-	-	-	ReadSync	-	-	-
SpecProperty	data_rate_config	-	-	-	ReadSync	-	-	-
SpecProperty	DATA_CLK_P_rate_Hz	-	-	-	ReadSync	-	-	-
SpecProperty	BIST_Mask_Channel_2_Q_data	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	BIST_Mask_Channel_2_I_data	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	BIST_Mask_Channel_1_Q_data	-	-	-	ReadSync, WriteSync	-	-	-
SpecProperty	BIST_Mask_Channel_1_I_data	-	-	-	ReadSync, WriteSync	-	-	-

Property	`digital_rx_block_delay_sec`	Struct (see Table 11)	2	-	Volatile, ReadSync	-		See UG-570 equation 14.

Table 11: Structure declaration for ad9361_config_proxy.rcc bist_tone property.

Name	Type	Valid Range
rf_port	Enum	RX1,RX2
delay_sec	Double	Standard

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

Performance and Resource Utilization

ad9361_config_proxy.rcc

Processor Type	Processor Frequency	Run Function Time
TBD	TBD	TBD

Test and Verification

The test outlined in [5] includes validation of a subset of this worker's functionality.

Troubleshooting

The following error message, which is produced by the No-OS library[2] utilized by ad9361_config_proxy.rcc, indicates a hardware communication error between the FPGA and the AD9361. This message would occur, for example, if the AD9361 existed on a card which was not plugged in to the PCB containing the FPGA.

```
ad9361_init : Unsupported PRODUCT_ID 0xC0ad9361_init : AD936x initialization error
```

References

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`https://github.com/analogdevicesinc/no-OS/commit/06bfc76060d5b9767ae9aad7bf40e3648474ebb7`

[2] AD9361 No-OS Software [Analog Devices Wiki]
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`https://github.com/analogdevicesinc/hdl`

[4] AD9361 Datasheet and Product Info
`https://www.analog.com/en/products/ad9361.html`

[5] AD9361 DAC Component Data Sheet
`https://opencpi.github.io/assets/AD9361_DAC.pdf`

[6] AD9361 Config Component Data Sheet
`https://opencpi.github.io/assets/AD9361_Config.pdf`

[7] AD9361 SPI Component Data Sheet
`https://opencpi.github.io/assets/AD9361_SPI.pdf`