Summary - AD9361 ADC SUB

Package Prefix	ocpi.assets.devices
Name	ad9361_adc_sub
Worker Type	Device
OpenCPI Release	v1.5 (released 4/2019)
Workers	ad9361_adc_sub.hdl
Tested Platforms	• Agilent Zedboard/Analog Devices FMCOMMS2 (Vivado only) • Agilent Zedboard/Analog Devices FMCOMMS3 (Vivado only) • x86/Xilinx ML605/Analog Devices FMCOMMS2 • x86/Xilinx ML605/Analog Devices FMCOMMS3 • Ettus E310 (Vivado only, application for testing exists in e310 project)

Functionality

The AD9361 ADC SUB is a subdevice worker whose primary purpose is to de-interleave the AD9361 IC pin-provided time-interleaved RX data streams (independent of which of the IC's P0/P1 buses the RX data stream came from). De-interleaving occurs according to the timing diagrams specified in [2]. This worker ingests RX data from devsignals from ad9361_data_sub.hdl[5], de-interleaves it into at most two 12-bit (Q0.11) RX channel data buses, and makes each channel bus available to an instance of the supported ad9361_adc.hdl device worker via a devsignal port.

Worker Implementation Details

ad9361_adc_sub.hdl

The ad9361_adc_sub.hdl subdevice worker handles registering and de-interleaving of ADC data made available via the `dev_data_from_pins` devsignal port. This worker's `LVDS_p`, `HALF_DUPLEX_p`, `SINGLE_PORT_p`, and `DATA_RATE_CONFIG_p` parameter properties allow for and enforce build-time configuration of the possible AD9361 RX data time-interleaved modes. The currently supported modes and their limitations are shown in the following table.

Table 2: Supported ADC Sampling Rates per RX channel

Platform/Cards which allow the AD9361 Data Port/Channel Mode	AD9361 Data Port Mode	AD9361 Channel Mode	Max AD9361-Supported Sampling Rate per RX channel	Max ad9361_adc_sub.hdl-Supported Sampling Rate per RX channel
E310	CMOS Single Port Half Duplex SDR			not yet supported
E310	CMOS Single Port Half Duplex DDR			not yet supported
E310	CMOS Single Port Full Duplex SDR			not yet supported
E310	CMOS Single Port Full Duplex DDR			not yet supported
E310	CMOS Dual Port Half Duplex SDR			not yet supported
E310	CMOS Dual Port Half Duplex DDR			not yet supported
E310	CMOS Dual Port Full Duplex SDR			not yet supported
E310	CMOS Dual Port Full Duplex DDR			not yet supported
E310	CMOS Single Port Full Duplex DDR	1R1T, 2R2T Timing=0	30.72 Msps	30.72 Msps
		1R1T, 2R2T Timing=1 2R1T 1R2T	15.36 Msps	15.36 Msps
FMCOMMS2/3	LVDS (Dual Port Full Duplex DDR)	all configs	61.44 Msps	61.44 Msps[1]

[1]There are limited guarantees of data fidelity on the FMCOMMS2/3 cards for certain multichannel modes on certain platforms, although tests at room temperature have always yielded 100% fidelity. For more info see tables 8 and 9.

Data is sent out the `dev_data_ch0_out` and `dev_data_ch1_out` devsignal ports for channel 0 and channel 1, respectively. Note that channel 0 corresponds to the AD9361 R1 channel and channel 1 corresponds to the AD9361 R2 channel when the `channels_are_swapped` property has a value of false. The channel relationship is otherwise reversed. Note that which of the two AD9361 RX analog RF port's signal is sent in the R1 and R2 time slots are variable depending on the AD9361 register configuration. This relationship is shown in the following table.

Table 3: Channel Connectivity (D.C. means Don't Care.)

`channels_are_swapped`	ad9361_adc_sub.hdl devsignal channel	AD9361 timing diagram channel	AD9361 RX RF Port	AD9361 Register 0x010 Bit D4[2]	AD9361 Register 0x003 Bits [D7 D6][3]	AD9361 Register 0x004 Bits [D5 D0]
False	0	R1	RX1A_N	0	[D.C. 1]	000001
False	0	R1	RX1A_P	0	[D.C. 1]	000010
False	0	R1	RX1B_N	0	[D.C. 1]	000100
False	0	R1	RX1B_P	0	[D.C. 1]	001000
False	0	R1	RX1C_N	0	[D.C. 1]	010000
False	0	R1	RX1C_P	0	[D.C. 1]	100000
False	0	R1	RX1A_P/RX1A_N	0	[D.C. 1]	000011
False	0	R1	RX1B_P/RX1B_N	0	[D.C. 1]	001100
False	0	R1	RX1C_P/RX1C_N	0	[D.C. 1]	110000
False	0	R1	RX2A_N	1	[1 D.C.]	000001
False	0	R1	RX2A_P	1	[1 D.C.]	000010
False	0	R1	RX2B_N	1	[1 D.C.]	000100
False	0	R1	RX2B_P	1	[1 D.C.]	001000
False	0	R1	RX2C_N	1	[1 D.C.]	010000
False	0	R1	RX2C_P	1	[1 D.C.]	100000
False	0	R1	RX2A_P/RX2A_N	1	[1 D.C.]	000011
False	0	R1	RX2B_P/RX2B_N	1	[1 D.C.]	001100
False	0	R1	RX2C_P/RX2C_N	1	[1 D.C.]	110000
False	1	R2[4]	RX2A_N	0	[1 D.C.]	000001
False	1	R2[4]	RX2A_P	0	[1 D.C.]	000010
False	1	R2[4]	RX2B_N	0	[1 D.C.]	000100
False	1	R2[4]	RX2B_P	0	[1 D.C.]	001000
False	1	R2[4]	RX2C_N	0	[1 D.C.]	010000
False	1	R2[4]	RX2C_P	0	[1 D.C.]	100000
False	1	R2[4]	RX2A_P/RX2A_N	0	[1 D.C.]	000011
False	1	R2[4]	RX2B_P/RX2B_N	0	[1 D.C.]	001100
False	1	R2[4]	RX2C_P/RX2C_N	0	[1 D.C.]	110000
False	1	R2[4]	RX1A_N	1	[D.C. 1]	000001
False	1	R2[4]	RX1A_P	1	[D.C. 1]	000010
False	1	R2[4]	RX1B_N	1	[D.C. 1]	000100
False	1	R2[4]	RX1B_P	1	[D.C. 1]	001000
False	1	R2[4]	RX1C_N	1	[D.C. 1]	010000
False	1	R2[4]	RX1C_P	1	[D.C. 1]	100000
False	1	R2[4]	RX1A_P/RX1A_N	1	[D.C. 1]	000011
False	1	R2[4]	RX1B_P/RX1B_N	1	[D.C. 1]	001100
False	1	R2[4]	RX1C_P/RX1C_N	1	[D.C. 1]	110000
True	0	R2[4]	RX2A_N	0	[1 D.C.]	000001
True	0	R2[4]	RX2A_P	0	[1 D.C.]	000010
True	0	R2[4]	RX2B_N	0	[1 D.C.]	000100
True	0	R2[4]	RX2B_P	0	[1 D.C.]	001000
True	0	R2[4]	RX2C_N	0	[1 D.C.]	010000
True	0	R2[4]	RX2C_P	0	[1 D.C.]	100000
True	0	R2[4]	RX2A_P/RX2A_N	0	[1 D.C.]	000011
True	0	R2[4]	RX2B_P/RX2B_N	0	[1 D.C.]	001100
True	0	R2[4]	RX2C_P/RX2C_N	0	[1 D.C.]	110000

[2]Note that AD9361 register 0x010 Bit D4 is controlled by no-OS's AD9361_InitParam struct's rx_channel_swap_enable member[2] and that the ad9361_config_proxy.rcc worker's `ad9361_init` property sets that member value[6].

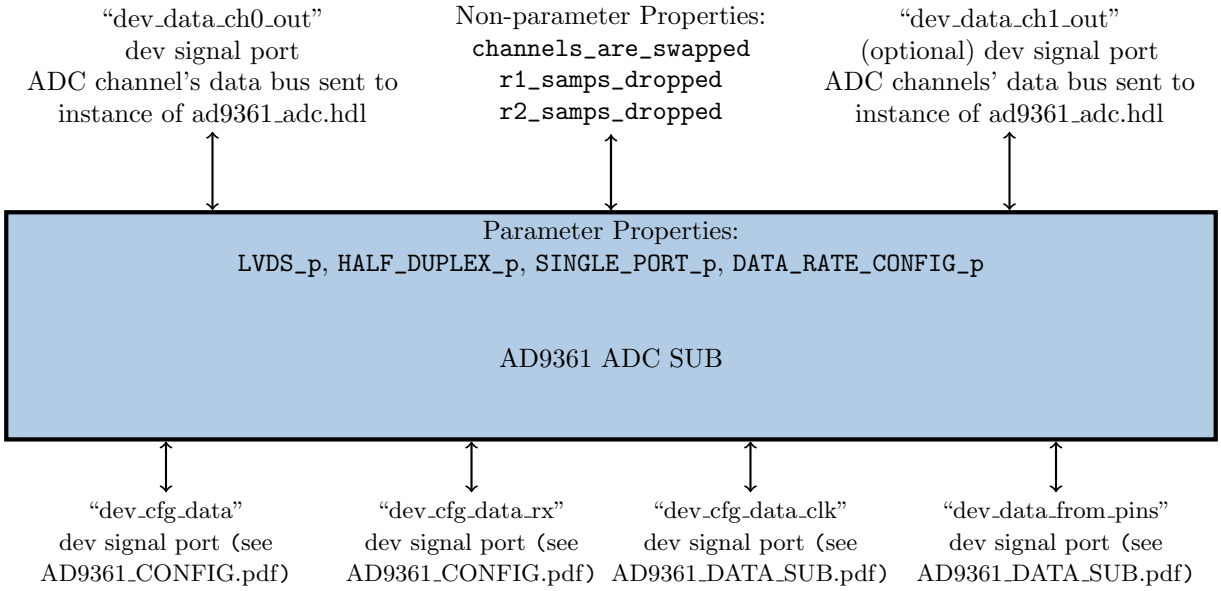
[3]Note that AD9361 register 0x003 Bits [D7 D6] are controlled by no-OS's AD9361_InitParam struct's one_rx_one_tx_use_rx_num member and two_rx_two_tx_mode_enable member[2] and that the ad9361_config_proxy.rcc worker's `ad9361_init` property sets these member values[6].

[4]Note that data will only ever be de-interleaved for the R2 time slot and sent out the devsignal when the AD9361 register 0x010 bit D2 is 1 (which forces 2R2T timing) or when AD9361 register 0x003 Bits D7 and D6 are 1 (which corresponds to one of 2R1T or 2R2T mode)

True	0	$R2^4$	RX1A_N	1	[D.C. 1]	000001
True	0	$R2^4$	RX1A_P	1	[D.C. 1]	000010
True	0	$R2^4$	RX1B_N	1	[D.C. 1]	000100
True	0	$R2^4$	RX1B_P	1	[D.C. 1]	001000
True	0	$R2^4$	RX1C_N	1	[D.C. 1]	010000
True	0	$R2^4$	RX1C_P	1	[D.C. 1]	100000
True	0	$R2^4$	RX1A_P/RX1A_N	1	[D.C. 1]	000011
True	0	$R2^4$	RX1B_P/RX1B_N	1	[D.C. 1]	001100
True	0	$R2^4$	RX1C_P/RX1C_N	1	[D.C. 1]	110000
True	1	R1	RX1A_N	0	[D.C. 1]	000001
True	1	R1	RX1A_P	0	[D.C. 1]	000010
True	1	R1	RX1B_N	0	[D.C. 1]	000100
True	1	R1	RX1B_P	0	[D.C. 1]	001000
True	1	R1	RX1C_N	0	[D.C. 1]	010000
True	1	R1	RX1C_P	0	[D.C. 1]	100000
True	1	R1	RX1A_P/RX1A_N	0	[D.C. 1]	000011
True	1	R1	RX1B_P/RX1B_N	0	[D.C. 1]	001100
True	1	R1	RX1C_P/RX1C_N	0	[D.C. 1]	110000
True	1	R1	RX2A_N	1	[1 D.C.]	000001
True	1	R1	RX2A_P	1	[1 D.C.]	000010
True	1	R1	RX2B_N	1	[1 D.C.]	000100
True	1	R1	RX2B_P	1	[1 D.C.]	001000
True	1	R1	RX2C_N	1	[1 D.C.]	010000
True	1	R1	RX2C_P	1	[1 D.C.]	100000
True	1	R1	RX2A_P/RX2A_N	1	[1 D.C.]	000011
True	1	R1	RX2B_P/RX2B_N	1	[1 D.C.]	001100
True	1	R1	RX2C_P/RX2C_N	1	[1 D.C.]	110000

Block Diagrams

Top level



Source Dependencies

ad9361_adc_sub.hdl

- assets/hdl/devices/ad9361_adc_sub.hdl/ad9361_adc_sub.vhd
- core/hdl/primitives/util/util_pkg.vhd
- core/hdl/primitives/util/sync_status.vhd
- core/hdl/primitives/bsv/imports/SyncBit.v
- core/hdl/primitives/bsv/imports/SyncResetA.v
- core/hdl/primitives/bsv/imports/SyncHandshake.v
- core/hdl/primitives/bsv/bsv_pkg.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
-	-	-	-	-	-	-	-

Worker Properties

ad9361_adc_sub.hdl

Scope	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	LVDS_p	Bool	-	-	Parameter	Standard	False	Use LVDS RX data bus de-interleaving scheme, otherwise use CMOS de-interleaving scheme. Default is CMOS.
Property	HALF_DUPLEX_p	Bool	-	-	Parameter	Standard	False	Use half duplex mode, otherwise use full duplex mode. Must be false when using LVDS mode.
Property	SINGLE_PORT_p	Bool	-	-	Parameter	Standard	False	Use single port, otherwise use both (dual) ports. Default is to use both ports. Must be false when using LVDS mode.
Property	DATA_RATE_CONFIG_p	Enum	-	-	Parameter	SDR, DDR	DDR	This should have a value of DDR when LVDS_p has a value of true. Either value is acceptable when LVDS_p has a value of false (i.e. CMOS mode is used).
Property	channels_are_swapped	Bool	-	-	Readable, Writable	Standard	False	This property exists not as a necessity driven from AD9361 functionality which must be accounted for, but rather as a convenient option to allow control of the routing between the AD9361 pin interface channels (R1 or R2 in the timing diagrams) and this worker's devsignal channels (0 or 1). When this property has a value of true, R1 is routed to channel 0 and R2 to channel 1. When false, the channel relationships are swapped.
Property	r1_samps_dropped	Bool	-	-	Volatile, Writable	Standard	-	A value of true indicates that one or more samples were sent from AD9361 for its R1 channel (see UG-570 timing diagrams) at a moment in time where no ad9361_adc.hdl worker was assigned to ingest them. A value of true is only possible when an assembly is built with only one ad9361_adc.hdl worker and when this worker's channels_are_swapped property has a value of true, together which is an erroneous condition which should be avoided. The purpose of this property is to be an error check for the aforementioned erroneous condition. Writing a value of false will force the value to false. Writing a value of true will do nothing.
Property	r2_samps_dropped	Bool	-	-	Volatile, Writable	Standard	-	A value of true indicates that one or more samples were sent from AD9361 for its R2 channel (see UG-570 timing diagrams) at a moment in time where no ad9361_adc.hdl worker was assigned to ingest them. A value of true is possible, for example, when when an assembly is built with only one ad9361_adc.hdl worker and the AD9361 is configured for multichannel mode (2X2), together which is an erroneous condition which should be avoided. The purpose of this property is to be an error check for the aforementioned erroneous condition. Writing a value of false will force the value to false. Writing a value of true will do nothing.

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

Worker Interfaces

ad9361_adc_sub.hdl

Type	Name	Count	Optional	Master	Signal	Direction	Width	Description
DevSignal	dev_cfg_data	1	False	True	config_is_two_r	Input	1	If 0, de-interleaving of R2 time slot data and monitoring of data drops via the `r2_samps_dropped` property are both disabled.
					ch0_handler_is_present	Output	1	Value is 1 if the dev_data_ch0 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					ch1_handler_is_present	Output	1	Value is 1 if the dev_data_ch1 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					data_bus_index_direction	Output	1	Value is 1 if the bus indexing of the P0_D/P1_D signals from dev_data_from_pins was reversed before processing. This is expected to be hardcoded at buildtime.
					data_clk_is_inverted	Output	1	Value is 1 if the clock in via dev_data_clk was inverted inside this worker before used as an active-edge rising clock. This is expected to be hardcoded at buildtime.
					islvds	Output	1	Value is 1 if `LVDS_p` has a value of true and 0 if `LVDS_p` has a value of false. Because `LVDS_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified LVDS/CMOS mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which LVDS/CMOS mode to use when initializing the AD9361 IC.
					isdualport	Output	1	Value is 1 if `SINGLE_PORT_p` has a value of false and 0 if `SINGLE_PORT_p` has a value of true. Because `SINGLE_PORT_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified single/dual port mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which single/-dual port mode to use when initializing the AD9361 IC.
					isfullduplex	Output	1	Value is 1 if `HALF_DUPLEX_p` has a value of false and 0 if `HALF_DUPLEX_p` has a value of true. Because `HALF_DUPLEX_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified half/full duplex mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which half/full duplex mode to use when initializing the AD9361 IC.
					isDDR	Output	1	Value is 1 if `DATA_RATE_CONFIG_p` has a value of DDR and 0 if `DATA_RATE_CONFIG_p` has a value of SDR. Because `DATA_RATE_CONFIG_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified SDR/DDR mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which half/full duplex mode to use when initializing the AD9361 IC.
					present	Output	1	Used to communicate to ad9361_config.hdl that it should validate the islvds, isdualport, isfullduplex, and isddr signals against similar signals in the ad9361_dac_sub.hdl and ad9361_data_sub.hdl workers if they are present in the bitstream. This is expected to be hardcoded at buildtime.

DevSignal	dev_cfg_data_rx	1	False	True	rx_frame_usage	Output	1	Value is 1 if worker was built with the assumption that the RX frame operates in its toggle setting and 0 if the assumption was that RX frame has a rising edge on the first sample and then stays high. This value is intended to match that of AD9361 register 0x010 BIT D3[3]. This is expected to be hardcoded at buildtime.
					rx_frame_is_inverted	Output	1	RX path-specific data port configuration. Used to tell other workers about the configuration that was enforced when this worker was compiled. This is expected to be hardcoded at buildtime.
DevSignal	dev_data_clk	1	False	True	DATA_CLK_P	Input	1	Buffered version of AD9361 DATA_CLK_P pin.
DevSignal	dev_data_from_pins	1	False	True	data	Input	24	Data bus containing configuration-specific AD9361 pins corresponding to the RX data path: * CMOS single port half duplex: [12'b0 P0_D[11:0]], * CMOS single port full duplex: [18'b0 P0_D[5:0]], * CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]], * CMOS dual port full duplex: [12'b0 P0_D[11:0]], * LVDS: [18'b0 RX_D[5:0]], or, if ports are swapped: * CMOS single port half duplex: [12'b0 P1_D[11:0]], * CMOS single port full duplex: [18'b0 P1_D[5:0]], * CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]], * CMOS dual port full duplex: [12'b0 P1_D[11:0]], * LVDS: (unsupported with port swap). For more info see [5].
					rx_frame	Input	1	Output of buffer whose input is the AD9361 RX_FRAME_P pin's signal.
DevSignal	dev_data_ch0_out	1	False	False	present	Output	1	Value is 1 if a worker is connected to this devsignal port.
					adc_data_I	Input	12	Signed Q0.11 I value of ADC sample corresponding to RX channel 0.
					adc_data_Q	Input	12	Signed Q0.11 Q value of ADC sample corresponding to RX channel 0.
					adc_clk	Input	1	Clock for adc_data_I, adc_data_Q, and adc_give.
					adc_give	Input	1	Indicates that the adc_data_I and adc_data_Q are valid and should be latched on the next rising edge of adc_clk.
DevSignal	dev_data_ch1_out	1	True	False	present	Output	1	Value is 1 if a worker is connected to this devsignal port.
					adc_data_I	Input	12	Signed Q0.11 I value of ADC sample corresponding to RX channel 1.
					adc_data_Q	Input	12	Signed Q0.11 Q value of ADC sample corresponding to RX channel 1.
					adc_clk	Input	1	Clock for adc_data_I, adc_data_Q, and adc_give.
					adc_give	Input	1	Indicates that the adc_data_I and adc_data_Q are valid and should be latched on the next rising edge of adc_clk.

Subdevice Connections

Supports Worker	Supports Worker Port	ad9361_adc_sub.hdl Port	ad9361_adc_sub.hdl Port Index
ad9361_adc	dev_adc	dev_data_ch0_out	0
ad9361_adc	dev_adc	dev_data_ch1_out	0

Control Timing and Signals

Clock Domains

The AD9361 ADC SUB subdevice worker contains two clock domains: the clock from the Control Plane, and the AD9361 DATA_CLK_P clock from the `dev_data_clk` devsignal. The control clock domain is only used to read or write the `channels_are_swapped`, `r1_samps_dropped`, and `r2_samps_dropped` properties (all of which are synchronized between the clock domains in one direction or the other). The DATA_CLK_P domain is used for the registering/de-interleaving of RX data. The data sent out the dev_data_ch0_out and dev_data_ch1_out dev signals is on the DATA_CLK_P domain.

Latency

For the LVDS configuration or CMOS Single Port Full Duplex (DDR) configuration, the latency from the first active edge of the AD9361 DATA_CLK_P clock on which an R1 channel's sample begins to the first rising edge of the output clock on the `dev_data_ch0_out/dev_data_ch1_out` port for the same sample is 6 DATA_CLK_P cycles. For these modes, the latency from the first active edge of the AD9361 DATA_CLK_P clock on which an R2 channel's sample begins to the first rising edge of the output clock on the `dev_data_ch0_out/dev_data_ch1_out` port for the same sample is 4 DATA_CLK_P cycles.

Multichannel Phase Coherency

Note that the aforementioned 6 cycle/4 cycle latency results on the multichannel data being output the devsignal ports in a clock-aligned, phase coherent fashion. However, just because the each channel's devsignal data is phase-aligned at the output of the ad9361_adc_sub.hdl worker's devsignals, that does not mean that the data is phase-aligned once each channel is ingested inside an instance of an ad9361_adc.hdl device worker because each ad9361_adc.hdl instance handles its data as an independent, uniquely flow-controlled data path.

Worker Configuration Parameters

ad9361_adc_sub.hdl

Table 5: Table of Worker Configurations for worker: ad9361_adc_sub

Configuration	DATA_RATE_CONFIG_p	HALF_DUPLEX_p	SINGLE_PORT_p	LVDS_p
0	DDR	false	false	true
1	DDR	false	true	false

Performance and Resource Utilization

ad9361_adc_sub.hdl

The FPGA resource utilization and Fmax are included for this worker. Fmax refers to the maximum allowable clock rate for any registered signal paths within a given clock domain for an FPGA design. Fmax in the table below is specific only to this worker and represents the maximum possible Fmax for any OpenCPI bitstream built with this worker included. Note that the Fmax value for a given clock domain for the final bitstream is often worse than the Fmax specific to this worker, even if this worker is the only one included in the bitstream. It's important to note that the full range of possible operating conditions for the AD9361 is not guaranteed to operate without error, e.g. maximum achievable RX sample rates in certain LVDS modes are less than AD9361 LVDS mode-maximum of 245.76 MHz[2]. For more information, see Tables 7, 8, and 9.

In the tables below, dev_data_clk is the worker source code name for the signal which is ultimately driven by, and has the same clock rate of, the AD9361 DATA_CLK pin pair.

Table 6: Resource Utilization Table for worker: ad9361_adc

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)		Memory/Special Functions
							control plane clock	dev_adc.adc_clk clock	
0	zynq	Vivado	2017.1	xc7z020clg484-1	175	87	315 [1]	418 [1]	BUFR: 1
0	virtex6	ISE	14.7	6vlx240tff1156-1	155	163	437.445		BUFR: 1
1	zynq	Vivado	2017.1	xc7z020clg484-1	175	87	315 [1]	442 [1]	N/A
1	virtex6	ISE	14.7	6vlx240tff1156-1	155	163	437.445		N/A

[1]These measurements were the result of a Vivado timing analysis which was different from the Vivado analysis performed by default for OpenCPI worker builds. For more info see Appendix 1

A notable example of the aforementioned potential discrepancy between worker Fmax and bitstream Fmax for a given clock domain is the maximum achievable AD9361 LVDS RX data clock rate for Zynq 7020 speed grade 1 bitstreams containing this worker. The bitstream Fmax in this case is significantly lower than the worker netlist Fmax of 418MHz on a Zynq 7020 speed grade 1. The timing analysis for the ad9361_adc_sub netlist is not capable of taking into account the paths from the internal-to-the-AD9361 registers which produce the RX data to the ad9361_adc_sub worker's DDR register inputs. The Fmax discrepancy in this case results from these external-to-the-ad9361_adc_sub paths being the limiting factor for the max bistream RX data clock rate. In order to perform a timing analysis which does include these paths, and therefore takes into account all paths which may limit the maximum achievable RX data clock rate, a timing analysis must be done 1) on a netlist/bitstream which includes the rest of the path from the DDR input from the FPGA pad (i.e. it includes the ad9361_data_sub worker) and 2) which includes delay/offset constraints which contain the information about the range of possible clock/data skews from the internal-to-the-AD9361 register which produced the RX data to the FPGA pad (i.e. constraints are used which include the AD9361 datasheet-specified t_{DDRX} and t_{DDDV} min/max values).

Table 7 includes the known theoretical limitations at the bitstream level (as opposed to ad9361_adc_sub level) for the AD9361 DATA_CLK clock rate for various hardware/software configurations. For convenience, Table 8 converts the AD9361 DATA_CLK rate limitations into their consequential RX sample rate limitations. Table 9 contains the experimental verification results for RX sample rate limitations.

Table 7: Theoretical bitstream clock period limitations for dev_data_clk (AD9361 DATA_CLK) clock domain.

Parameter	Conditions	Min	Typ	Max	Unit	Notes
min dev_data_clk (AD9361 DATA_CLK) clock period	Zedboard w/ FMC voltage 2.5V, FMCOMMS2/3 Vivado 2017.1 Design Suite AD9361 DATA_CLK duty cycle=50% [2] AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0	5.712 [1]		5.712 [1]	ns	(approx 175.070028011 MHz), guaranteed by FPGA timing analysis
	ISE 14.7 Design Suite AD9361 DATA_CLK duty cycle=50% [2] AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=3, AD9361 Rx Data Delay=0, AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]	4.294 [1]		4.294 [1]	ns	(approx 232.883092687 MHz), guaranteed by FPGA timing analysis
	ML605, one FMCOMMS2/3 in either slot ISE 14.7 Design Suite AD9361 DATA_CLK duty cycle=50% [2] AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0, AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]		3.545		ns	(approx 282 MHz), guaranteed by FPGA timing analysis
	Ettus E310 Vivado 2017.1 Design Suite AD9361 DATA_CLK duty cycle=50% [2] AD9361 LVDS Mode=0 AD9361 Half Duplex Mode=0 AD9361 Single Port Mode=1 AD9361 Single Data Rate=0 AD9361 DATA_CLK Delay=11, AD9361 Rx Data Delay=0	16.276		16.276	ns	(approx 61.44 MHz), guaranteed by FPGA timing analysis

[1] Note this is more than the minimum AD9361 LVDS DATA_CLK Clock Period of 4.069 ns, i.e. not all possible AD9361 LVDS clock rates can be accounted for.

[2] Note that a) this condition is driven by the limitations of the capabilities of Xilinx ISE/Vivado constraints, and b) the range of value(s) for this condition does not cover the full range of possible values for AD9361 for the given mode.

Table 8: Theoretical bitstream limits for AD9361 RX sample rates per antenna port / channel.

Parameter	Conditions	Min	Typ	Max	Unit	Notes
bitstream minimum supported RX sample period for a given AD9361 antenna port / channel	Zedboard w/ FMC voltage jumper setting 2.5V, FMCOMMS2/3 Vivado 2017.1 Design Suite bitstream AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2]	11.424		11.424	ns	(approx 87.535014005 Msps complex per RX channel), guaranteed by FPGA timing analysis
	AD9361 2R1T mode or 2R2T mode or AD9361 2R2T Timing = 1 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2]	22.848 [1]		22.848 [1]	ns	(approx 43.767507002 Msps complex [1] per RX channel), guaranteed by FPGA timing analysis
	ISE 14.7 Design Suite bitstream AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=3, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2], AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]	8.588		8.588	ns	(approx 116.441546343 Msps complex per RX channel), guaranteed by FPGA timing analysis
	AD9361 2R1T mode or 2R2T mode or AD9361 2R2T Timing = 1 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2], AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]	17.176 [1]		17.176 [1]	ns	(approx 58.220773171 Msps complex [1] per RX channel), guaranteed by FPGA timing anaylysis
	ML605, one FMCOMMS2/3 in either slot AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2], AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]		7.090		ns	(approx 141.043723554 Msps complex per RX channel), guaranteed by FPGA timing anaylysis
	AD9361 2R1T mode or 2R2T mode or AD9361 2R2T Timing = 1 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2], AD9361 $t_{DDRX} = 0.75ns$ [2], AD9361 $t_{DDDV} = 0.75ns$ [2]		14.180		ns	(approx 70.521861777 Msps complex per RX channel), guaranteed by FPGA timing anaylysis

	Ettus E310 Vivado 2017.1 Design Suite bitstream AD9361 LVDS Mode=0 AD9361 Half Duplex Mode=0 AD9361 Single Port Mode=1 AD9361 Single Data Rate=0 AD9361 DATA_CLK Delay=11, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2] AD9361 2R1T mode or 2R2T mode or AD9361 2R2T Timing = 1 full range of FPGA voltages/temperatures, AD9361 DATA_CLK duty cycle=50% [2]		32.552 65.104		ns ns	(approx 30.72 Msps complex per RX channel), guaranteed by FPGA timing anaylysis (approx 15.36 Msps complex per RX channel), guaranteed by FPGA timing anaylysis

[1]Note this value corresponds to less than the maximum possible AD9361 sample rate per AD9361 antenna port/channel for the given mode.

[2]Note that a) this condition is driven by the limitations of the capabilities of Xilinx ISE constraints, and b) the range of value(s) for this condition does not cover the full range of possible values for AD9361 for the given mode.

Table 9: Experimentally verified RX bit error rates.

Parameter	Conditions	Min	Typ	Max	Unit	Notes
RX bit error rate	Zedboard w/ FMC voltage jumper setting 2.5V, FMCOMMS2/3 Vivado 2017.1 Design Suite bitstream AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 room temperature, RX sample rate=61.44 Msps complex (approx, nominal)	0	0		%	AD9361 PRBS test
	AD9361 1R1T mode, AD9361 2R2T Timing = 1 room temperature, RX sample rate=43.767507 Msps complex [1] (approx, nominal)	0	0		%	
	ISE 14.7 Design Suite bitstream AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=3, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 room temperature, RX sample rate=61.44 Msps complex (approx, nominal)	0	0		%	
	AD9361 1R1T mode, AD9361 2R2T Timing = 1 room temperature, RX sample rate=58.220773 Msps complex [1] (approx, nominal)	0	0		%	
	ML605 in CentOS7 x86 machine PCIe slot, one FMCOMMS2/3 in either slot AD9361 LVDS Mode=1 AD9361 DATA_CLK Delay=2, AD9361 Rx Data Delay=0 AD9361 1R1T mode room temperature, RX sample rate=61.44 Msps complex (approx, nominal)	0	0		%	
	Ettus E310 Vivado 2017.1 Design Suite bitstream AD9361 LVDS Mode=0 AD9361 Half Duplex Mode=0 AD9361 Single Port Mode=1 AD9361 DATA_CLK Delay=11, AD9361 Rx Data Delay=0 AD9361 1R1T mode, AD9361 2R2T Timing = 0 room temperature, RX sample rate=30.72 Msps complex (approx, nominal) AD9361 1R1T mode, AD9361 2R2T Timing = 1	0	0		%	

	room temperature, RX sample rate=15.36 Msps complex (approx, nominal)	0	0		%	

Test and Verification

No unit test for this component exists. However, a hardware-in-the-loop application (which is NOT a unit test) exists for testing purposes (see assets/applications/ad9361_adc_test).

References

[1] AD9361 Datasheet and Product Info
`https://www.analog.com/en/products/ad9361.html`

[2] AD9361 Reference Manual UG-570
AD9361_Reference_Manual_UG-570.pdf

[3] AD9361 Register Map Reference Manual UG-671
AD9361_Register_Map_Reference_Manual_UG-671.pdf

[4] AD9361 ADC Component Data Sheet
`https://opencpi.github.io/assets/AD9361_ADC.pdf`

[5] AD9361 Data Sub Component Data Sheet
`https://opencpi.github.io/assets/AD9361_Data_Sub.pdf`

[6] AD9361 Config Proxy Component Data Sheet
`https://opencpi.github.io/assets/AD9361_Config_Proxy.pdf`

[1] Note this value corresponds to less than the maximum possible AD9361 sample rate per AD9361 antenna port/channel for the given mode.

1 Appendix - Vivado Timing Analysis

The Vivado timing report that OpenCPI runs for device workers may erroneously report a max delay for a clocking path which should have been ignored. Custom Vivado tcl commands had to be run for this device worker to extract pertinent information from Vivado timing analysis. After building the worker, the following commands were run from the assets project directory (after the Vivado settings64.sh was sourced):

```
cd hdl/devices/
vivado -mode tcl
```

Then the following commands were run inside the Vivado tcl terminal. ***Note this example is for build configuration 0 only***.

```
open_project ad9361_adc_sub.hdl/target-zynq/ad9361_adc_sub_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_adc_sub_rv -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets {ctl_in[Clk]}]
create_clock -name clk2 -period 0.001 [get_nets {dev_data_clk_in[DATA_CLK_P]}]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
```

The following is the output of the timing reports. The Fmax for the control plane clock for this worker is computed as the maximum magnitude slack with a control plane clock of 1 ps plus 2 times the assumed 1 ps control plane clock period (3.172 ns + 0.002 ns = 3.174 ns, 1/3.174 ns = 315.06 MHz). The Fmax for the dev_data_clk clock from the devsignal is computed as the maximum magnitude slack with dev_data_clk of 1 ps plus 2 times the assumed 1 ps dev_data_clk period (2.387 ns + 0.002 ns = 2.389 ns, 1/2.389 ns = 418.59 MHz).

```
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-242] The property HD.CLK_SRC of clock port "ctl_in[Clk]" is not set. In out-of-context mode, this prevents timing estimation for clock \
      delay/skew
Resolution: Set the HD.CLK_SRC property of the out-of-context port to the location of the clock buffer instance in the top-level design
WARNING: [Timing 38-242] The property HD.CLK_SRC of clock port "dev_data_clk_in[DATA_CLK_P]" is not set. In out-of-context mode, this prevents timing \
      estimation for clock delay/skew
Resolution: Set the HD.CLK_SRC property of the out-of-context port to the location of the clock buffer instance in the top-level design
INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type min_max -sort_by slack.
Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2017.1 (lin64) Build 1846317 Fri Apr 14 18:54:47 MDT 2017
| Date         : Mon Oct 1 14:28:58 2018
| Host         : <removed> running 64-bit CentOS Linux release 7.5.1804 (Core)
| Command      : report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
| Design       : ad9361_adc_sub_rv
| Device       : 7z020-clg484
| Speed File   : -1  PRODUCTION 1.11 2014-09-11
------------------------------------------------------------------------------------------------


Timing Report


Slack (VIOLATED) :      -3.172ns (required time - arrival time)
  Source:               wci/wci_decode/my_state_r_reg[2]/C
                          (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Destination:          wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
                          (rising edge-triggered cell FDSE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Path Group:           clk1
```

```
 Path Type:           Setup (Max at Slow Process Corner)
 Requirement:         0.002ns (clk1 rise@0.002ns - clk1 rise@0.000ns)
 Data Path Delay:     2.921ns (logic 0.937ns (32.078%) route 1.984ns (67.922%))
 Logic Levels:        2  (LUT6=2)
 Clock Path Skew:     -0.049ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
   Source Clock Delay    (SCD):   0.973ns
   Clock Pessimism Removal (CPR): 0.000ns
 Clock Uncertainty:   0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter   (TSJ):   0.071ns
   Total Input Jitter    (TIJ):   0.000ns
   Discrete Jitter        (DJ):   0.000ns
   Phase Error            (PE):   0.000ns

   Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
 ------------------------------------------------------------------- -------------------
                     (clock clk1 rise edge)    0.000    0.000 r
                                               0.000    0.000 r ctl_in[Clk] (IN)
                     net (fo=41, unset)        0.973    0.973   wci/wci_decode/ctl_in[Clk]
                     FDRE                                   r  wci/wci_decode/my_state_r_reg[2]/C
 ------------------------------------------------------------------- -------------------
                     FDRE (Prop_fdre_C_Q)      0.518    1.491 r wci/wci_decode/my_state_r_reg[2]/Q
                     net (fo=7, unplaced)      1.000    2.491   wci/wci_decode/wci_state[2]
                                                        r  wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/I0
                     LUT6 (Prop_lut6_I0_O)     0.295    2.786 r wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/O
                     net (fo=4, unplaced)      0.473    3.259   wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2_n_0
                                                        r  wci/wci_decode/FSM_onehot_my_access_r[4]_i_2/I2
                     LUT6 (Prop_lut6_I2_O)     0.124    3.383 r wci/wci_decode/FSM_onehot_my_access_r[4]_i_2/O
                     net (fo=8, unplaced)      0.511    3.894   wci/wci_decode/my_access_r
                     FDSE                                   r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
 ------------------------------------------------------------------- -------------------

                     (clock clk1 rise edge)    0.002    0.002 r
                                               0.000    0.002 r ctl_in[Clk] (IN)
                     net (fo=41, unset)        0.924    0.926   wci/wci_decode/ctl_in[Clk]
                     FDSE                                   r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/C
                     clock pessimism           0.000    0.926
                     clock uncertainty        -0.035    0.891
                     FDSE (Setup_fdse_C_CE)   -0.169    0.722   wci/wci_decode/FSM_onehot_my_access_r_reg[0]
 -------------------------------------------------------------------
                     required time                      0.722
                     arrival time                      -3.894
 -------------------------------------------------------------------
                     slack                             -3.172




report_timing: Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 2089.160 ; gain = 497.523 ; free physical = 604 ; free virtual = 55948
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk2

Timing Report

Slack (VIOLATED) :      -2.387ns (required time - arrival time)
 Source:                worker/data_mode_lvds.rx_frame_p_ddr/C
                          (rising edge-triggered cell IDDR clocked by clk2 {rise@0.000ns fall@0.001ns period=0.001ns})
 Destination:           worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/CE
```

```
                      (rising edge-triggered cell FDRE clocked by clk2 {rise@0.000ns fall@0.001ns period=0.001ns})
Path Group:           clk2
Path Type:            Setup (Max at Slow Process Corner)
Requirement:          0.002ns (clk2 rise@0.002ns - clk2 rise@0.000ns)
Data Path Delay:      2.007ns (logic 0.686ns (34.185%) route 1.321ns (65.815%))
Logic Levels:         1  (LUT3=1)
Clock Path Skew:      -0.145ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 1.849ns = ( 1.851 - 0.002 )
  Source Clock Delay    (SCD):   2.094ns
  Clock Pessimism Removal (CPR): 0.099ns
Clock Uncertainty:    0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter  (TSJ):   0.071ns
  Total Input Jitter   (TIJ):   0.000ns
  Discrete Jitter       (DJ):   0.000ns
  Phase Error           (PE):   0.000ns

  Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
-------------------------------------------------------------------- -------------------
                     (clock clk2 rise edge)    0.000    0.000 r
                                               0.000    0.000 r dev_data_clk_in[DATA_CLK_P] (IN)
                     net (fo=0)                0.973    0.973   worker/dev_data_clk_in[DATA_CLK_P]
                                                         r  worker/BUFR_inst/I
                     BUFR (Prop_bufr_I_O)      0.537    1.510 r worker/BUFR_inst/O
                     net (fo=140, unplaced)    0.584    2.094   worker/dev_data_ch0_out_out[adc_clk]
                     IDDR                               r  worker/data_mode_lvds.rx_frame_p_ddr/C
-------------------------------------------------------------------- -------------------
                     IDDR (Prop_iddr_C_Q2)     0.508    2.602 r worker/data_mode_lvds.rx_frame_p_ddr/Q2
                     net (fo=3, unplaced)      0.800    3.401   worker/adc_rx_frame_p_buf_rr13_out
                                                         r  worker/adc_r1_i_h_rrr/I0
                     LUT3 (Prop_lut3_I0_O)     0.178    3.579 r worker/adc_r1_i_h_rrr/O
                     net (fo=12, unplaced)     0.521    4.100   worker/adc_r1_q_h_rrr_0
                     FDRE                               r  worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/CE
-------------------------------------------------------------------- -------------------


                     (clock clk2 rise edge)    0.002    0.002 r
                                               0.000    0.002 r dev_data_clk_in[DATA_CLK_P] (IN)
                     net (fo=0)                0.924    0.926   worker/dev_data_clk_in[DATA_CLK_P]
                                                         r  worker/BUFR_inst/I
                     BUFR (Prop_bufr_I_O)      0.486    1.412 r worker/BUFR_inst/O
                     net (fo=140, unplaced)    0.439    1.851   worker/dev_data_ch0_out_out[adc_clk]
                     FDRE                               r  worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/C
                     clock pessimism           0.099    1.951
                     clock uncertainty        -0.035    1.915
                     FDRE (Setup_fdre_C_CE)   -0.202    1.713   worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]
-------------------------------------------------------------------
                     required time                      1.713
                     arrival time                      -4.100
-------------------------------------------------------------------
                     slack                             -2.387
```

These calculations can be verified by replacing the `create_clock` lines above with the following values and rerunning the `report_timing` commands and observing a value of 0.000 ns for the slacks:

```
create_clock -name clk1 -period 3.174 [get_nets {ctl_in[Clk]}]
create_clock -name clk2 -period 2.389 [get_nets {dev_data_clk_in[DATA_CLK_P]}]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
```

For the clk2 example:

```
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk2


Timing Report


Slack (MET) :           0.000ns (required time - arrival time)
 Source:                worker/data_mode_lvds.rx_frame_p_ddr/C
                          (rising edge-triggered cell IDDR clocked by clk2 {rise@0.000ns fall@1.194ns period=2.389ns})
 Destination:           worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/CE
                          (rising edge-triggered cell FDRE clocked by clk2 {rise@0.000ns fall@1.194ns period=2.389ns})
 Path Group:            clk2
 Path Type:             Setup (Max at Slow Process Corner)
 Requirement:           2.389ns (clk2 rise@2.389ns - clk2 rise@0.000ns)
 Data Path Delay:       2.007ns (logic 0.686ns (34.185%) route 1.321ns (65.815%))
 Logic Levels:          1  (LUT3=1)
 Clock Path Skew:       -0.145ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 1.849ns = ( 4.238 - 2.389 )
   Source Clock Delay    (SCD):   2.094ns
   Clock Pessimism Removal (CPR): 0.099ns
 Clock Uncertainty:     0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter  (TSJ):   0.071ns
   Total Input Jitter   (TIJ):   0.000ns
   Discrete Jitter       (DJ):   0.000ns
   Phase Error           (PE):   0.000ns

   Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
 -------------------------------------------------------------------- -------------------
                      (clock clk2 rise edge)    0.000    0.000 r
                                                0.000    0.000 r dev_data_clk_in[DATA_CLK_P] (IN)
                      net (fo=0)                0.973    0.973   worker/dev_data_clk_in[DATA_CLK_P]
                                                              r  worker/BUFR_inst/I
                      BUFR (Prop_bufr_I_O)      0.537    1.510 r worker/BUFR_inst/O
                      net (fo=140, unplaced)    0.584    2.094   worker/dev_data_ch0_out_out[adc_clk]
                      IDDR                                 r  worker/data_mode_lvds.rx_frame_p_ddr/C
 -------------------------------------------------------------------- -------------------
                      IDDR (Prop_iddr_C_Q2)     0.508    2.602 r worker/data_mode_lvds.rx_frame_p_ddr/Q2
                      net (fo=3, unplaced)      0.800    3.401   worker/adc_rx_frame_p_buf_rr13_out
                                                              r  worker/adc_r1_i_h_rrr/I0
                      LUT3 (Prop_lut3_I0_O)     0.178    3.579 r worker/adc_r1_i_h_rrr/O
                      net (fo=12, unplaced)     0.521    4.100   worker/adc_r1_q_h_rrr_0
                      FDRE                                 r  worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/CE
 -------------------------------------------------------------------- -------------------


                      (clock clk2 rise edge)    2.389    2.389 r
                                                0.000    2.389 r dev_data_clk_in[DATA_CLK_P] (IN)
                      net (fo=0)                0.924    3.313   worker/dev_data_clk_in[DATA_CLK_P]
                                                              r  worker/BUFR_inst/I
                      BUFR (Prop_bufr_I_O)      0.486    3.799 r worker/BUFR_inst/O
                      net (fo=140, unplaced)    0.439    4.238   worker/dev_data_ch0_out_out[adc_clk]
                      FDRE                                 r  worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]/C
                      clock pessimism           0.099    4.338
                      clock uncertainty        -0.035    4.302
                      FDRE (Setup_fdre_C_CE)   -0.202    4.100   worker/data_mode_lvds.adc_r1_i_h_rrr_reg[0]
 -------------------------------------------------------------------
                      required time                      4.100
                      arrival time                      -4.100
```

```
-------------------------------------------------------------------
                    slack                                 0.000
```