Summary - Data_Src

Name	data_src
Worker Type	Application
Version	v1.3
Release Date	June 2017
Component Library	ocpi.assets.misc_comps
Workers	data_src.hdl
Tested Platforms	isim

Functionality

The Data_Src component selects one data bus from multiple data generation sources, packs it in bit-forward order in an I data bus and bit-reverse order in a Q data bus, and sends that I/Q bus out an iqstream output port. The available data sources consist of:

- a counter,
- a walking ones bus (e.g. b'100 →b'010 →b'001 →b'100 →etc),
- a Linear Feedback Shift Register (LFSR),
- and a property-driven fixed value.

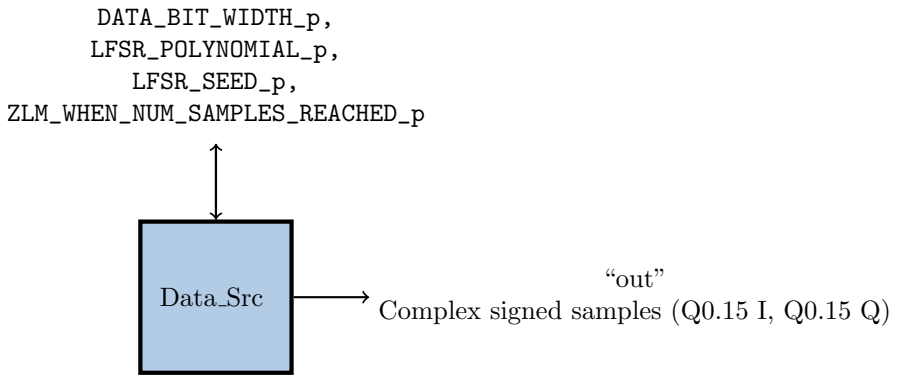
The bitwidth common to all data source buses is parameterized. In the case that the data source bus width is less than the iqstream I/Q widths of 16 bits, the bus is packed into the most significant bits of I and Q. This aids in data alignment when this component is connected directly to a DAC device worker, which commonly takes the DAC bitwidth-most significant bits of I and Q from an iqstream input port for its data transmission.
This component includes a property-driven setting which can optionally disable the output port once a specified number of samples have been sent. This component can also be parameterized to send a Zero-Length Message (ZLM) once the output port is disabled.

Worker Implementation Details

In keeping with good data flow control practices, backpressure from the output port will suspend the advancement of each data generation source. The `ZLM_WHEN_NUM_SAMPLES_REACHED_p` parameter, when having a value of true, forces the worker to send a single ZLM when the output port has been disabled (i.e. when the `num_samples` property has a value of more than 1 and `num_samples` amount of samples have been sent out the output port). This is useful for allowing applications which use this worker to terminate once this worker's output port is disabled.

Block Diagrams

Top level



Source Dependencies

data_src.hdl

- ocpiassets/components/misc_comps/data_src.hdl/data_src.vhd
- ocpiassets/primitives/misc_prims/lfsr/src/lfsr.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
DATA_BIT_WIDTH_p	ushort	-	-	Parameter	-	16	Determines the width of the buses for each of the I and Q data generation memory elements - if less than 16, the most significant `DATA_BIT_WIDTH_p` bits of I and Q on the out port will be filled. Value is expect to be less than or equal to 16.
LFSR_POLYNOMIAL_p	bool	-	DATA_BIT_WIDTH_p	Parameter	-	0	E.g., a value of 1,1,0,1 would correspond to an LFSR polynomial of $x^4 + x^3 + (0 * x^2) + x^1 + 1$ (+1 is always implied regardless of value).
LFSR_SEED_p	bool	-	DATA_BIT_WIDTH_p	Parameter	-	0	Out-of-reset value of the Linear Feedback Shift Register (only affects output data in LFSR mode). This value should never be all zeros, which would cause the register to always have a value of all zeros regardless of polynomial value.
ZLM_WHEN_NUM_SAMPLES_REACHED_p	bool	-	-	Parameter	-	false	When value is true and `num_samples` property value is not -1, worker will generate Zero-Length-Message after `num_samples` amount of samples have been sent out the output port.
messageSize_bytes	ulong	-	-	Readable, Initial	-	4096	Message size in bytes. When the value of (`num_samples` * num bytes per sample) is less than this property's value, the value of (`num_samples` * num bytes per sample) is used as the message size.
num_samples	long	-	-	Readable, Writeable	-	-1	Maximum number of samples which will be sent out of the output port once out of reset. Note that samples are only sent when the `enable` property has a value of true. When the value of this property is -1, samples will be sent indefinitely (obeying backpressure from the connected worker, of course).
fixed_value	bool	-	DATA_BIT_WIDTH_p	Readable, Writeable	-	0x5a5a	The value of this property will be used for I (and the bit-reversed version of this value will be used for Q) to send to the output port when the `mode` property's value is 'fixed'.
mode	enum	-	-	Readable, Writeable	count,walking, LFSR,fixed	count	Counter, walking ones, Linear Feedback Shift Register, or fixed value.
enable	bool	-	-	Readable, Writeable	-	true	When the worker is not in reset, this property must have a value of true for the data to be sent to the output.
LFSR_bit_reverse	bool	-	-	Readable, Writeable	-	true	Used to determine the LFSR shift direction. When true, the `DATA_BIT_WIDTH_p`-bits wide LFSR will be reversed for both I and Q.

Worker Properties

data_src.hdl

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
out	true	iqstream_protocol	False	ZeroLengthMessages=true	Complex signed samples (Q0.15 I, Q0.15 Q). This port generates data while obeying backpressure. This port is disabled when either the enable property has a value of false or when the `num_samples` property has a value of greater than 0 and `num_samples` amount of samples have been sent out this port.

Worker Interfaces

data_src.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	out	32	-	-

Control Timing and Signals

data_src.hdl

The FIFO worker uses the clock from the Control Plane and standard Control Plane signals.

Performance and Resource Utilization

data_src.hdl

Worker Build Configuration "0":
Table entries are a result of building the worker with the following parameter sets:

- `LFSR_POLYNOMIAL_p=1,1,1,0,0,0,0,0,1,0,0,0`
- `DATA_BIT_WIDTH_p=12`
- `LFSR_SEED_p=1,1,1,1,1,1,1,1,1,1,1,1`
- `ZLM_WHEN_NUM_SAMPLES_REACHED_p=true`
- `ocpi_endian=little`
- `ocpi_debug=false`

Table 1: Worker Build Configuration "0"

OpenCPI Target	Tool	Version	Device	Registers	LUTs	Fmax (MHz)	Memory/Special Functions
stratix4	Quartus	15.1.0	N/A	270	404	N/A	N/A
virtex6	ISE	14.7	6vcx75tff484-2	257	332	304.807	N/A
zynq	Vivado	2017.1	xc7z020clg400-3	269	348	258.598	N/A
zynq_ise	ISE	14.7	7z010clg400-3	255	332	369.753	N/A

- `DATA_WIDTH_p=12`
- `LFSR_POLYNOMIAL_p=1,1,1,0,0,0,0,0,1,0,0,0`
- `LFSR_SEED_p=0,0,0,0,0,0,0,0,0,0,0,0`
- `ZLM_WHEN_NUM_SAMPLES_REACHED_p=true`

Device	Registers	LUTs	Fmax	Memory/Special Functions	GCLK	I/O	Design Suite
Stratix4 EP4SGX230K-C2-F40	270	378	-	-	1	129	Quartus 12.1 SP1
Virtex6 XC6VLX240T-1-FF1156	244	320	271 MHz	-	1	129	ISE 14.7
Zynq XC7Z020-1-CLG484	244	320	341 MHz	-	1	129	ISE 14.7

- `DATA_WIDTH_p=12`
- `LFSR_POLYNOMIAL_p=1,1,1,0,0,0,0,0,1,0,0,0`
- `LFSR_SEED_p=0,0,0,0,0,0,0,0,0,0,0,0`
- `ZLM_WHEN_NUM_SAMPLES_REACHED_p=false`

Device	Registers	LUTs	Fmax	Memory/Special Functions	GCLK	I/O	Design Suite
Stratix4 EP4SGX230K-C2-F40	269	377	-	-	1	129	Quartus 12.1 SP1
Virtex6 XC6VLX240T-1-FF1156	243	396	281 MHz	-	1	129	ISE 14.7
Zynq XC7Z020-1-CLG484	243	396	352 MHz	-	1	129	ISE 14.7

Test and Verification

For verification, multiple test are run with varying values for the `num_samples` property for each of the available data source modes. The output file is checked for expected length and data contents, with the data content check being specific to the given data source mode.