Summary - CIC Interpolator

Name	cic_int
Worker Type	Application
Version	v1.4
Release Date	February 2018
Component Library	ocpi.assets.dsp_comps
Workers	cic_int.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The CIC interpolator has `N` cascaded comb stages with an input data rate of $\frac{f_s}{R}$, followed by a rate change by a factor `R`, followed by `N` cascaded integrator stages with an output data rate of f_s. The differential delay, `M`, affects the slope of the transition region. Figure 1 diagrams the interpolating CIC filter.

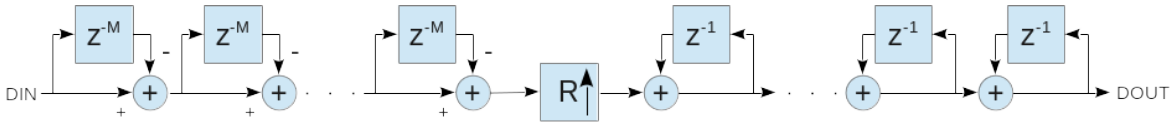

Figure 1: Cascaded Integration Comb Decimation filter Block Diagram

Worker Implementation Details

cic_int.hdl

Number of Stages

The generic `N` sets the number of integrators and comb stages in the filter. Increasing the number of stages increases the attenuation in the sidelobes, as well as the bandwidth of the passband. The recommended range for this parameter is 3 to 6. Consult the reference material for an in depth discussion of the frequency response of the filter as a function of the generics in this module.

Bit Growth

For this design, the output data width for the comb stages is configurable via `ACC_WIDTH`. To adjust for bit growth in the data path and to ensure no quantization error at the output, this equation should be used to determine the value of `ACC_WIDTH`.

$$ACC\_WIDTH = N * CEIL(log_2(R * M)) + DIN\_WIDTH \tag{1}$$

Theory

A CIC filter is comprised of `N` integrator sections cascaded together with `N` comb sections. Combining the transfer functions for the two sections, we arrive at the system response function seen in Equation 1.

$$H(z) = [H_{int}(z)]^N [H_{comb}(z)]^N = \frac{1}{(1-z^{-1})^N}(1-z^{-R+M})^N = \frac{(1-z^{-R+M})^N}{(1-z^{-1})^N} \tag{2}$$

The magnitude response of the CIC filter is low pass with nulls at multiples of $f = \frac{1}{RM}$. The region surrounding the nulls is where aliasing occurs, so this aliasing effect must be considering when choosing `N`, `M`, and `R`.

Block Diagrams

Top level

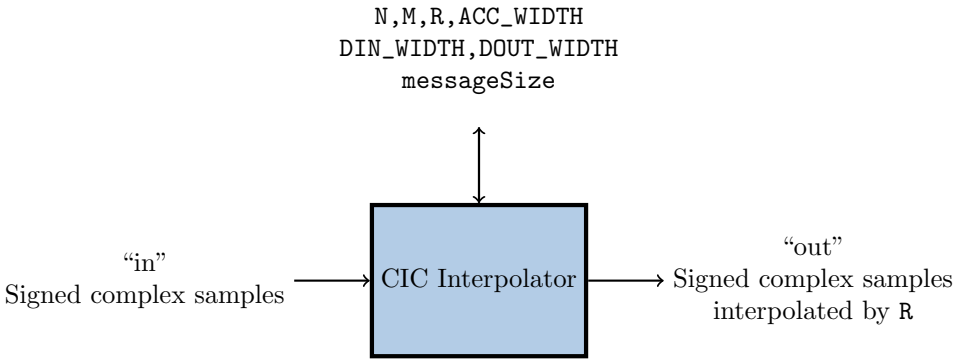

Figure 2: Top Level Block Diagram

State Machine

Only one finite-state machine (FSM) is implemented by this worker. The FSM supports Zero-Length Messages.

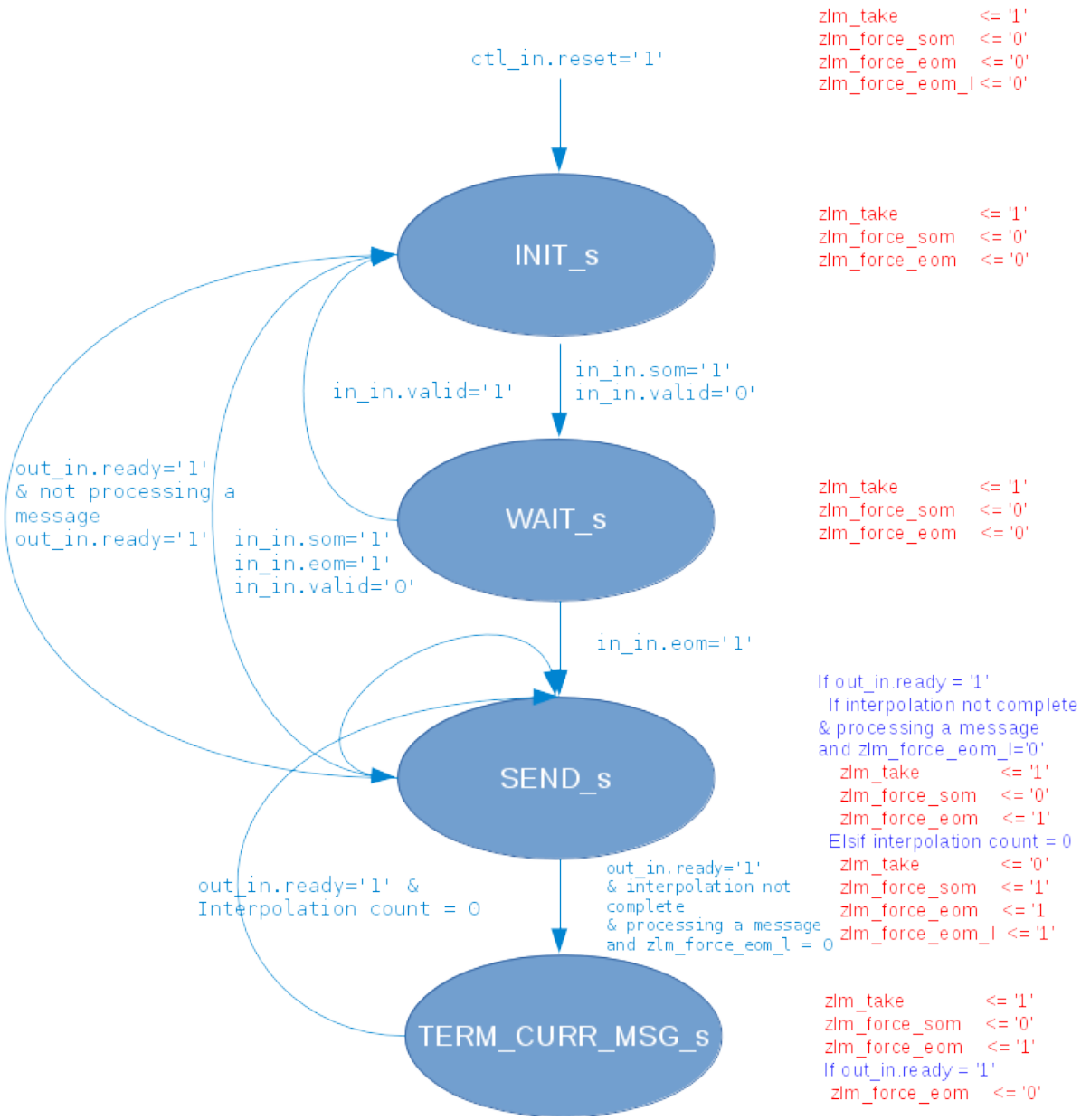

Figure 3: Zero-Length Message FSM

Source Dependencies

cic_int.hdl

- assets/components/dsp_comps/cic_int.hdl/cic_int.vhd
- assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  assets/hdl/primitives/dsp_prims/cic/src/cic_int_gen.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
N	UChar	-	-	Readable	-	-	Number of Stages
M	UChar	-	-	Readable	-	-	Differential Delay
R	UShort	-	-	Readable	-	-	Interpolation Factor
ACC_WIDTH	UChar	-	-	Readable	-	-	Accumulation Width *(2)
DIN_WIDTH	UChar	-	-	Readable	-	-	Input data width
DOUT_WIDTH	UChar	-	-	Readable	-	-	Output data width
messageSize	UShort	-	-	Readable, Writable	-	8192	Number of bytes in output message

Worker Properties

cic_int.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
SpecProperty	N	-	-	-	Parameter	3-6	3	Number of Stages
SpecProperty	M	-	-	-	Parameter	1-2	1	Differential Delay
SpecProperty	R	-	-	-	Parameter	4-8192	4	Decimation Factor
SpecProperty	DIN_WIDTH	-	-	-	Parameter	16	16	Input Data Width
SpecProperty	ACC_WIDTH	-	-	-	Parameter	*	22	Accumulation Width *(2)
SpecProperty	DOUT_WIDTH	-	-	-	Parameter	16	16	Output Data Width
Property	CHIPSCOPE_p	Bool	-	-	Readable, Parameter	Standard	false	Include ISE ChipScope circuit
Property	VIVADO_ILA_p	Bool	-	-	Readable, Parameter	Standard	false	Include Vivado Integrated Logic Analyzer circuit

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	False	iqstream_protocol	False	-	Complex signed samples (Q0.15 I, Q0.15 Q).
out	False	iqstream_protocol	False	-	Complex signed samples (Q0.15 I, Q0.15 Q).

Worker Interfaces

cic_int.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	ZeroLengthMessages=true	Signed complex samples
StreamInterface	out	32	ZeroLengthMessages=true	Signed complex samples

Control Timing and Signals

The CIC Interpolation filter HDL worker uses the clock from the Control Plane and standard Control Plane signals.

This worker has a latency of `N*2+1` valid input data clock cycles.

Latency
`N*2+1`

Worker Configuration Parameters

cic_int.hdl

Table 1: Table of Worker Configurations for worker: cic_int

Configuration	ocpi_endian	ocpi_debug	ACC_WIDTH	DOUT_WIDTH	CHIPSCOPE_p	DIN_WIDTH	N	M	VIVADO_ILA_p	R
0	little	false	22	16	false	16	3	1	false	4
1	little	false	25	16	false	16	3	2	false	4
2	little	false	23	16	false	16	3	1	false	5
3	little	false	26	16	false	16	3	2	false	5
4	little	false	25	16	false	16	3	1	false	8
5	little	false	28	16	false	16	3	1	false	16
6	little	false	49	16	false	16	3	1	false	2048
7	little	false	52	16	false	16	3	2	false	2048
8	little	false	60	16	false	16	4	1	N/A	2048
9	little	false	55	16	false	16	3	1	N/A	8191
10	little	false	58	16	false	16	3	2	N/A	8191
11	little	false	55	16	false	16	3	1	N/A	8192
12	little	false	58	16	false	16	3	2	N/A	8192

Performance and Resource Utilization

cic_int.hdl

Table 2: Resource Utilization Table for worker: cic_int

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	zynq	Vivado	2017.1	xc7z020clg484-1	582	453	N/A	N/A
0	virtex6	ISE	14.7	6vlx240tff1156-1	545	540	329.707	N/A
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	584	475	N/A	N/A
1	zynq	Vivado	2017.1	xc7z020clg484-1	734	483	N/A	N/A
1	virtex6	ISE	14.7	6vlx240tff1156-1	665	558	329.707	N/A
1	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	736	499	N/A	N/A
2	zynq	Vivado	2017.1	xc7z020clg484-1	597	458	N/A	N/A
2	virtex6	ISE	14.7	6vlx240tff1156-1	553	550	329.707	N/A
2	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	597	486	N/A	N/A
3	zynq	Vivado	2017.1	xc7z020clg484-1	751	488	N/A	N/A
3	virtex6	ISE	14.7	6vlx240tff1156-1	673	568	329.707	N/A
3	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	751	510	N/A	N/A
4	zynq	Vivado	2017.1	xc7z020clg484-1	621	485	N/A	N/A
4	virtex6	ISE	14.7	6vlx240tff1156-1	565	562	329.707	N/A
4	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	621	504	N/A	N/A
5	zynq	Vivado	2017.1	xc7z020clg484-1	656	518	N/A	N/A
5	virtex6	ISE	14.7	6vlx240tff1156-1	585	585	327.335	N/A
5	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	658	531	N/A	N/A
6	zynq	Vivado	2017.1	xc7z020clg484-1	915	731	N/A	N/A
6	virtex6	ISE	14.7	6vlx240tff1156-1	725	748	305.46	N/A
6	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	917	699	N/A	N/A
7	zynq	Vivado	2017.1	xc7z020clg484-1	1121	761	N/A	N/A
7	virtex6	ISE	14.7	6vlx240tff1156-1	845	767	304.09	N/A
7	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1123	725	N/A	N/A
8	zynq	Vivado	2017.1	xc7z020clg484-1	1408	1089	N/A	N/A
8	virtex6	ISE	14.7	6vlx240tff1156-1	990	974	301.643	N/A
8	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1410	1029	N/A	N/A
9	zynq	Vivado	2017.1	xc7z020clg484-1	989	802	N/A	N/A
9	virtex6	ISE	14.7	6vlx240tff1156-1	765	792	297.044	N/A
9	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	991	748	N/A	N/A
10	zynq	Vivado	2017.1	xc7z020clg484-1	1207	832	N/A	N/A
10	virtex6	ISE	14.7	6vlx240tff1156-1	885	810	297.044	N/A
10	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1209	774	N/A	N/A
11	zynq	Vivado	2017.1	xc7z020clg484-1	989	799	N/A	N/A
11	virtex6	ISE	14.7	6vlx240tff1156-1	764	794	297.044	N/A
11	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	991	751	N/A	N/A
12	zynq	Vivado	2017.1	xc7z020clg484-1	1207	828	N/A	N/A
12	virtex6	ISE	14.7	6vlx240tff1156-1	885	821	301.296	N/A
12	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1209	777	N/A	N/A

Test and Verification

Two test cases are implemented to validate the CIC Interpolator component:

1. Unity gain response to DC: The CIC Interpolator gain is calculated using the following equation:

$$CIC\ Gain = \frac{(R * M)^N}{2^{CEIL(N * log_2(R * M))}} \tag{3}$$

2. Tone waveform: A waveform containing a tone at 50 Hz is sampled at 1024000/R and processed by the worker. The output data (interpolated waveform) is checked to ensure the 50 Hz tone is present.

For the plots below, a CIC Interpolator with the following parameter set was used: `N`=3, `M`=1, `R`=2048, and `ACC_WIDTH`=49.

For Case #1, the plots below show the input with the I-leg zoomed in the show the amplitude is 32767, and output data with the I-leg zoomed to show an amplitude of 32767, which can be calculated using 3, shown below, and the Q-leg showing the worker delay before reaching it steady-state value.

$$OutputAmplitude = 32767 * \frac{(2048 * 1)^3}{2^{CEIL(3 * log_2(2038 * 1))}} = 32767 * 1 = 32767 \tag{4}$$

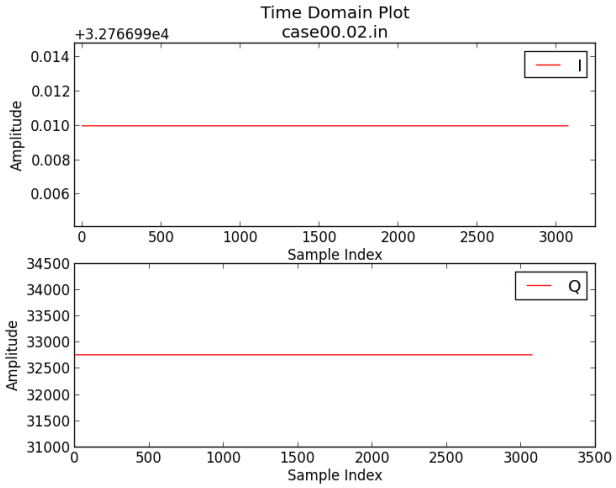

Figure 4: Time Domain: DC with amp=32767

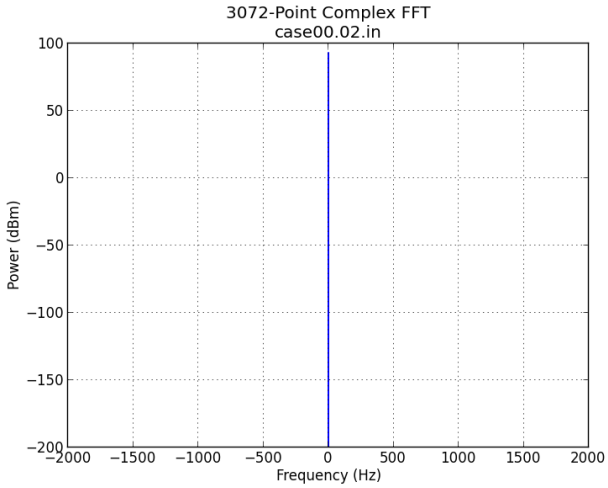

Figure 5: Frequency Domain: 0 Hz

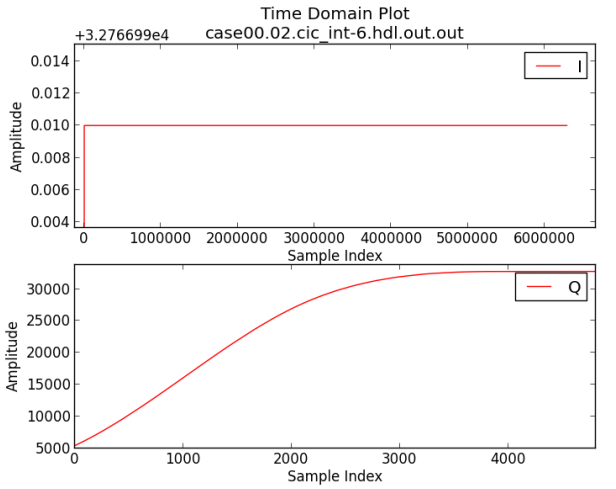

Figure 6: Time Domain: DC with amp=32767

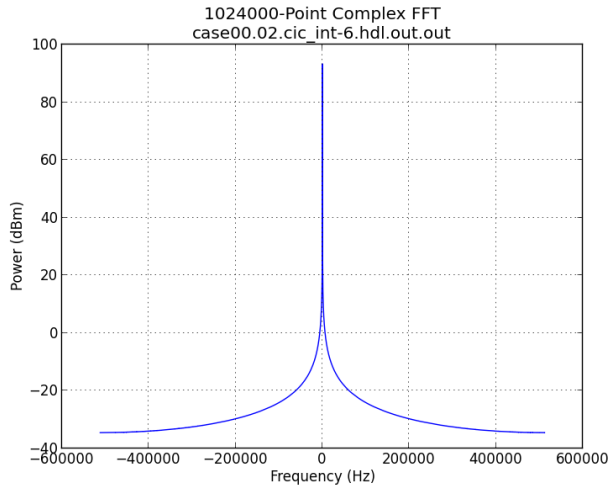

Figure 7: Frequency Domain: 0 Hz

The input time-domain plot below shows the I-leg zoomed into one cycle and Q-leg showing all samples of a 50 Hz tone sampled at 1024000/R=1024000/2048=500 Hz, which results in 10 samples/cycle. The input freq-domain plot shows the generated tone at 50 Hz. The output time-domain plot below shows the I-leg zoomed into approximately two cycles and Q-leg showing all samples of a 50 Hz tone sampled at (1024000/R)*R=(1024000/2048)*2048=1024000 Hz, which results in 20480 samples/cycle. The output freq-domain plot shows the expected tone at 50 Hz.

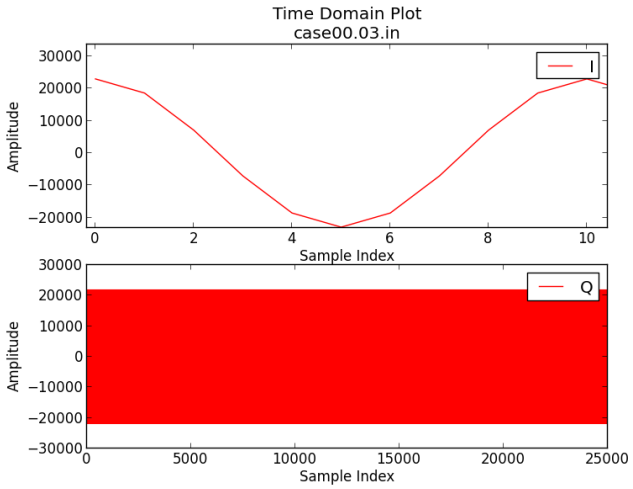

Figure 8: Time Domain

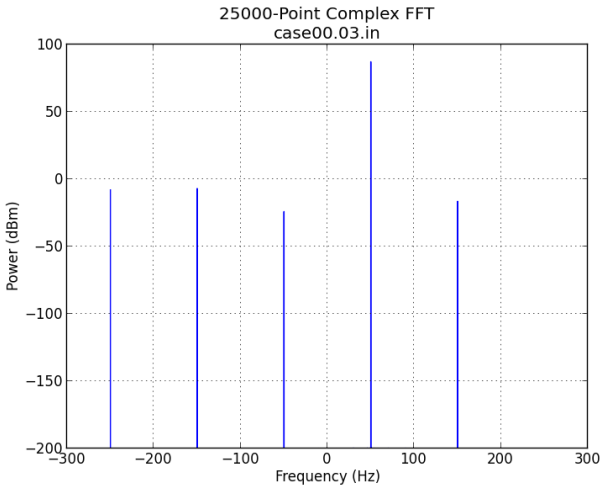

Figure 9: Frequency Domain: 50 Hz

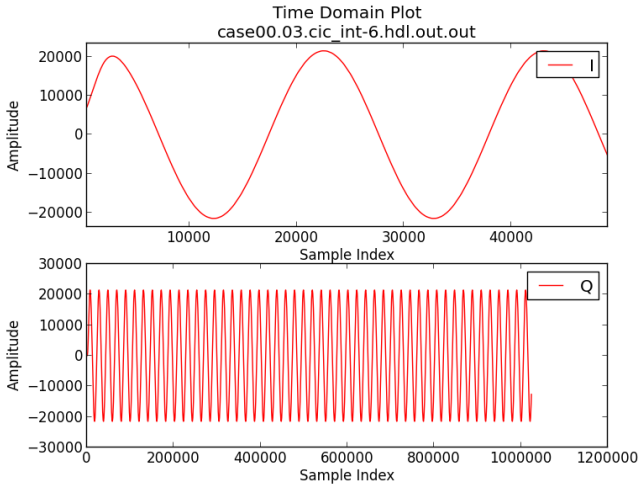

Figure 10: Time Domain

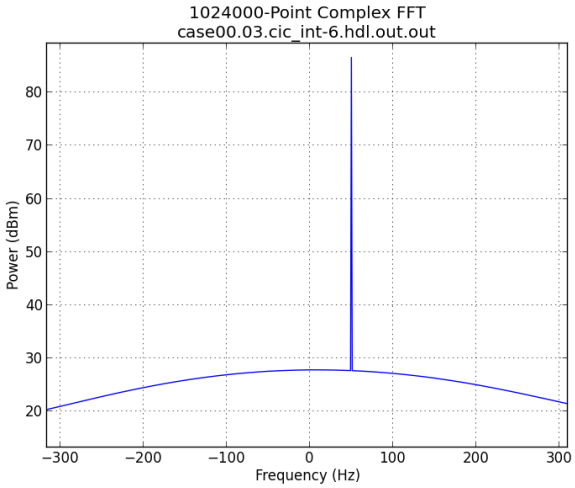

Figure 11: Frequency Domain: 50 Hz

References

(1) Ronald E. Crochiere and Lawrence R. Rabiner. Multirate Digital Signal Processing. Prentice-Hall Signal Processing Series. Prentice Hall, Englewood Cli_s, 1983.
(2) Eugene B. Hogenauer, An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, April 1981.