Summary - CIC Decimator

Name	cic_dec
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets.dsp_comps
Workers	cic_dec.hdl
Tested Platforms	xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)

Functionality

The CIC decimator has `N` cascaded integrator stages with an input data rate of f_s, followed by a rate change by a factor `R`, followed by `N` cascaded comb stages with an output data rate of $\frac{f_s}{R}$. The differential delay, `M`, affects the slope of the transition region. Figure 1 diagrams the decimating CIC filter.

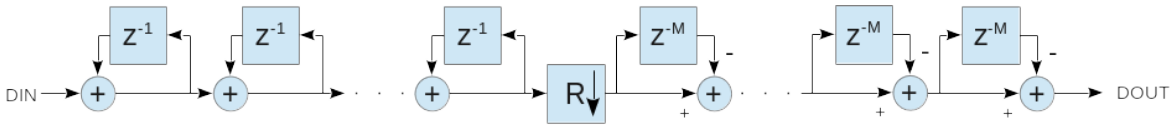

Figure 1: Cascaded Integration Comb Decimation filter Block Diagram

Worker Implementation Details

cic_dec.hdl

Number of Stages

The generic `N` sets the number of integrators and comb stages in the filter. Increasing the number of stages increases the attenuation in the sidelobes and decreases the 3dB bandwidth of the passband. The recommended range for this parameter is 3 to 6. Consult the reference material for an in depth discussion of the frequency response of the filter as a function of the generics in this module.

Bit Growth

For this design, the output data width for the comb stages is configurable via `ACC_WIDTH`. To adjust for bit growth in the data path and to ensure no quantization error at the output, this equation should be used to determine the value of `ACC_WIDTH`.

$$ACC\_WIDTH = N * CEIL(log_2(R * M)) + DIN\_WIDTH \tag{1}$$

Theory

A CIC filter is comprised of `N` integrator sections cascaded together with `N` comb sections. Combining the transfer functions for all sections results in the system response function seen in Equation 2. Note that the filter has zeros at integer multiples of $\frac{f_s}{RM}$ Hz.

$$H(z) = \Big[H_{int}(z)\Big]^N \Big[H_{comb}(z)\Big]^N = \Big[\frac{1}{(1-z^{-1})^N}\Big]\Big[(1-z^{-RM})^N\Big] = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \tag{2}$$

Block Diagrams

Top level

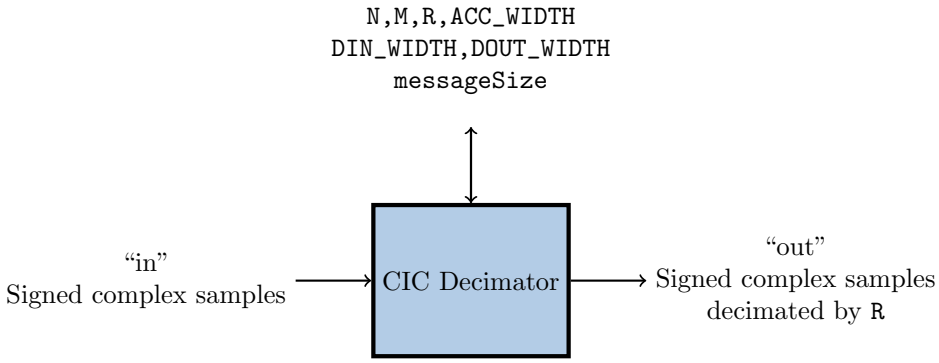

Figure 2: Top Level Block Diagram

Source Dependencies

cic_dec.hdl

- assets/components/dsp_comps/cic_dec.hdl/cic_dec.vhd
- assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  assets/hdl/primitives/dsp_prims/cic/src/cic_dec_gen.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
N	UChar	-	-	Readable	-	-	Number of Stages
M	UChar	-	-	Readable	-	-	Differential Delay
R	UShort	-	-	Readable	-	-	Decimation Factor
ACC_WIDTH	UChar	-	-	Readable	-	-	Accumulation Width *(2)
DIN_WIDTH	UChar	-	-	Readable	-	-	Input data width
DOUT_WIDTH	UChar	-	-	Readable	-	-	Output data width
messageSize	UShort	-	-	Readable, Writable	-	8192	Number of bytes in output message

Worker Properties

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Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
SpecProperty	N	-	-	-	Parameter	3-6	3	Number of Stages
SpecProperty	M	-	-	-	Parameter	1-2	1	Differential Delay
SpecProperty	R	-	-	-	Parameter	4-8192	4	Decimation Factor
SpecProperty	DIN_WIDTH	-	-	-	Parameter	16	16	Input Data Width
SpecProperty	ACC_WIDTH	-	-	-	Parameter	*	22	Accumulation Width *(2)
SpecProperty	DOUT_WIDTH	-	-	-	Parameter	16	16	Output Data Width

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	False	iqstream_protocol	False	-	Complex signed samples (Q0.15 I, Q0.15 Q).
out	False	iqstream_protocol	False	-	Complex signed samples (Q0.15 I, Q0.15 Q).

Worker Interfaces

cic_dec.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	32	ZeroLengthMessages=true	Signed complex samples
StreamInterface	out	32	ZeroLengthMessages=true	Signed complex samples

Control Timing and Signals

The CIC Decimation filter HDL worker uses the clock from the Control Plane and standard Control Plane signals.

This worker has a latency of `N*2+1` valid input data clock cycles.

Latency
`N*2+1`

Worker Configuration Parameters

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Table 1: Table of Worker Configurations for worker: cic_dec

Configuration	DOUT_WIDTH	ocpi_debug	M	R	DIN_WIDTH	ocpi_endian	N	ACC_WIDTH
0	16	false	1	4	16	little	3	22
1	16	false	2	4	16	little	3	25
2	16	false	1	5	16	little	3	23
3	16	false	2	5	16	little	3	26
4	16	false	1	8	16	little	3	25
5	16	false	1	16	16	little	3	28
6	16	false	1	2048	16	little	3	49
7	16	false	2	2048	16	little	3	52
8	16	false	1	2048	16	little	4	60
9	16	false	1	8191	16	little	3	55
10	16	false	2	8191	16	little	3	58
11	16	false	1	8192	16	little	3	55
12	16	false	2	8192	16	little	3	58

Performance and Resource Utilization

cic_dec.hdl

Table 2: Resource Utilization Table for worker "cic_dec"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	727	450	N/A	N/A
0	zynq	Vivado	2017.1	xc7z020clg484-1	725	520	N/A	N/A
0	zynq_ise	ISE	14.7	7z020clg484-1	722	668	289.185	N/A
0	virtex6	ISE	14.7	6vlx240tff1156-1	722	668	267.881	N/A
1	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	931	486	N/A	N/A
1	zynq	Vivado	2017.1	xc7z020clg484-1	929	556	N/A	N/A
1	zynq_ise	ISE	14.7	7z020clg484-1	926	704	289.185	N/A
1	virtex6	ISE	14.7	6vlx240tff1156-1	926	704	267.881	N/A
2	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	746	464	N/A	N/A
2	zynq	Vivado	2017.1	xc7z020clg484-1	745	534	N/A	N/A
2	zynq_ise	ISE	14.7	7z020clg484-1	742	682	289.185	N/A
2	virtex6	ISE	14.7	6vlx240tff1156-1	742	682	267.881	N/A
3	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	956	500	N/A	N/A
3	zynq	Vivado	2017.1	xc7z020clg484-1	955	570	N/A	N/A
3	zynq_ise	ISE	14.7	7z020clg484-1	952	718	289.185	N/A
3	virtex6	ISE	14.7	6vlx240tff1156-1	952	718	267.881	N/A
4	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	782	488	N/A	N/A
4	zynq	Vivado	2017.1	xc7z020clg484-1	781	558	N/A	N/A
4	zynq_ise	ISE	14.7	7z020clg484-1	778	706	289.185	N/A
4	virtex6	ISE	14.7	6vlx240tff1156-1	778	706	267.881	N/A
5	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	837	524	N/A	N/A
5	zynq	Vivado	2017.1	xc7z020clg484-1	837	594	N/A	N/A
5	zynq_ise	ISE	14.7	7z020clg484-1	834	743	289.185	N/A
5	virtex6	ISE	14.7	6vlx240tff1156-1	834	743	267.881	N/A
6	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1222	798	N/A	N/A
6	zynq	Vivado	2017.1	xc7z020clg484-1	1229	858	N/A	N/A
6	zynq_ise	ISE	14.7	7z020clg484-1	1226	1018	289.185	N/A
6	virtex6	ISE	14.7	6vlx240tff1156-1	1226	1016	267.881	N/A
7	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1588	834	N/A	N/A
7	zynq	Vivado	2017.1	xc7z020clg484-1	1595	894	N/A	N/A
7	zynq_ise	ISE	14.7	7z020clg484-1	1592	1054	289.185	N/A
7	virtex6	ISE	14.7	6vlx240tff1156-1	1592	1052	267.881	N/A
8	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1780	1170	N/A	N/A
8	zynq	Vivado	2017.1	xc7z020clg484-1	1787	1230	N/A	N/A
8	zynq_ise	ISE	14.7	7z020clg484-1	1784	1390	289.185	N/A
8	virtex6	ISE	14.7	6vlx240tff1156-1	1784	1388	267.881	N/A
9	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1332	872	N/A	N/A
9	zynq	Vivado	2017.1	xc7z020clg484-1	1341	957	N/A	N/A
9	zynq_ise	ISE	14.7	7z020clg484-1	1338	1120	289.185	N/A

9	virtex6	ISE	14.7	6vlx240tff1156-1	1338	1124	267.881	N/A
10	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1734	908	N/A	N/A
10	zynq	Vivado	2017.1	xc7z020clg484-1	1743	993	N/A	N/A
10	zynq_ise	ISE	14.7	7z020clg484-1	1740	1156	289.185	N/A
10	virtex6	ISE	14.7	6vlx240tff1156-1	1740	1160	267.881	N/A
11	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1332	872	N/A	N/A
11	zynq	Vivado	2017.1	xc7z020clg484-1	1341	956	N/A	N/A
11	zynq_ise	ISE	14.7	7z020clg484-1	1338	1120	289.185	N/A
11	virtex6	ISE	14.7	6vlx240tff1156-1	1338	1124	267.881	N/A
12	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	1734	908	N/A	N/A
12	zynq	Vivado	2017.1	xc7z020clg484-1	1743	992	N/A	N/A
12	zynq_ise	ISE	14.7	7z020clg484-1	1740	1156	289.185	N/A
12	virtex6	ISE	14.7	6vlx240tff1156-1	1740	1160	267.881	N/A

Test and Verification

Two test cases are implemented to validate the CIC Decimator component:

1. Unity gain response to DC: The CIC Decimator gain is calculated using the following equation:

$$CIC\ Gain = \frac{(R * M)^N}{2^{CEIL(N * log_2(R * M))}} \tag{3}$$

2. Tone waveform: A waveform containing tones at 50 Hz, 100 Hz and Fs/R sampled at 1024000 is processed by the worker. The tones at 50 Hz and 100 Hz are within the bandwidth of the filter, while the Fs/R tone is at the first null. The power levels of the input tones and output tones are measured and compared.

For the plots below, a CIC decimator with the following parameter set was used: `N`=3, `M`=1, `R`=2048, and `ACC_WIDTH`=49.

For Case #1, the plots below show the input with the I-leg zoomed in the show the amplitude is 32767, and output data with the I-leg zoomed to show an amplitude of 32767, which can be calculated using 3, shown below, and the Q-leg showing the worker delay before reaching it steady-state value.

$$OutputAmplitude = 32767 * \frac{(2048 * 1)^3}{2^{CEIL(3 * log_2(2038 * 1))}} = 32767 * 1 = 32767 \tag{4}$$

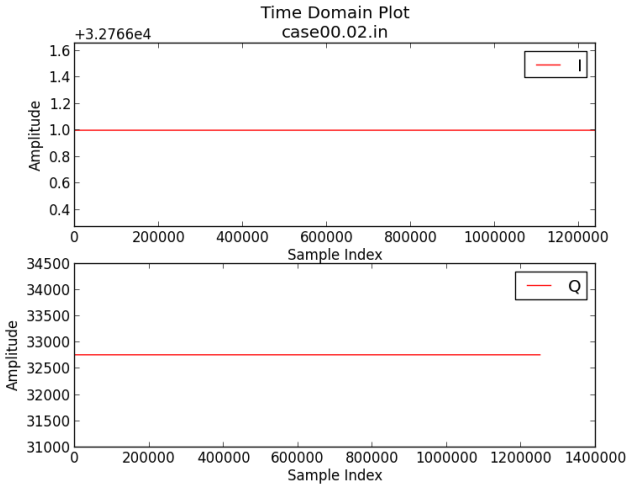

Figure 3: Time Domain: DC with amp=32767

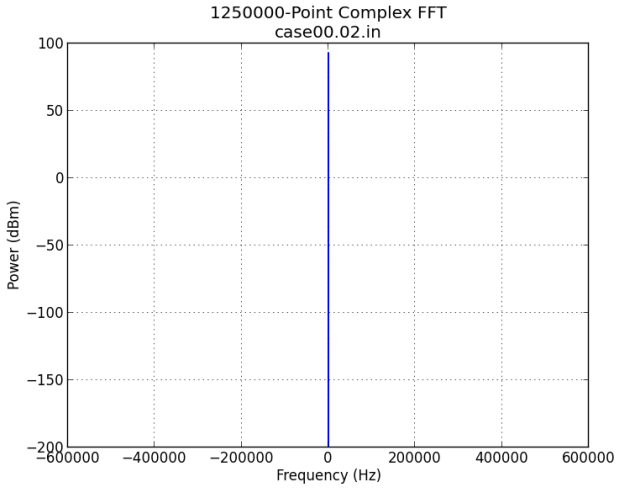

Figure 4: Frequency Domain: 0 Hz

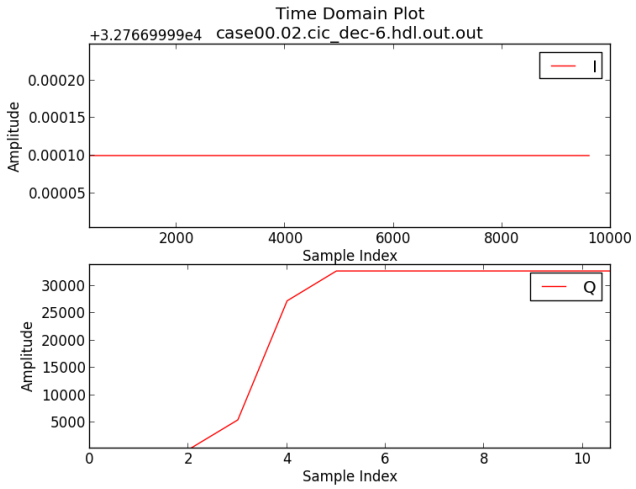

Figure 5: Time Domain: DC with amp=32767

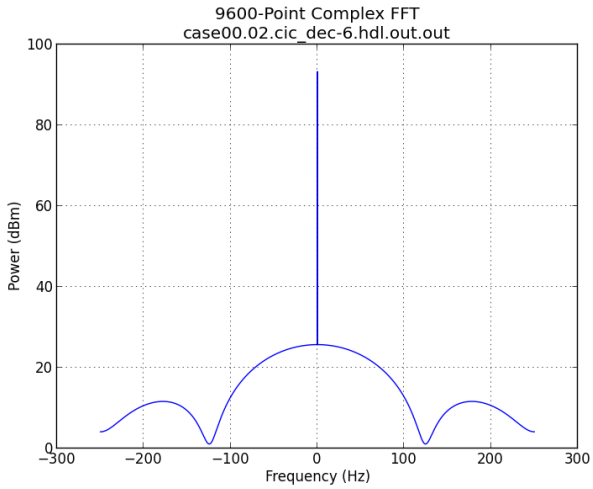

Figure 6: Frequency Domain: 0 Hz

For Case #2, the plots below show the input and output data (I-leg zoomed). The input plots show a complex waveform with frequency=50 Hz, 100 Hz, Fs/R Hz, where Fs=1024000 Hz and R=2048. The output FFT plot shows the Fs/R Hz has been filtered by the CIC decimator, but 50 Hz, 100 Hz were retained because they are within the bandwidth of the filter.

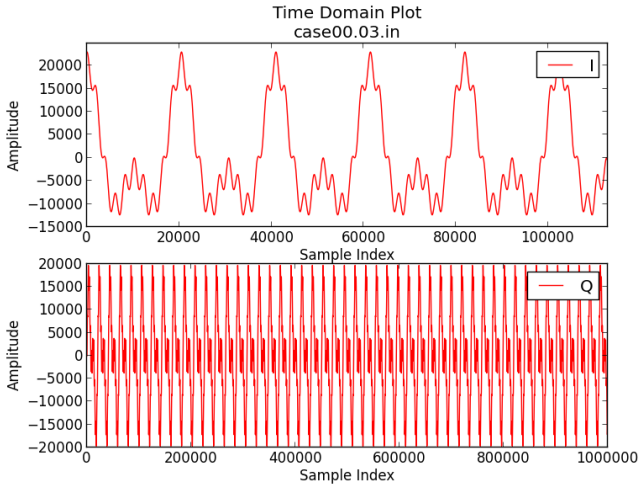

Figure 7: Time Domain

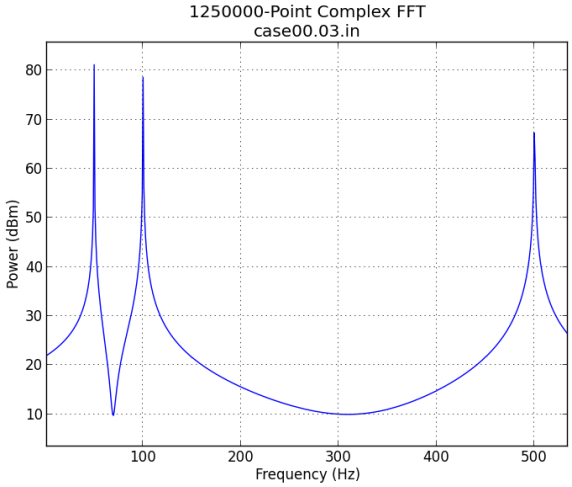

Figure 8: Frequency Domain: 50 Hz, 100 Hz, 1024000/2048 Hz

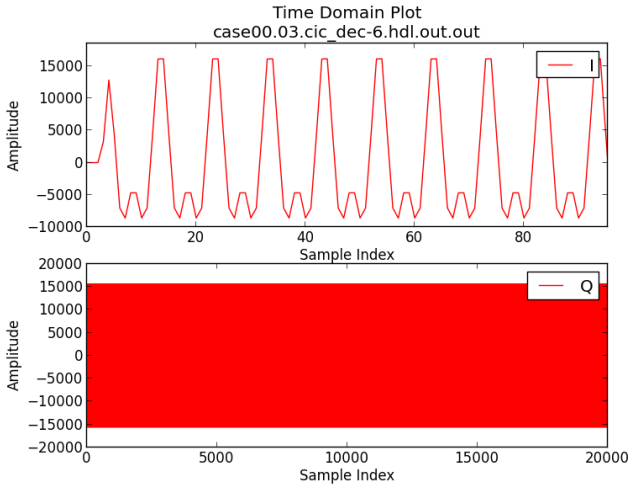

Figure 9: Time Domain

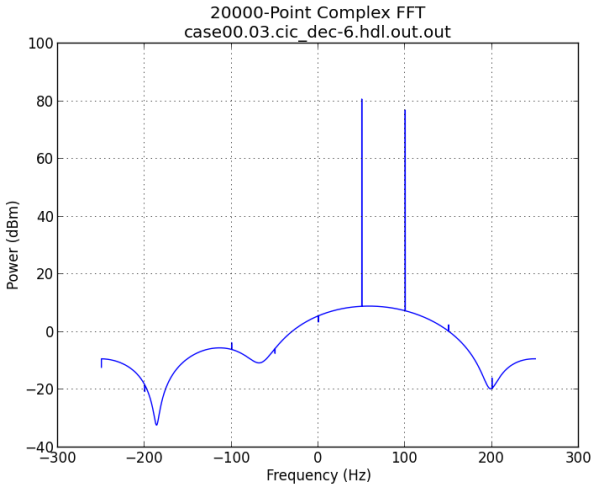

Figure 10: Frequency Domain: 50 Hz, 100 Hz

References

(1) Ronald E. Crochiere and Lawrence R. Rabiner. Multirate Digital Signal Processing. Prentice-Hall Signal Processing Series. Prentice Hall, Englewood Cli_s, 1983.
(2) Eugene B. Hogenauer, An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, No. 2, April 1981.
(3) Matthew P. Donadio, CIC Filter Introduction, http://home.mit.bme.hu/ kollar/papers/cic.pdf