Summary - AD9361 SPI

Name	ad9361_spi
Worker Type	Device
Version	v1.3
Release Date	Aug 2017
Component Library	ocpi.devices
Workers	ad9361_spi.hdl
Tested Platforms	Zedboard (ISE), Zedboard (Vivado), ML605 (FMC LPC slot)

Functionality

The AD9361 SPI subdevice worker implements a SPI state machine for communication with the AD9361 IC[1].

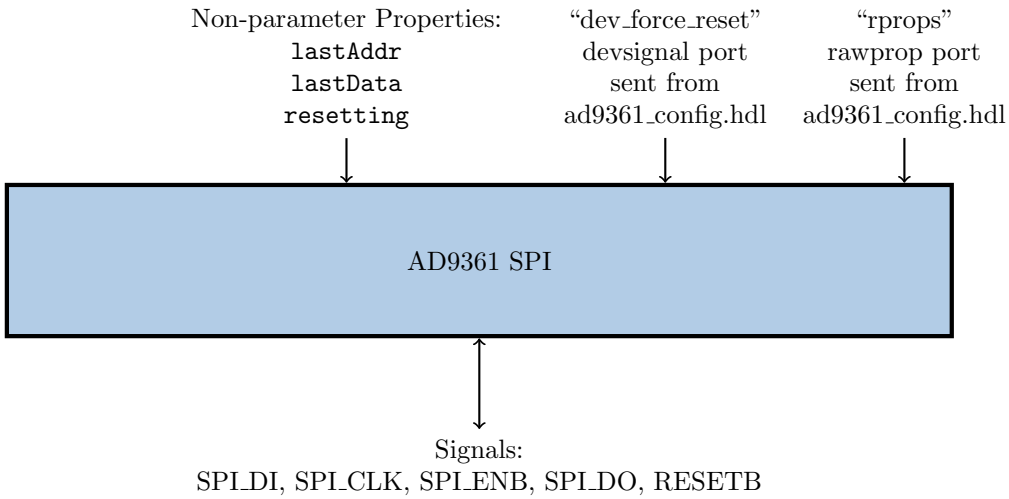
Worker Implementation Details

ad9361_spi.hdl

The ad9361_spi.hdl subdevice worker is intend for use in platforms/cards where a SPI bus exists which addresses only the AD9361. SPI read/writes are actuated by the `rprops` rawprop port. A devsignal is also sent in which can force the AD9361 RESETB pin, which is active-low, to logic 0.

Block Diagrams

Top level



Source Dependencies

ad9361_spi.hdl

- opencpi/hdl/devices/ad9361_spi.hdl/comp.vhd
- opencpi/hdl/devices/ad9361_spi.hdl/signals.vhd
- opencpi/hdl/primitives/util/spi.vhd
- opencpi/hdl/primitives/util/util_pkg.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
CP_CLK_FREQ_HZ_p	Float	-	-	Parameter	Standard	100e6	Value will determine assumed frequency of the Control Plane (CP) clock. This value is used to calculate the dividor for the SPI clock
SPI_CLK_FREQ_HZ_p	Bool	-	-	Parameter	Standard	6.25e6	-
lastAddr	UShort	-	-	Volatile	Standard	-	-
lastAddr	UChar	-	-	Volatile	Standard	-	-
lastAddr	Bool	-	-	Volatile	Standard	-	-

Worker Properties

ad9361_spi.hdl

Scope	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
-	-	-	-	-	-	-	-	-

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

Worker Interfaces

ad9361_spi.hdl

Type	Name	Optional	Usage
RawProp	rprops	True	-

Type	Name	Count	Optional	Master	Signal	Direction	Width	Description
DevSignal	dev_force_spi_reset	1	False	False	force_reset	Output	1	Used to force AD9361 RESETB pin, which is active-low, to logic 0.

Control Timing and Signals

The AD9361 SPI.hdl device worker operates entirely in the control plane clock domain. All SPI data and SPI clock signals are generated in the control plane clock domain. Note that SPI clock can only be a divided version of the control plane clock.

Performance and Resource Utilization

ad9361_spi.hdl

Fmax refers to the maximum allowable clock rate for any registered signal paths within a given clock domain for an FPGA design. Fmax in the table below is specific only to this worker and represents the maximum possible Fmax for any OpenCPI bitstream built with this worker included. Note that the Fmax value for a given clock domain for the final bitstream is often worse than the Fmax specific to this worker, even if this worker is the only one included in the bitstream.

Table entries are a result of building the worker with the following parameter property sets:

- `CP_CLK_FREQ_HZ_p`=100e6
- `SPI_CLK_FREQ_HZp`=6.25e6

Device	Registers (typical)	LUTs (typical)	Fmax (typical)	Memory/Special Functions	Design Suite
Zynq XC7Z020-1-CLG484	67	97	315 MHz [1]	-	Vivado 2017.1
	64	121	430 MHz	-	ISE 14.7
Virtex-6 XC6VCX75T-2FF484	64	131	437 MHz	-	ISE 14.7
Stratix IV EP4SGX230K-C2-F40	70	140	2	-	Quartus Prime 15.1

- `CP_CLK_FREQ_HZ_p`=125e6
- `SPI_CLK_FREQ_HZp`=6.25e6

Device	Registers (typical)	LUTs (typical)	Fmax (typical)	Memory/Special Functions	Design Suite
Zynq XC7Z020-1-CLG484	68	98	280 MHz [1]	-	Vivado 2017.1
	65	126	444 MHz	-	ISE 14.7
Virtex-6 XC6VCX75T-2FF484	65	134	412 MHz	-	ISE 14.7
Stratix IV EP4SGX230K-C2-F40	71	140	2	-	Quartus Prime 15.1

Test and Verification

The test outlined in [3] includes validation of a subset of this worker's functionality.

References

[1] AD9361 Datasheet and Product Info
`http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband-transceivers-ic/ad9361.html`

[2] AD9361 Reference Manual UG-570
AD9361_Reference_Manual_UG-570.pdf

[3] AD361 DAC Component Data Sheet
AD9361_DAC.pdf

[1] These measurements were the result of a Vivado timing analysis which was different from the Vivado analysis performed by default for OpenCPI worker builds. For more info see Appendix 1

[2] Quartus does not perform timing analysis at the OpenCPI worker build (i.e. synthesis) stage.

1 Appendix - Vivado Timing Analysis

The Vivado timing report that OpenCPI runs for device workers may erroneously report a max delay for a clocking path which should have been ignored. Custom Vivado tcl commands had to be run for this device worker to extract pertinent information from Vivado timing analysis. After building the worker, the following commands were run from the base project directory (after the Vivado settings64.sh was sourced):

```
cd hdl/devices/
vivado -mode tcl
```

Then the following commands were run inside the Vivado tcl terminal for the parameter property set:

- `CP_CLK_FREQ_HZ_p`=100e6
- `SPI_CLK_FREQ_HZp`=6.25e6

```
open_project ad9361_spi.hdl/target-zynq/ad9361_spi_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_spi_rv -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets {ctl_in[Clk]}]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
```

The following is the output of the timing report. The Fmax for the control plane clock for this worker is computed as the maximum magnitude slack with a control plane clock of 1 ps plus 2 times the assumed 1 ps control plane clock period (3.169 ns + 0.002 ns = 3.171 ns, 1/3.171 ns = 315.36 MHz).

```
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk1


Timing Report


Slack (VIOLATED) :     -3.169ns (required time - arrival time)
  Source:              wci/wci_decode/my_control_op_r_reg[0]/C
                         (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Destination:         wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
                         (rising edge-triggered cell FDSE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Path Group:          clk1
  Path Type:           Setup (Max at Slow Process Corner)
  Requirement:         0.002ns (clk1 rise@0.002ns - clk1 rise@0.000ns)
  Data Path Delay:     2.918ns (logic 0.937ns (32.111%) route 1.981ns (67.889%))
  Logic Levels:        2  (LUT6=2)
  Clock Path Skew:     -0.049ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
    Source Clock Delay    (SCD):   0.973ns
    Clock Pessimism Removal (CPR): 0.000ns
  Clock Uncertainty:   0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter   (TSJ):   0.071ns
    Total Input Jitter    (TIJ):   0.000ns
    Discrete Jitter        (DJ):   0.000ns
    Phase Error            (PE):   0.000ns

    Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
  -------------------------------------------------------------------- -------------------
                       (clock clk1 rise edge)    0.000    0.000 r
                                                 0.000    0.000 r ctl_in[Clk] (IN)
                       net (fo=66, unset)        0.973    0.973   wci/wci_decode/ctl_in[Clk]
                       FDRE                                    r  wci/wci_decode/my_control_op_r_reg[0]/C
  -------------------------------------------------------------------- -------------------
                       FDRE (Prop_fdre_C_Q)      0.518    1.491 r wci/wci_decode/my_control_op_r_reg[0]/Q
```

```
                    net (fo=6, unplaced)      0.997    2.488   wci/wci_decode/wci_control_op[0]
                                                        r  wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/I0
                    LUT6 (Prop_lut6_I0_O)     0.295    2.783 r wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2/O
                    net (fo=4, unplaced)      0.473    3.256   wci/wci_decode/ctl_out[SResp][1]_INST_0_i_2_n_0
                                                        r  wci/wci_decode/FSM_onehot_my_access_r[4]_i_2/I3
                    LUT6 (Prop_lut6_I3_O)     0.124    3.380 r wci/wci_decode/FSM_onehot_my_access_r[4]_i_2/O
                    net (fo=8, unplaced)      0.511    3.891   wci/wci_decode/my_access_r
                    FDSE                                 r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/CE
  ------------------------------------------------------------------- -------------------

                    (clock clk1 rise edge)    0.002    0.002 r
                                              0.000    0.002 r ctl_in[Clk] (IN)
                    net (fo=66, unset)        0.924    0.926   wci/wci_decode/ctl_in[Clk]
                    FDSE                                 r  wci/wci_decode/FSM_onehot_my_access_r_reg[0]/C
                    clock pessimism           0.000    0.926
                    clock uncertainty        -0.035    0.891
                    FDSE (Setup_fdse_C_CE)   -0.169    0.722   wci/wci_decode/FSM_onehot_my_access_r_reg[0]
  -------------------------------------------------------------------
                    required time                      0.722
                    arrival time                      -3.891
  -------------------------------------------------------------------
                    slack                             -3.169
```

```
report_timing: Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 2091.074 ; gain = 497.523 ; free physical = 13904 ; free virtual = 87949
```

Then the following commands were run inside the Vivado tcl terminal for the parameter property set:

- CP_CLK_FREQ_HZ_p=125e6
- SPI_CLK_FREQ_HZp=6.25e6

```
open_project ad9361_spi.hdl/target-1-zynq/ad9361_spi_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_spi_rv_c1 -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets {ctl_in[Clk]}]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
```

The following is the output of the timing report. The Fmax for the control plane clock for this worker is computed as the maximum magnitude slack with a control plane clock of 1 ps plus 2 times the assumed 1 ps control plane clock period (3.567 ns + 0.002 ns = 3.569 ns, 1/3.569 ns = 280.19 MHz).

```
Vivado% report_timing -delay_type min_max -sort_by slack -input_pins -group clk1

Timing Report

Slack (VIOLATED) :      -3.567ns (required time - arrival time)
  Source:               worker/spi/clk_count_r_reg[4]/C
                          (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Destination:          worker/spi/bit_count_r_reg[0]/CE
                          (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
  Path Group:           clk1
  Path Type:            Setup (Max at Slow Process Corner)
  Requirement:          0.002ns (clk1 rise@0.002ns - clk1 rise@0.000ns)
  Data Path Delay:      3.316ns (logic 1.061ns (31.996%) route 2.255ns (68.004%))
  Logic Levels:         3  (LUT5=2 LUT6=1)
```

```
Clock Path Skew:      -0.049ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
  Source Clock Delay    (SCD):   0.973ns
  Clock Pessimism Removal (CPR): 0.000ns
Clock Uncertainty:    0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter  (TSJ):   0.071ns
  Total Input Jitter   (TIJ):   0.000ns
  Discrete Jitter       (DJ):   0.000ns
  Phase Error           (PE):   0.000ns

  Location           Delay type              Incr(ns) Path(ns)   Netlist Resource(s)
------------------------------------------------------------------- -------------------
                     (clock clk1 rise edge)    0.000    0.000 r
                                               0.000    0.000 r ctl_in[Clk] (IN)
                     net (fo=67, unset)        0.973    0.973   worker/spi/ctl_in[Clk]
                     FDRE                                   r  worker/spi/clk_count_r_reg[4]/C
------------------------------------------------------------------- -------------------
                     FDRE (Prop_fdre_C_Q)      0.518    1.491 r worker/spi/clk_count_r_reg[4]/Q
                     net (fo=5, unplaced)      0.834    2.325   worker/spi/sel0[4]
                                                        r  worker/spi/bit_count_r[4]_i_5/I0
                     LUT5 (Prop_lut5_I0_O)     0.295    2.620 r worker/spi/bit_count_r[4]_i_5/O
                     net (fo=2, unplaced)      0.460    3.080   worker/spi/bit_count_r[4]_i_5_n_0
                                                        r  worker/spi/bit_count_r[4]_i_3/I4
                     LUT6 (Prop_lut6_I4_O)     0.124    3.204 r worker/spi/bit_count_r[4]_i_3/O
                     net (fo=2, unplaced)      0.460    3.664   worker/spi/bit_count_r[4]_i_3_n_0
                                                        r  worker/spi/bit_count_r[4]_i_1/I4
                     LUT5 (Prop_lut5_I4_O)     0.124    3.788 r worker/spi/bit_count_r[4]_i_1/O
                     net (fo=5, unplaced)      0.501    4.289   worker/spi/bit_count_r[4]_i_1_n_0
                     FDRE                                   r  worker/spi/bit_count_r_reg[0]/CE
------------------------------------------------------------------- -------------------

                     (clock clk1 rise edge)    0.002    0.002 r
                                               0.000    0.002 r ctl_in[Clk] (IN)
                     net (fo=67, unset)        0.924    0.926   worker/spi/ctl_in[Clk]
                     FDRE                                   r  worker/spi/bit_count_r_reg[0]/C
                     clock pessimism           0.000    0.926
                     clock uncertainty        -0.035    0.891
                     FDRE (Setup_fdre_C_CE)   -0.169    0.722   worker/spi/bit_count_r_reg[0]
------------------------------------------------------------------------
                     required time                       0.722
                     arrival time                       -4.289
------------------------------------------------------------------------
                     slack                              -3.567



report_timing: Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 2091.832 ; gain = 497.520 ; free physical = 13906 ; free virtual = 8795
```