

Summary - E3xx

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| | |
| Name | e3xx |
| Worker Type | Platform |
| Version | v1.4 |
| Release Date | Sept 2018 |
| Component Library | ocpi.bsp.e310.platforms |
| Workers | e3xx |

Functionality

The E3xx Platform worker is the interface between the Processing System and the FPGA on the Ettus E310 Platform. It makes the connections between the AXI buses on the ARM and the OpenCPI Control and Data Planes.

Worker Implementation Details

The E3XX Platform Worker provides the device, device proxy, and application workers with interfaces to the control and data planes as necessary. The Platform Worker also instantiates and connects to the time_server.hdl device worker. A block diagram of the full Board Support Package, including device workers, device proxy workers, the platform Worker, and their connections is shown below:

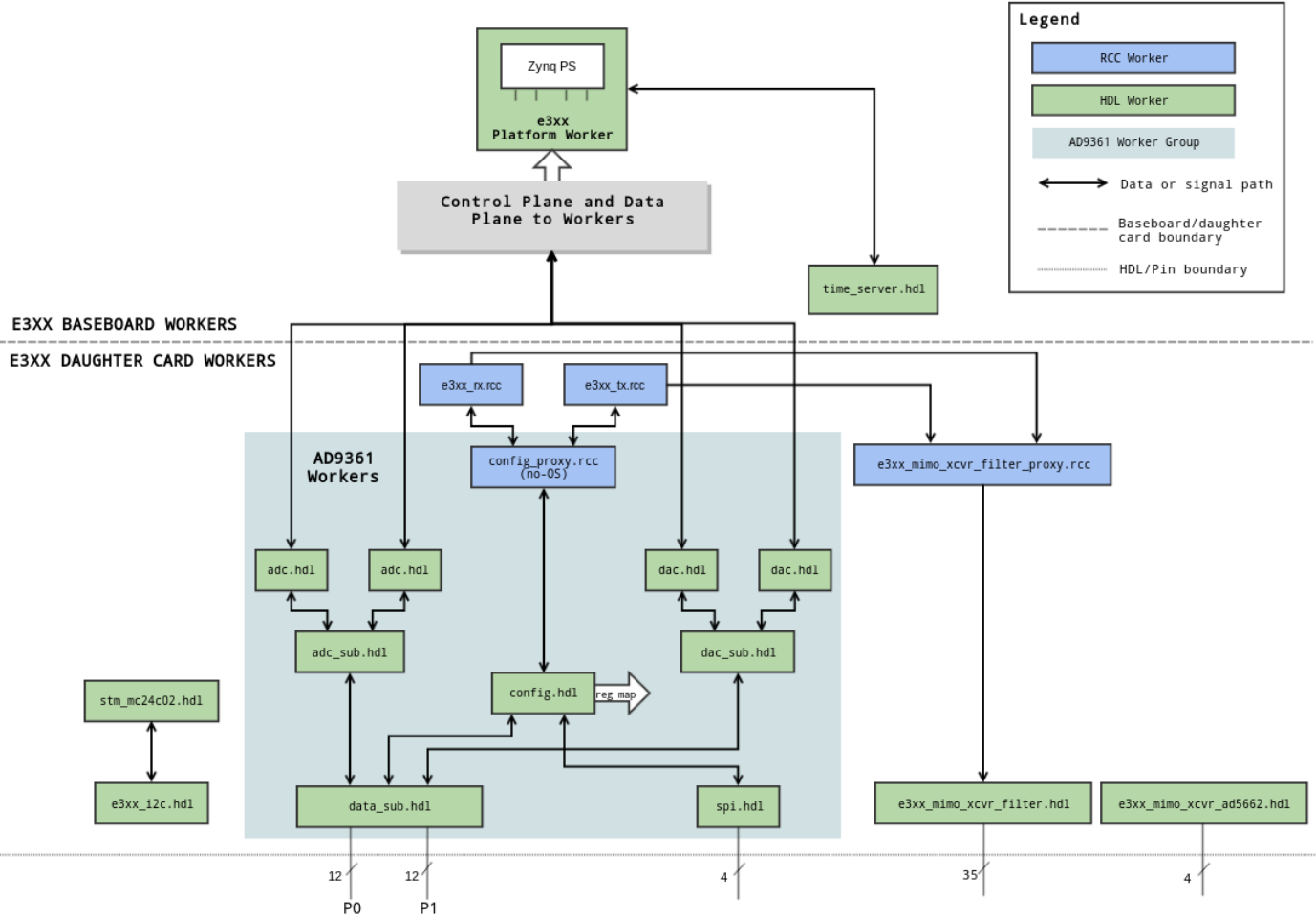


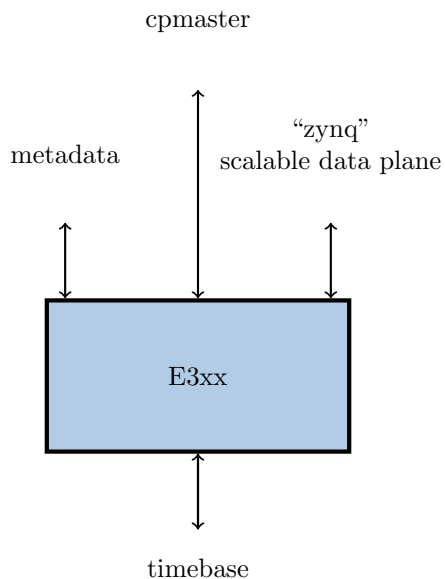
Figure 1: E3XX BSP - Top Level Block Diagram

Daughterboard

This platform contains a daughterboard which is comprised of an AD9361 RF IC, an analog filter bank along with control signals, and an AD5662 IC. Each of these has one or more device workers and/or a device proxy worker for control. Because the AD9361 device workers are platform-agnostic, they do not contain E310-specific support. More information on each of these workers can be found in its respective data sheet.

Block Diagrams

Top level



State Machines

Various state machines exist in the zynq, axi, and sdp primitive libraries. See primitive library source code for details. The explicit source code files included in the aforementioned primitives are enumerated in the following section.

Source Dependencies

- `ocpi.bsp.e310/hdl/platforms/e3xx/e3xx.vhd`
- `opencpi/hdl/primitives/zynq/zynq_pkg.vhd`
- `opencpi/hdl/primitives/zynq/zynq_ps.vhd`
- `opencpi/hdl/primitives/axi/axi_pkg.vhd`
- `opencpi/hdl/primitives/axi/axi2cp.vhd`
- `opencpi/hdl/primitives/sdp/sdp2axi_rd.vhd`
- `opencpi/hdl/primitives/sdp/sdp2axi.vhd`
- `opencpi/hdl/primitives/sdp/sdp2axi_wd.vhd`
- `opencpi/hdl/primitives/sdp/sdp_axi_pkg.vhd`
- `opencpi/hdl/primitives/sdp/sdp_pkg.vhd`
- `opencpi/hdl/primitives/sdp/sdp_body.vhd`

Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|-------------------|-----------|----------------|-----------------|--------------------|-------------|---------|---|
| platform | String | 31 | - | Parameter | Standard | - | Name of this platform |
| sdp_width | UChar | - | - | Parameter | Standard | 1 | Width of data plane in DWORDS |
| UUID | ULong | - | 16 | Readable | Standard | - | UUID of this platform |
| oldtime | ULongLong | - | - | Padding | Standard | - | N/A |
| romAddr | UShort | - | - | Writable | Standard | - | |
| romData | ULong | - | - | Volatile | Standard | - | |
| nSwitches | ULong | - | - | Readable | Standard | - | Number of switches |
| nLEDs | ULong | - | - | Readable | Standard | - | Number of LEDs |
| memories_length | ULong | - | - | Readable | Standard | - | |
| memories | ULong | - | 4 | Readable | Standard | - | The memory regions that may be used by various other elements, which indicates aliasing etc. The values describing each region are: Bit 31:28 - External bus/BAR connected to this memory (0 is none) Bit 27:14 - Offset in bus/BAR of this memory (4KB units) Bit 13:0 - Size of this memory (4KB units) units) |
| dna | ULongLong | - | - | Readable | Standard | - | DNA (unique chip serial number) of this platform |
| switches | ULong | - | - | Volatile | Standard | - | Current value of any switches in the platform |
| LEDS | ULong | - | - | Writable, Readable | Standard | - | Setting of LEDs in the platform, with readback |
| nSlots | ULong | - | - | Parameter | Standard | 0 | Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property. |
| slotNames | String | 32 | - | Parameter | Standard | "" | A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property. |
| slotCardIsPresent | Bool | - | 64 | Volatile | Standard | - | An array of booleans, where each index contains an indication whether a card is physically present in the given index's slot. For a description of a given index's slot, see the corresponding comma-separated string contents in the slotName property. Note that only the first min(nSlots,64) of the 64 indices contain pertinent information. |

Worker Properties

| Property Type | Name | Data Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|---------------|---------------|-----------|----------------|-----------------|---------------|-------------|-----------|--|
| SpecProperty | platform | String | 31 | - | Parameter | Standard | e3xx | Name of this platform |
| SpecProperty | nSlots | ULong | - | - | Parameter | Standard | 1 | Number of slots available for cards, which indicates the usable length of the slotCardIsPresent array property. |
| SpecProperty | slotNames | String | 32 | - | Parameter | Standard | e3xx-conn | A string which is intended to include comma-separated names of the slots available for cards. The inter-comma position of each name corresponds to the same index of the slotCardIsPresent array property. |
| Property | useGP1 | Bool | - | - | Parameter | Standard | false | |
| Property | axi_error | Bool | - | 4 | Volatile | Standard | - | |
| Property | sdpDropCount | UChar | - | - | Volatile | Standard | - | |
| Property | debug_state | ULongLong | - | 4 | Volatile | Standard | - | |
| Property | debug_state1 | ULongLong | - | 4 | Volatile | Standard | - | |
| Property | debug_state2 | ULongLong | - | 4 | Volatile | Standard | - | |
| Property | onswitch_db_p | Bool | - | - | Volatile | Standard | - | Property required to force a pull-up on the ON_SWITCH_DB pin. This is required because the compilation tools seem to otherwise optimize out the pull-up. |

Component Ports

No ports are implemented for the given component specification.

Worker Interfaces

| Type | Name | Master | Count | Usage |
|----------|------|--------|-------|--|
| metadata | - | true | - | Access to container metadata via the platform worker. All platform workers must provide this port. |
| timebase | - | true | - | Providing a timebase for the time service. All platform workers must provide this port. |
| cpmaster | - | true | - | This platform worker provides a control plane. |
| sdp | zynq | true | 4 | Scalable data plane. |

Worker Devices

The following is a table which enumerates which device workers are allowed in platform configurations and in assembly containers. The parameter values specify restricted/allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

| Name | Property Name | Property Value | Worker Signal | Platform Signal |
|-------------|---------------|---------------------|---------------|-----------------|
| time_server | frequency | 100*10 ⁶ | | |

Worker Devices on E3XX MIMO XCVR Card

The following is a table which enumerates which device workers are allowed in platform configurations and in assembly containers. The parameter values specify restricted/allowed implementations. Note that the worker signals listed are only those who are unconnected on the platform or whose platform signal name differ from the worker signal name. Note that device workers allowed by cards are not included in this list.

| Name | Property Name | Property Value | Worker Signal | Platform Signal |
|--------------------------|------------------|-----------------------------|---------------|-----------------|
| e3xx_mimo_xcvr_ad5662 | | | - | - |
| e3xx_i2c | | | - | - |
| e3xx_mimo_xcvr_filter | | | - | - |
| ad9361_spi | CP_CLK_FREQ_HZ_p | 100e6 | - | - |
| ad9361_config | | | - | - |
| ad9361_data_sub | lvds_p | false | - | - |
| | half_duplex_p | false | - | - |
| | single_port_p | true | - | - |
| | swap_ports_p | false (true also supported) | - | - |
| | DATA_CLK_Delay | 7 | - | - |
| | RX_Data_Delay | 0 | - | - |
| | FB_CLK_Delay | 12 | - | - |
| | TX_Data_Delay | 0 | - | - |
| ad9361_adc_sub | lvds_p | false | - | - |
| | half_duplex_p | false | - | - |
| | single_port_p | true | - | - |
| ad9361_dac_sub | lvds_p | false | - | - |
| | half_duplex_p | false | - | - |
| | single_port_p | true | - | - |
| ad9361_adc0 ¹ | - | - | - | - |
| ad9361_dac0 ¹ | - | - | - | - |
| ad9361_adc1 ¹ | - | - | - | - |
| ad9361_dac1 ¹ | - | - | - | - |

Signals

Note that this signal table does not include signals that may be provided by slots.

| Name | Type | Differential | Width | Description |
|-------------|--------|--------------|-------|---|
| PPS_EXT_IN | Output | false | 1 | Connected to time_server. Requires external connection. Note that the timer_server has not been thoroughly tested on this system. |
| ONSWITCH_DB | Input | false | 1 | Onswitch pin to be debounced - tied to pull-up and a volatile property. This is needed in order to enforce that the onswitch is tied to a pull-up, or the radio reboots when the bitstream is loaded. The volatile property forces the compilation tools <i>not</i> to optimize the signal and pull-up out. |

¹Depending on the mode (0rx1tx,1rx0tx,1rx1tx...2rx2tx), there may be between 0 and 2 ad9361_adc/dac workers in the platform configuration.

Slots

The following table enumerates the available slots for this platform and the signals they include. Note that the signals listed are only those who are unconnected on the platform or whose platform signal name do not match the slot signal name.

| Name | Type | Slot Signal | Platform Signal |
|-----------|-----------|-------------|-----------------|
| E3XX_CONN | e3xx_conn | - | - |

Platform Configurations

| Name | Platform Configuration Workers | Card | Slot |
|------------------------------------|--------------------------------|------|------|
| base | e3xx | - | - |
| | time_server | - | - |
| cfg-[0 1 2]rx-[0 1 2]tx_mode-[2 3] | e3xx | - | - |
| | time_server | - | - |
| | e3xx_mimo_xcvr_ad5662 | - | - |
| | e3xx_mimo_xcvr_filter | - | - |
| | e3xx_i2c | - | - |
| | ad9361_spi | - | - |
| | ad9361_data_sub | - | - |
| | ad9361_config | - | - |
| | ad9361_adc_sub | - | - |
| | ad9361_dac_sub | - | - |
| | ad9361_adc ¹ | - | - |
| | ad9361_dac ¹ | - | - |

Control Timing and Signals

Control Domain

All control clocking in the E3XX platform originates from the PS7 processing clock 1 (FCLK1), which is set to 100 MHz.

Sampling Domain

The sampling clock domain originates from the AD9361's DATA_CLK_P output. It is labeled CAT_DATA_CLK on the daughterboard connector, and is ultimately assigned to the E3XX_CONN_CAT_DATA_CLK input pin in the constraints file. This clock is routed to the AD9361 device workers (specifically ad9361_data_sub.hdl) via OpenCPI card/slot constructs.

This clock is used by the ad9361_adc_sub.hdl and ad9361_dac_sub.hdl workers. Additionally, the ad9361_dac_sub.hdl generates FB_CLK, which is routed through the card/slot to the E3XX_CONN_CAT_FB_CLK output pin in the constraints file. This clock is transmitted alongside TX data in a source synchronous fashion. See the AD9361 device worker documentation and ADI's UG-570 for more information regarding the relationships between these clocks.

¹Depending on the mode (0rx1tx,1rx0tx,1rx2tx...2rx2tx), there may be between 0 and 2 ad9361_adc/dac workers in the platform configuration.

Performance and Resource Utilization

Table 2: Resource Utilization Table for hdl-platform: e3xx

| Configuration | OCPI Target | Tool | Version | Device | Registers (Typ) | LUTs (Typ) | Fmax (MHz) (Typ) | Memory/Special Functions |
|-------------------------|-------------|--------|---------|-----------------|-----------------|------------|------------------|--|
| base | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 2290 | 2702 | N/A | BUFGCTRL: 1 BUFG: 1 |
| cfg_0rx_1tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 2899 | 3585 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 1 BUFG: 2 |
| cfg_0rx_1tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 2899 | 3585 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 1 BUFG: 2 |
| cfg_0rx_2tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3134 | 3810 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 2 BUFG: 2 |
| cfg_0rx_2tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3134 | 3810 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 2 BUFG: 2 |
| cfg_1rx_0tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3003 | 3544 | N/A | BUFGCTRL: 2 ODDR: 1 RAMB18E1: 1 BUFG: 2 |
| cfg_1rx_0tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3003 | 3544 | N/A | BUFGCTRL: 2 ODDR: 1 RAMB18E1: 1 BUFG: 2 |
| cfg_1rx_1tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3262 | 3805 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 2 BUFG: 2 |
| cfg_1rx_1tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3262 | 3805 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 2 BUFG: 2 |
| cfg_1rx_2tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3497 | 4030 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 3 BUFG: 2 |
| cfg_1rx_2tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3497 | 4030 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 3 BUFG: 2 |
| cfg_2rx_0tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3191 | 3677 | N/A | BUFGCTRL: 2 ODDR: 1 RAMB18E1: 2 BUFG: 2 |
| cfg_2rx_0tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3191 | 3677 | N/A | BUFGCTRL: 2 ODDR: 1 RAMB18E1: 2 BUFG: 2 |
| cfg_2rx_1tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3450 | 3938 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 3 BUFG: 2 |
| cfg_2rx_1tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3450 | 3938 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 3 BUFG: 2 |
| cfg_2rx_2tx_mode_2_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3685 | 4163 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 4 BUFG: 2 |
| cfg_2rx_2tx_mode_3_cmos | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 3685 | 4163 | N/A | BUFGCTRL: 2 ODDR: 8 RAMB18E1: 4 BUFG: 2 |

Note that there are many possible configurations of this platform. For each combination of CMOS Single/Dual Port, Half/Full Duplex and ports-swapped/not swapped, there is also a 0rx1tx, 1rx0tx, 1rx1tx, ... 2rx2tx. The resource utilization is only listed here for some of these, but can be extracted from the synthesized platform configuration for the supported modes. For now, the only supported modes are those corresponding to CMOS Single Port Full Duplex.

Test and Verification

Testing performed to verify functionality of the Platform Worker includes running of basic unit/application tests to test the Platform Worker itself, as well as device worker unit tests and system level application tests.

To test the basic functionality of the Platform Worker, simple applications such as `testbias` and unit tests such as `bias.test` were executed. These verify the basic functionality of the Platform Worker and its communication with the `xilinx13.4` Software Platform.

To further test the Platform Worker's functionality paired with its device workers, device worker unit tests were modified and performed for the AD9361 device workers, the E3XX XCVR Filter device worker and proxy, the AD5662 device worker, and the RX and TX proxy workers. Each of these tests has its own document that can be reviewed for further information.

Finally, OpenCPI reference applications were modified and tested on the E310 radio using the AD9361 workers in CMOS Single Port Full Duplex DDR mode. This provides a full system test along the RX and TX paths.