Component Data Sheet ANGRYVIPER Team

### Summary - TimeIQ to IQstream

Name	${ m timeiq\_to\_iqstream}$				
Worker Type	Application				
Version	1.5				
Release Date	4/2019				
Component Library	ocpi.assets.misc_comps				
Workers	timeiq_to_iqstream.hdl				
Tested Platforms	isim, xsim, modelsim, zed, matchstiq_z1, e3xx, alst4, ml605				

### **Functionality**

The TimeIQ to IQstream component adapts the TimeStamped IQ protocol to the iqstream protocol.

### Worker Implementation Details

#### $timeiq\_to\_iqstream.hdl$

The TimeStamped\_IQ protocol consists of multiple opcodes which include complex IQ samples, and the iqstream protocol consists only of complex IQ samples. The timeiq\_to\_iqstream worker inspects the opcode of the input port and only forwards data with the samples opcode.

### **Block Diagrams**

#### Top level



## Source Dependencies

#### $timeiq_to_iqstream.hdl$

 $\bullet \ bsp\_picoflexor/components/timeiq\_to\_iqstream.hdl/timeiq\_to\_iqstream.vhd\\$ 

# Component Spec Properties

There are no component spec properties for this component

# Worker Properties

There are no worker implementation-specific properties for this component

## **Component Ports**

Name	Producer	Protocol	Optional Advanced		$_{ m Usage}$		
in	n false TimeStamped_IQ-prot		false	-	Signed complex samples plus other operations		
out	out true iqstream_protocol		false	-	Signed complex samples		

### Worker Interfaces

### $timeiq\_to\_iqstream.hdl$

Type	Name	DataWidth	Advanced	Usage		
StreamInterface	in	32	-	Signed complex samples plus other operations		
StreamInterface	out	32	-	Signed complex samples		

# Control Timing and Signals

The timeiq\_to\_iqstreamworker uses the clock from the Control Plane and standard Control Plane signals.

# Worker Configuration Parameters

#### $timeiq\_to\_iqstream.hdl$

Table 1: Table of Worker Configurations for worker: timeiq\_to\_iqstream



## Performance and Resource Utilization

Table 2: Resource Utilization Table for worker "timeiq\_to\_iqstream"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	N/A	257	171	N/A	N/A
0	zynq	Vivado	2017.1	xc7z020clg400-3	257	255	N/A	N/A
0	zynq_ise	ISE	14.7	7z010clg400-3	248	407	398.756	N/A
0	virtex6	ISE	14.7	6vcx75tff484-2	248	407	315.751	N/A

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### Test and Verification

The input file contains message metadata and uses three different opcodes from the TimeStamped\_IQ protocol, and is formatted in the following manner:

- 1. 8 byte time operation
- 2. 8 byte interval operation
- 3. 2880 byte samples operation
- 4. 8 byte time operation
- 5. 2880 byte samples operation

The data in the samples operation is a ramp from 0 to 2087.

The expected output waveform is the identical ramp with all other operations removed. For verification, the output file is compared to a golden input file.