# OpenCPI E3xx MIMO RCVR Filter Proxy Test App Guide

#### Version 1.5

#### Revision History

Revision	Description of Change	Date
v1.4	Initial release.	9/2018
v1.5	Version bump only	4/2019

# 1 Description

This application is intended to perform a hardware-in-the-loop test of the e3xx\_mimo\_xcvr\_filter\_proxy.rcc device proxy. The application is meant to exercise the properties of the proxy worker dynamically while the application is running. The different modes of the frontend are cycled through for various different frequency/filter bank settings to visually verify the LEDs are responding appropriately. The following steps are taken in the application:

- 1. Set the frequency of the RX and TX LOs
- 2. Set the mode for Frontend A to TX,RX i.e. full duplex
- 3. Set the mode for Frontend B to TX,RX i.e. full duplex
- 4. Request user input for validation
- 5. Set the mode for Frontend A to RX,off
- 6. Set the mode for Frontend B to TX,RX i.e. full duplex
- 7. Request user input for validation
- 8. Set the mode for Frontend A to RX.off
- 9. Set the mode for Frontend B to RX,off
- 10. Request user input for validation
- 11. Set the mode for Frontend A to TX,RX i.e. full duplex
- 12. Set the mode for Frontend B to RX,off
- 13. Request user input for validation
- 14. Set the mode for Frontend A to TX,RX i.e. full duplex
- 15. Set the mode for Frontend B to off, off
- 16. Request user input for validation
- 17. Set the mode for Frontend A to off, off
- 18. Set the mode for Frontend B to TX,RX i.e. full duplex
- 19. Request user input for validation

- 20. Set the mode for Frontend A to off, off
- 21. Set the mode for Frontend B to off, off
- 22. Request user input for validation
- 23. Repeat steps 1 through 22 for each frequency being tested

# 2 Hardware Portability

This application is intended to test e3xx\_mimo\_filter\_proxy.rcc, which is by design specific to the e3xx platform.

## 3 Execution

# 3.1 Prerequisites

The following must be true before application execution:

- The following assets are built and their build artifacts (FPGA bitstream file/shared object file) are contained within the directory list of the OCPLLIBRARY\_PATH environment variable.
  - for e3xx/xilinx13\_4 HDL/RCC platforms:
    - \* empty/cnt\_e3xx\_mimo\_xcvr\_filter assembly/container
    - \* e3xx\_mimo\_xcvr\_filter\_proxy.rcc
- The current directory is the applications/e3xx\_mimo\_xcvr\_filter\_proxy\_test directory.

### 3.2 Command(s)

./<target-dir>/e3xx\_mimo\_xcvr\_filter\_proxy\_test

## 4 Verification

Verification is performed by running the application and visually verifying that the LEDs on the E3xx match the values printed to stdout. An application exit status which is non-zero indicates that the test could not complete.