XL9535, XL9555

16-bit I²C-bus and SMBus I/O port Expander With Interrupt Output and Configuration Registers

Rev. 2.3 — 2018

1. DESCRIPTION

This device (XL9535/XL9555) is a 24-pin CMOS IC that provides 16-bit of General Purpose parallel Input/Output (GPIO) expansion for most micro-controller families via the I²C-bus/SMBus interface [serial clock line (SCL), serial data line (SDA)]. These device is designed for 2.3-V to 5.5-V V_{CC} operation. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

These device consists of two 8-bit Configuration (Input or Output selection); Input Port, Output Port and Polarity Inversion (active-HIGH or active-LOW operation) registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

These device open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The system master can reset these device in the event of a timeout or other improper operation by utilizing the power-on reset feature. The power-on reset sets the registers to their default values and initializes the I²C/SMBus state machine. Three hardware address pins (A0, A1 and A2) vary the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus.

2. FEATURES

- I²C-bus to 16-bit GPIO expander
- Operating power supply voltage range of 2.3-V to 5.5-V
- Low standby current consumption
- 5 V tolerant I/O ports
- 400 kHz fast-mode I²C-bus clock frequency
- Noise filter on SCL/SDA inputs
- Internal power-on reset
- No glitch on power-up
- Polarity Inversion register
- Address by 3 hardware address pins for use of up to 8 devices
- Open-drain active LOW interrupt output
- 16 I/O pins which default to 16 inputs
- Latch-up testing exceeds 100 mA per JESD 78
- ESD protection exceeds JESD 22
  2000 V HBM, 200 V MM and 1000 V CDM

3. ORDERING INFORMATION

Table 1. Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL9535D	XL9535D	SOP24(300mil)	15.4 × 7.50	-40 to +85	MSL3	T&R 13"	1000
XL9535SS	XL9535SS	SSOP24(209mil)	8.20 × 5.30	-40 to +85	MSL3	T&R 13"	2500
XL9535	XL9535	TSSOP24	7.80 × 4.40	-40 to +85	MSL3	T&R 13"	4000
XL9535QF24	XL9535QF24	QFN24-4×4	4.00 × 4.00	-40 to +85	MSL3	T&R 13"	5000
XL9555D	XL9555D	SOP24(300mil)	15.4 × 7.50	-40 to +85	MSL3	T&R 13"	1000
XL9555SS	XL9555SS	SSOP24(209mil)	8.20 × 5.30	-40 to +85	MSL3	T&R 13"	2500
XL9555	XL9555	TSSOP24	7.80 × 4.40	-40 to +85	MSL3	T&R 13"	4000
XL9555QF24	XL9555QF24	QFN24-4×4	4.00 × 4.00	-40 to +85	MSL3	T&R 13"	5000

4. PIN CONFIGURATIONS AND FUNCTIONS

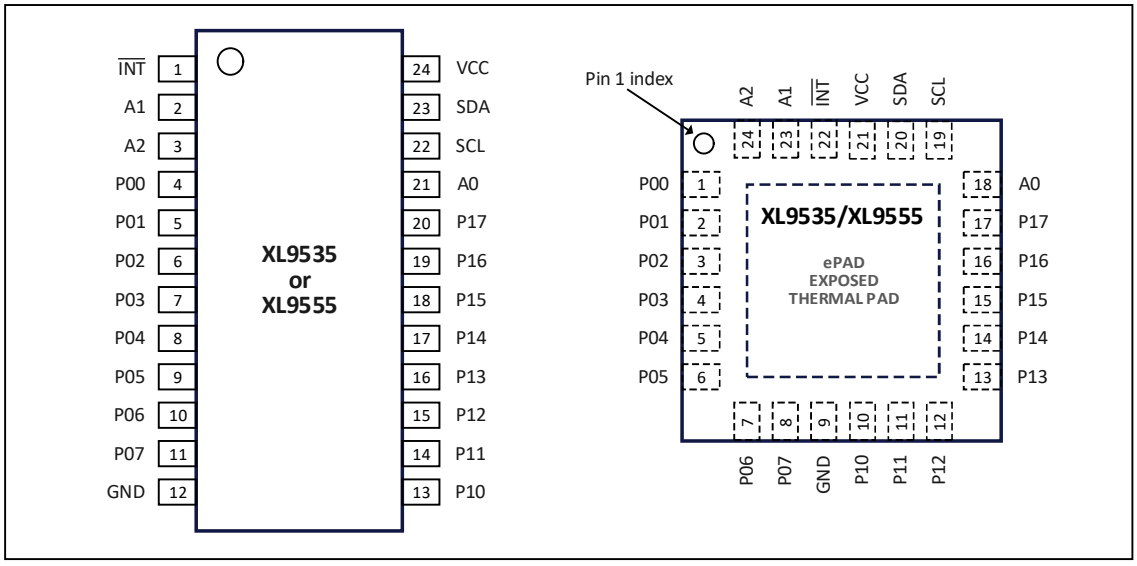


Figure 1. Pin configuration for SOP24/SSOP24/TSSOP24 (TOP VIEW)

Figure 2. Pin configuration for QFN24 (TOP VIEW)

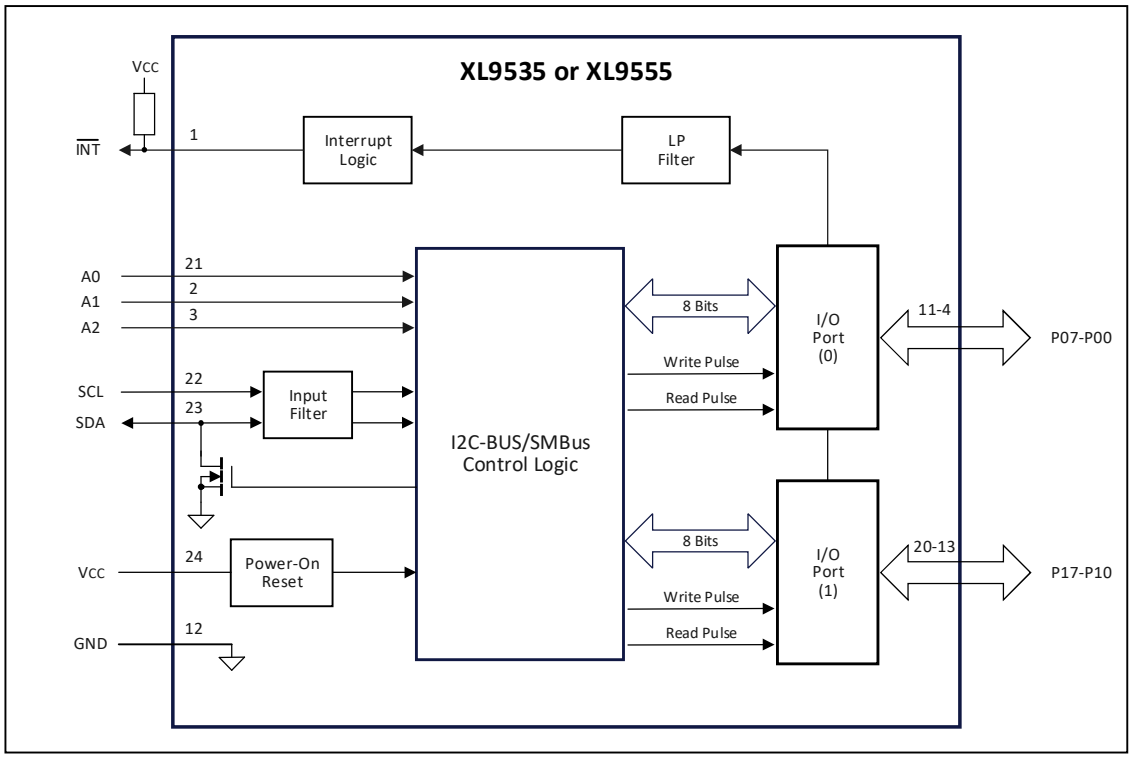
Table 2. Pin Functions

PIN NAME	PIN NUMBER		DESCRIPTION
	SOP/SSOP/TSSOP	QFN	
$\overline{INT}$	1	22	Interrupt output (open-drain). Connect to V_{CC} through a pull-up resistor.
A1	2	23	Address input 1. Connect directly to V_{CC} or ground.
A2	3	24	Address input 2. Connect directly to V_{CC} or ground.
P00	4	1	Port 0 input/output. Push-pull design structure. At power on, P00-P07 are configured as an input. [1]
P01	5	2	
P02	6	3	
P03	7	4	
P04	8	5	
P05	9	6	
P06	10	7	
P07	11	8	
GND	12	9 [2]	Supply ground.
P10	13	10	Port 1 input/output. Push-pull design structure. At power on, P10-P17 are configured as an input. [1]
P11	14	11	
P12	15	12	
P13	16	13	
P14	17	14	
P15	18	15	
P16	19	16	
P17	20	17	
A0	21	18	Address input 0. Connect directly to V_{CC} or ground.
SCL	22	19	Serial clock line. Connect to V_{CC} through a pull-up resistor.
SDA	23	20	Serial data line. Connect to V_{CC} through a pull-up resistor.
V_{CC}	24	21	Supply voltage.
ePAD	-	Y [2]	Exposed thermal pad. Connect directly to ground.

[1] XL9535 and XL9555 I/Os are totem pole. For XL9555 inside, note that there is a high value resistor tied to V_{CC} at each pin.

[2] QFN24 package die supply ground is connected to both the GND pin and the exposed thermal pad(ePAD). The GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the ePAD needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

5. FUNCTIONAL BLOCK DIAGRAM



REMARK: (1) All I/Os are set to inputs at reset.

(2) Pin numbers shown are for the TSSOP24 package.

Figure 3. Block Diagram

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings [3]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	+6	V
V_{IN}	Input pin voltage range [4]		-0.5	+6	V
V_O	Output pin voltage range [4]		-0.5	+6	V
I_{IK}	Input clamp current	V_{IN}<0	-	-20	mA
I_{OK}	Output clamp current	V_O<0	-	-20	mA
I_{IOK}	Input/output clamp current	V_O<0 or V_O>V_{CC}	-	±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}	-	+50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}	-	-50	mA
I_{CC}	Continuous current through GND		-	-250	mA
	Continuous current through V_{CC}		-	+160	mA
P_{tot}	Total Power Dissipation		-	200	mW
T_{stg}	Storage temperature range		-65	+150	℃
T_{amb}	Ambient temperature range	Operating	-40	+85	℃
MSL	Moisture Sensitivity			Level 3	

[3] Stresses exceeding those listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[4] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2. Thermal Resistance Characteristics

SYMBOL	PARAMETER	PACKAGE				UNIT
	TEST CONDITIONS	SOP24	SSOP24	TSSOP24	QFN24	
$R_{\theta JA}$	Package thermal impedance, Junction-to -ambient (free air) [5]	108.8	92.9	48.4	43.6	℃/W

[5] Measured with minimum pad spacing on an FR4 PCB board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.

6.3. ESD Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{ESD}	Electrostatic Discharge	Human Body Mode (HBM), all pins [6]	0	2000	V
		Charged Device Model (MM), all pins [7]	0	200	V
		Charged Device Model (CDM), all pins [8]	0	1000	V

[6] Tested to EIA / JESD22−A114−A.

[7] Tested to EIA / JESD22−A115−A.

[8] Tested to JESD22−C101−A.

6.4. Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	$V_{CC(MAX)}$ = 5.5V	2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7×V_{CC}	V_{CC}	V
		A2–A0, P07–P00, P17–P10	0.7×V_{CC}	V_{CC}	V
V_{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3×V_{CC}	V
		A2–A0, P07–P00, P17–P10	-0.5	0.3×V_{CC}	V
I_{OH}	High-level output current	P07–P00, P17–P10	-	-10	mA
I_{OL}	Low-level output current	P07–P00, P17–P10	-	25	mA
T_A	Operating free-air temperature		-40	+85	℃

6.5. Electrical Characteristics

V_{CC} = 2.3 V to 5.5 V; GND = 0 V; T_A = free-air temperature range; unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Power Supplies								
I_{CC}	Supply Current, in operating mode	XL9535	I/O = inputs, f_{SCL} = 100 kHz, I_O = 0, No load	5.5 V	-	135	200	µA
		XL9555	I/O = inputs, f_{SCL} = 100 kHz, I_O = 0, No load	5.5 V	-	135	200	µA
I_{STB}	Standby Current, in standby mode	XL9535	V_{IN} = GND, I/O = inputs, f_{SCL} = 0 kHz, I_O = 0, No load	5.5 V	-	0.25	1	µA

			V_{IN} = V_{CC} , I/O = inputs, f_{SCL} = 0 kHz, I_O = 0, No load	5.5 V	-	0.25	1	µA
		XL9555	V_{IN} = GND, I/O = inputs, f_{SCL} = 0 kHz, I_O = 0, No load	5.5 V	-	1.1	1.5	mA
			V_{IN} = V_{CC} , I/O = inputs, f_{SCL} = 0 kHz, I_O = 0, No load	5.5 V	-	0.25	1	µA
ΔI_{CC}	Additional current in standby mode	XL9535	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			200	µA
		XL9555	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
V_{PORR}	Power-on reset voltage, V_{CC} rising [9]		V_{IN} = V_{CC} or GND, I_O = 0, no load;		-	1.7	2.2	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_{IN} = V_{CC} or GND, I_O = 0, no load;		0.7	1	-	V
Input SCL; input/output SDA								
V_{IL}	LOW-level input voltage			2.3 V to 5.5 V	-0.5	-	0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage			2.3 V to 5.5 V	0.7×V_{CC}		5.5	V
I_{OL}	LOW-level output current		V_{OL} = 0.4 V	2.3 V to 5.5 V	3	-	-	mA
I_L	leakage current		V_{IN} = V_{CC} or GND	2.3 V to 5.5 V	-1	-	+1	µA
C_I	input capacitance		V_{IN} = GND	2.3 V to 5.5 V	-	6	10	pF
I/Os								
V_{IL}	LOW-level input voltage			2.3 V to 5.5 V	-0.5	-	0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage			2.3 V to 5.5 V	0.7×V_{CC}		5.5	V
I_{OL}	LOW-level output current [10]	XL9535	V_{OL} = 0.5 V	2.3 V to 5.5 V	8	10	-	mA
			V_{OL} = 0.7 V	2.3 V to 5.5 V	10	14	-	mA
		XL9555	V_{OL} = 0.5 V	2.3 V to 5.5 V	8	(8 to 20)	-	mA
			V_{OL} = 0.7 V	2.3 V to 5.5 V	10	(10 to 24)	-	mA
V_{OH}	HIGH-level output voltage [11]		I_{OH} = -8 mA	2.3 V	1.8	-	-	V
				3 V	2.6	-	-	V
				4.75 V	4.1	-	-	V
			I_{OH} = -10 mA	2.3 V	1.7	-	-	V
				3 V	2.5	-	-	V
				4.75 V	4	-	-	V
I_{LIH}	HIGH-level input leakage current		V_{IN} = V_{CC}	5.5 V	-	-	1	µA
I_{LIL}	LOW-level input leakage current	XL9535	V_{IN} = GND	5.5 V	-	-	-1	µA
		XL9555	V_{IN} = GND	5.5 V	-	-	-100	µA
C_I	input capacitance			2.3 V to 5.5 V	-	3.7	5	pF
C_O	output capacitance			2.3 V to 5.5 V	-	3.7	5	pF
Interrupt ($\overline{INT}$)								
I_{OL}			V_{OL} = 0.4 V	2.3 V to 5.5 V	3	-	-	mA
C_O	output capacitance			2.3 V to 5.5 V	-	3.7	5	pF
Select inputs A0, A1, A2								

V_{IL}	LOW-level input voltage		2.3 V to 5.5 V	-0.5	-	0.3×V_{CC}	V
V_{IH}	HIGH-level input voltage		2.3 V to 5.5 V	0.7×V_{CC}		5.5	V
I_L	leakage current	V_{IN} = V_{CC} or GND	2.3 V to 5.5 V	-1	-	+1	µA
C_I	input capacitance		2.3 V to 5.5 V	-	2.5	5	pF

[9] V_{CC} must be lowered than 0.2 V for at least 5 µs in order to reset the part.

[10] Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.

[11] The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

6.6. Dynamic Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

SYMBOL	PARAMETER	TEST CONDITIONS	Standard-mode		Fast-mode		UNIT
			MIN	MAX	MIN	MAX	
I²C-bus Interface Timing							
f_{SCL}	I²C-bus SCL Clock frequency		0	100	0	400	kHz
t_{BUF}	I²C-bus free time between a STOP and START Condition		4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition		4.0	-	0.6	-	µs
$t_{SU:STA}$	Set-up Time for a Repeated START Condition		4.7	-	0.6	-	µs
$t_{SU:STO}$	Set-up Time for STOP Condition		4.0	-	0.6	-	µs
$t_{VD:ACK}$	Data Valid Acknowledge Time [12]		0.3	3.45	0.1	0.9	µs
$t_{HD:DAT}$	Data Hold Time		0	-	0	-	ns
$t_{VD:DAT}$	Data Valid Time [13]		300	-	50	-	ns
$t_{SU:DAT}$	Data Set-up Time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	Fall Time of both SDA and SCL signals [14, 15]		-	300	20 + 0.1C_b [16]	300	ns
t_r	Rise Time of both SDA and SCL signals		-	300	20 + 0.1C_b [16]	300	ns
t_{sp}	Pulse Width of Spikes that must be Suppressed by the Input Filter [17]			50		50	ns
C_b	I²C-bus capacitive load [16]			400		400	pF
Port timing							
$t_{pv(Q)}$	Output data valid time [18]		-	200	-	200	ns
$t_{ps(D)}$	Input data set-up time		150	-	150	-	ns
$t_{ph(D)}$	Input data hold time		1	-	1	-	µs
Interrupt timing							
$t_{iv(INT\_N)}$	Interrupt valid time, on pin $\overline{INT}$		-	4	-	4	µs
$t_{irst(INT\_N)}$	Interrupt reset delay time, on pin $\overline{INT}$		-	4	-	4	µs

[12] $t_{VD:ACK}$ = time for Acknowledgment signal from SCL LOW to SDA (out) LOW.

[13] $t_{VD:DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[14] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[15] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.

[16] C_b = total capacitance of one bus line in pF.

[17] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

[18] $t_{pv(Q)}$ measured from 0.7×V_{CC} on SCL to 50 % I/O output (XL9535).(see Figure 6)

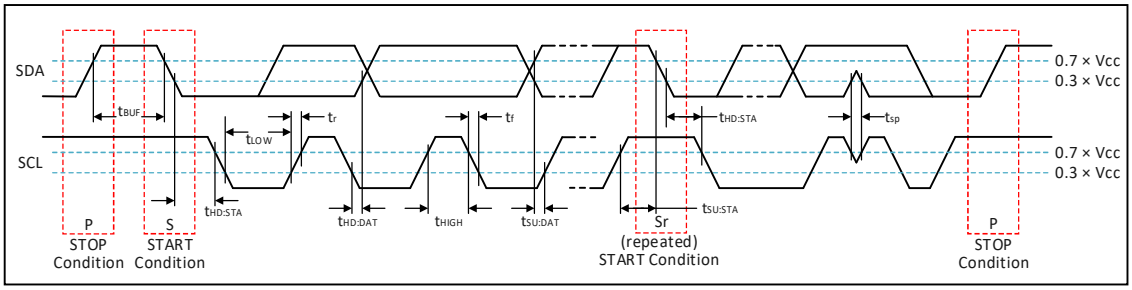


Figure 4. Definition of timing on the I²C-bus

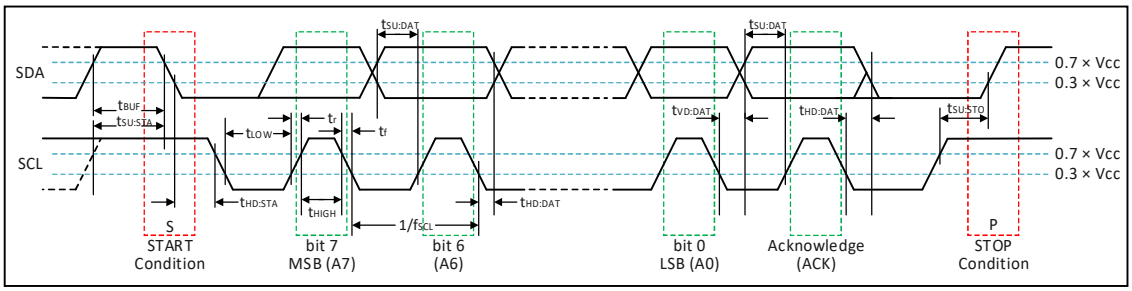


Figure 5. I²C-bus timing diagram

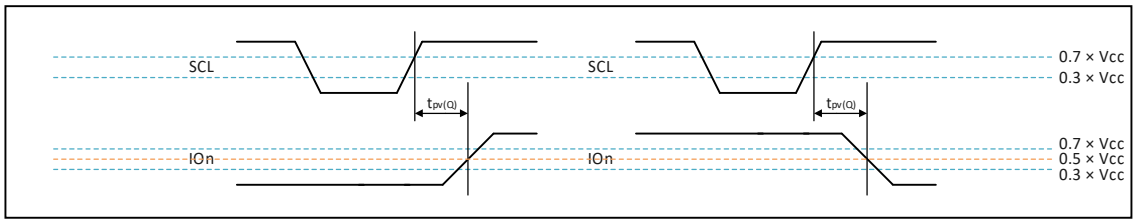
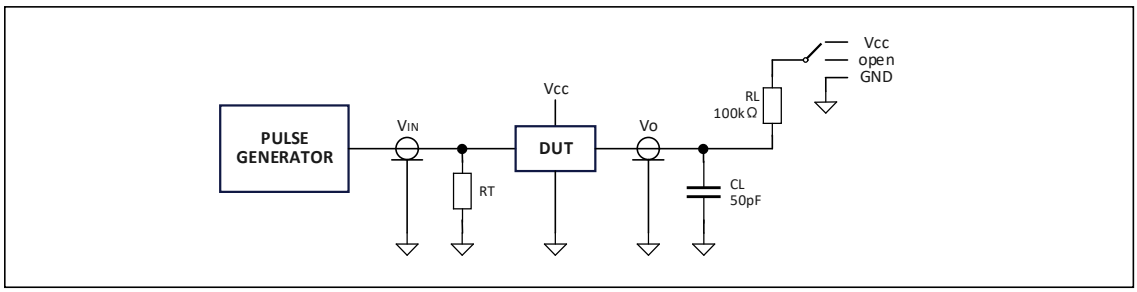


Figure 6. $t_{pv(Q)}$ timing

7. TEST INFORMATION



REMARK: R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Zo of the pulse generators.

Figure 7. Test circuitry for switching times

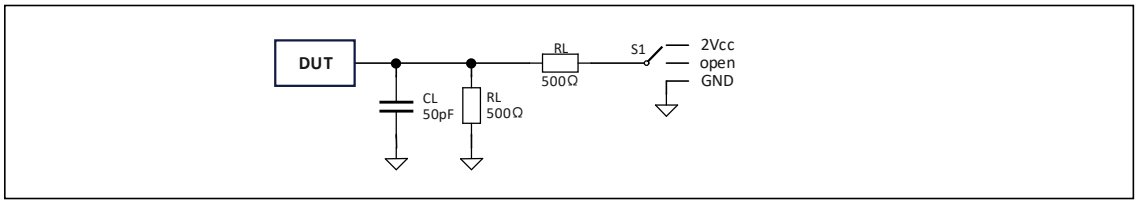


Figure 8. Load circuit

8. CHARACTERISTICS OF THE I²C-BUS INTERFACE

The bidirectional I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1. Bit Transfer

On the I²C-bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals (see Figure 9).

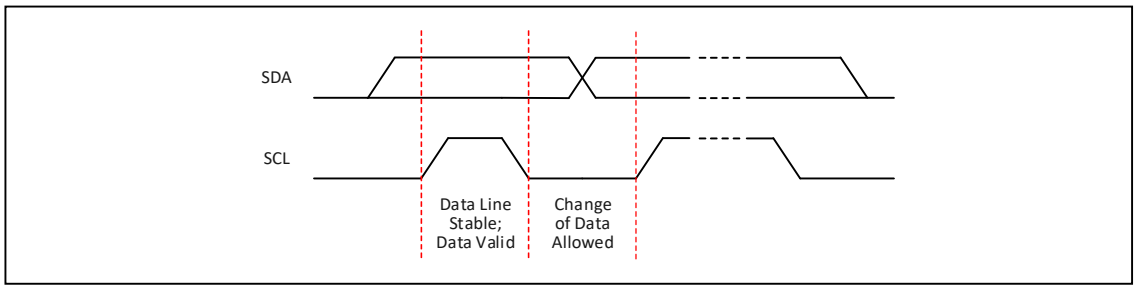


Figure 9. Bit Transfer

8.2. START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. I²C communication with this device is initiated by a master sending a START condition (S). A HIGH-to-LOW transition of the SDA data line input/output while the SCL clock is HIGH is defined as the START condition. A LOW-to-HIGH transition of the SDA data line input/output while the SCL clock is HIGH is defined as the STOP condition (P), is sent by the master (see Figure 10).

After the START condition, the device address byte is sent, MSB first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address.

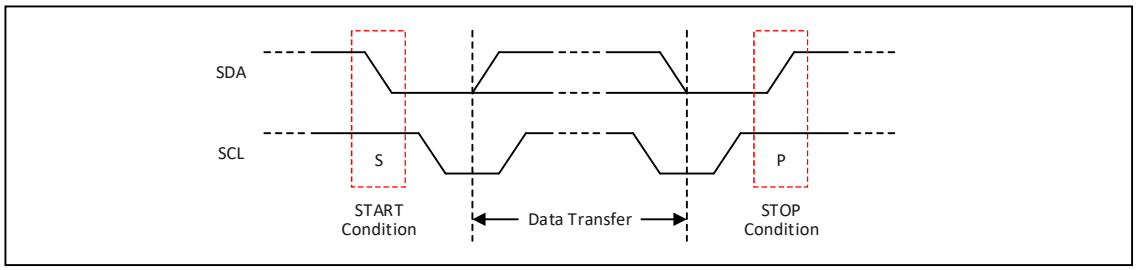


Figure 10. Definition of START and STOP Conditions

8.3. System Configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 11).

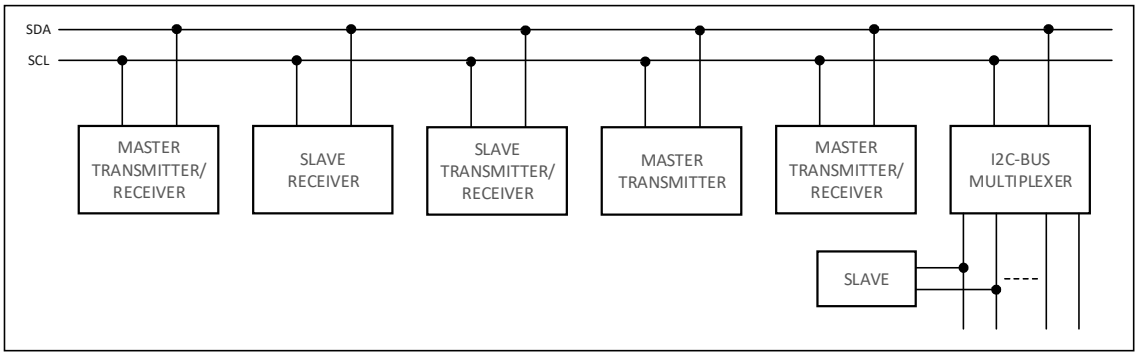


Figure 11. System Configuration

8.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The ACK bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra ACK-related clock pulse.

When a slave receiver which is addressed, it must generate an ACK after the reception of each byte. Similarly, the master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable LOW during the HIGH period of the ACK-related clock pulse (see Figure 12). Set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must leave the SDA data line HIGH to enable the master to generate a STOP condition.

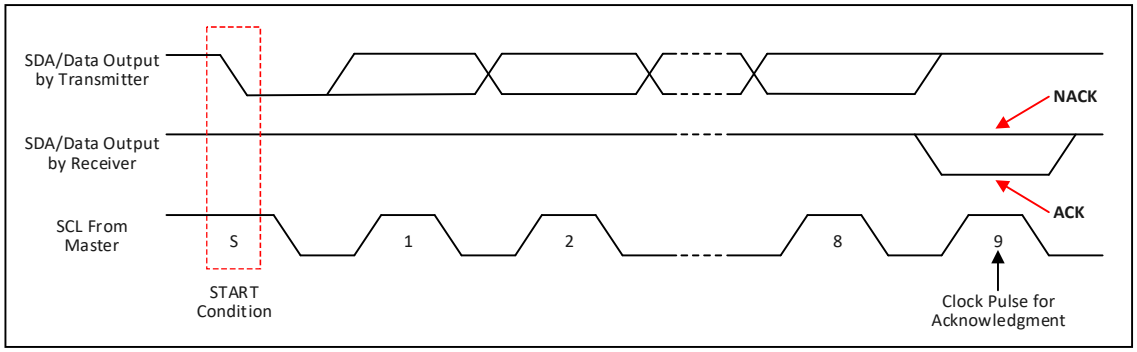


Figure 12. Acknowledgement on the I²C-bus

9. FUNCTIONAL DESCRIPTION

9.1. Device Address

Table 3 shows the address byte of the XL9535 and XL9555.

Table 3. XL9535 and XL9555 device address

Bit	7	6	5	4	3	2	1	0
Symbol	0	1	0	0	A2	A1	A0	R/$\overline{W}$
	Fixed bits				Programmable bits			read / write
	Slave Address							

The last bit (R/$\overline{W}$) of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Table 4. Address Reference

INPUTS			I²C-BUS SLAVE ADDRESS
A2	A1	A0	
0	0	0	32 (decimal), 0x20 (hexadecimal)
0	0	1	33 (decimal), 0x21 (hexadecimal)
0	1	0	34 (decimal), 0x22 (hexadecimal)
0	1	1	35 (decimal), 0x23 (hexadecimal)
1	0	0	36 (decimal), 0x24 (hexadecimal)
1	0	1	37 (decimal), 0x25 (hexadecimal)
1	1	0	38 (decimal), 0x26 (hexadecimal)
1	1	1	39 (decimal), 0x27 (hexadecimal)

The device features 3 hardware address pins (A0, A1, and A2) to allow the user to program the device's I²C address by pulling each pin to either V_{CC} or GND to signify the bit value in the address. This allows up to 8 devices to be on the same bus without address conflicts. The voltage on the pins must not change while the device is powered up in order to prevent possible I²C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V_{CC} or GND and cannot be left floating.

9.2. Register

9.2.1. Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the device (XL9535 or XL9555). Three bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion, or configuration) that will be affected. This register can be written or read through the I^2C-bus interface. The command byte is sent only during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

Table 5. Control Register Bits

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	B2	B1	B0

Table 6. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	XXXX XXXX
0	0	1	0x01	Input Port 1	Read byte	XXXX XXXX
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

9.2.2. Registers 0 and 1: Input port registers

The Input Port register (Registers 0 and 1) is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration registers (Registers 6 and 7). It only acts on read operation. Writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the the I^2C device that the Input Port register will be accessed next.

Table 7. Registers 0 (Input Port Register)

Bit	7	6	5	4	3	2	1	0
Symbol	**I0.7**	**I0.6**	**I0.5**	**I0.4**	**I0.3**	**I0.2**	**I0.1**	**I0.0**
Default	X	X	X	X	X	X	X	X

Table 8. Registers 1 (Input Port Register)

Bit	7	6	5	4	3	2	1	0
Symbol	**I1.7**	**I1.6**	**I1.5**	**I1.4**	**I1.3**	**I1.2**	**I1.1**	**I1.0**
Default	X	X	X	X	X	X	X	X

9.2.3. Registers 2 and 3: Output port registers

This Output Port register (Registers 2 and 3) is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Configuration registers (Registers 6 and 7). Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 9. Registers 2 (Output Port Register)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 10. Registers 3 (Output Port Register)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

9.2.4. Registers 4 and 5: Polarity Inversion registers

This Polarity Inversion register (Registers 4 and 5) allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 11. Registers 4 (Polarity Inversion Port 0 Register)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 12. Registers 5 (Polarity Inversion Port 1 Register)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

9.2.5. Registers 6 and 7: Configuration registers

This Configuration registers (Registers 6 and 7) configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the device's ports are inputs with a pull-up to V_{CC}. For XL9555 inside, note that there is a high value resistor tied to V_{CC} at each pin.

Table 13. Registers 6 (Configuration Port 0 Register)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 14. Registers 7 (Configuration Port 1 Register)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

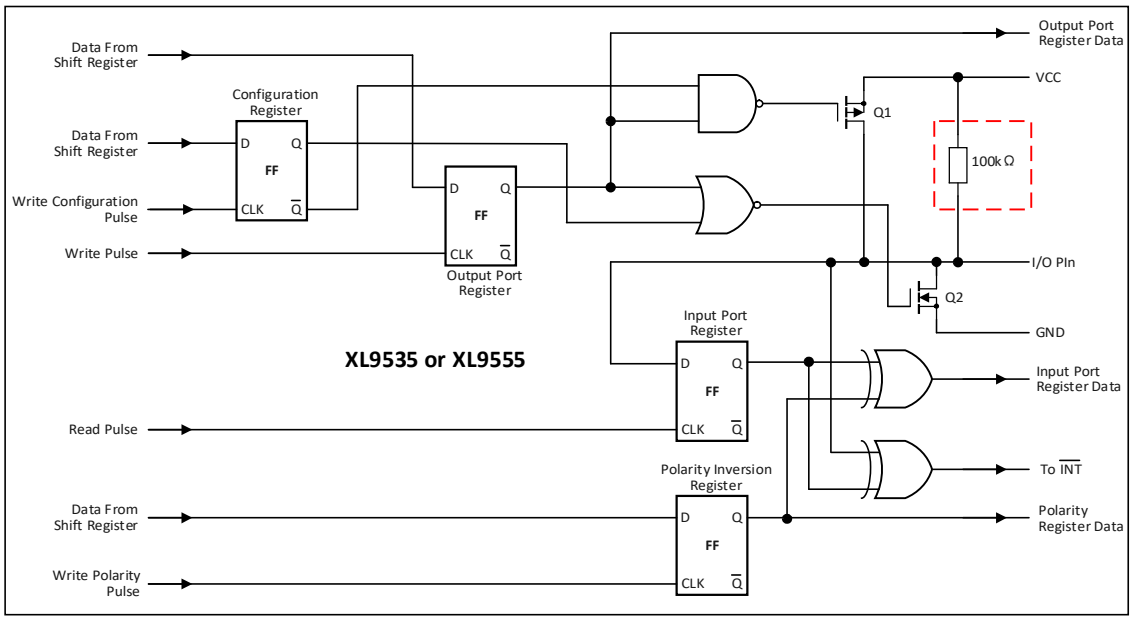
9.3. Power-on Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the device (XL9535 or XL9555) in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the device registers and I^2C/SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device. For a power-reset cycle, V_{CC} must be lowered below 0.2 V and then restored to the operating voltage.

9.4. I/O Port

When an I/O is configured as an input on device (XL9535), FETs Q1 and Q2 (see Figure 13) are off, which creates a high-impedance input. In the case of device (XL9555), FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, then on device (XL9535 or XL9555) either Q1 or Q2 is enabled (on), depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. Care should be exercised if an external voltage is applied to this I/O configured as an output should not exceed the recommended levels for proper operation.



REMARK: (1) At power-on reset, all registers return to default values.

(2) The portion of the schematic marked inside the red dotted line box is not in XL9535. Only for XL9555.

Figure 13. Simplified Schematic of Ports I/Os

9.5. Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time ($t_{iv(INT)}$) the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 14). Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by Port 0 is not cleared by a read of Port 1, or the other way around.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

9.6. Bus Transactions

Data is exchanged between the master and the device (XL9535 or XL9555) through write and read commands, and this is accomplished by reading from or writing to registers in the slave device. Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

9.6.1. Writing to the Port Registers

Data is transmitted to the device (XL9535 or XL9555) by sending the device address and setting the LSB bit to a logic 0 (R/$\overline{W}$=0) (see Table 3. “XL9535 and XL9555 device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the device (XL9535 or XL9555) are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 15 and Figure 16). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Figure 14 shows an example of writing a single byte to a slave register, write to the Polarity Inversion Register (0x04).

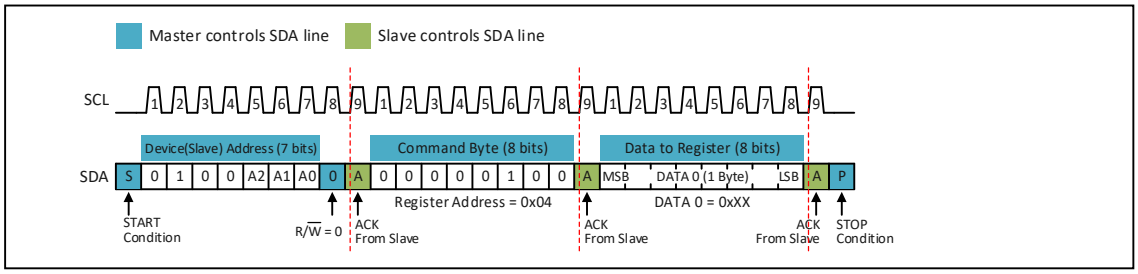


Figure 14. Write a single byte to Polarity Inversion Register

Figure 15 shows the Write to Output Port Registers (0x02 and 0x03).

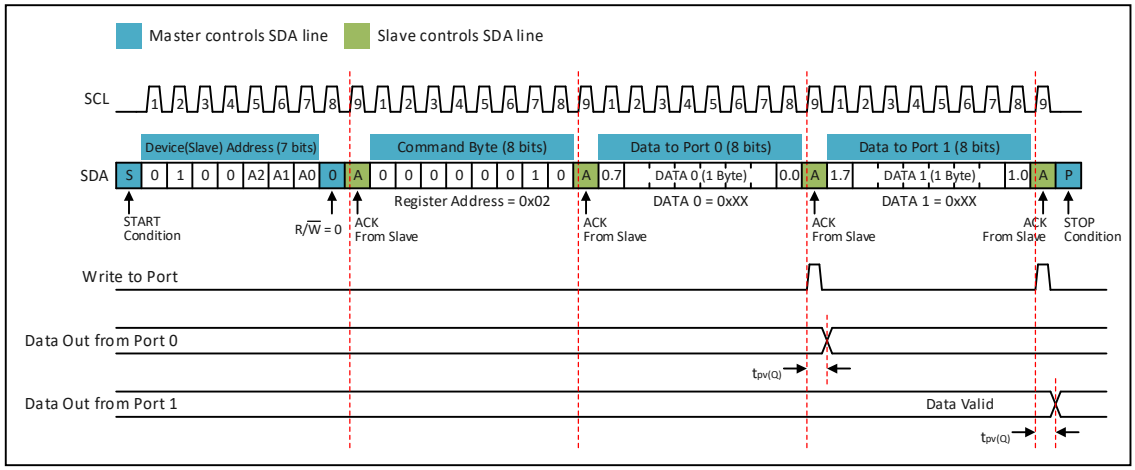


Figure 15. Write to Output Port Registers

Figure 16 shows the Write to the Configuration Register (0x06 and 0x07).

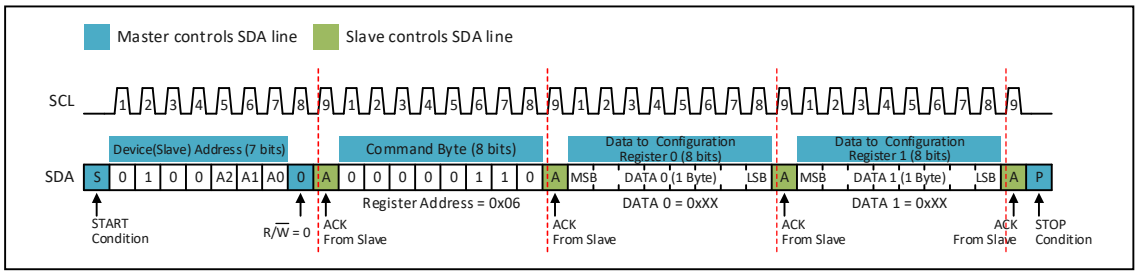


Figure 16. Write to Configuration Registers

9.6.2. Reading the Port Registers

In order to read data from the device (XL9535 or XL9555), the bus master must first send the device address with the LSB bit set to a logic 0 (R/$\overline{W}$=0) (see Table 3. “XL9535 and XL9555 device address”). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the LSB bit is set to a logic 1 (R/$\overline{W}$=1). Data from the register defined by the command byte will then be sent by the device (see Figure 17, 18, 19 and Figure 20). After the first byte is read, additional bytes may be read, but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. Data is clocked into the register on the falling edge of the

acknowledge clock pulse. There is no limitation on the number of data bytes received in one read transmission, but the final byte received, the bus master must not acknowledge the data.

Figure 17 shows an example of reading a single byte from a slave register.

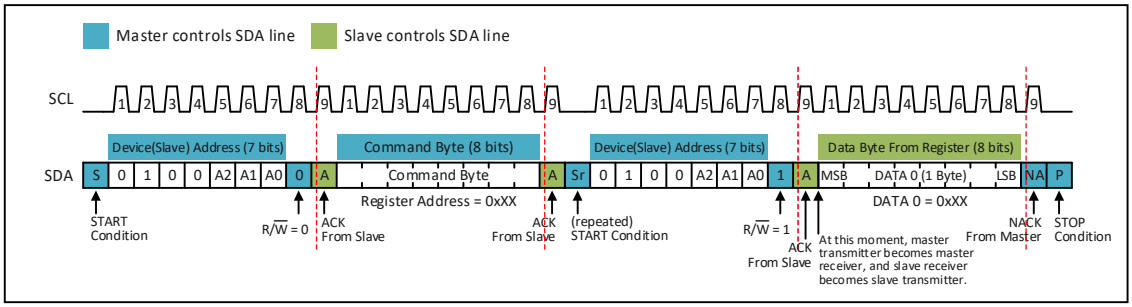
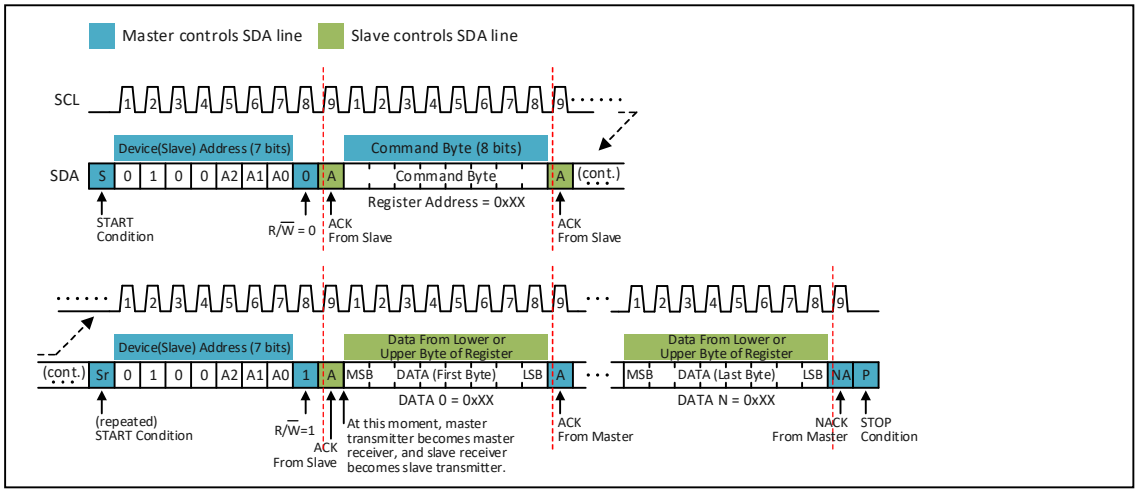
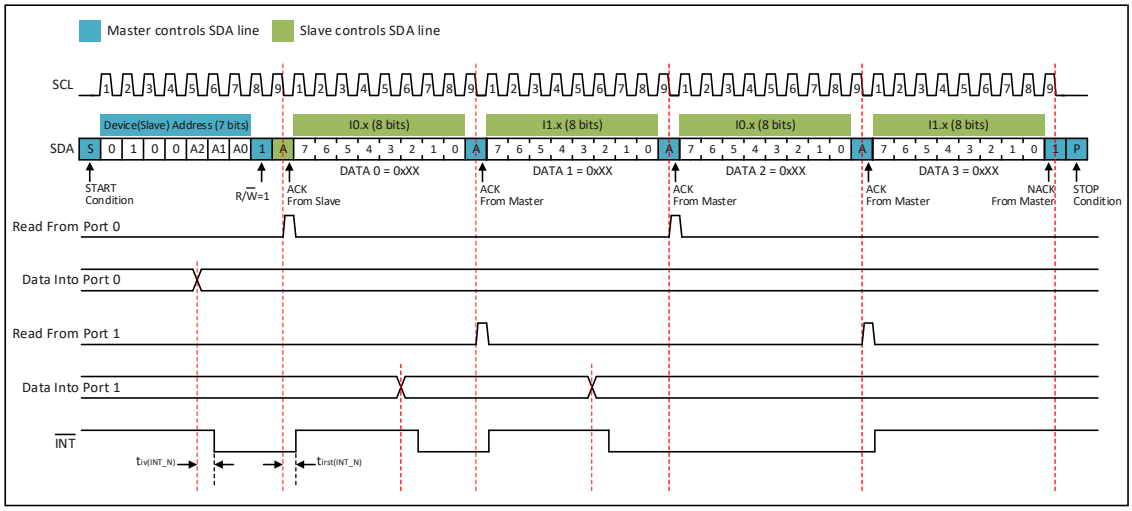


Figure 17. Read a single byte from Register



REMARK: Transfer can be stopped at any time by a STOP condition.

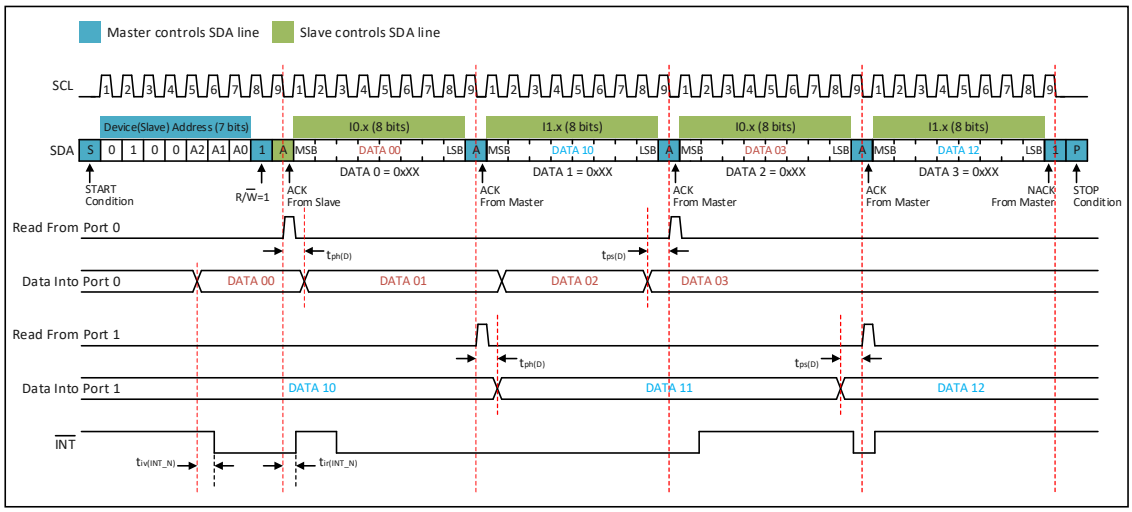
Figure 18. Read bytes from Register



REMARK: (1) Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

(2) This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 18 for these details).

Figure 19. Read Input Port Register, Scenario 1



REMARK: (1) Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

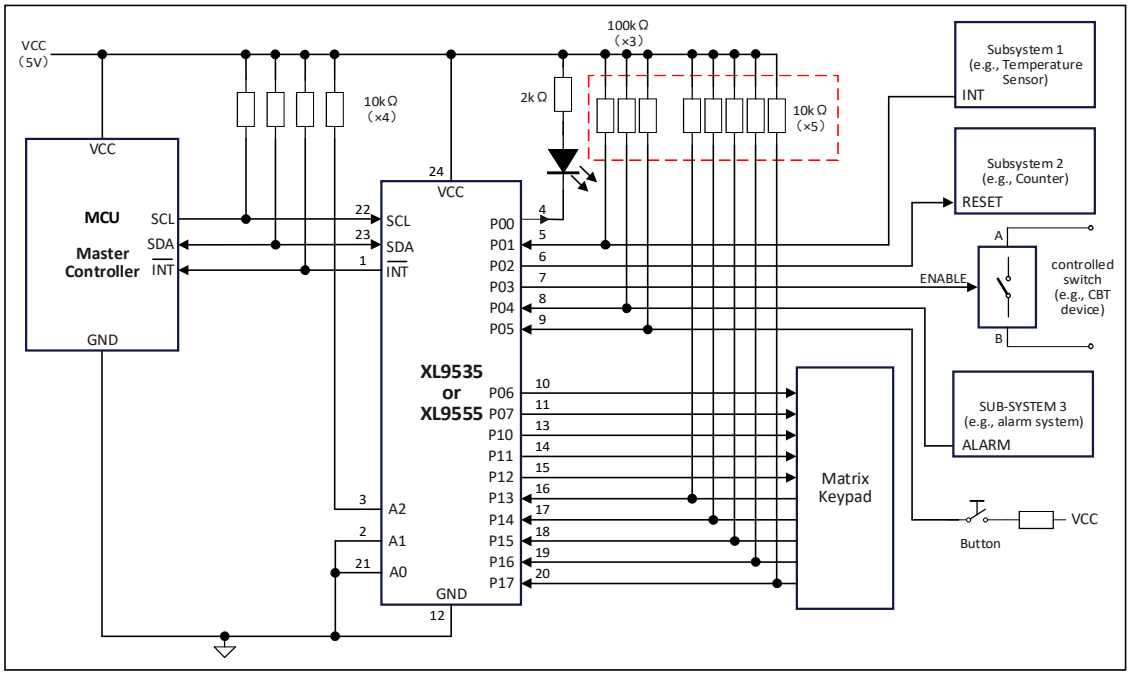
(2) This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 18 for these details).

Figure 20. Read Input Port Register, Scenario 2

10. APPLICATION INFORMATION

10.1. Typical Application

Figure 21 shows an application in which the device (XL9535 or XL9555) can be used.



REMARK: (1) Device address is configured as 0100 100xb for this example.

(2) P00, P02-P03, and P10-P12 are configured as outputs.

(3) P01, P04–P05, and P13–P17 are configured as inputs.

(4) Pin numbers shown are for SOP24/SSOP24/TSSOP24 packages.

Figure 21. Typical Application

10.2. Minimizing I_{CC} when the I/Os are used to control LEDs

When the device I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 22. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how the supply current (I_{CC}) increases as V_{IN} becomes lower than V_{CC}. Designs needing to minimize current consumption, such as for battery-powered applications, should consider maintaining the voltage of I/O pins greater than or equal to V_{CC} when the LED is off.

Figure 22 shows a high-value resistor in parallel with the LED. Figure 23 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

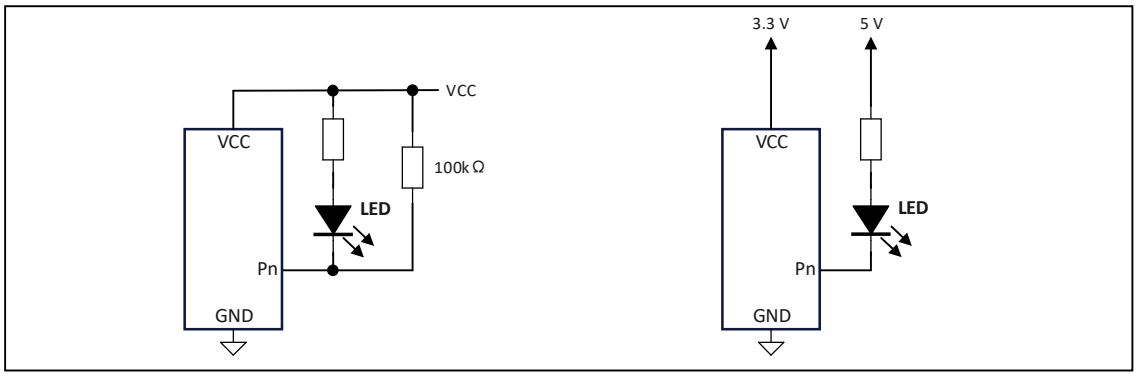


Figure 22. High-Value Resistor In Parallel With the LED

Figure 23. Device Supplied By a Lower Voltage

11. ESD AND HANDLING INFORMATION

This IC can be damaged by Electrostatic Discharge (ESD). It recommends that all ICs be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision ICs may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

These devices have limited built-in ESD protection. All input and output pins are protected against ESD under normal handling. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

12. ABBREVIATIONS

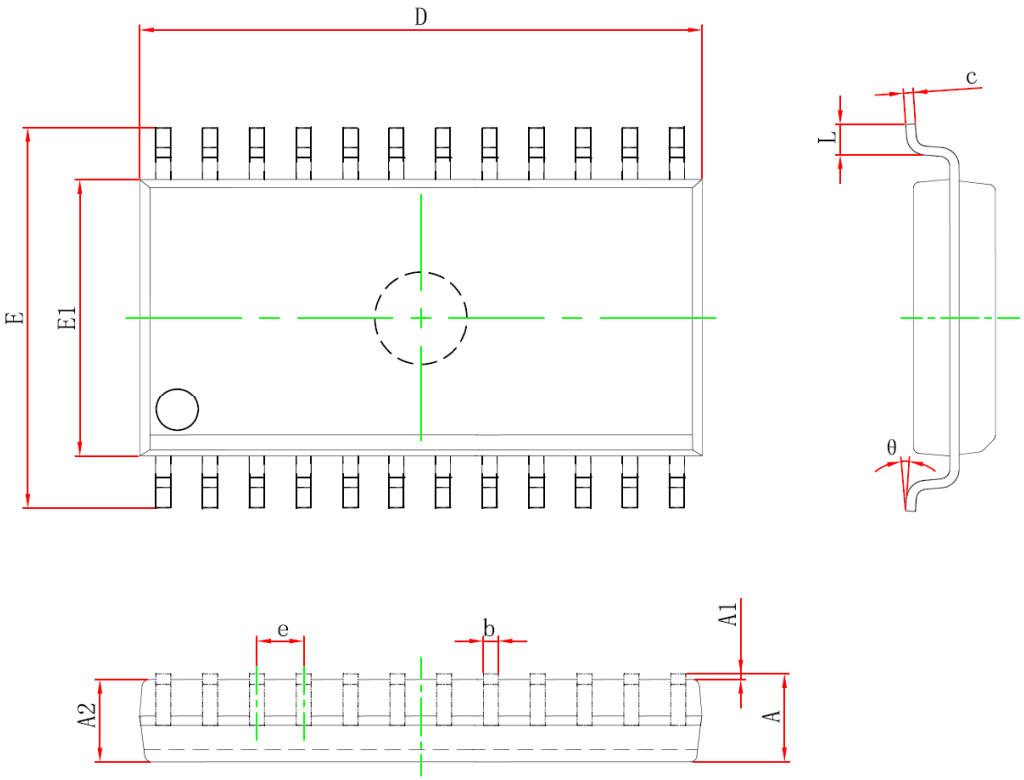
Table 15. Abbreviations

ACRONYM	DESCRIPTION
ACPI	Advanced Configuration and Power Interface
CMOS	Complementary Metal Oxide Semiconductor
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
IC	Integrated Circuit
I/O	Input/Output
I^2C-bus	Inter-Integrated Circuit bus
SMBus	System Management Bus
ESD	Electrostatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charged Device Model
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
MCU	Microcontroller Unit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board

13. PACKAGE INFORMATION

13.1. SOP24(300mil) Package outline dimensions

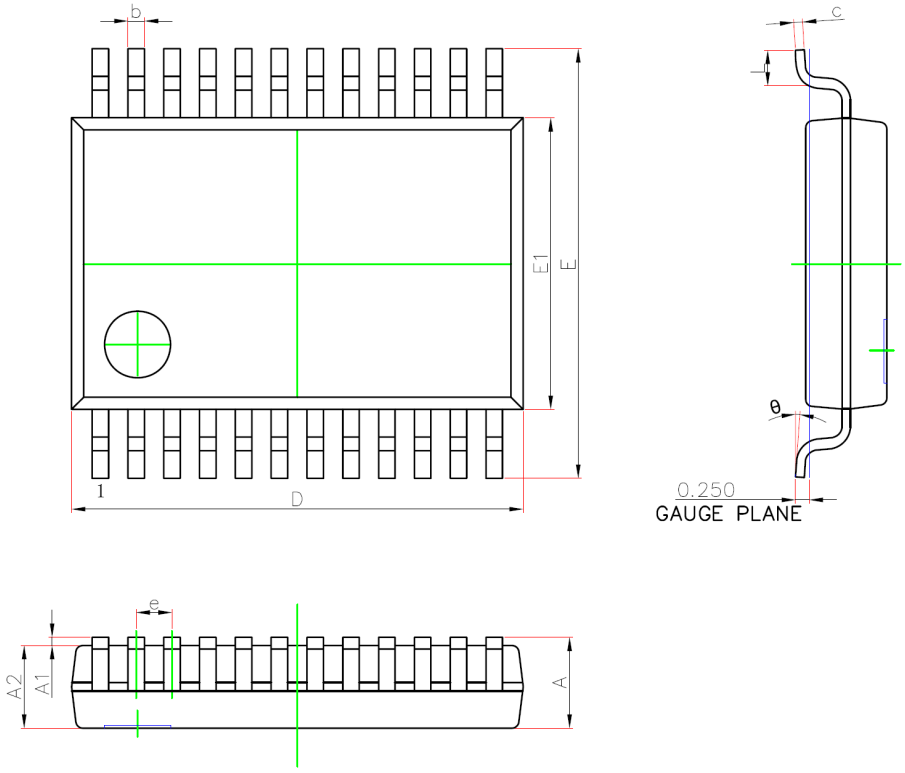
SOP24(300mil): plastic small outline package; 24 leads; Wide body. body width 7.5 mm/300mil.



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	—		2.650	—		0.104
A1	0.100		0.300	0.004		0.012
A2	2.100		—	0.083		—
b	0.330		0.510	0.013		0.020
c	0.204		0.330	0.008		0.013
D	15.200		15.600	0.598		0.614
e	1.270 (BSC)			0.050 (BSC)		
E	10.210		10.610	0.402		0.418
E1	7.400	7.500	7.600	0.291	0.300	0.299
L	0.400		1.270	0.016		0.500
θ	0°		8°	0°		8°

13.2. SSOP24(209mil) Package outline dimensions

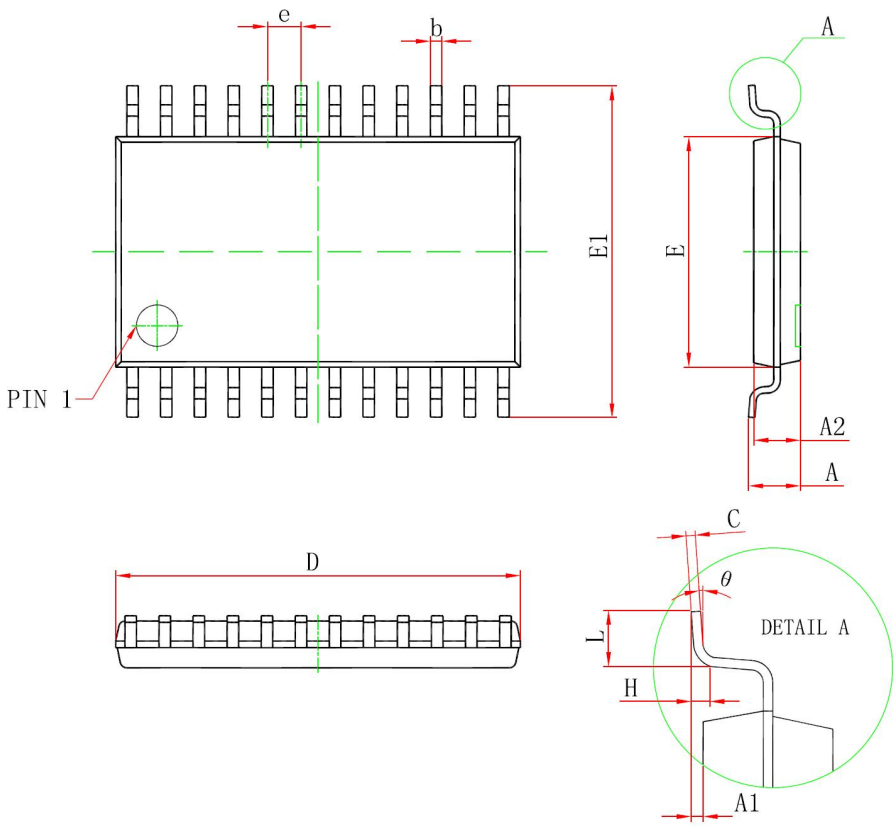
SSOP24(209mil): plastic shrink small outline package; 24 leads; body width 5.3 mm/209mil.



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	—		1.850	—		0.073
A1	0.050		—	0.002		—
A2	1.400		1.600	0.055		0.063
b	0.220		0.380	0.009		0.015
c	0.090		0.250	0.004		0.010
D	7.900		8.500	0.311		0.335
e	0.650 (BSC)			0.026 (BSC)		
E	7.400		8.200	0.291		0.323
E1	5.000	5.300	5.600	0.197	0.209	0.220
L	0.550		0.950	0.022		0.037
θ	0°		8°	0°		8°

13.3. TSSOP24 Package outline dimensions

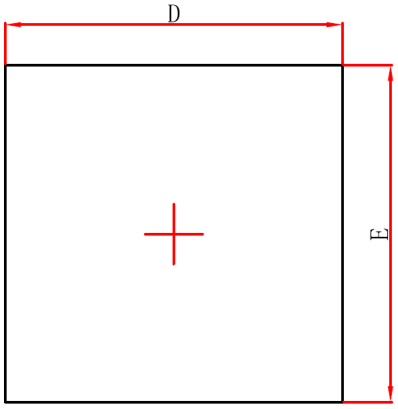
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm



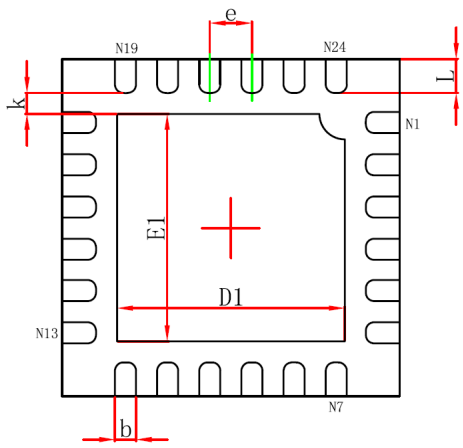
SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	—		1.200	—		0.047
A1	0.050		0.150	0.002		0.006
A2	0.800		1.000	0.031		0.039
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D	7.700	7.800	7.900	0.303	0.307	0.311
e	0.650 (BSC)			0.026 (BSC)		
E	4.300	4.400	4.500	0.169	0.173	0.177
E1	6.250	6.400	6.550	0.246	0.252	0.258
H	0.250 (TYP)			0.010 (TYP)		
L	0.500		0.700	0.020		0.028
θ	1°		7°	1°		7°

13.4. QFN24-4×4 Package outline dimensions

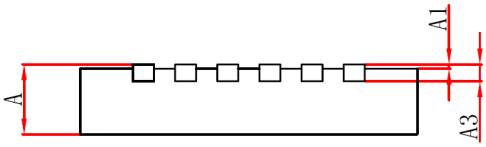
QFN24-4×4: plastic thermal enhanced very thin quad flat package; no leads; body size 4×4 mm



Top View



Bottom View



Side View

SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000		0.050	0.000		0.002
A3	0.203 (REF)			0.008 (REF)		
b	0.200		0.300	0.008		0.012
D	3.924	4.000	4.076	0.154	0.157	0.160
E	3.924	4.000	4.076	0.154	0.157	0.160
e	0.500 (BSC)			0.020 (BSC)		
D1	2.600	2.700	2.800	0.102	0.106	0.110
E1	2.600	2.700	2.800	0.102	0.106	0.110
L	0.324		0.476	0.013		0.019
k	0.200 (MIN)			0.008 (MIN)		